PMP40071 Test Results

1 General

1.1 Purpose

This test report is to provide the detailed data for evaluating and verifying the PMP40071 which employs two Buck Controllers ---- TPS56C215 for dual-channel output. The PMP40071 reference design is designed for the telecom application with a DC input of 8.3V~14V achieving the lowest component count. The output voltage could be modified by resistors over the resistor divider from 0.6V to 3.63V. The maximum output current each channel can achieve 10A.

1.2 Reference Documentation

Schematic: PMP40071_Sch.pdf

Gerber: PMP40071_GerberNCdrills.zip

Layer Plot: PMP40071_PCBlayers.pdf

Assembly Drawing: PMP40071_Assy.pdf

CAD File: PMP40071_CAD.zip

BOM: PMP40071_BOM.pdf

1.3 Test Equipment

Multi-meter (current): Fluke 287C

Multi-meter (voltage): Fluke 287C

DC Source: Chroma 62006P-100-25

E-Load: Chroma 63105A module

Oscilloscope: Tektronix DPO3054

Electrical Thermography: Fluke Ti9

2 Performance Data and Waveform

2.1 Efficiency

2.1.1 Input voltage: 8.3V

V_{in}(V)	I_{in}(A)	V_o1(V)	I_o1(A)	V_o2(V)	I_o2(A)	Efficiency
8.295	0.327	1.199	0.986	1.199	1	87.79%
8.291	0.636	1.199	1.991	1.199	2.003	90.82%
8.287	0.943	1.199	2.994	1.199	3.01	92.12%
8.282	1.251	1.199	3.985	1.199	3.998	92.38%
8.278	1.57	1.199	4.988	1.199	5.003	92.17%
8.273	1.894	1.199	5.992	1.199	6.008	91.82%
8.268	2.219	1.198	6.982	1.199	6.998	91.32%
8.263	2.557	1.198	7.987	1.199	8.003	90.70%
8.257	2.901	1.198	8.991	1.199	9.009	90.06%
8.252	3.248	1.198	9.98	1.199	9.996	89.32%

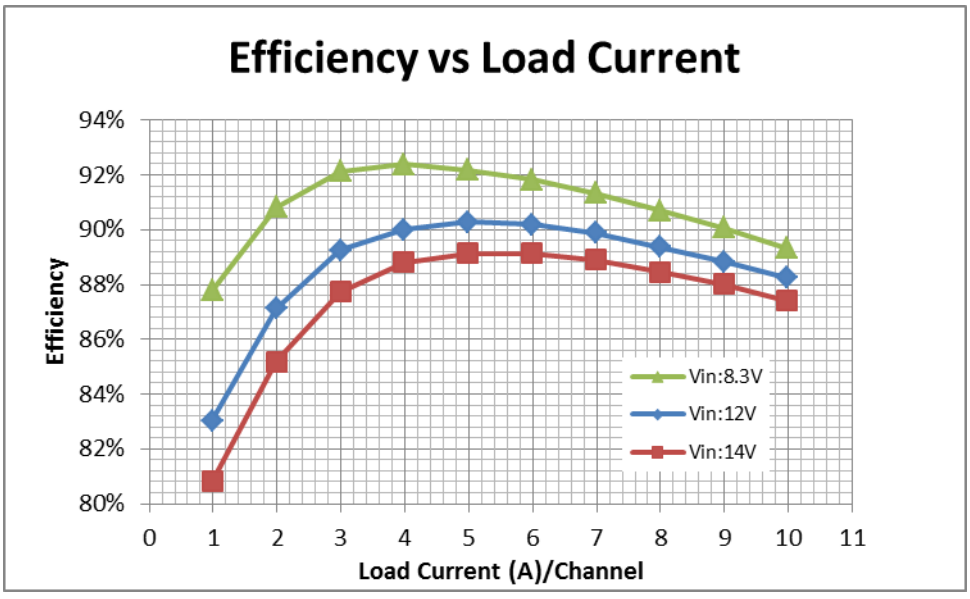
2.1.2 Input voltage: 12V

V_{in}(V)	I_{in}(A)	V_o1(V)	I_o1(A)	V_o2(V)	I_o2(A)	Efficiency
12	0.239	1.199	0.986	1.198	1.001	83.03%
11.998	0.458	1.199	1.991	1.198	2.004	87.13%
11.996	0.672	1.199	2.995	1.198	3.008	89.25%
11.994	0.886	1.199	3.984	1.198	3.997	90.01%
11.992	1.106	1.199	4.988	1.198	5.002	90.27%
11.989	1.33	1.199	5.993	1.198	6.007	90.20%
11.987	1.555	1.199	6.983	1.198	6.998	89.89%
11.985	1.788	1.198	7.987	1.197	8.004	89.36%
11.983	2.025	1.198	8.991	1.197	9.008	88.82%

11.98	2.263	1.198	9.98	1.197	9.996	88.24%

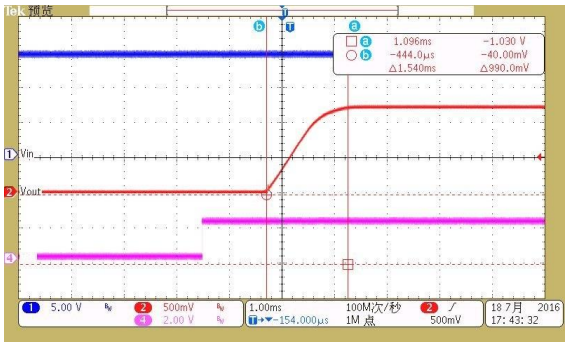
2.1.3 Input voltage: 14V

V_{in}(V)	I_{in}(A)	V_o1(V)	I_o1(A)	V_o2(V)	I_o2(A)	Efficiency
14.001	0.21	1.198	0.986	1.197	0.998	80.80%
13.999	0.401	1.198	1.991	1.197	2.002	85.18%
13.998	0.585	1.198	2.994	1.196	3.008	87.73%
13.997	0.769	1.198	3.984	1.197	3.999	88.81%
13.996	0.959	1.198	4.988	1.197	5.004	89.15%
13.994	1.152	1.198	5.992	1.197	6.009	89.15%
13.992	1.346	1.198	6.982	1.197	6.998	88.89%
13.991	1.547	1.198	7.987	1.197	8.003	88.47%
13.989	1.751	1.198	8.991	1.197	9.01	88.00%
13.987	1.956	1.197	9.98	1.197	9.998	87.41%

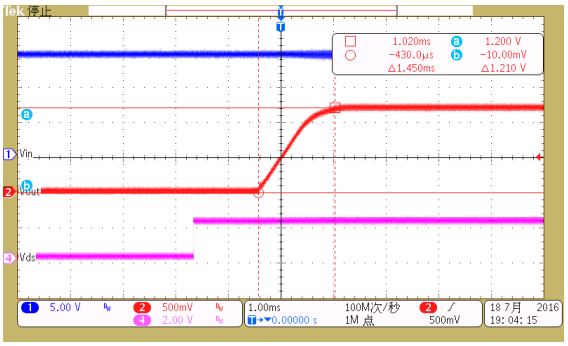


2.2 Start up and shut down

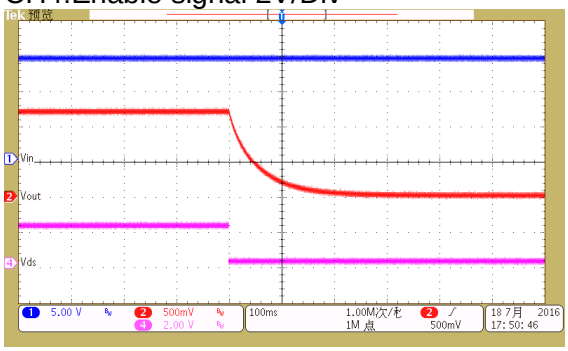
2.2.1 $14V_{in}$&$1.2V_o$



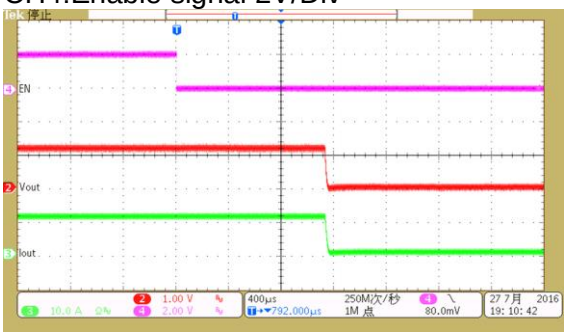
No load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div



Full load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div

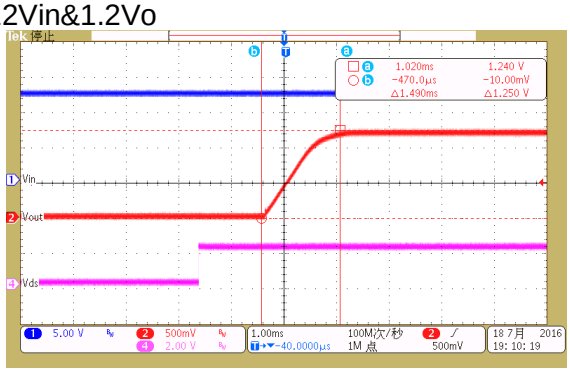


No load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div

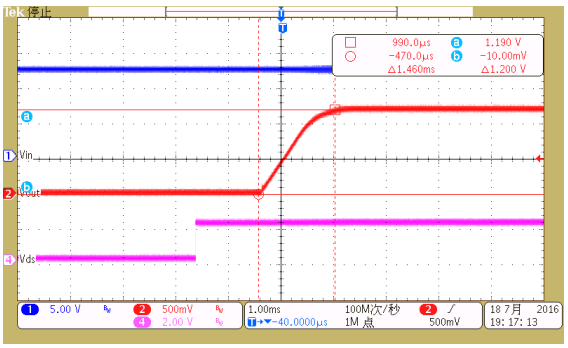


Full load
CH2: Output voltage 1V/Div
CH3: Load Current 10A/Div
CH4:Enable signal 2V/Div

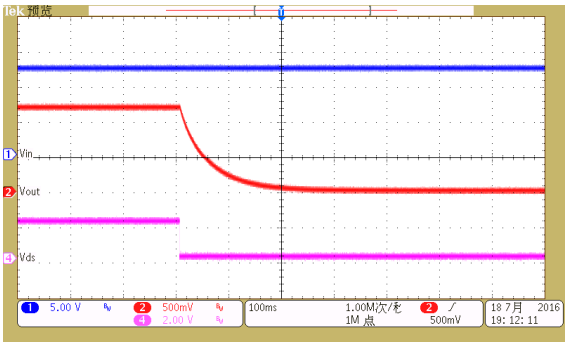
2.2.2 12Vin&1.2Vo



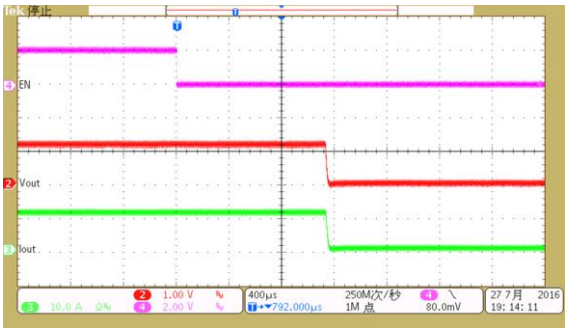
No load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div



Full load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div

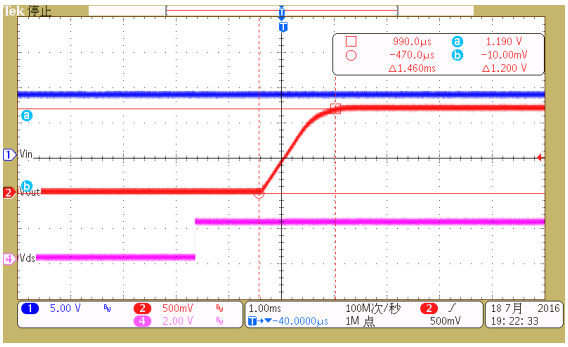


No load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div

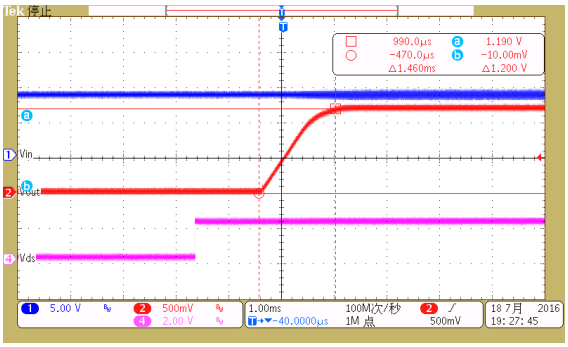


Full load
CH2: Output voltage 1V/Div
CH3: Load Current 10A/Div
CH4:Enable signal 2V/Div

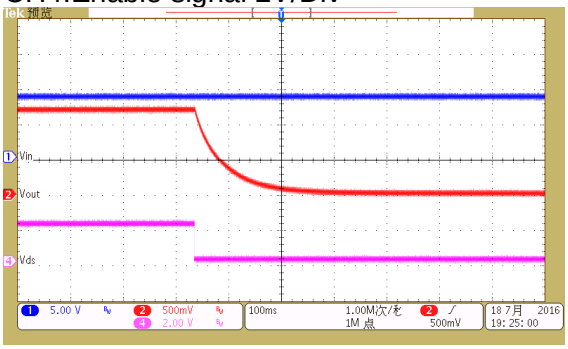
2.2.3 8.3Vin&1.2Vo



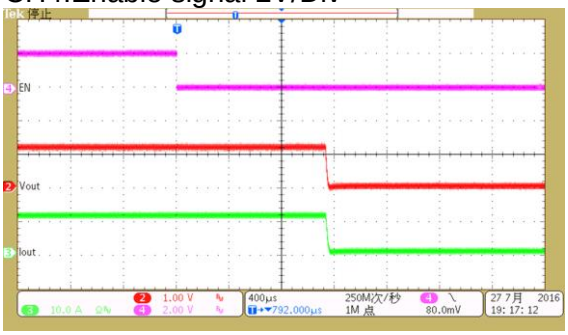
No load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div



Full load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div



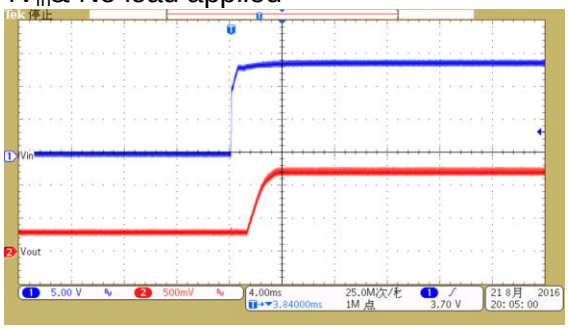
No load
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div
CH4:Enable signal 2V/Div



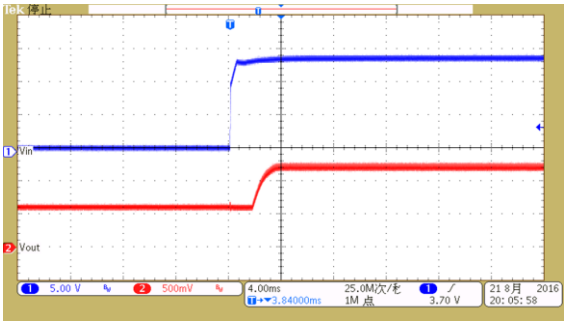
Full load
CH2: Output voltage 1V/Div
CH3: Load Current 10A/Div
CH4:Enable signal 2V/Div

2.3 Pre-bias Start up

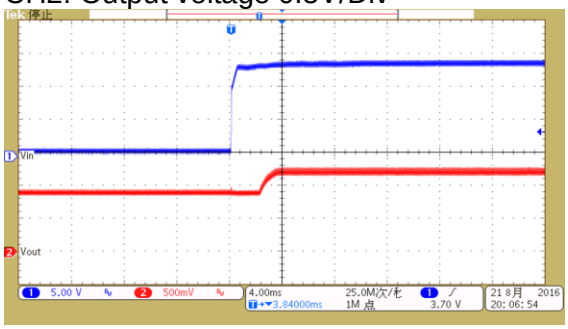
2.3.1 14V_{in}& No load applied



Residual Voltage: 25% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div

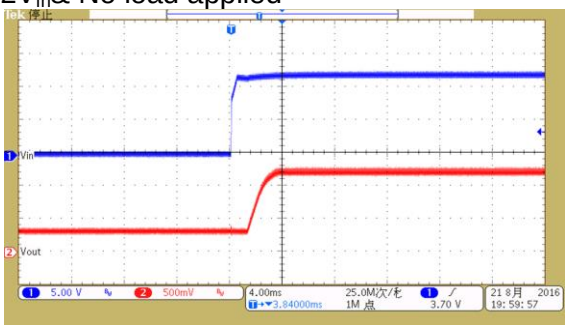


Residual Voltage: 50% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div

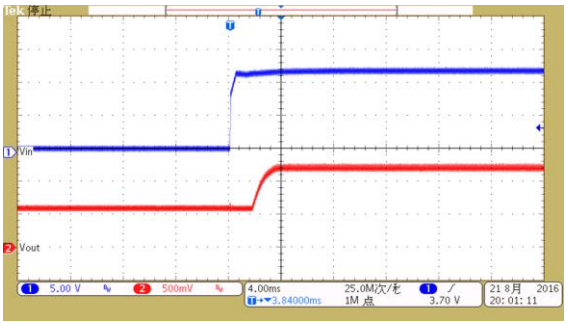


Residual Voltage: 75% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div

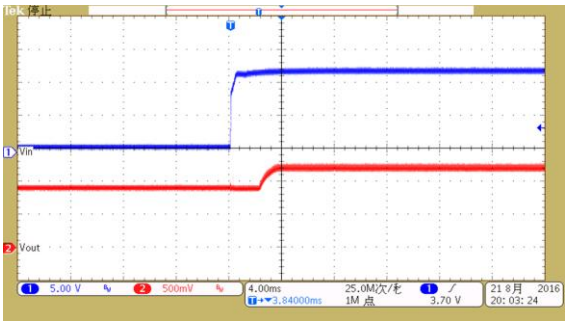
2.3.2 12V_{in}& No load applied



Residual Voltage: 25% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div

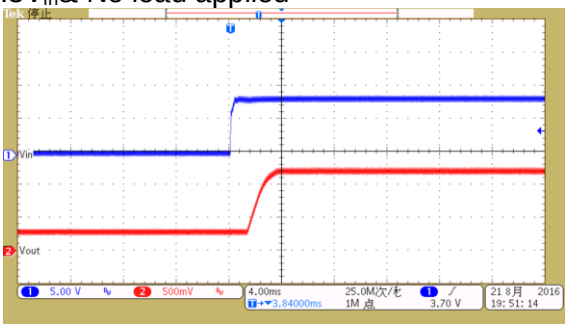


Residual Voltage: 50% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div

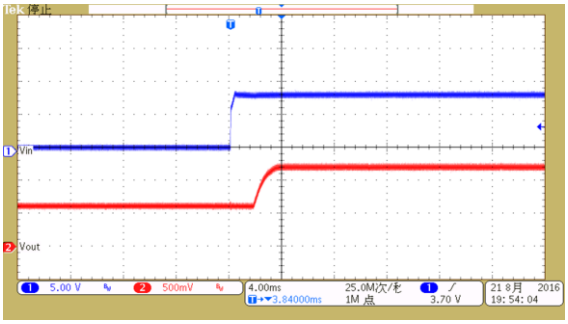


Residual Voltage: 75% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div

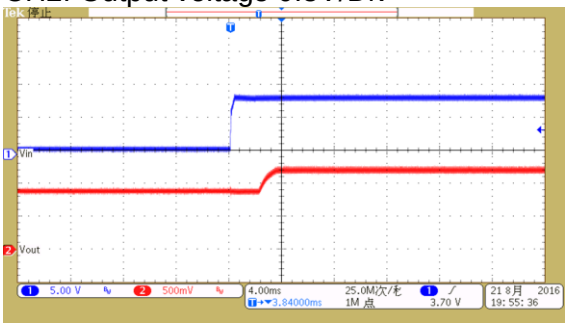
2.3.3 8.3V_{in}& No load applied



Residual Voltage: 25% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div



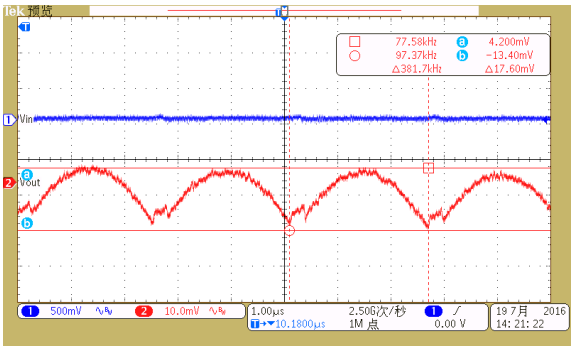
Residual Voltage: 50% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div



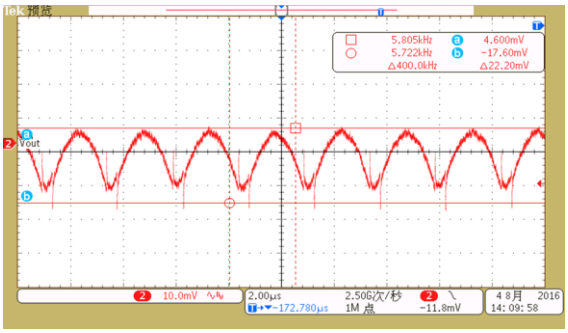
Residual Voltage: 75% Vo
CH1: Input voltage 5V/Div
CH2: Output voltage 0.5V/Div

2.4 Output Voltage Ripple

2.4.1 Input Voltage: 8.3V, Output Voltage: 1.2V

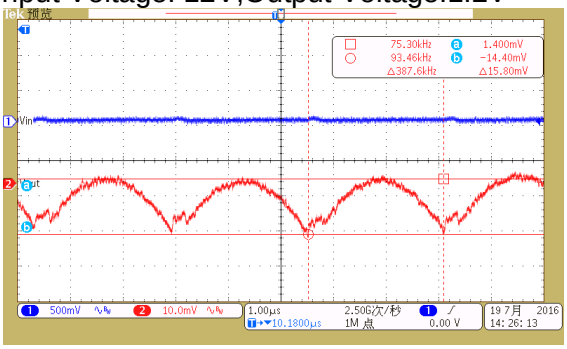


No Load
CH2: Output voltage 10mV/Div

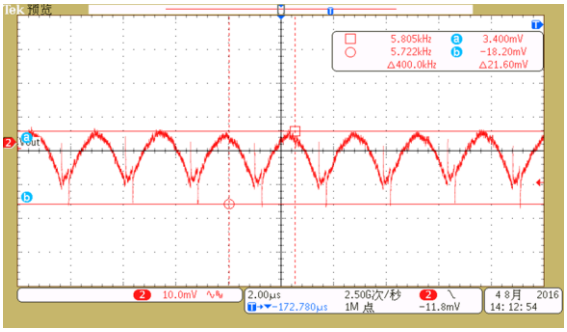


Full Load
CH2: Output voltage 10mV/Div

2.4.2 Input Voltage: 12V,Output Voltage:1.2V

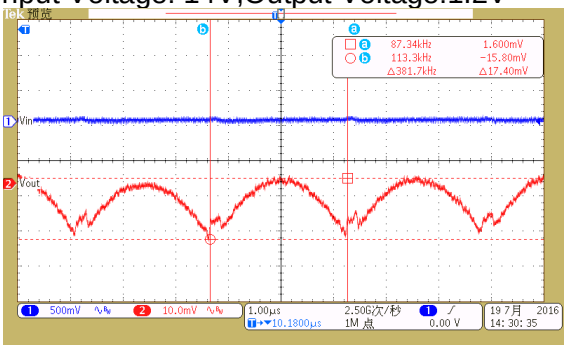


No Load
CH2: Output voltage 10mV/Div

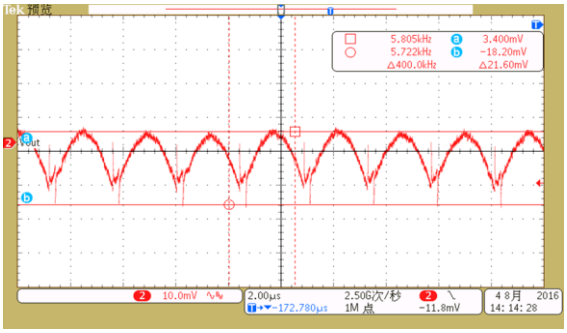


Full Load
CH2: Output voltage 10mV/Div

2.4.3 Input Voltage: 14V,Output Voltage:1.2V



No Load
CH2: Output voltage 10mV/Div

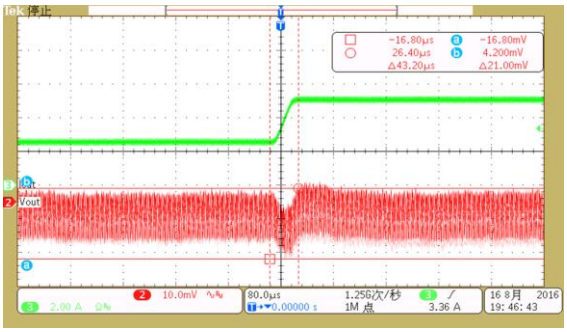


Full Load
CH2: Output voltage 10mV/Div

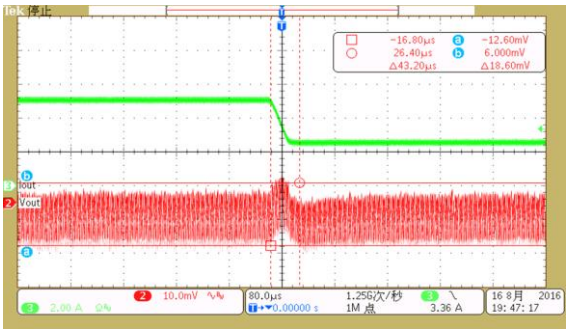
2.5 Dynamic Performance

2.5.1 Input Voltage: 8.3V, Output Voltage: 1.2V

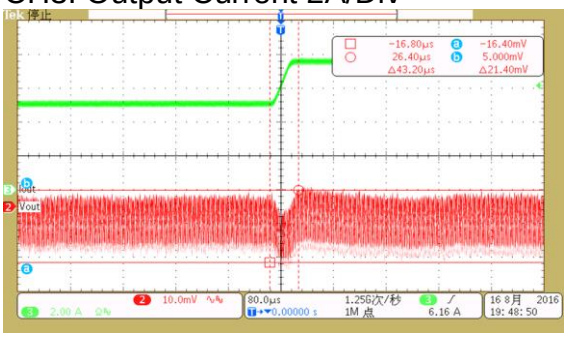
Load Step @100mA/us



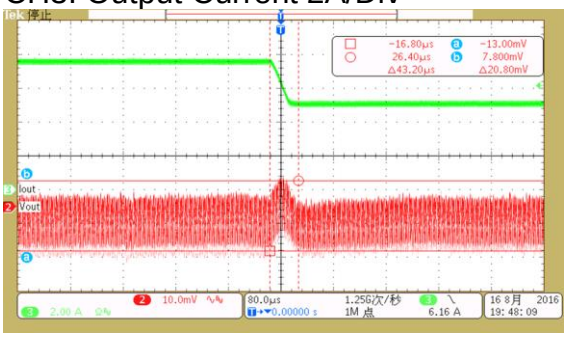
Load switching from 25% to 50% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



Load switching from 50% to 25% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



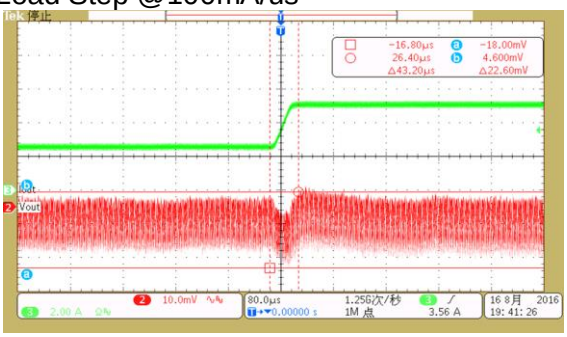
Load switching from 50% to 75% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



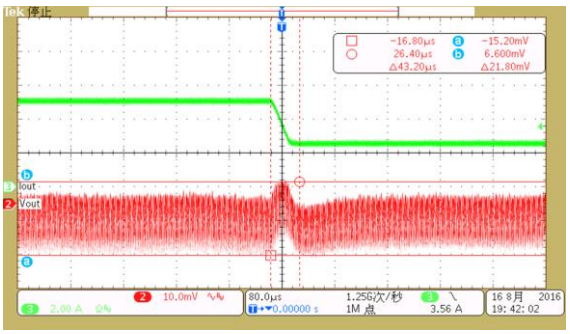
Load switching from 75% to 50% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div

2.5.2 Input Voltage: 12V, Output Voltage: 1.2V

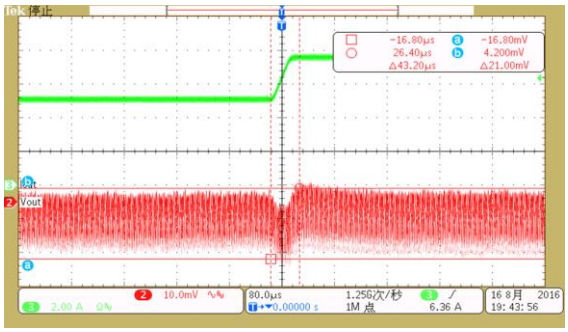
Load Step @100mA/us



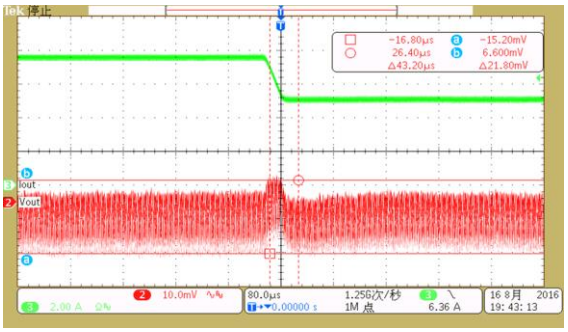
Load switching from 25% to 50% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



Load switching from 50% to 25% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



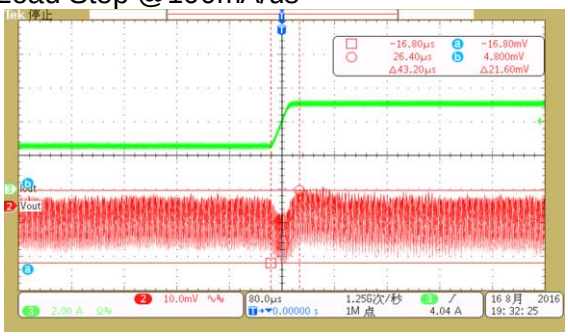
Load switching from 50% to 75% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



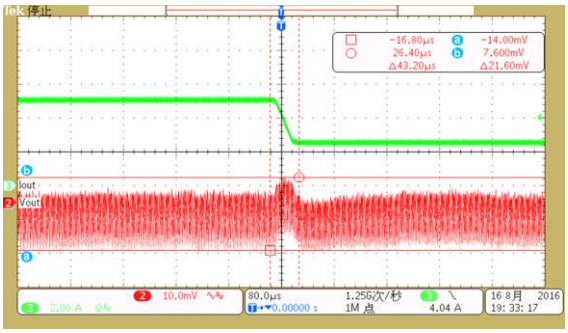
Load switching from 75% to 50% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div

2.5.3 Input Voltage: 14V, Output Voltage: 1.2V

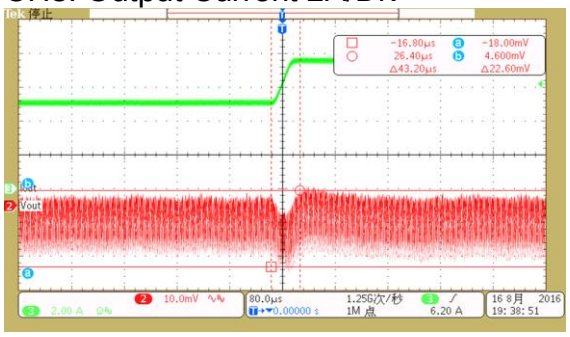
Load Step @100mA/us



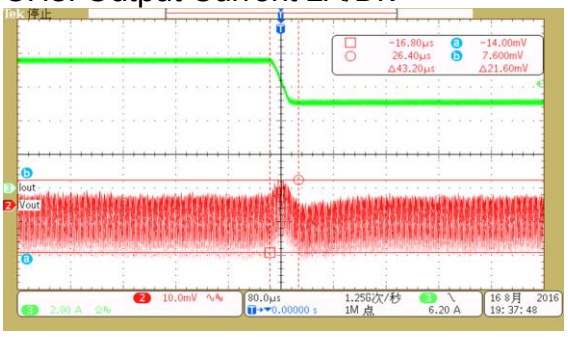
Load switching from 25% to 50% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



Load switching from 50% to 25% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



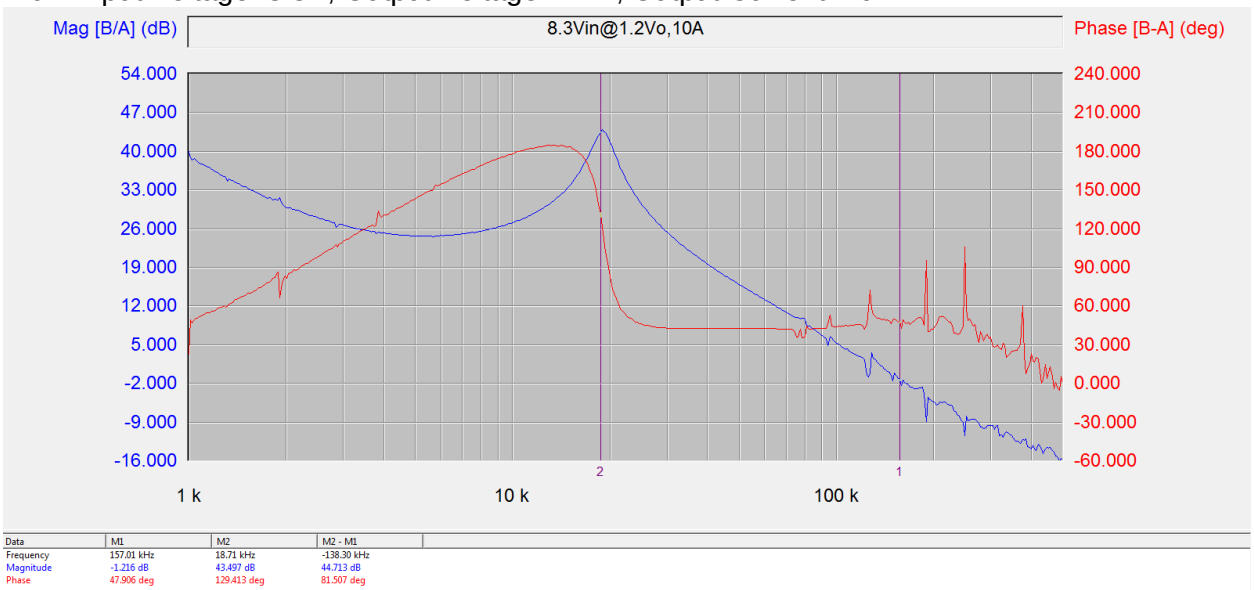
Load switching from 50% to 75% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div



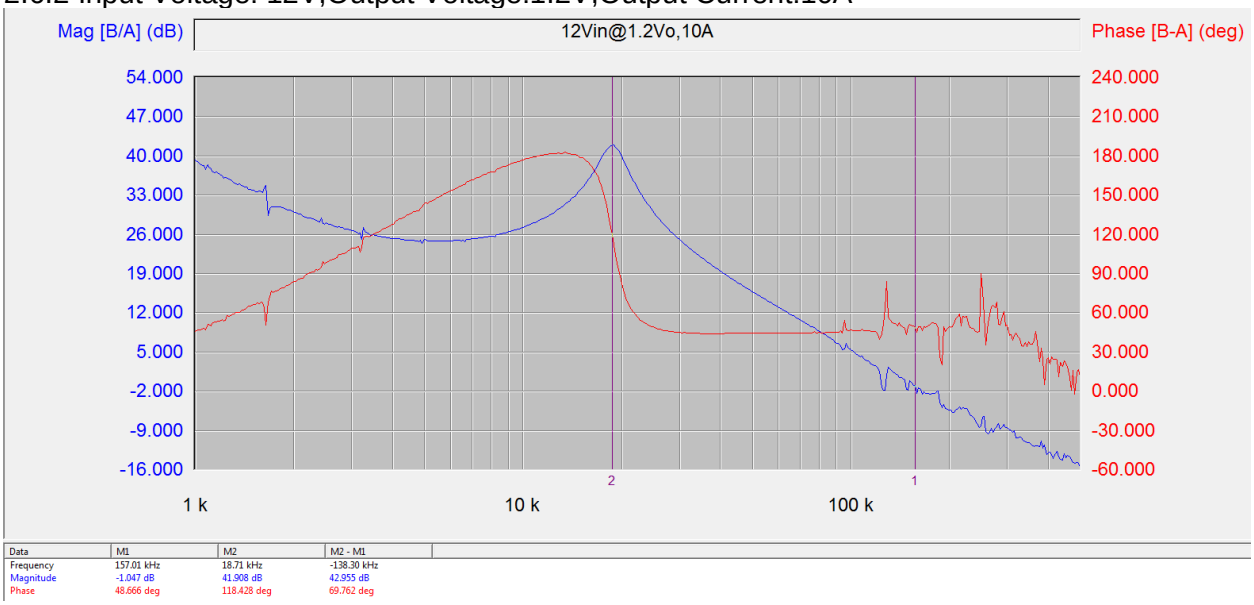
Load switching from 75% to 50% Load
CH2: Output Voltage 10mV/Div
CH3: Output Current 2A/Div

2.6 Bode Plot

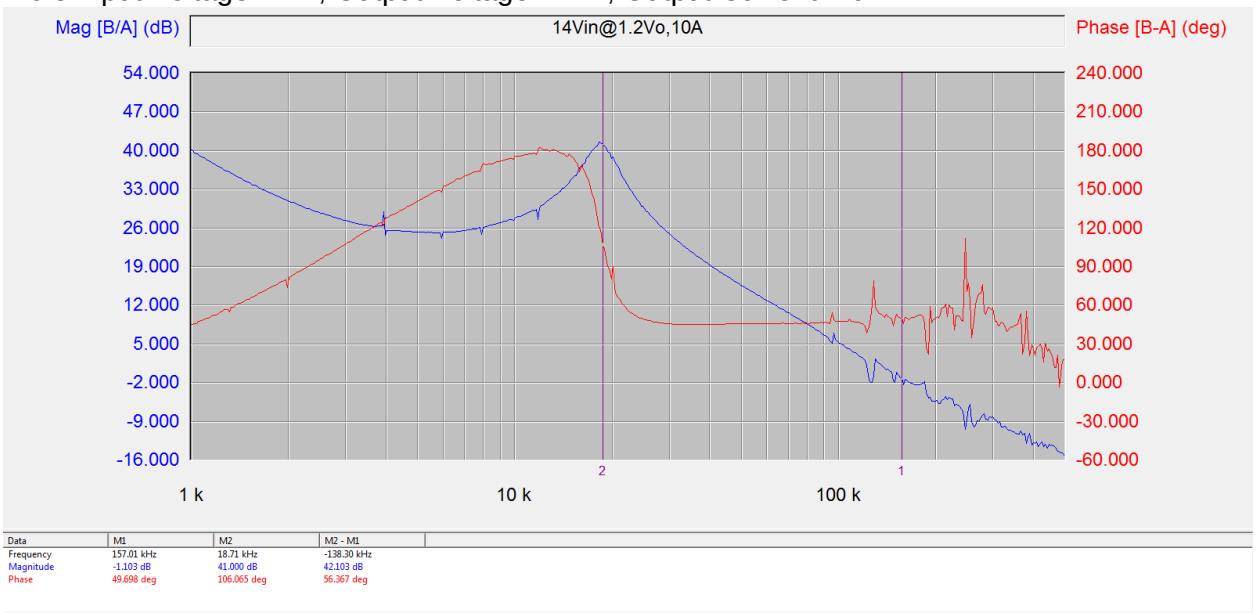
2.6.1 Input Voltage: 8.3V, Output Voltage: 1.2V, Output Current: 10A



2.6.2 Input Voltage: 12V,Output Voltage:1.2V,Output Current:10A

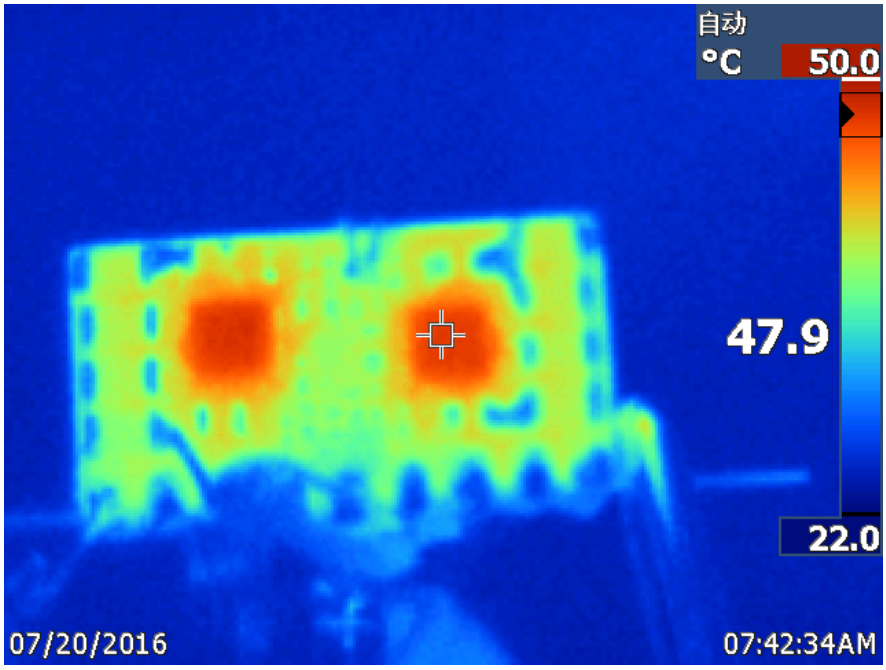


2.6.3 Input Voltage: 14V, Output Voltage: 1.2V, Output Current: 10A

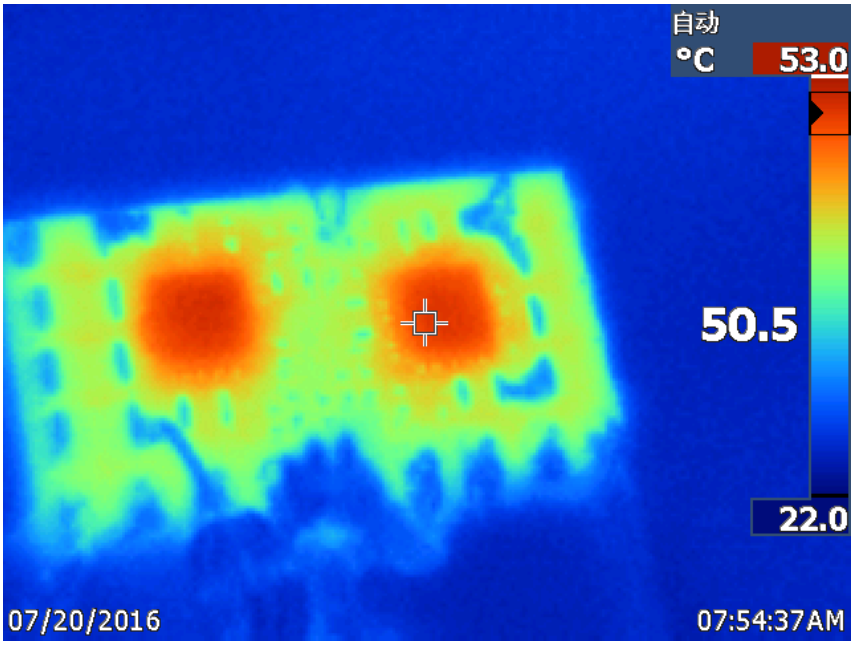


2.7 Thermal Performance

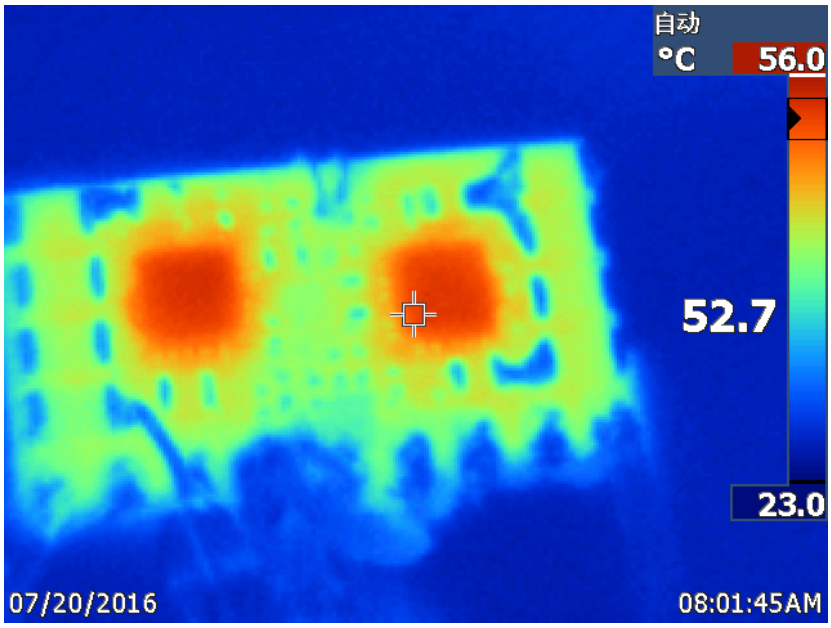
The board is powered up by 8.3V DC voltage and output 1.2V/10A load to each output port. Run about 10min for warming up, with a fan 2m/s.



The board is powered up by 12V DC voltage and output 1.2V/10A load to each output port. Run about 10min for warming up, with a fan 2m/s.



The board is powered up by 14V DC voltage and output 1.2V/10A load to each output port. Run about 10min for warming up, with a fan 2m/s.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265