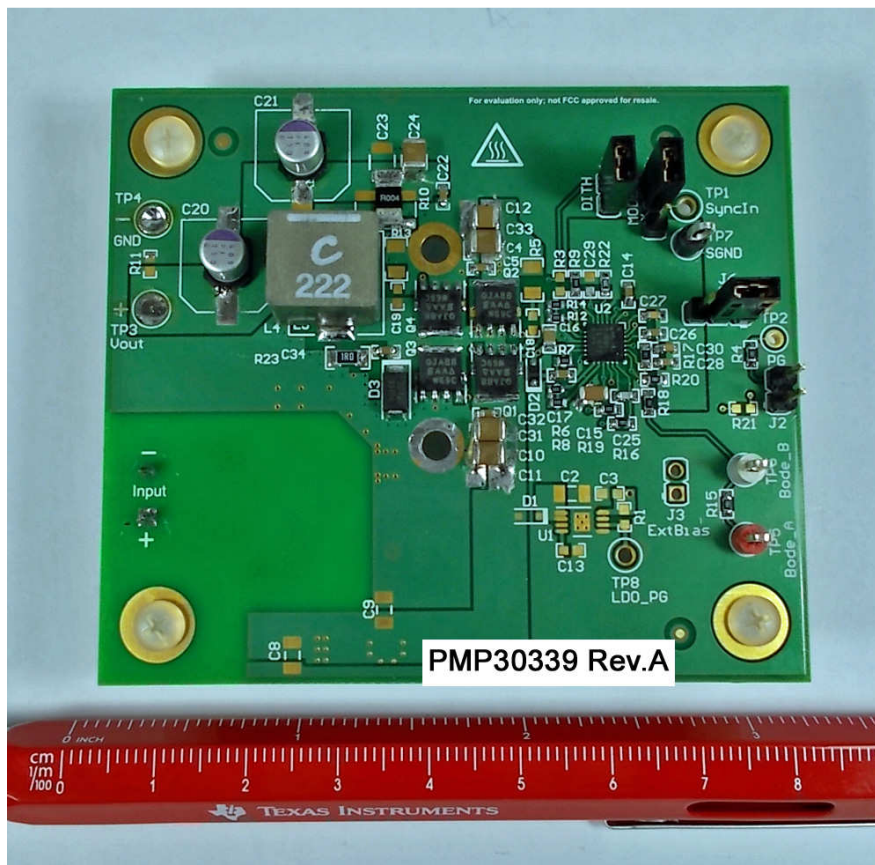


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Automotive Synchronous Buck

- Input 9.0 .. 18.0V nominal, 4.5 .. 32.0V short time operation
- Output 3.3V @ 12.0A
- Free-Running-Switching Frequency of 440 kHz



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1. Startup

The startup waveform at 12.0V input voltage and no load on the 3.3V output is shown in Figure 1.

Channel C1 **12.0V Input Voltage**

2V/div, 2ms/div

Channel C2 **3.3V Output Voltage**

1V/div, 2ms/div

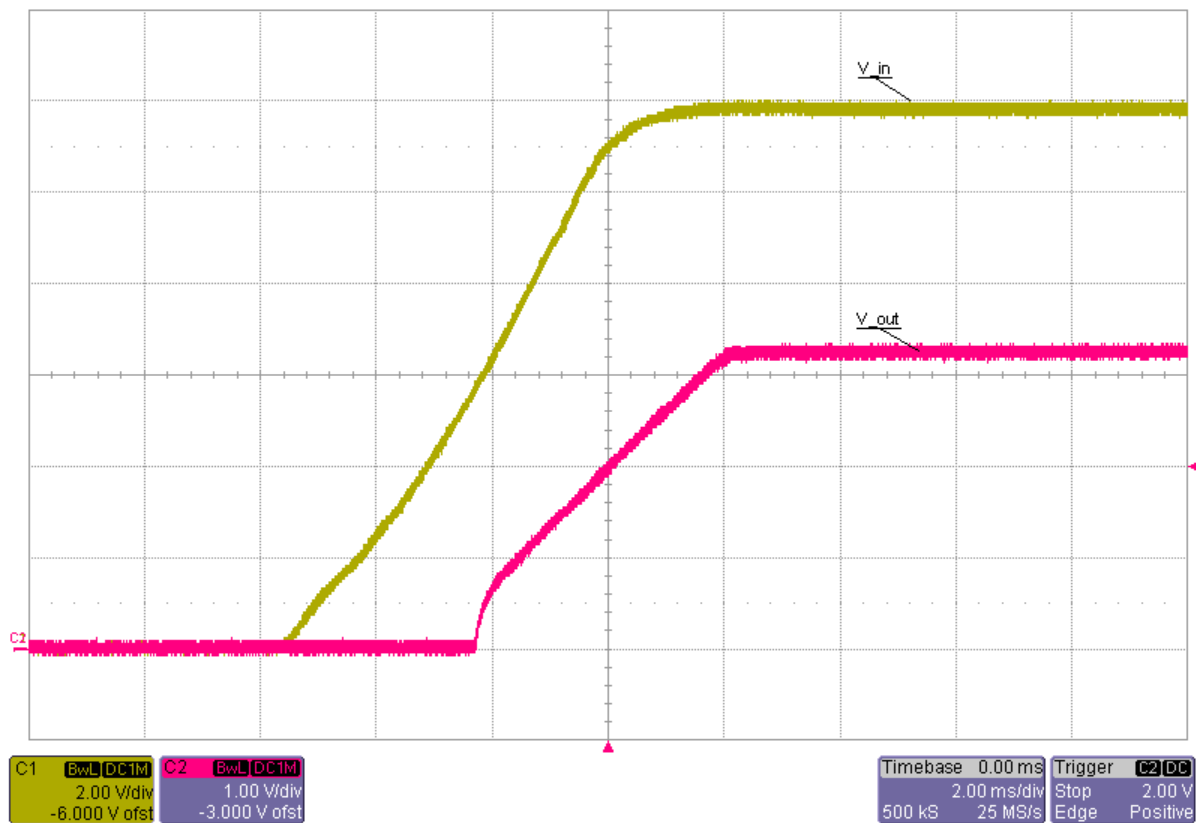


Figure 1

2. Shutdown

The shutdown waveform at 12.0V input voltage and 10.0A load at 3.3V output voltage is shown in Figure 2.

Channel C1 **12.0V Input Voltage**
2V/div, 500us/div

Channel C2 **3.3V Output Voltage**
1V/div, 500us/div

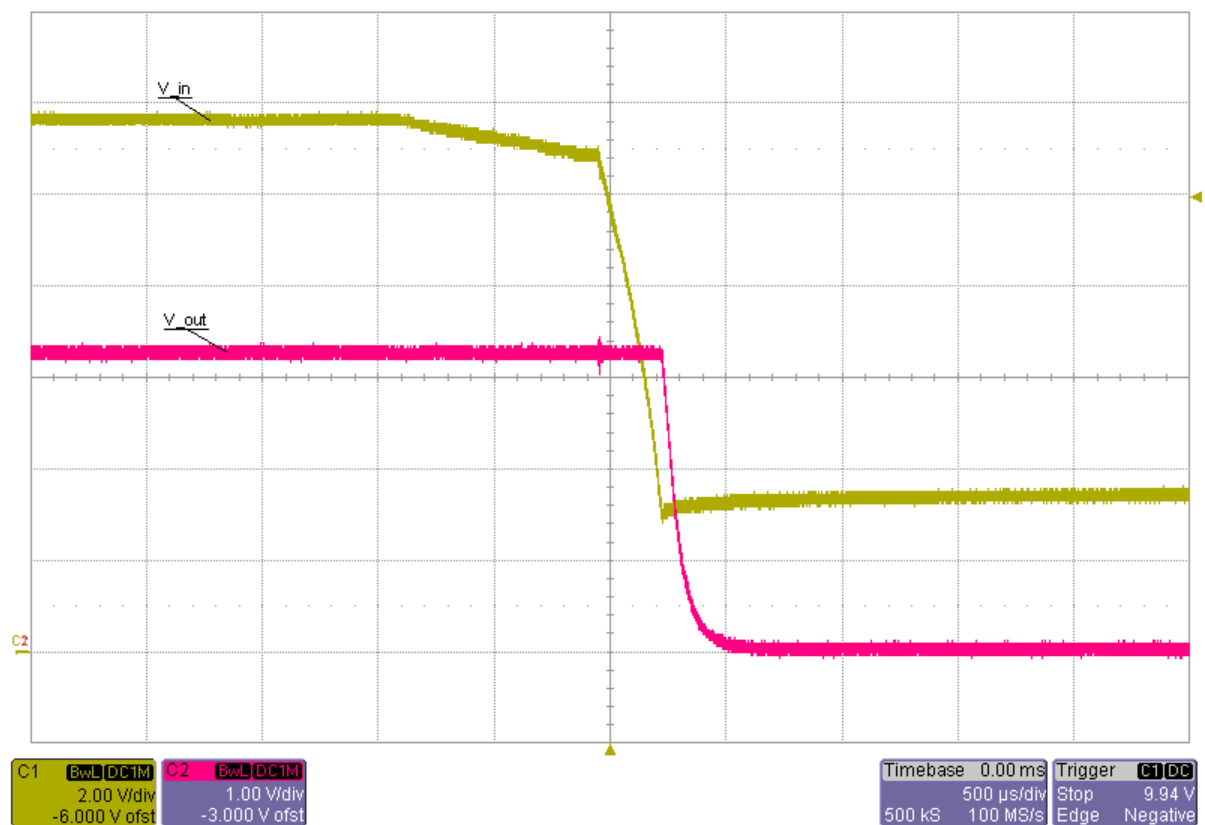


Figure 2

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3. Efficiency

The efficiency and load regulation are shown in Figure 3 and Figure 4.

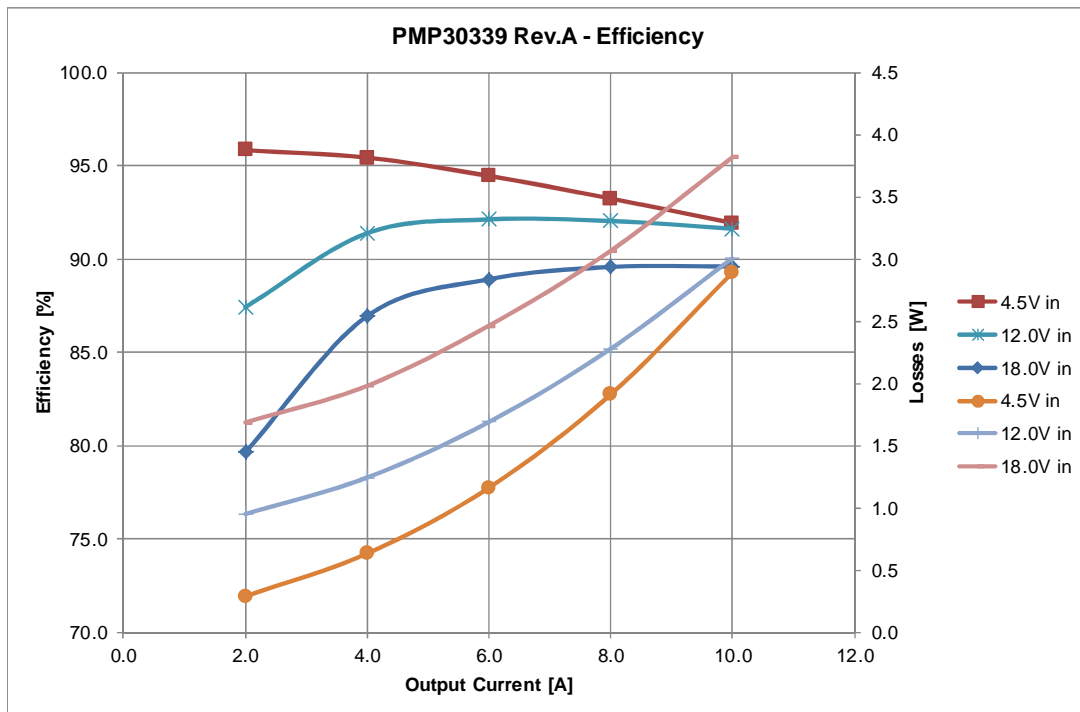


Figure 3

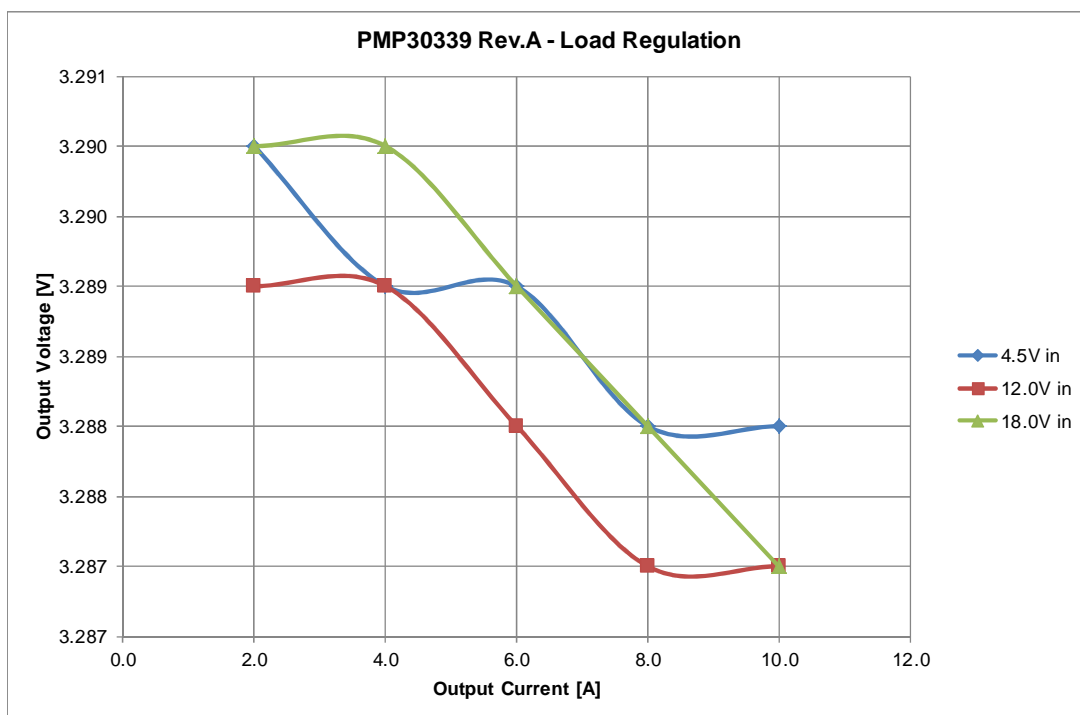


Figure 4

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4. Transient Response

The response to a load step at 12.0V output voltage is shown in Figure 5.

Channel C1 **Output Current**, Load Step 5.0A to 10.0A
5A/div, 1ms/div

Channel C2 **Output Voltage**, -90mV undershoot (2.7%), 1.91V overshoot (2.5%)
50mV/div, 1ms/div, AC coupled

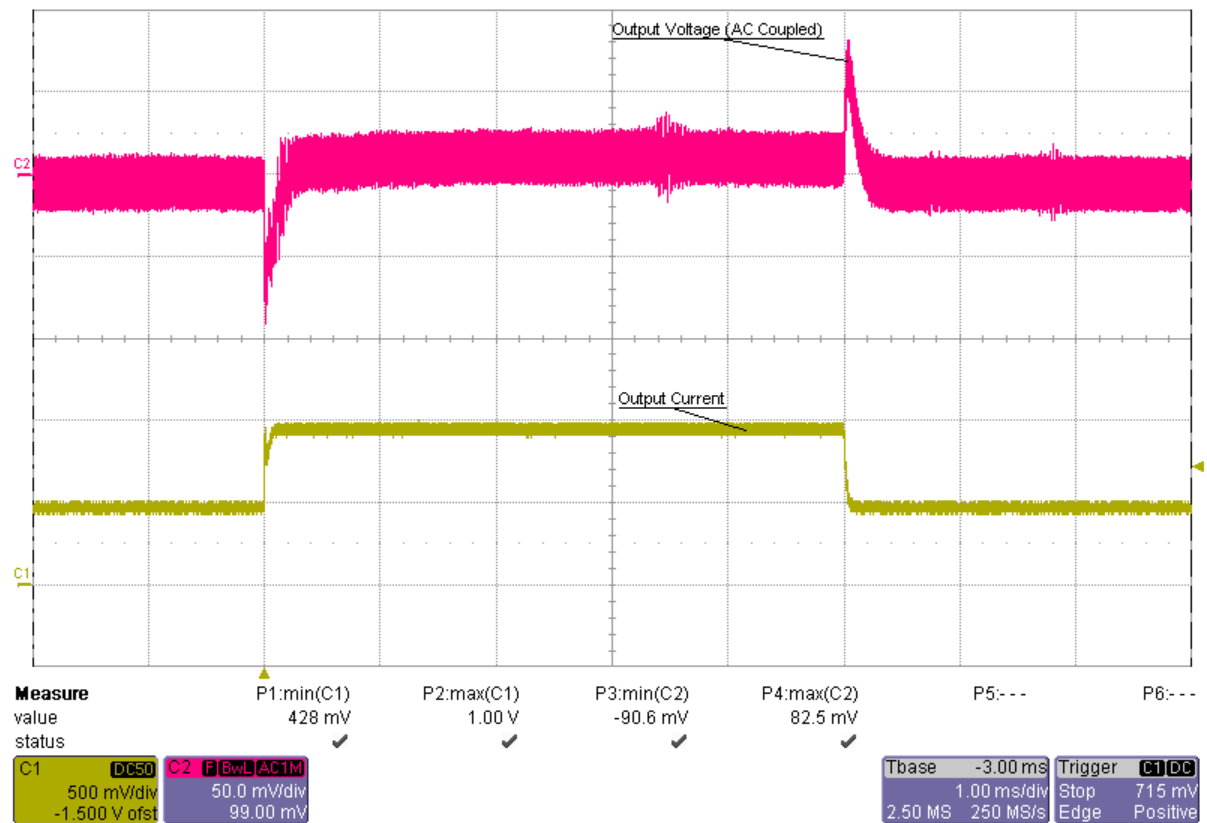


Figure 5

5. Frequency Response

The frequency response for the 2.0A load range is shown in Figure 6.

| | |
|-------------------------|---|
| 4.5V Input, 10.0A Load | 21.9 kHz Bandwidth, 64 deg Phase Margin, -19 dB Gain Margin |
| 9.0V Input, 10.0A Load | 23.0 kHz Bandwidth, 64 deg Phase Margin, -20 dB Gain Margin |
| 12.0V Input, 10.0A Load | 23.2 kHz Bandwidth, 64 deg Phase Margin, -20 dB Gain Margin |
| 18.0V Input, 10.0A Load | 23.1 kHz Bandwidth, 64 deg Phase Margin, -20 dB Gain Margin |

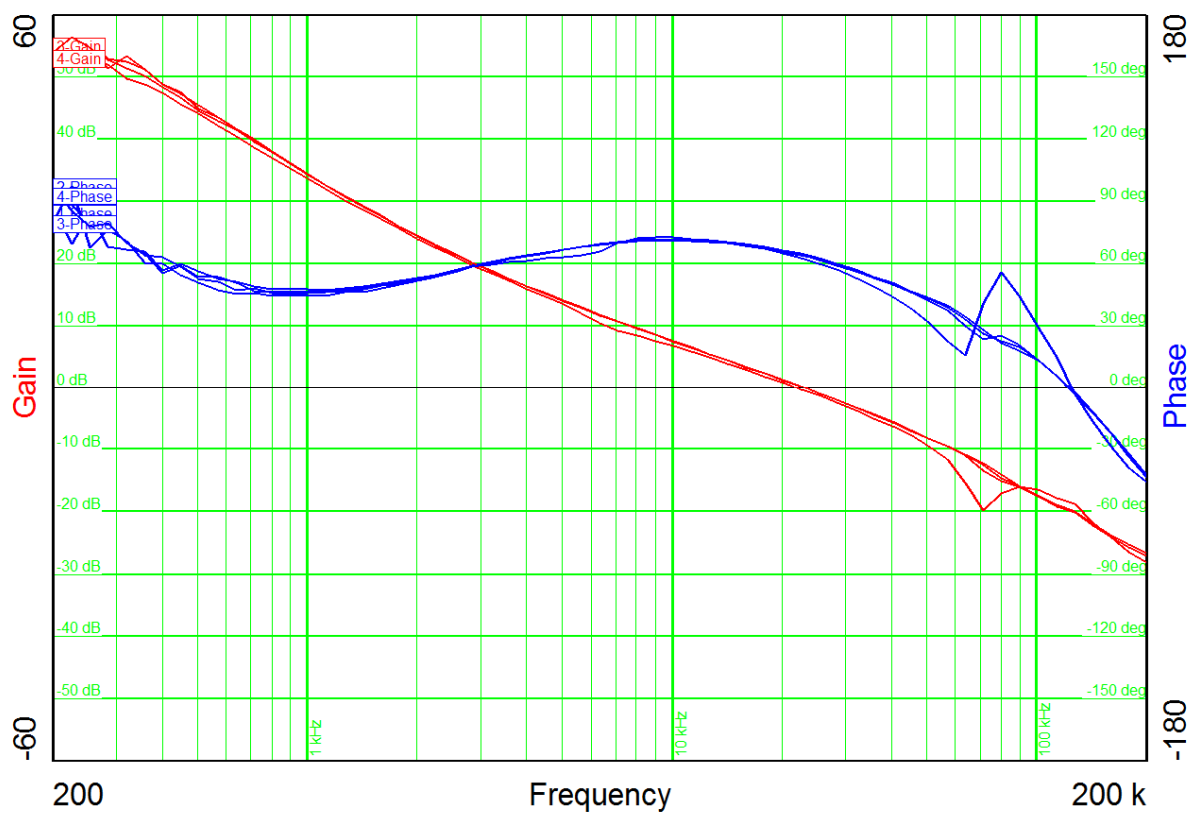


Figure 6

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6. Input Ripple – After Input Filter

The input ripple on the connector (after the input filter) is shown in Figure 7.

Channel M1 **Input Voltage @ 4.5V Input / 10.0A Load**, 13mV peak-peak (0.3%)
10mV/div, 5 μ s/div

Channel M2 **Input Voltage @ 12.0V Input / 10.0A Load**, 17mV peak-peak (0.1%)
10mV/div, 5 μ s/div

Channel M3 **Input Voltage @ 18.0V Input / 10.0A Load**, 17mV peak-peak (0.1%)
10mV/div, 5 μ s/div

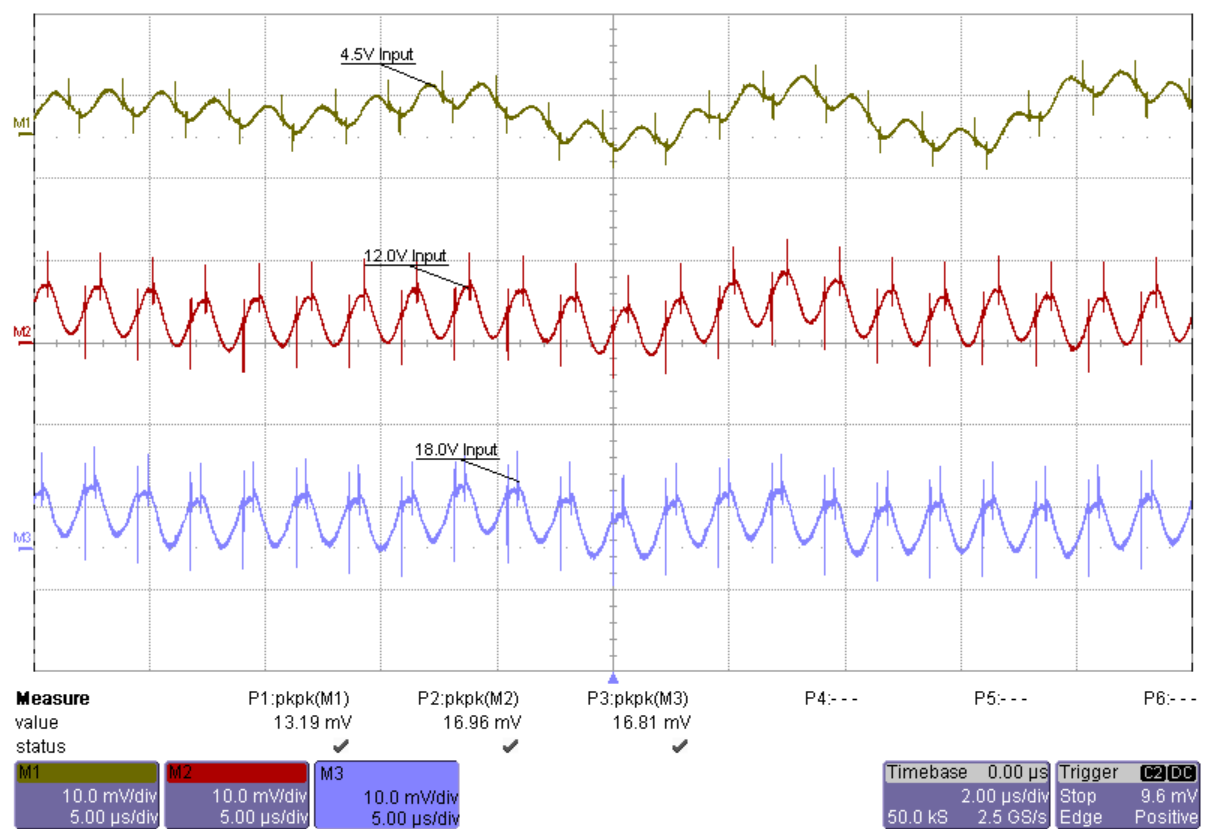


Figure 7

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7. Input Ripple – Before Input Filter

The input ripple on the power stage (before the input filter) is shown in Figure 8. Figure 7

Channel M1 **Input Voltage @ 4.5V Input / 10.0A Load**, 155mV peak-peak (3.4%)
100mV/div, 5us/div

Channel M2 **Input Voltage @ 12.0V Input / 10.0A Load**, 243mV peak-peak (2.0%)
100mV/div, 5us/div

Channel M3 **Input Voltage @ 18.0V Input / 10.0A Load**, 260mV peak-peak (1.4%)
100mV/div, 5us/div

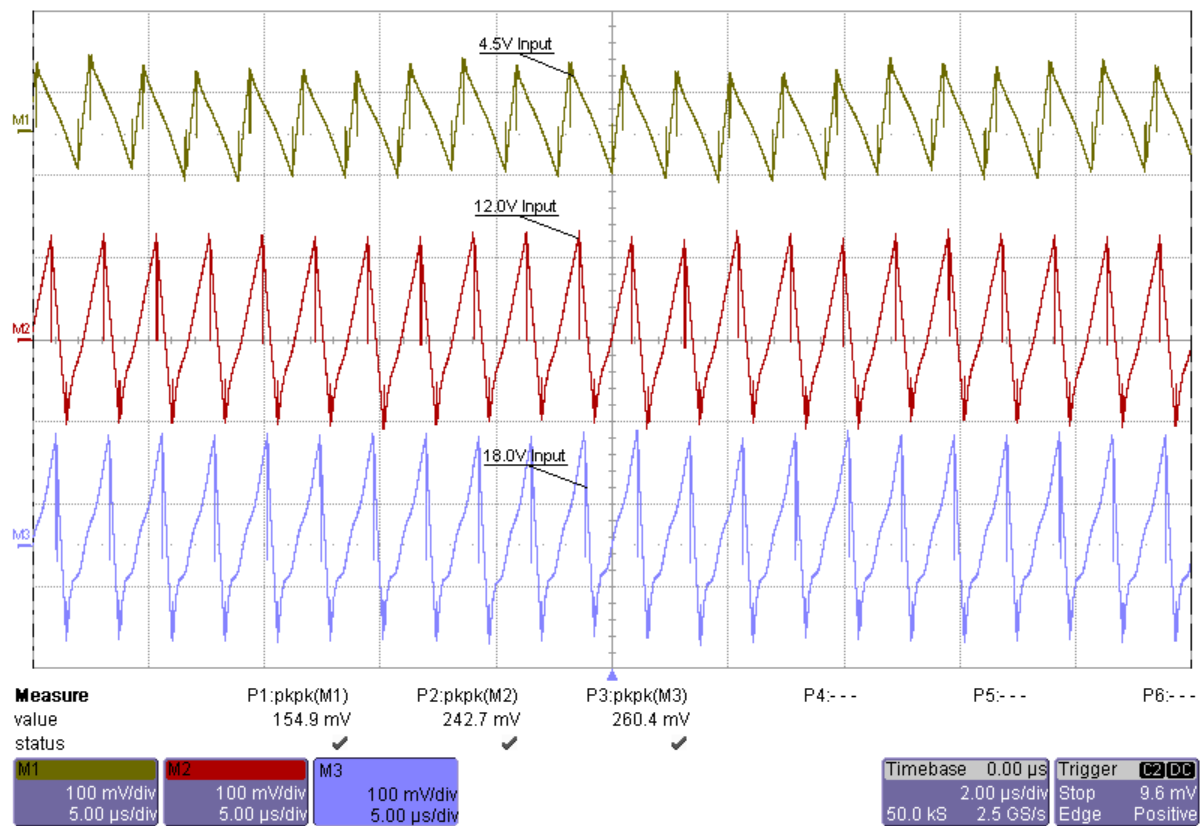


Figure 8

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8. Output Ripple

The output ripple voltage is shown in Figure 9.

Channel M1 **Output Voltage @ 4.5V Input / 10.0A Load**, 11mV peak-peak (0.3%)

10mV/div, 2us/div

Channel M2 **Output Voltage @ 12.0V Input / 10.0A Load**, 23mV peak-peak (0.7%)

10mV/div, 2us/div

Channel M3 **Output Voltage @ 18.0V Input / 10.0A Load**, 24mV peak-peak (0.7%)

10mV/div, 2us/div

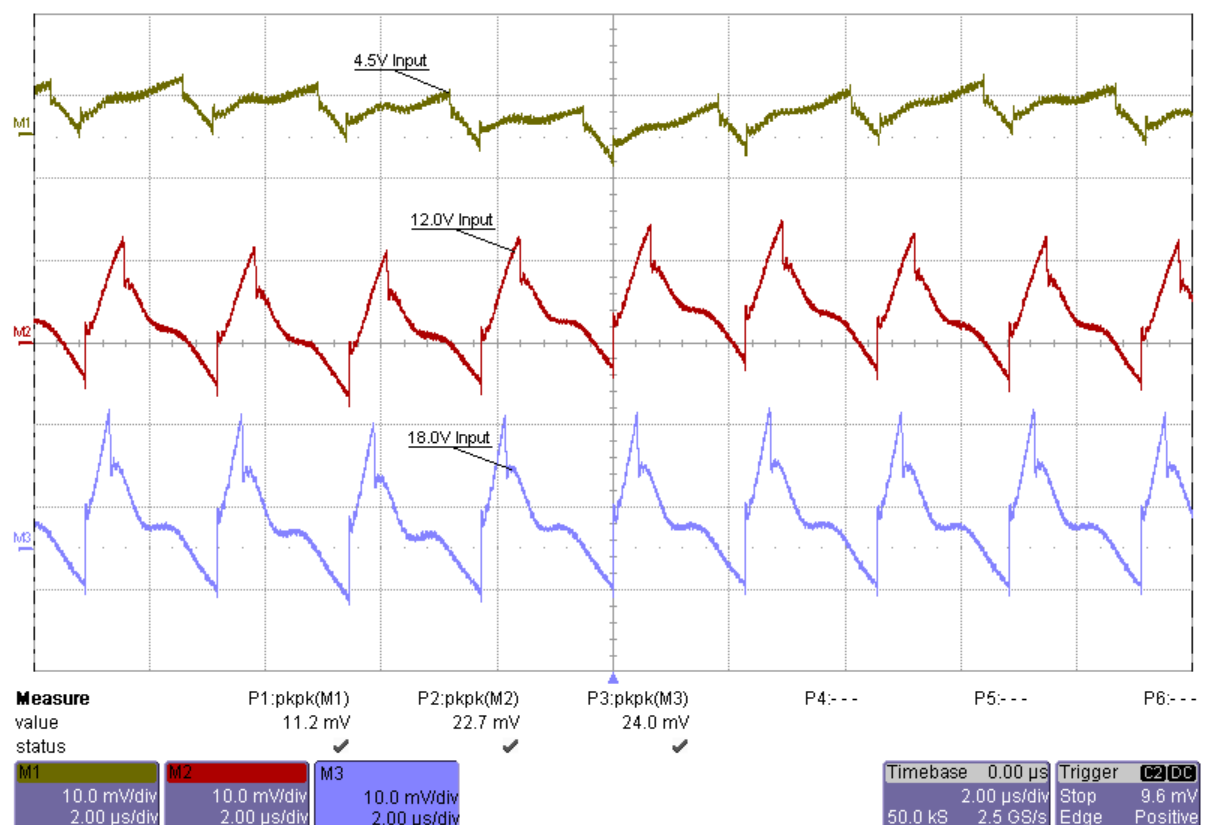


Figure 9

9. Low-Side FET (Switching Node)

The drain-source voltage of the low-side FET at 12.0V input voltage and 10.0A load on the output is shown in Figure 10.

Channel C1 **Drain-Source Voltage**, -1.2V minimum, 15.3V maximum
5V/div, 500ns/div

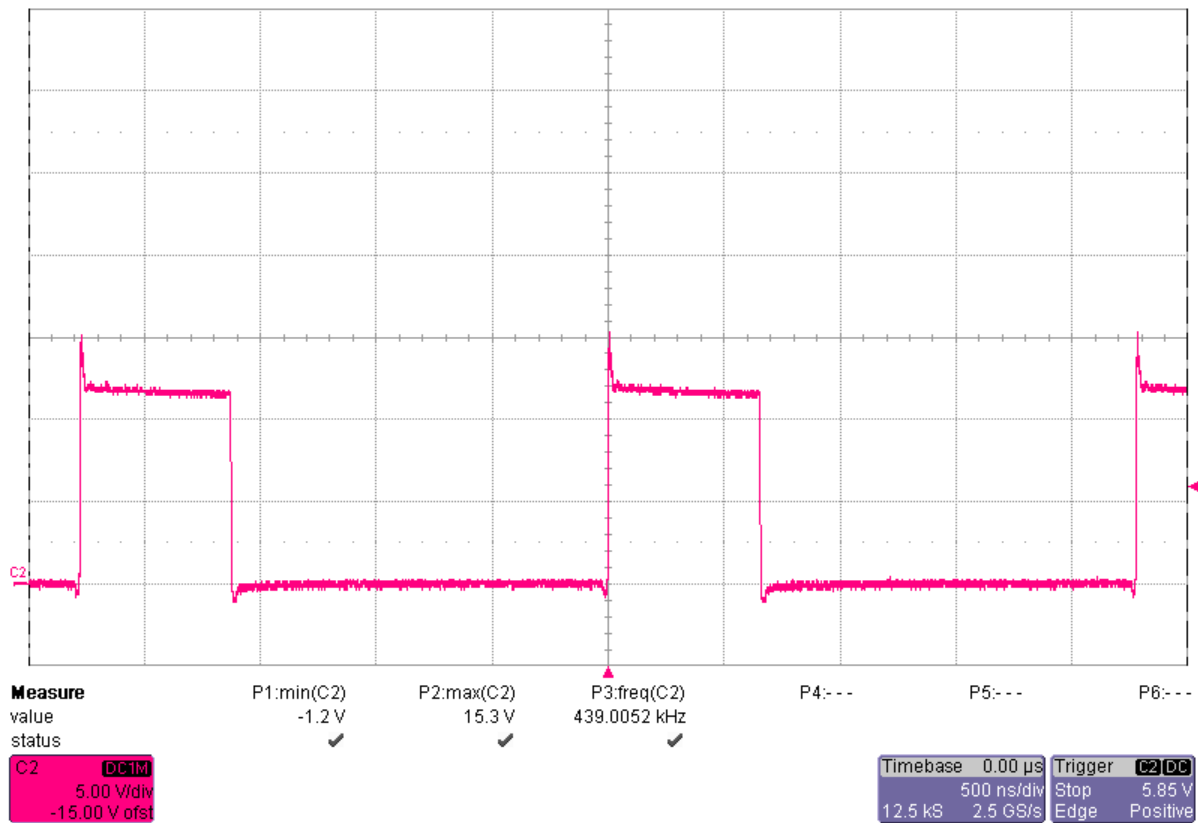


Figure 10

11. Thermal Image

The thermal image (Figure 11) shows the circuit at an ambient temperature of 20°C with an input voltage of 12.0V and 10.0A load on the output.

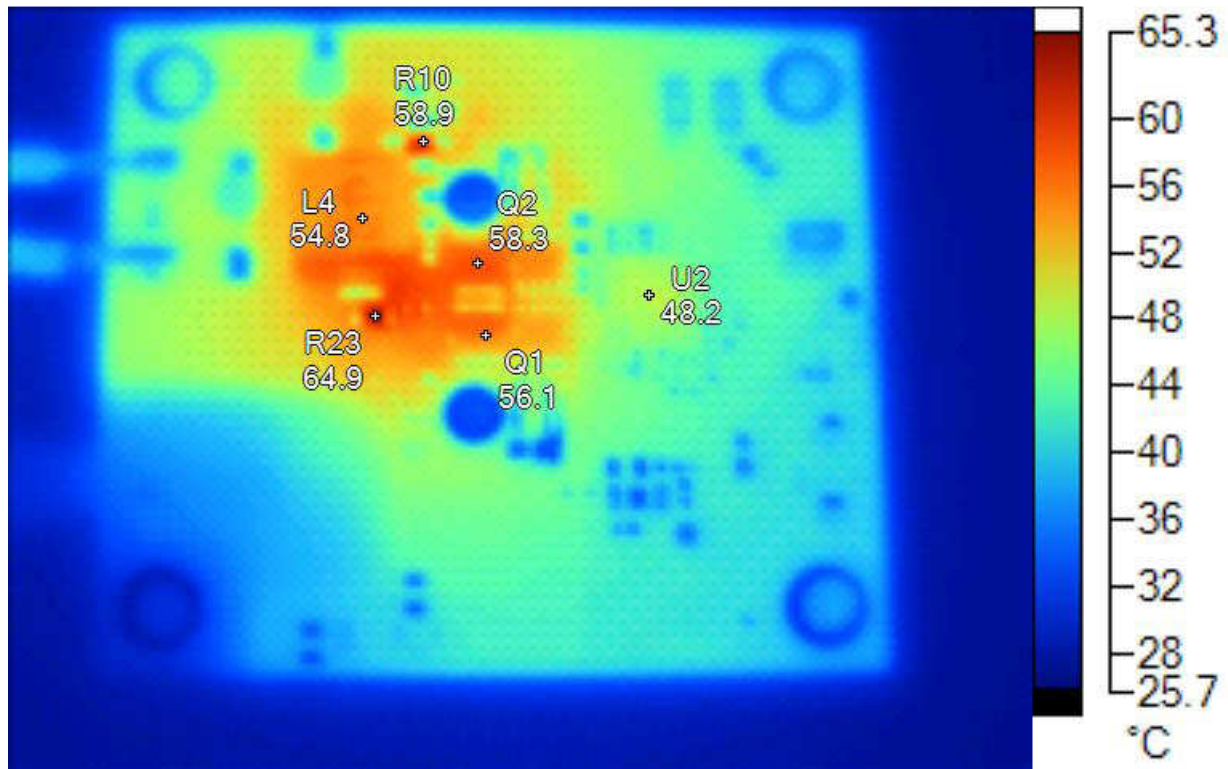


Figure 11

| Name | Temperature | Emissivity | Background |
|------|-------------|------------|------------|
| L4 | 54.8°C | 0.95 | 20.0°C |
| R10 | 58.9°C | 0.95 | 20.0°C |
| Q1 | 56.1°C | 0.95 | 20.0°C |
| Q2 | 58.3°C | 0.95 | 20.0°C |
| R23 | 64.9°C | 0.95 | 20.0°C |
| U2 | 48.2°C | 0.95 | 20.0°C |

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