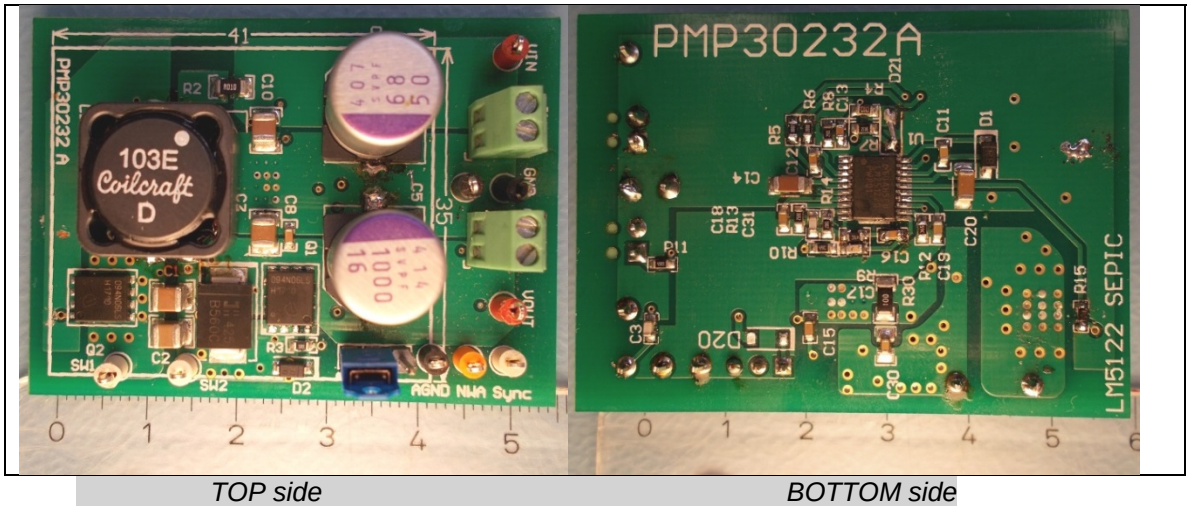
PMP30331RevB Test Results

Topology: SEPIC
Device: LM25122
Switching frequency approx.. 250kHz, measured 258kHz
ON ~4.99V
OFF ~3.71V
(measured at 3A resistive load)

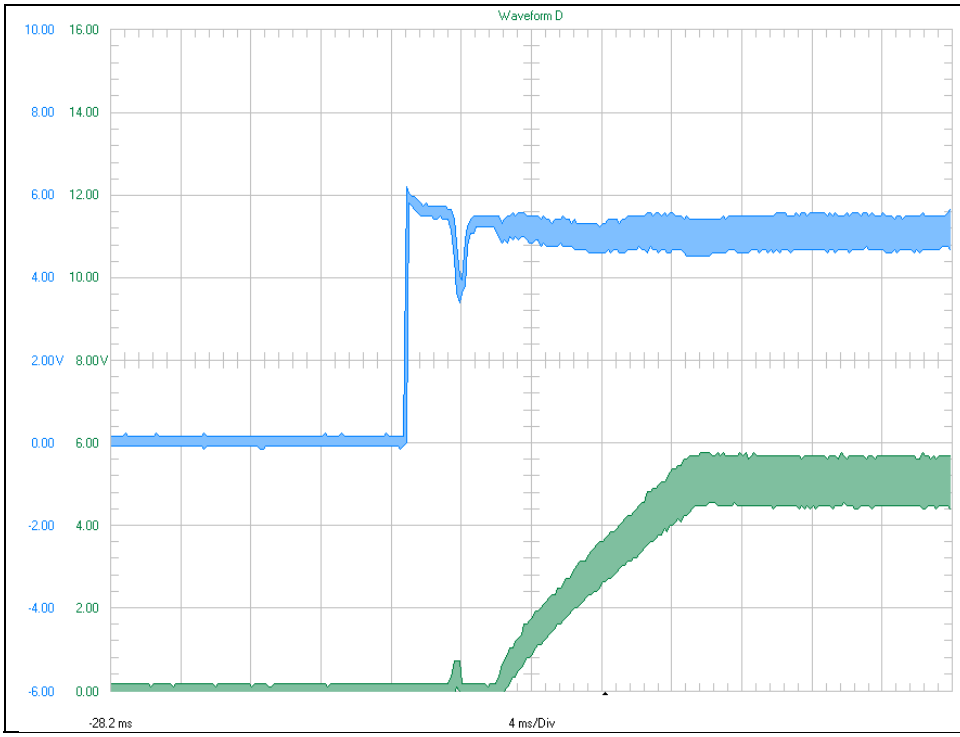
Unless otherwise mentioned the output current was set to 3A (with electronic load) and the MODE was set to forced PWM



TOP side *BOTTOM side*

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set to 5V.



Ch1=> input voltage 2V/div

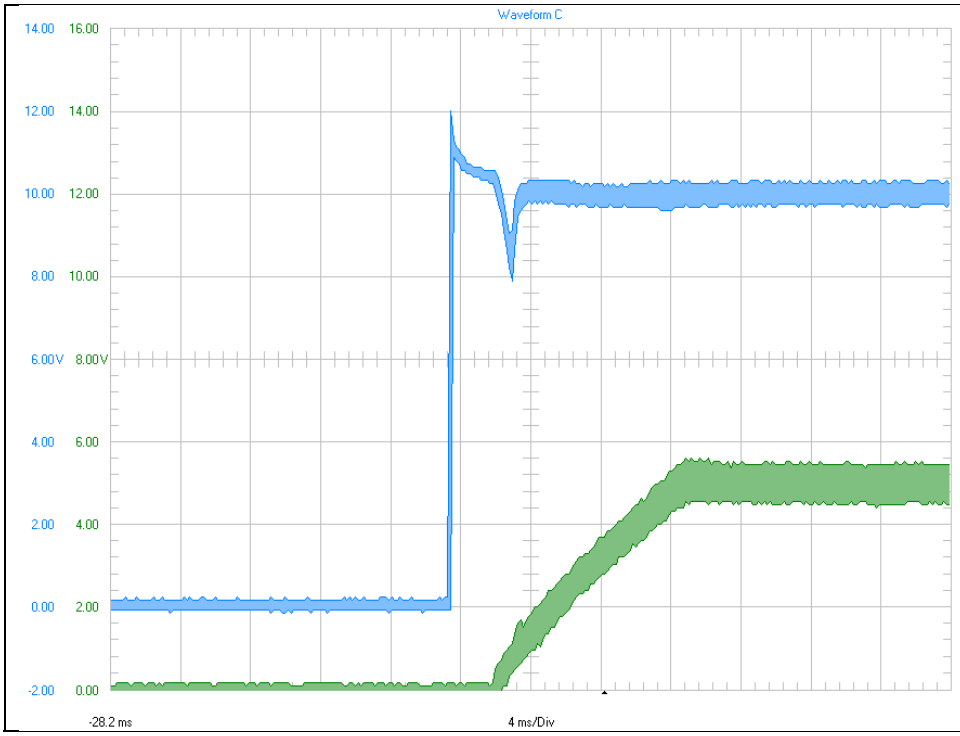
Ch2=> output voltage 2V/div

4ms/div

20MHz bw

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set to 10V.



Ch1=> input voltage 2V/div

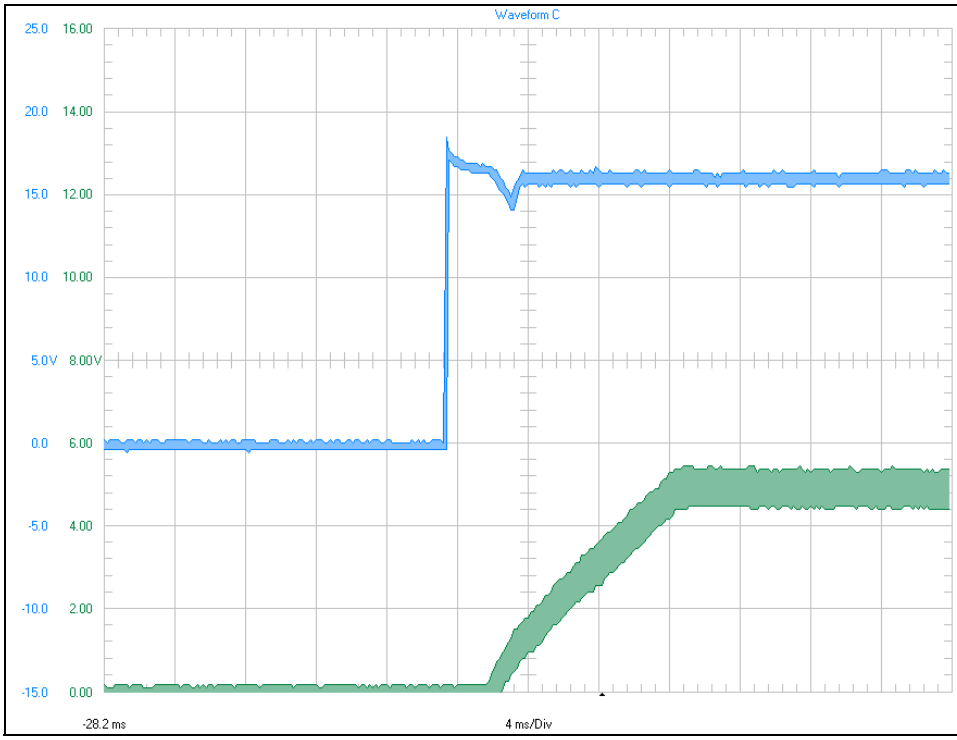
Ch2=> output voltage 2V/div

4ms/div

20MHz bw

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set to 16V.



Ch1=> input voltage 5V/div

Ch2=> output voltage 2V/div

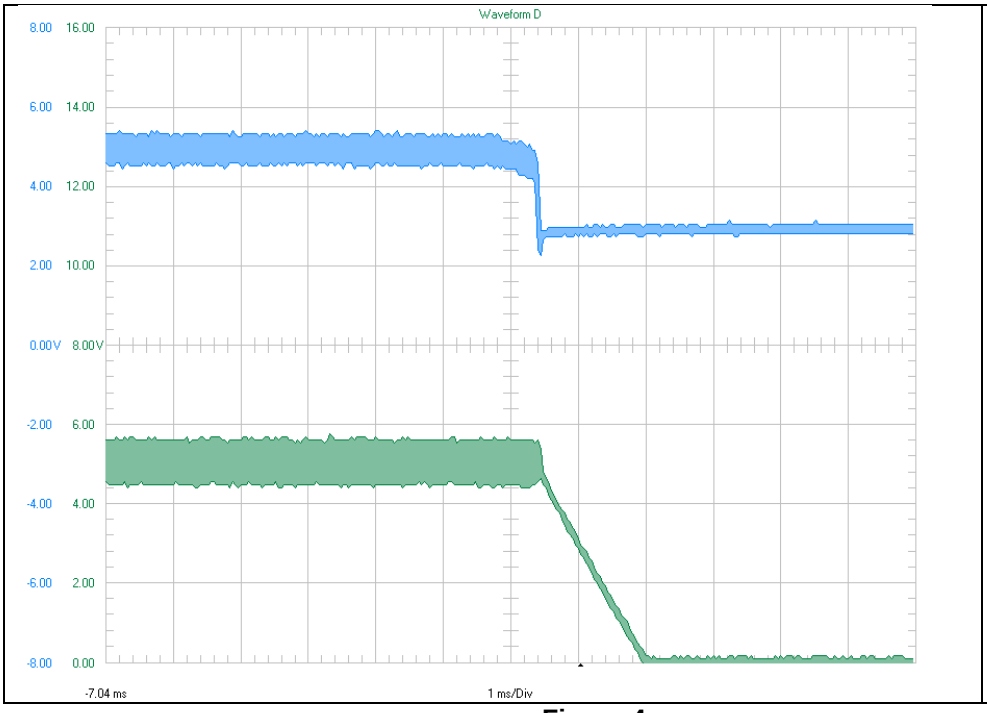
4ms/div

20MHz bw

Figure 3

2 Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set to 5 V.
The power supply was disconnected**.**



Ch1=> input voltage 2V/div

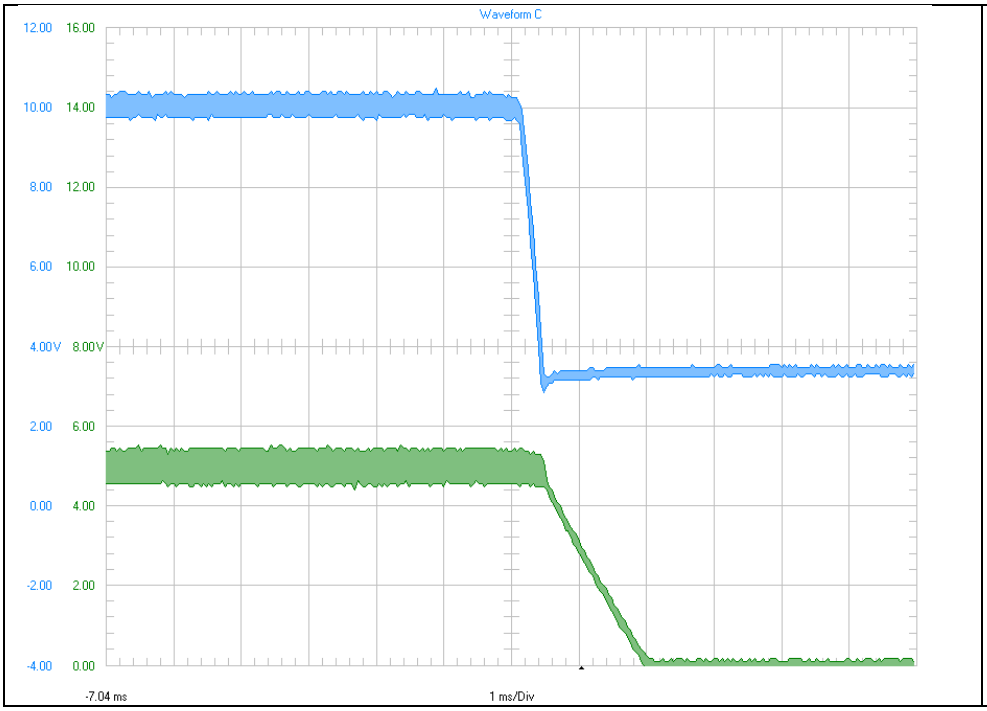
Ch2=> output voltage 2V/div

1ms/div

20MHz bw

Figure 4

The shutdown waveform is shown in the Figure 5. The input voltage was set to 10V.
The power supply was disconnected.



Ch1=> input voltage 2V/div

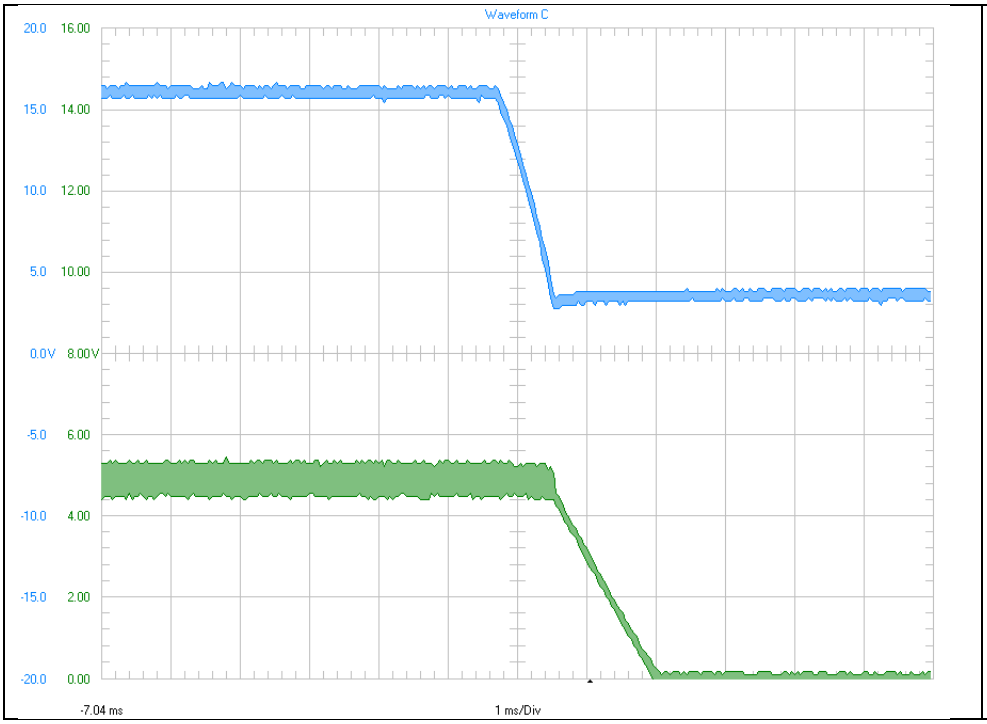
Ch2=> output voltage 2V/div

1ms/div

20MHz bw

Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set to 16V.
The power supply was disconnected.



Ch1=> input voltage 5V/div

Ch2=> output voltage 2V/div

1ms/div

20MHz bw

Figure 6

3 Efficiency

3.1 Forced PWM

The efficiency and loss (PIN-POUT) is shown in the Figure 7 below.
The input voltage was set to 5V, 10V and 16V. The mode was set to **forced PWM**.

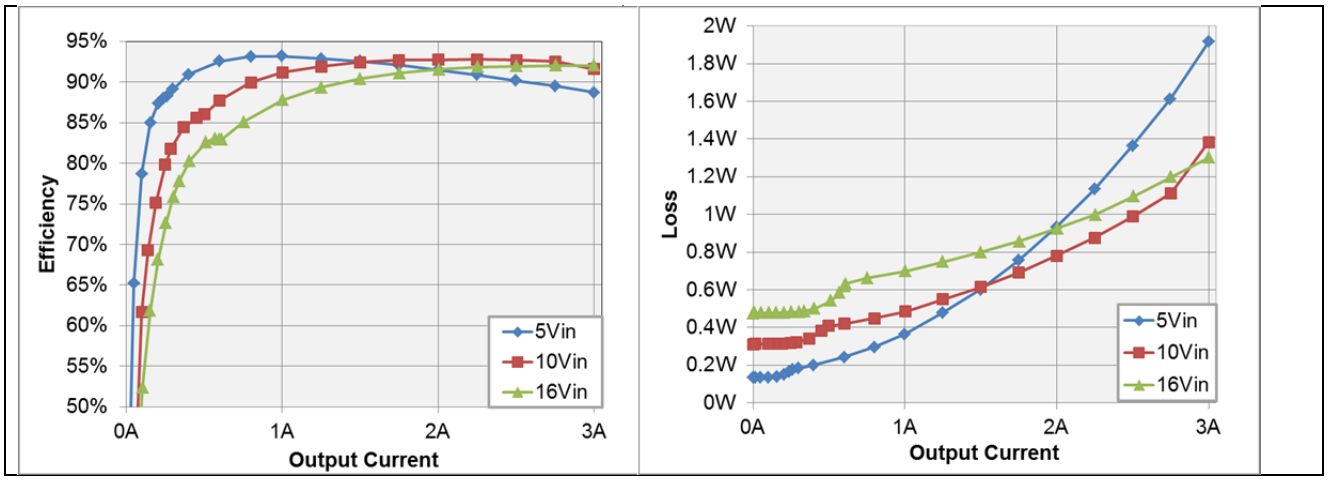


Figure 7

3.2 Diode Emulation

The efficiency and loss (PIN-POUT) is shown in the Figure 8 below.
The input voltage was set to 5V, 10V and 16V. The mode was set to **diode Emulation**.

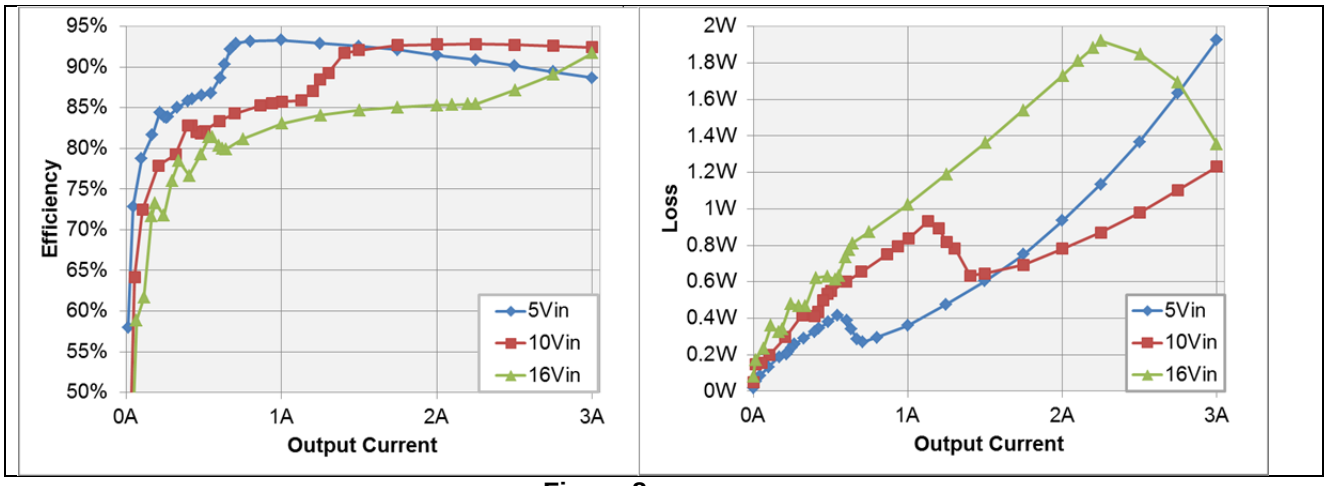
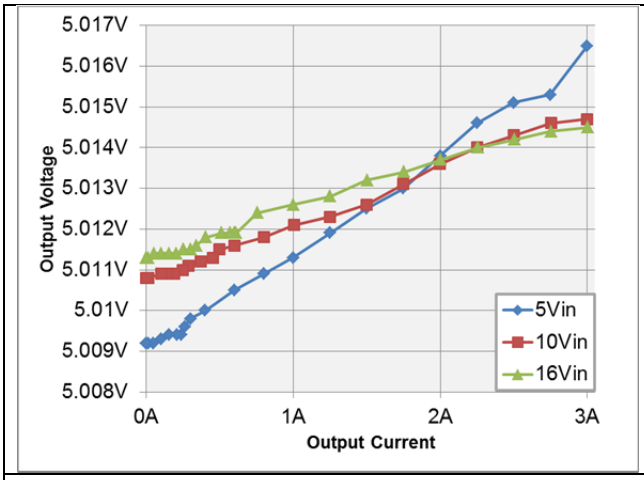


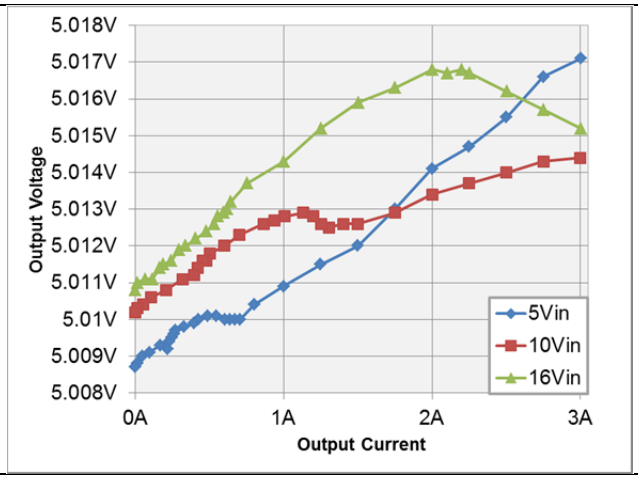
Figure 8

4 Load Regulation

The load regulation of the output is shown in the Figure 9 below.
The input voltage was set to 5V, 10V and 16V.



forced PWM



diode emulation

Figure 9

5 Line Regulation

The line regulation is shown in Figure 10. The output current was set to 3A.

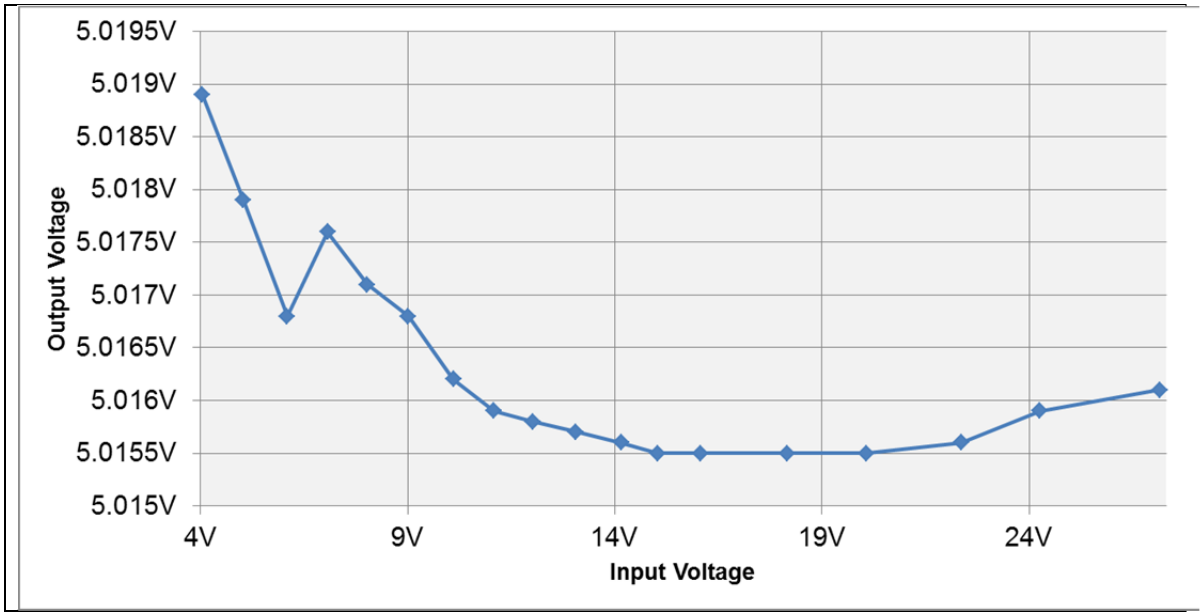


Figure 10

With the same setup efficiencies and losses were calculated. This is shown in Figure 11

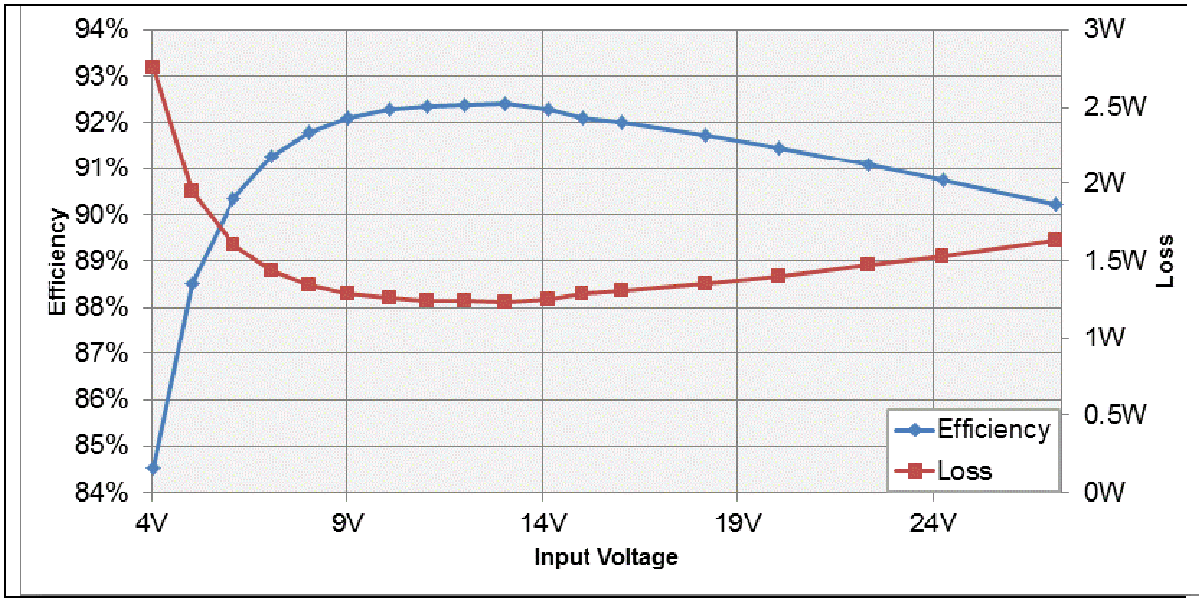
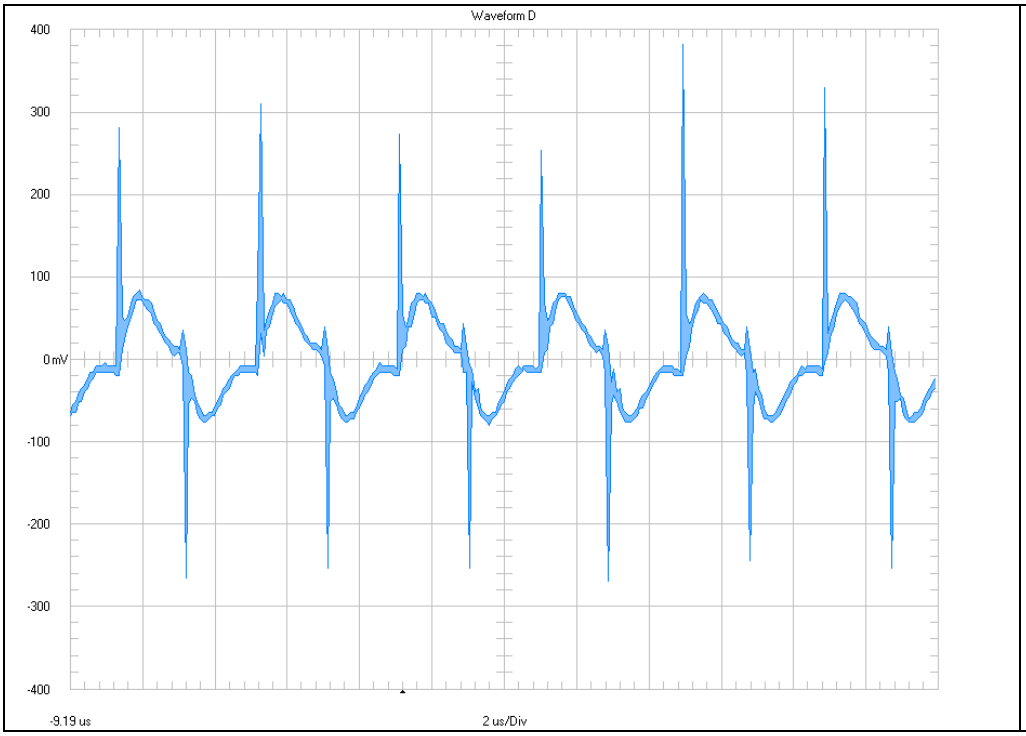


Figure 11

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 12. Input voltage was set to 5V



Ch1 => output ripple

100mV/div

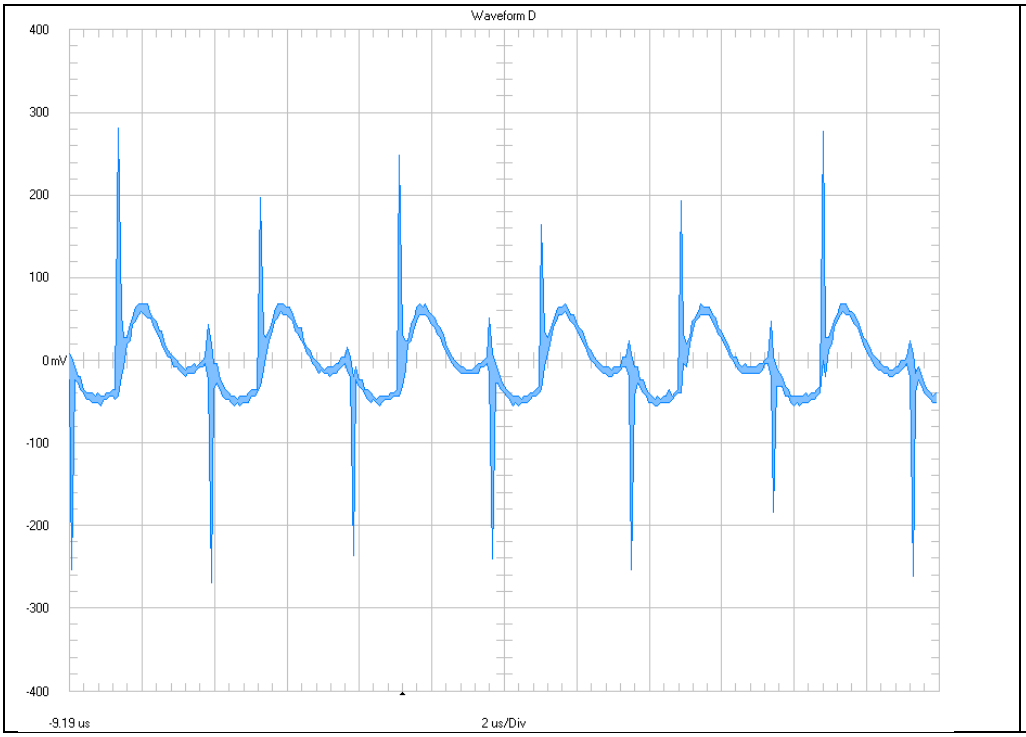
AC coupled

20MHz bw

2µs/div

Figure 12

The output ripple voltage is shown in Figure 13. Input voltage was set to 10V



Ch1 => output ripple

100mV/div

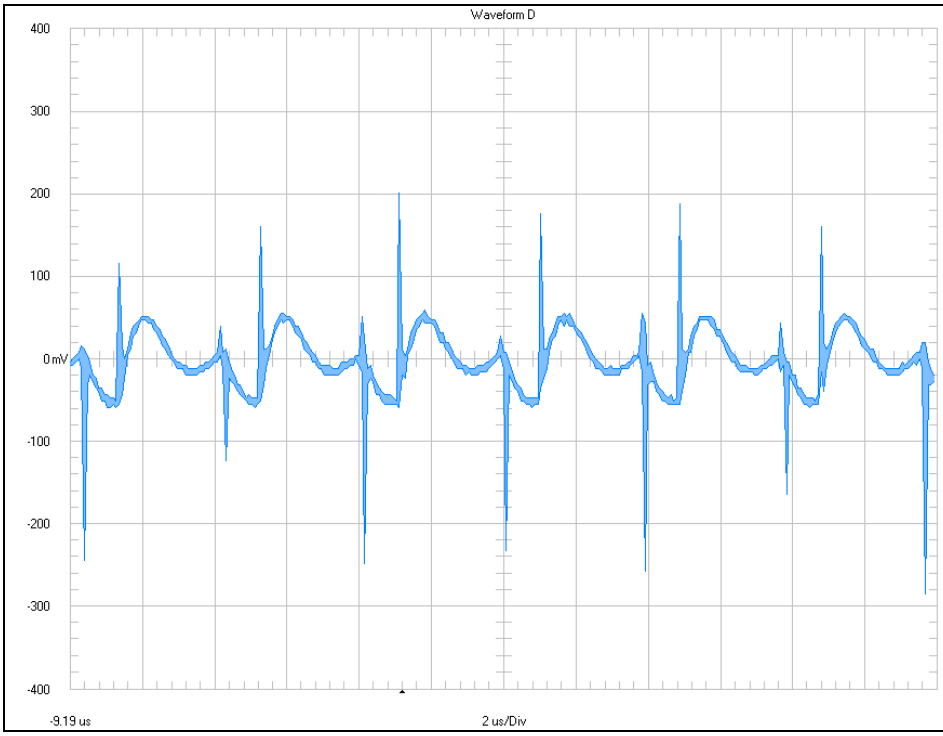
AC coupled

20MHz bw

2µs/div

Figure 13

The output ripple voltage is shown in Figure 14. Input voltage was set to 16V.



Ch1 => output ripple

100mV/div

AC coupled

20MHz bw

2µs/div

Figure 14

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 15. Input voltage was set to 5V

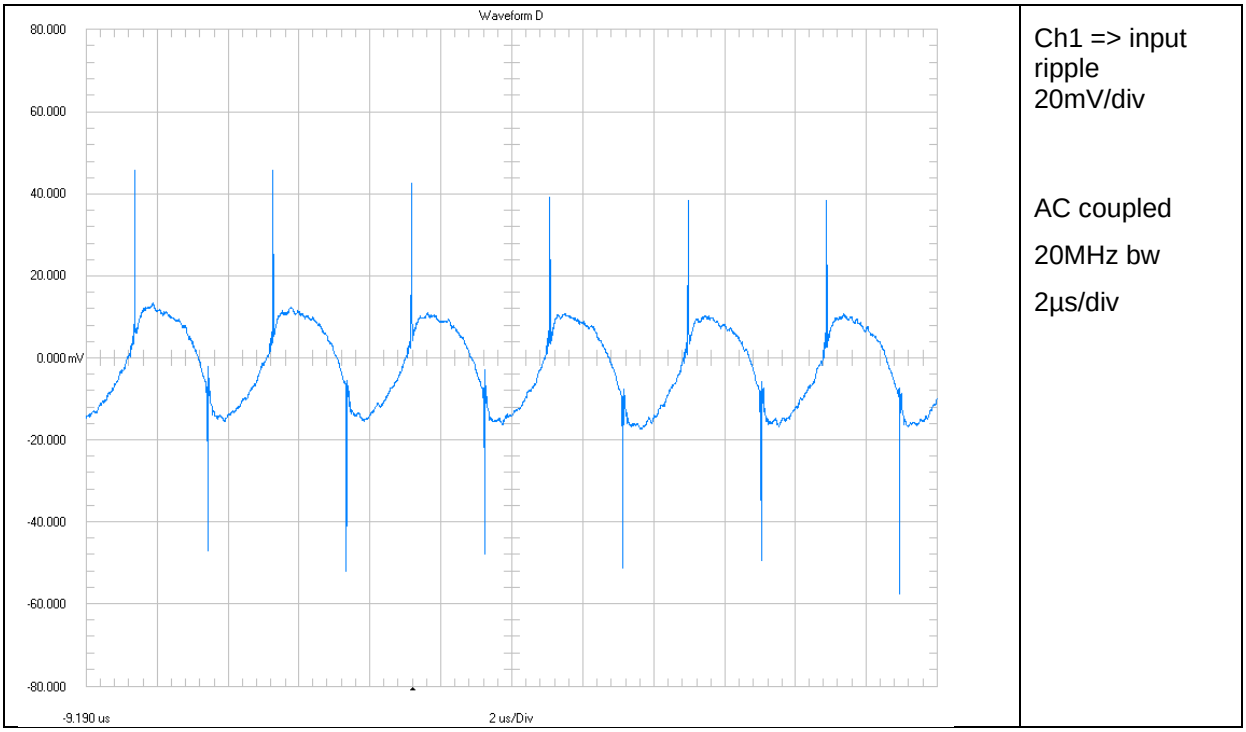


Figure 15

The input ripple voltage is shown in Figure 16. Input voltage was set to 10V.

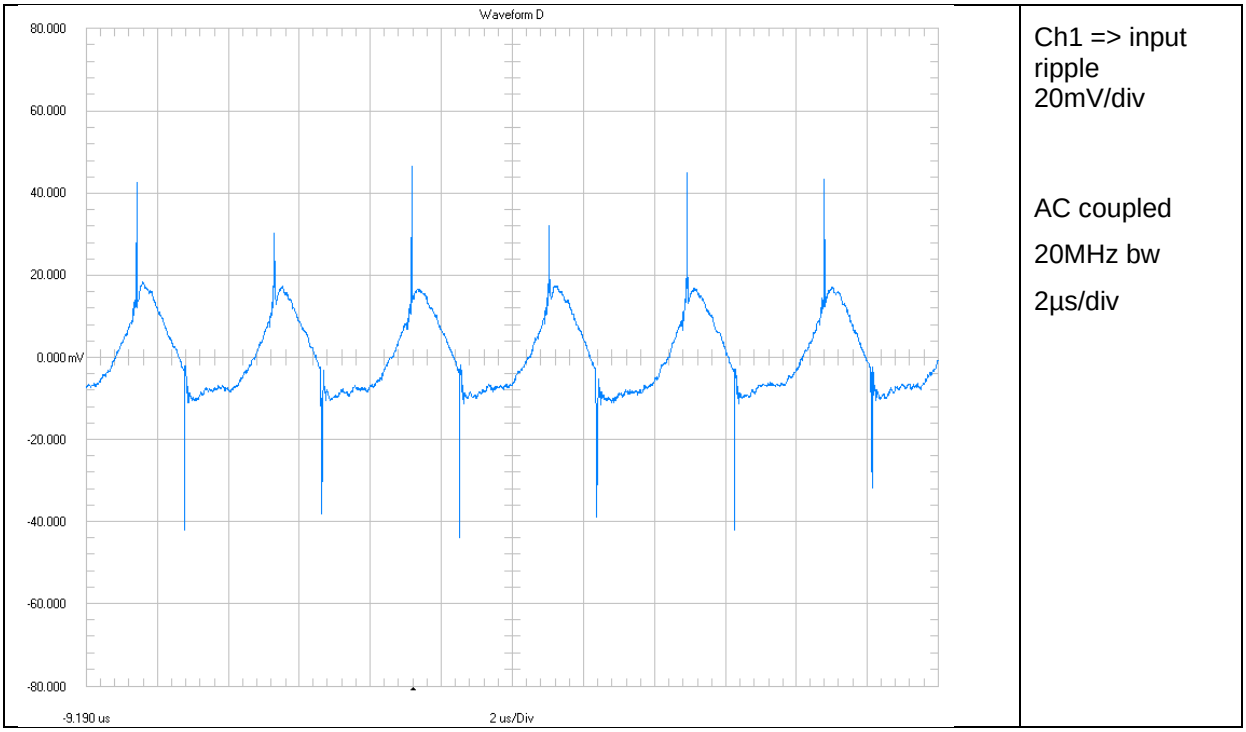
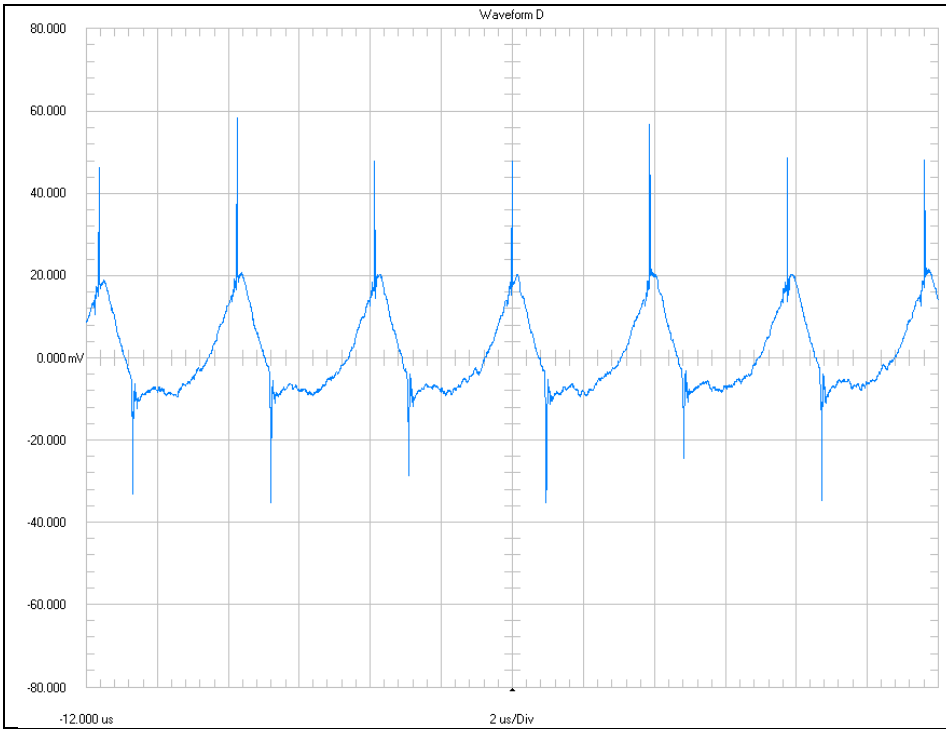


Figure 16

The input ripple voltage is shown in Figure 17. Input voltage was set to 16V.



Ch1 => input ripple 50mV/div

AC coupled

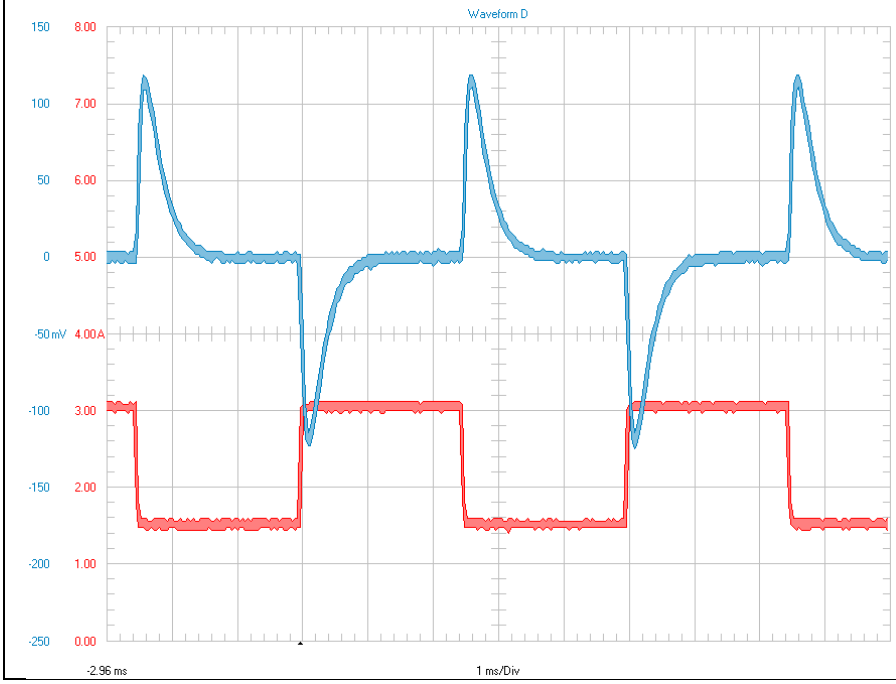
20MHz bw

2µs/div

Figure 17

8 Load Transients

The Figure 18 shows the response to load transients for 5V input voltage. The load is switching from 1.5A to 3A (200Hz)



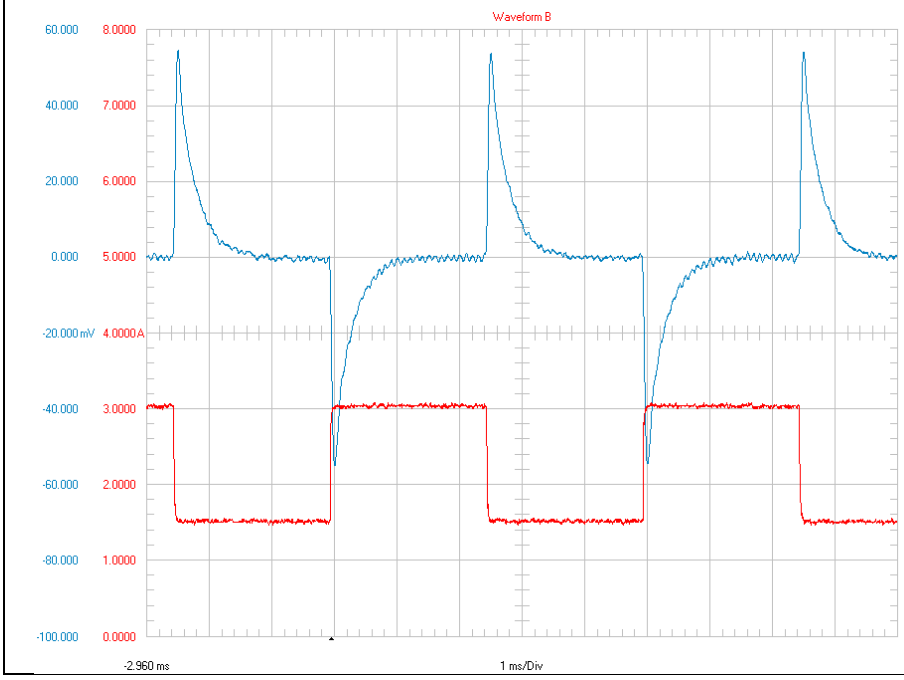
Ch1 => output voltage
50mV/div
AC coupling
10kHz bw

Ch2 => output current 1A/div
20MHz bw

1ms/div

Figure 18

The Figure 19 shows the response to load transients for 10V input voltage. The load is switching from 1.5A to 3A,



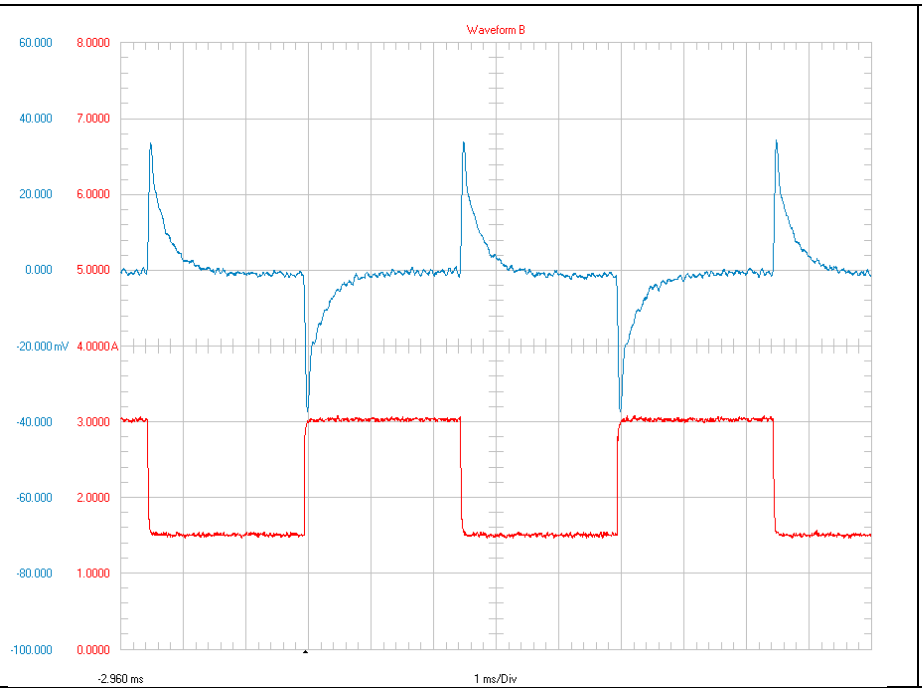
Ch1 => output voltage
20mV/div
AC coupling
10kHz bw

Ch2 => output current 1A/div
20MHz bw

1ms/div

Figure 19

The Figure 20 shows the response to load transients for 16V input voltage. The load is switching from 1.5A to 3A.



Ch1 => output voltage
20mV/div
AC coupling
10kHz bw

Ch2 => output current 1A/div
20MHz bw

1ms/div

Figure 20

9 Control Loop Frequency Response

Figure 21 shows the loop response for 5V. Load is about 3A (resistor).

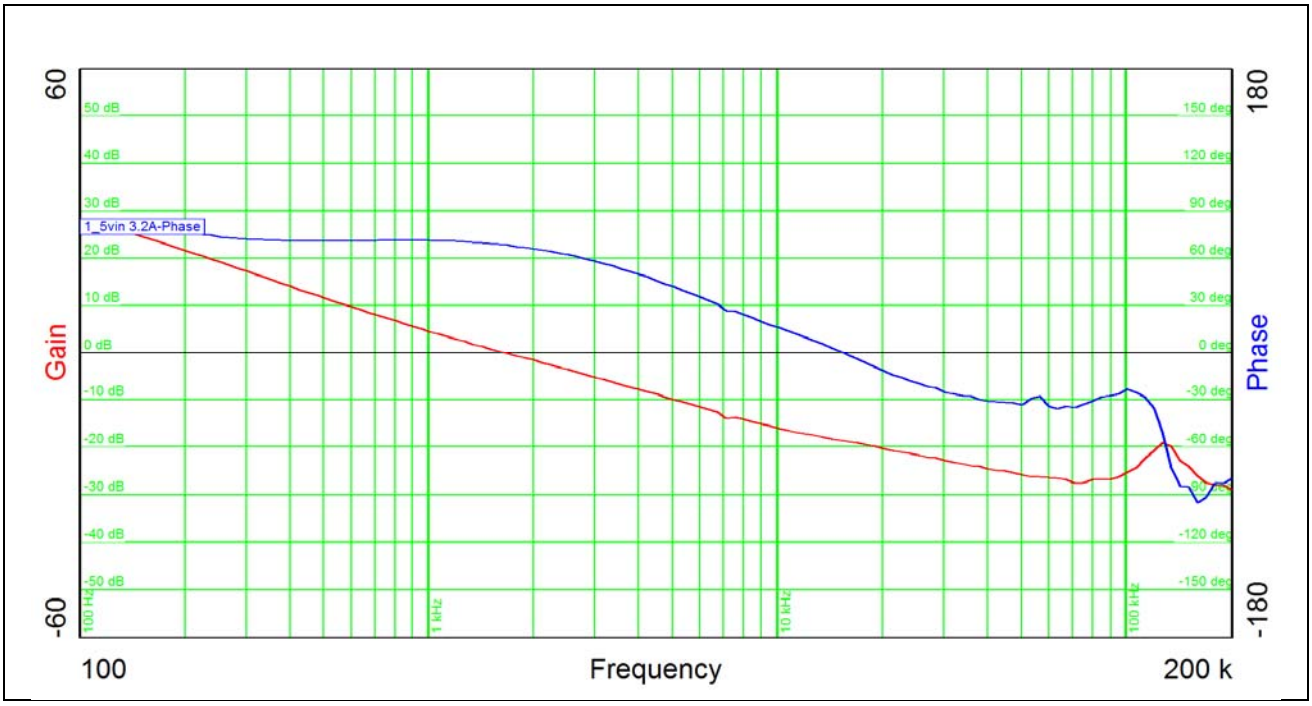


Figure 21

Figure 22 shows the loop response for 10V. Load is about 3A (resistor).

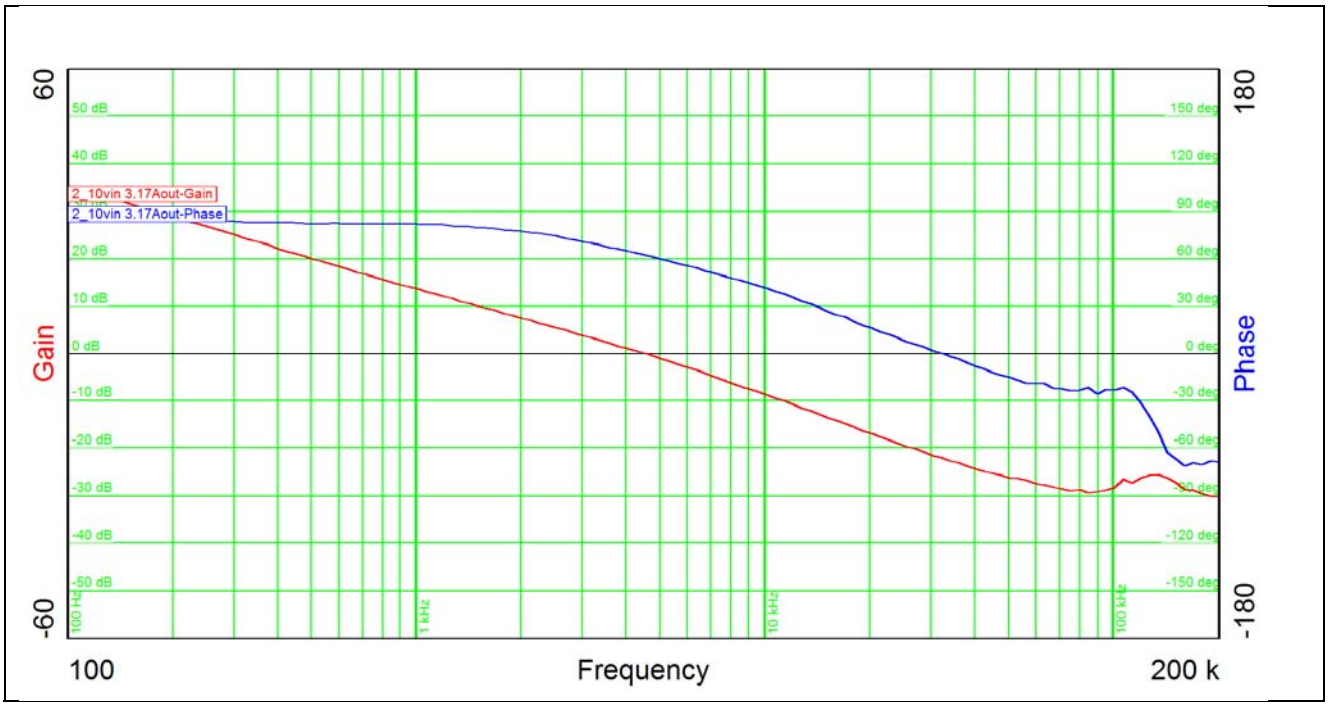


Figure 22

Figure 23 shows the loop response for 16V. Load is about 3A (resistor).

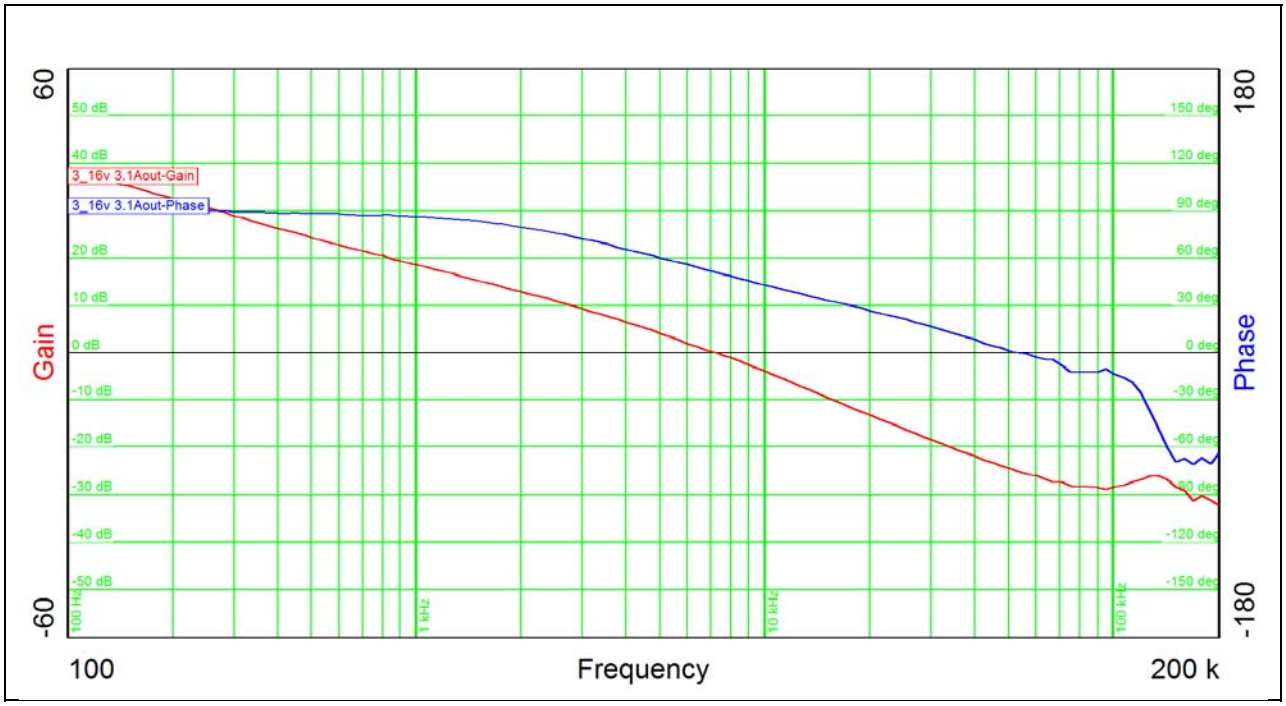


Figure 23

Table 1 summarizes the results of the above measurements

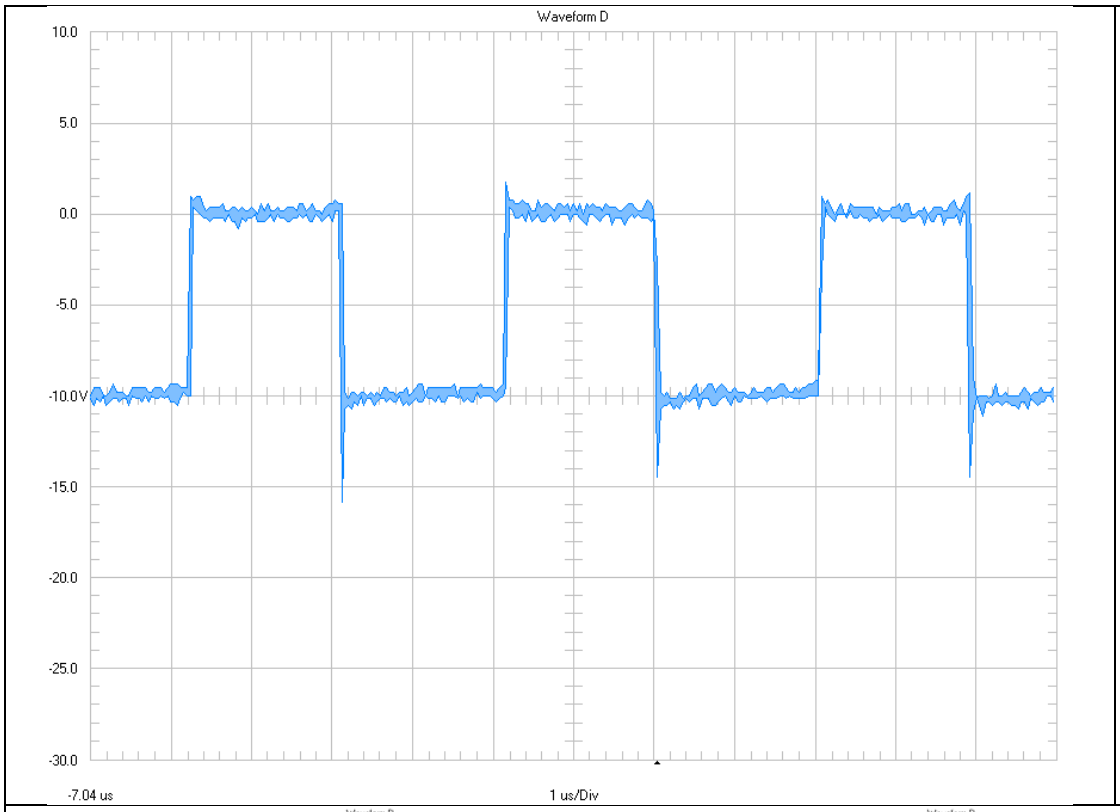
Vin	5V	10V	16V
Bandwidth (kHz)	1.65	4.85	7.16
Phase margin	68°	62°	51°
slope (20dB/decade)	-1	-1.1	-1.34
gain margin (dB)	-18.5	-22	-25
slope (20dB/decade)	-0.66	-1.05	-1.27
freq (kHz)	15.6	32	52.7

Table 1

10 Miscellaneous Waveforms

10.1 Q1 Switch Node (source-VOUT)

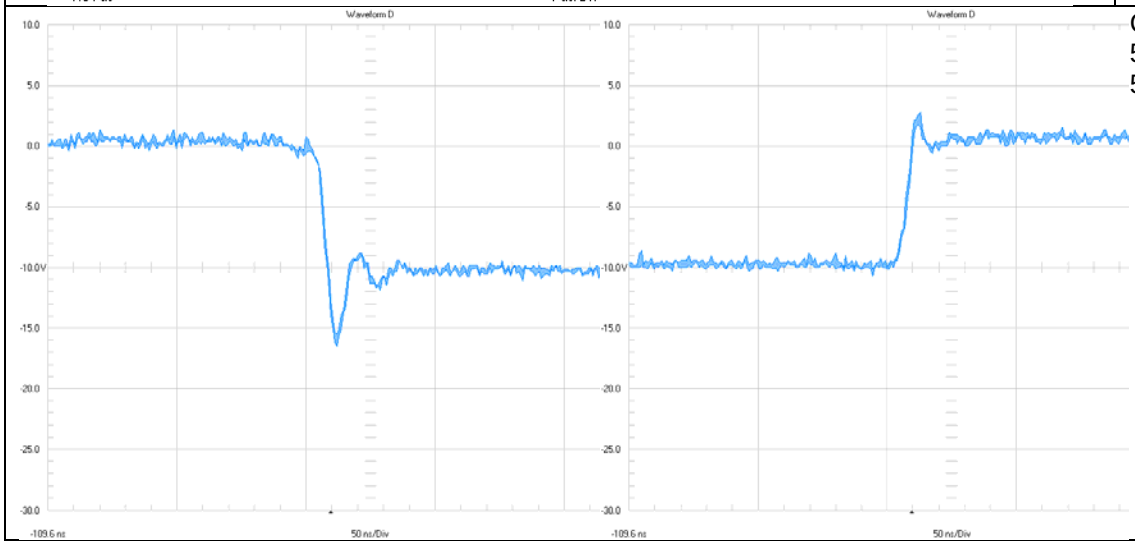
The waveform of the voltage on switchnode is shown in Figure 24. Input voltage was set to 5V.



Ch1 =>
5V/div

1µs/div

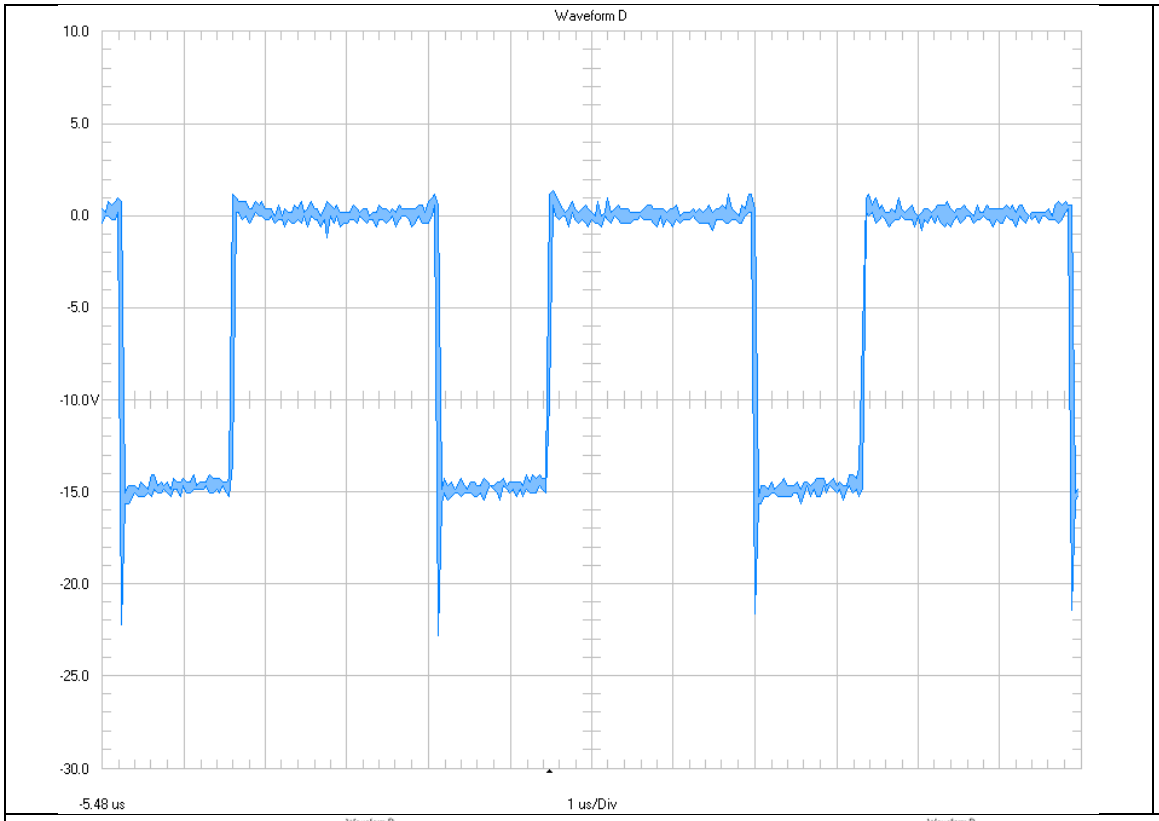
full bandwidth



Ch1 =>
5V/div
50ns/major div

Figure 24

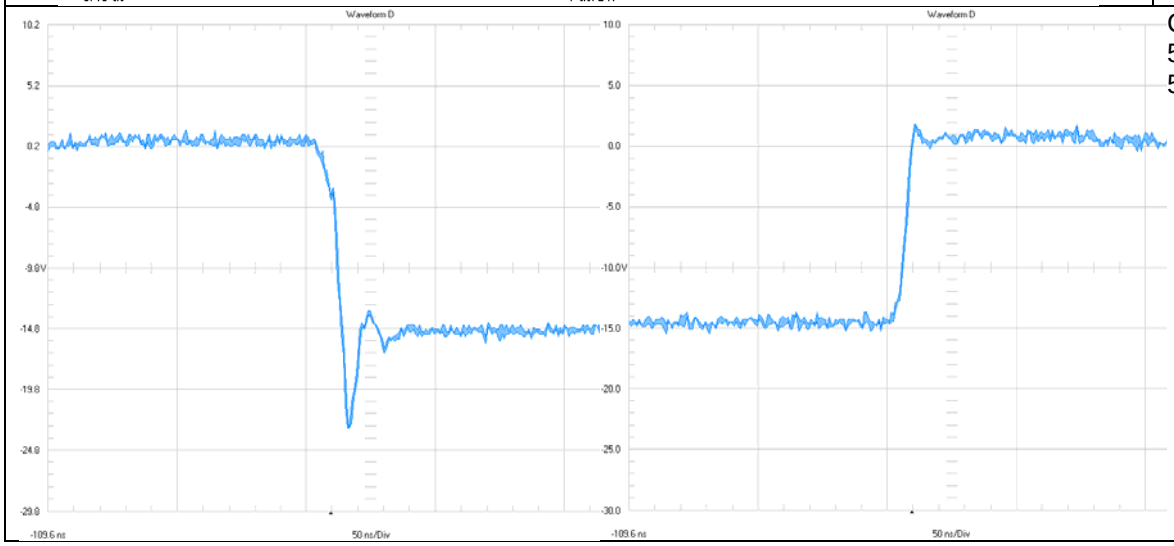
The waveform of the voltage on the switchnode is shown in Figure 25. Input voltage was set to 10V.



Ch1 =>
5V/div

1µs/div

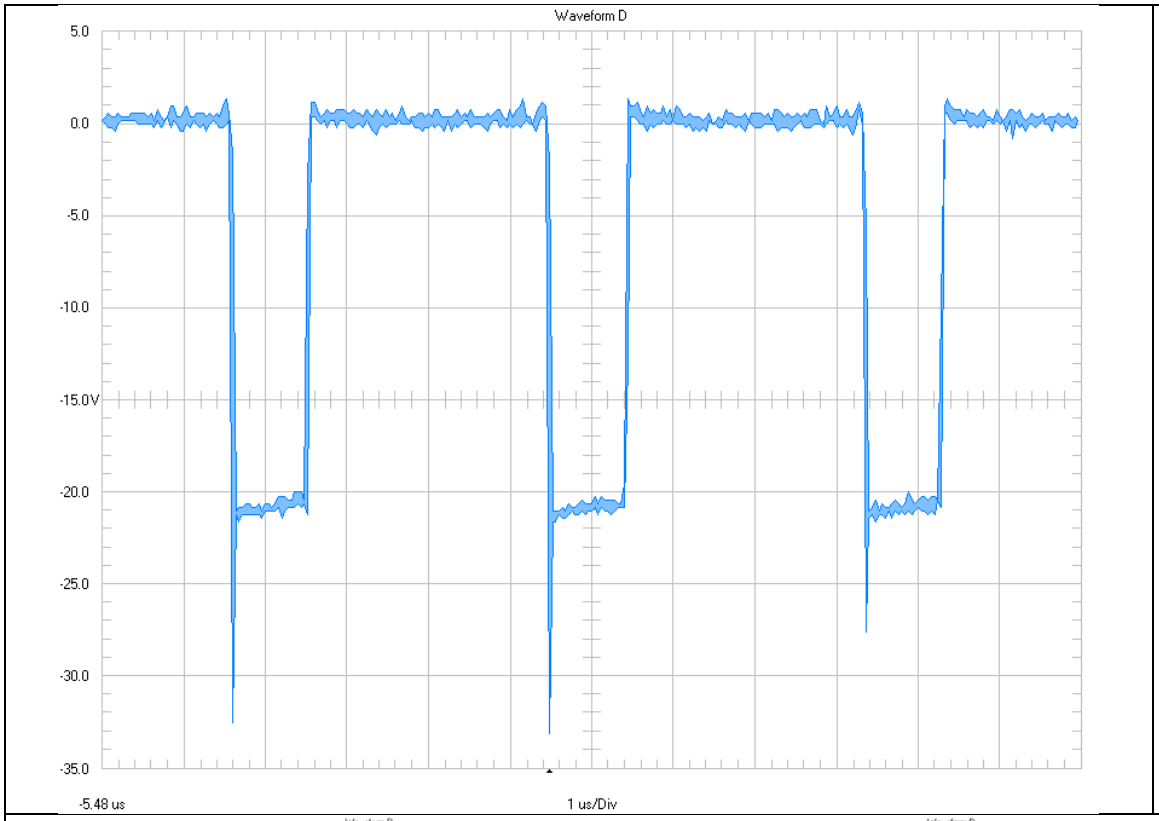
full bandwidth



Ch1 =>
5V/div
50ns/major div

Figure 25

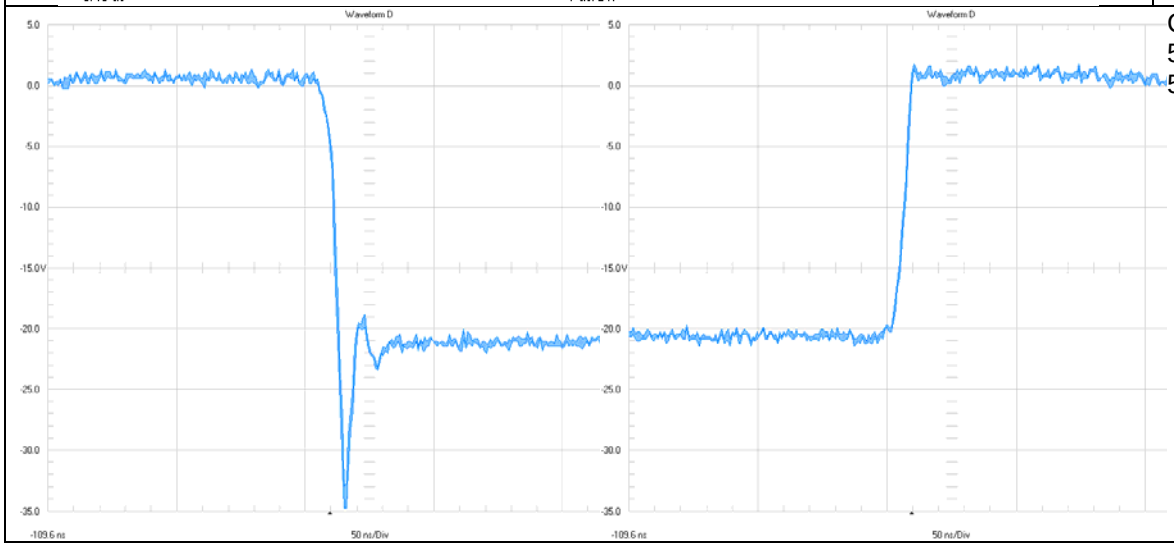
The waveform of the voltage on the switchnode is shown in Figure 26. Input voltage was set to 16V.



Ch1 =>
5V/div

1µs/div

full bandwidth



Ch1 =>
5V/div
50ns/major div

Figure 26

10.2 Q1 Gate – Source

The waveform of the voltage on gate to source is shown in Figure 27. Input voltage was set to 5V.

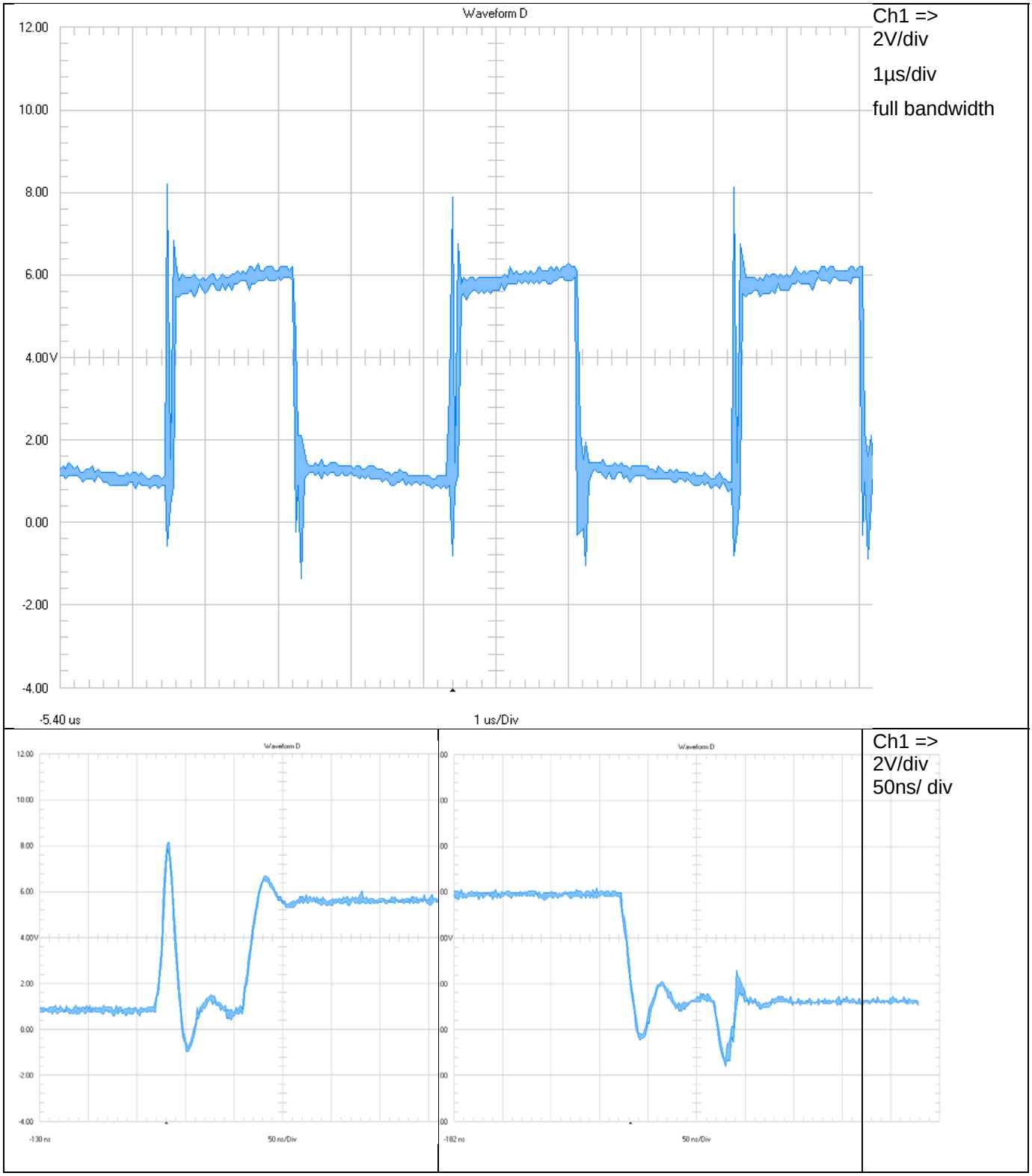
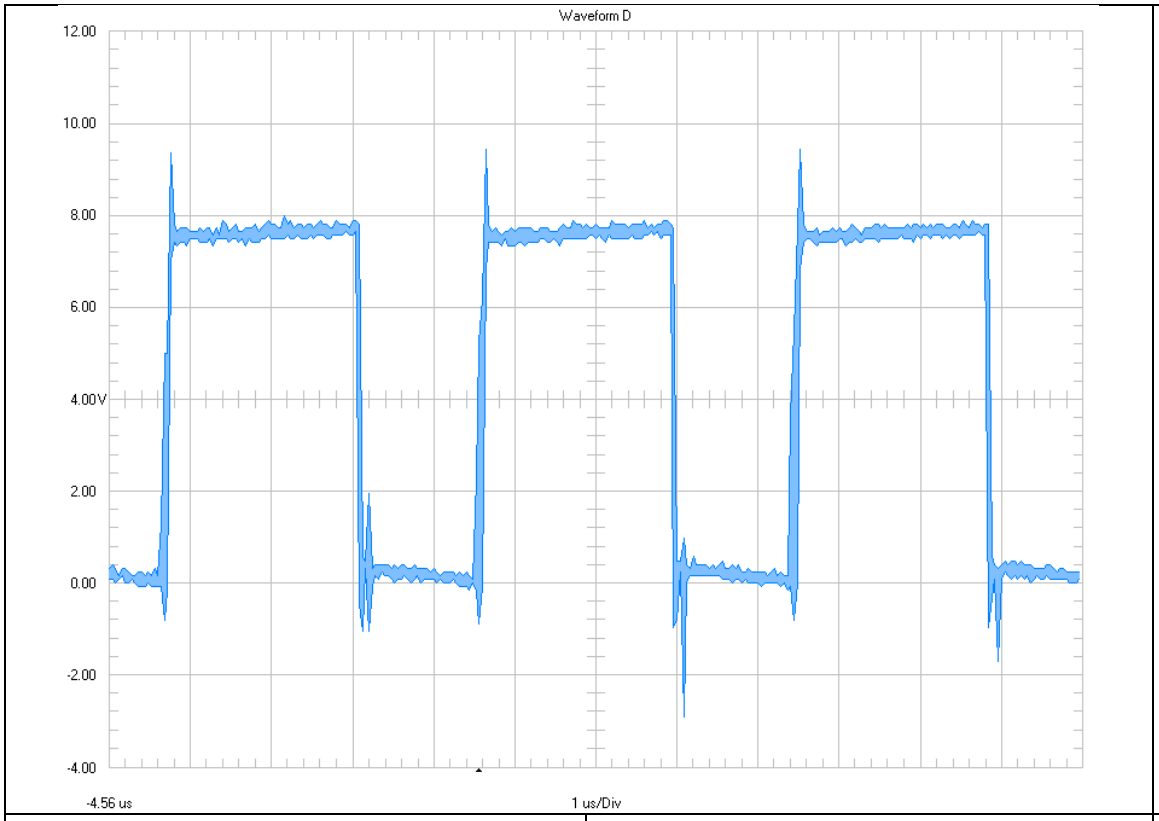


Figure 27

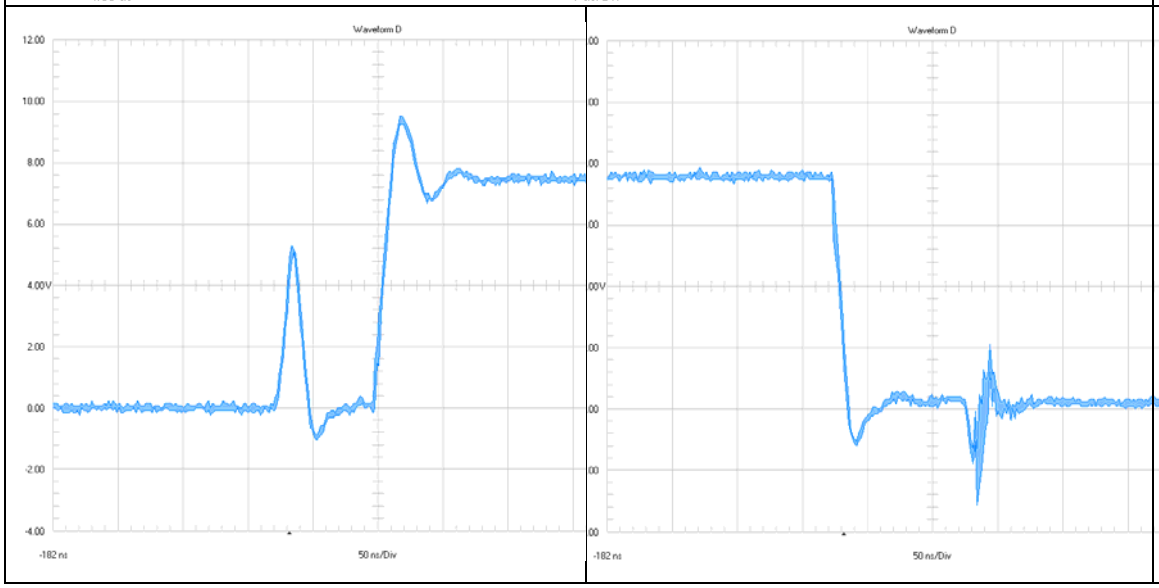
The waveform of the voltage on gate to source is shown in Figure 28. Input voltage was set to 10V.



Ch1 =>
2V/div

1µs/div

full bandwidth



Ch1 =>
2V/div
50ns/ div

Figure 28

The waveform of the voltage on gate to source is shown in Figure 29. Input voltage was set to 16V.

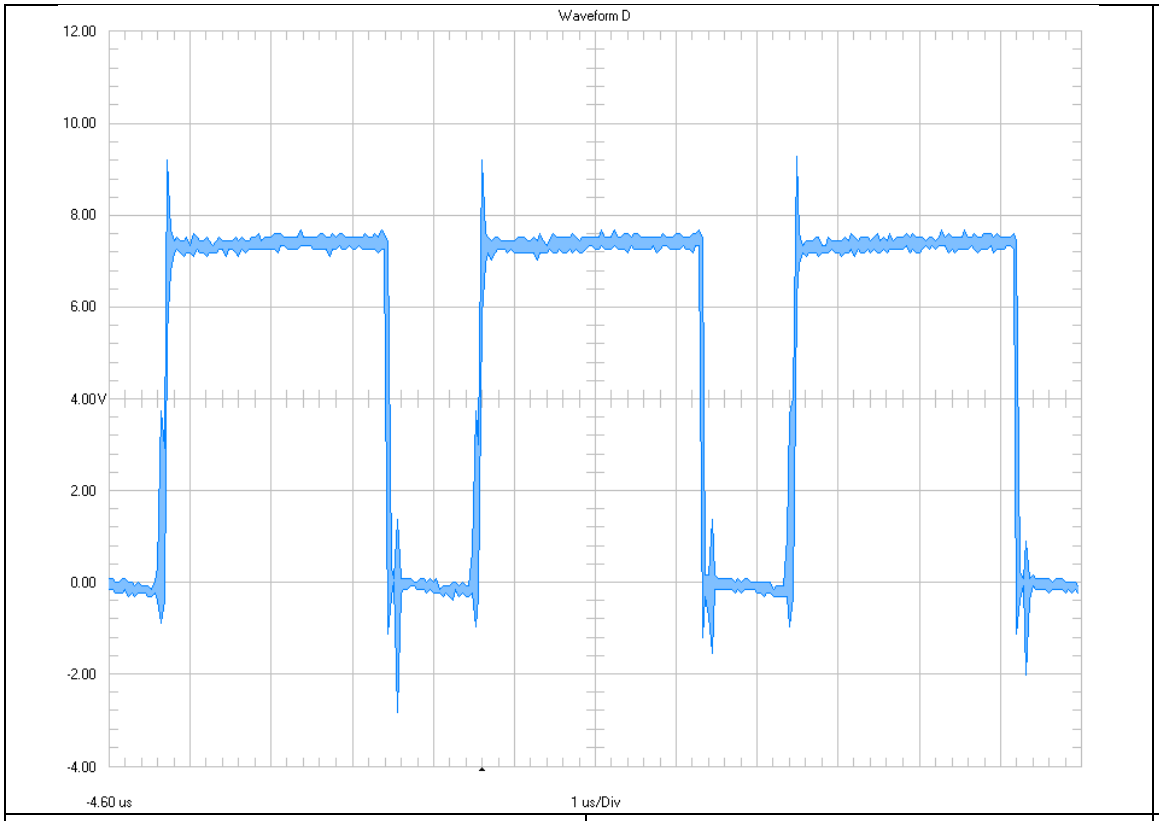
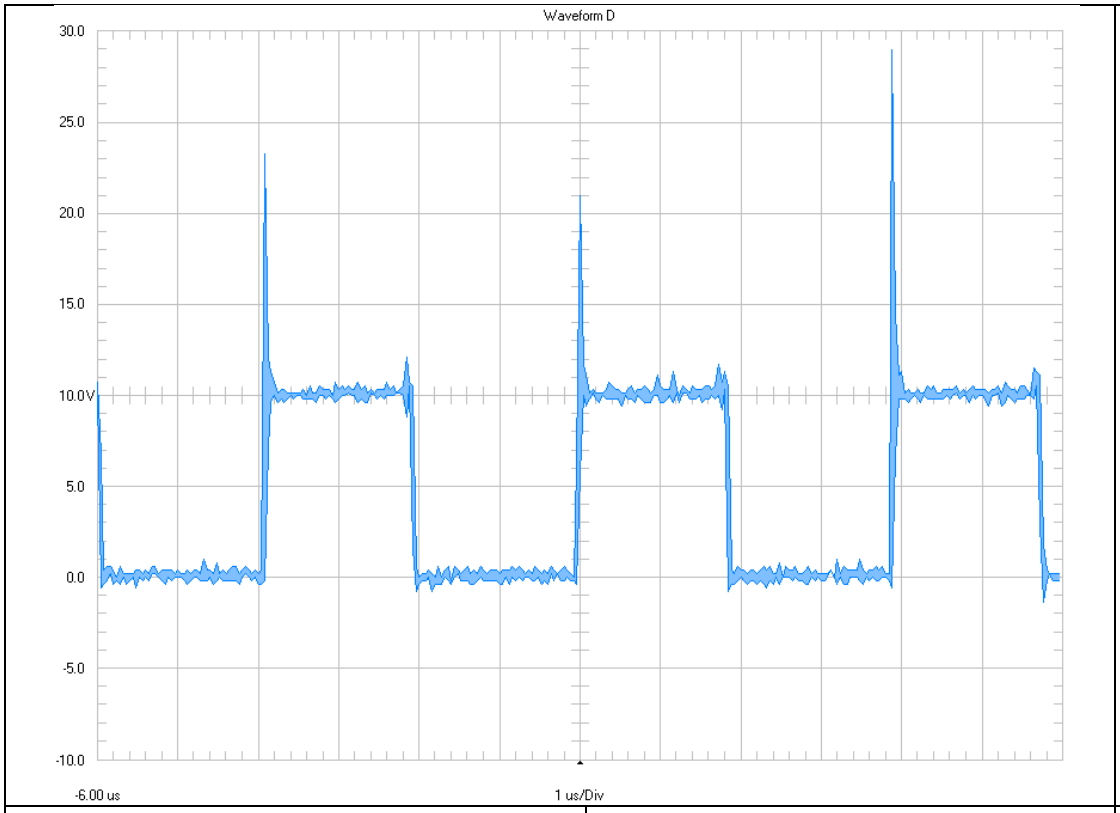


Figure 29

10.3 Q2 switchnode (drain-GND)

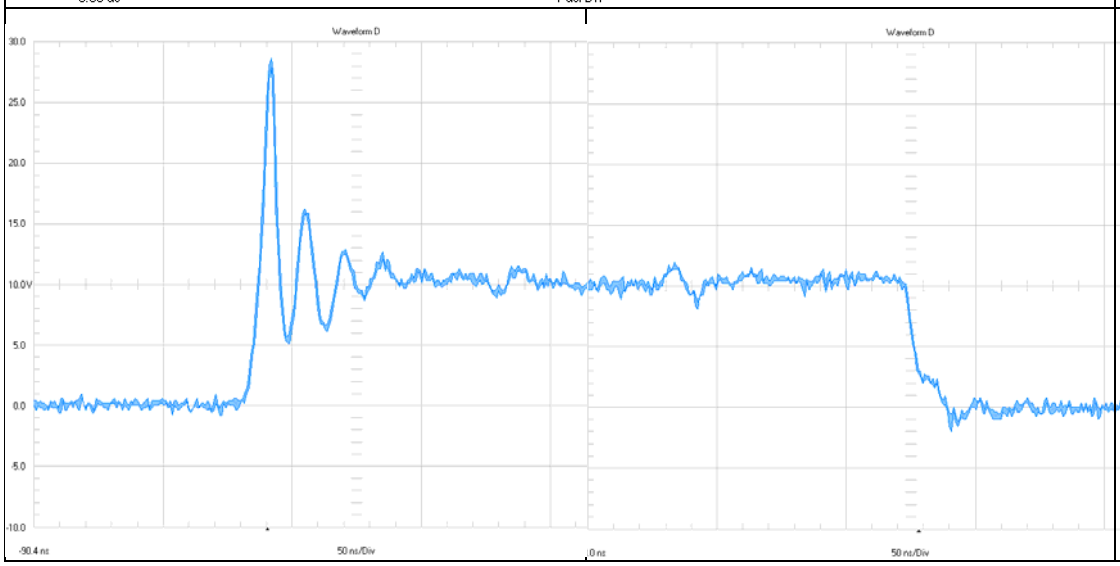
The waveform of the voltage is shown in Figure 30. Input voltage was set to 5V.



Ch1 =>
5V/div

1µs/div

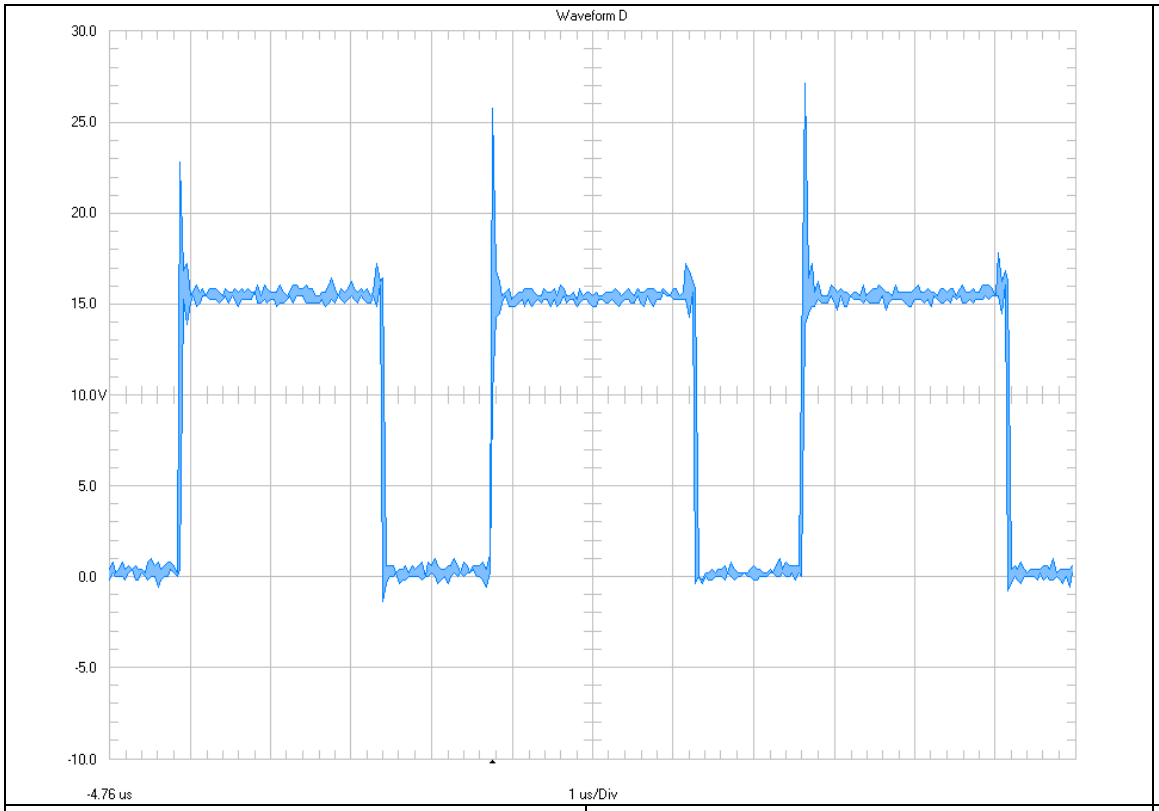
full bandwidth



Ch1 =>
5V/div
50ns/major div

Figure 30

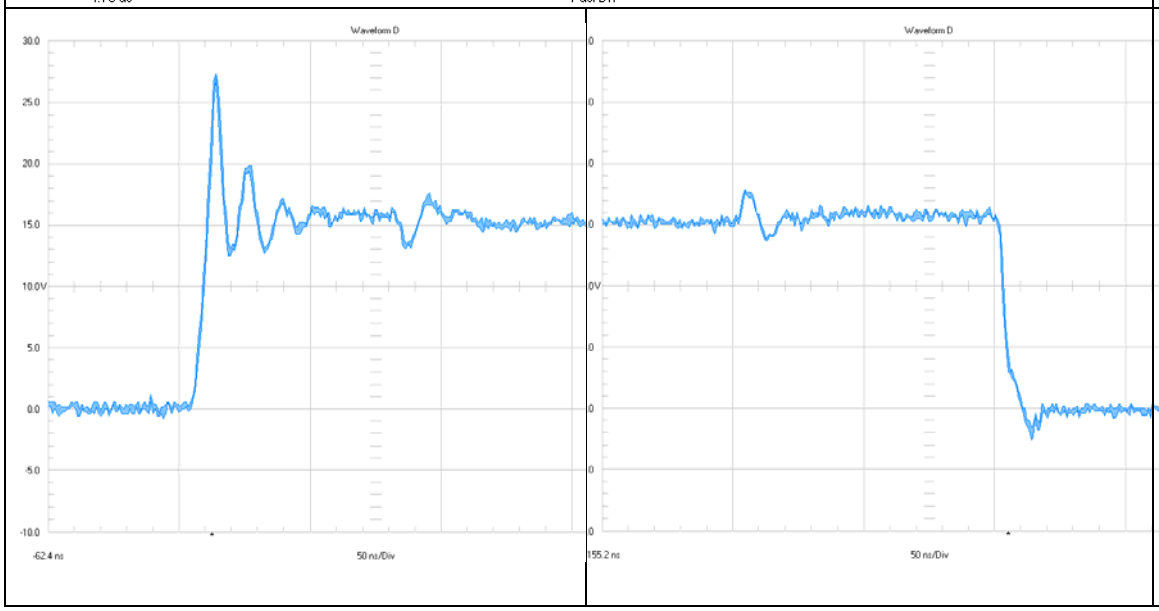
The waveform of the voltage is shown in Figure 31. Input voltage was set to 10V.



Ch1 =>
5V/div

1µs/div

full bandwidth



Ch1 =>
5V/div
50ns/major div

Figure 31

The waveform of the voltage is shown in Figure 32. Input voltage was set to 16V.

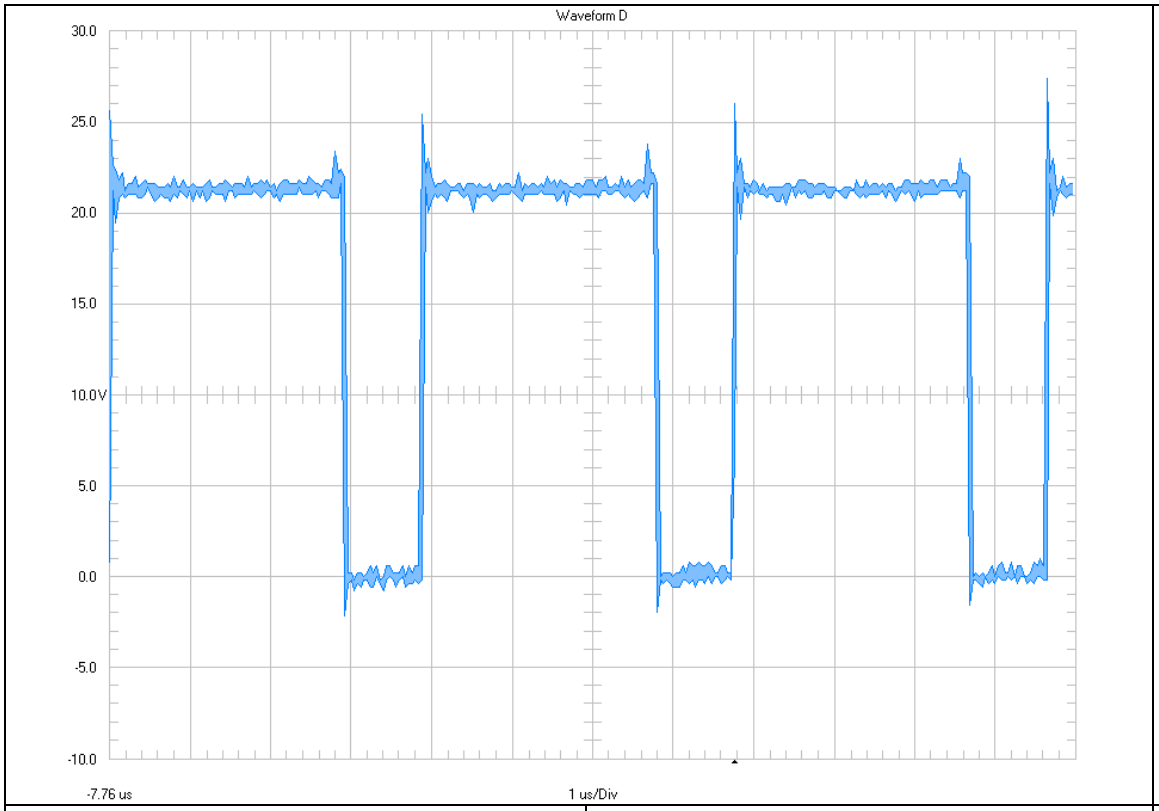
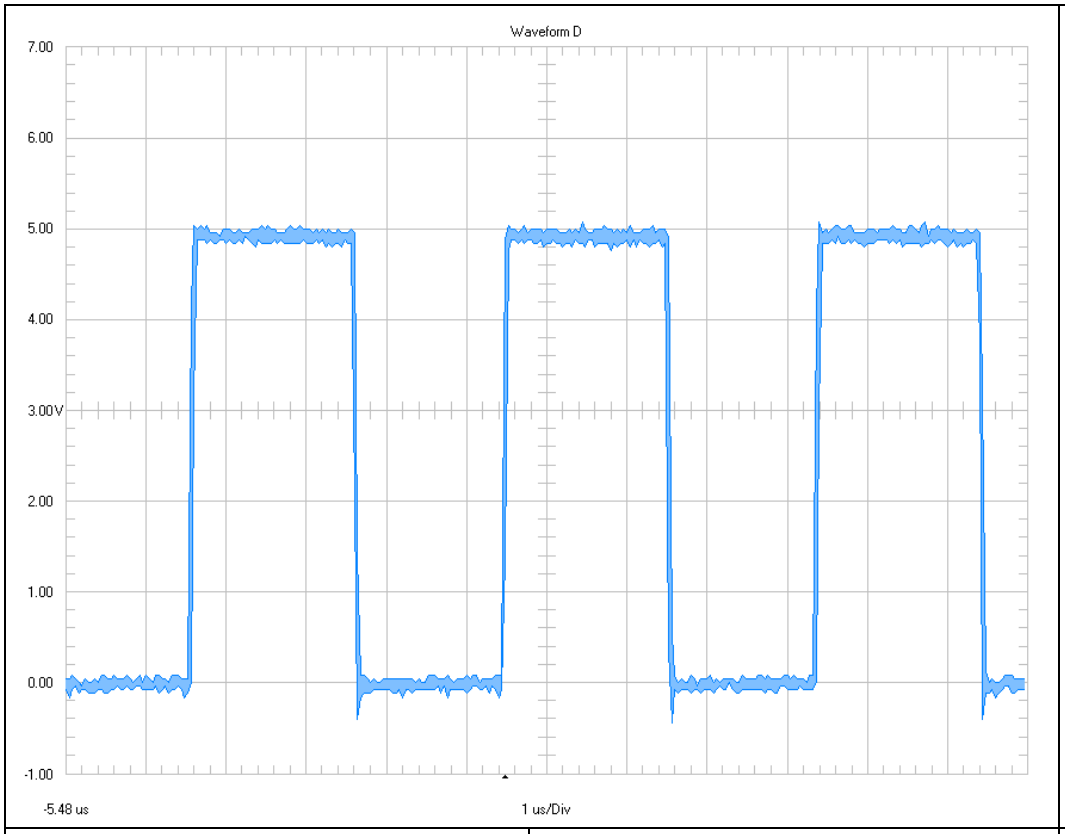


Figure 32

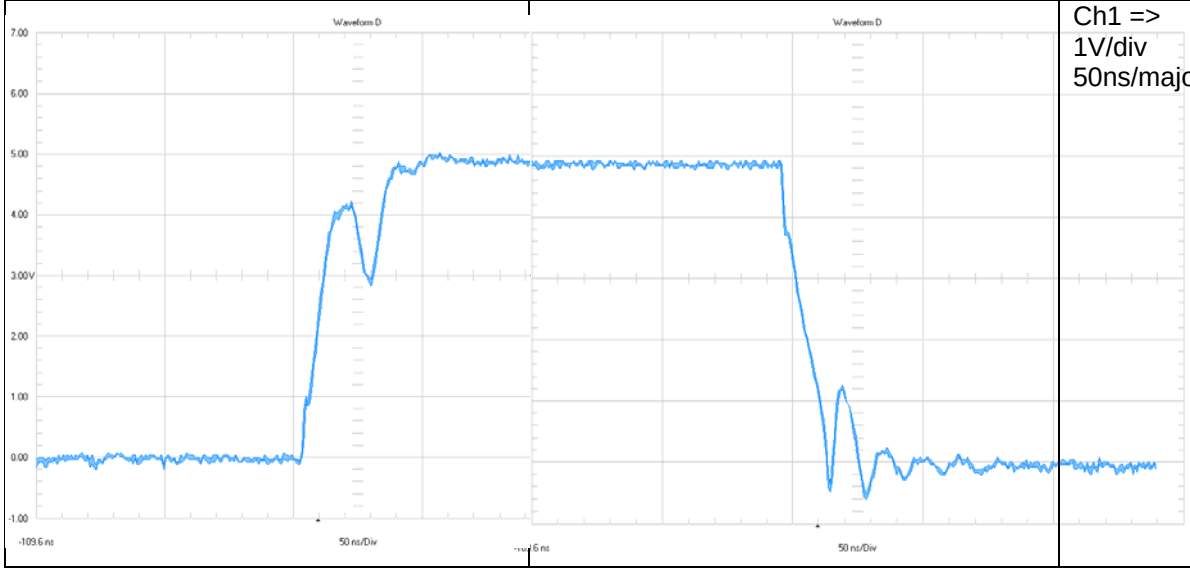
10.4 Q2 Gate-GND

The waveform of the voltage is shown in Figure 33. Input voltage was set to 5V.



Ch1 =>
1V/div

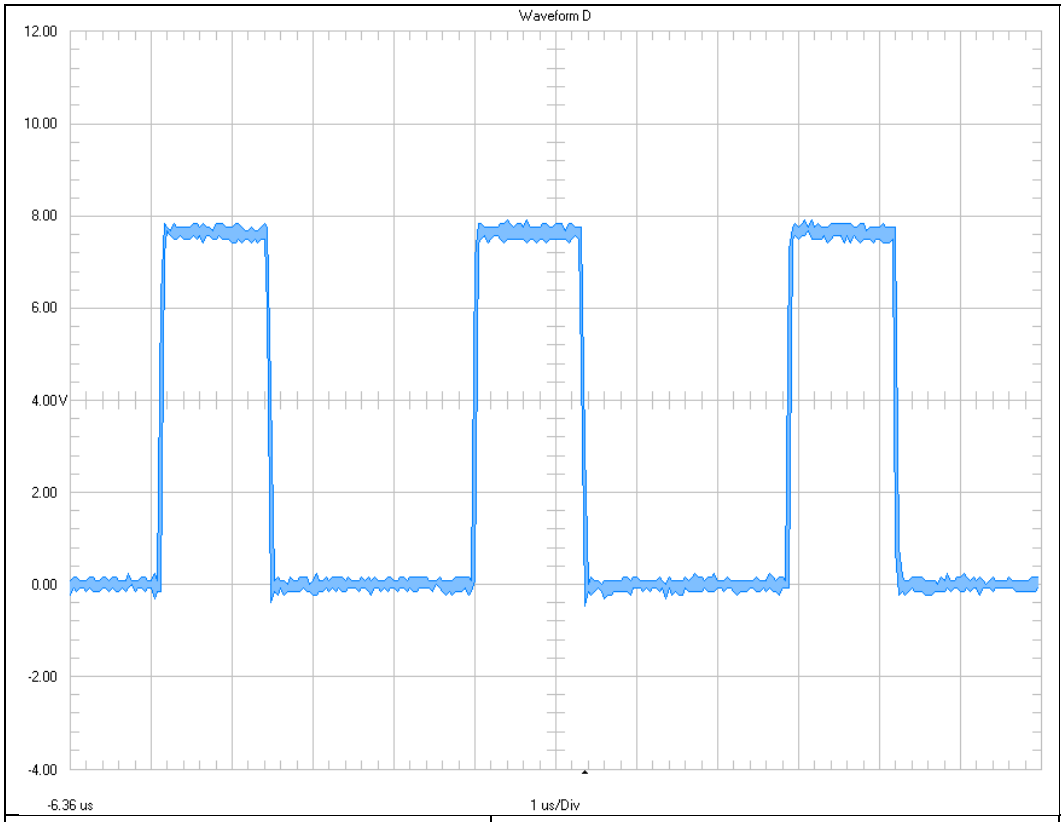
1µs/div
full bandwidth



Ch1 =>
1V/div
50ns/major div

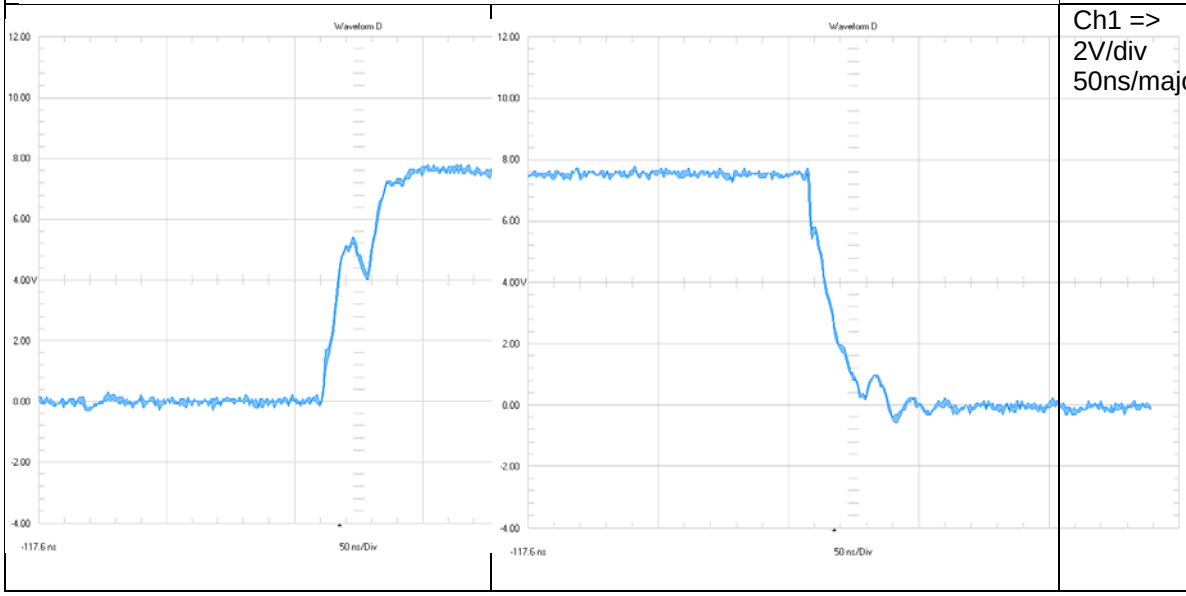
Figure 33

The waveform of the voltage is shown in Figure 34. Input voltage was set to 10V.



Ch1 =>
2V/div

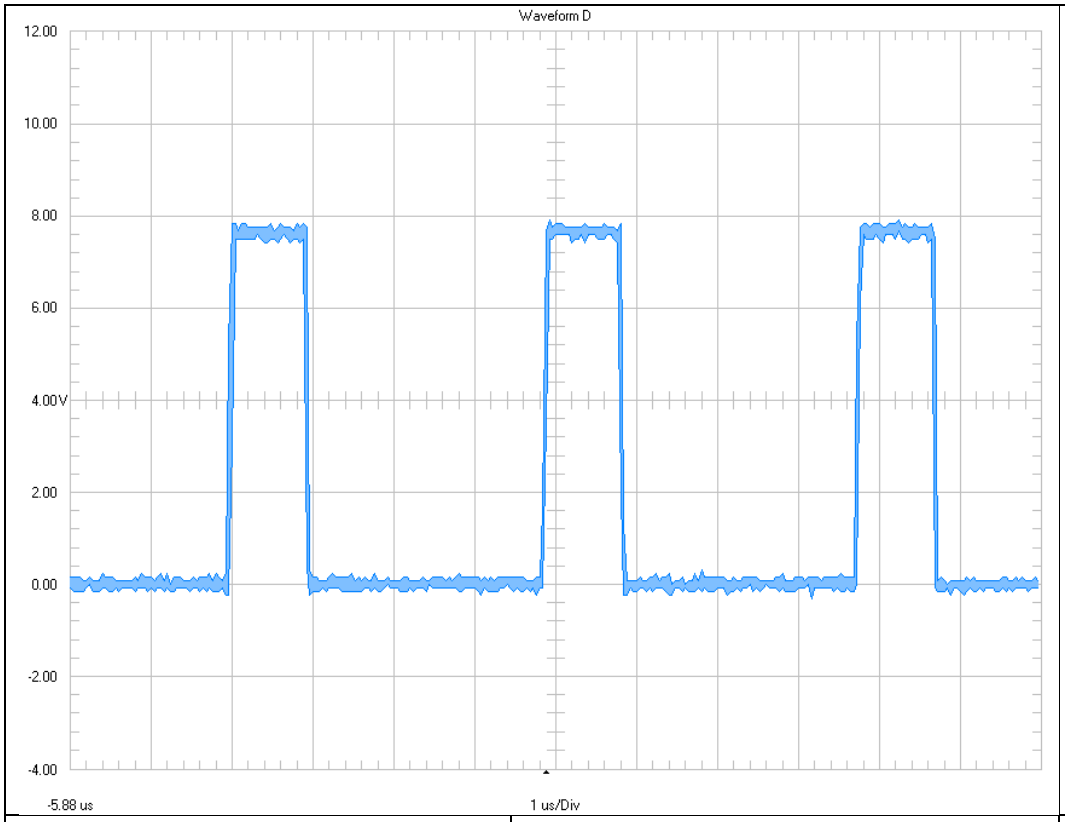
1µs/div
full bandwidth



Ch1 =>
2V/div
50ns/major div

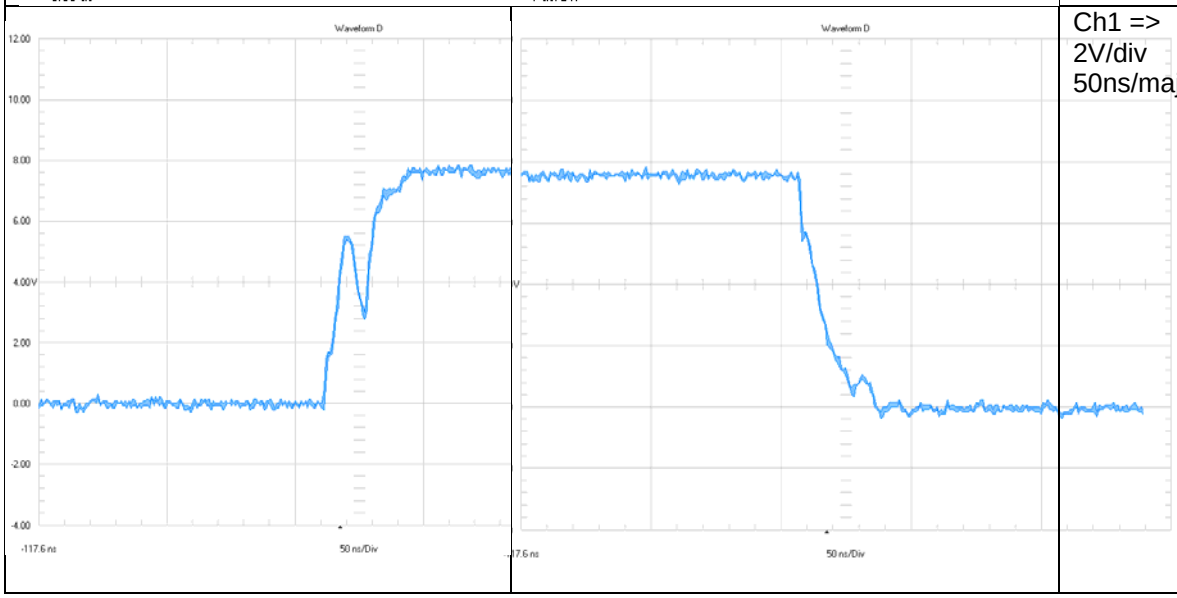
Figure 34

The waveform of the voltage is shown in Figure 35. Input voltage was set to 16V.



Ch1 =>
2V/div

1µs/div
full bandwidth



Ch1 =>
2V/div
50ns/major div

Figure 35

11 Thermal Image

Figure 36 shows the thermal image at 5V input voltage and 3A output current.

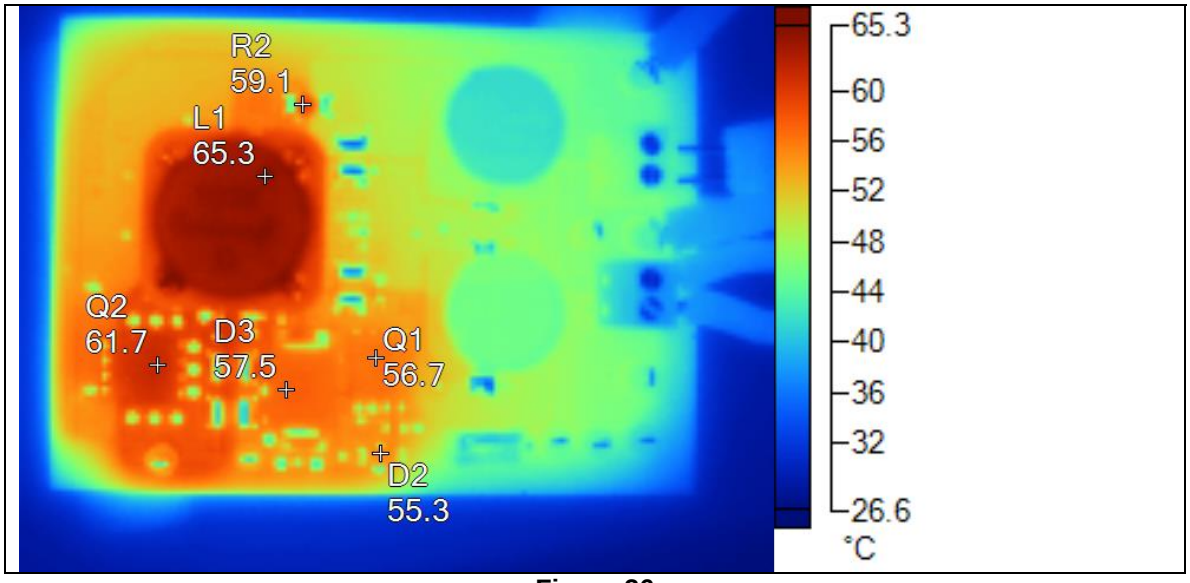


Figure 36

Name	Temperature
L1	65.3°C
Q2	61.7°C
R2	59.1°C
D3	57.5°C
Q1	56.7°C
D2	55.3°C

Figure 37 shows the thermal image at 10V input voltage and 3A output current.

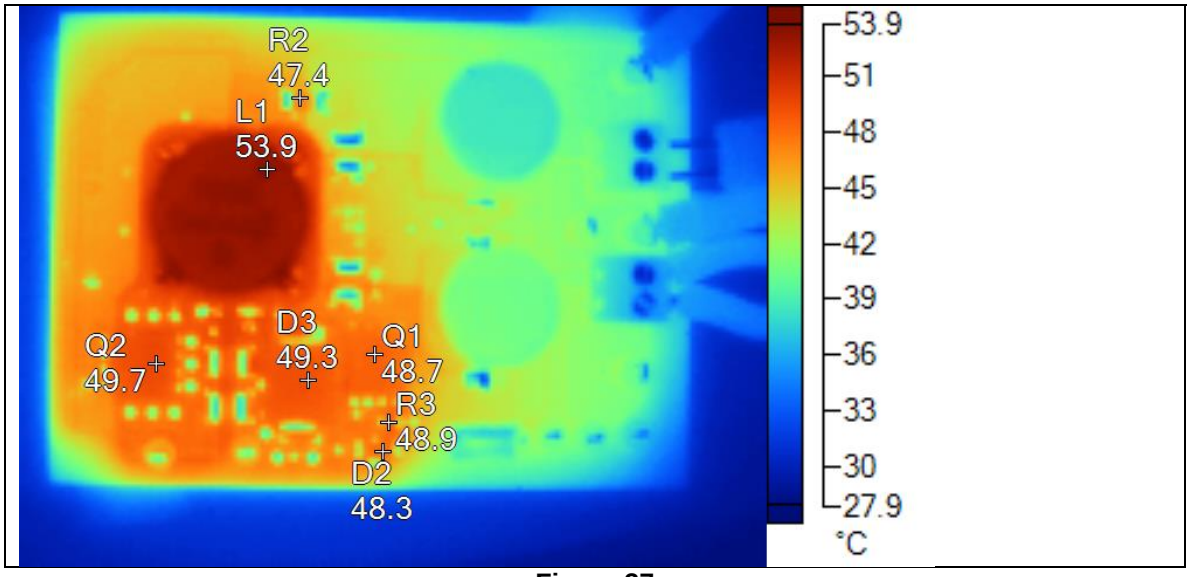


Figure 37

Name	Temperature
L1	53.9°C
Q2	49.7°C
D3	49.3°C
R3	48.9°C
Q1	48.7°C
D2	48.3°C
R2	47.4°C

Figure 38 shows the thermal image at 16V input voltage and 3A output current.

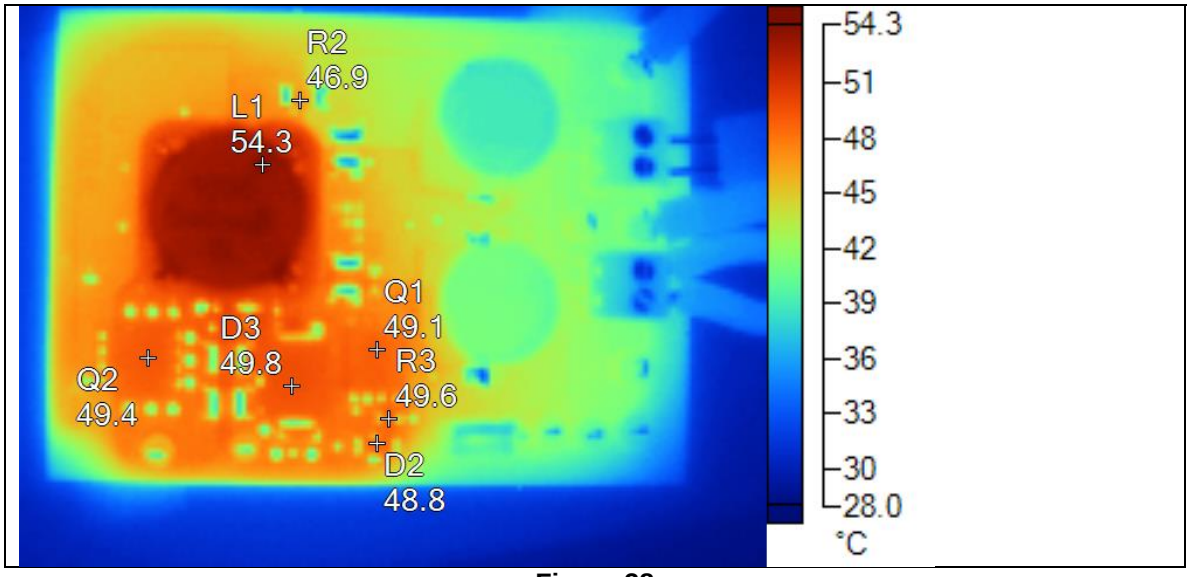


Figure 38

Name	Temperature
L1	54.3°C
D3	49.8°C
R3	49.6°C
Q2	49.4°C
Q1	49.1°C
D2	48.8°C
R2	46.9°C

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265