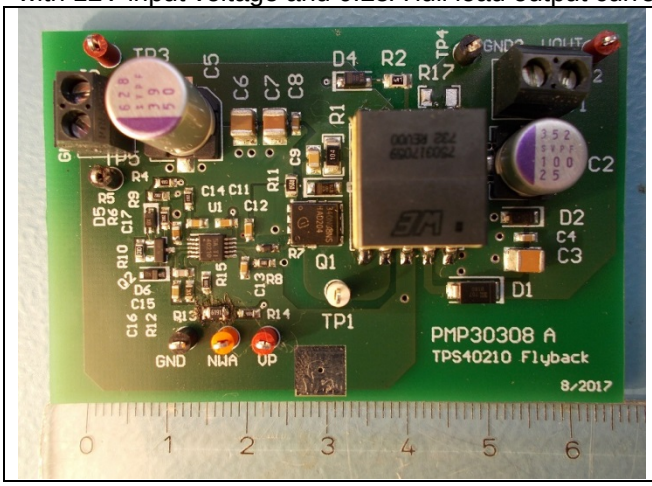
PMP30336RevB Test Results

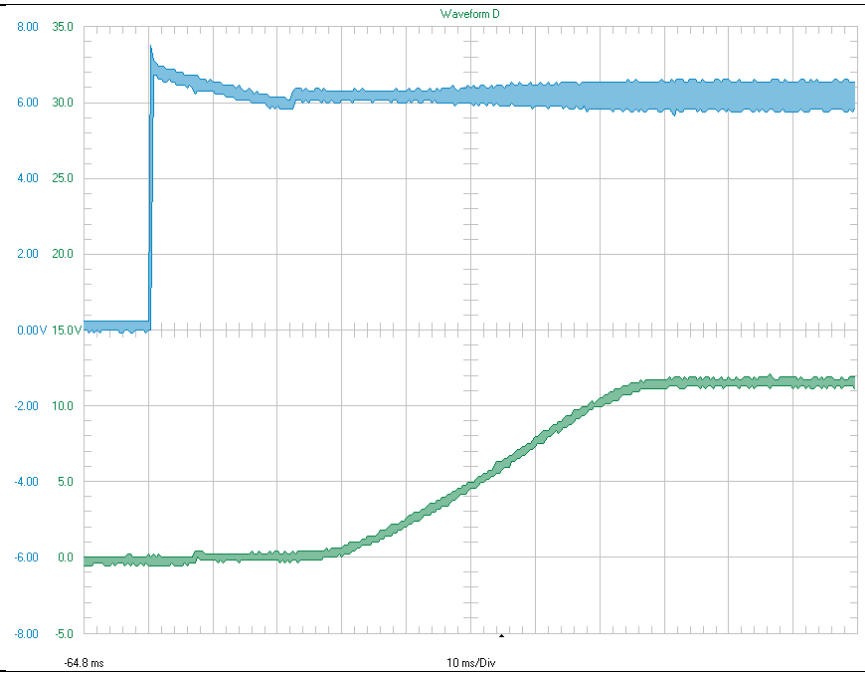
Topology: Flyback (DCM)
Device: TPS40210
Fsw: approx.. 200kHz, measured 203kHz; ON @ 6.06V, OFF @ 5.66V

Unless otherwise mentioned all measurements were done
with 12V input voltage and 0.25A lull load output current (resistive load).



1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set to 6V. Power supply was connected.



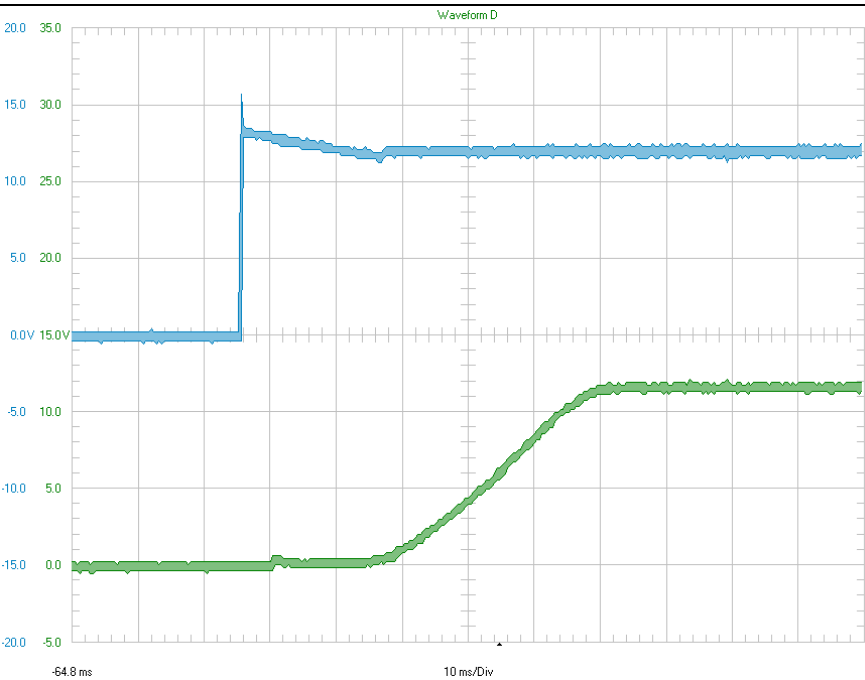
Ch1=> input voltage
2V/div

Ch2=> output voltage
5V/div

10ms/div

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set to 12V. Power supply was connected.



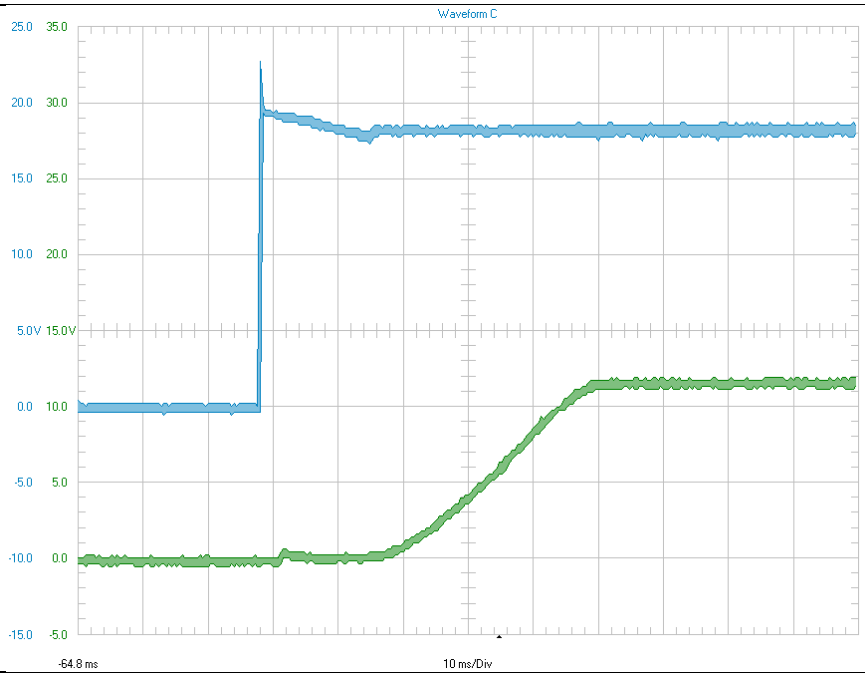
Ch1=> input voltage
5V/div

Ch2=> output voltage
5V/div

10ms/div

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set to 18V.Power supply was connected.



Ch1=> input voltage 5V/div

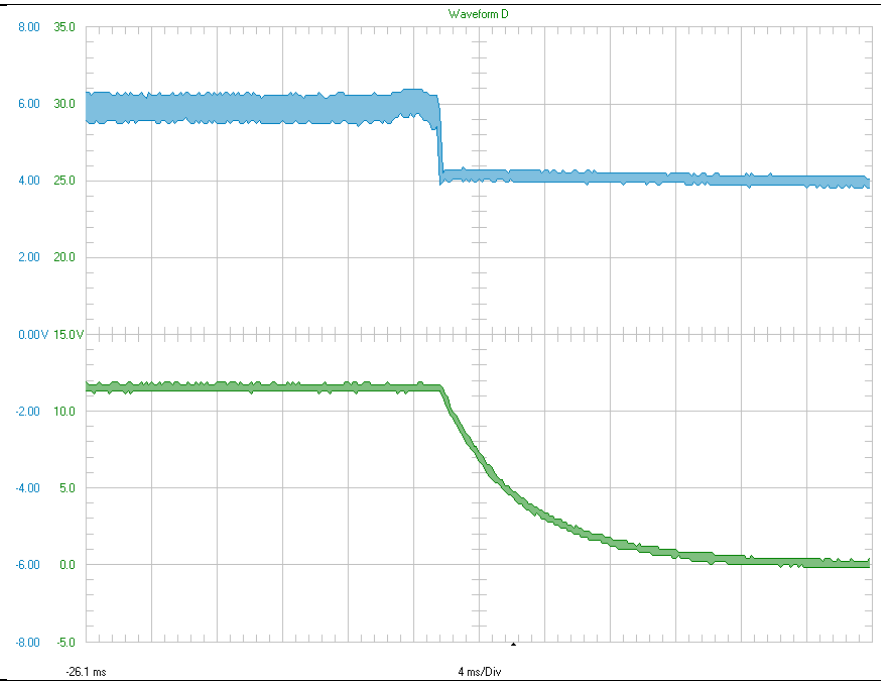
Ch2=> output voltage 5V/div

10ms/div

Figure 3

2 Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set to 6V. Power supply was disconnected



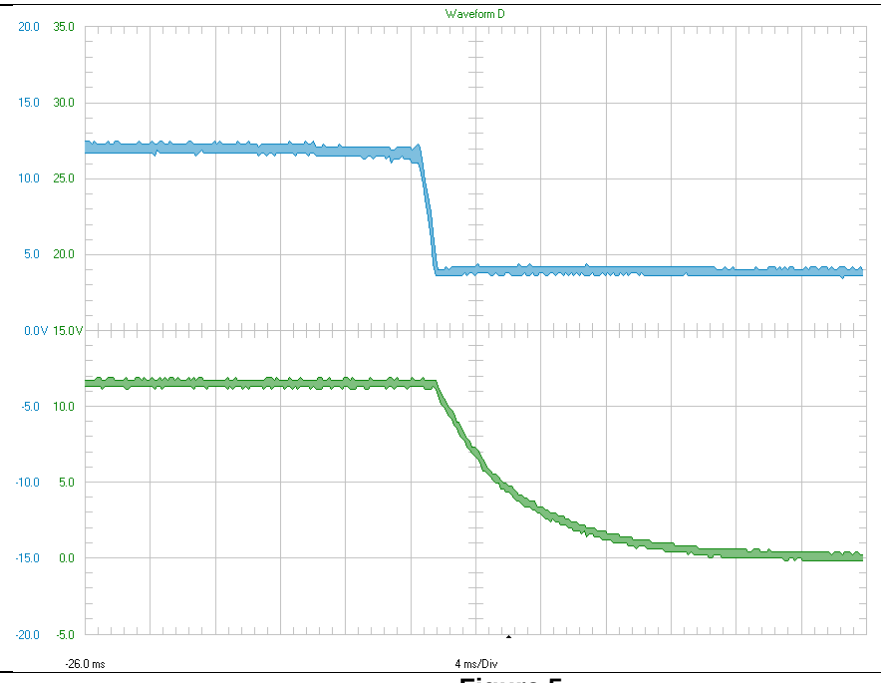
Ch1=> input voltage 2V/div

Ch2=> output voltage 5V/div

4ms/div

Figure 4

The shutdown waveform is shown in the Figure 5. The input voltage was set to 12V. Power supply was disconnected



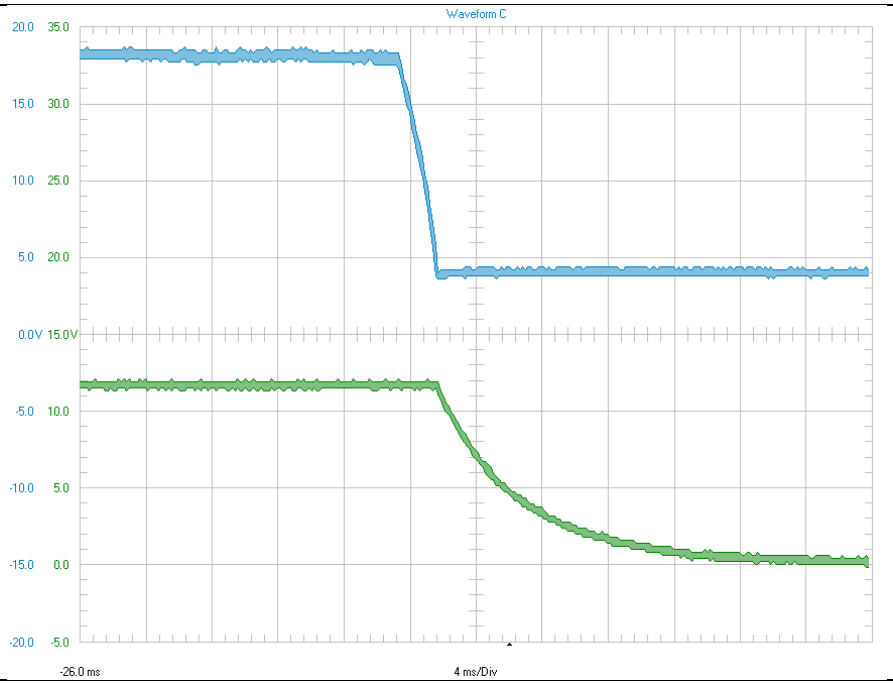
Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

4ms/div

Figure 5

The shutdown waveform is shown in the Figure 4. The input voltage was set to 18V. Power supply was disconnected



Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

4ms/div

Figure 6

3 Efficiency

The efficiency is shown in the Figure 7 below, at 12Vin/18Vin tested up to 500mA load

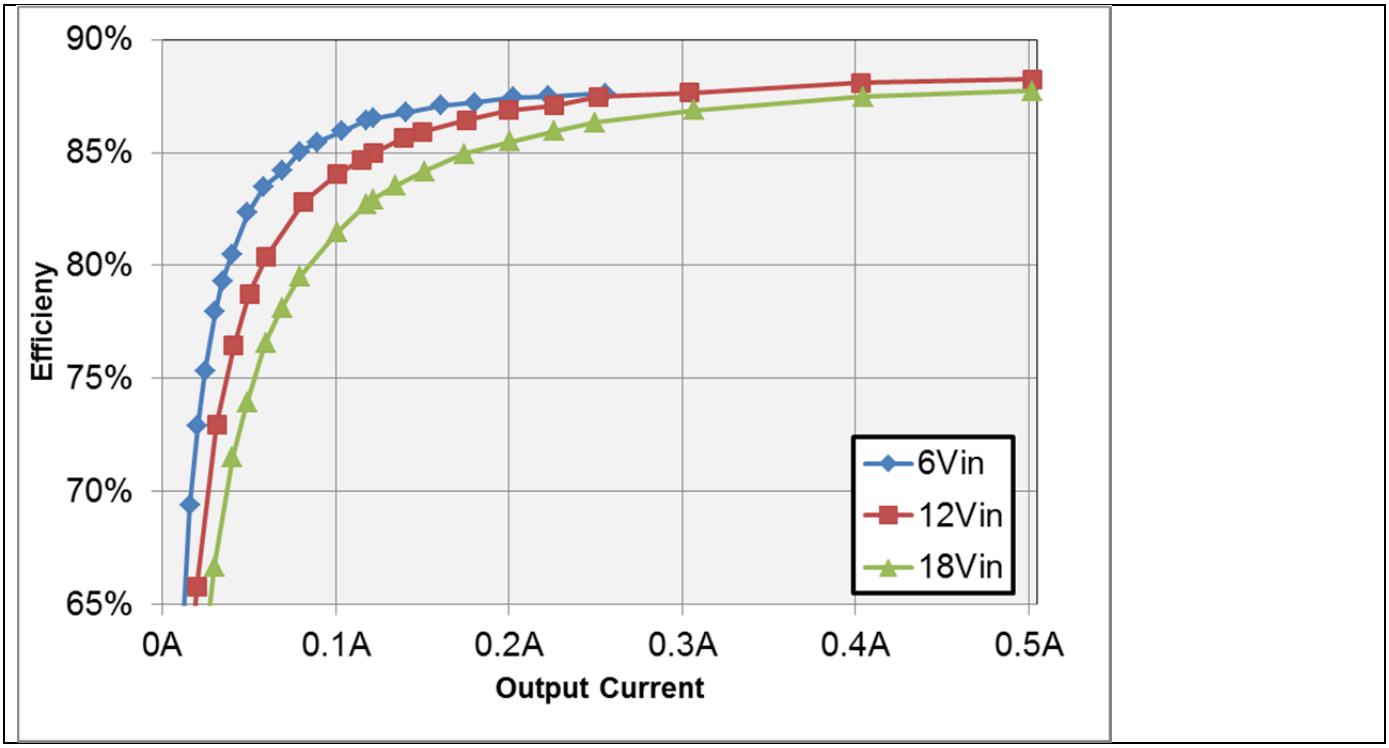


Figure 7

The loss (PIN - POUT) is shown in Figure 8

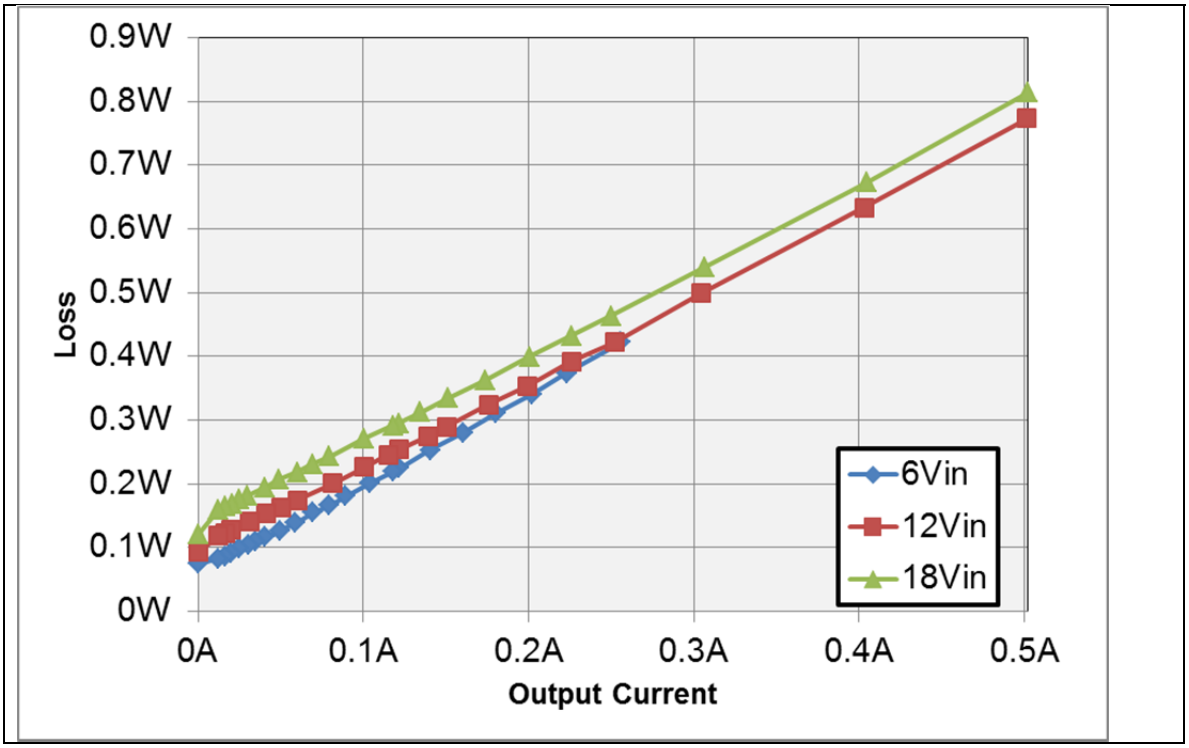


Figure 8

4 Load Regulation

The load regulation of the output is shown in the Figure 9 below.

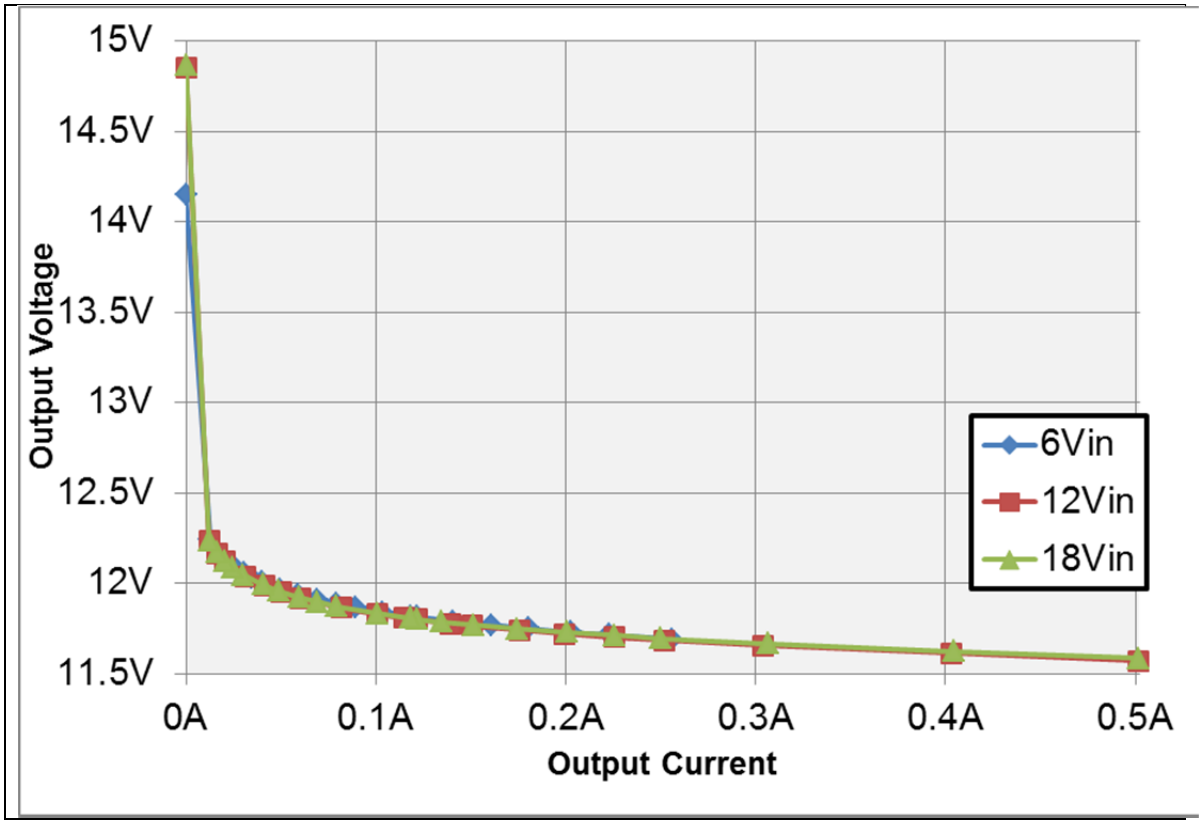


Figure 9

primary side regulation needs a minimum load > 5mA

5 Line Regulation

Figure 10 shows the line regulation with a load current of 0.25A

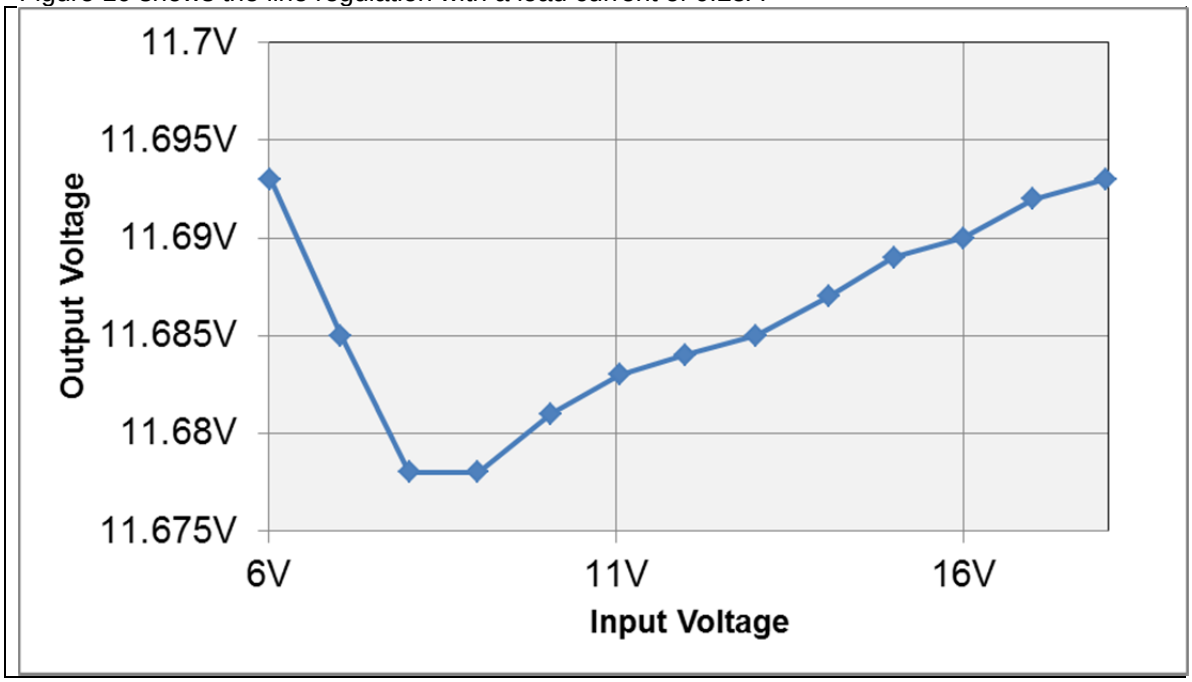


Figure 10

Efficiency and loss were calculated and is shown in Figure 11

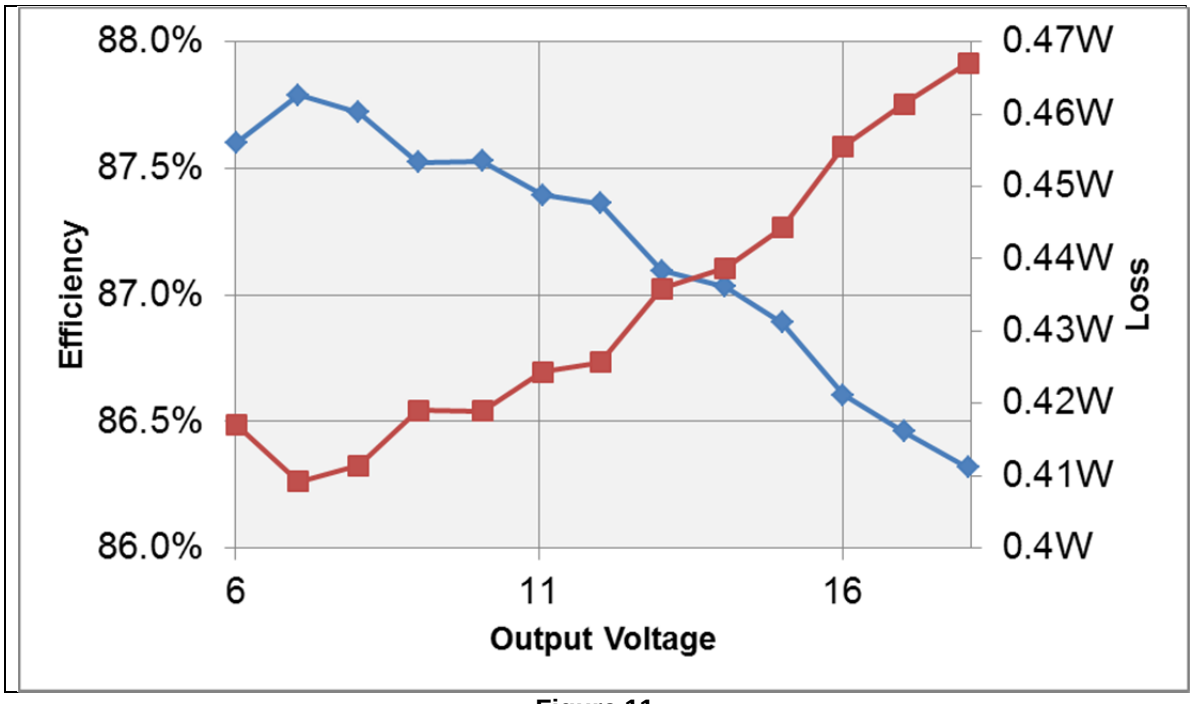
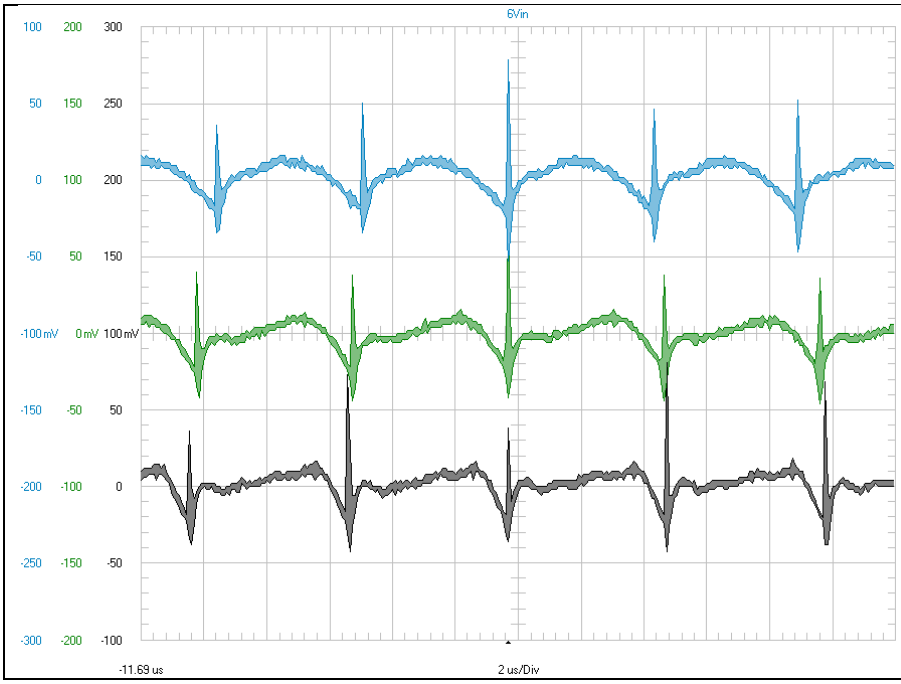


Figure 11

6 Ripple Voltage

6.1 Input

The input ripple voltage is shown in Figure 12.



Ch1 => input voltage 6V 50mV/div

Ch2 => input voltage 12V 50mV/div

Ch3 => input voltage 18V 50mV/div

AC coupled

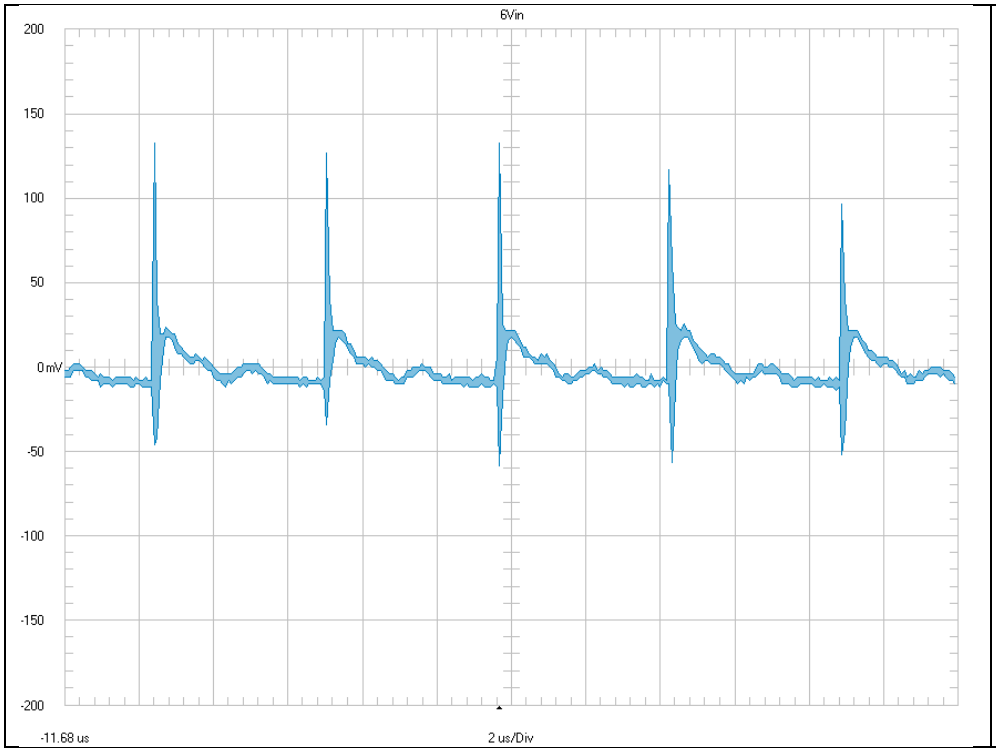
20MHz bandwidth setting

2µs/div

Figure 12

6.2 Output

The output ripple voltage is shown in Figure 13. The input voltage is set to 6V.



Ch1 => output voltage

50mV/div

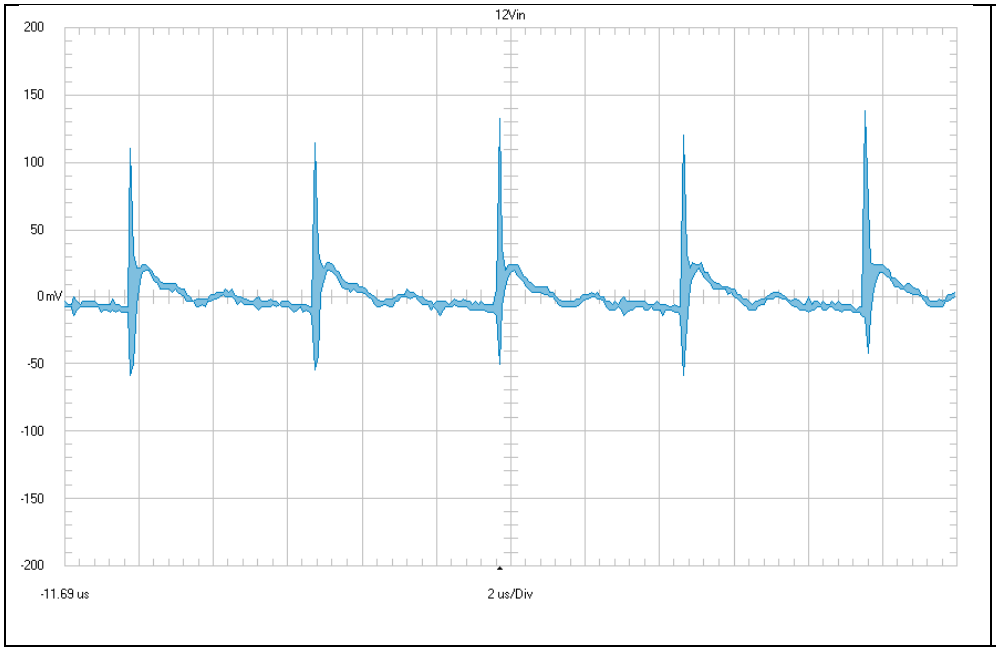
AC coupled

20MHz bandwidth setting

2µs/div

Figure 13

The output ripple voltage is shown in Figure 14. The input voltage is set to 12V.



Ch1 => output voltage

50mV/div

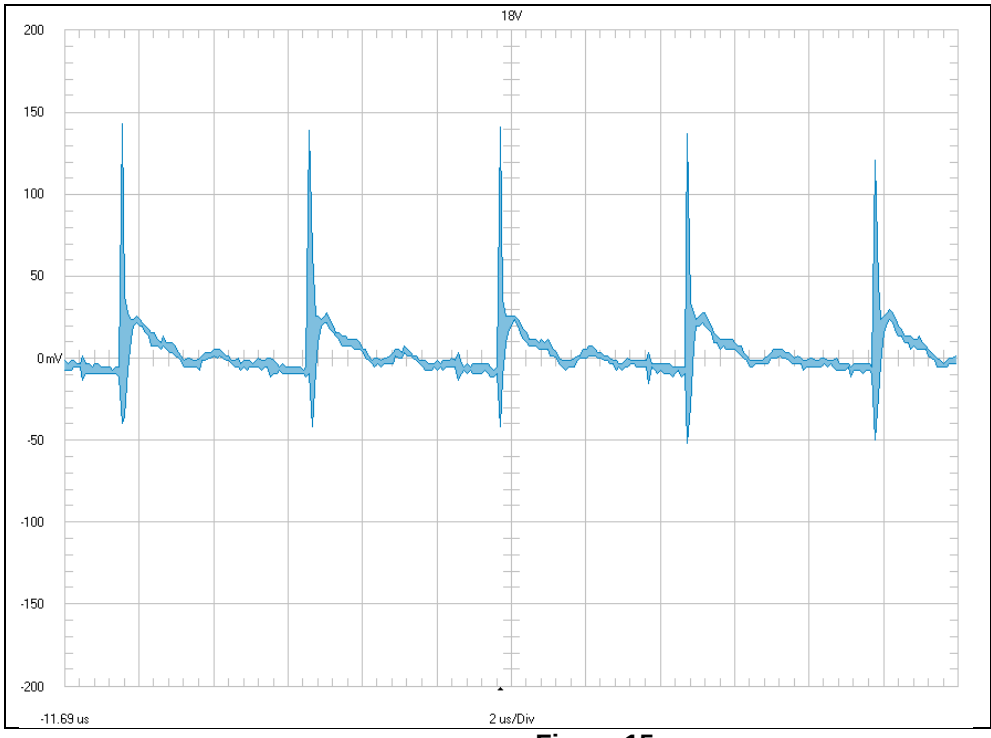
AC coupled

20MHz bandwidth setting

2µs/div

Figure 14

The output ripple voltage is shown in Figure 15. The input voltage is set to 18V.



Ch1 => output voltage

50mV/div

AC coupled

20MHz bandwidth setting

2µs/div

Figure 15

7 Control Loop Frequency Response

Figure 16 shows the loop response with 0.25A load and 6V input.

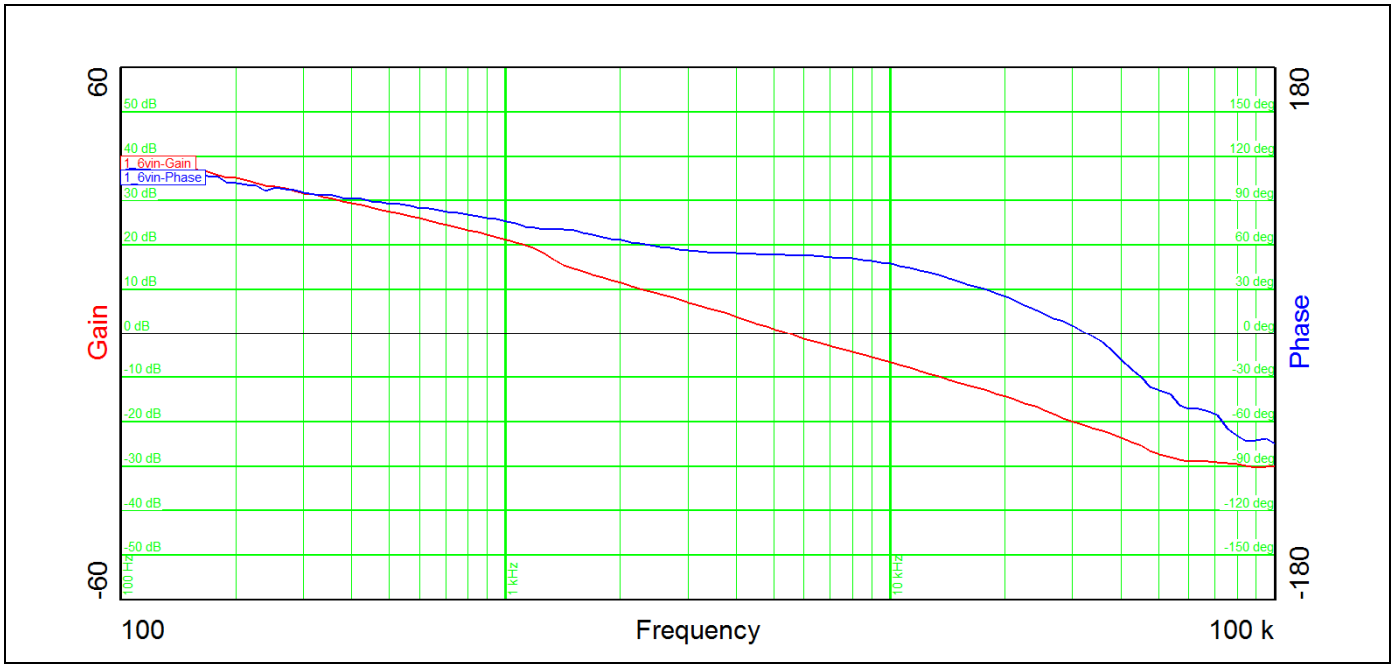


Figure 16

Figure 17 shows the loop response with 0.25A load and 12V input.

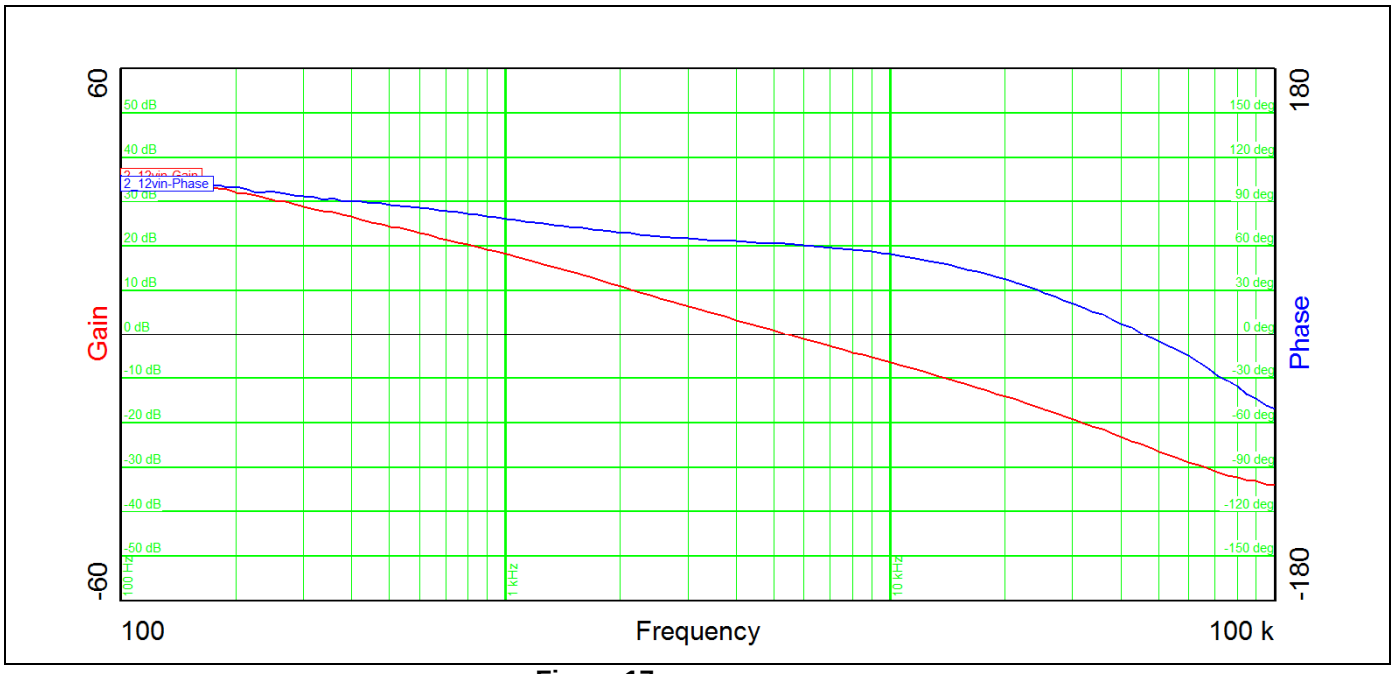


Figure 17

Figure 18 shows the loop response with 0.25A load and 18V input.

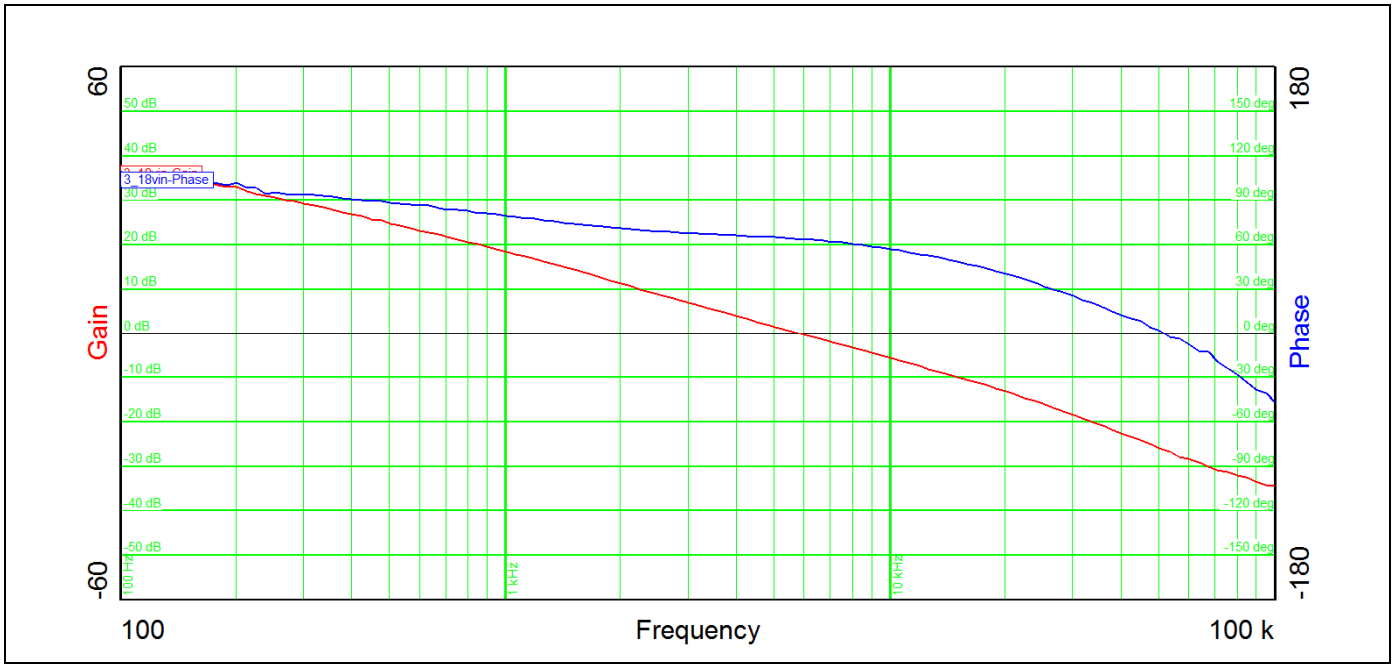


Figure 18

Table 1 summarizes the results

	6V	12V	18V
Bandwidth (kHz)	5.42	5.42	5.8
Phasemargin	53°	61°	64°
slope (20dB/decade)	-1.36	-1.24	-1.21
gain margin (dB)	-21.1	-21.1	-26.4
slope (20dB/decade)	-1.45	-1.45	-1.89
freq (kHz)	32.7	32.7	51.8

Table 1

8 Load Transients

The Figure 19 shows the response to load transients. The load is switching from 0.125A to 0.25A (30 Hz with electronic load N3305A). The input voltage was set to 6V.

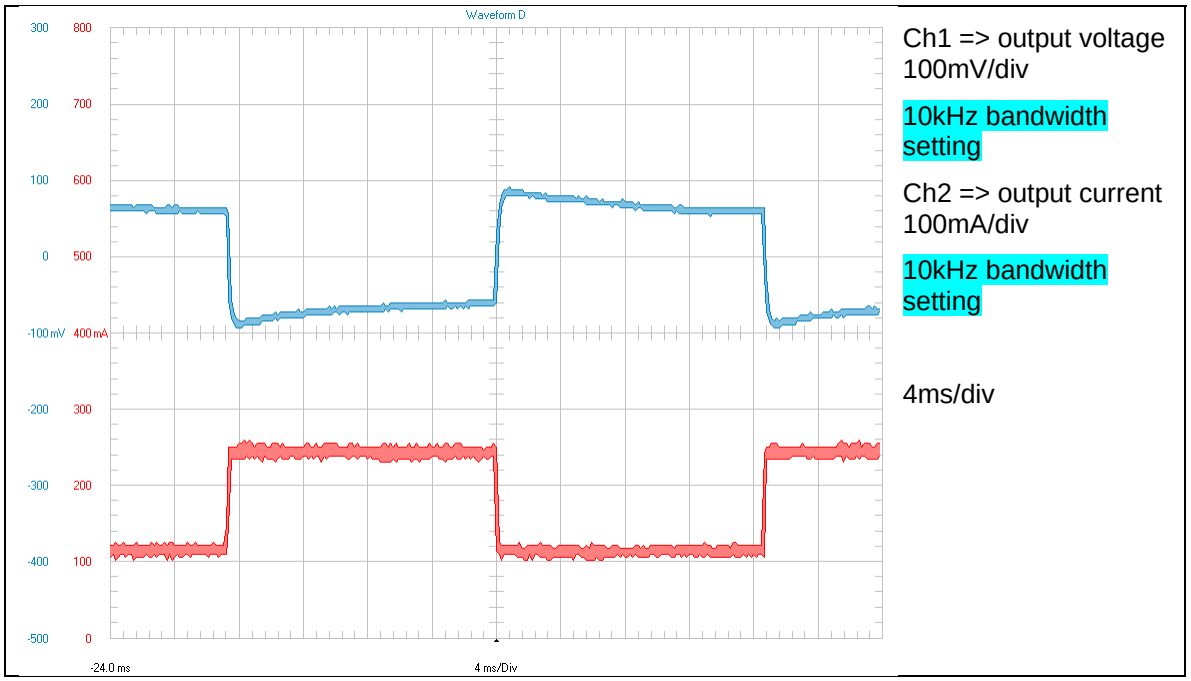


Figure 19

The Figure 20 shows the response to load transients. The load is switching from 0.125A to 0.25A (30 Hz with electronic load N3305A). The input voltage was set to 12V.

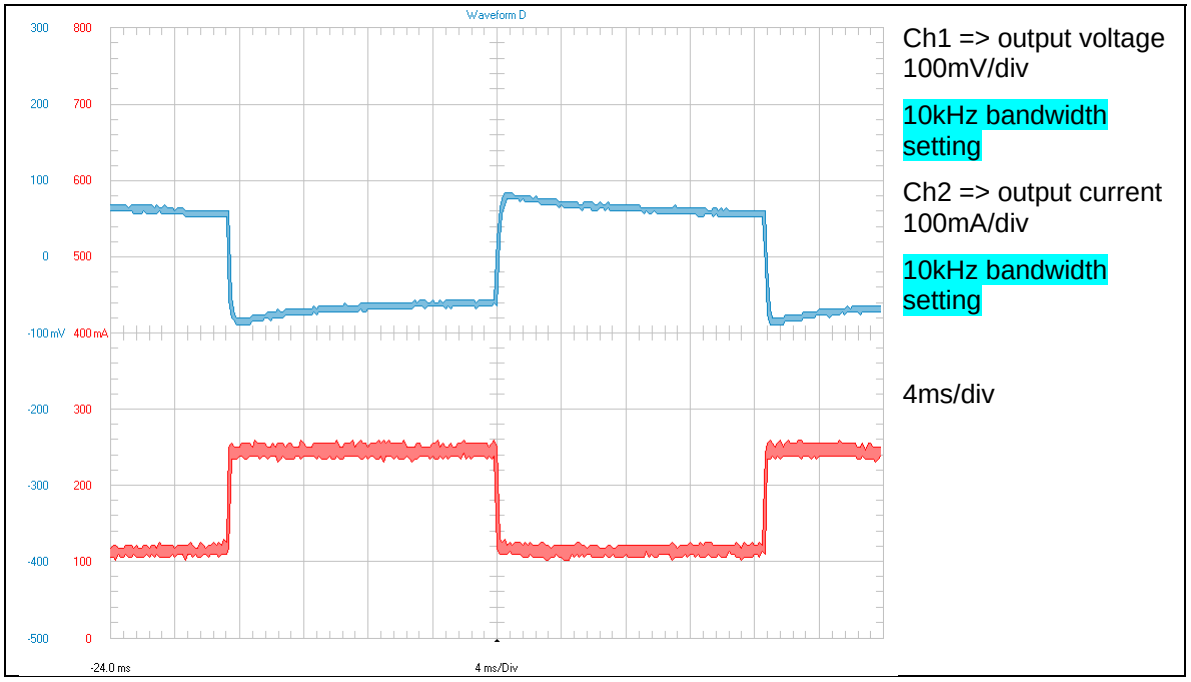


Figure 20

The Figure 21 shows the response to load transients. The load is switching from 0.125A to 0.25A (30 Hz with electronic load N3305A). The input voltage was set to 18V.

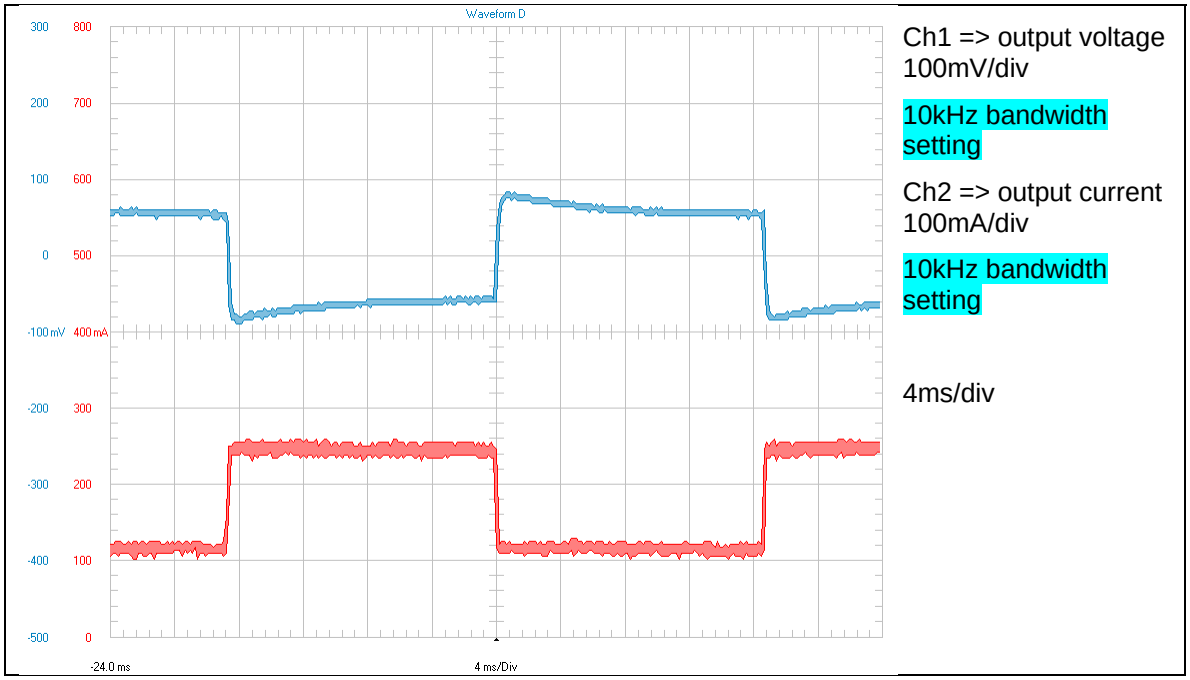


Figure 21

the DC error is related to primary side regulation

9 Miscellaneous Waveforms

9.1 Switch

Waveform at the switchnode (Q1 to GND) is shown in Figure 22

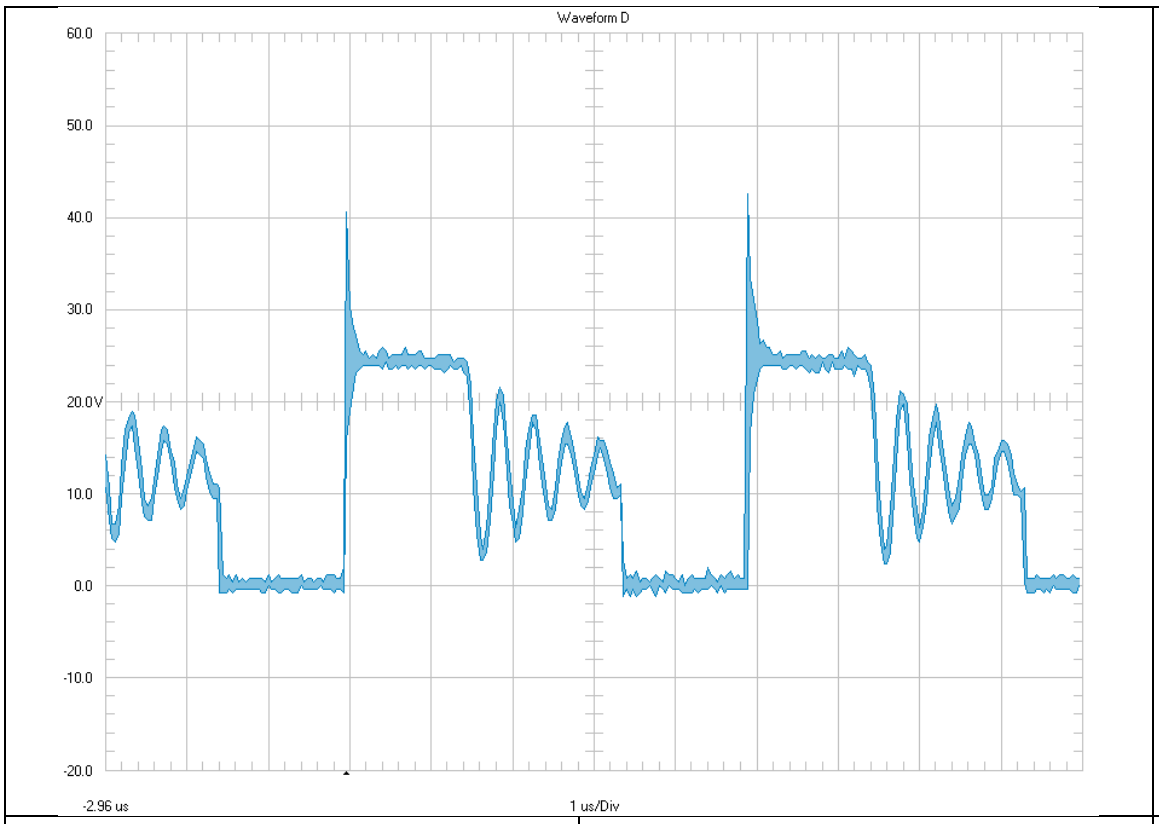
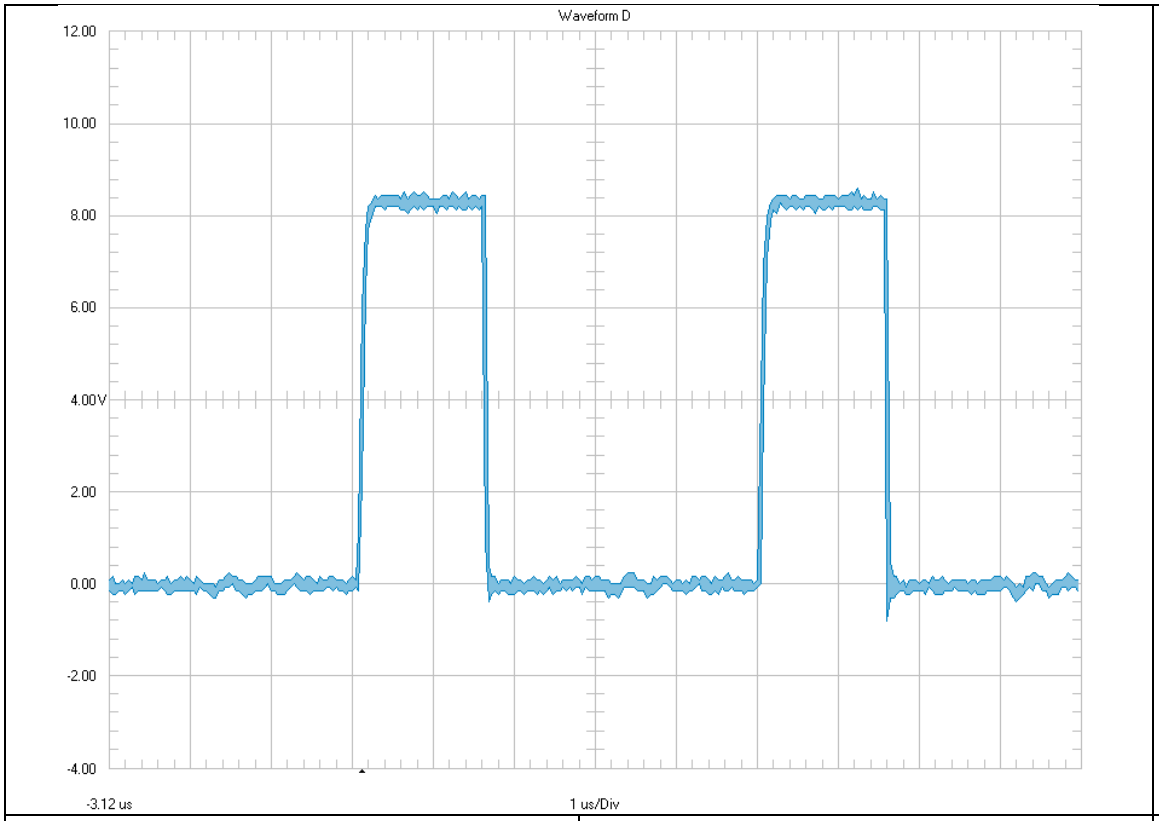


Figure 22

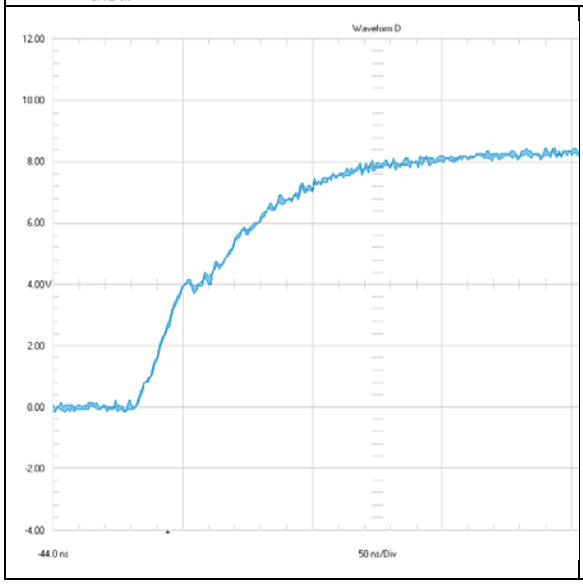
9.2 Gate to GND

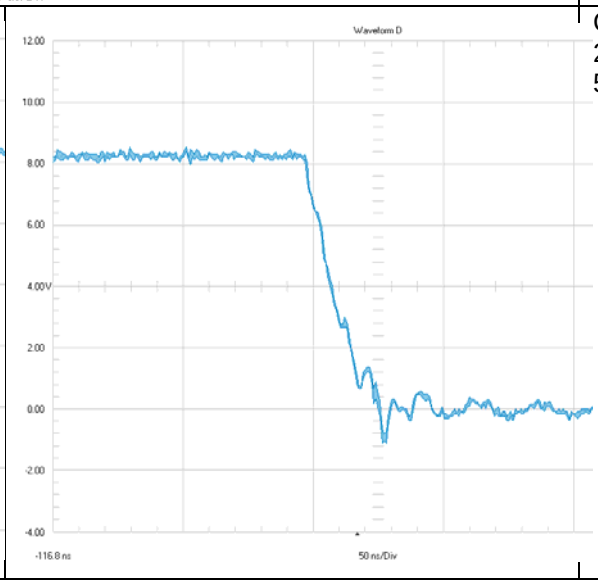
Waveform from gate to ground is shown in Figure 23



Ch1 =>
2V/div

1µs/div



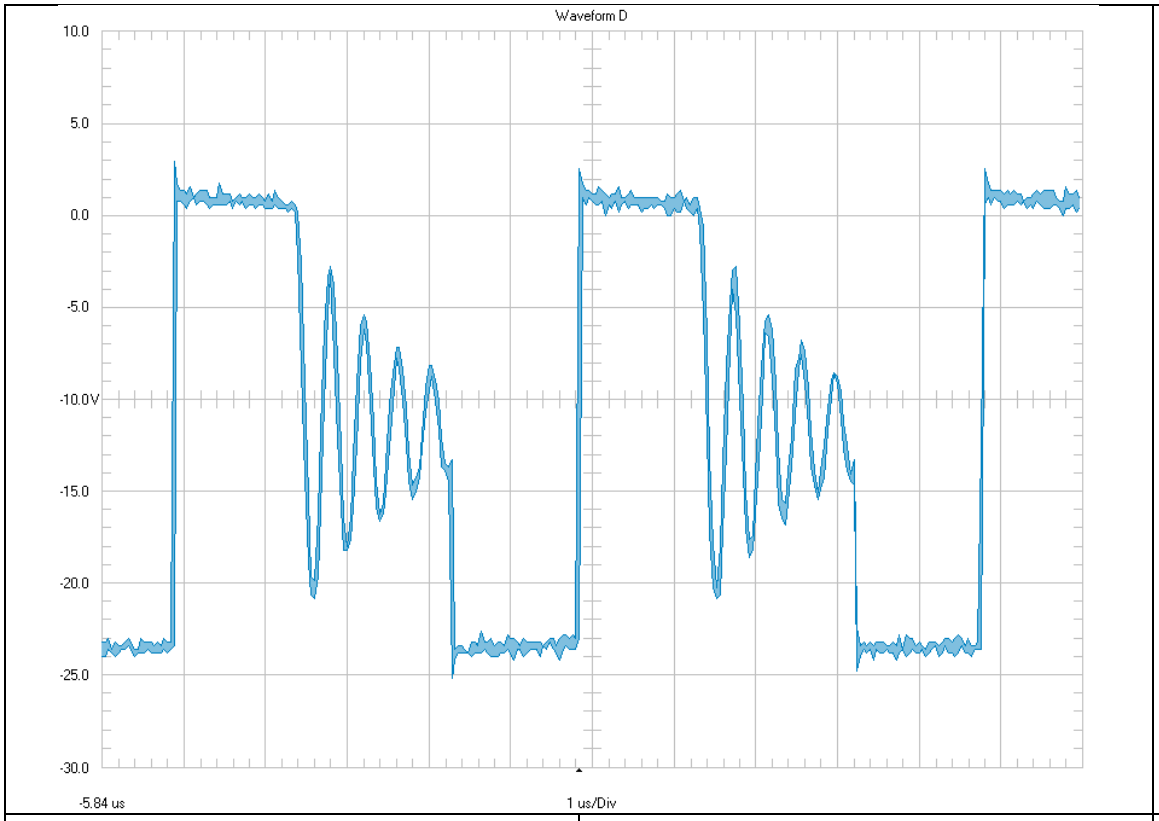


Ch1 =>
2V/div
50ns/major div

Figure 23

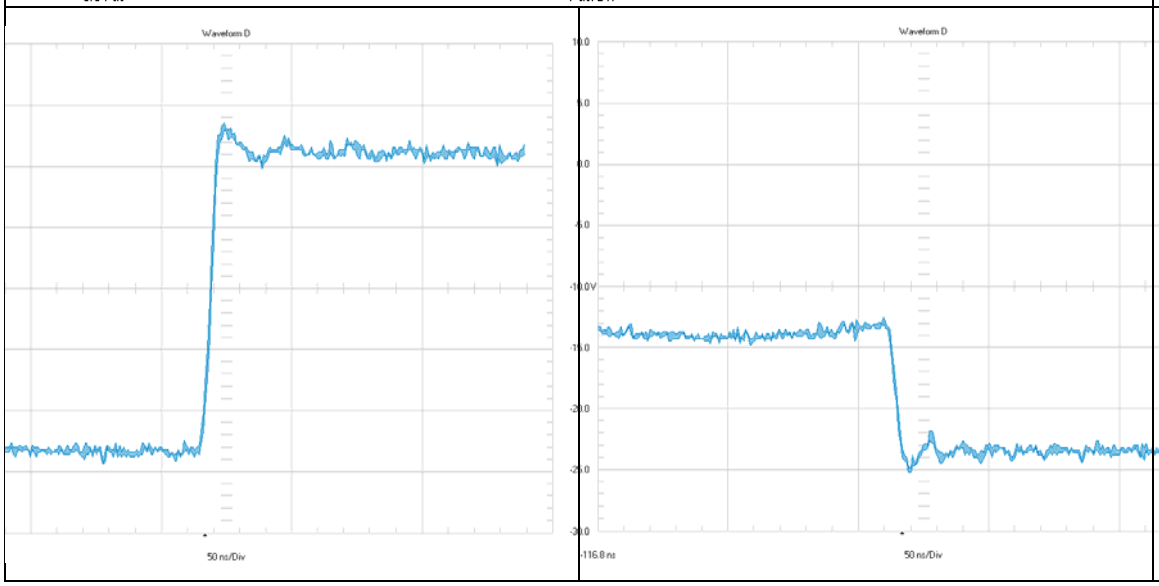
9.3 D1

Waveform at the Diode D1 (referenced to VOUT) is shown in Figure 24



Ch1 =>
5V/div

1µs/div



Ch1 =>
5V/div
50ns/major div

Figure 24

10 Thermal Image

10.1 6Vin / 250mA out

Thermal image with input voltage set to 250mA is shown in Figure 25

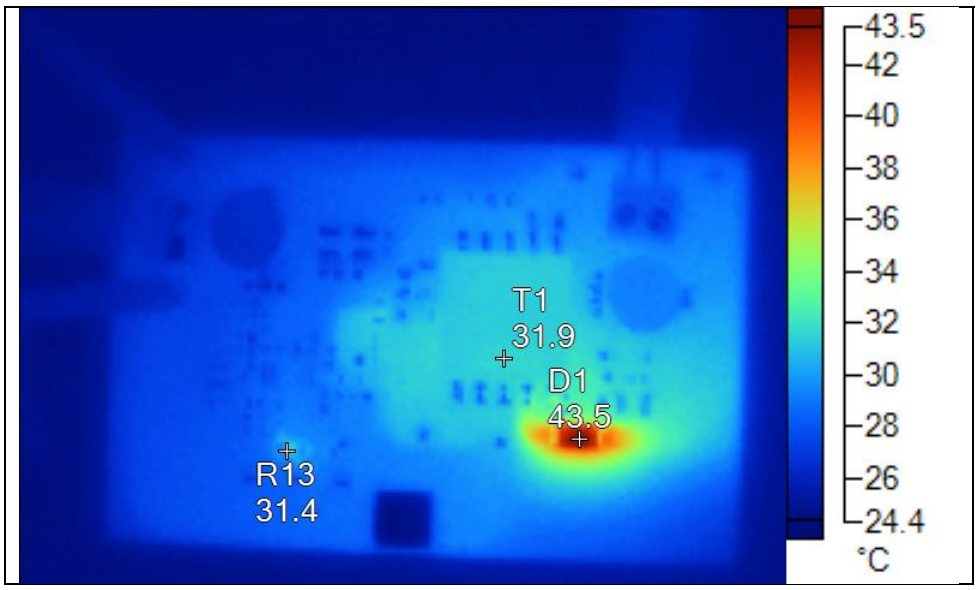


Figure 25

Name	Temperature
D1	43.5°C
R13	31.4°C
T1	31.9°C

Table 2

10.2 12Vin / 250mA out

Thermal image with input voltage set to 12V is shown in Figure 26

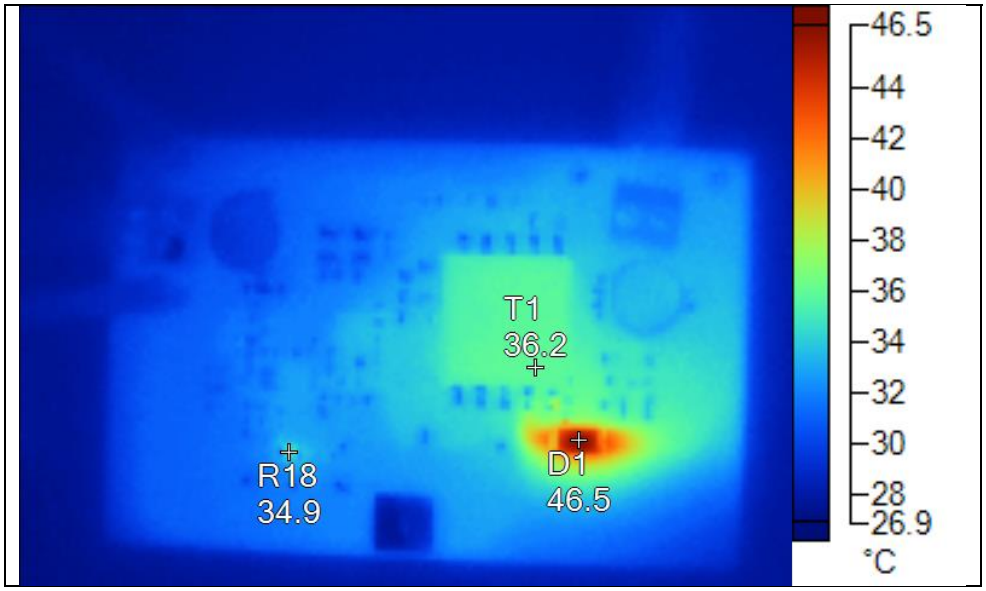


Figure 26

Name	Temperature
D1	46.5°C
T1	36.2°C
R18	34.9°C

Table 3

10.3 18Vin / 250mA out

Thermal image with input voltage set to 18V is shown in Figure 27

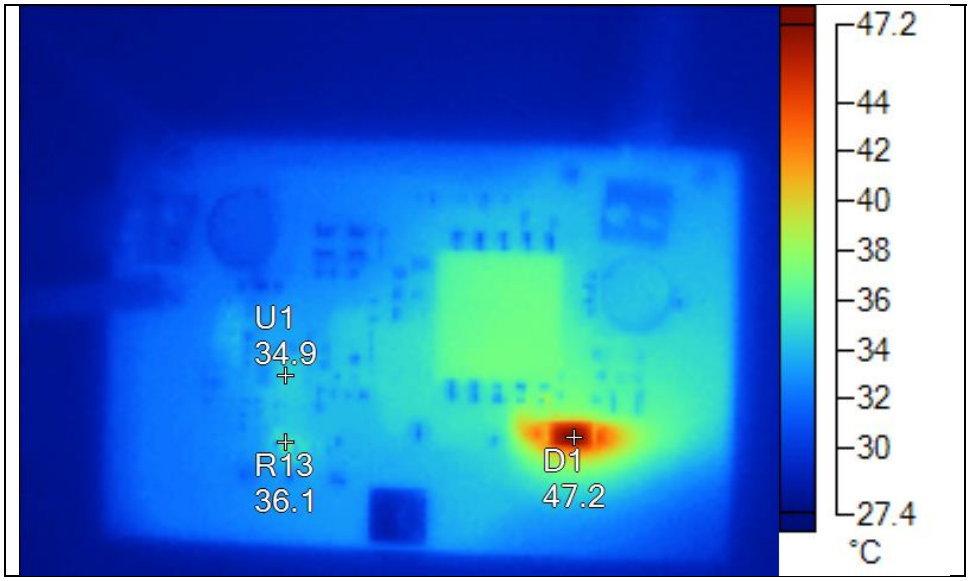


Figure 27

Name	Temperature
D1	47.2°C
R13	36.1°C
U1	34.9°C

Table 4

10.4 12Vin / 500mA out

Thermal image with input voltage set to 12V and output current 500mA is shown in Figure 28

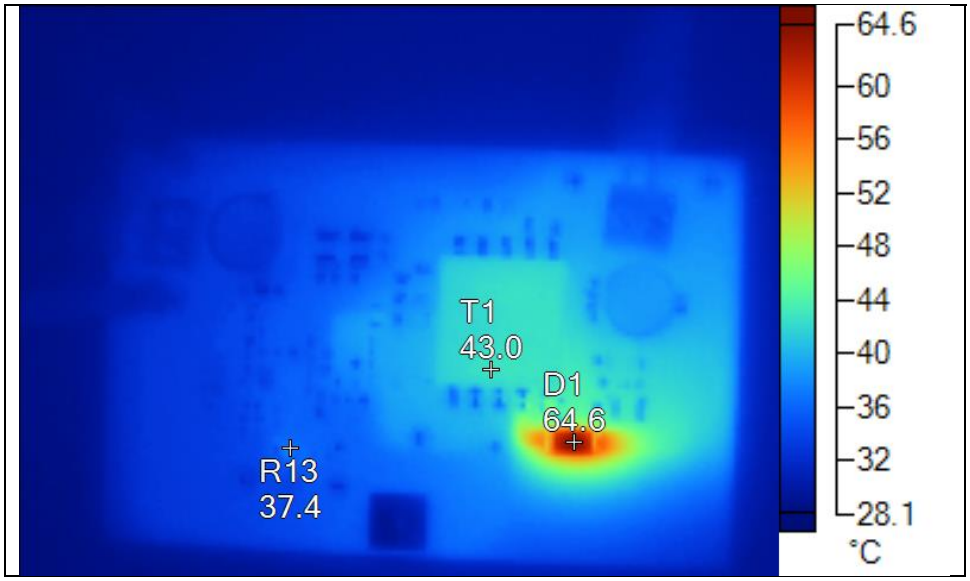


Figure 28

Name	Temperature
D1	64.6°C
T1	43.0°C
R13	37.4°C

Table 5

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