NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P3P3V" represents connection to the +3.3V digital power plane.
2. The netname "P1P8V" represents connection to the +1.8V digital power plane.
3. The netname "P1P1V" represents connection to the +1.1V digital power plane.
4. The symbol ⏚ represents connection to the digital ground plane.
5. A "Z" suffix on a signal name indicates an active low signal.
6. A "_S" suffix on a signal name indicates a trace that is between a driver and a series termination resistor.
7. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
8. The letters DNI near a part mean "do not install".

COMPUTER GENERATED DRAWING. DO NOT REVISE MANUALLY

REVISIONS

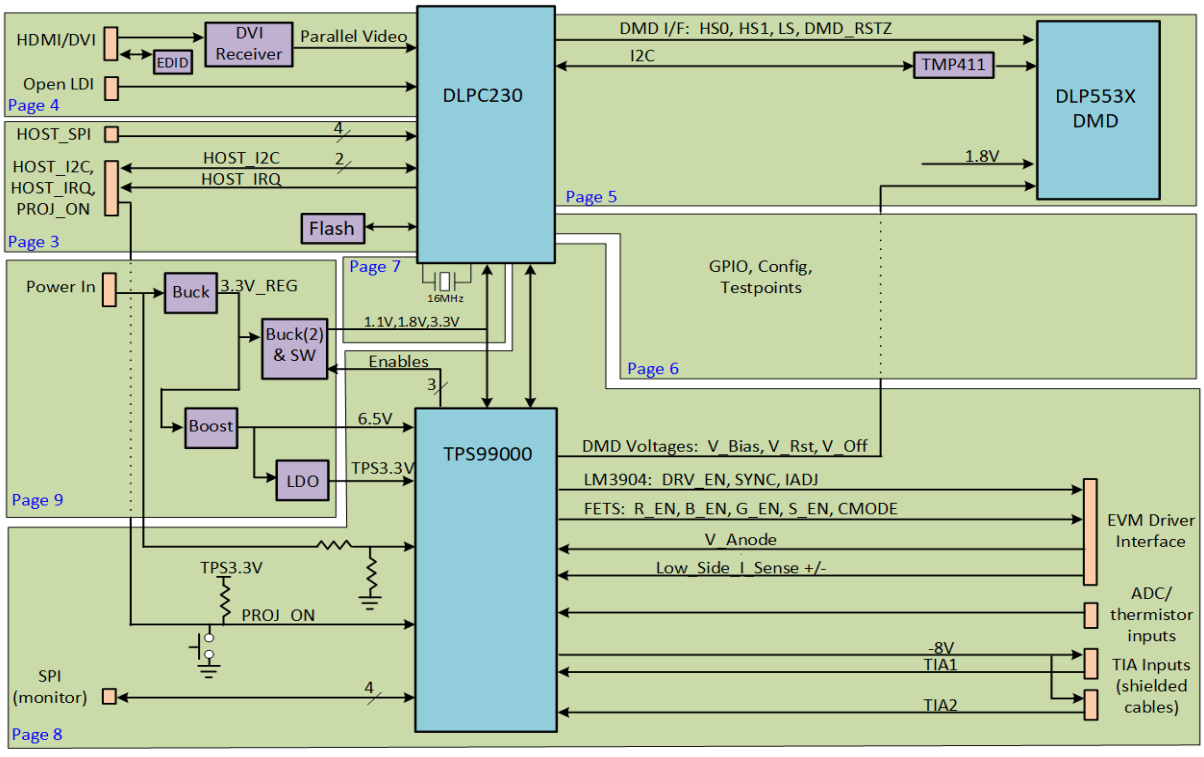
REV	DESCRIPTION	DATE	APPROVED
A	Initial Release		
B	Corrected 1.1V and 1.8V enables to regulator		

Z_PCB1

PCB, DLP553X Controller
DLP033B

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

		DWN George Pawlowski DATE 4/12/2019	TEXAS INSTRUMENTS (C) COPYRIGHT 2017 TEXAS INSTRUMENTS ALL RIGHTS RESERVED
		ENGR	
		SYST	
		PRJ	TITLE DLP553x EVM Controller
NEXT ASSY	USED ON		D DRAWING NO DLP033 REV B
APPLICATION		SW Cadence Capture 16.6	SCALE SHEET 1 of 9



TEXAS INSTRUMENTS

Drawn: George Pavlowski DATE: 4/12/2019

Issue Date: <Issue Date>

D

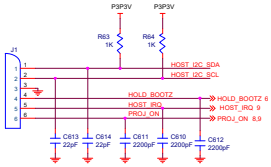
DRAWING NO: DLP033

REV: B

SCALE:

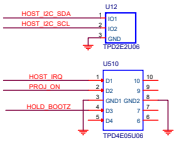
SHEET 2 OF 9

HOST I2C, PROJ_ON, IRQ, HOLD_BOOT CONNECTOR

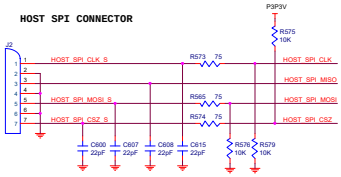


Capacitors to ground are for EMC reduction if needed.

ESD PROTECTION

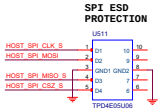


HOST SPI CONNECTOR



75 ohm series resistors are to reduce undershoot and overshoot with Cheetah adapter. Capacitors to ground are for EMC reduction if needed.

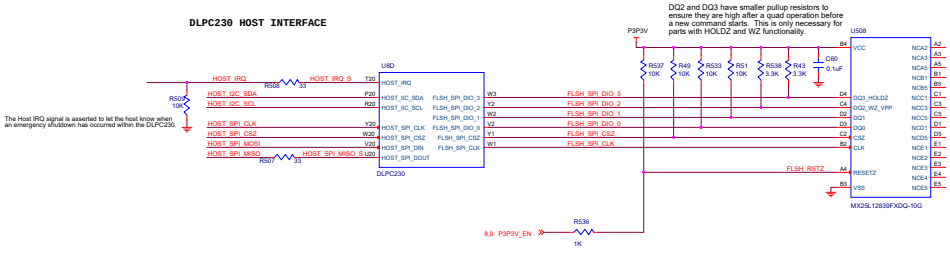
SPI ESD PROTECTION



DLPC230 CONFIGURATION FLASH

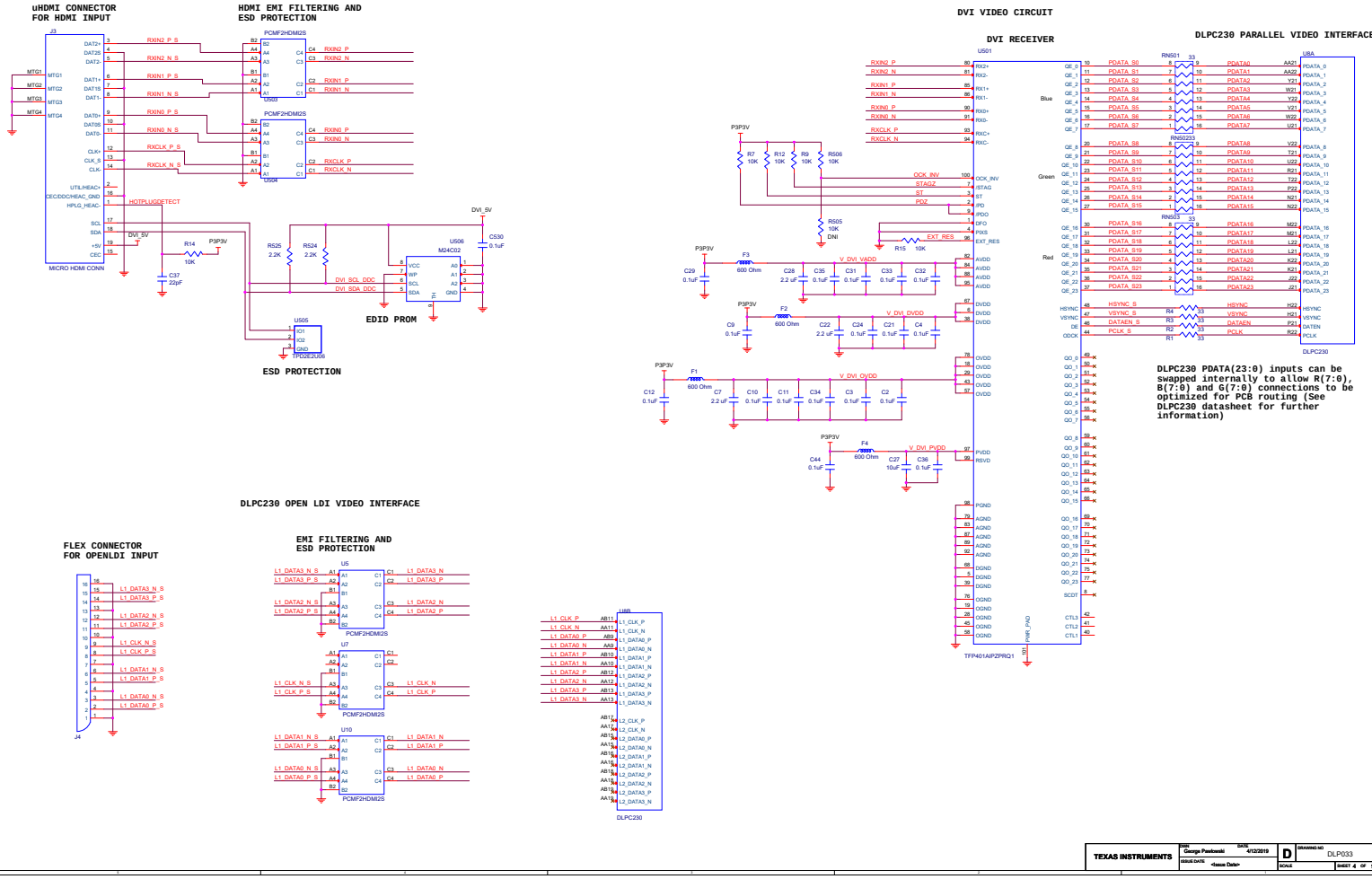
DQ2 and DQ3 have smaller pullup resistors to ensure they are high after a quad operation before a new command starts. This is only necessary for parts with HOLDZ and WZ functionality.

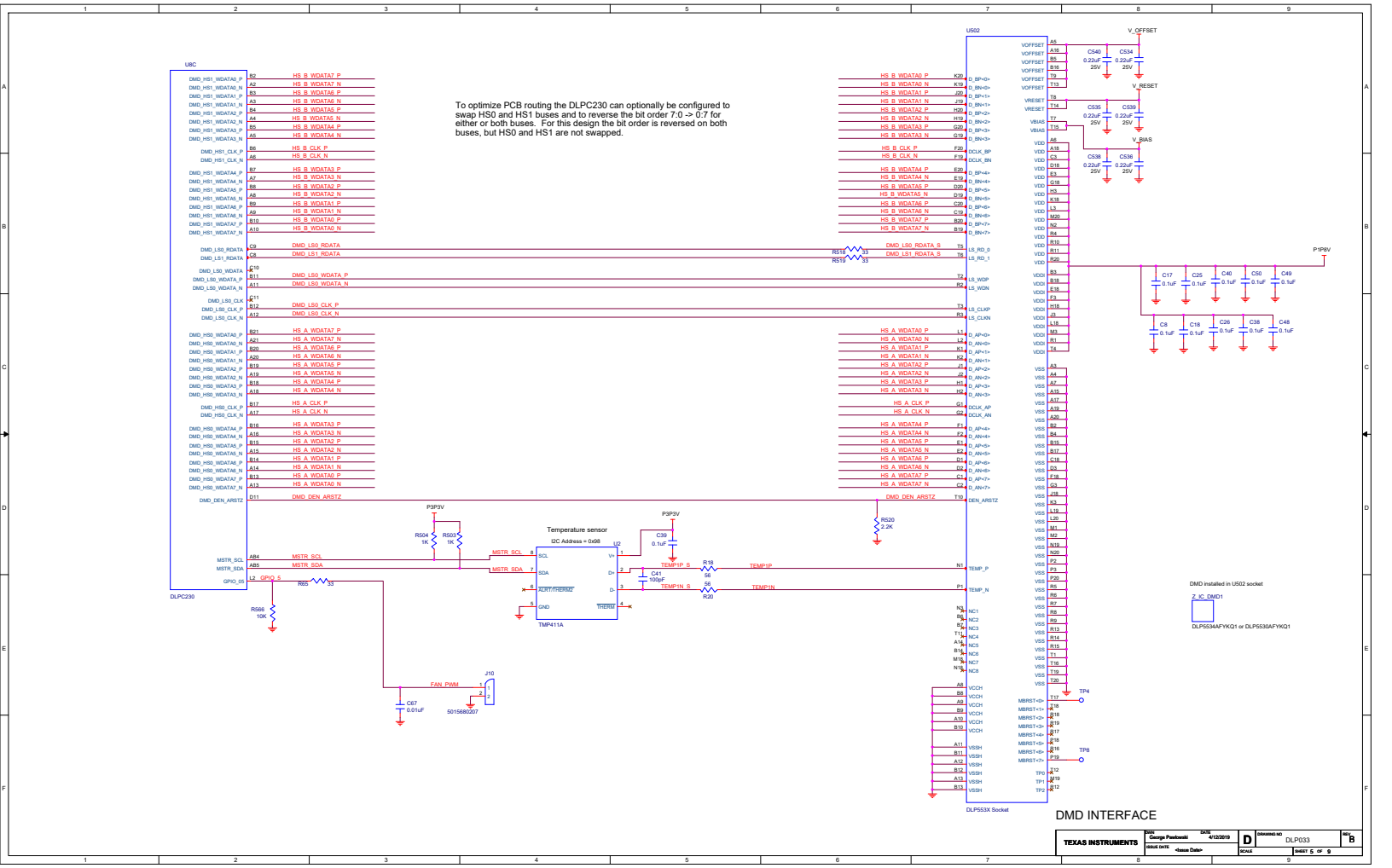
DLPC230 HOST INTERFACE



The Host IRQ signal is asserted to let the host know when an emergency shutdown has occurred within the DLPC230.

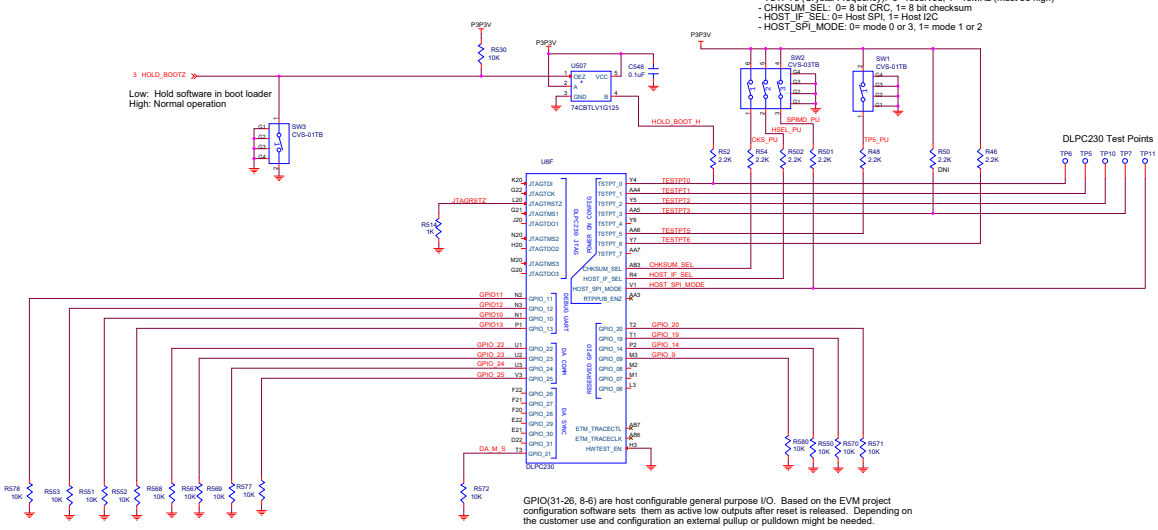
TEXAS INSTRUMENTS	DESIGNED George Pavlowski	DATE 4/12/2019	D	DRAWING NO DLP033	REV B
	CHECKED DATE <Issue Date>		SCALE	SHEET 3 OF 9	


uHDMI CONNECTOR FOR HDMI INPUT
HDMI EMI FILTERING AND ESD PROTECTION
DVI VIDEO CIRCUIT
DVI RECEIVER
DLPC230 PARALLEL VIDEO INTERFACE
EDID PROM
ESD PROTECTION
DLPC230 PDATA(23:0) inputs can be swapped internally to allow R(7:0), B(7:0) and G(7:0) connections to be optimized for PCB routing (See DLPC230 datasheet for further information)
DLPC230 OPEN LDI VIDEO INTERFACE
FLEX CONNECTOR FOR OPENLDI INPUT
EMI FILTERING AND ESD PROTECTION
TEXAS INSTRUMENTS
DLP033
SHEET 4 OF 9


To optimize PCB routing the DLPC230 can optionally be configured to swap HS0 and HS1 buses and to reverse the bit order 7:0 -> 0:7 for either or both buses. For this design the bit order is reversed on both buses, but HS0 and HS1 are not swapped.
U8C
DLPC230
U502
DLP553X Socket
Temperature sensor
I2C Address = 0x98
TMP411A
DMD installed in U502 socket
Z_IC_DMD1
DLP5534AFYKQ1 or DLP5530AFYKQ1
V_OFFSET
V_RESET
V_BIAS
P1P8V
P3P3V
P5P3V
DMD INTERFACE
TEXAS INSTRUMENTS
DLP033

- TSTPT(7:0), CHKSUM_SEL, HOST_IF_SEL, HOST_SPI_SEL are inputs when RESETZ is low and have internal weak pulldown resistors. The states of the inputs are sampled after reset transitions from low to high to determine configuration options. Pins are then set as outputs.

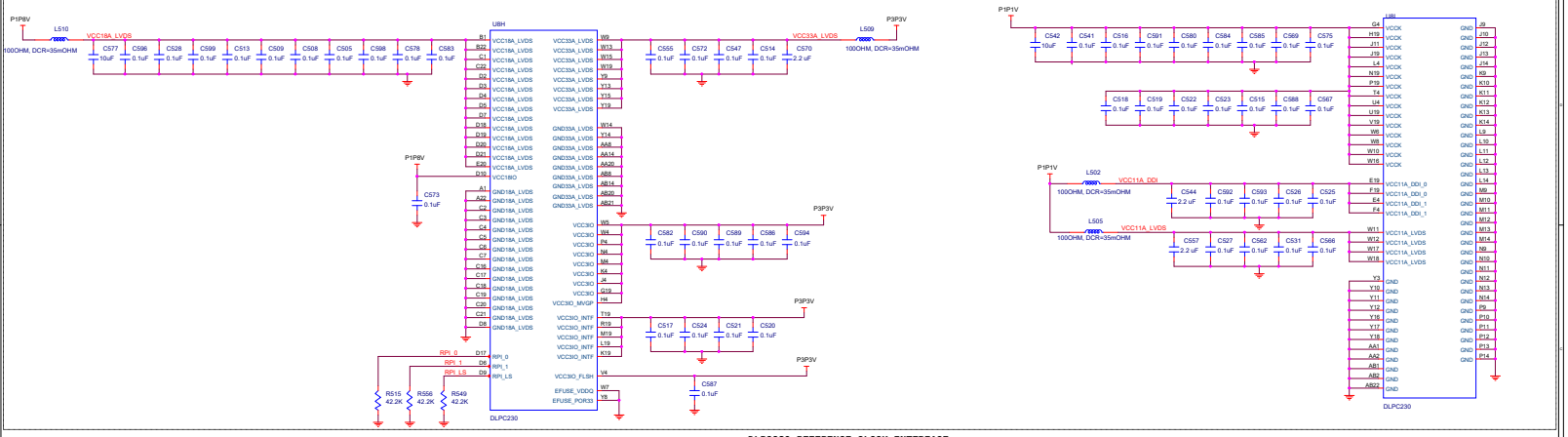
CONFIGURATION OPTIONS
- TSTPT0 (STAY-IN-BOOT): 0= load main app, 1= stay in boot app
- TSTPT1 (EXT-BOOT-EN): 0= internal boot (must be low)
- TSTPT2 (I2C-ADDR-SEL): 0=0x36 (must be low)
- TSTPT3 (ALT-MADR-SEL): 0= load main app 1, 1= load main app 2
- TSTPT4 (BOOT-SPI-MASTER-EN): 0= disabled (must by low)
- TSTPT5 (Spread Spectrum Enable): 0= disabled, 1= enabled
- TSTPT6 (Crystal Frequency): 0= reserved, 1= 16MHz (must be high)
- CHKSUM_SEL: 0= 8 bit CRC, 1= 8 bit checksum
- HOST_IF_SEL: 0= Host SPI, 1= Host I2C
- HOST_SPI_MODE: 0= mode 0 or 3, 1= mode 1 or 2



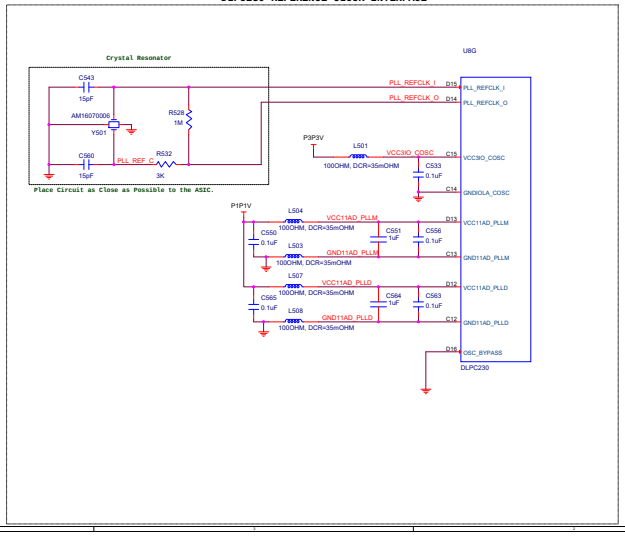
GPIO(31-26, 8-6) are host configurable general purpose I/O. Based on the EVM project configuration software sets them as active low outputs after reset is released. Depending on the customer use and configuration an external pullup or pulldown might be needed.

TEXAS INSTRUMENTS	Design: George Pavlowski	Date: 4/12/2019	D
	Check by: <Issue Date>	Drawing no: DLP033	Rev: B
	Scale:	Sheet 8 of 9	

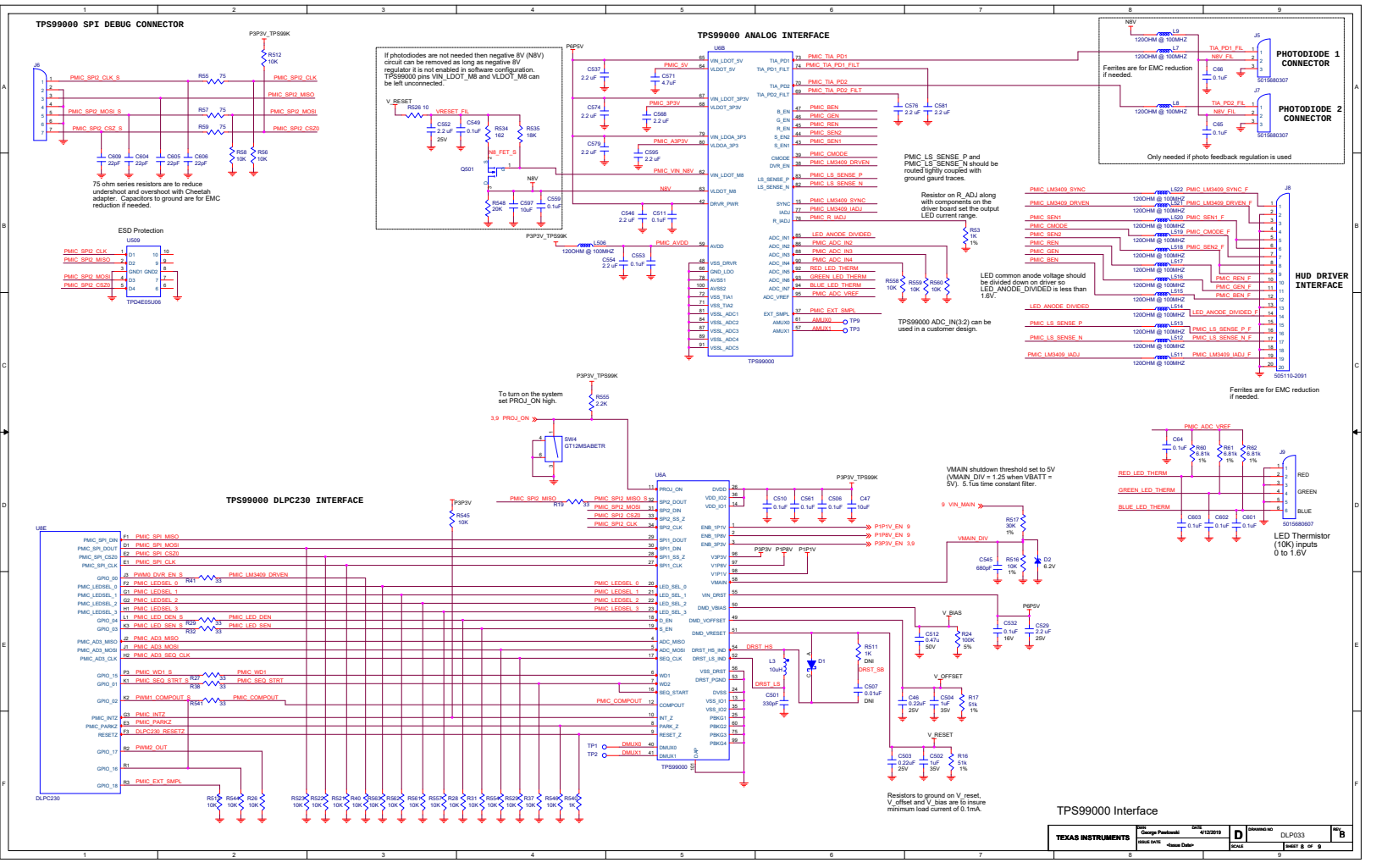
DLPC230 POWER

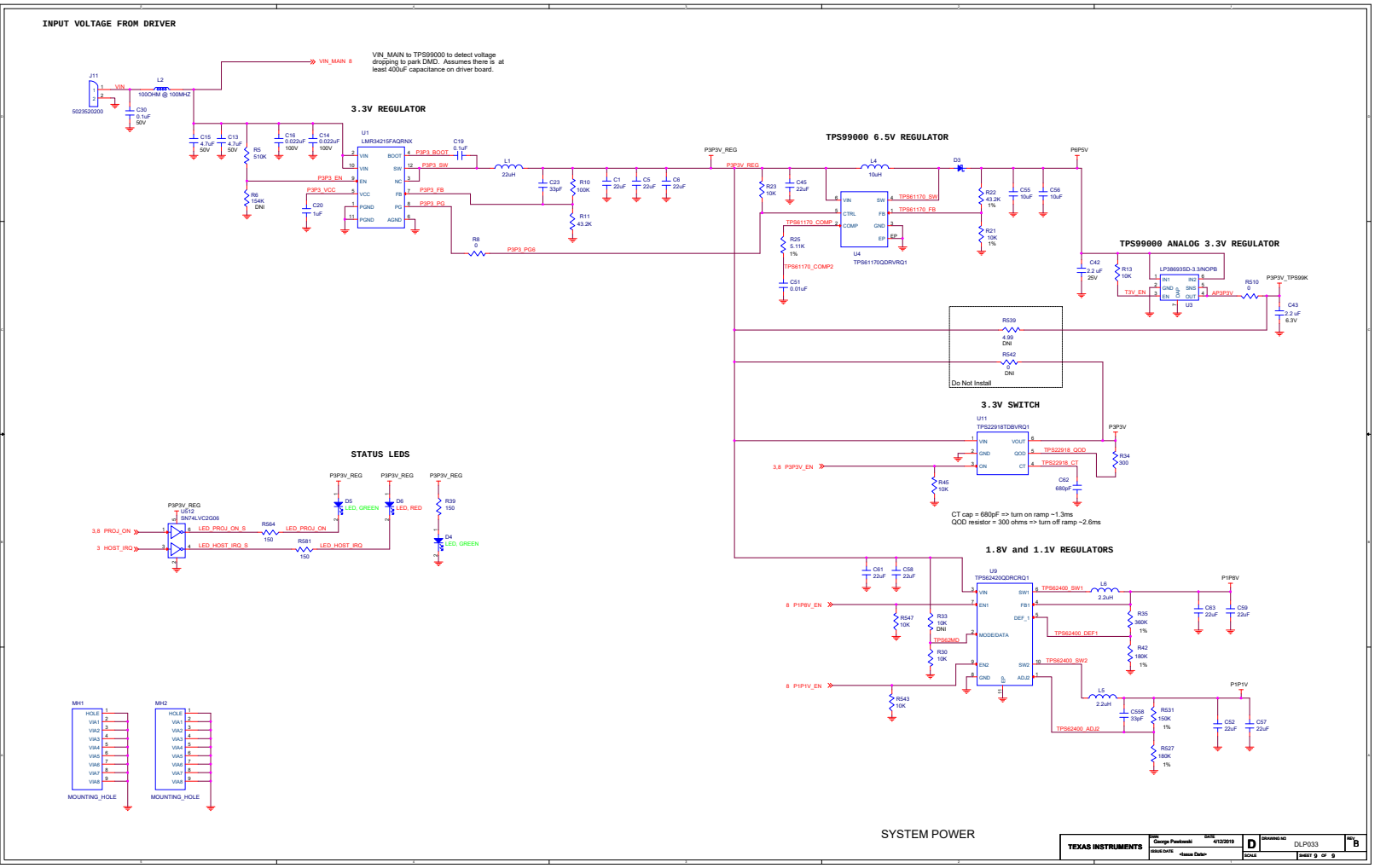


DLPC230 REFERENCE CLOCK INTERFACE



TEXAS INSTRUMENTS	Design: George Pavlowski	Date: 4/12/2019	D	Drawing no: DLP033
	Check by:	<Issue Date>	Scale:	Sheet 7 of 9


TPS99000 SPI DEBUG CONNECTOR
TPS99000 ANALOG INTERFACE
TPS99000 DLPC230 INTERFACE
PHOTODIODE 1 CONNECTOR
PHOTODIODE 2 CONNECTOR
HUD DRIVER INTERFACE
ESD Protection
TPD4E05U06
TPS99000
DLPC230
To turn on the system set PROJ_ON high.
LED Thermistor (10K) inputs 0 to 1.6V
TPS99000 Interface
TEXAS INSTRUMENTS
DLP033


INPUT VOLTAGE FROM DRIVER
VIN_MAIN to TPS99000 to detect voltage dropping to park DMD. Assumes there is at least 400uF capacitance on driver board.
3.3V REGULATOR
TPS99000 6.5V REGULATOR
TPS99000 ANALOG 3.3V REGULATOR
3.3V SWITCH
STATUS LEDS
1.8V and 1.1V REGULATORS
Do Not Install
CT cap = 680pF => turn on ramp ~1.3ms
QOD resistor = 300 ohms => turn off ramp ~2.6ms
SYSTEM POWER
TEXAS INSTRUMENTS
George Pavlowski
4/12/2019
DLP033
B
SHEET 9 OF 9