

MAXWELL CUSTOMER PROCESSOR BOARD

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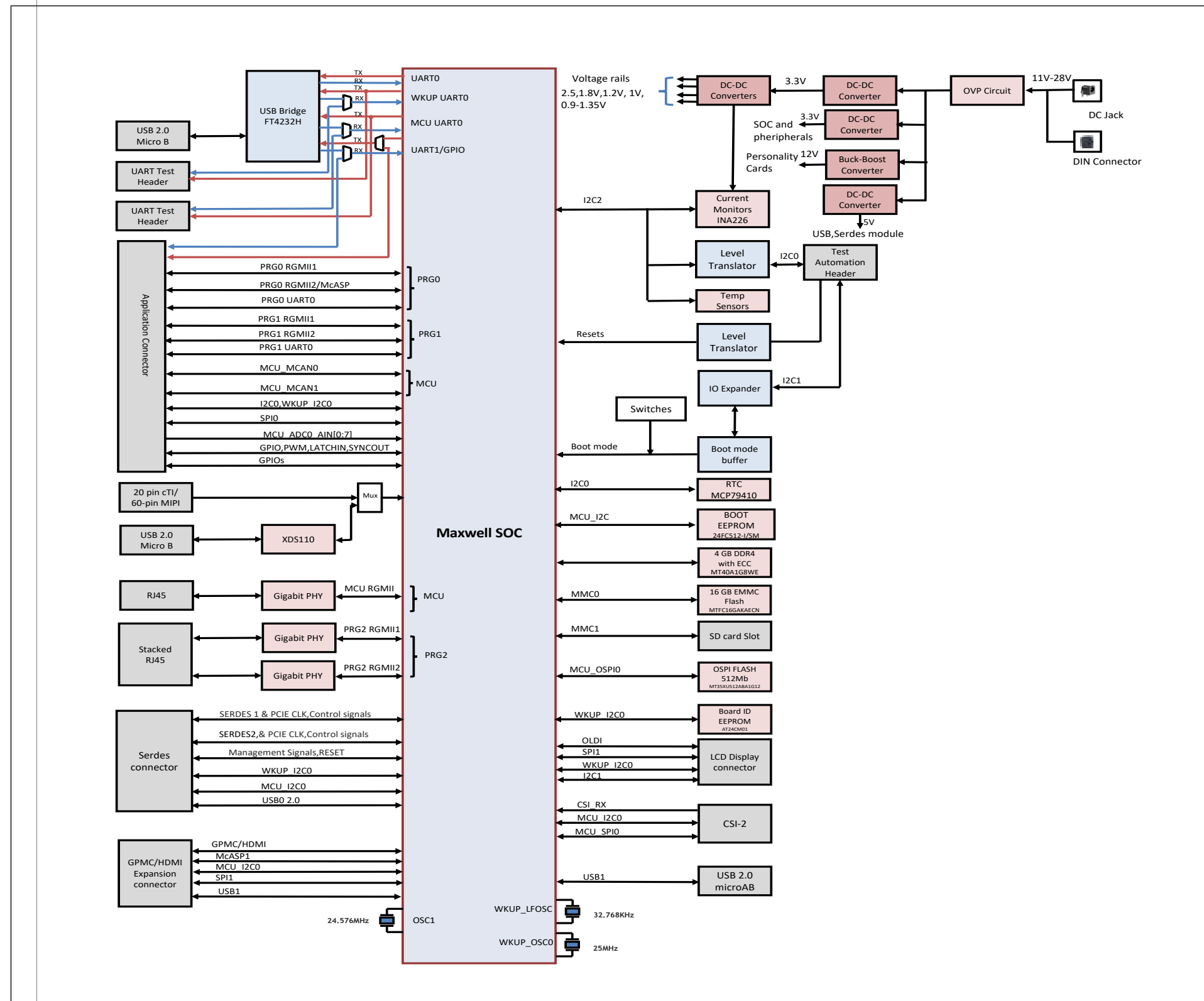
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REV	E3
VER	1.0

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	29th MAY 2018	Drafted from "PROC062_REV E2_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	13th JUN 2018	Updated REV E3 schematic as per change list document.	Mistral Design Team	AJIT MB	AJIT MB
1.0	04th SEP 2018	Baselined	Mistral Design Team	AJIT MB	AJIT MB

BLOCK DIAGRAM_CP BOARD



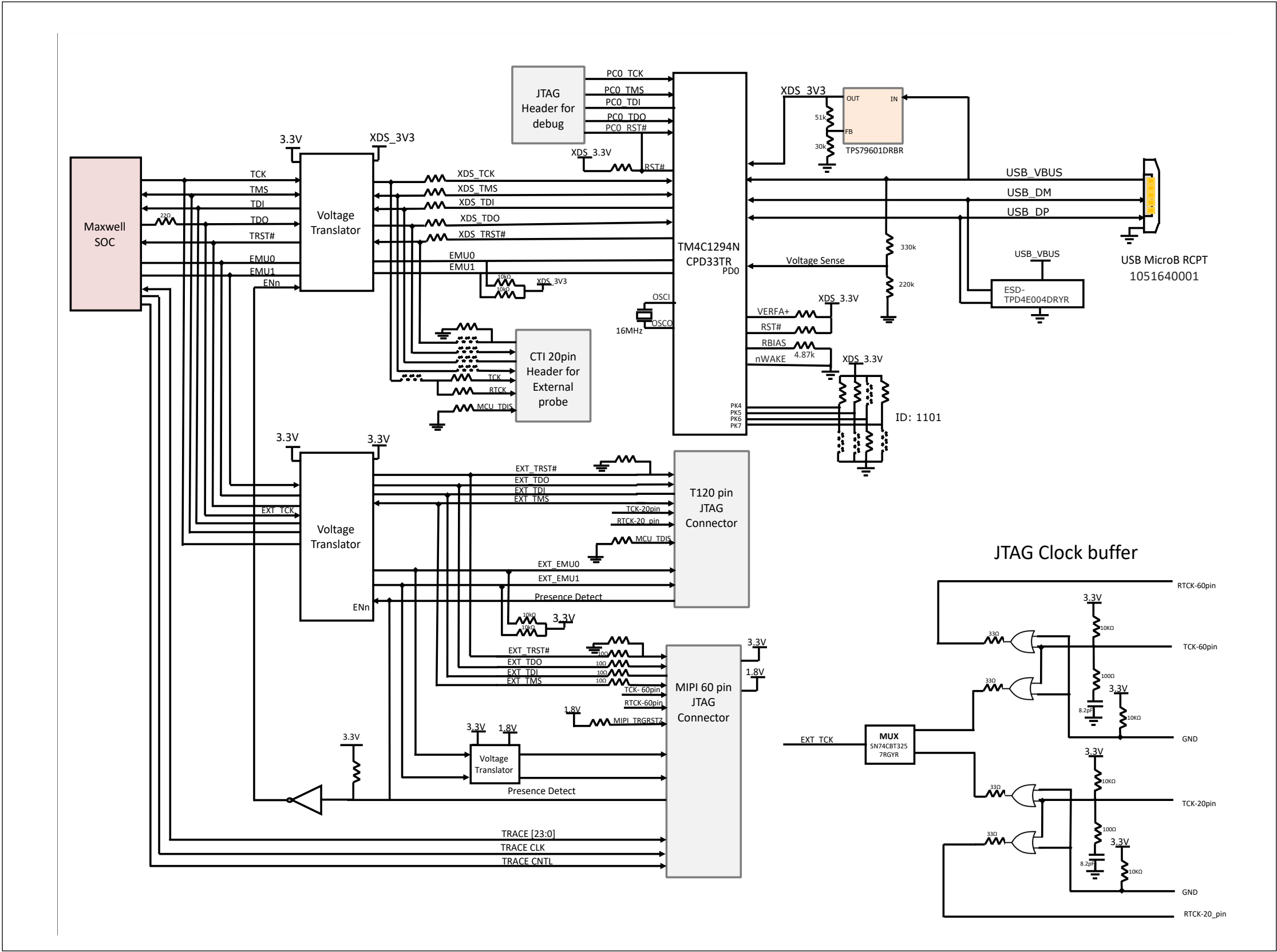
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Title BLOCK DIAGRAM_CP BOARD

Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
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BLOCK DIAGRAM_XDS110



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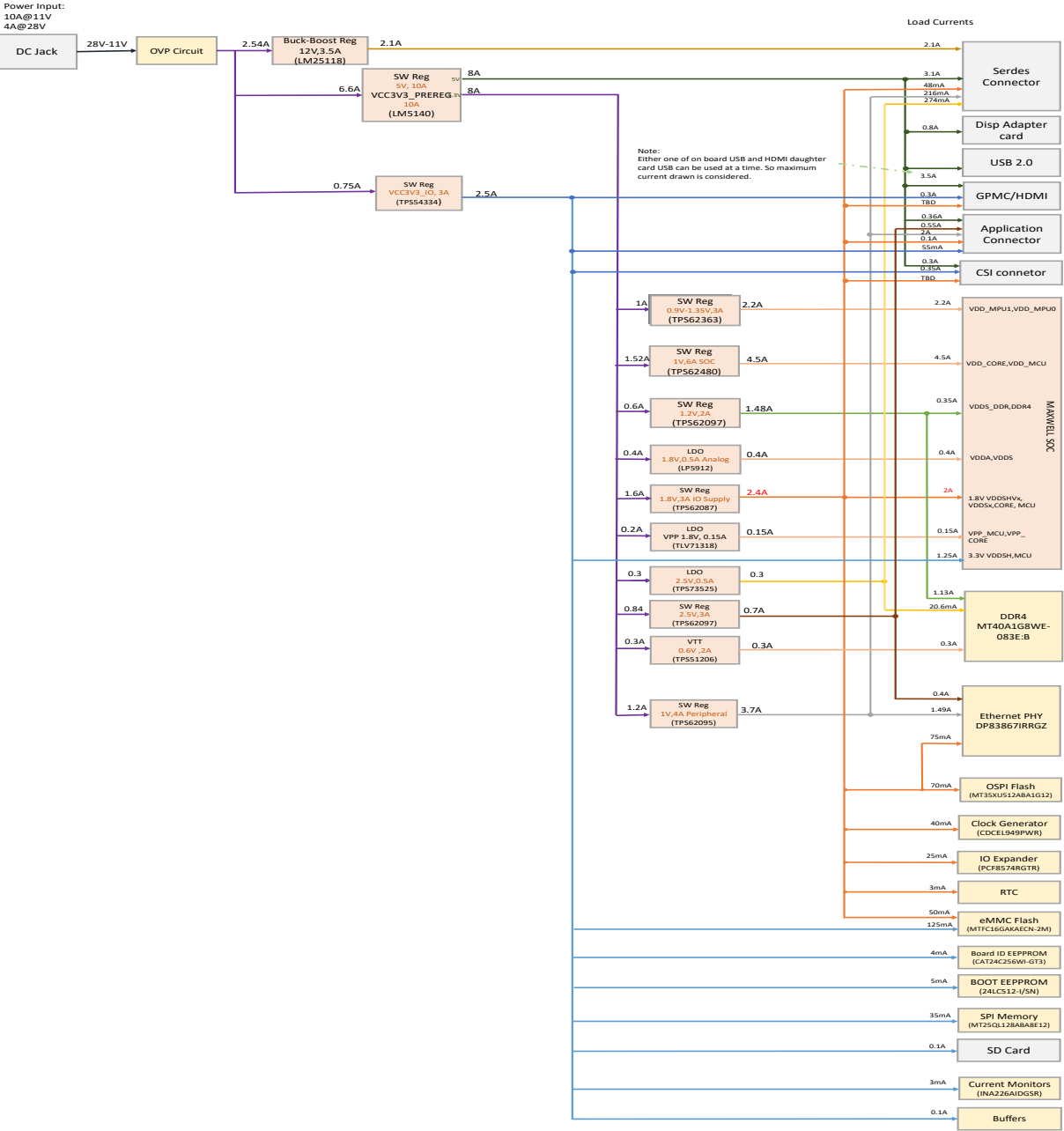
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Size Variant Name = PROC062 001 OPN#TMDX654IDKEVM Rev E3

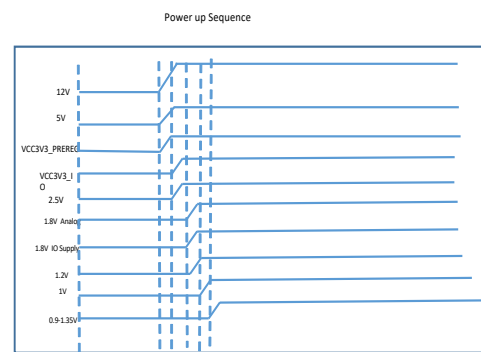
Date: Tuesday, July 24, 2018

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POWER FLOW DIAGRAM

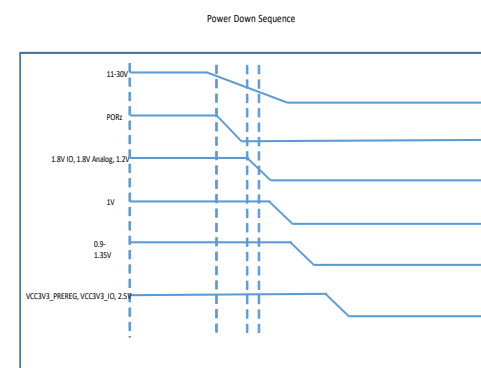


POWER SEQUENCE

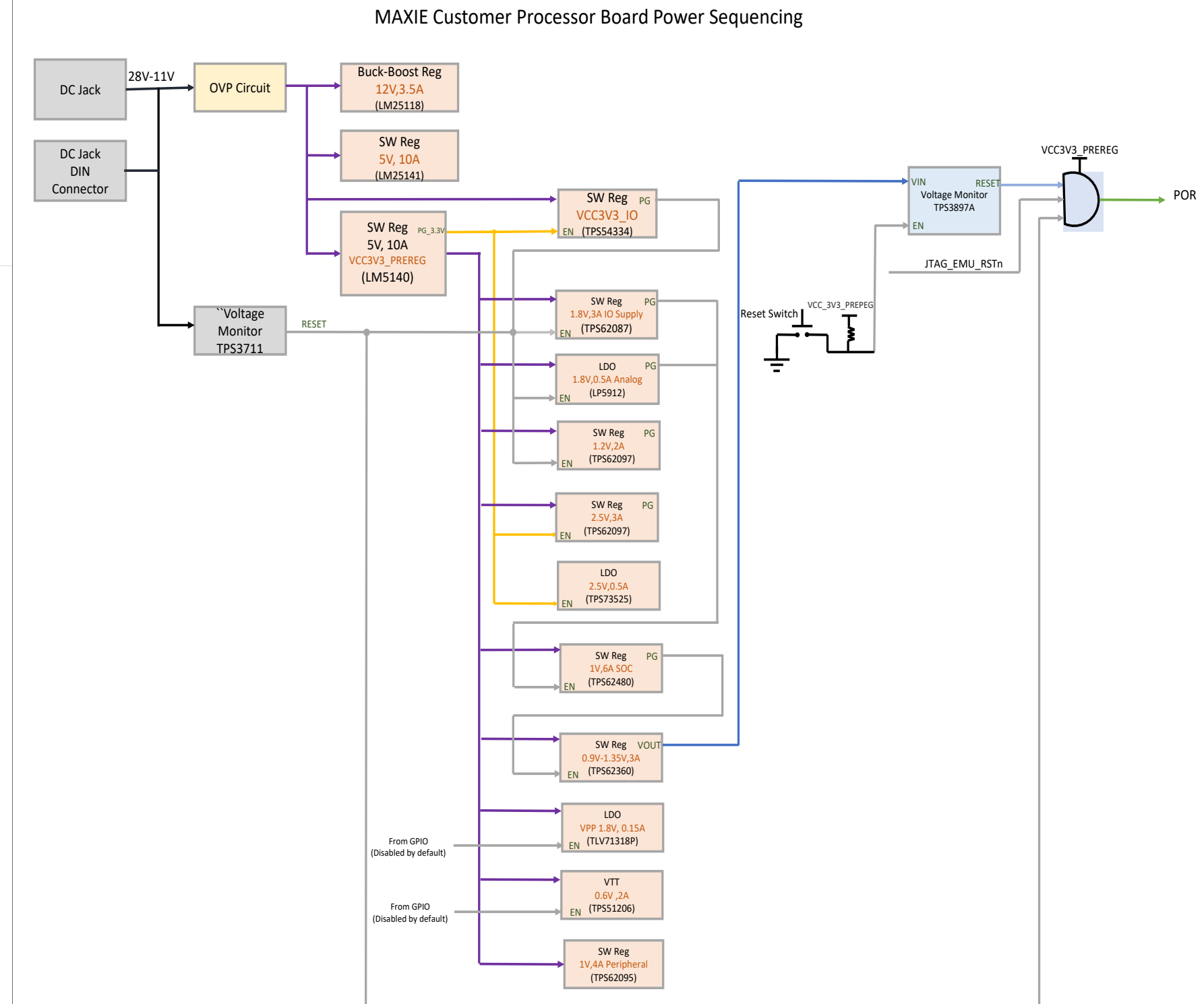


Power up Sequence:
12V, 5V, 3V3_PREREG ---> VCC3V3_IO, 2.5V ---> 1.8V Analog, 1.8V IO Supply ---> 1V SOC ---> 0.9-1.35V

There is no sequencing for 1V Peripheral supply



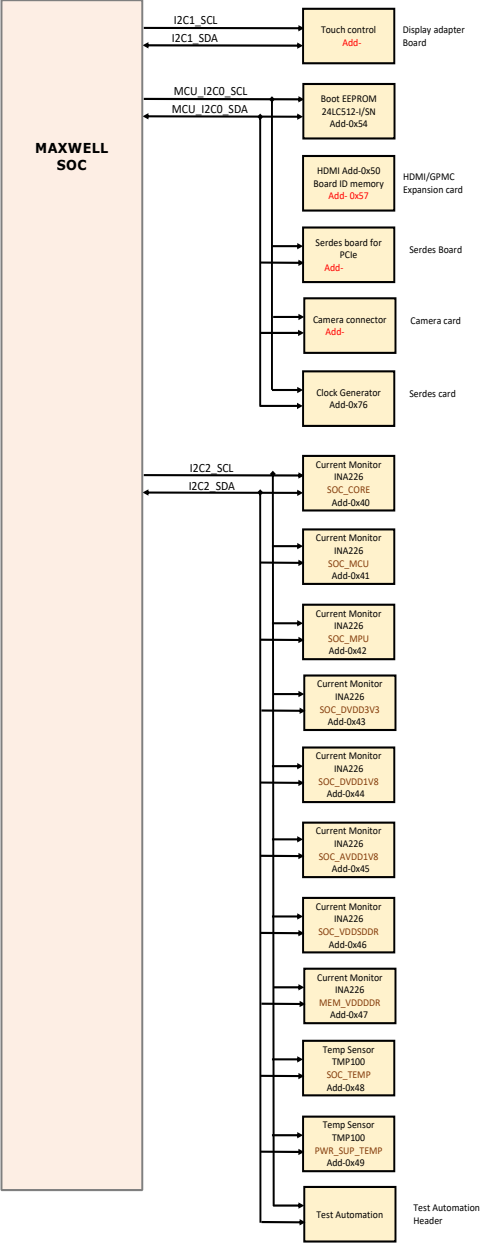
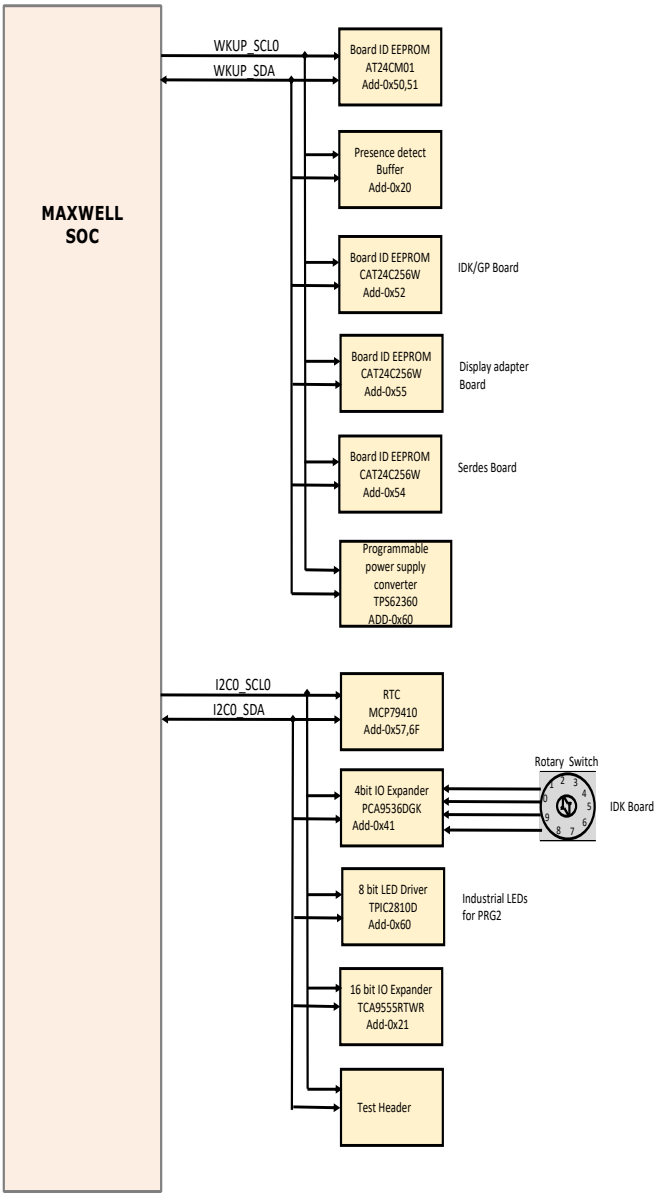
Power down Sequence:
1.2V, 1.8V Analog, 1.8V IO Supply, 1V SOC, 0.9V-1.35V, ---->VCC3V3_PREREG, VCC3V3_IO, 2.5V



GPIO MAPPING TABLE

Total No of GPIOs Required from Maxwell SoC								
SI No	GPIO Description	Required on	FUNCTIONALITY	GPIO Number	SoC Muxed Signal name	Direction WRT CTRL	Default state	Active state
1	Two MCU Domain GPIO for CP board push button1	Customer Processor Board	Push button	WKUP_GPIO0_24	MCU_OSPI0_CSN1	Input	High	Low
2	Two MCU Domain GPIO for CP board push button1	Customer Processor Board	Push button	WKUP_GPIO0_27	MCU_OSPI1_DQS	Input	High	Low
3	eMMC Reset control GPIO	Customer Processor Board	Reset	I2C_GPIO_Expander		Output	High	Low
4	OSPI flash Reset control GPIO	Customer Processor Board	Reset	I2C_GPIO_Expander		Output	High	Low
5	SPI NOR flash Reset control GPIO	Customer Processor Board	Reset	I2C_GPIO_Expander		Output	High	Low
6	ICSSG_PRG2_Ethernet PHY Reset control GPIO	Customer Processor Board	Reset	I2C_GPIO_Expander		Output	High	Low
7	ICSSG_PRG2_Ethernet PHY Interrupt GPIO	Customer Processor Board	Interrupt	GPIO1_87	EXT_REFCLK1	Input/Output	High	Low
8	ICSSG_Ethernet PHY_1_Link Detection GPIO	Customer Processor Board	Link Detection (GPIO Input)	GPIO1_13	MMC0_SDCD	Input	Low	High
9	ICSSG_Ethernet PHY_2_Link Detection GPIO	Customer Processor Board	Link Detection (GPIO Input)	GPIO1_14	MMC0_SDWP	Input	Low	High
10	MCU domain Ethernet PHY Reset Control GPIO	Customer Processor Board	Reset	I2C_GPIO_Expander		Output	High	Low
11	MCU domain Ethernet PHY Interrupt GPIO	Customer Processor Board	Interrupt	GPIO1_80	MMC1_SDWP	Input/Output	High	Low
12	Three GPIO's are required to control the Mux select between UART test header RX , Application board & FT4232_UART_RX	Customer Processor Board	Mux Selection	I2C_GPIO_Expander		Output	High	Low
13				I2C_GPIO_Expander		Output	High	Low
14				I2C_GPIO_Expander		Output	High	Low
15	VPP LDO enable	Customer Processor Board	VPP_EN	WKUP_GPIO0_26	MCU_OSPI1_LBCLKO	Output	Low	High
16	One WKUP_GPIO for VTT Regulator Enable	Customer Processor Board	VTT_EN	WKUP_GPIO0_28	MCU_OSPI1_D0	Output	Low	High
17	GPIO0 to drive PRG2 LED0	Customer Processor Board	LEDs	WKUP_GPIO0_8	WKUP_GPIO0_8	Output	Low	High
18	GPIO1 to drive PRG2 LED1	Customer Processor Board	LEDs	WKUP_GPIO0_0	WKUP_GPIO0_0	Output	Low	High
19	GPIO2 to drive PRG2 LED2	Customer Processor Board	LEDs	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	Low	High
20	GPIO3 to drive PRG2 LED3	Customer Processor Board	LEDs	WKUP_GPIO0_50	MCU_SPI0_D1	Output	Low	High
21	IDK_ICSSG_PRG0_Ethernet PHY Reset Control GPIO	IDK_GP_Application board	Reset	GPIO1_34	PRG0_PRU0GPO5	Output	High	Low
22	IDK_ICSSG_PRG0_Ethernet PHY Interrupt GPIO	IDK_GP_Application board	Interrupt	GPIO1_37	PRG0_PRU0GPO8	Input/Output	High	Low
23	IDK_ICSSG_PRG1_Ethernet PHY Reset Control GPIO	IDK_GP_Application board	Reset	GPIO0_61	PRG1_PRU0GPO5	Output	High	Low
24	IDK_ICSSG_PRG1_Ethernet PHY Interrupt GPIO	IDK_GP_Application board	Interrupt	GPIO0_81	PRG1_PRU1GPO5	Output	High	Low
25	IDK_ICSSG_Ethernet PHY_1_Link Detection GPIO	IDK_GP_Application board	Link Detection (GPIO Input)	GPIO0_84	PRG1_PRU1GPO8	Input	Low	High
26	IDK_ICSSG_Ethernet PHY_2_Link Detection GPIO	IDK_GP_Application board	Link Detection (GPIO Input)	GPIO0_64	PRG1_PRU0GPO8	Input	Low	High
27	IDK_ICSSG_Ethernet PHY_3_Link Detection GPIO	IDK_GP_Application board	Link Detection (GPIO Input)	GPIO1_39	PRG0_PRU0GPO10	Input	Low	High
28	IDK_ICSSG_Ethernet PHY_4_Link Detection GPIO	IDK_GP_Application board	Link Detection (GPIO Input)	GPIO1_57	PRG0_PRU1GPO8	Input	Low	High
29	IDK_ICSSG0_Ethernet LED0	IDK_GP_Application board	LEDs	GPIO0_83	PRG1_PRU1GPO7	Output	Low	High
30	IDK_ICSSG0_Ethernet LED0	IDK_GP_Application board	LEDs	GPIO0_93	PRG1_PRU1GPO17	Output	Low	High
31	IDK_ICSSG0_Ethernet LED0	IDK_GP_Application board	LEDs	GPIO0_95	PRG1_PRU1GPO19	Output	Low	High
32	IDK_ICSSG0_Ethernet LED0	IDK_GP_Application board	LEDs	GPIO0_94	PRG1_PRU1GPO18	Output	Low	High
33	IDK_ICSSG0_Ethernet LED0	IDK_GP_Application board	LEDs	GPIO1_58	PRG0_PRU1GPO9	Output	Low	High
34	IDK_ICSSG0_Ethernet LED0	IDK_GP_Application board	LEDs	GPIO1_54	PRG0_PRU1GPO5	Output	Low	High
35	IDK_ICSSG0_Ethernet LED0	IDK_GP_Application board	LEDs	GPIO1_38	PRG0_PRU0GPO9	Output	Low	High
36	IDK_ICSSG0_Ethernet LED0	IDK_GP_Application board	LEDs	GPIO1_59	PRG0_PRU1GPO10	Output	Low	High
37	Touch Reset Control GPIO	LCD Adapter Board	Reset	I2C_GPIO_Expander		Output	High	Low
38	Touch Interrupt GPIO	LCD Adapter Board	Interrupt	I2C_GPIO_Expander		Input	Low	High
39	LCD Display Enable GPIO	LCD Adapter Board	LCD_EN	I2C_GPIO_Expander		Output	High	Low
40	CSI Camera Module Reset Control GPIO	CSI Connector	Reset	I2C_GPIO_Expander		Output	High	Low
41	Display_Power_Down GPIO	HDMI / GPMC Daughter Card	Display_PowerDown	I2C_GPIO_Expander		Output	High	Low
42	Touch Event GPIO	HDMI / GPMC Daughter Card	Interrupt	I2C_GPIO_Expander		Input	High	Low
43	SGMII PHY reset control	Serdes Modules	Reset	I2C_GPIO_Expander		Output	High	Low
44	SGMII PHY Interrupt	Serdes Modules	Interrupt	GPIO1_81	NMIN	Input/Output	High	Low

I2C TREE



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Title I2C TREE

Size C Variant Name = PROC062 001 OPN#TMDX654IDKEVM

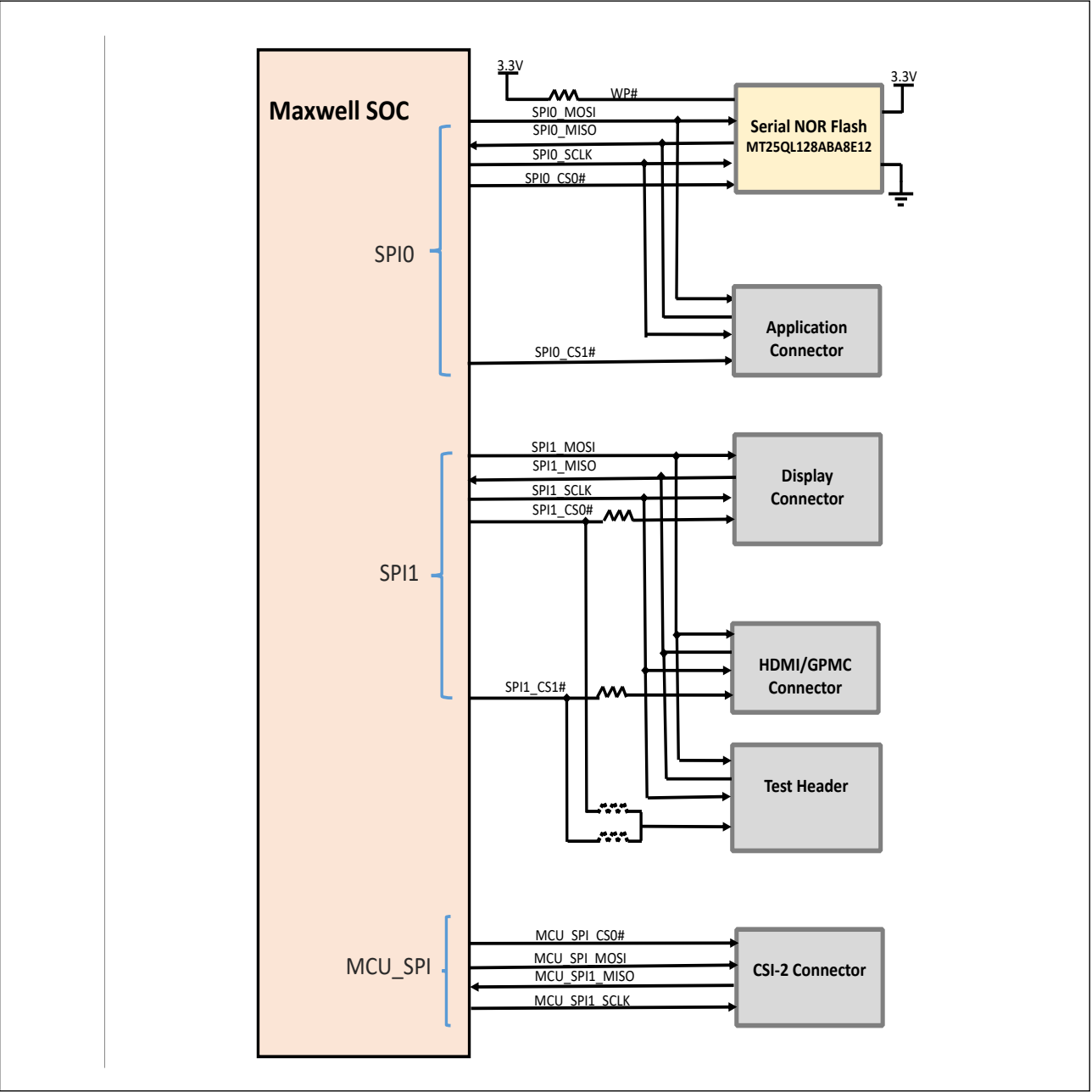
Rev

E3

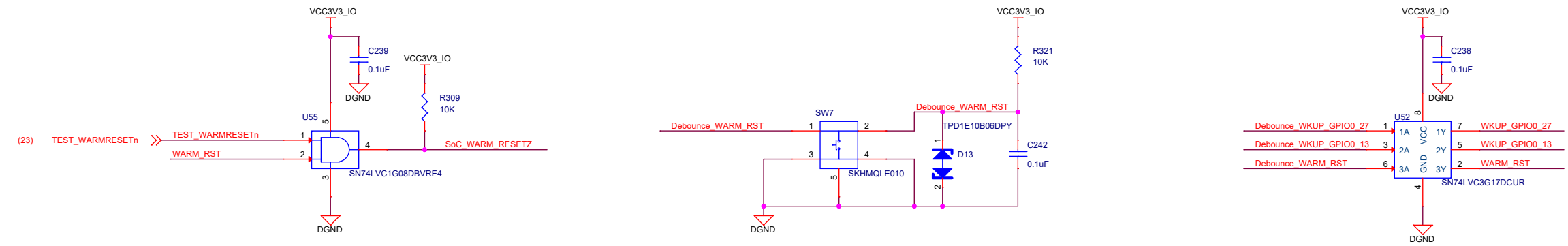
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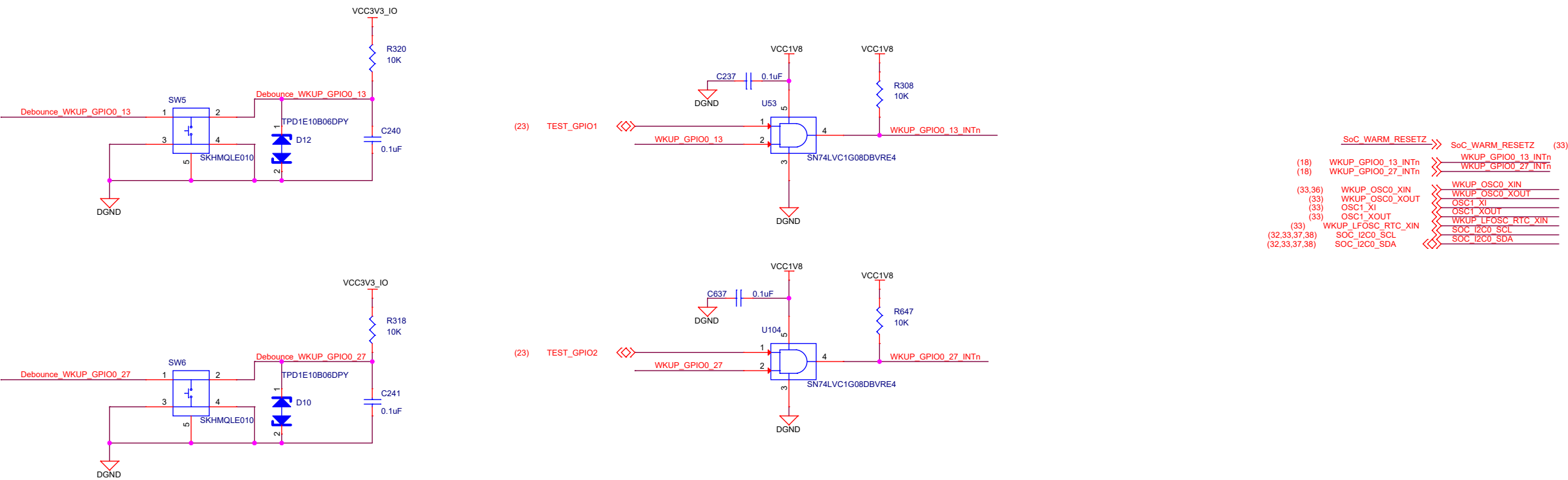
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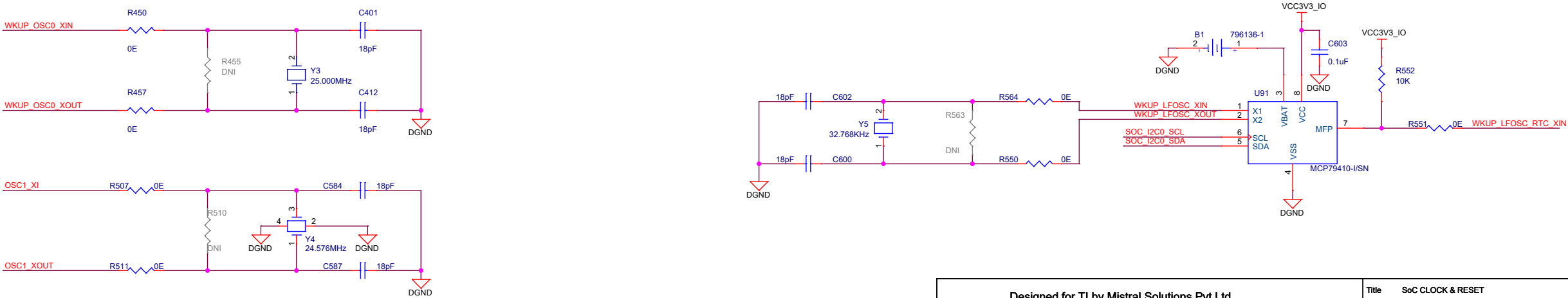
SoC WARM_RST



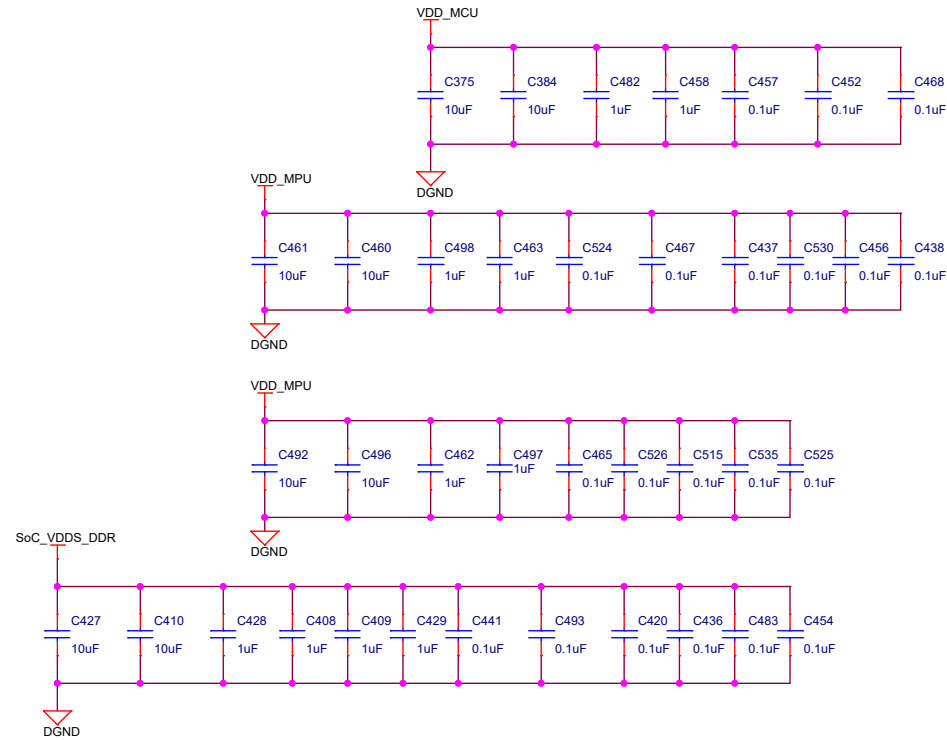
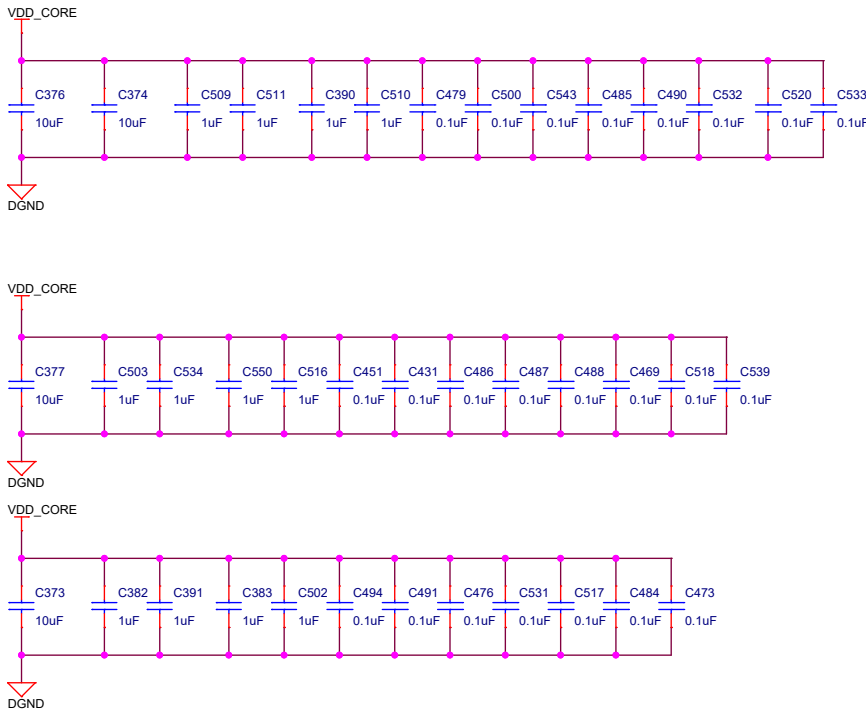
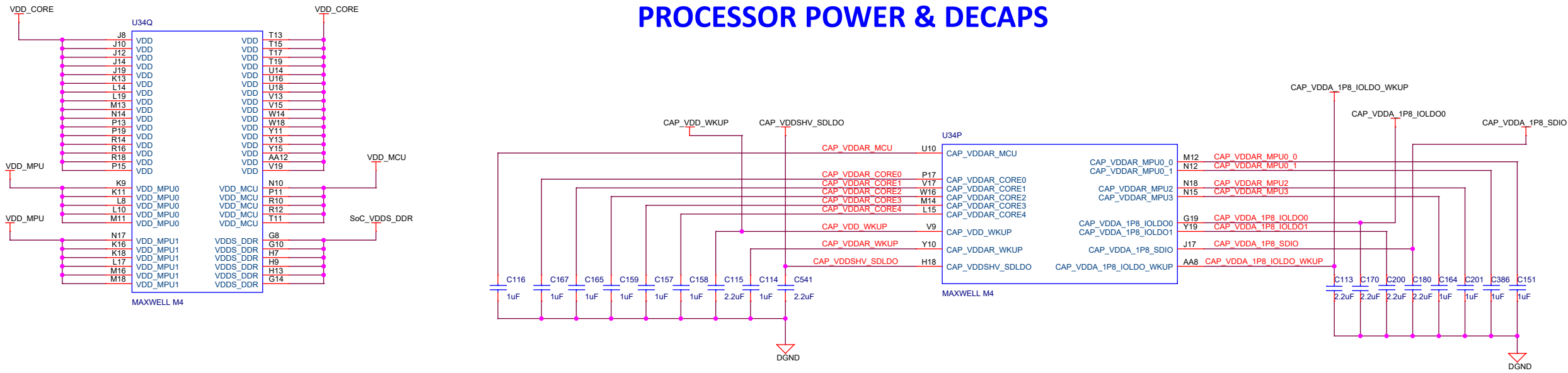
MCU_PUSH BUTTONS



SoC CLOCK



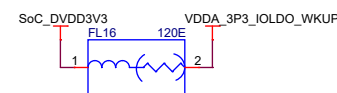
PROCESSOR POWER & DECAPS



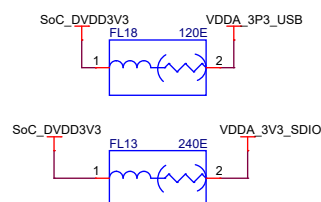
SoC POWER



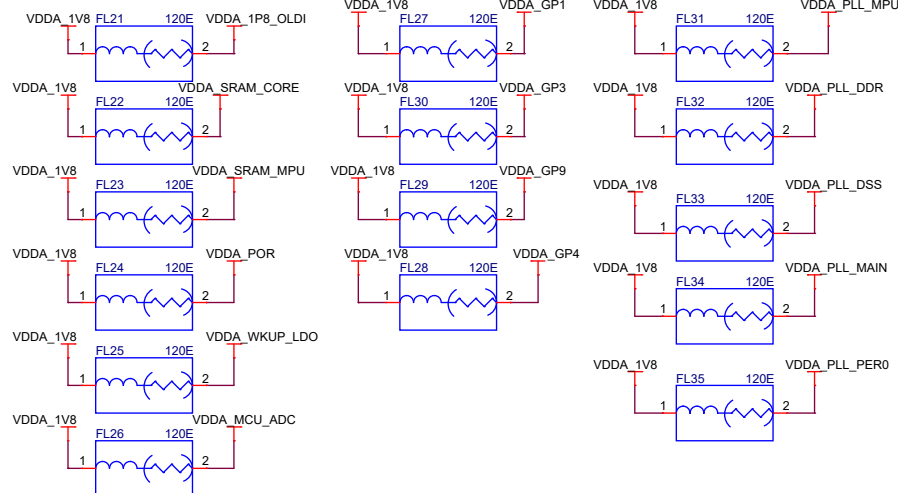
3.3V IO SUPPLY



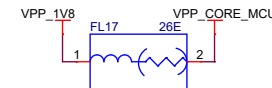
3.3V ANALOG SUPPLY



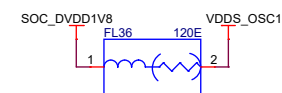
1.8V Analog SUPPLY



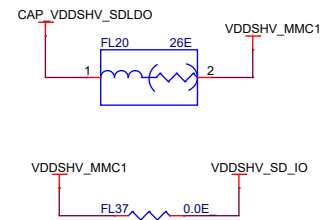
VPP SUPPLY



OSCILLATOR SUPPLY



MMC1 IO SUPPLY



CORE SUPPLY



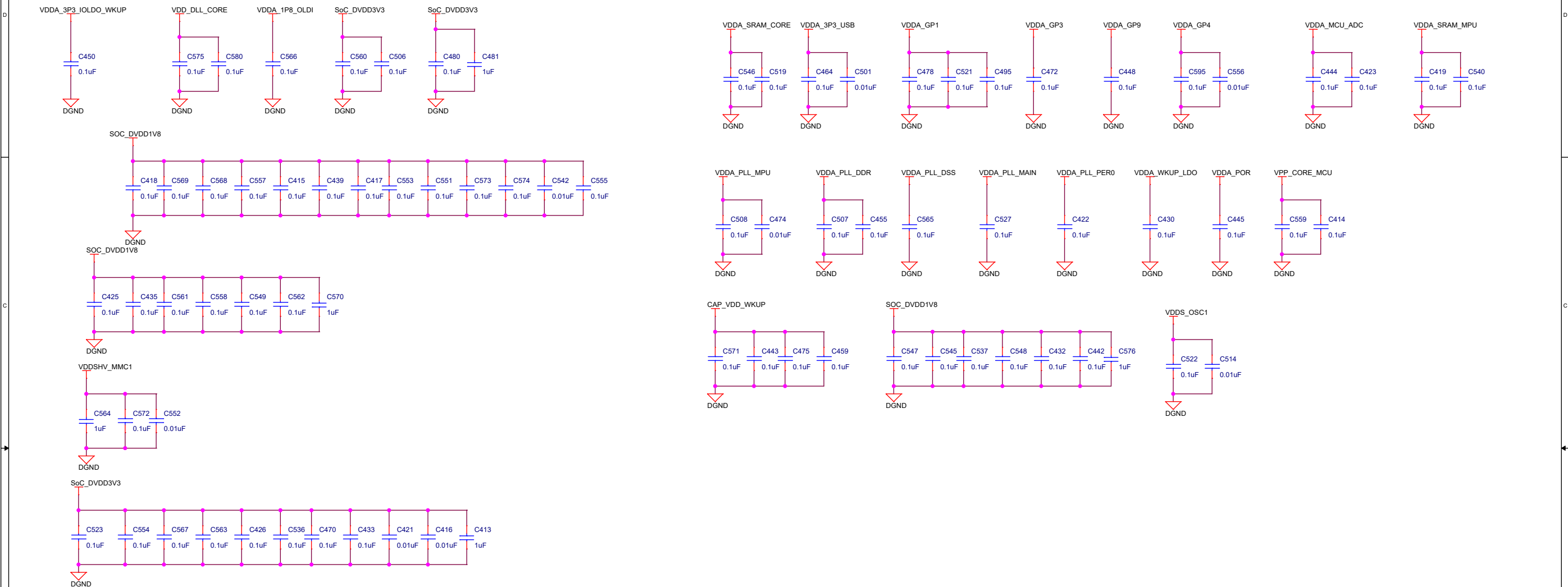
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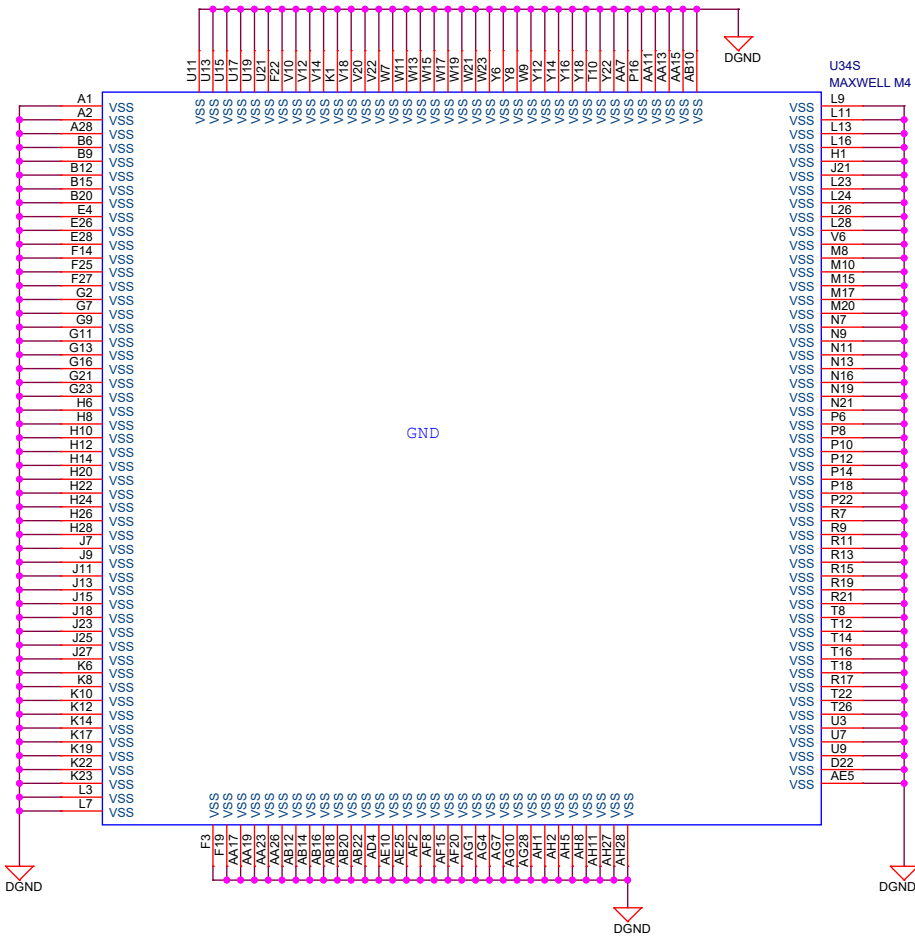
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Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
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PROCESSOR DECAPS



SoC POWER - VSS



1

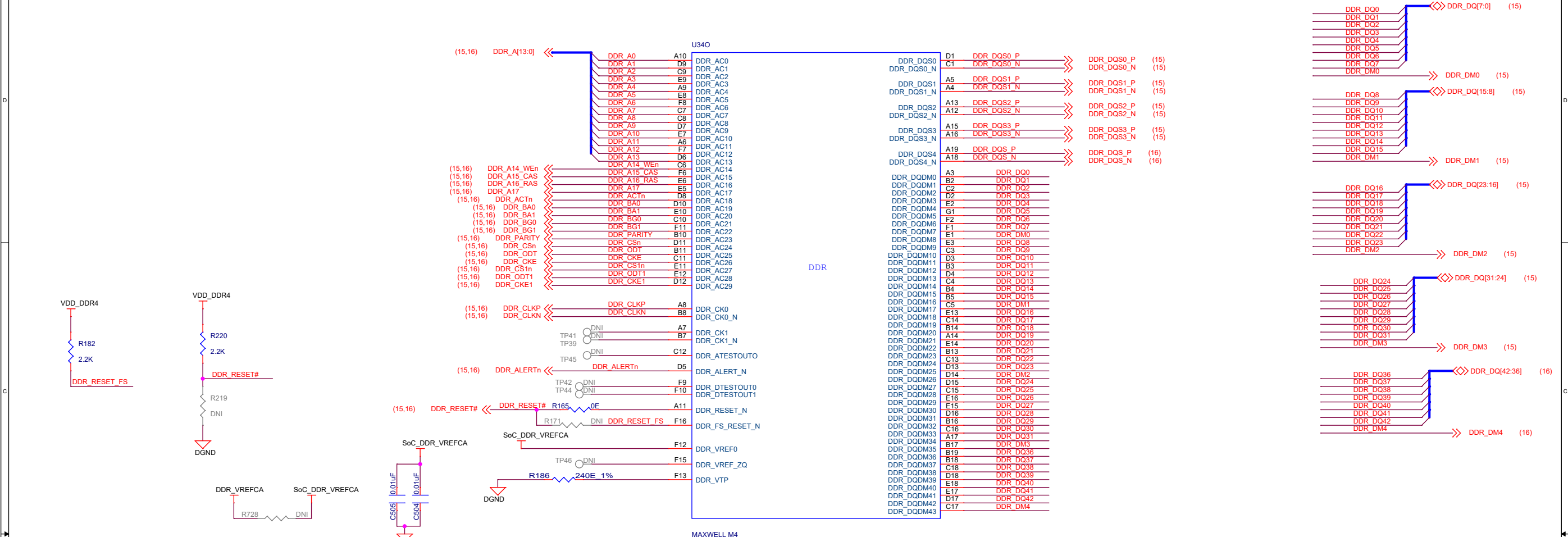


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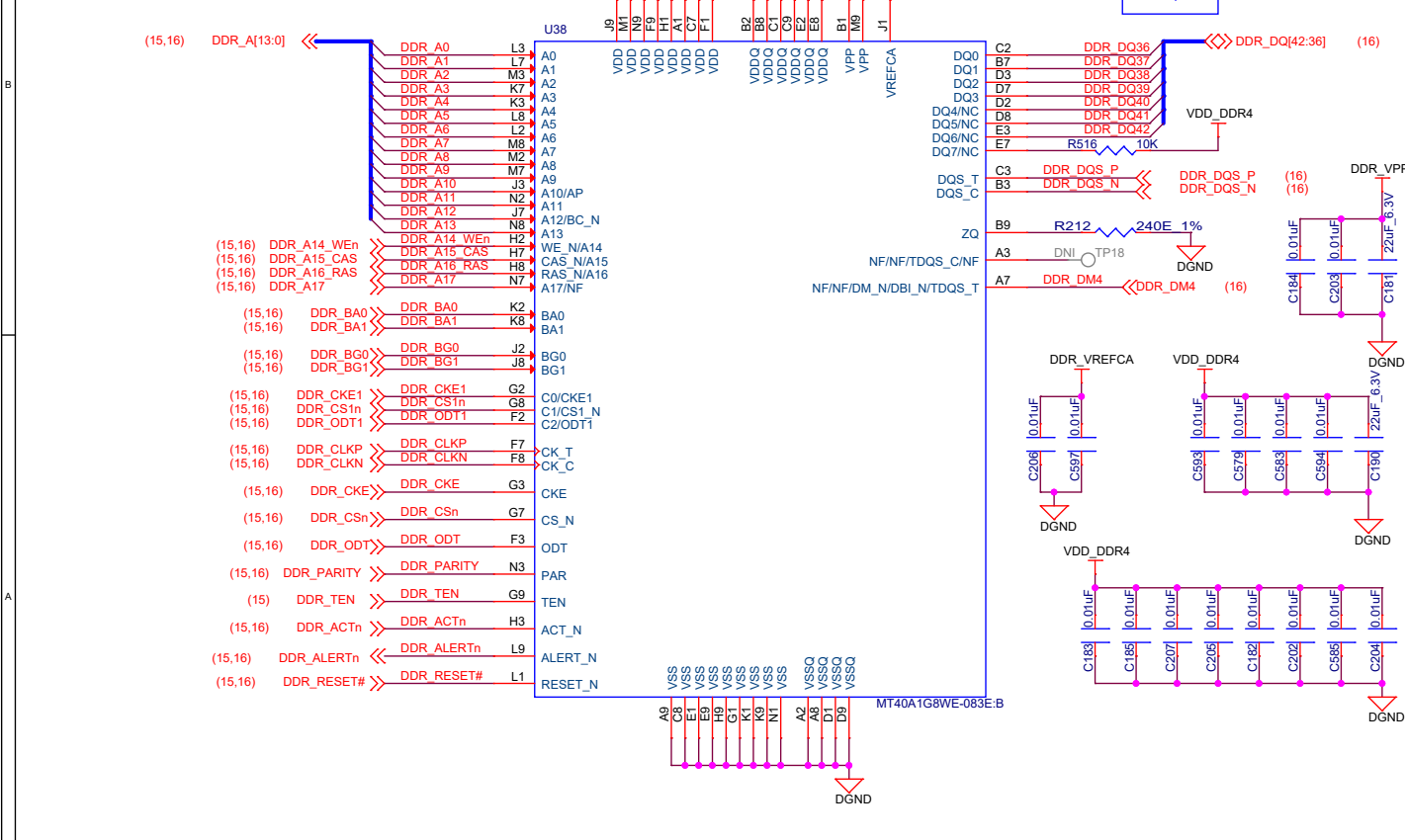




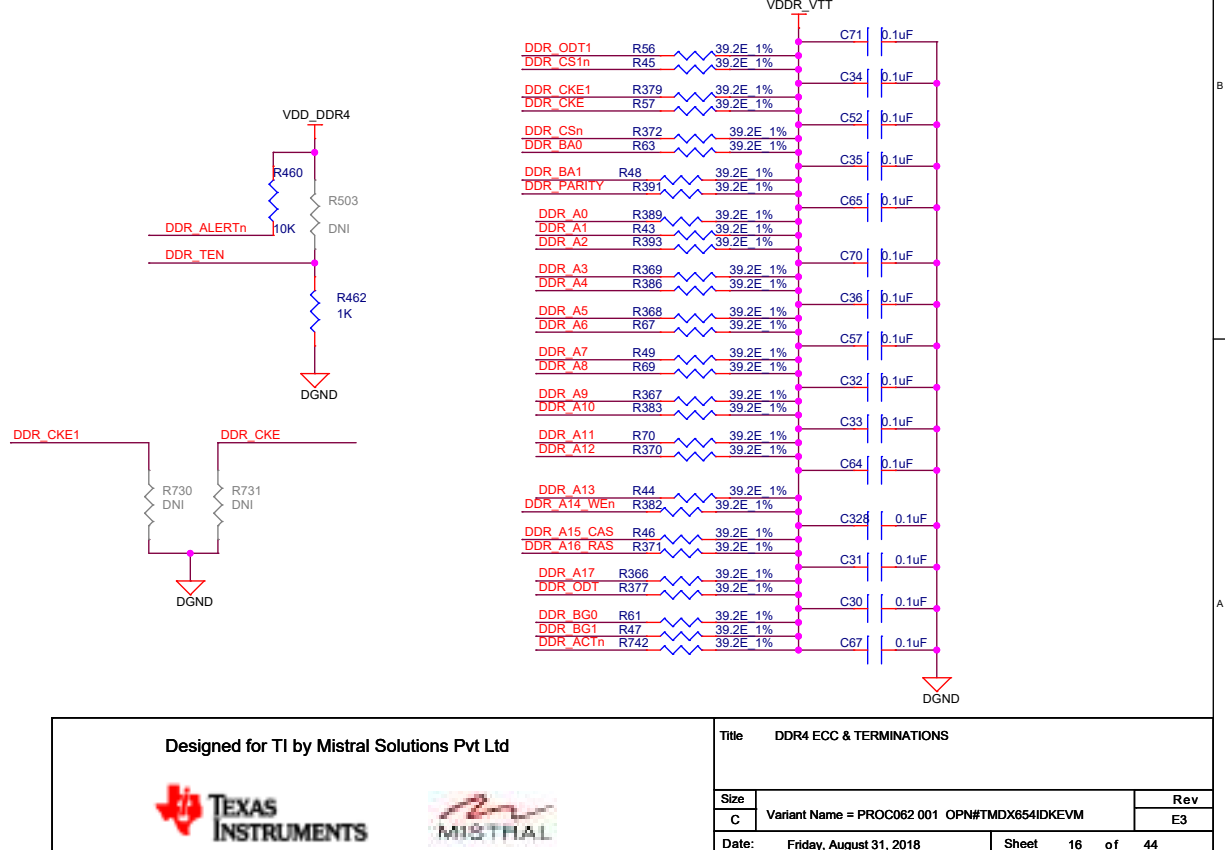
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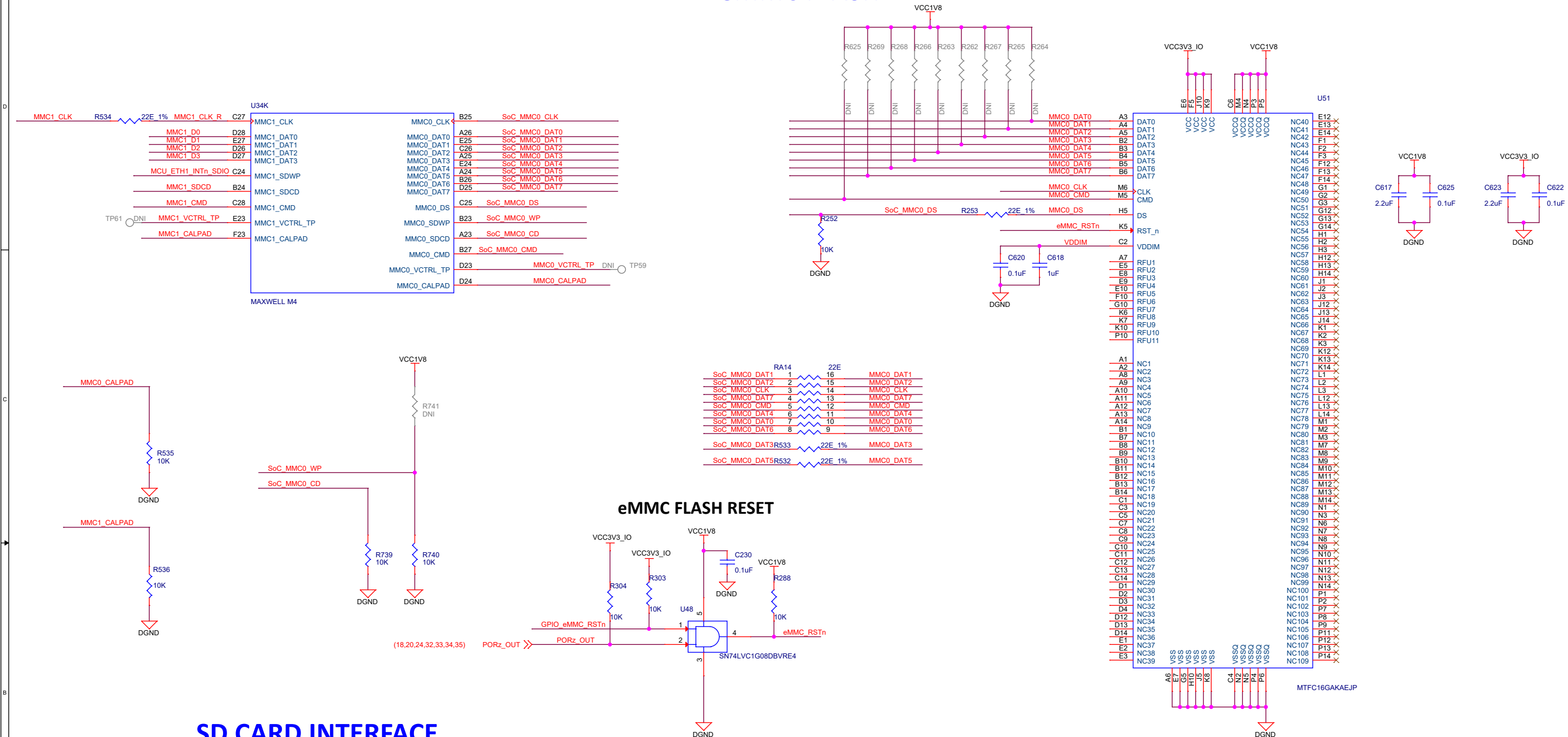
ECC DEVICE



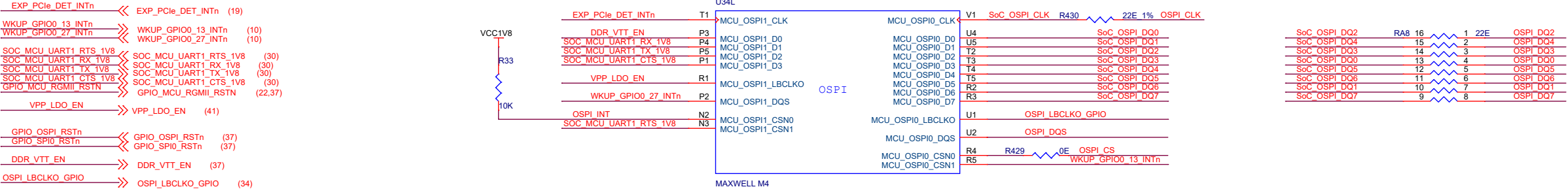
DDR TERMINATION



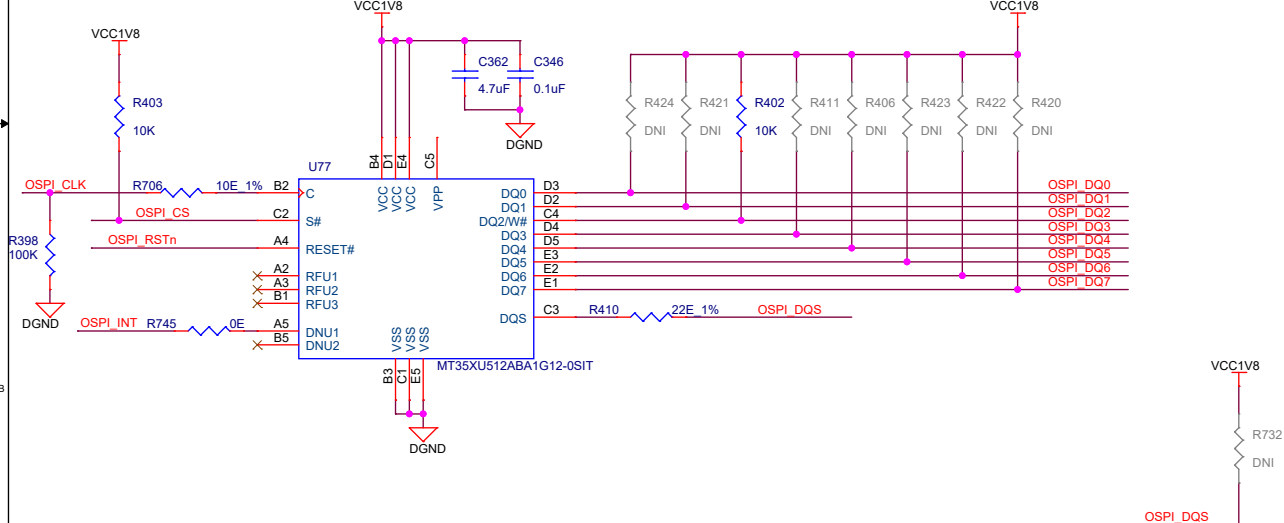
eMMC FLASH



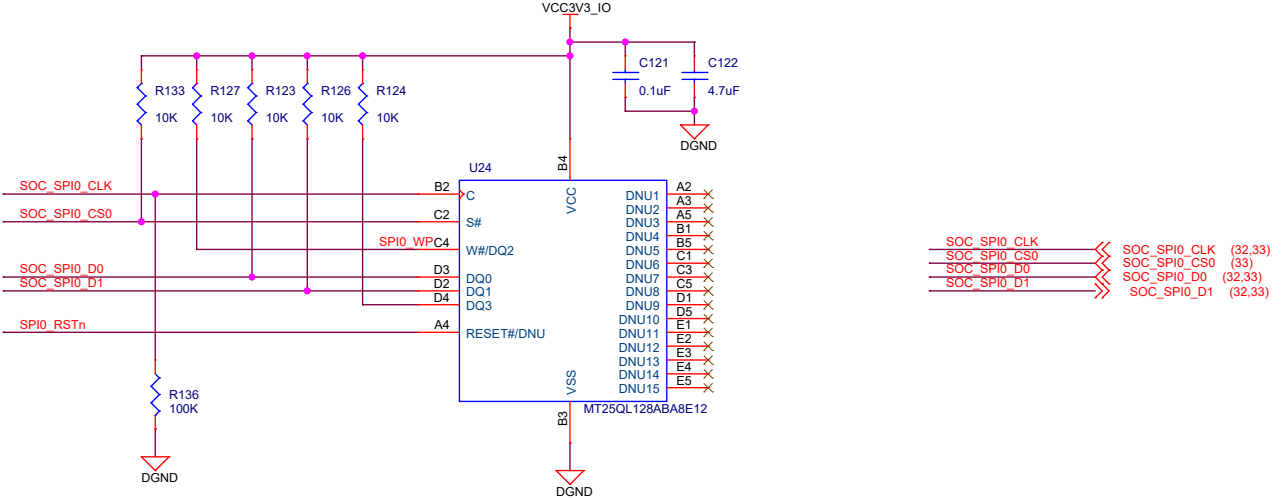
SOC OSPI INTERFACE



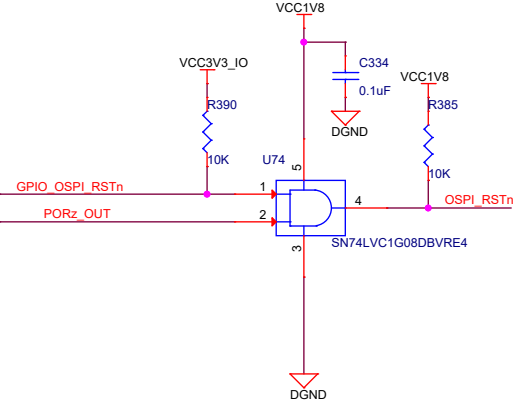
OSPI FLASH



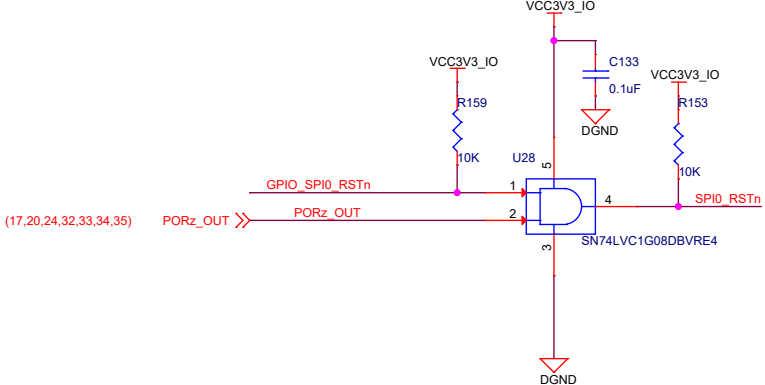
SPI NOR Flash



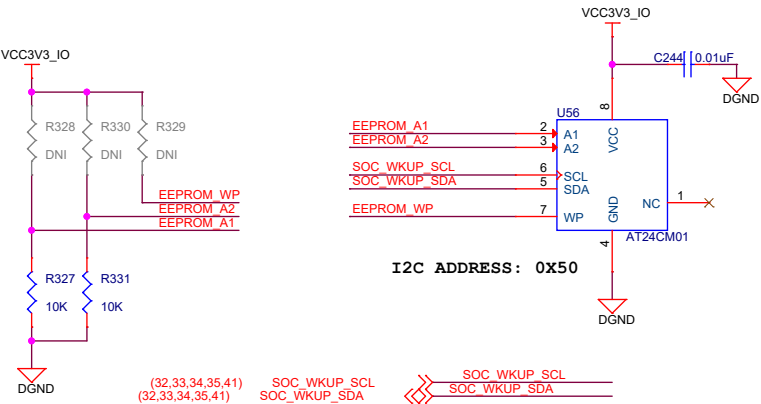
OSPI FLASH RESET



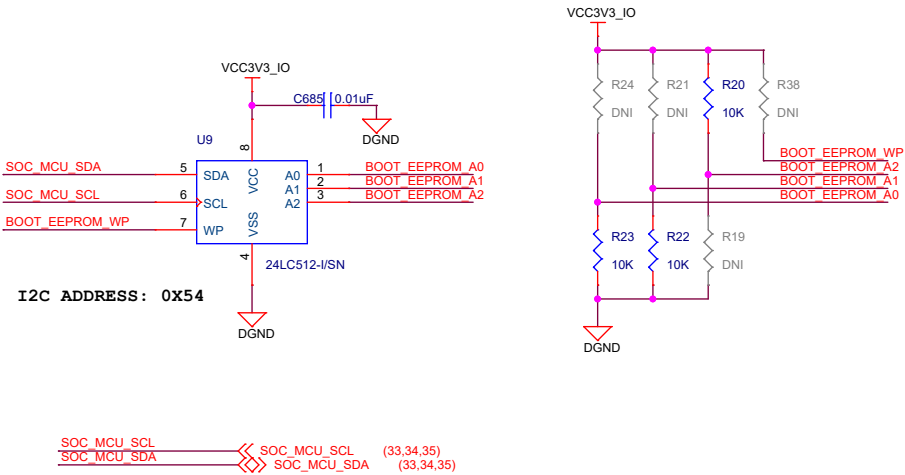
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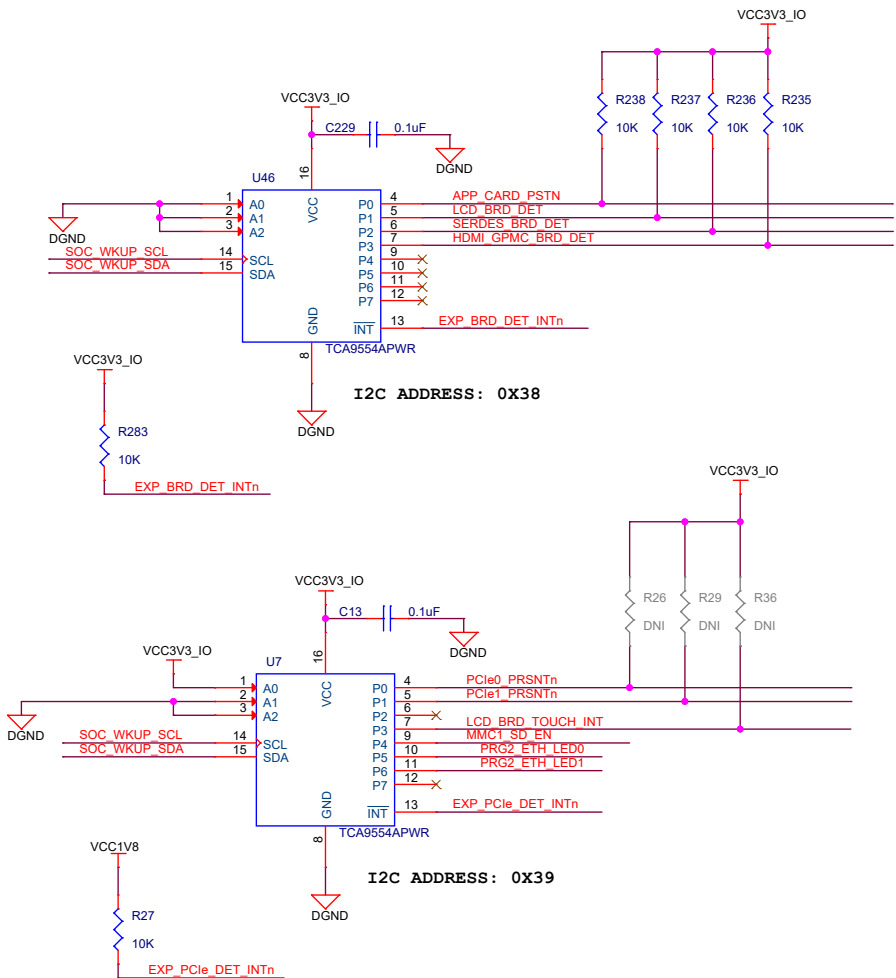
BOARD ID EEPROM



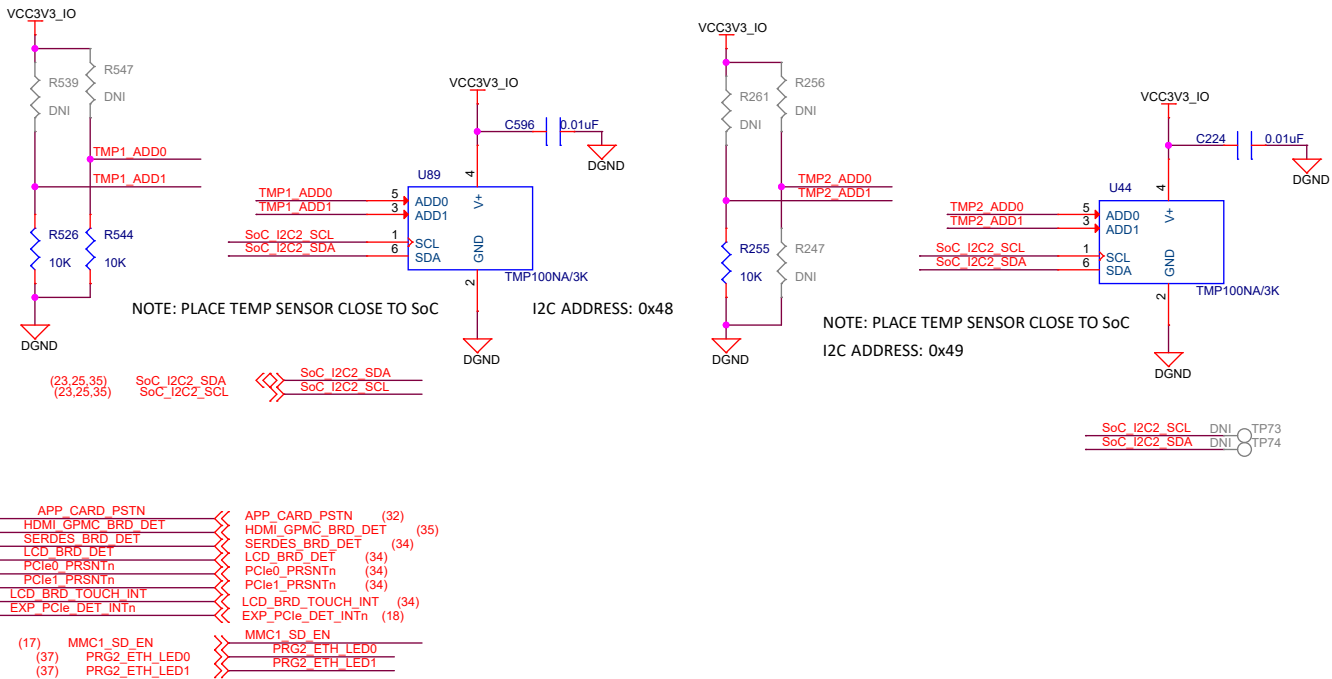
BOOT EEPROM



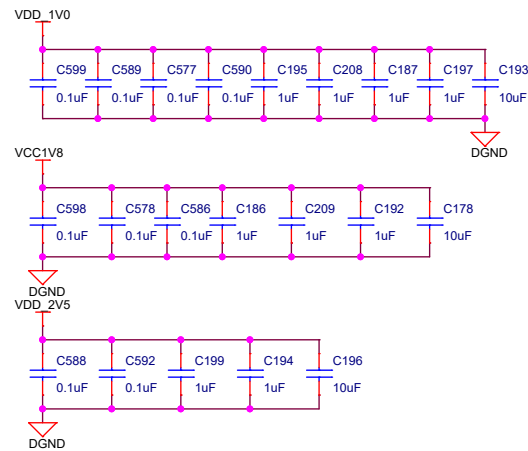
BOARD PRESENCE DETECT CIRCUIT



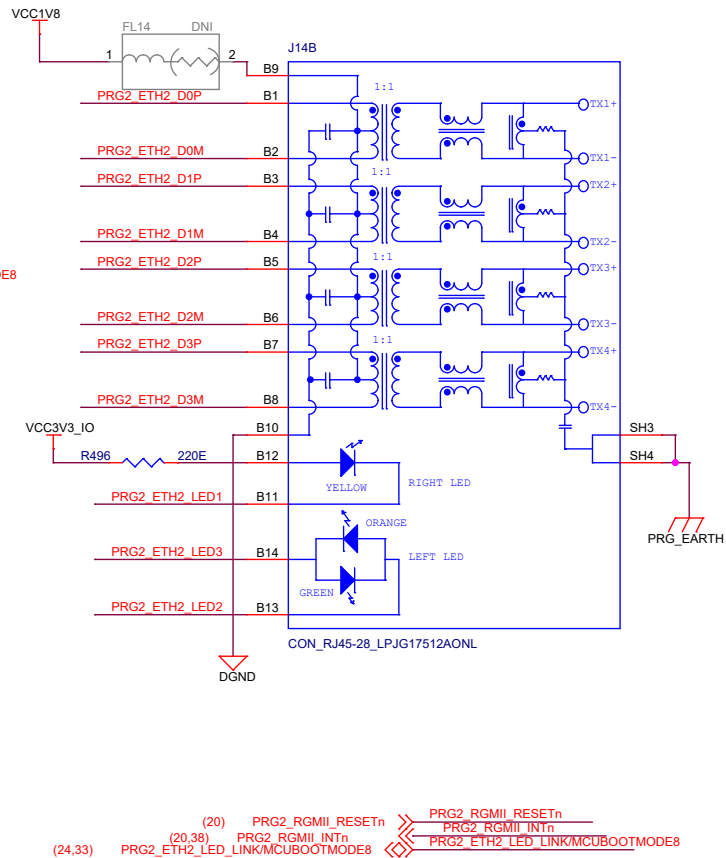
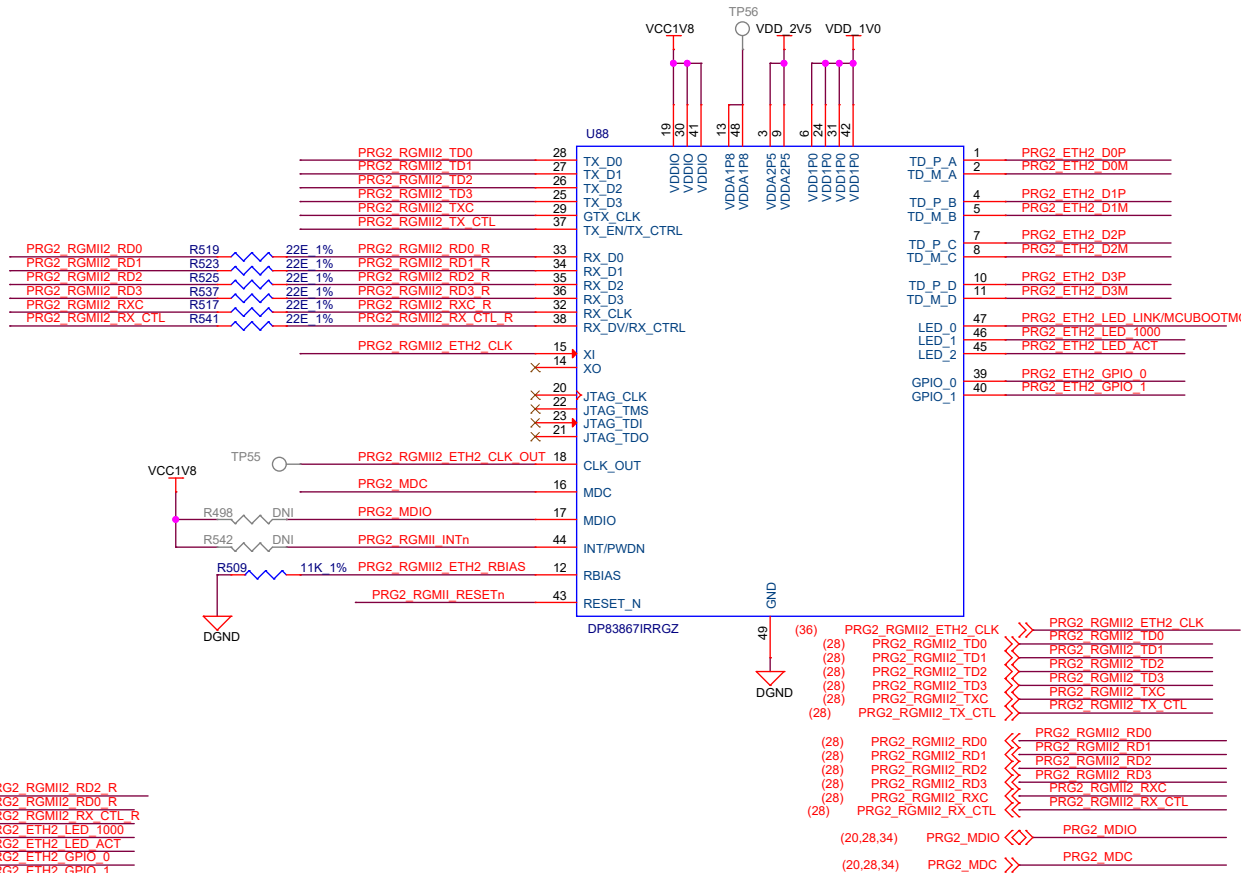
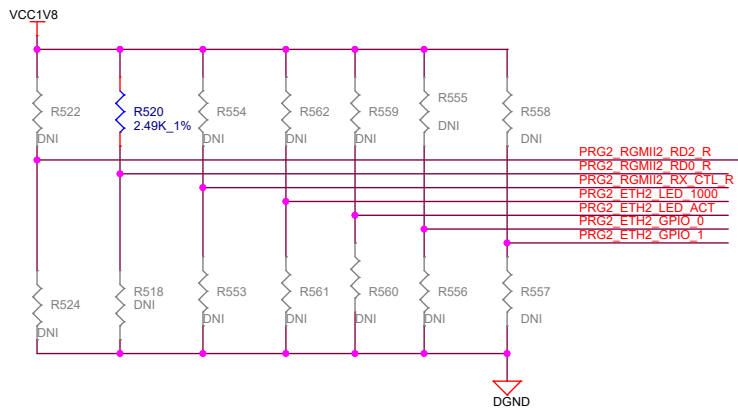
TEMPERATURE SENSOR



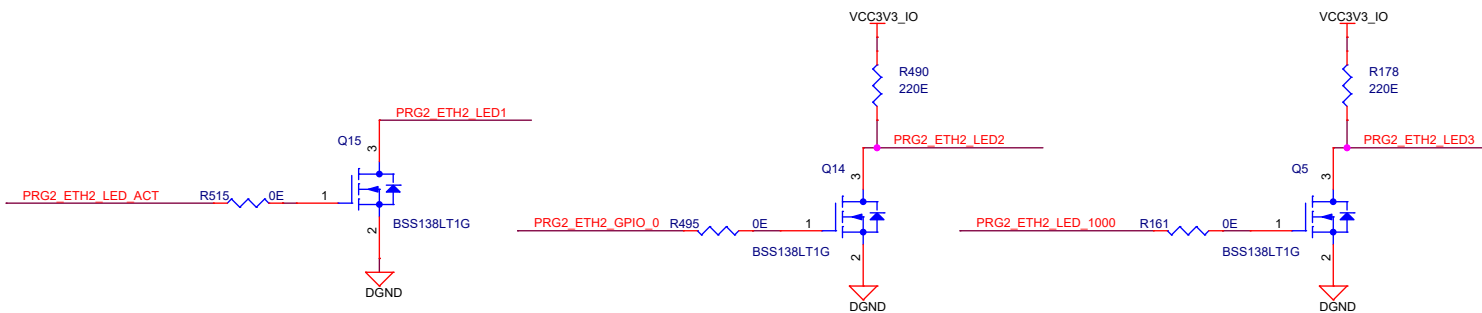
PRG2 RGMII 2



STRAPPING RESISTORS



PRG2_ETHERNET - 2 SPEED & ACTIVITY LED 's DRIVERS



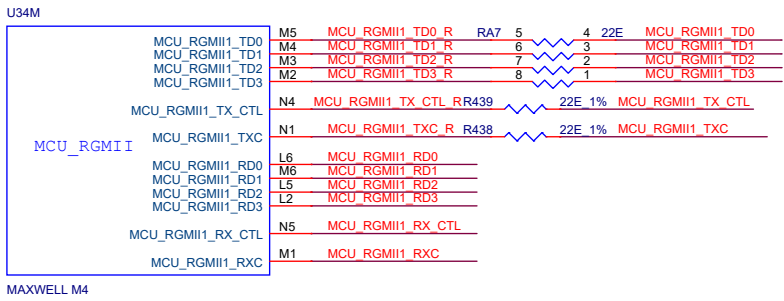
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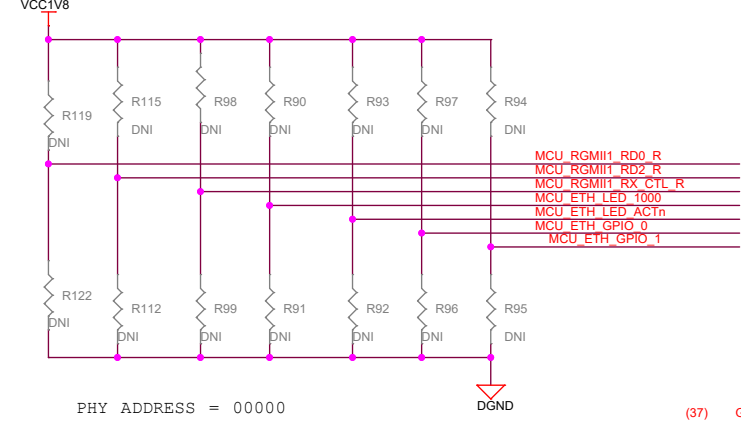
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Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
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RGMII ETHERNET PHY - MCU

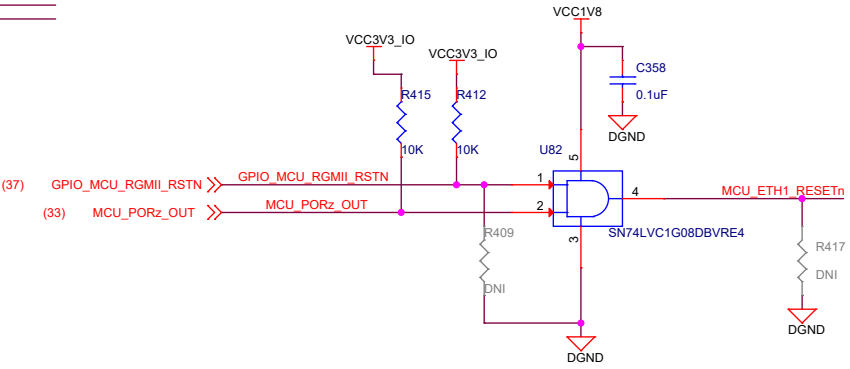
MCU_RGMII



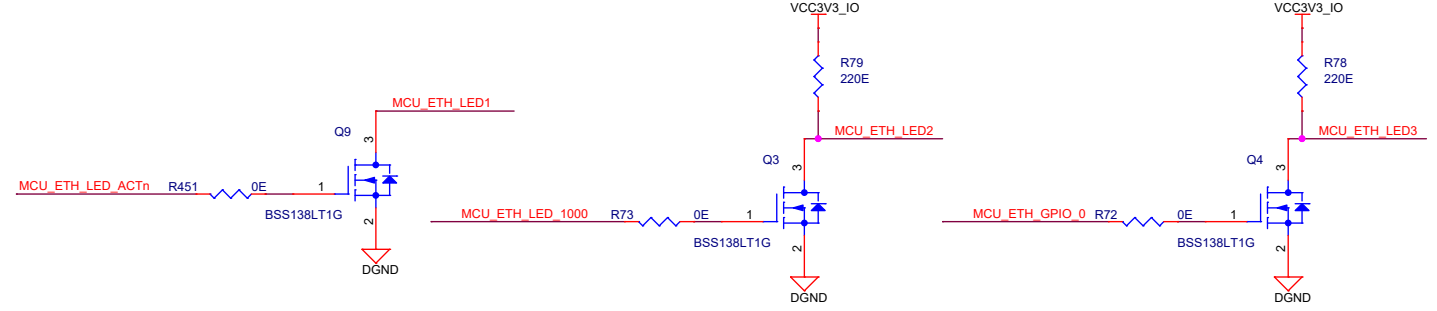
STRAPPING



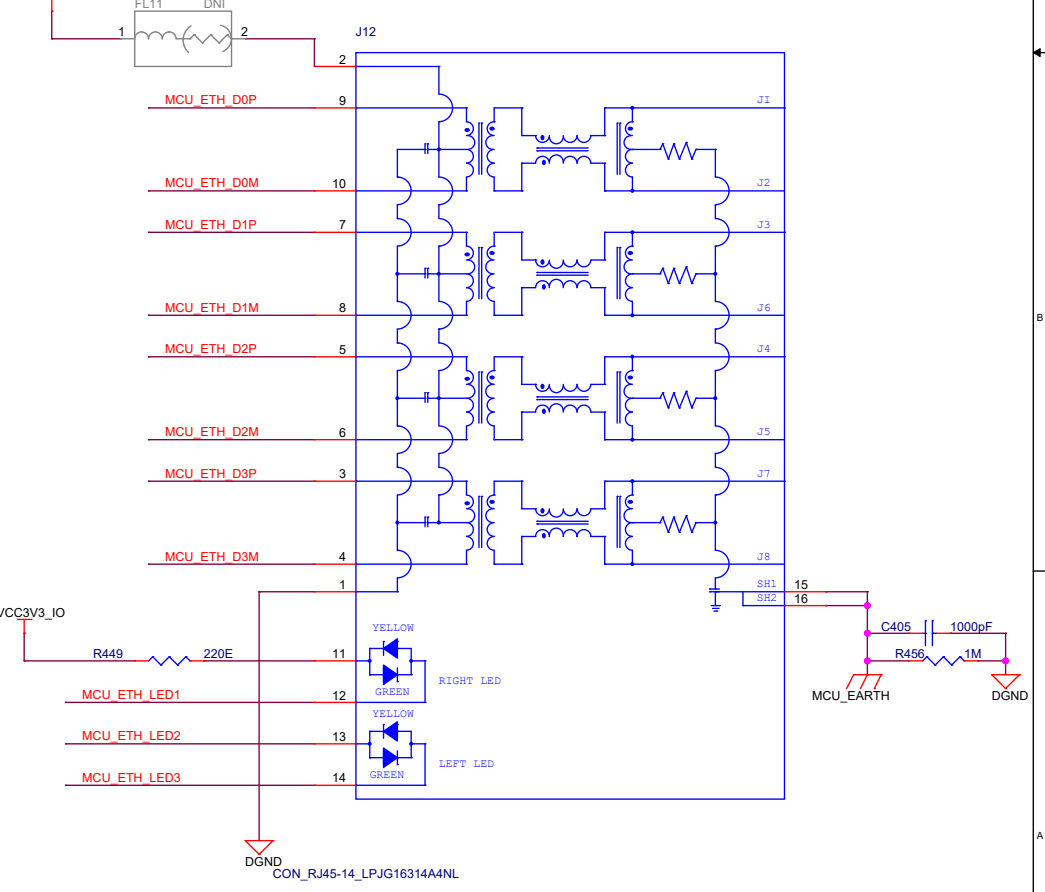
PHY_RESET



MCU SPEED & ACTIVITY LED DRIVERS



RJ45 with Integrated Magnetics



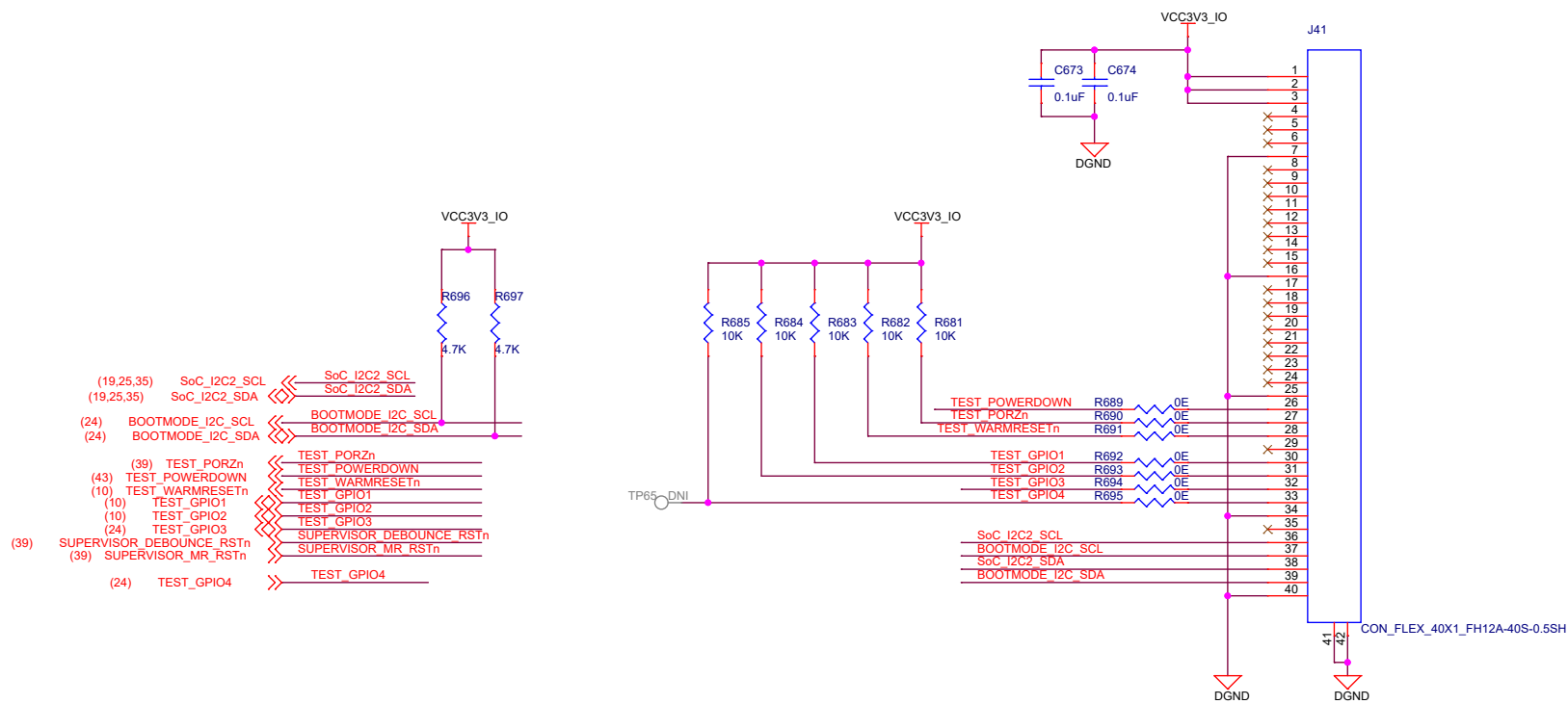
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Size			Rev	
C	Variant Name = PROC062 001 OPN#TMDX654IDKEVM		E3	
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TEST AUTOMATION

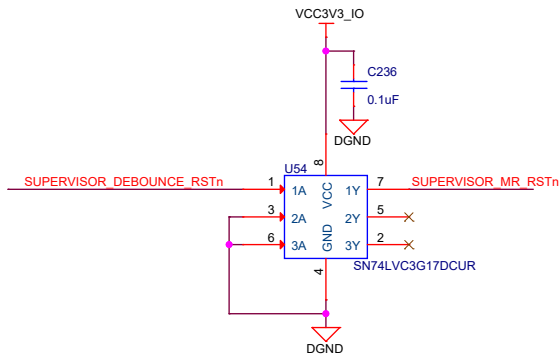
40-PIN AUTOMATION HEADER



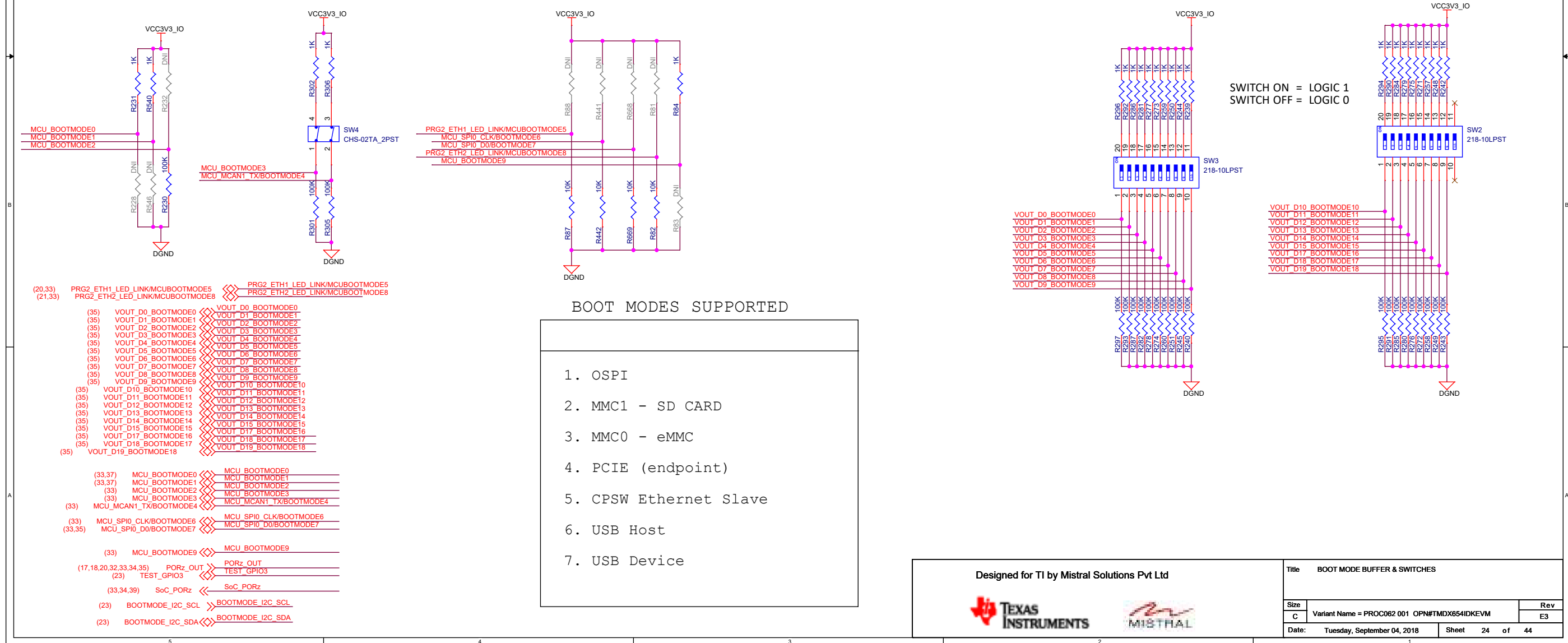
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on WKUP_GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Used to Generate the interrupt on WKUP_GPIO0_27_INTn	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

DEBOUNCE CIRCUIT



BOOT CONFIGURATION SETTINGS



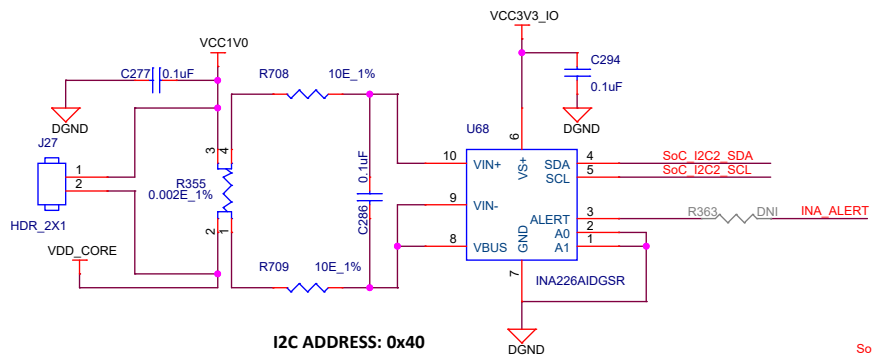
1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. PCIE (endpoint)
5. CPSW Ethernet Slave
6. USB Host
7. USB Device



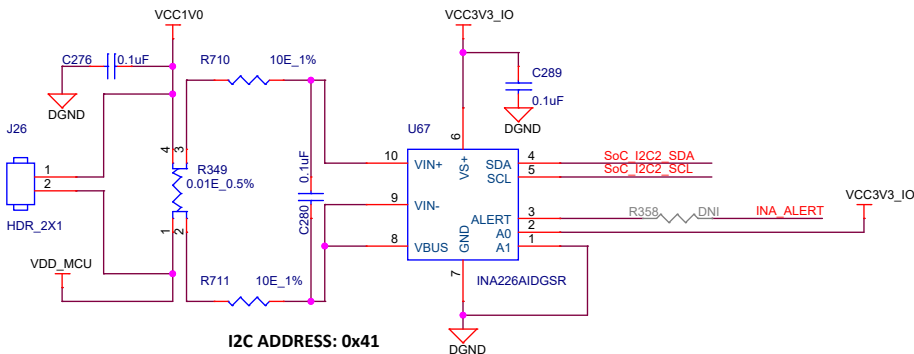
Date:	Tuesday, September 04, 2018	Sheet	24	of	44
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CURRENT MONITORING DEVICES

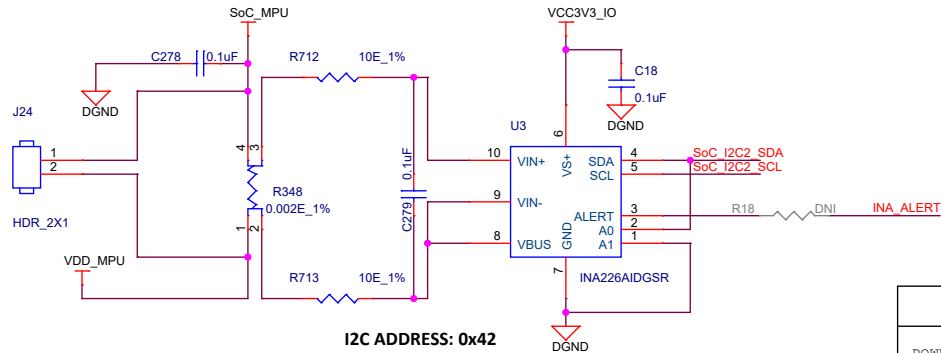
VDD_CORE



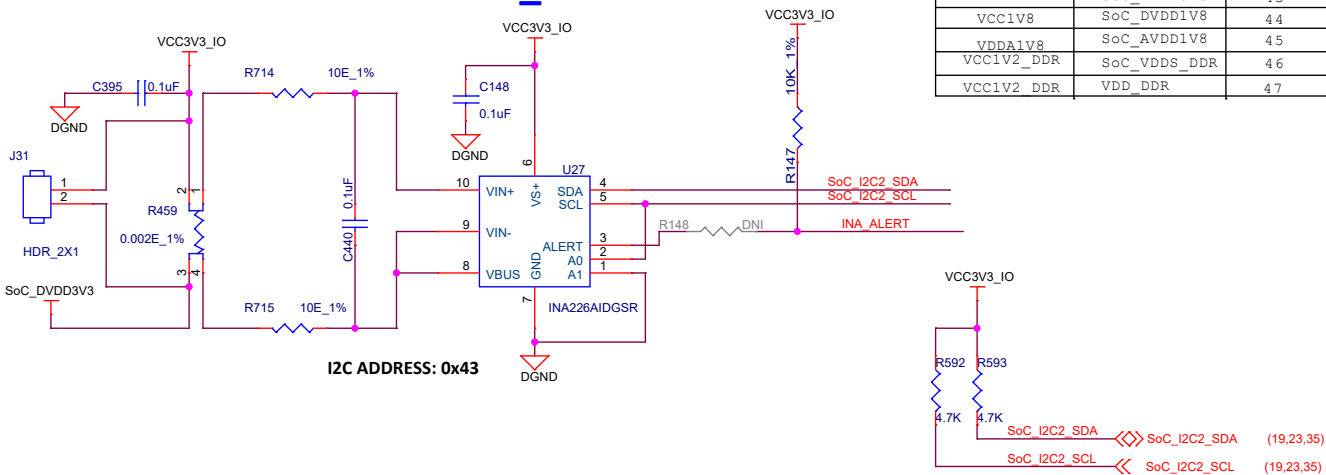
VDD_MCU



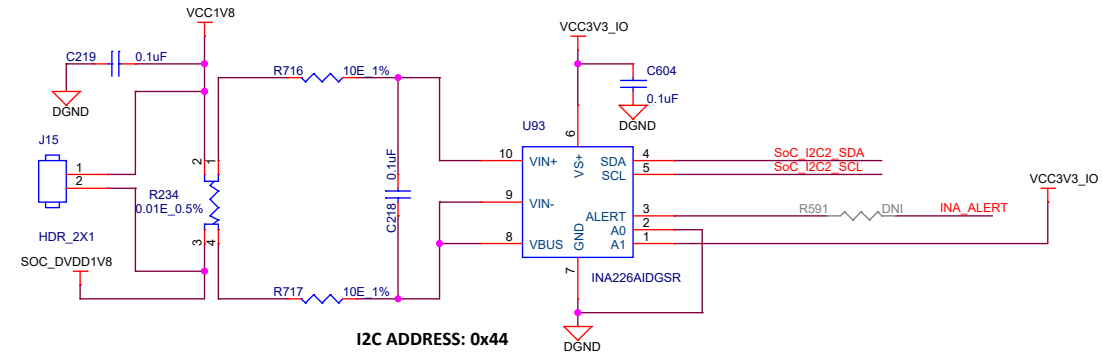
VDD_MPU



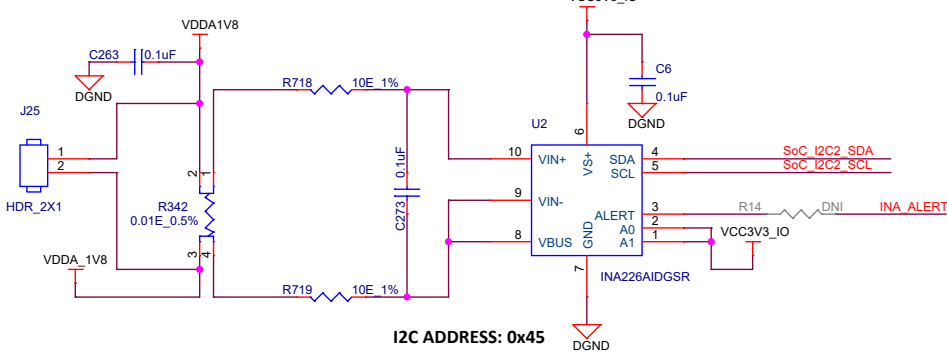
SoC_DVDD3V3



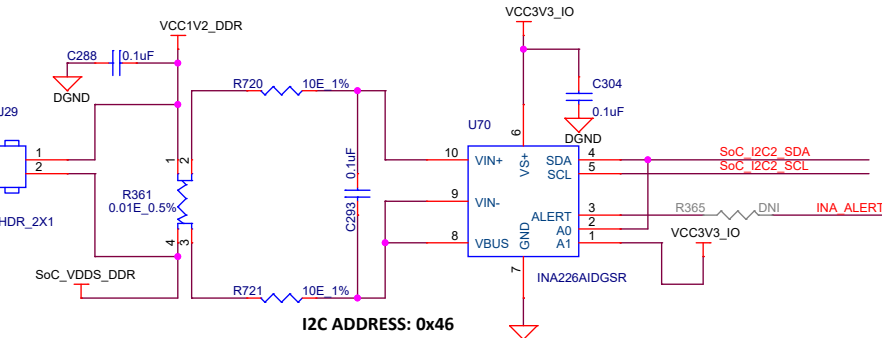
SoC_DVDD1V8



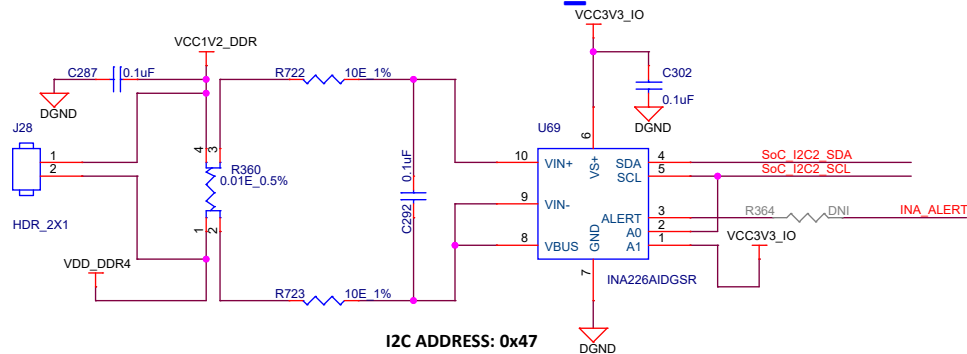
SoC_AVDD1V8



SoC_VDDS_DDR



VDD_DDR



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Title CURRENT MONITORING DEVICES

Size Variant Name = PROC062 001 OPN#TMDX654IDKEVM

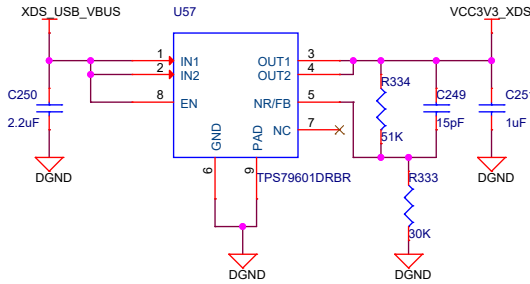
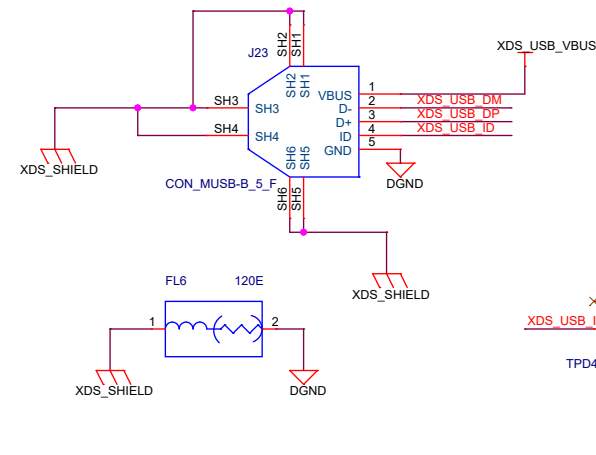
Date: Tuesday, July 24, 2018

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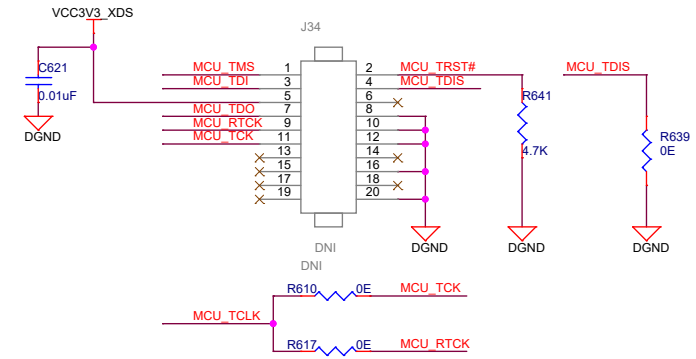
Rev E3

XDS110 POWER

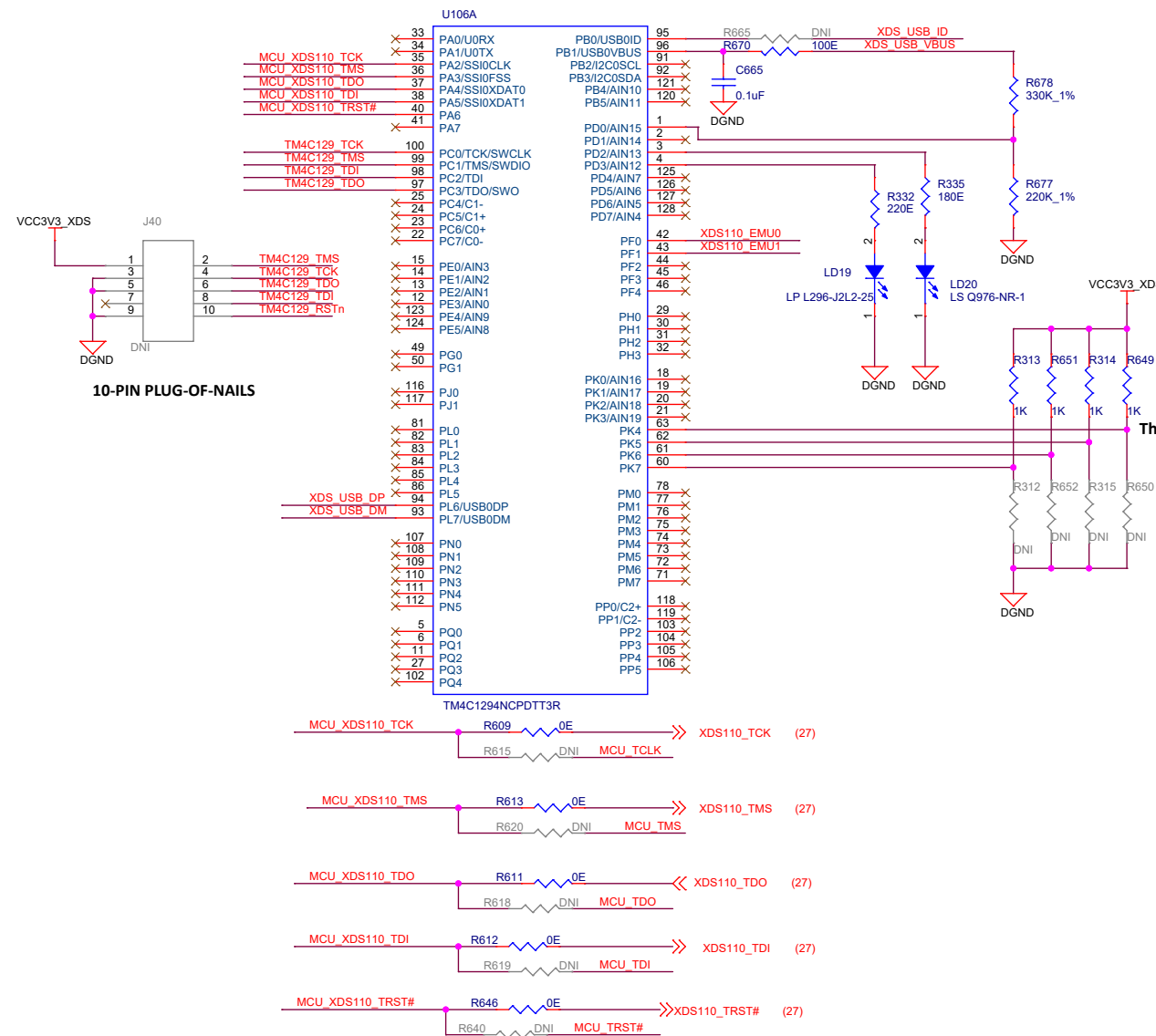
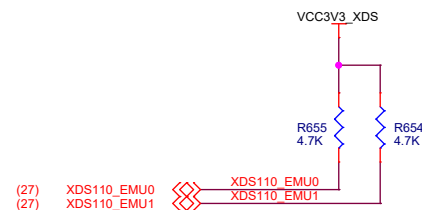
USB Connector



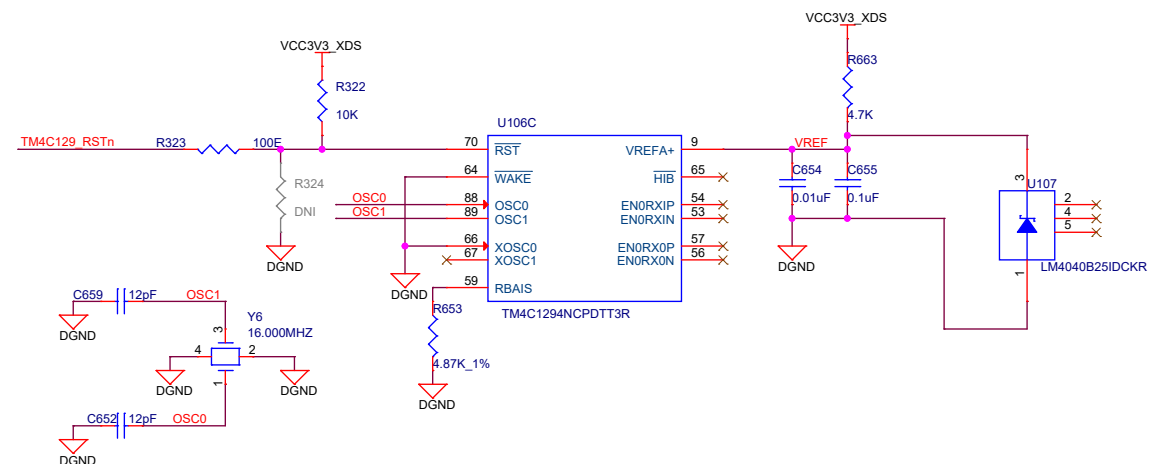
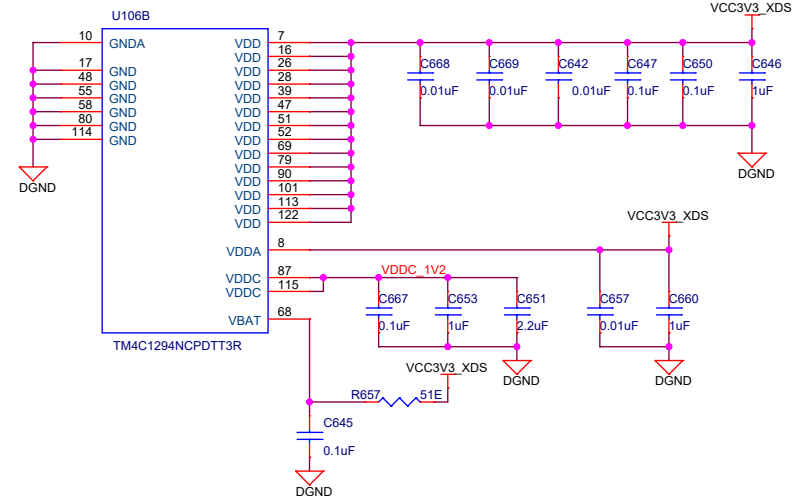
CTI 20 Pin Header external probe



XDS110 DEBUGGER



This will indicate the unique ID of the Debugger



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Title XDS110 DEBUGGER

Size
C Variant Name = PROC062 001 OPN#TMDX654IDKEVM

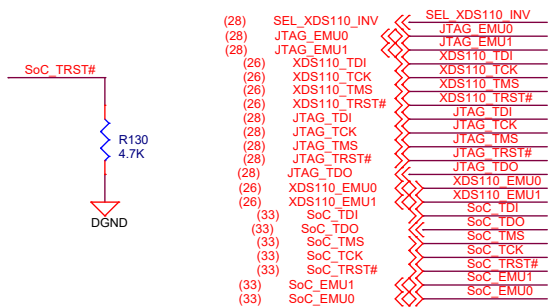
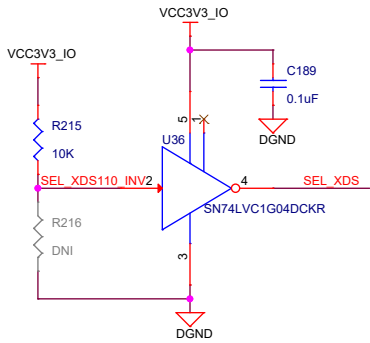
Rev
E3

Date: Friday, August 31, 2018

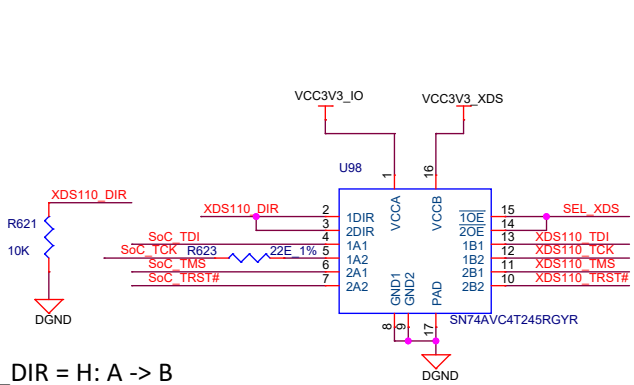
Sheet 26 of 44

0- Ohm Res MUX between XDS110 JTAG and MCU cti 20 pin connector.
-For XDS110 JTAG R609,R613,R611,R612 and R646 Should be installed and R615,R620,R618,R619 and R640 Should be DNI'd.
-For MCU cti 20 pin , R615,R620,R618,R619 and R640 Should be installed and R609,R613,R611,R612 and R646 Should be DNI'd.

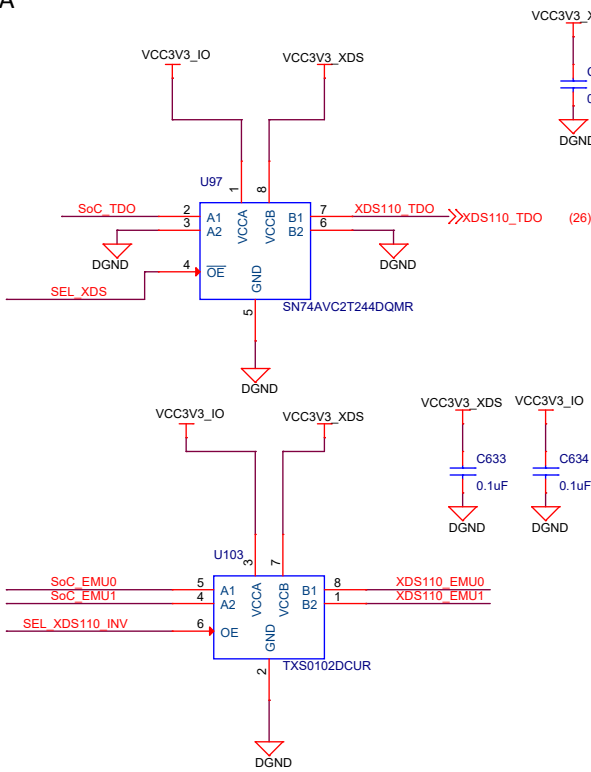
JTAG BUFFER



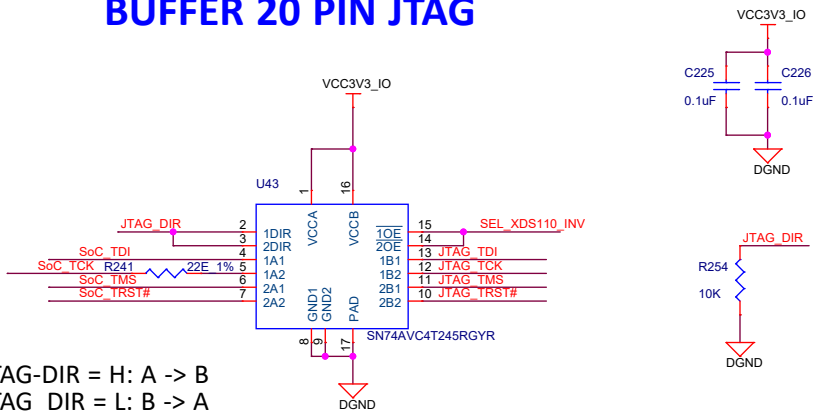
BUFFER XDS110



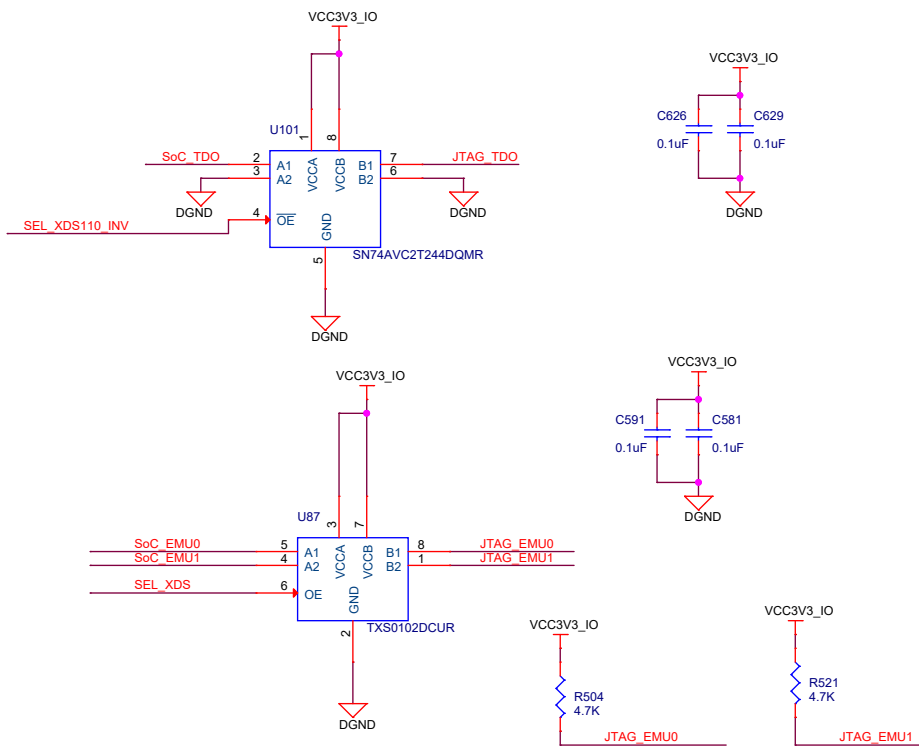
XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z



BUFFER 20 PIN JTAG



JTAG-DIR = H: A -> B
JTAG-DIR = L: B -> A
OE = H: output = Hi-Z



Designed for TI by Mistral Solutions Pvt Ltd



Title JTAG BUFFER

Size Variant Name = PROC062 001 OPN#TMDX654IDKEVM

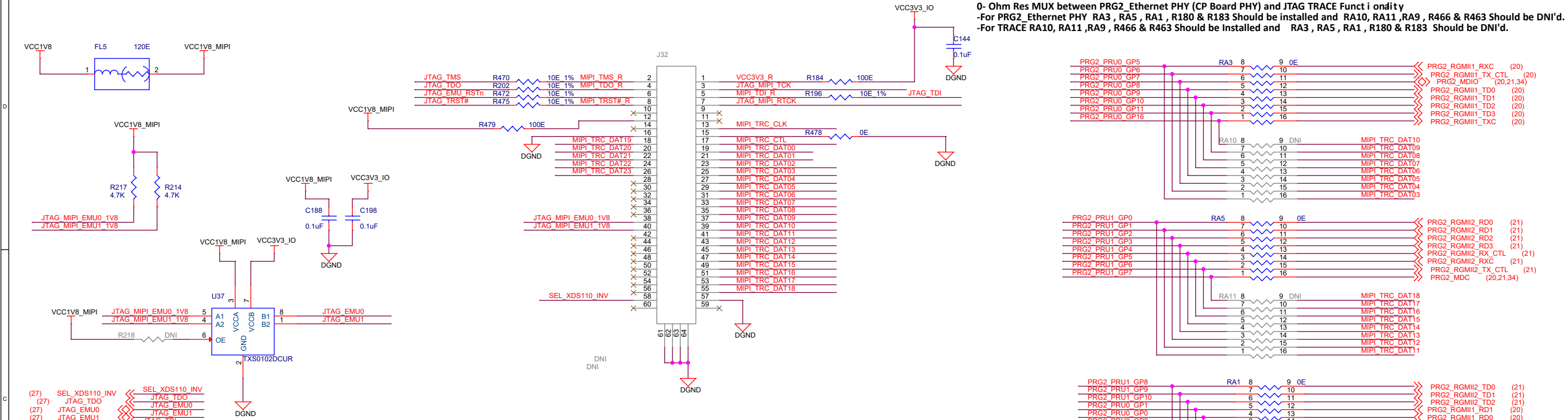
Date: Friday, August 31, 2018

Sheet 27 of 44

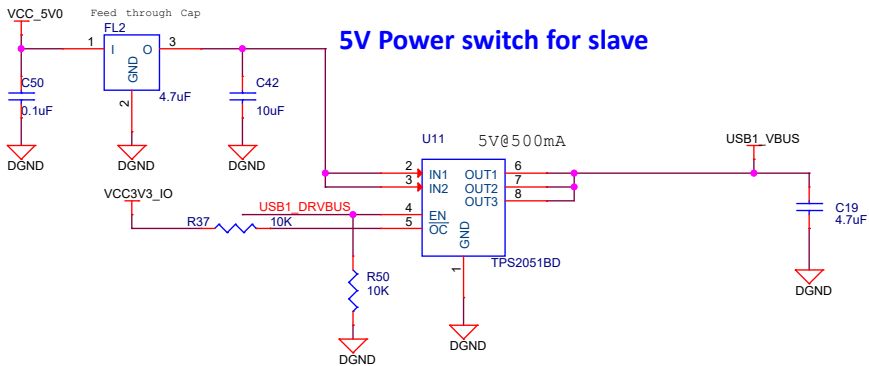
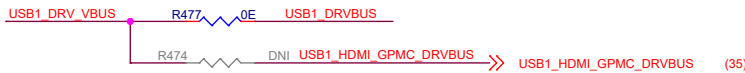
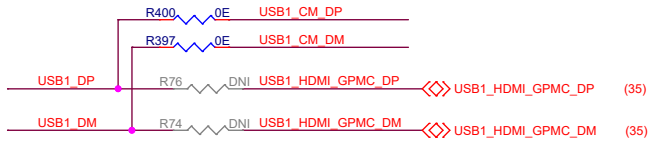
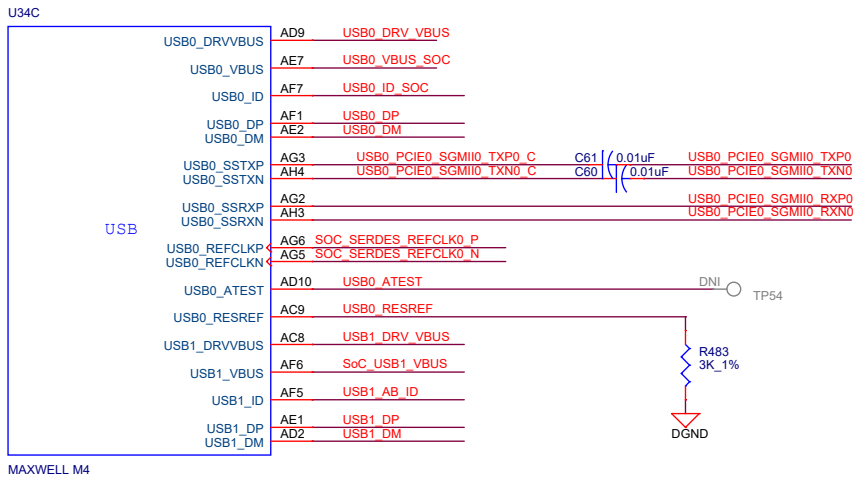
Rev E3

MIPI 60 PIN CONNECTOR

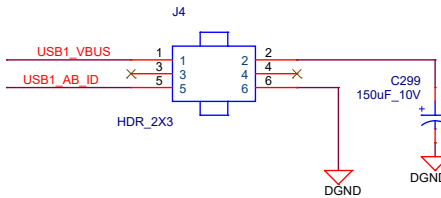
0- Ohm Res MUX between PRG2_Ethernet PHY (CP Board PHY) and JTAG TRACE Funct i ondi ty
-For PRG2_Ethernet PHY RA3 , RA5 , RA1 , R180 & R183 Should be installed and RA10, RA11 ,RA9 , R466 & R463 Should be DNI'd.
-For TRACE RA10, RA11 ,RA9 , R466 & R463 Should be Installed and RA3 , RA5 , RA1 , R180 & R183 Should be DNI'd.



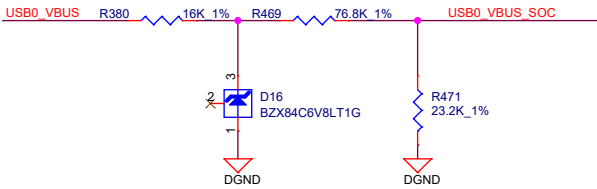
USB 2.0 INTERFACE



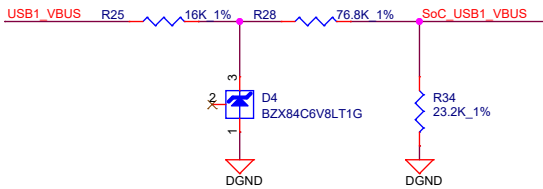
2X3 header to enable bulk capacitance on USB1_VBUS in host mode and to ground USB_AB_ID pin, if a non standard cable is used



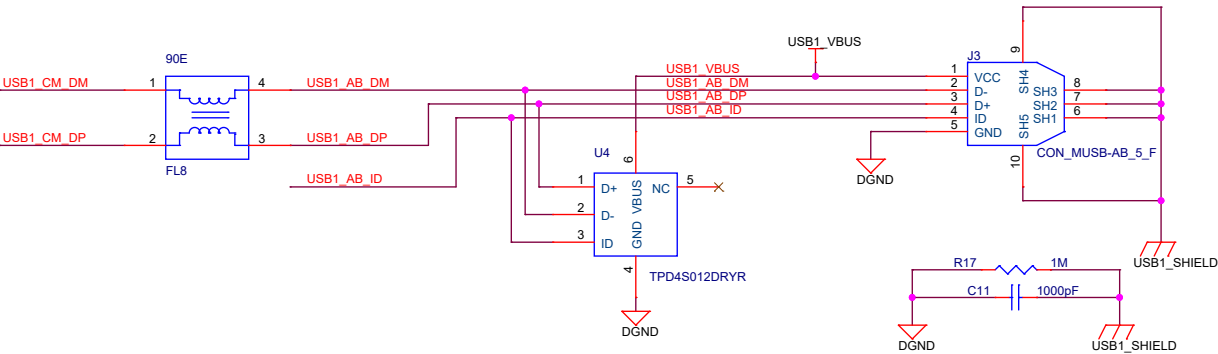
Resistor divider on SOC_VBUS



Resistor divider on SOC_VBUS



Micro USB 2.0 AB Connector



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Title USB 2.0 INTERFACE

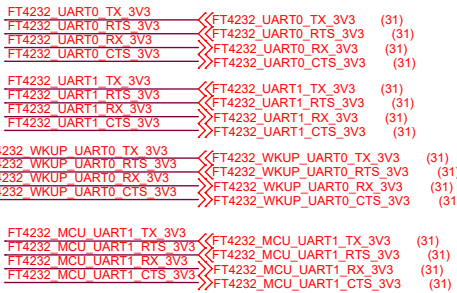
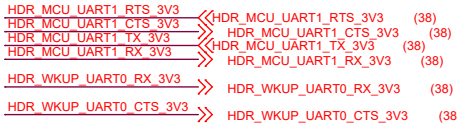
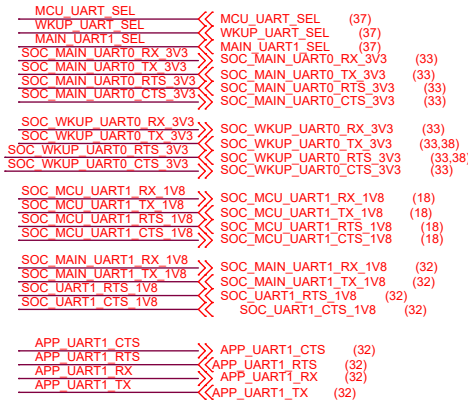
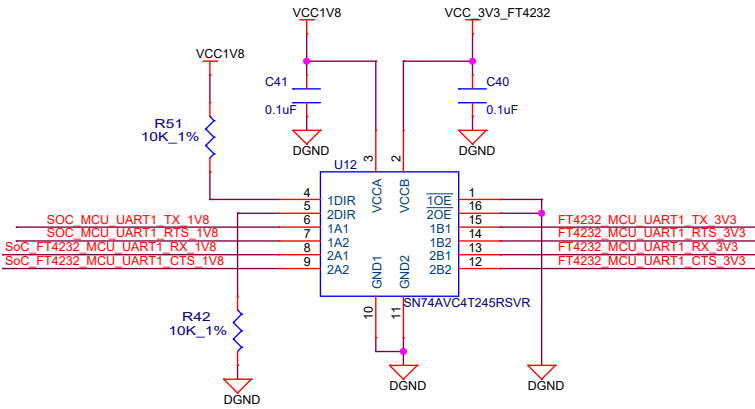
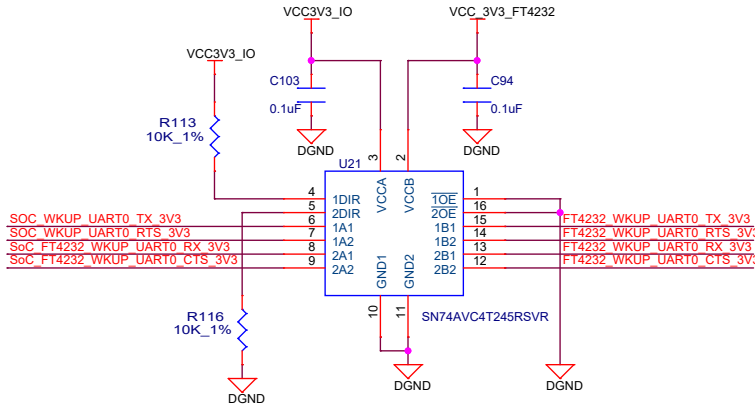
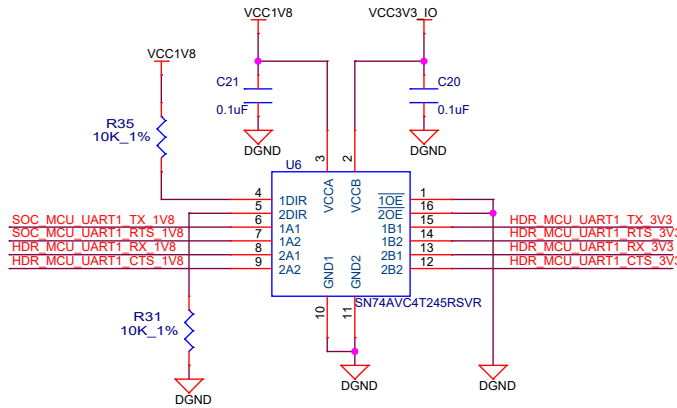
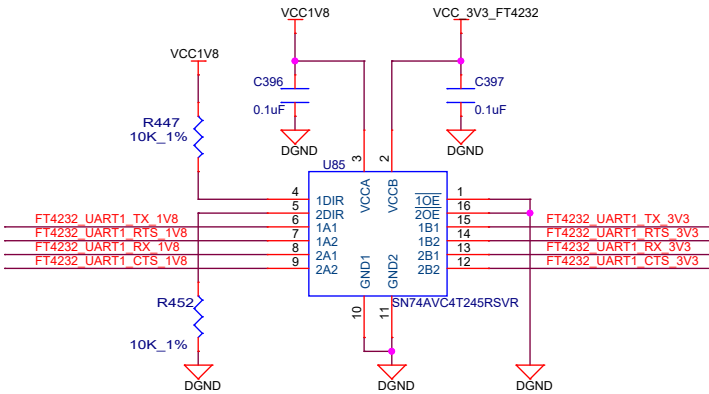
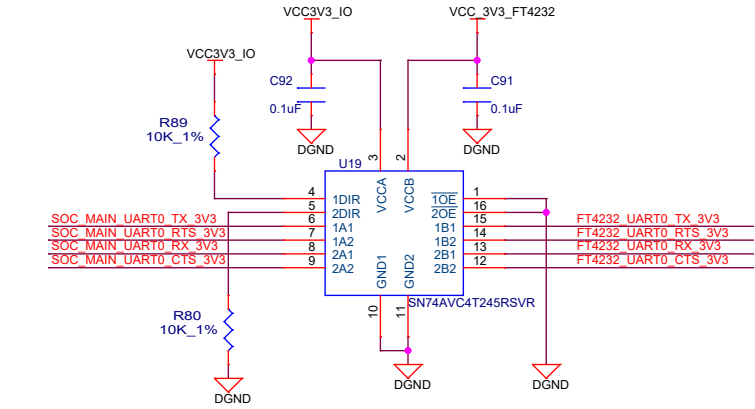
Size Variant Name = PROC062 001 OPN#TMDX654IDKEVM

Rev

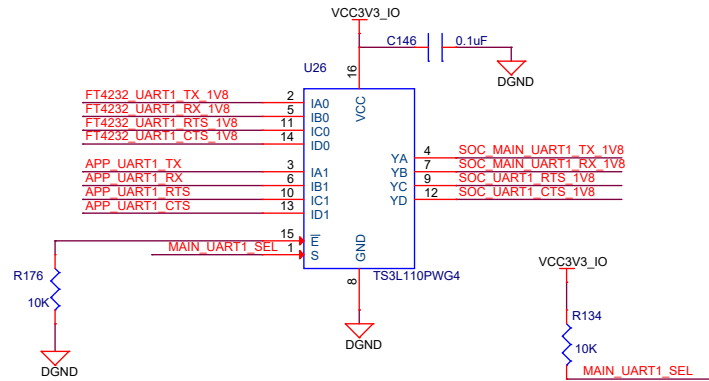
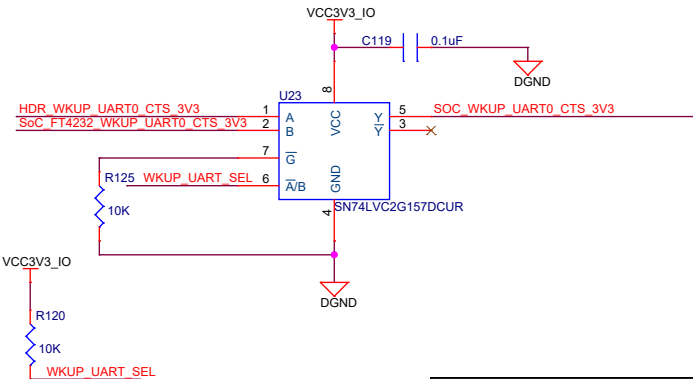
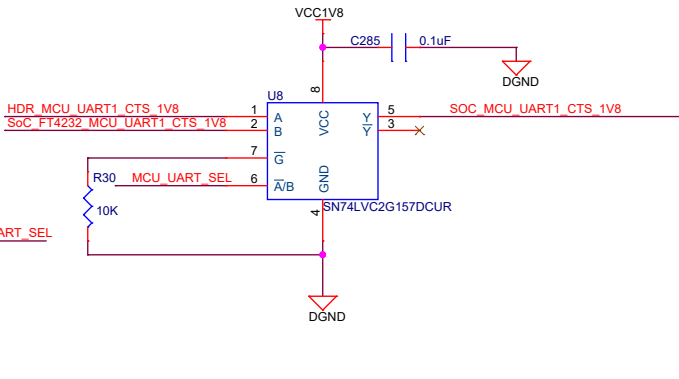
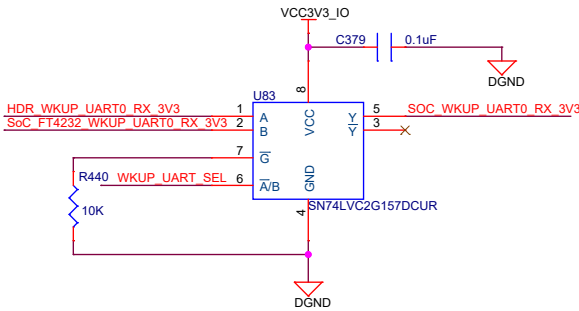
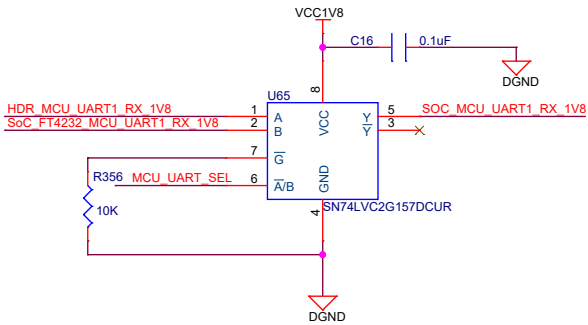
Date: Tuesday, July 24, 2018

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FT4232 LEVEL TRANSLATOR



2:1 MUX



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Title FT4232 LEVEL TRANSLATOR

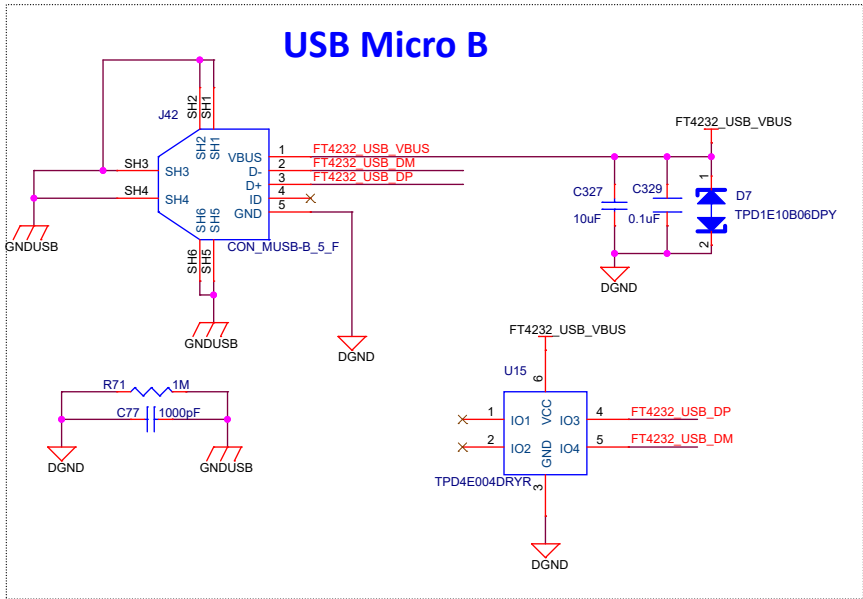
Size Variant Name = PROC062 001 OPN#TMDX654IDKEVM

Date: Tuesday, September 04, 2018

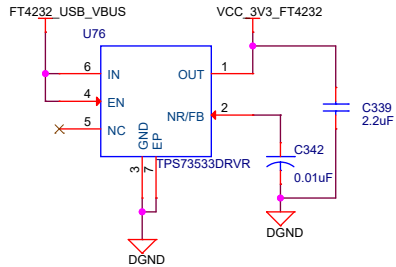
Sheet 30 of 44

Rev E3

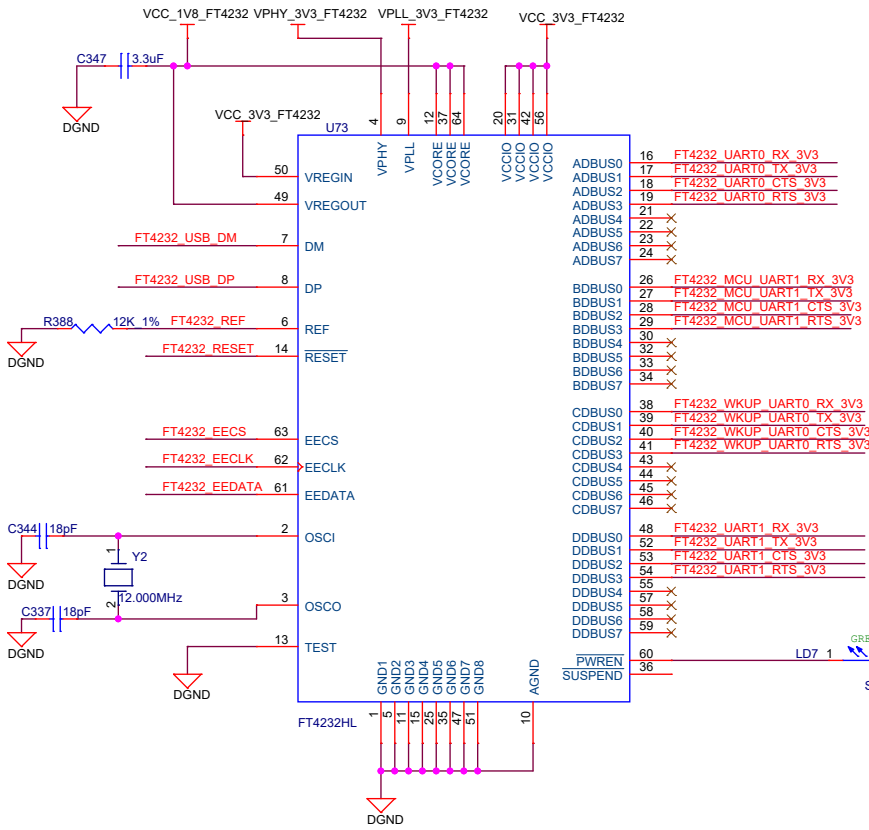
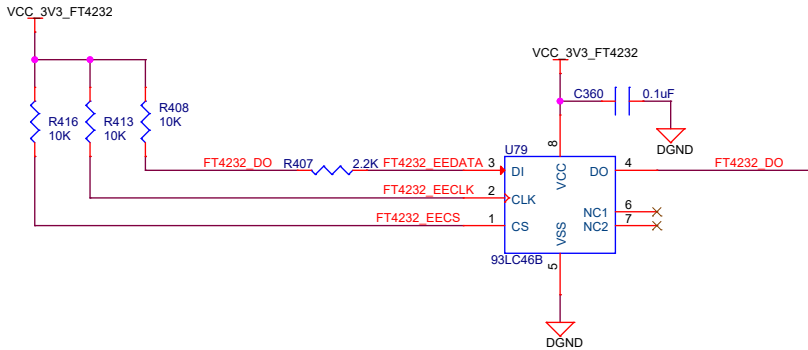
FT4232 UART



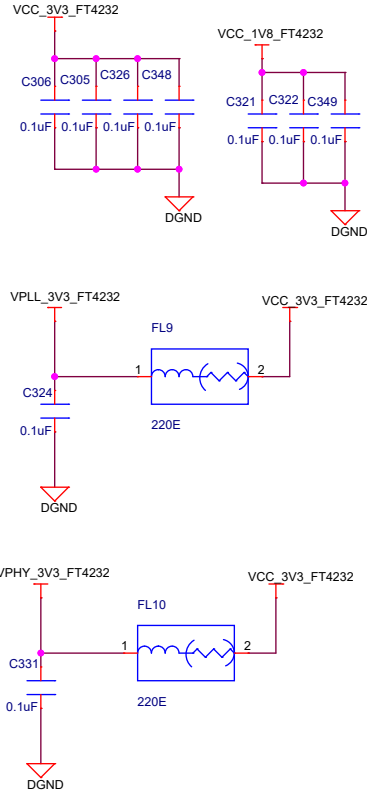
FT4232: 5V to 3.3V@500mA LDO



EEPROM



FT4232_UART0_TX_3V3	<<FT4232_UART0_TX_3V3	(30)
FT4232_UART0_RTS_3V3	<<FT4232_UART0_RTS_3V3	(30)
FT4232_UART0_RX_3V3	<<FT4232_UART0_RX_3V3	(30)
FT4232_UART0_CTS_3V3	<<FT4232_UART0_CTS_3V3	(30)
FT4232_UART1_TX_3V3	<<FT4232_UART1_TX_3V3	(30)
FT4232_UART1_RTS_3V3	<<FT4232_UART1_RTS_3V3	(30)
FT4232_UART1_RX_3V3	<<FT4232_UART1_RX_3V3	(30)
FT4232_UART1_CTS_3V3	<<FT4232_UART1_CTS_3V3	(30)
FT4232_WKUP_UART0_TX_3V3	<<FT4232_WKUP_UART0_TX_3V3	(30)
FT4232_WKUP_UART0_RTS_3V3	<<FT4232_WKUP_UART0_RTS_3V3	(30)
FT4232_WKUP_UART0_RX_3V3	<<FT4232_WKUP_UART0_RX_3V3	(30)
FT4232_WKUP_UART0_CTS_3V3	<<FT4232_WKUP_UART0_CTS_3V3	(30)
FT4232_MCU_UART1_TX_3V3	<<FT4232_MCU_UART1_TX_3V3	(30)
FT4232_MCU_UART1_RTS_3V3	<<FT4232_MCU_UART1_RTS_3V3	(30)
FT4232_MCU_UART1_RX_3V3	<<FT4232_MCU_UART1_RX_3V3	(30)
FT4232_MCU_UART1_CTS_3V3	<<FT4232_MCU_UART1_CTS_3V3	(30)



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Title FT4232 UART TO USB BRIDGE

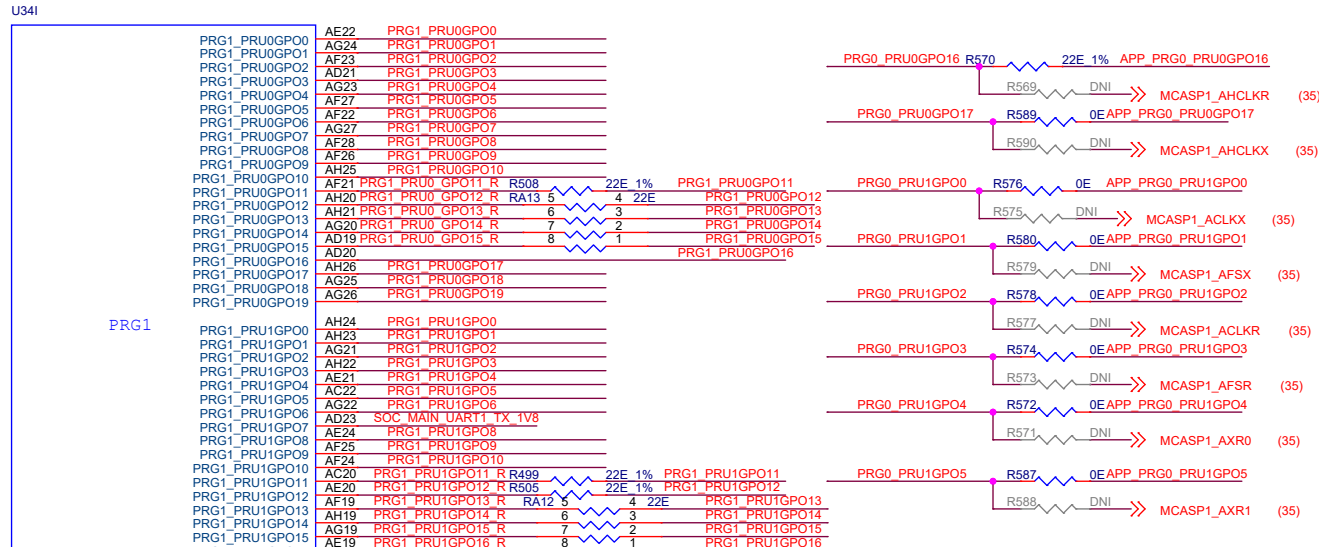
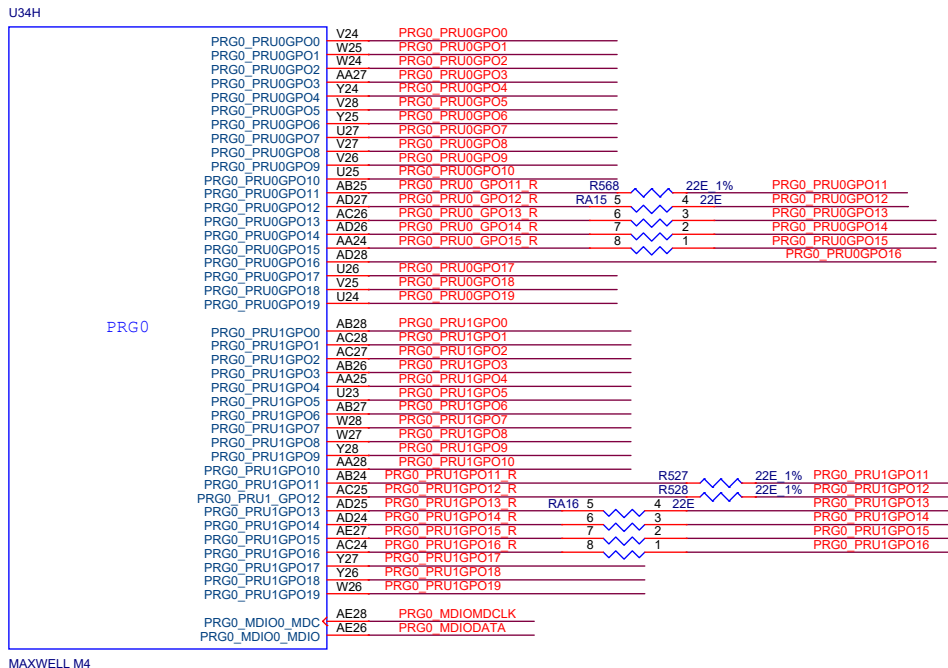
Size Variant Name = PROC062 001 OPN#TMDX654IDKEVM

Date: Friday, August 31, 2018

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Rev E3

APPLICATION BOARD INTERFACE

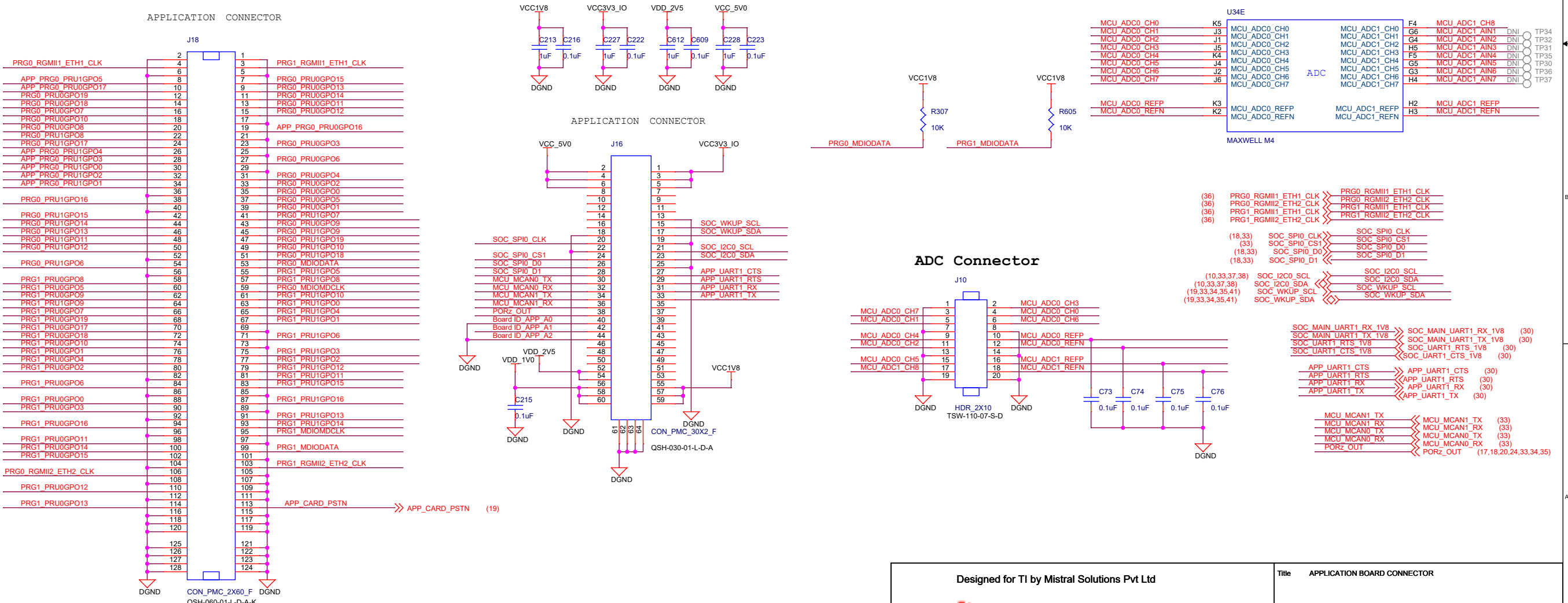


0- Ohm Res MUX between APPLICATION Board connector and HDMI / GPMC Daughter card.

-For APPLICATION Board connector R570 ,R589 ,R576 ,R580 ,R578, R574 ,R572 & R587 Should be installed and R569, R590, R575, R579 ,R577 , R573, R571 & R588 Should be DNI'd.

-For HDMI / GPMC Daughter card R569, R590, R575, R579 ,R577 , R573, R571 & R588 Should be Installed and R570 , R589 ,R576 ,R580 ,R578, R574 ,R572 & R587 Should be DNI'd.

APPLICATION BOARD CONNECTORS



Designed for TI by Mistral Solutions Pvt Ltd

Title APPLICATION BOARD CONNECTOR

Size	
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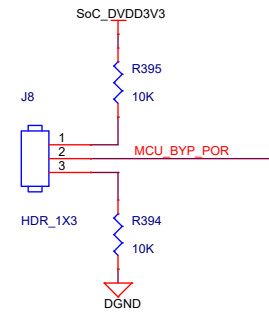
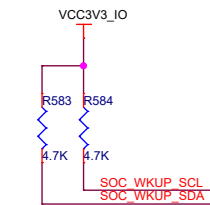
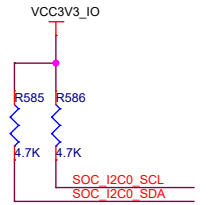
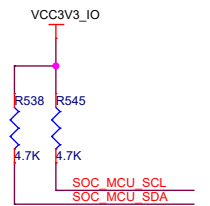
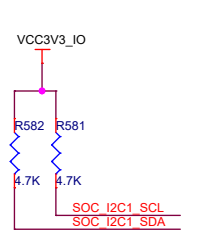
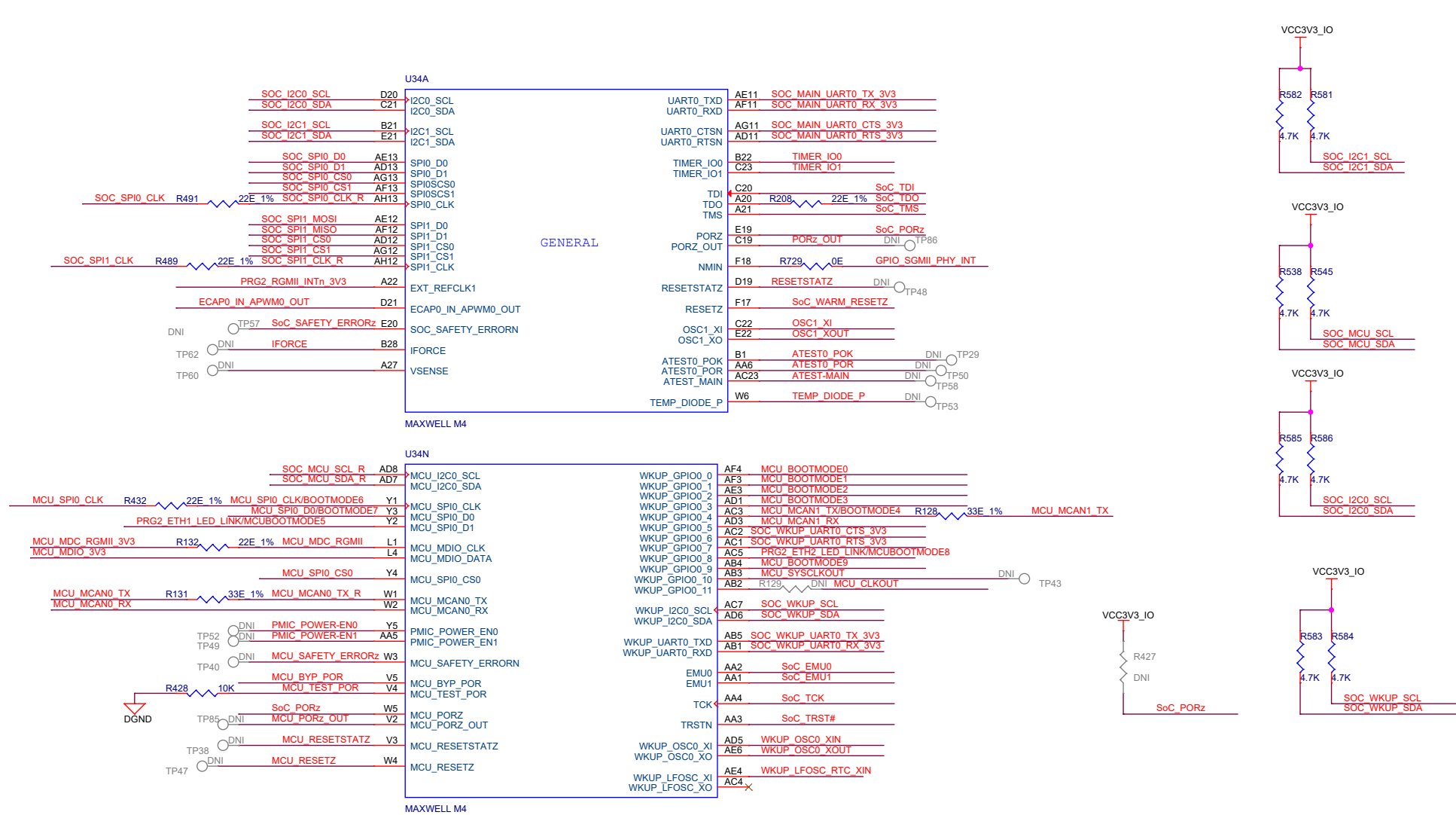
C	Variant Name = PROC062 001 OPN#TMDX654IDKEVM
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Date: Tuesday, September 04, 2018	Sheet 32 of 44
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Rev

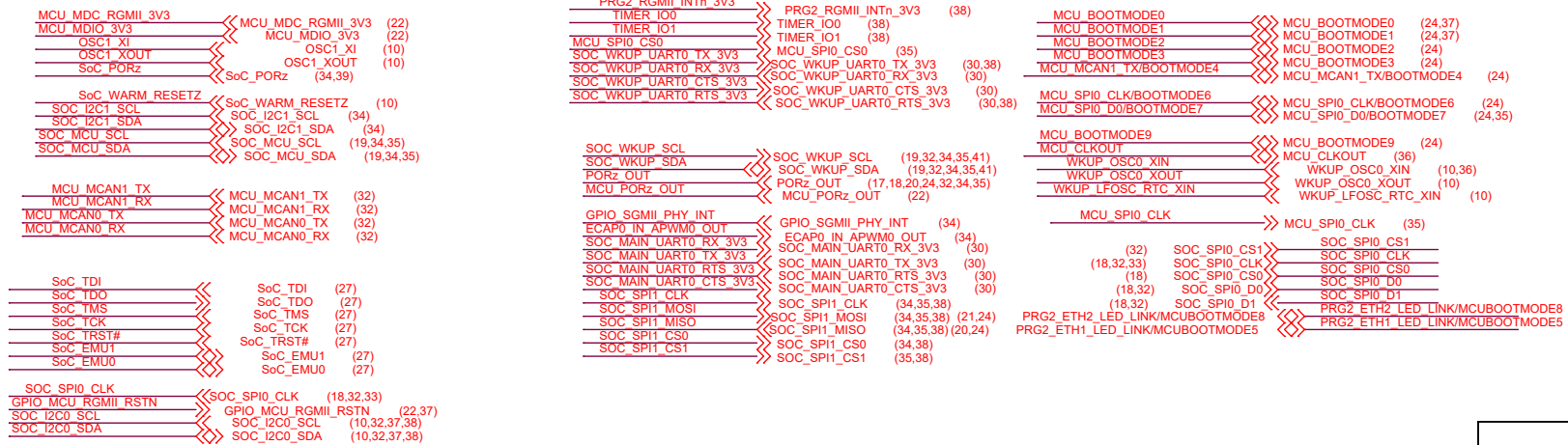
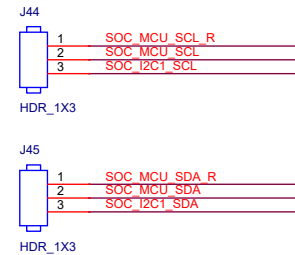
E3

GENERAL & MCU_GENERAL



To Disable the Internal PORz ,
Connect the Jumper between Pin no 1 & 2 of J8.
To Enable the Internal PORz,
Connect the Jumper between Pin no 2 & 3 of J8

Jumper option to connect the peripherals connected on MCU_I2C to SoC I2C1



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Title	SOC_GENERAL & MCU GENERAL
-------	---------------------------

Size

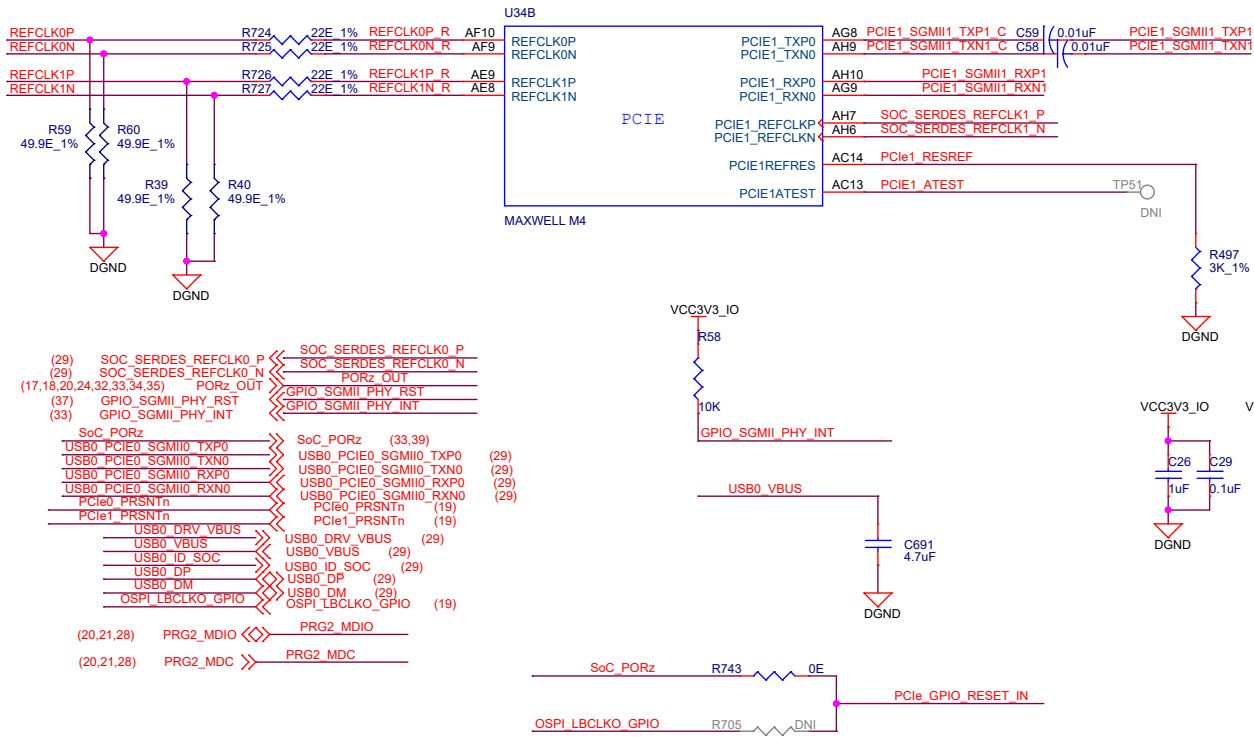
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Date: Tuesday, September 04, 2018

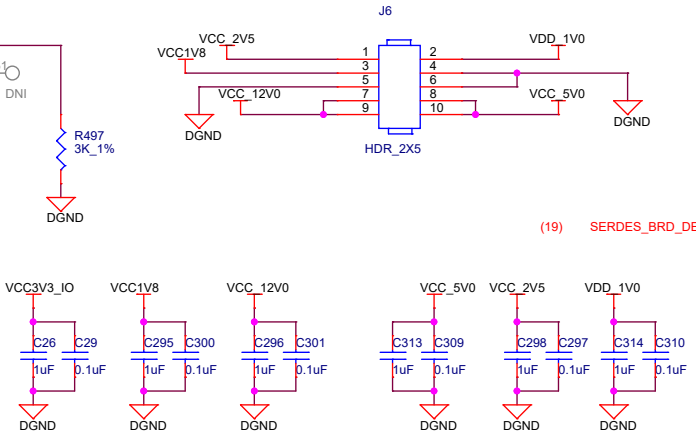
Rev

E3

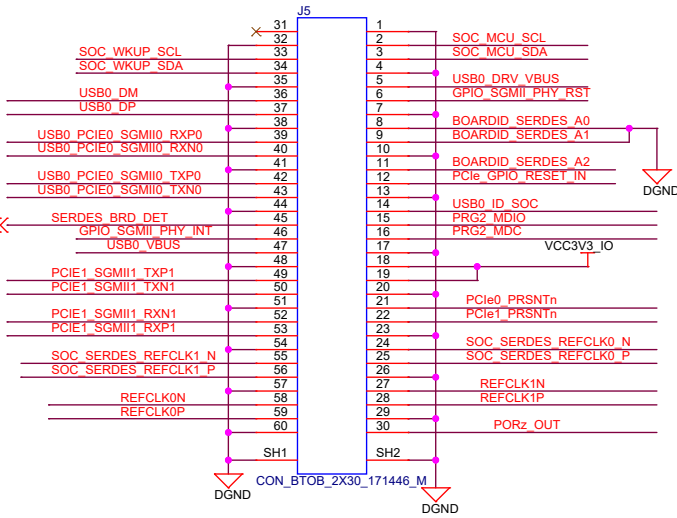
SERDES INTERFACE



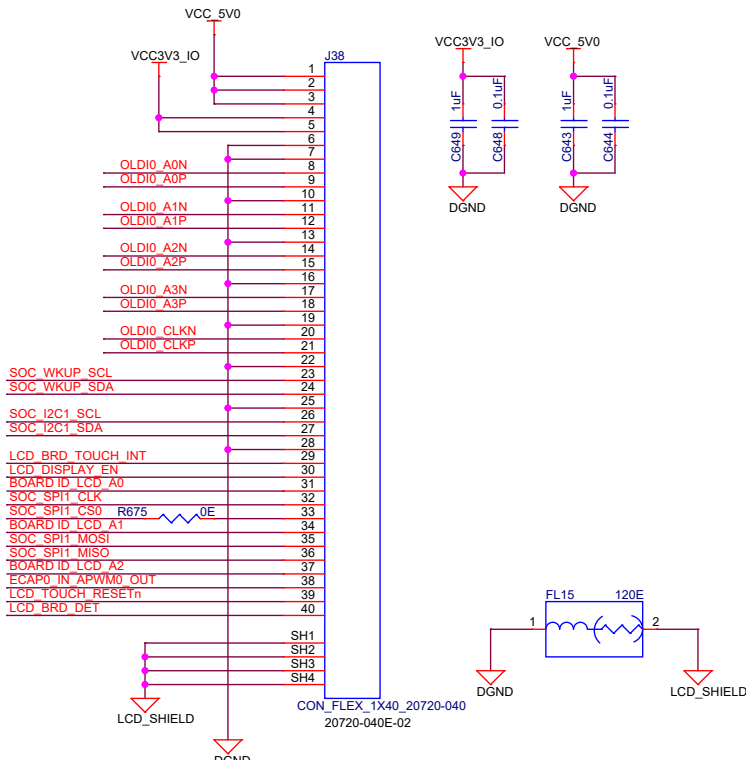
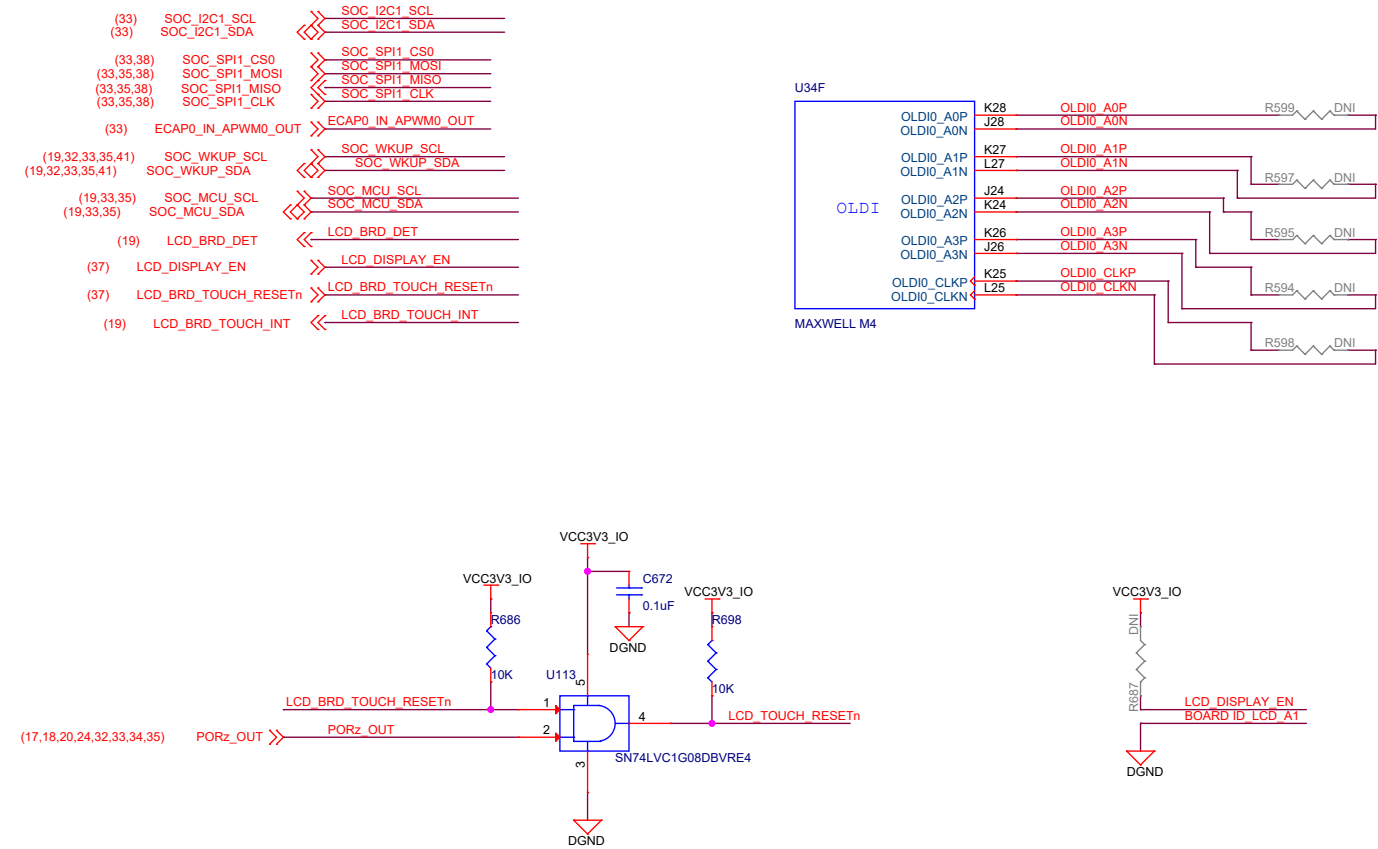
SERDES POWER CONNECTOR



SERDES CONNECTOR



OLDI INTERFACE



Designed for TI by Mistral Solutions Pvt Ltd



Title SERDES & DISPLAY INTERFACE

Size
C Variant Name = PROC062 001 OPN#TMDX654IDKEVM

Rev
E3

Date: Tuesday, September 04, 2018

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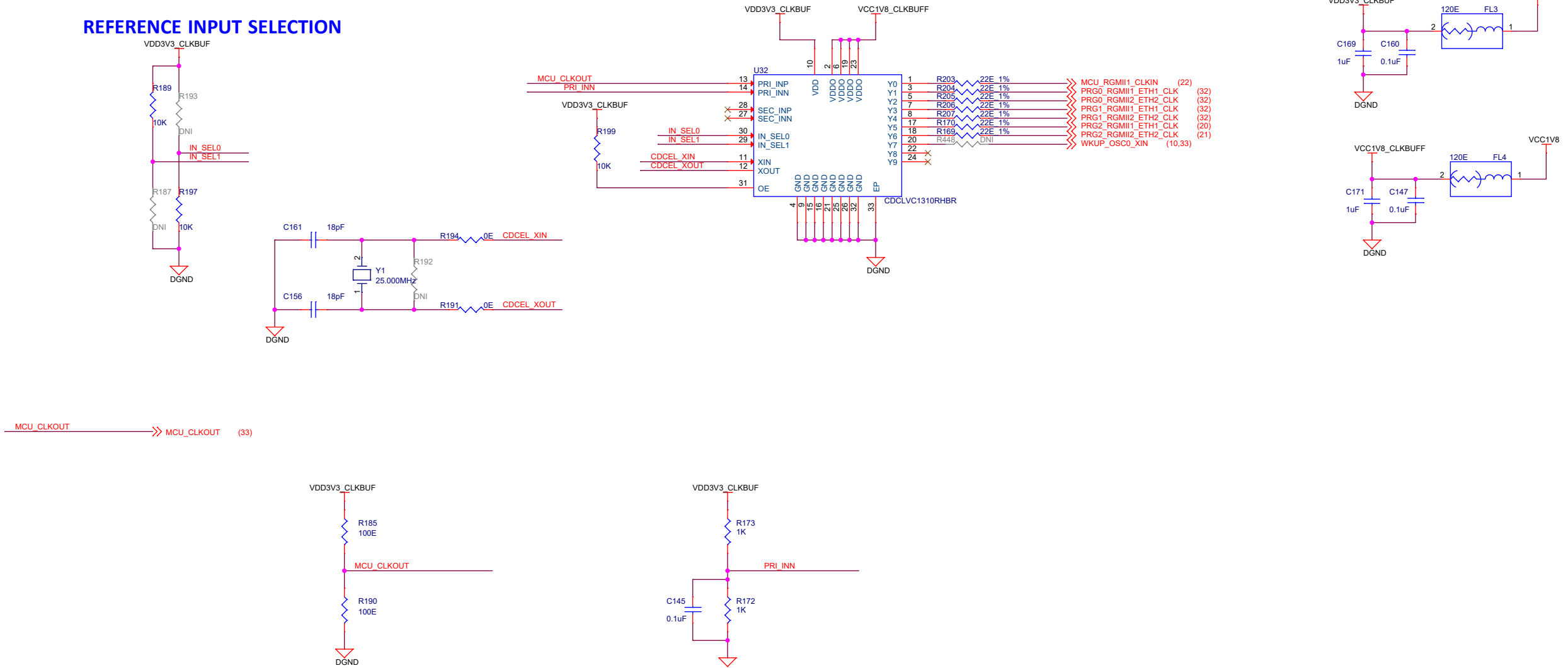
VCC HDR



Title		CSI, GPMC/DSS INTERFACE	
Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM		Rev
C			E3
Date:	Tuesday, September 04, 2018	Sheet	35 of 44

ETHERNET PHY CLOCK BUFFER

REFERENCE INPUT SELECTION



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Title ETHERNET PHY CLOCK GENERATOR

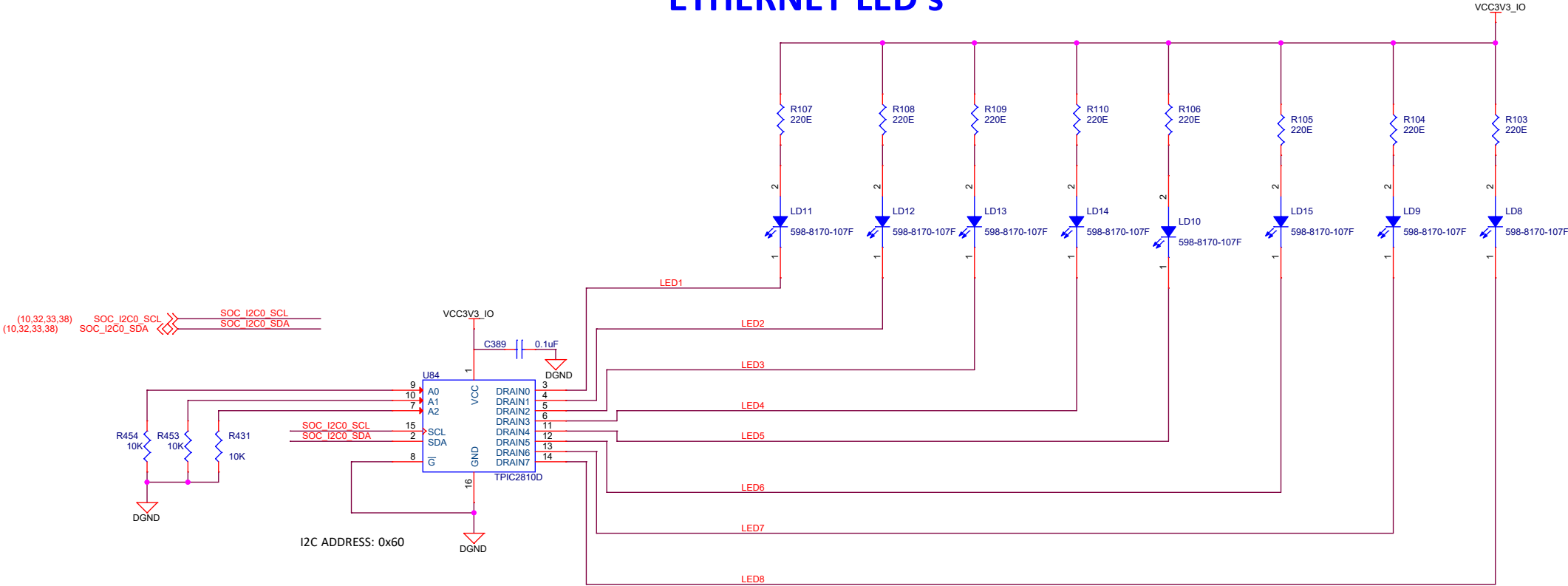
Size Variant Name = PROC062 001 OPN#TMDX654IDKEVM

Rev

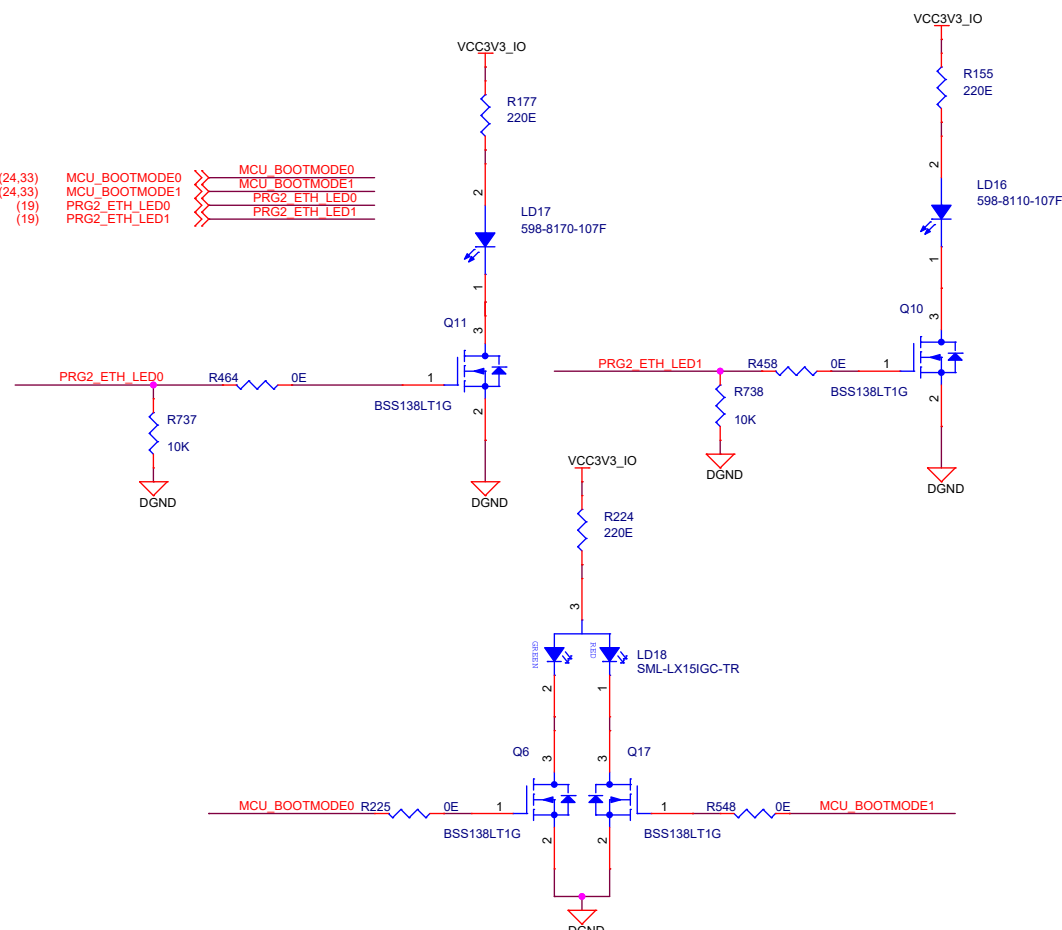
Date: Friday, August 31, 2018

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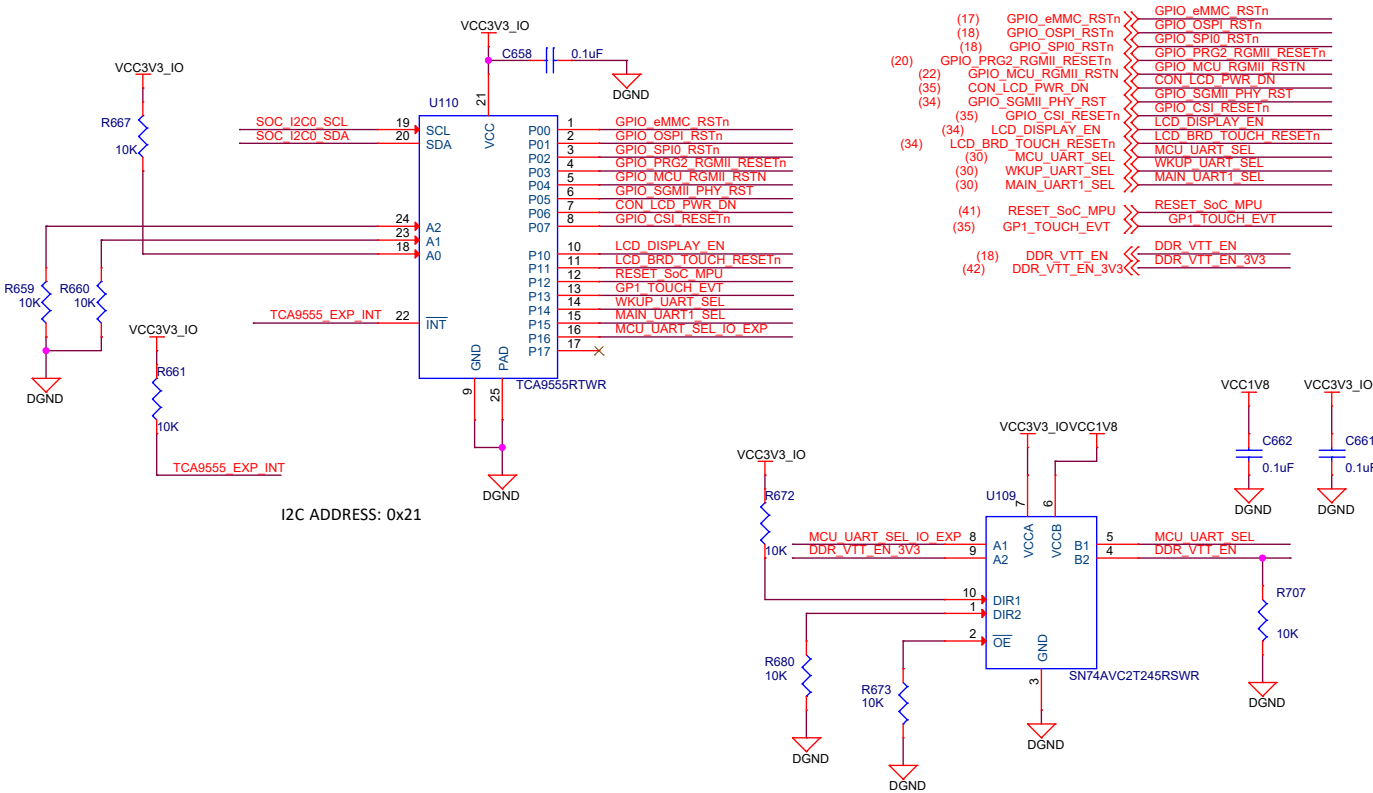
ETHERNET LED's



PRG2 ETHERNET LED's

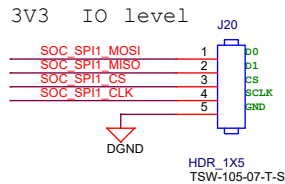
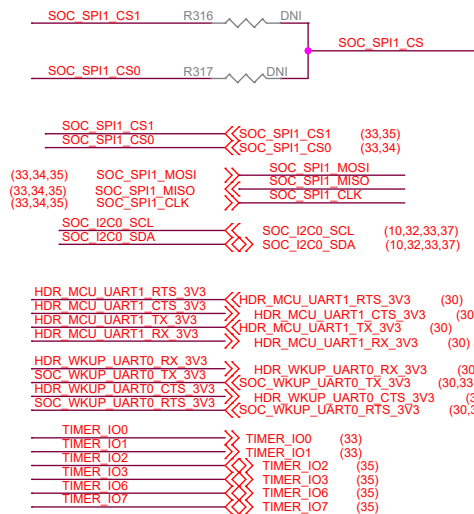


I2C IO Expander

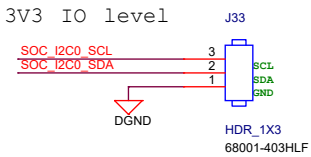


TEST HEADER

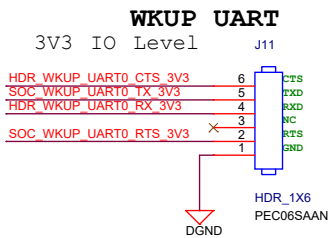
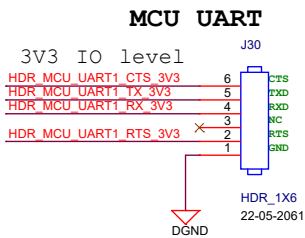
SPI TEST HEADER



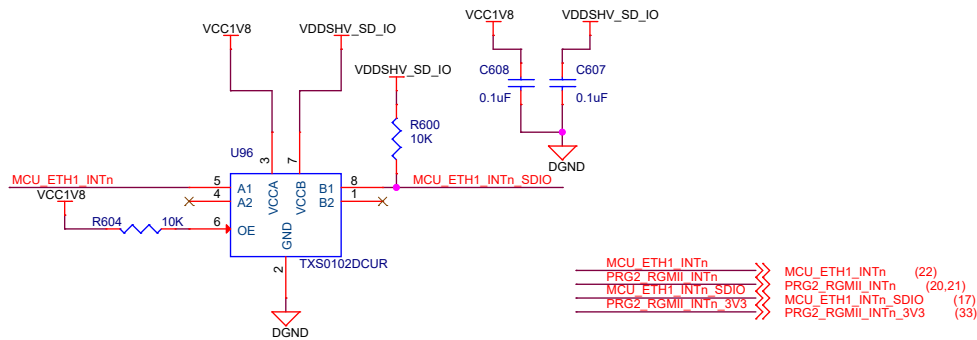
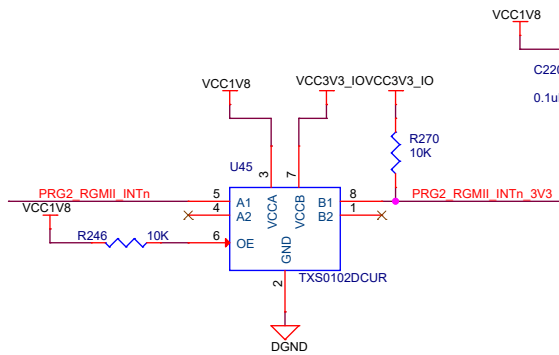
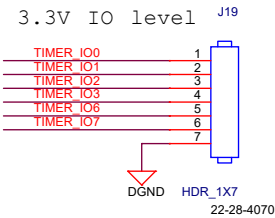
I2C TEST HEADER



UART TEST HEADER



TIMER SIGNALS TEST HEADER



Designed for TI by Mistral Solutions Pvt Ltd



Title TEST HEADER

Size Variant Name = PROC062 001 OPN#TMDX654IDKEVM

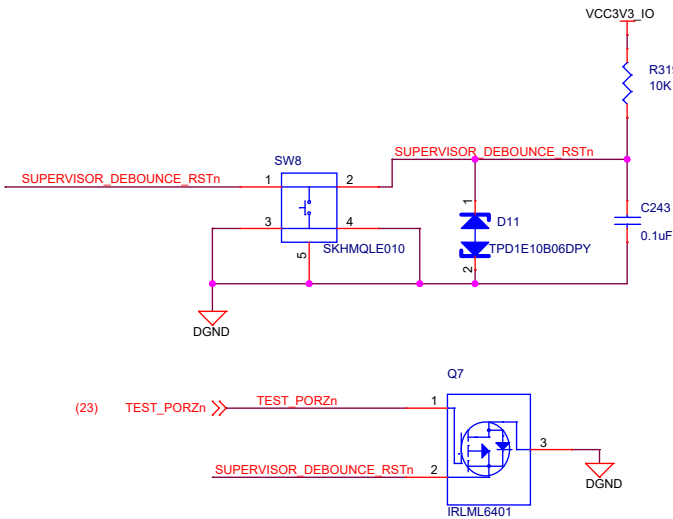
Rev E3

Date: Tuesday, July 24, 2018

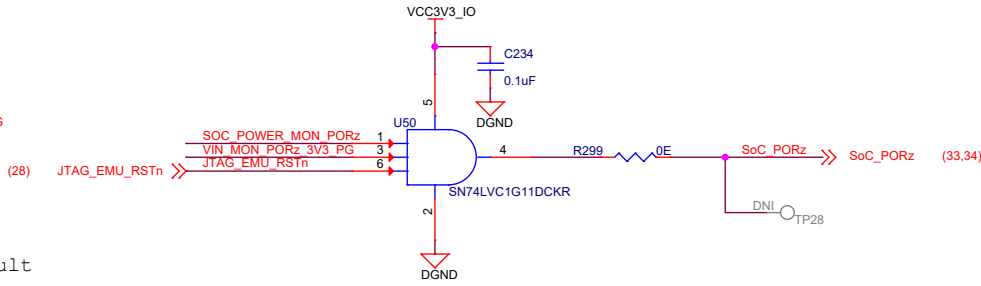
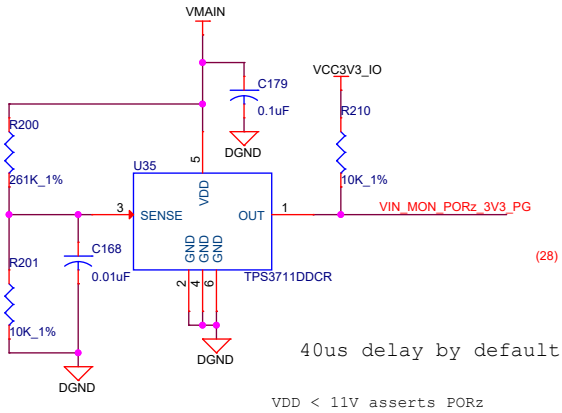
Sheet 38 of 44

VOLTAGE SUPERVISOR

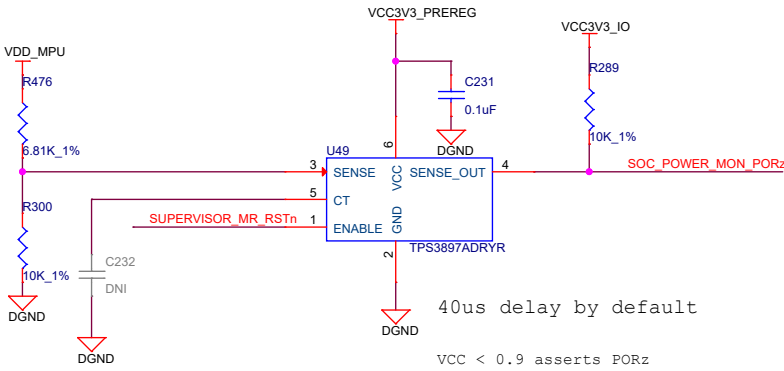
Under Voltage Monitor (VMAIN)



(23) SUPERVISOR_DEBOUNCE_RSTn
(23) SUPERVISOR_MR_RSTn
(41,42) VIN_MON_PORz_3V3_PG



Under Voltage Monitor (VDD_MPU)



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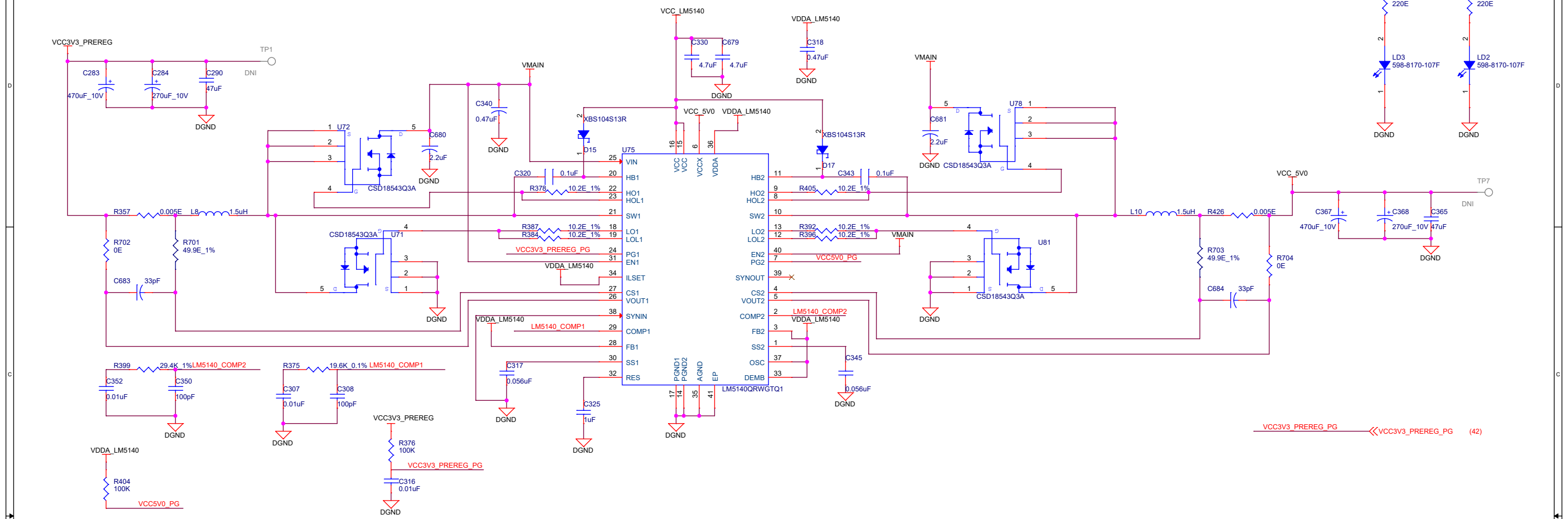


Title VOLTAGE SUPERVISOR & WKUP LEDs

Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Friday, August 31, 2018	Sheet 39 of 44

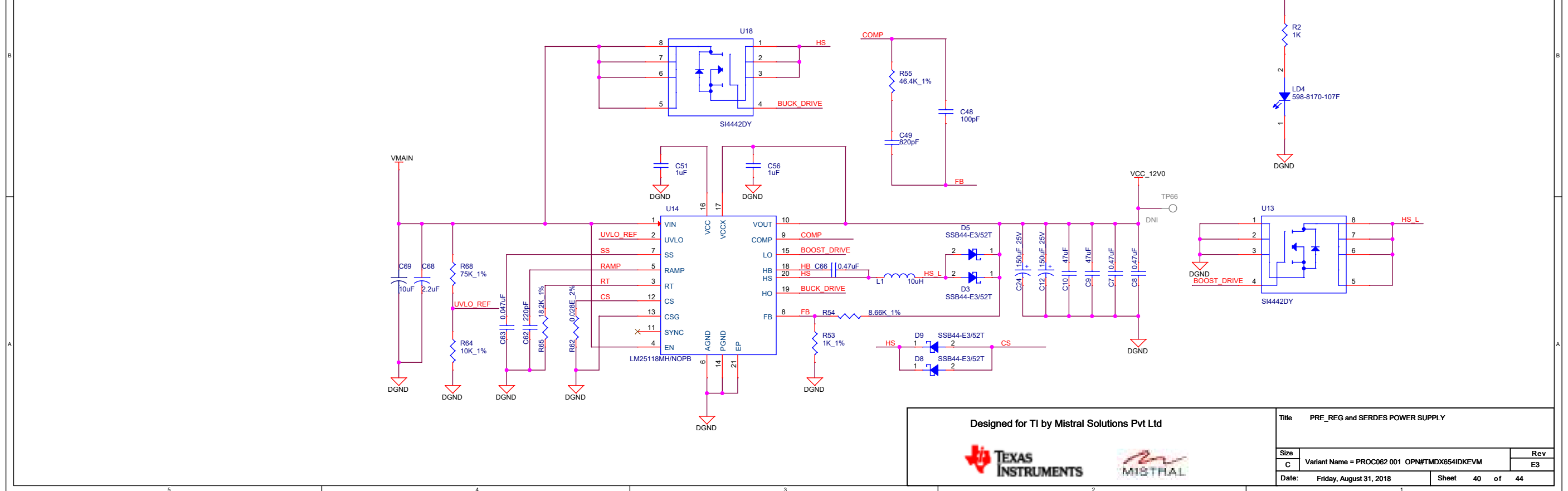
PRE_REG POWER SUPPLY

5V,10A and 3.3V,10A Dual SUPPLY



SERDES POWER SUPPLY

12V, 3A SUPPLY



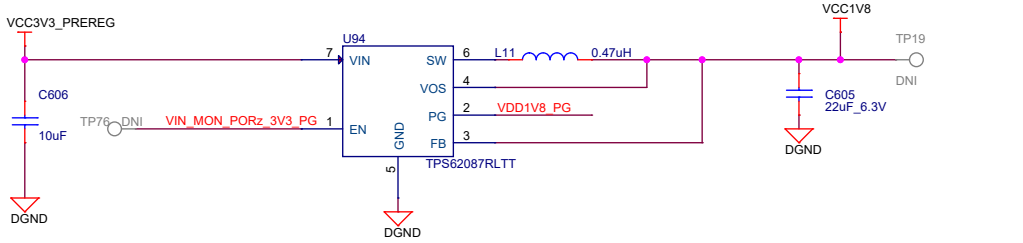
Designed for TI by Mistral Solutions Pvt Ltd



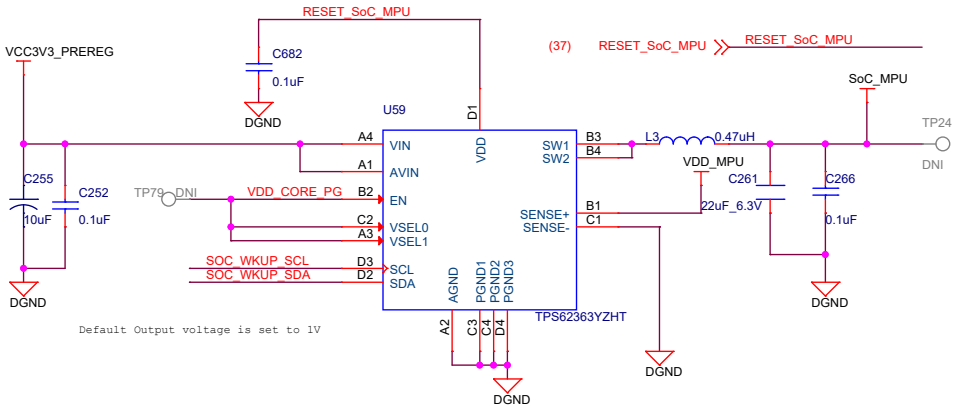
Title		
PRE_REG and SERDES POWER SUPPLY		
Size	Rev	
C	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	E3
Date:	Friday, August 31, 2018	Sheet 40 of 44

SoC POWER SUPPLY

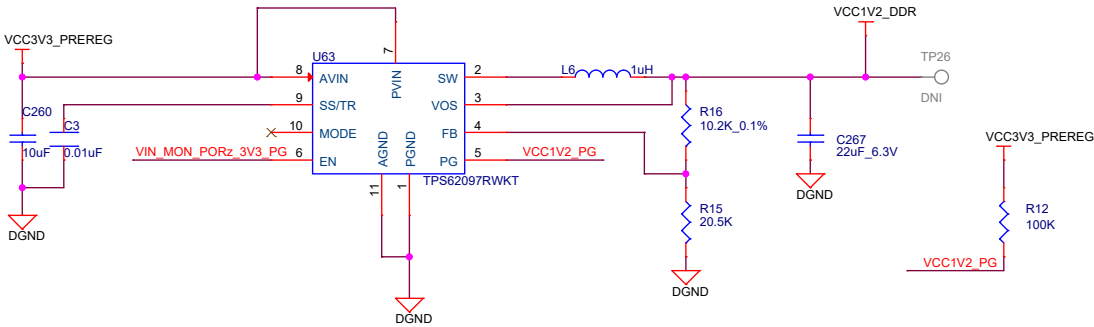
1.8V IO, 3.0AMPS SUPPLY



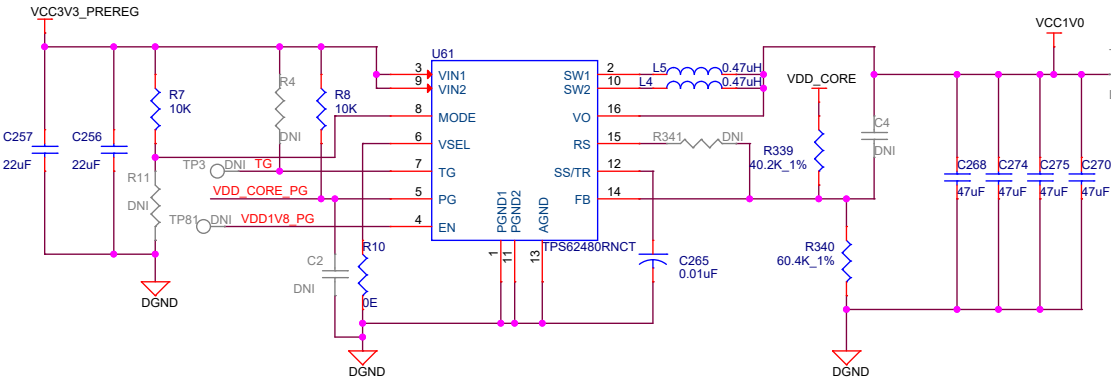
0.9-1.35V, 3.0AMPS SUPPLY



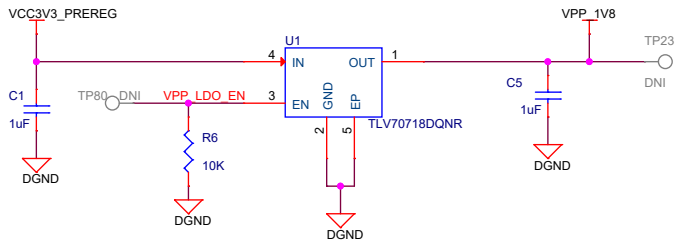
1.2V, 2.0AMPS SUPPLY



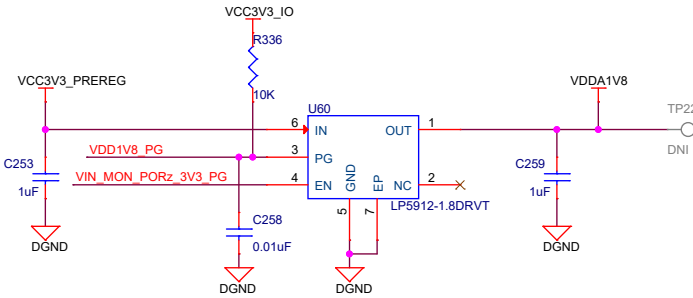
VDD_CORE 1.0V, 6.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY



1.8V Analog , 0.4AMPS SUPPLY



(19,32,33,34,35) SOC_WKUP_SCL >>> SOC_WKUP_SCL
(19,32,33,34,35) SOC_WKUP_SDA >>> SOC_WKUP_SDA
(18) VPP_LDO_EN <<< VPP_LDO_EN
(39,42) VIN_MON_PORz_3V3_PG <<< VIN_MON_PORz_3V3_PG

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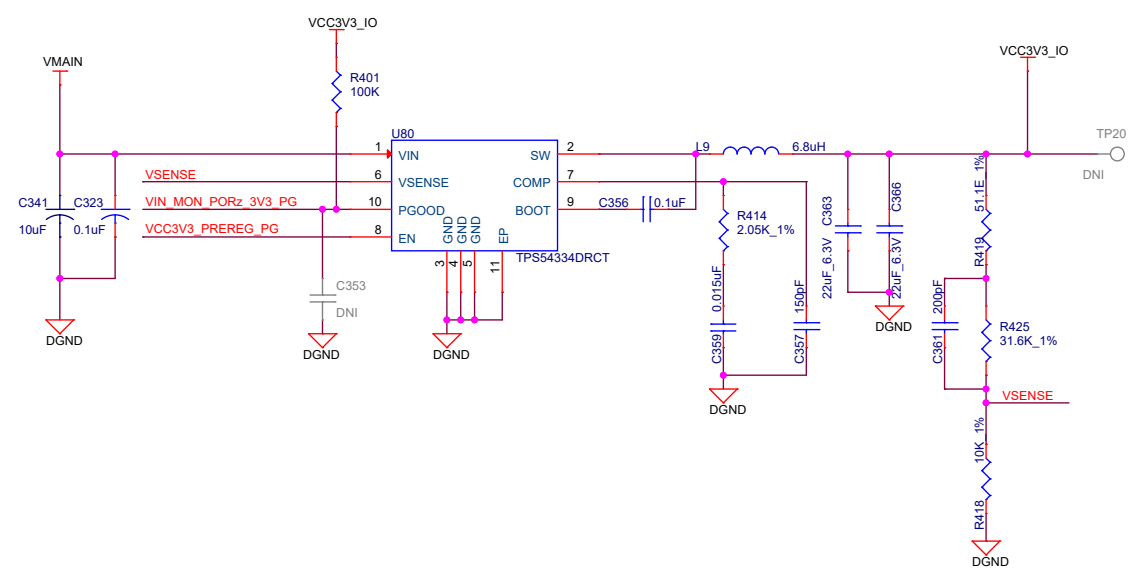


Title SoC POWER SUPPLY

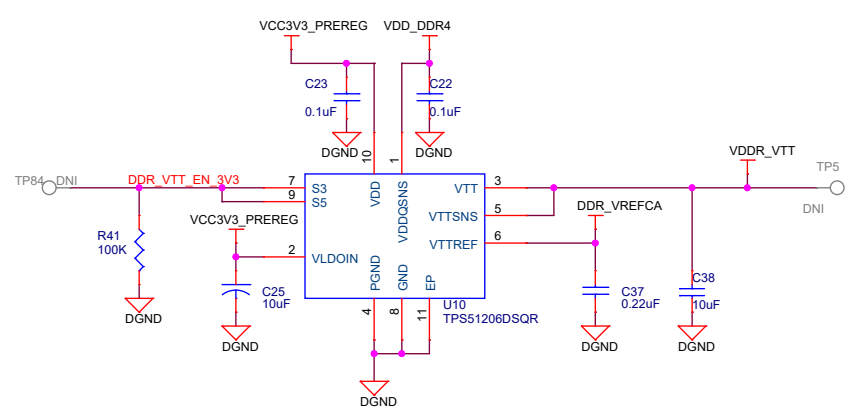
Size	Rev
C	E3
Variant Name = PROC062 001 OPN#TMDX654IDKEVM	
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PERIPHERAL POWER SUPPLY

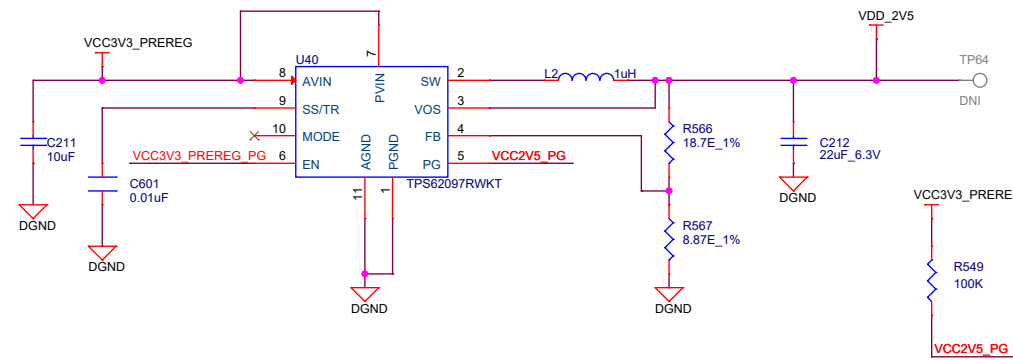
3.3V, 3.0AMPS SUPPLY



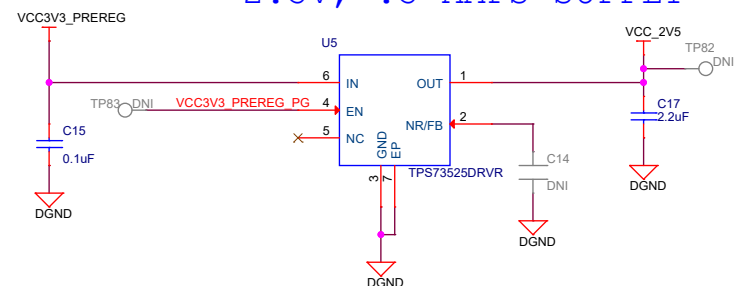
VTT SUPPLY FOR DDR4



2.5V, 2.0AMPS SUPPLY

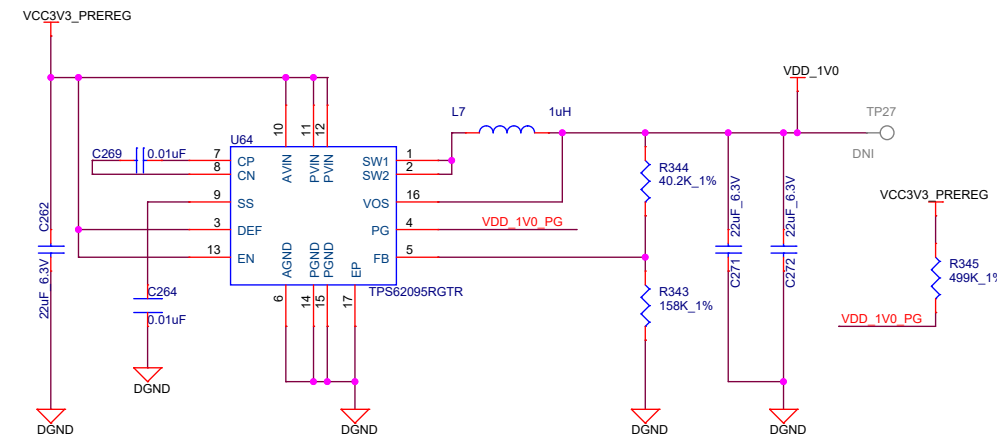


2.5V, .5 AMPS SUPPLY



(40) VCC3V3_PREREG_PG >> VCC3V3_PREREG_PG
(39,41) VIN_MON_PORz_3V3_PG << VIN_MON_PORz_3V3_PG
(37) DDR_VTT_EN_3V3 << DDR_VTT_EN_3V3

1.0V ETHERNET PHY POWER SUPPLY

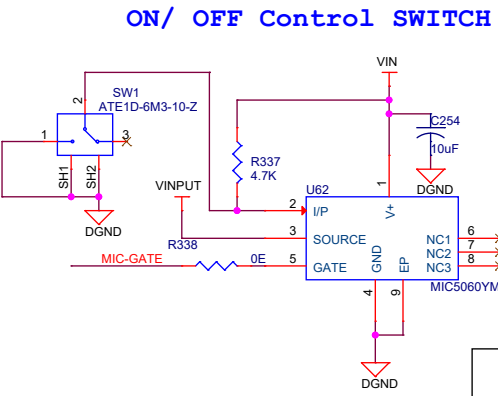
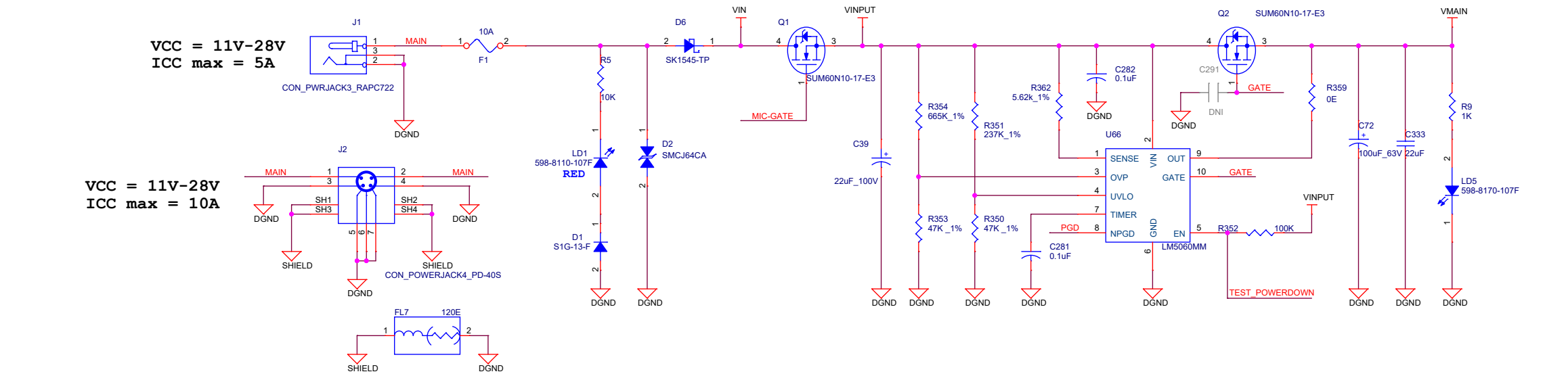


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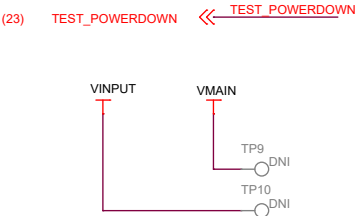
Title PERIPHERAL POWER SUPPLY		
Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date: Tuesday, September 04, 2018	Sheet 42 of 44	

OVER VOLTAGE PROTECTION CIRCUIT

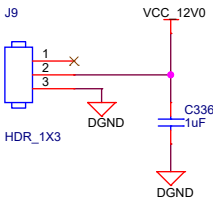


Note:-
UVLO set for 11V
OVP set for 28V

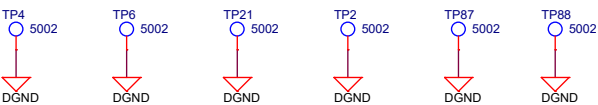
Condition	LED Status (LD1)
Reverse Voltage	ON



Cooling FAN Header



Ground test points



Fault Indication

Condition	LED Status (LD6)
VINPUT between 11 to 28V	OFF
VINPUT above 28V or below 11V	ON

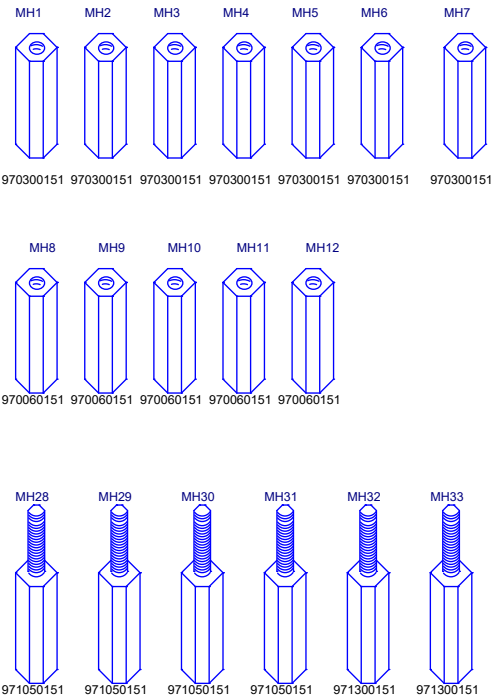
Note:-
When fault is indicated ,set to proper voltage and power cycle the board.

HARDWARE SCHEMATICS

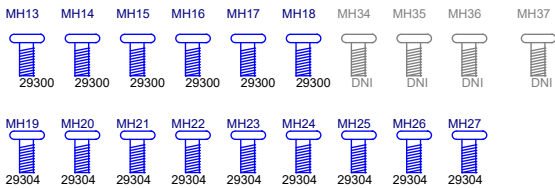
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

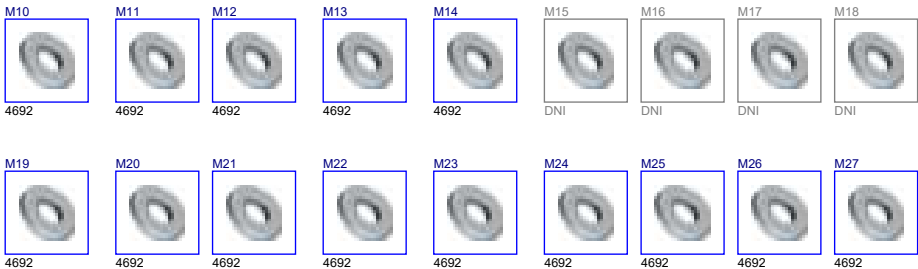
STANDOFFs



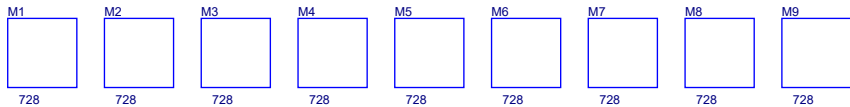
SCREWS



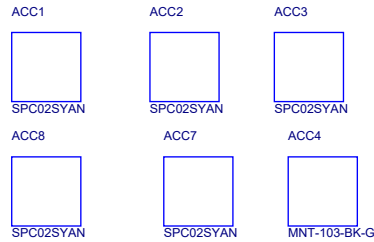
WASHER's



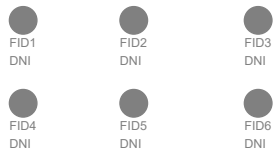
RUBBER FEET



JUMPERS



FIDUCIALS



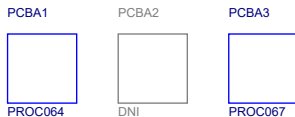
Socket & Processor as Accessories



BARE PCB



Assembled PCB's



Board Serial No.

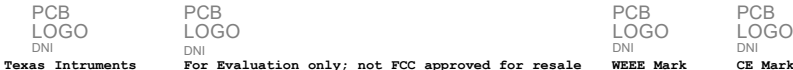
LABELS

ORDERABLE PART NO



Orderable part number	
Variant	Label Text
001	TMDX654IDKEVM
002	TMDX654HSEVM
003	TMDX654GPEVM
004	TMDX654IDKEVM-S
005	TMDX654GPEVM-S

LOGOs



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Title HARDWARE SCHEMATICS

Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
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