ADC344x Quad-Channel, 14-Bit, 25-MSPS to 125-MSPS, Analog-to-Digital Converters

1 Features

- Quad Channel
- 14-Bit Resolution
- Single Supply: 1.8 V
- Serial LVDS Interface
- Flexible Input Clock Buffer With Divide-by-1, -2, -4
- SNR = 72.4 dBFS, SFDR = 87 dBc at f_{IN} = 70 MHz
- Ultra-Low Power Consumption:
  - 98 mW/Ch at 125 MSPS
- Channel Isolation: 105 dB
- Internal Dither and Chopper
- Support for Multi-Chip Synchronization
- Pin-to-Pin Compatible With 12-Bit Version
- Package: VQFN-56 (8 mm × 8 mm)

2 Applications

- Multi-Carrier, Multi-Mode Cellular Base Stations
- Radar and Smart Antenna Arrays
- Munitions Guidance
- Motor Control Feedback
- Network and Vector Analyzers
- Communications Test Equipment
- Nondestructive Testing
- Microwave Receivers
- Software-Defined Radios (SDRs)
- Quadrature and Diversity Radio Receivers

3 Description

The ADC344x devices are a high-linearity, ultra-low power, quad-channel, 14-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization.

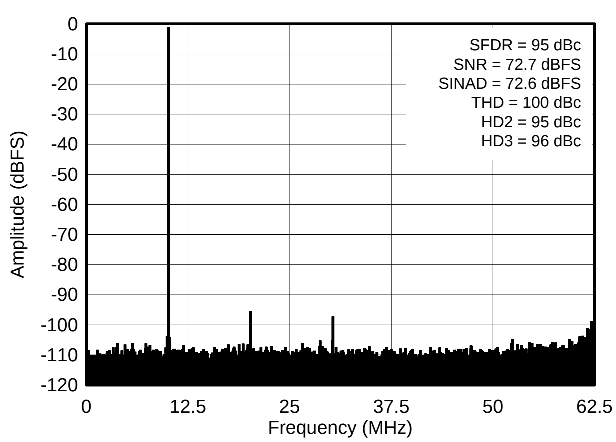
The ADC344x family supports serial low-voltage differential signaling (LVDS) to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. Optionally, a one-wire serial LVDS interface is available. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 14-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are transmitted as LVDS outputs.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC344x	VQFN (56)	8.00 mm × 8.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Spectrum at 10 MHz



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2015) to Revision B — **Page**

- Added description for availability of one-wire serial LVDS interface in *Description* section 1
- Changed *Spectrum at 10 MHz* figure to show conditions within curve 1
- Changed description of AVDD, DVDD, and GND pins and added *active high* to description of PDN pin in *Pin Functions* table 5
- Deleted *maximum* from parameter description in *Recommended Operating Conditions* table 6
- Changed Digital Outputs, R_{LOAD} parameter description in *Recommended Operating Conditions* table 6
- Changed conditions of all *Electrical Characteristics* and *AC Performance* tables 7
- Added minimum and maximum specifications to Analog Input, $V_{OC(VCM)}$ parameter in *Electrical Characteristics: General* table 7
- Changed description of Analog Input, *Analog input bandwidth* parameter in *Electrical Characteristics: General* table 7
- Deleted footnote 1 from *Electrical Characteristics: General* table 7
- Added DC Accuracy, E_G parameter with its test conditions and footnote 3 to *Electrical Characteristics: General* table 7
- Deleted $E_{G(REF)}$ and $E_{G(CHAN)}$ from DC Accuracy in *Electrical Characteristics: General* table 7
- Changed DC Accuracy, $\alpha_{(EGCHAN)}$ to α_{EG} and updated its parameter in *Electrical Characteristics: General* table 7
- Changed Channel-to-Channel Isolation, *Crosstalk* parameter in *Electrical Characteristics: General* table: changed test conditions, added footnote 2 7
- Changed test conditions for IMD3 parameter in *AC Performance: ADC3441* table 10
- Added INL and DNL rows to all *AC Performance* tables 10
- Changed *Digital Inputs (SYSREFP, SYSREFM)* subsection in *Digital Characteristics* table, added footnote 2 17

Revision History (continued)

- Changed specifications of Digital Outputs (LVDS Interface), V_{OCM} parameter in *Digital Characteristics* table.................... 17
- Changed *rising* to *falling* in description of *SYSREF reference time* parameter in *Timing Requirements: General* table ... 17
- Changed *Typical Characteristics* sections: added *dither on* to all section condition statements, changed *Non 23* to *excluding HD2, HD3* 19
- Added INL and DNL plots in Typical Characteristics: ADC3441 section 24
- Changed conditions of Figure 34, Figure 35 25
- Added INL and DNL plots in Typical Characteristics: ADC3442 section 30
- Changed conditions of Figure 67, Figure 68 31
- Added INL and DNL plots in Typical Characteristics: ADC3443 section 36
- Changed conditions of Figure 100, Figure 101 37
- Added INL and DNL plots in Typical Characteristics: ADC3444 section. 42
- Changed conditions of Figure 134 43
- Added Figure 141 to *Timing Diagrams* section 44
- Added *Using the SYSREF Input* section 50
- Changed the description about synchronization of the phase of the divided clock in each device to the common sampling clock in Using the SYSREF Input section. 50
- Added *ADC3441 Power-Up Requirements* section, deleted the *Register Initialization* section 57
- Added last sentence to *Detailed Design Procedure* section of first typical application 75
- Added *Chopper On* to caption of Figure 198 75
- Added *Chopper Off* to caption of Figure 200 76
- Changed the caption of Figure 202 from *FFT for 450-MHz Input Signal (Dither On)* to *FFT for 450-MHz Input Signal (Chopper Off, Dither On)* 77

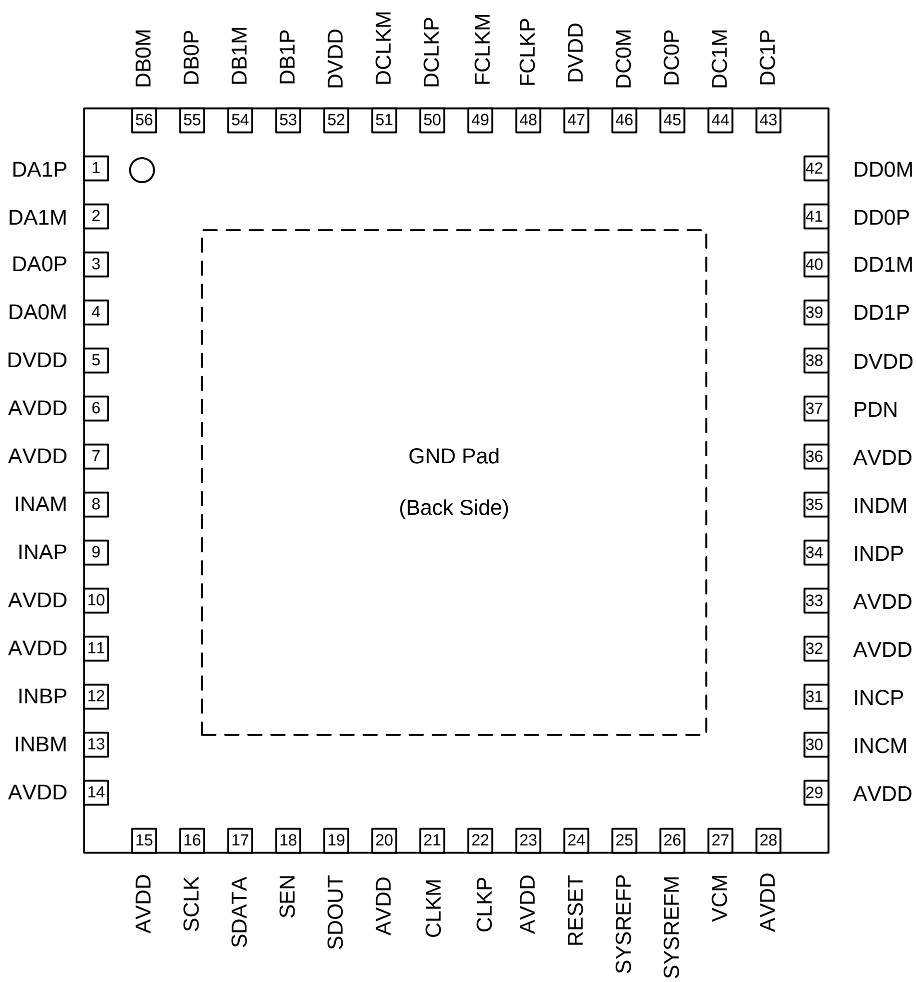
Changes from Original (July 2014) to Revision A	**Page**
• Released to production..	1

5 Device Comparison Table

INTERFACE	RESOLUTION (Bits)	25 MSPS	50 MSPS	80 MSPS	125 MSPS	160 MSPS
Serial LVDS	12	ADC3421	ADC3422	ADC3423	ADC3424	—
	14	ADC3441	ADC3442	ADC3443	ADC3444	—
JESD204B	12	—	ADC34J22	ADC34J23	ADC34J24	ADC34J25
	14	—	ADC34J42	ADC34J43	ADC34J44	ADC34J45

6 Pin Configuration and Functions

RTQ Package
56-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	6, 7, 10, 11, 14, 15, 20, 23, 28, 29, 32, 33, 36	I	Analog 1.8-V power supply, decoupled with capacitors
CLKM	21	I	Negative differential clock input for the ADC
CLKP	22	I	Positive differential clock input for the ADC
DA0M	4	O	Negative serial LVDS output for wire-0 of channel A
DA0P	3	O	Positive serial LVDS output for wire-0 of channel A
DA1M	2	O	Negative serial LVDS output for wire-1 of channel A
DA1P	1	O	Positive serial LVDS output for wire-1 of channel A
DB0M	56	O	Negative serial LVDS output for wire-0 of channel B
DB0P	55	O	Positive serial LVDS output for wire-0 of channel B
DB1M	54	O	Negative serial LVDS output for wire-1 of channel B
DB1P	53	O	Positive serial LVDS output for wire-1 of channel B1
DC0M	46	O	Negative serial LVDS output for wire-0 of channel C
DC0P	45	O	Positive serial LVDS output for wire-0 of channel C
DC1M	44	O	Negative serial LVDS output for wire-1 of channel C
DC1P	43	O	Positive serial LVDS output for wire-1 of channel C
DD0M	42	O	Negative serial LVDS output for wire-0 of channel D
DD0P	41	O	Positive serial LVDS output for wire-0 of channel D
DD1M	40	O	Negative serial LVDS output for wire-1 of channel D
DD1P	39	O	Positive serial LVDS output for wire-1 of channel D
DCLKM	51	O	Negative bit clock output
DCLKP	50	O	Positive bit clock output
DVDD	5, 38, 47, 52	I	Digital 1.8-V power supply, decoupled with capacitors
FCLKM	49	O	Negative frame clock output
FCLKP	48	O	Positive frame clock output
GND	PowerPAD™	I	Ground, 0 V. Connect to the printed circuit board (PCB) ground plane.
INAM	8	I	Negative differential analog input for channel A
INAP	9	I	Positive differential analog input for channel A
INBM	13	I	Negative differential analog input for channel B
INBP	12	I	Positive differential analog input for channel B
INCM	30	I	Negative differential analog input for channel C
INCP	31	I	Positive differential analog input for channel C
INDM	35	I	Negative differential analog input for channel D
INDP	34	I	Positive differential analog input for channel D
PDN	37	I	Power-down control; active high. This pin may be configured through the SPI. This pin has an internal 150-kΩ pulldown resistor.
RESET	24	I	Hardware reset; active high. This pin has an internal 150-kΩ pulldown resistor.
SCLK	16	I	Serial interface clock input. This pin has an internal 150-kΩ pulldown resistor.
SDATA	17	I	Serial interface data input. This pin has an internal 150-kΩ pulldown resistor.
SDOUT	19	O	Serial interface data output
SEN	18	I	Serial interface enable; active low. This pin has an internal 150-kΩ pullup resistor to AVDD.
SYSREFM	26	I	Negative external SYSREF input
SYSREFP	25	I	Positive external SYSREF input
VCM	27	O	Common-mode voltage for analog inputs

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Analog supply voltage range, AVDD		–0.3	2.1	V
Digital supply voltage range, DVDD		–0.3	2.1	V
Voltage applied to input pins	INAP, INBP, INAM, INBM	–0.3	min (1.9, AVDD + 0.3)	V
	CLKP, CLKM	–0.3	AVDD + 0.3	
	SYSREFP, SYSREFM	–0.3	AVDD + 0.3	
	SCLK, SEN, SDATA, RESET, PDN	–0.3	3.9	
Temperature	Operating free-air, T_A	–40	85	ºC
	Operating junction, T_J		125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage range		1.7	1.8	1.9	V
DVDD	Digital supply voltage range		1.7	1.8	1.9	V
ANALOG INPUT						
V_{ID}	Differential input voltage	For input frequencies < 450 MHz		2		V_{PP}
		For input frequencies < 600 MHz		1		
V_{IC}	Input common-mode voltage			VCM ± 0.025		V
CLOCK INPUT						
	Input clock frequency	Sampling clock frequency	15[2]		125[3]	MSPS
	Input clock amplitude (differential)	Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LPECL, ac-coupled		1.6		
		LVDS, ac-coupled		0.7		
	Input clock duty cycle		35%	50%	65%	
	Input clock common-mode voltage			0.95		V
DIGITAL OUTPUTS						
C_{LOAD}	External load capacitance from each output pin to GND			3.3		pF
R_{LOAD}	Differential load resistance to be placed across the positive and negative pins of the LVDS output pair			100		Ω

(1) After power-up, only use the RESET pin to reset the device for the first time; see the *Register Initialization* section for details.
(2) See Table 3 for details.
(3) With the clock divider enabled by default for divide-by-1. Maximum sampling clock frequency for the divide-by-4 option is 500 MSPS.

7.4 Thermal Information

THERMAL METRIC(1)		ADC344x RTQ (VQFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: General

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Differential input full-scale				2.0		V_{PP}
r_i	Input resistance	Differential at dc			6.6		kΩ
c_i	Input capacitance	Differential at dc			3.7		pF
$V_{OC(VCM)}$	VCM common-mode voltage output			0.8	0.95	1.1	V
	VCM output current capability				10		mA
	Input common-mode current	Per analog input pin			1.5		µA/MSPS
	Analog input bandwidth (–3-dB point)	50-Ω differential source driving 50-Ω termination across INP and INM			540		MHz
DC ACCURACY							
E_O	Offset error			–25		25	mV
α_{EO}	Temperature coefficient of offset error				±0.024		mV/°C
E_G	Overall dc gain error of a channel	ADC3441		–2		2	%FS
		ADC3442, ADC3443, ADC3444		-2.5		2.5	
α_{EG}	Temperature coefficient of overall gain error				0.005		Δ%FS/°C
CHANNEL-TO-CHANNEL ISOLATION							
	Crosstalk(1)(2)	f_{IN} = 10 MHz	Between near channels		105		dB
			Between far channels		105		
		f_{IN} = 100 MHz	Between near channels		95		
			Between far channels		105		
		f_{IN} = 200 MHz	Between near channels		94		
			Between far channels		105		
		f_{IN} = 230 MHz	Between near channels		92		
			Between far channels		105		
		f_{IN} = 300 MHz	Between near channels		85		
			Between far channels		105		

(1) Crosstalk is measured with a –1-dBFS input signal on the aggressor channel and no input on the victim channel.
(2) Channels A and B are near to each other but far from channels C and D. Similarly, channels C and D are near to each other but far from channels A and B; see the *Pin Configuration and Functions* section for more information.

7.6 Electrical Characteristics: ADC3441, ADC3442

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER	ADC3441			ADC3442			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			25			50	MSPS
Resolution	14			14			Bits
1.8-V analog supply current		54	74		71	97	mA
1.8-V digital supply current		45	67		56	83	mA
Total power dissipation		177	215		228	277	mW
Global power-down dissipation		5	17		5	17	mW
Standby power-down dissipation		34	103		35	103	mW

7.7 Electrical Characteristics: ADC3443, ADC3444

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER	ADC3443			ADC3444			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			80			125	MSPS
Resolution	14			14			Bits
1.8-V analog supply current		92	125		119	162	mA
1.8-V digital supply current		68	101		98	145	mA
Total power dissipation		288	350		391	475	mW
Global power-down dissipation		5	17		5	17	mW
Standby power-down dissipation		40	103		43	103	mW

7.8 AC Performance: ADC3441

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER		TEST CONDITIONS	ADC3441 (f_S = 25 MSPS) DITHER ON MIN	DITHER ON TYP	DITHER ON MAX	DITHER OFF MIN	DITHER OFF TYP	DITHER OFF MAX	UNIT
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		73.1			73.5		dBFS
		f_{IN} = 20 MHz	70.9	72.9			73.4		
		f_{IN} = 70 MHz		72.5			73		
		f_{IN} = 100 MHz		72.4			72.7		
		f_{IN} = 170 MHz		71.4			71.7		
		f_{IN} = 230 MHz		70.3			70.5		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.4			72.9		
		f_{IN} = 20 MHz		72.2			72.7		
		f_{IN} = 70 MHz		71.9			72.4		
		f_{IN} = 100 MHz		71.7			72.0		
		f_{IN} = 170 MHz		70.9			71.1		
		f_{IN} = 230 MHz		69.7			69.9		
NSD (1)	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–143.7			–144.1		dBFS/Hz
		f_{IN} = 20 MHz		–143.5	–141.5		–143.9		
		f_{IN} = 70 MHz		–143.1			–143.6		
		f_{IN} = 100 MHz		–143.0			–143.3		
		f_{IN} = 170 MHz		–142.0			–142.3		
		f_{IN} = 230 MHz		–140.9			–141.1		
SINAD (1)	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.1			73.4		dBFS
		f_{IN} = 20 MHz	69.9	72.9			73.2		
		f_{IN} = 70 MHz		71.7			71.9		
		f_{IN} = 100 MHz		72.6			72.8		
		f_{IN} = 170 MHz		71.2			71.4		
		f_{IN} = 230 MHz		69.9			70.1		
ENOB (1)	Effective number of bits	f_{IN} = 10 MHz		11.9			11.9		Bits
		f_{IN} = 20 MHz	11.3	11.8			11.8		
		f_{IN} = 70 MHz		11.7			11.8		
		f_{IN} = 100 MHz		11.8			11.8		
		f_{IN} = 170 MHz		11.5			11.6		
		f_{IN} = 230 MHz		11.3			11.4		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		91			89		dBc
		f_{IN} = 20 MHz	82	91			85		
		f_{IN} = 70 MHz		92			87		
		f_{IN} = 100 MHz		85			82		
		f_{IN} = 170 MHz		86			85		
		f_{IN} = 230 MHz		81			81		

(1) Reported from a 1-MHz offset.

AC Performance: ADC3441 (continued)

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER		TEST CONDITIONS	ADC3441 (f_S = 25 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		92			93		dBc
		f_{IN} = 20 MHz	82	92			91		
		f_{IN} = 70 MHz		92			91		
		f_{IN} = 100 MHz		96			94		
		f_{IN} = 170 MHz		86			85		
		f_{IN} = 230 MHz		84			84		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		96			90		dBc
		f_{IN} = 20 MHz	82	93			89		
		f_{IN} = 70 MHz		93			88		
		f_{IN} = 100 MHz		85			82		
		f_{IN} = 170 MHz		89			89		
		f_{IN} = 230 MHz		82			82		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		100			93		dBc
		f_{IN} = 20 MHz	87	97			92		
		f_{IN} = 70 MHz		97			92		
		f_{IN} = 100 MHz		97			94		
		f_{IN} = 170 MHz		92			90		
		f_{IN} = 230 MHz		98			92		
THD	Total harmonic distortion	f_{IN} = 10 MHz		90			86		dBc
		f_{IN} = 20 MHz	79	90			85		
		f_{IN} = 70 MHz		90			85		
		f_{IN} = 100 MHz		84			80		
		f_{IN} = 170 MHz		84			83		
		f_{IN} = 230 MHz		80			80		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz, each tone at –7 dBFS		–97			–97		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, each tone at –7 dBFS		–88			–88		
INL	Integral nonlinearity	f_{IN} = 20 MHz		±0.75	±3		±0.75		LSBs
DNL	Differential nonlinearity	f_{IN} = 20 MHz	–0.95	±0.6			±0.6		LSBs

7.9 AC Performance: ADC3442

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER		TEST CONDITIONS	ADC3442 (f_S = 50 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		73.1			73.5		dBFS
		f_{IN} = 20 MHz	70.7	72.9			73.3		
		f_{IN} = 70 MHz		72.7			73.1		
		f_{IN} = 100 MHz		71.9			72.6		
		f_{IN} = 170 MHz		71.5			71.8		
		f_{IN} = 230 MHz		70.4			70.8		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.5			72.9		
		f_{IN} = 20 MHz		72.3			72.7		
		f_{IN} = 70 MHz		71.9			72.3		
		f_{IN} = 100 MHz		71.3			72.1		
		f_{IN} = 170 MHz		71.0			71.2		
		f_{IN} = 230 MHz		69.8			70.2		
NSD(1)	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–146.9			–147.3		dBFS/Hz
		f_{IN} = 20 MHz		–146.7	–144.5		–146.9		
		f_{IN} = 70 MHz		–146.5			–146.9		
		f_{IN} = 100 MHz		–145.7			–146.4		
		f_{IN} = 170 MHz		–145.3			–145.6		
		f_{IN} = 230 MHz		–144.2			–144.6		
SINAD(1)	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73			73.4		dBFS
		f_{IN} = 20 MHz	69.7	72.2			72.7		
		f_{IN} = 70 MHz		72.2			72.7		
		f_{IN} = 100 MHz		72.1			73.2		
		f_{IN} = 170 MHz		71.4			71.8		
		f_{IN} = 230 MHz		69.8			70.1		
ENOB(1)	Effective number of bits	f_{IN} = 10 MHz		11.9			11.9		Bits
		f_{IN} = 20 MHz	11.3	11.8			11.8		
		f_{IN} = 70 MHz		11.8			11.8		
		f_{IN} = 100 MHz		11.7			11.9		
		f_{IN} = 170 MHz		11.6			11.6		
		f_{IN} = 230 MHz		11.4			11.4		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		90			90		dBc
		f_{IN} = 20 MHz	82	92			90		
		f_{IN} = 70 MHz		92			90		
		f_{IN} = 100 MHz		87			87		
		f_{IN} = 170 MHz		86			84		
		f_{IN} = 230 MHz		83			82		

(1) Reported from a 1-MHz offset.

AC Performance: ADC3442 (continued)

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER		TEST CONDITIONS	ADC3442 (f_S = 50 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		95			92		dBc
		f_{IN} = 20 MHz	83	99			94		
		f_{IN} = 70 MHz		93			91		
		f_{IN} = 100 MHz		92			92		
		f_{IN} = 170 MHz		87			85		
		f_{IN} = 230 MHz		85			83		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		90			92		dBc
		f_{IN} = 20 MHz	82	94			91		
		f_{IN} = 70 MHz		94			91		
		f_{IN} = 100 MHz		87			87		
		f_{IN} = 170 MHz		88			89		
		f_{IN} = 230 MHz		83			88		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		99			95		dBc
		f_{IN} = 20 MHz	87	99			93		
		f_{IN} = 70 MHz		99			93		
		f_{IN} = 100 MHz		92			94		
		f_{IN} = 170 MHz		97			89		
		f_{IN} = 230 MHz		97			91		
THD	Total harmonic distortion	f_{IN} = 10 MHz		89			87		dBc
		f_{IN} = 20 MHz	79	90			87		
		f_{IN} = 70 MHz		90			87		
		f_{IN} = 100 MHz		86			85		
		f_{IN} = 170 MHz		85			83		
		f_{IN} = 230 MHz		81			81		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		–92			–92		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		–87			–87		
INL	Integral nonlinearity	f_{IN} = 20 MHz		±0.8	±3		±0.8		LSBs
DNL	Differential nonlinearity	f_{IN} = 20 MHz	–0.95	±0.6			±0.6		LSBs

7.10 AC Performance: ADC3443

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER		TEST CONDITIONS	ADC3443 (f_S = 80 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		72.9			73.2		dBFS
		f_{IN} = 70 MHz	70.7	72.8			73.1		
		f_{IN} = 100 MHz		72.5			72.9		
		f_{IN} = 170 MHz		72.1			72.4		
		f_{IN} = 230 MHz		71.4			71.7		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.5			72.8		
		f_{IN} = 70 MHz		72.4			72.8		
		f_{IN} = 100 MHz		72.1			72.6		
		f_{IN} = 170 MHz		71.7			72.0		
		f_{IN} = 230 MHz		71.1			71.4		
NSD[1]	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–148.8			–149.1		dBFS/Hz
		f_{IN} = 70 MHz		–148.7	–146.6		–149.0		
		f_{IN} = 100 MHz		–148.4			–148.8		
		f_{IN} = 170 MHz		–148.0			–148.3		
		f_{IN} = 230 MHz		–147.3			–147.6		
SINAD[1]	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.8			73.2		dBFS
		f_{IN} = 70 MHz	69.7	72.2			72.4		
		f_{IN} = 100 MHz		72.7			73		
		f_{IN} = 170 MHz		71.9			72.2		
		f_{IN} = 230 MHz		71.2			71.4		
ENOB[1]	Effective number of bits	f_{IN} = 10 MHz		11.8			11.9		Bits
		f_{IN} = 70 MHz	11.3	11.8			11.8		
		f_{IN} = 100 MHz		11.8			11.8		
		f_{IN} = 170 MHz		11.7			11.7		
		f_{IN} = 230 MHz		11.5			11.6		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		89			89		dBc
		f_{IN} = 70 MHz	81	90			89		
		f_{IN} = 100 MHz		92			92		
		f_{IN} = 170 MHz		88			86		
		f_{IN} = 230 MHz		86			84		

(1) Reported from a 1-MHz offset.

AC Performance: ADC3443 (continued)

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER		TEST CONDITIONS	ADC3443 (f_S = 80 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		94			91		dBc
		f_{IN} = 70 MHz	81	96			91		
		f_{IN} = 100 MHz		97			94		
		f_{IN} = 170 MHz		88			86		
		f_{IN} = 230 MHz		87			85		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		89			90		dBc
		f_{IN} = 70 MHz	81	91			90		
		f_{IN} = 100 MHz		94			100		
		f_{IN} = 170 MHz		95			93		
		f_{IN} = 230 MHz		87			87		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		100			95		dBc
		f_{IN} = 70 MHz	86	98			94		
		f_{IN} = 100 MHz		95			94		
		f_{IN} = 170 MHz		95			94		
		f_{IN} = 230 MHz		94			92		
THD	Total harmonic distortion	f_{IN} = 10 MHz		88			86		dBc
		f_{IN} = 70 MHz	78	89			87		
		f_{IN} = 100 MHz		91			90		
		f_{IN} = 170 MHz		87			84		
		f_{IN} = 230 MHz		84			82		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		–98			–98		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		–88			–88		
INL	Integral nonlinearity	f_{IN} = 70 MHz		±0.8	±3		±0.8		LSBs
DNL	Differential nonlinearity	f_{IN} = 70 MHz	–0.95	±0.7			±0.7		LSBs

7.11 AC Performance: ADC3444

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER		TEST CONDITIONS	ADC3444 (f_S = 125 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		72.6			73		dBFS
		f_{IN} = 70 MHz	70.2	72.5			72.9		
		f_{IN} = 100 MHz		72.2			72.7		
		f_{IN} = 170 MHz		71.7			72.3		
		f_{IN} = 230 MHz		70.8			71.7		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		72.4			72.8		
		f_{IN} = 70 MHz		72.3			72.7		
		f_{IN} = 100 MHz		72.1			72.5		
		f_{IN} = 170 MHz		71.5			72.1		
		f_{IN} = 230 MHz		70.6			71.5		
NSD[(1)]	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–150.4			–150.9		dBFS/Hz
		f_{IN} = 70 MHz		–150.4	–148.1		–150.8		
		f_{IN} = 100 MHz		–150.1			–150.5		
		f_{IN} = 170 MHz		–149.5			–150.2		
		f_{IN} = 230 MHz		–148.7			–149.6		
SINAD[(1)]	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.6			72.9		dBFS
		f_{IN} = 70 MHz	69.3	72.3			72.7		
		f_{IN} = 100 MHz		72.3			72.7		
		f_{IN} = 170 MHz		71.5			72		
		f_{IN} = 230 MHz		69.9			70.6		
ENOB[(1)]	Effective number of bits	f_{IN} = 10 MHz		11.8			11.8		Bits
		f_{IN} = 70 MHz	11.2	11.8			11.8		
		f_{IN} = 100 MHz		11.7			11.8		
		f_{IN} = 170 MHz		11.6			11.7		
		f_{IN} = 230 MHz		11.4			11.6		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		92			87		dBc
		f_{IN} = 70 MHz	80	93			88		
		f_{IN} = 100 MHz		89			89		
		f_{IN} = 170 MHz		86			84		
		f_{IN} = 230 MHz		82			82		

(1) Reported from a 1-MHz offset.

AC Performance: ADC3444 (continued)

at maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); typical values are specified at an ambient temperature of 25°C; minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C

PARAMETER		TEST CONDITIONS	ADC3444 (f_S = 125 MSPS)						UNIT
			DITHER ON			DITHER OFF			
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		93			93		dBc
		f_{IN} = 70 MHz	80	94			91		
		f_{IN} = 100 MHz		90			90		
		f_{IN} = 170 MHz		86			85		
		f_{IN} = 230 MHz		81			80		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		96			88		dBc
		f_{IN} = 70 MHz	81	95			89		
		f_{IN} = 100 MHz		95			89		
		f_{IN} = 170 MHz		93			87		
		f_{IN} = 230 MHz		87			86		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		100			93		dBc
		f_{IN} = 70 MHz	86	99			94		
		f_{IN} = 100 MHz		94			92		
		f_{IN} = 170 MHz		96			93		
		f_{IN} = 230 MHz		94			90		
THD	Total harmonic distortion	f_{IN} = 10 MHz		91			85		dBc
		f_{IN} = 70 MHz	77	91			85		
		f_{IN} = 100 MHz		88			86		
		f_{IN} = 170 MHz		85			82		
		f_{IN} = 230 MHz		80			78		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		–97			–97		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		–87			–87		
INL	Integral nonlinearity	f_{IN} = 70 MHz		±0.75	±3		±0.75		LSBs
DNL	Differential nonlinearity	f_{IN} = 70 MHz	–0.95	±0.7			±0.7		LSBs

7.12 Digital Characteristics

the dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1; AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, PDN)							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current	RESET, SDATA, SCLK, PDN	V_{HIGH} = 1.8 V		10		µA
		SEN(1)	V_{HIGH} = 1.8 V		0		
I_{IL}	Low-level input current	RESET, SDATA, SCLK, PDN	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		10		
DIGITAL INPUTS (SYSREFP, SYSREFM)							
	Differential swing			0.2	0.8	1.0	V
	Common-mode voltage for SYSREF(2)				0.9		V
DIGITAL OUTPUTS (CMOS Interface, SDOUT)							
V_{OH}	High-level output voltage			DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS (LVDS Interface)							
V_{ODH}	High-level output differential voltage		With an external 100-Ω termination	280	350	–280	mV
V_{ODL}	Low-level output differential voltage		With an external 100-Ω termination	–460	–350	–460	mV
V_{OCM}	Output common-mode voltage			0.9	1.05	1.2	V

(1) SEN has an internal 150-kΩ pullup resistor to AVDD. SPI pins (SEN, SCLK, SDATA) may be driven by 1.8 V or 3.3 V CMOS buffers.
(2) SYSREF is internally biased to 0.9 V.

7.13 Timing Requirements: General

typical values are at T_A = 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C

			MIN	TYP	MAX	UNIT
t_A	Aperture delay		1.24	1.44	1.64	ns
	Aperture delay matching between two channels of the same device			±70		ps
	Variation of aperture delay between two devices at the same temperature and supply voltage			±150		ps
t_J	Aperture jitter			130		f_S rms
	Wake-up time	Time to valid data after exiting standby power-down mode		35	200	µs
		Time to valid data after exiting global power-down mode (in this mode, both channels power down)		85	450	µs
	ADC latency(1)	2-wire mode (default)		9		Clock cycles
		1-wire mode		8		Clock cycles
t_{SU_SYSREF}	SYSREF reference time	Setup time for SYSREF referenced to input clock falling edge	1000			ps
t_{H_SYSREF}		Hold time for SYSREF referenced to input clock falling edge	100			ps

(1) Overall latency = ADC latency + t_{PDI}; see Figure 141.

7.14 Timing Requirements: LVDS Output

typical values are at 25°C, AVDD = DVDD = 1.8 V, –1-dBFS differential input, 7x serialization (2-wire mode), C_{LOAD} = 3.3 pF[(1)], and R_{LOAD} = 100 Ω[(2)] (unless otherwise noted); minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C[(3)(4)]

			MIN	TYP	MAX	UNIT
t_{SU}	Data setup time: data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)[(5)]		0.36	0.42		ns
t_{HO}	Data hold time: zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid[(5)]		0.36	0.47		ns
	LVDS bit clock duty cycle: duty cycle of differential clock (CLKOUTP – CLKOUTM)			49%		
t_{PDI}	Clock propagation delay: input clock falling edge cross-over to frame clock rising edge cross-over 15 MSPS < sampling frequency < 125 MSPS	1-wire mode	2.7	4.5	6.5	ns
		2-wire mode		$0.44 \times t_S + t_{DELAY}$		ns
t_{DELAY}	Delay time		3	4.5	5.9	ns
t_{FALL}, t_{RISE}	Data fall time, data rise time: rise time measured from –100 mV to 100 mV, *15 MSPS ≤ Sampling frequency ≤ 125 MSPS*			0.11		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time: rise time measured from –100 mV to 100 mV, *15 MSPS ≤ Sampling frequency ≤ 125 MSPS*			0.11		ns

(1) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(2) R_{LOAD} is the differential load resistance between the LVDS output pair.
(3) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(4) Timing parameters are ensured by design and characterization and are not tested in production.
(5) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.

Table 1. LVDS Timings at Lower Sampling Frequencies: 7x Serialization (2-Wire Mode)

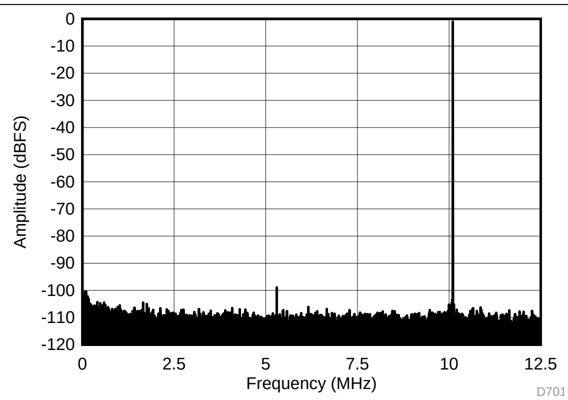
SAMPLING FREQUENCY (MSPS)	SETUP TIME (t_{SU}, ns)			HOLD TIME (t_{HO}, ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
25	2.27	2.6		2.41	2.6	
40	1.44	1.6		1.51	1.7	
50	1.2	1.32		1.24	1.4	
60	0.95	1.04		0.97	1.09	
80	0.68	0.75		0.72	0.81	
100	0.5	0.57		0.53	0.62	

Table 2. LVDS Timings at Lower Sampling Frequencies: 14x Serialization (1-Wire Mode)

SAMPLING FREQUENCY (MSPS)	SETUP TIME (t_{SU}, ns)			HOLD TIME (t_{HO}, ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
25	1.1	1.24		1.19	1.34	
40	0.66	0.72		0.74	0.82	
50	0.48	0.55		0.54	0.64	
60	0.35	0.41		0.42	0.51	
80	0.17	0.24		0.3	0.38	

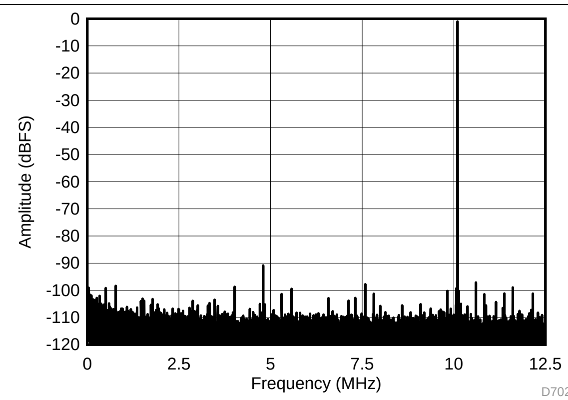
7.15 Typical Characteristics: ADC3441

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



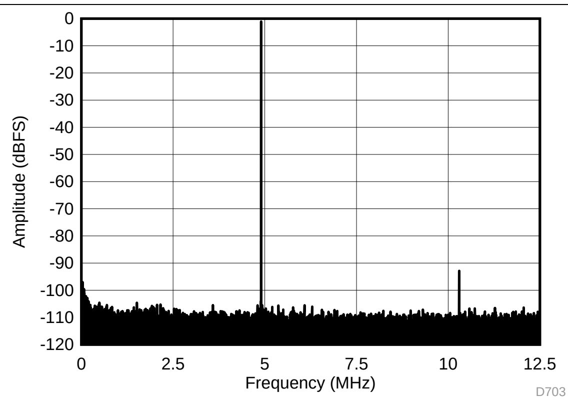
SFDR = 98 dBc, SNR = 73.1 dBFS, SINAD = 73 dBFS,
THD = 97 dBc, HD2 = 110.0 dBc,
HD3 = 98 dBc, SFDR = 100 dBc (excluding HD2, HD3)

Figure 1. FFT for 10-MHz Input Signal (Dither On)



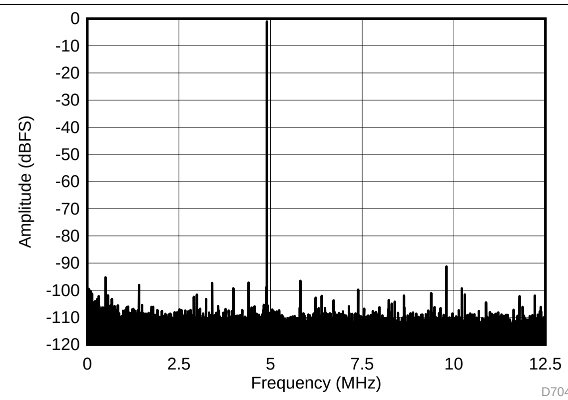
SFDR = 90 dBc, SNR = 73.5 dBFS, SINAD = 73.2 dBFS,
THD = 88 dBc, HD2 = 90 dBc,
HD3 = 100 dBc, SFDR = 92 dBc (excluding HD2, HD3)

Figure 2. FFT for 10-MHz Input Signal (Dither Off)



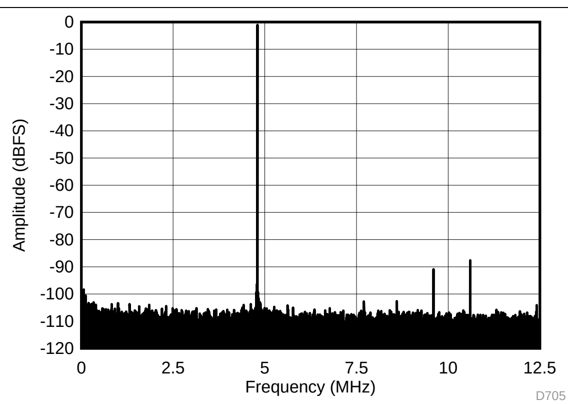
SFDR = 92 dBc, SNR = 72.5 dBFS, SINAD = 72.3 dBFS,
THD = 91 dBc, HD2 = 108 dBc,
HD3 = 92 dBc, SFDR = 101 dBc (excluding HD2, HD3)

Figure 3. FFT for 70-MHz Input Signal (Dither On)



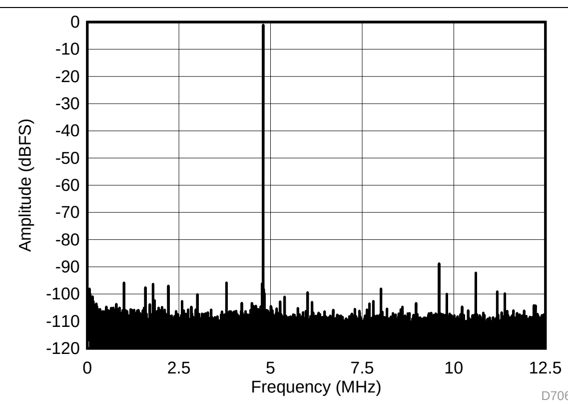
SFDR = 90 dBc, SNR = 72.9 dBFS, SINAD = 72.7 dBFS,
THD = 89 dBc, HD2 = 90 dBc,
HD3 = 101 dBc, SFDR = 93 dBc (excluding HD2, HD3)

Figure 4. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 87 dBc, SNR = 71.5 dBFS, SINAD = 71.1 dBFS,
THD = 85 dBc, HD2 = 90 dBc,
HD3 = 87 dBc, SFDR = 100 dBc (excluding HD2, HD3)

Figure 5. FFT for 170-MHz Input Signal (Dither On)

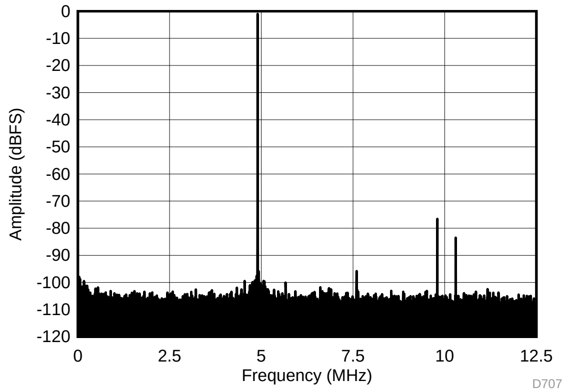


SFDR = 88 dBc, SNR = 71.7 dBFS, SINAD = 71.4 dBFS,
THD = 85 dBc, HD2 = 88 dBc,
HD3 = 91 dBc, SFDR = 93 dBc (excluding HD2, HD3)

Figure 6. FFT for 170-MHz Input Signal (Dither Off)

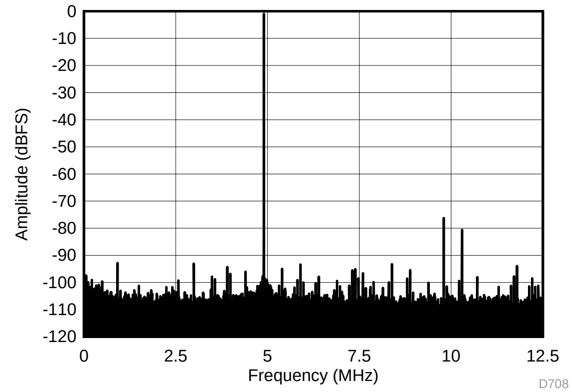
Typical Characteristics: ADC3441 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



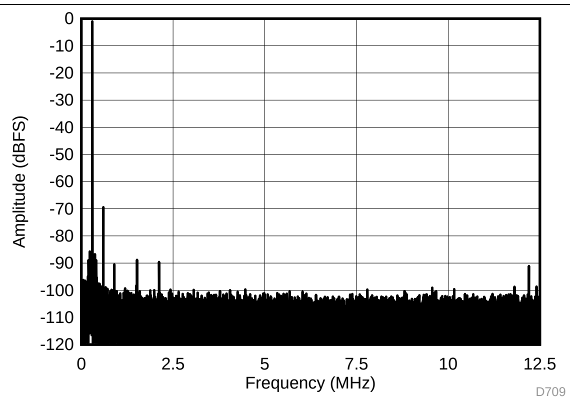
SFDR = 76 dBc, SNR = 69.4 dBFS, SINAD = 68.8 dBFS, THD = 75 dBc, HD2 = 76 dBc, HD3 = 83 dBc, SFDR = 96 dBc (excluding HD2, HD3)

Figure 7. FFT for 270-MHz Input Signal (Dither On)



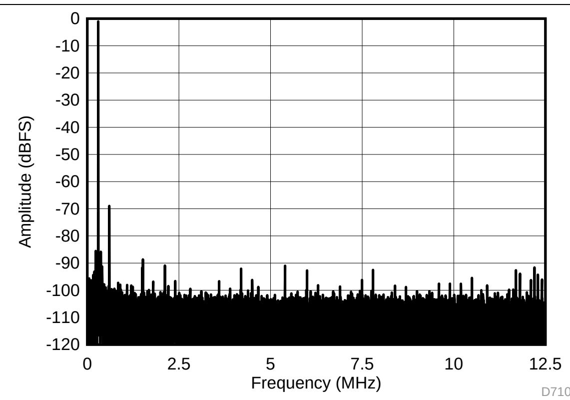
SFDR = 75 dBc, SNR = 69.6 dBFS, SINAD = 68.6 dBFS, THD = 74 dBc, HD2 = 75 dBc, HD3 = 80 dBc, SFDR = 91 dBc (excluding HD2, HD3)

Figure 8. FFT for 270-MHz Input Signal (Dither Off)



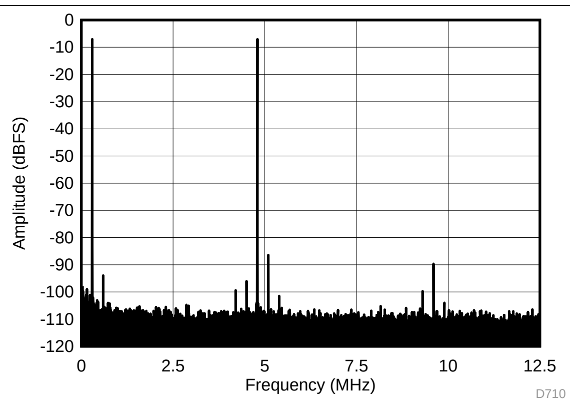
SFDR = 68 dBc, SNR = 66.7 dBFS, SINAD = 66.5 dBFS, THD = 92 dBc, HD2 = 68 dBc, HD3 = 90 dBc, SFDR = 91 dBc (excluding HD2, HD3)

Figure 9. FFT for 450-MHz Input Signal (Dither On)



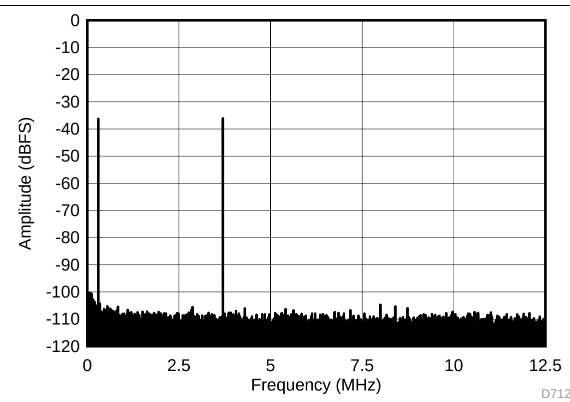
SFDR = 66 dBc, SNR = 66.8 dBFS, SINAD = 66.5 dBFS, THD = 88 dBc, HD2 = 66 dBc, HD3 = 97 dBc, SFDR = 90 dBc (excluding HD2, HD3)

Figure 10. FFT for 450-MHz Input Signal (Dither Off)



f_{IN1} = 46.3 MHz, f_{IN2} = 50.3 MHz, IMD3 = 86 dBFS, each tone at –7 dBFS

Figure 11. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

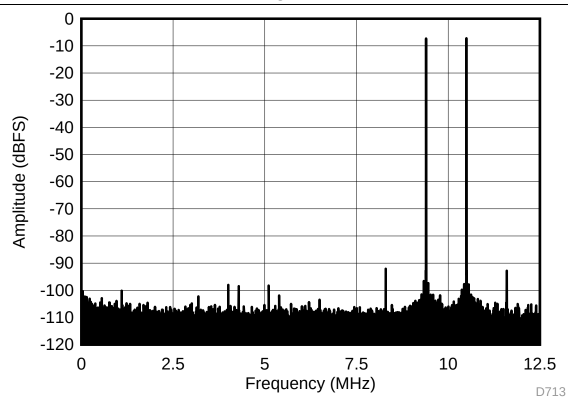


f_{IN1} = 46.3 MHz, f_{IN2} = 50.3 MHz, IMD3 = 105 dBFS, each tone at –36 dBFS

Figure 12. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

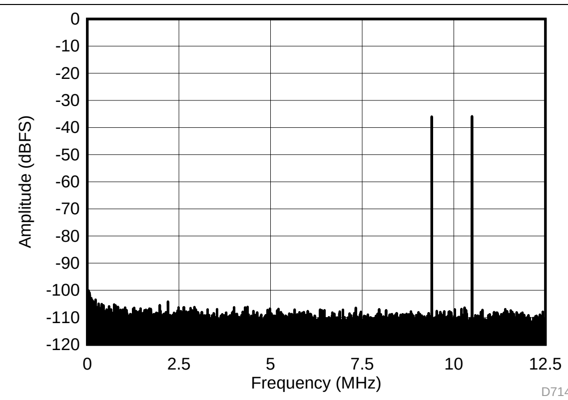
Typical Characteristics: ADC3441 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



f_{IN1} = 184.5 MHz, f_{IN2} = 189.5 MHz, IMD3 = 93 dBFS, each tone at –7 dBFS

Figure 13. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



f_{IN1} = 184.5 MHz, f_{IN2} = 189.5 MHz, IMD3 = 109 dBFS, each tone at –36 dBFS

Figure 14. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

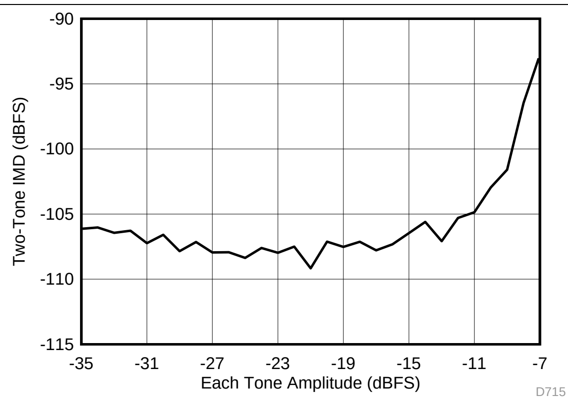


Figure 15. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

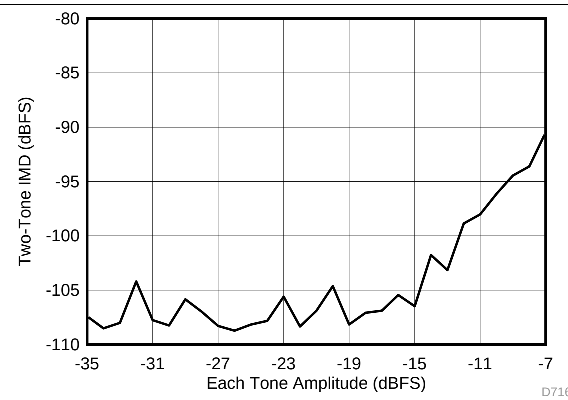


Figure 16. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

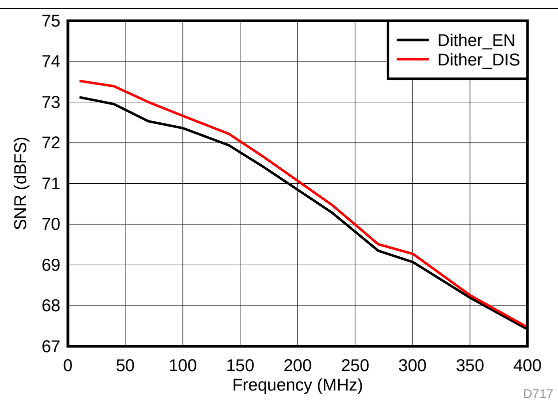


Figure 17. Signal-to-Noise Ratio vs Input Frequency

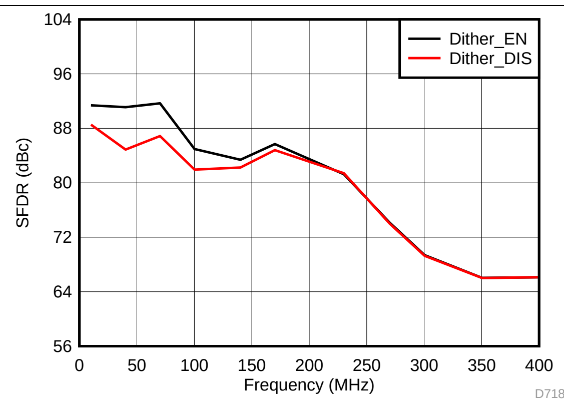


Figure 18. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC3441 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

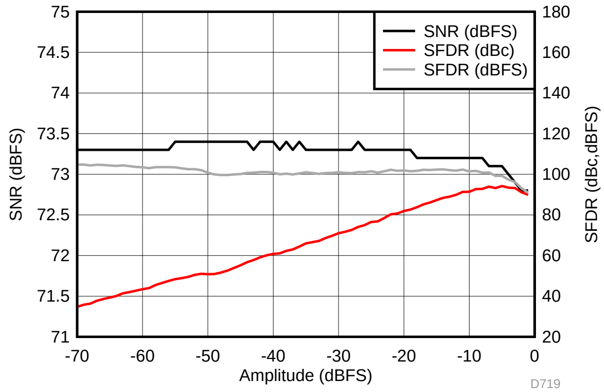


Figure 19. Performance vs Input Amplitude (30 MHz)

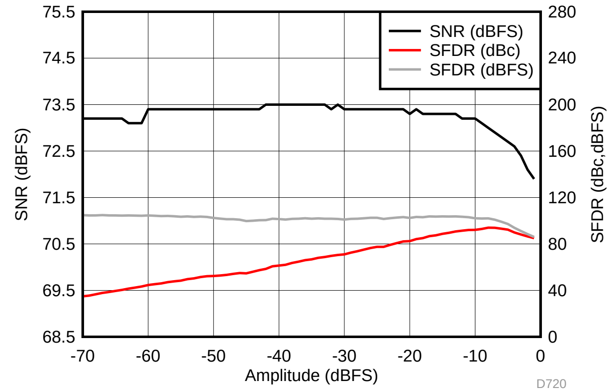


Figure 20. Performance vs Input Amplitude (170 MHz)

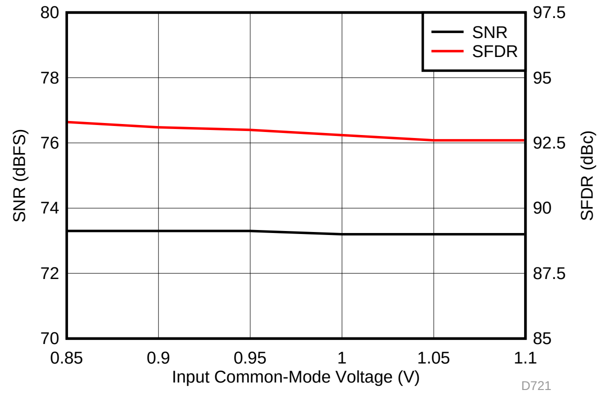


Figure 21. Performance vs Input Common-Mode Voltage (30 MHz)

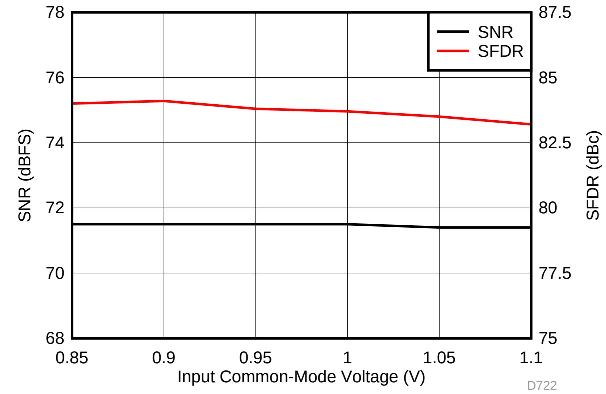


Figure 22. Performance vs Input Common-Mode Voltage (170 MHz)

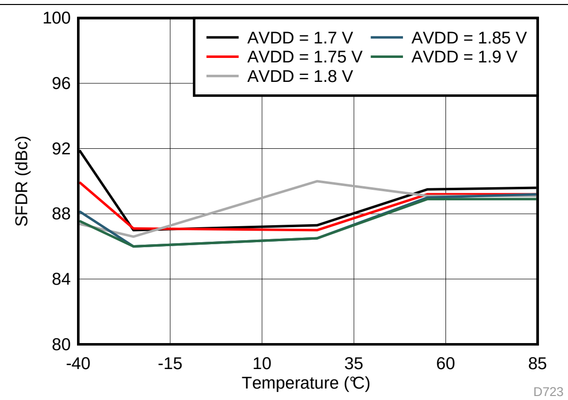


Figure 23. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (30 MHz)

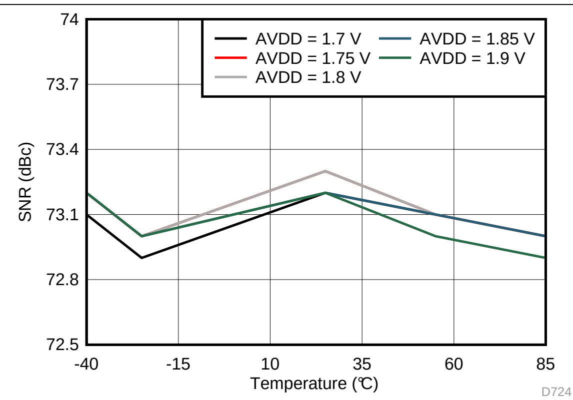


Figure 24. Signal-to-Noise Ratio vs AVDD Supply and Temperature (30 MHz)

Typical Characteristics: ADC3441 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

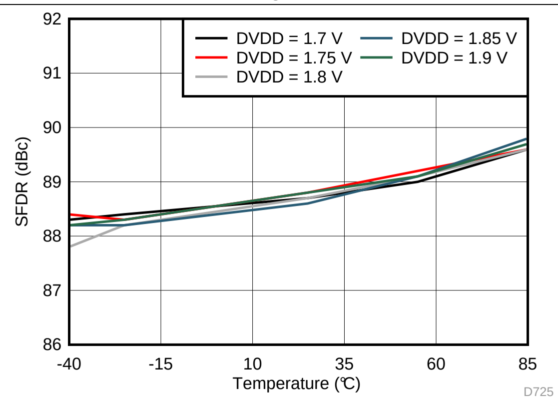


Figure 25. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)

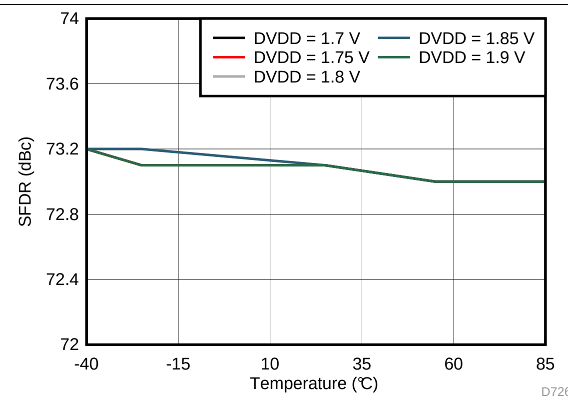


Figure 26. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)

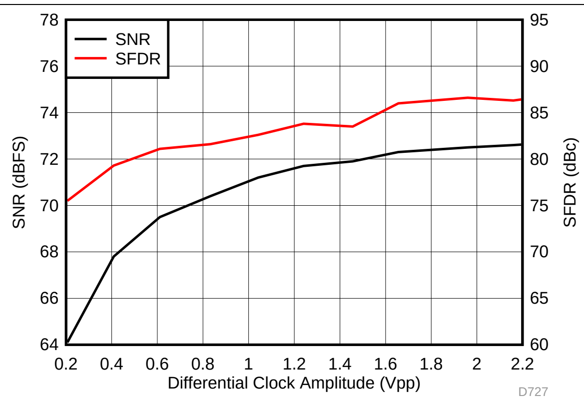


Figure 27. Performance vs Clock Amplitude (40 MHz)

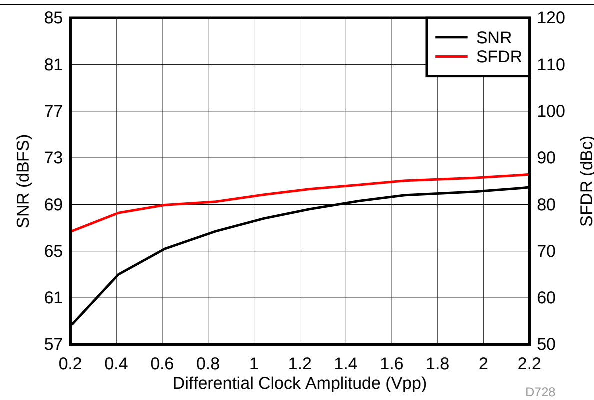


Figure 28. Performance vs Clock Amplitude (150 MHz)

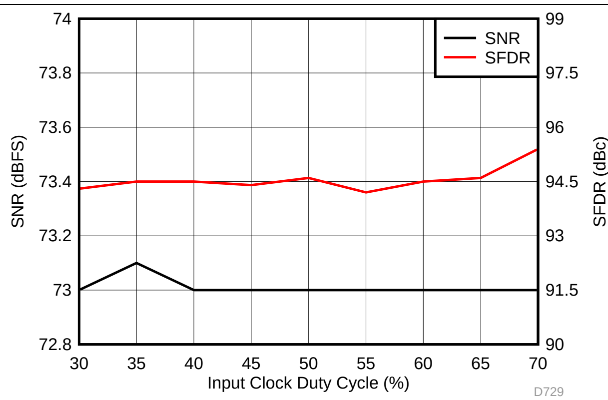


Figure 29. Performance vs Clock Duty Cycle (30 MHz)

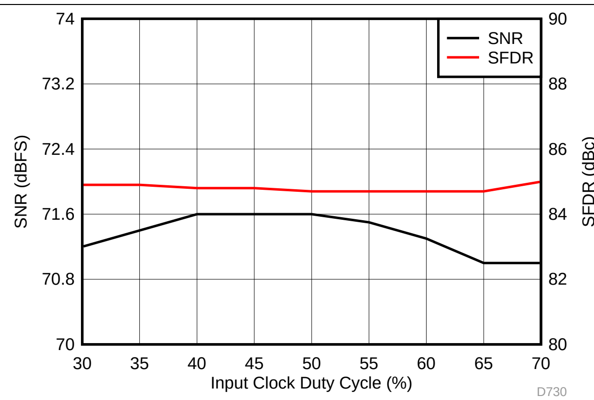


Figure 30. Performance vs Clock Duty Cycle (150 MHz)

Typical Characteristics: ADC3441 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

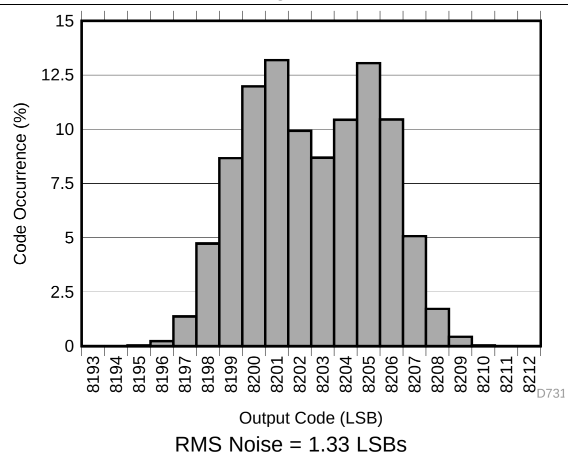


Figure 31. Idle Channel Histogram

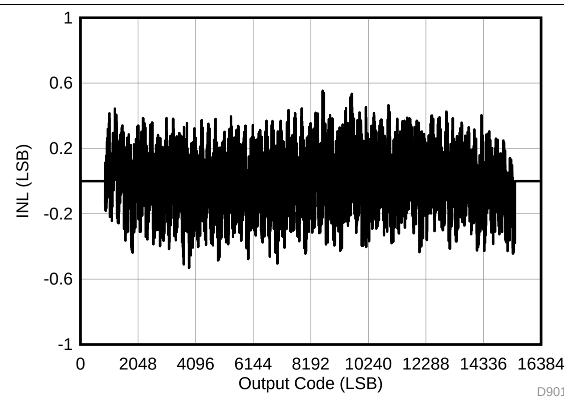


Figure 32. Integral Nonlinearity for 20-MHz Input

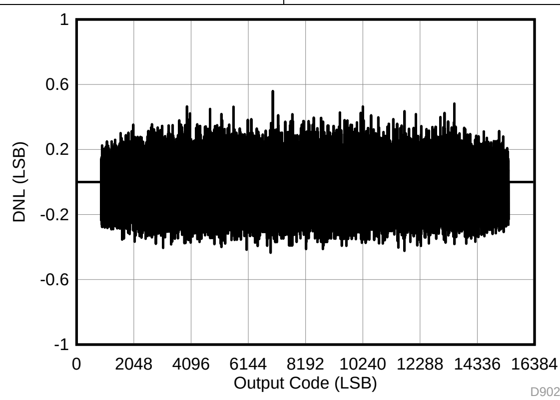
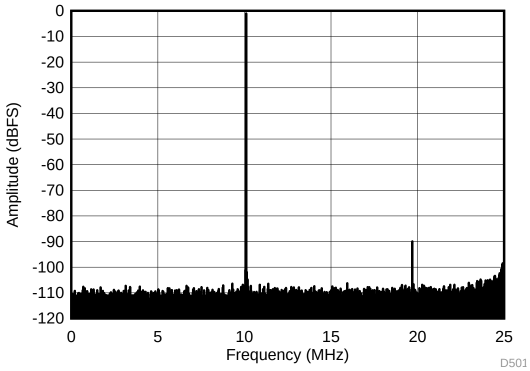


Figure 33. Differential Nonlinearity for 20-MHz Input

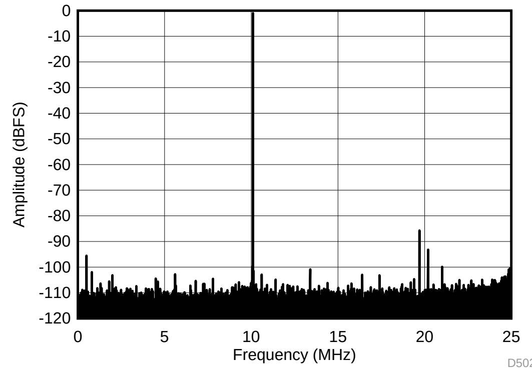
7.16 Typical Characteristics: ADC3442

typical values are at T_A = 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



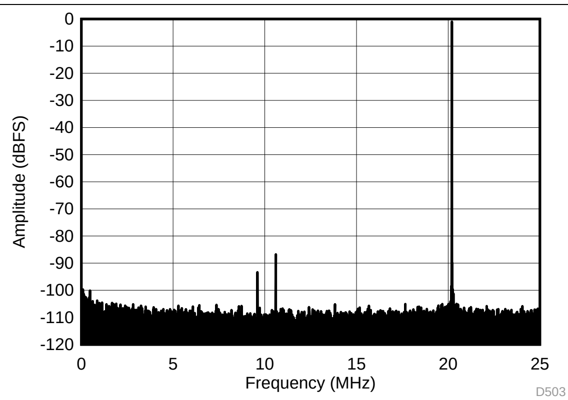
SFDR = 89 dBc, SNR = 73.1 dBFS, SINAD = 73 dBFS,
THD = 89 dBc, HD2 = 111 dBc,
HD3 = 89 dBc, SFDR = 100 dBc (excluding HD2, HD3)

Figure 34. FFT for 10-MHz Input Signal (Chopper On, Dither On)



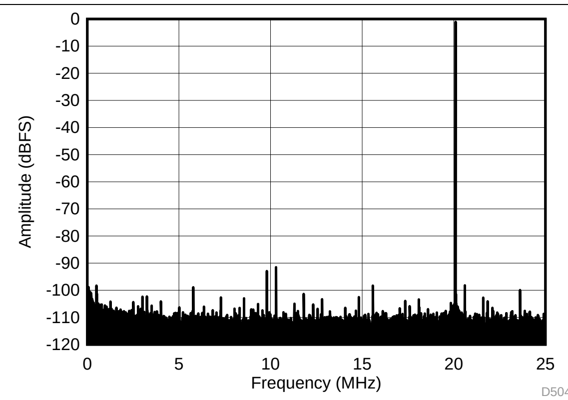
SFDR = 85 dBc, SNR = 73.5 dBFS, SINAD = 73.3 dBFS,
THD = 84 dBc, HD2 = 92 dBc,
HD3 = 85 dBc, SFDR = 96 dBc (excluding HD2, HD3)

Figure 35. FFT for 10-MHz Input Signal (Chopper On, Dither Off)



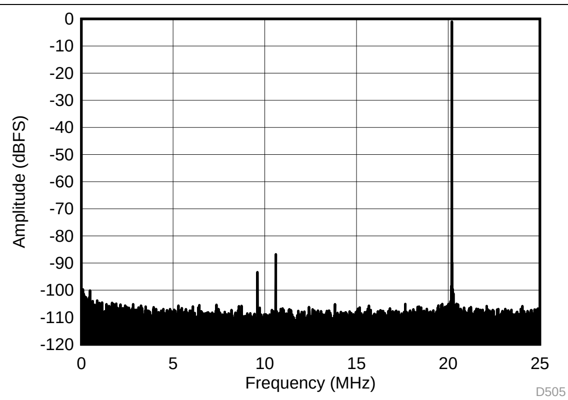
SFDR = 86 dBc, SNR = 72.7 dBFS, SINAD = 72.5 dBFS,
THD = 85 dBc, HD2 = 92 dBc,
HD3 = 86 dBc, SFDR = 100 dBc (excluding HD2, HD3)

Figure 36. FFT for 70-MHz Input Signal (Dither On)



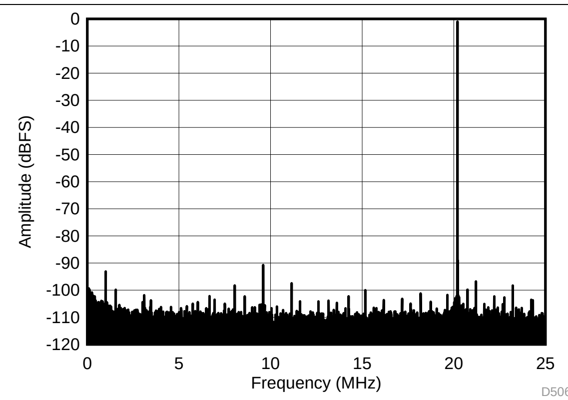
SFDR = 90 dBc, SNR = 73.1 dBFS, SINAD = 73 dBFS,
THD = 88 dBc, HD2 = 92 dBc,
HD3 = 90 dBc, SFDR = 95 dBc (excluding HD2, HD3)

Figure 37. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 86 dBc, SNR = 71.6 dBFS, SINAD = 71.4 dBFS,
THD = 85 dBc, HD2 = 92 dBc,
HD3 = 86 dBc, SFDR = 99 dBc (excluding HD2, HD3)

Figure 38. FFT for 170-MHz Input Signal (Dither On)

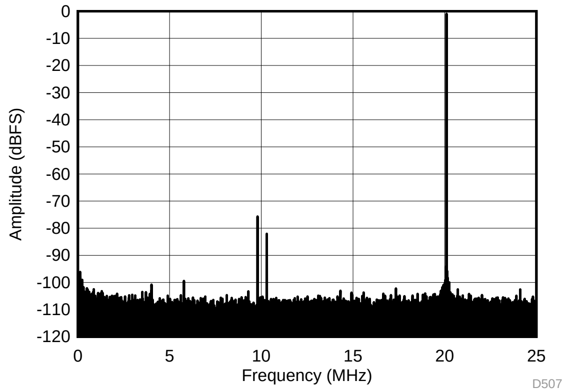


SFDR = 90 dBc, SNR = 71.8 dBFS, SINAD = 71.6 dBFS,
THD = 87 dBc, HD2 = 90 dBc,
HD3 = 108 dBc, SFDR = 93 dBc (excluding HD2, HD3)

Figure 39. FFT for 170-MHz Input Signal (Dither Off)

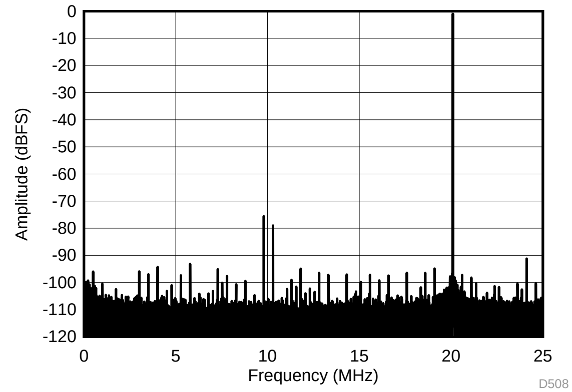
Typical Characteristics: ADC3442 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



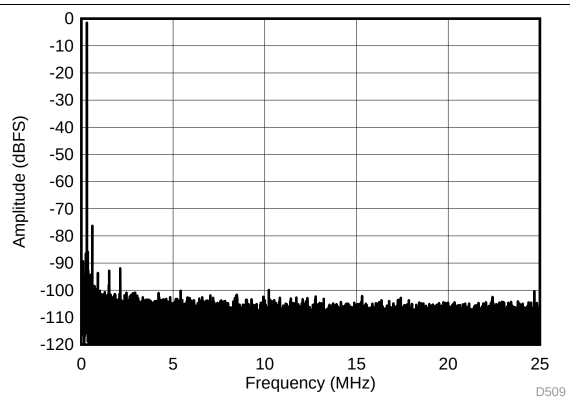
SFDR = 75 dBc, SNR = 70.3 dBFS, SINAD = 69.1 dBFS,
THD = 74 dBc, HD2 = -75 dBc,
HD3 = 81 dBc, SFDR = 95 dBc (excluding HD2, HD3)

Figure 40. FFT for 270-MHz Input Signal (Dither On)



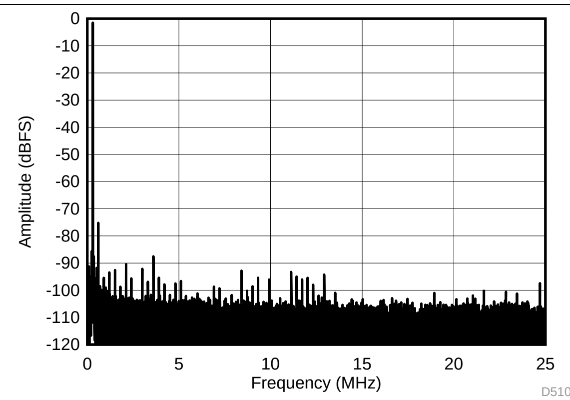
SFDR = 75 dBc, SNR = 70.6 dBFS, SINAD = 69.6 dBFS,
THD = 73 dBc, HD2 = 75 dBc,
HD3 = 78 dBc, SFDR = 91 dBc (excluding HD2, HD3)

Figure 41. FFT for 270-MHz Input Signal (Dither Off)



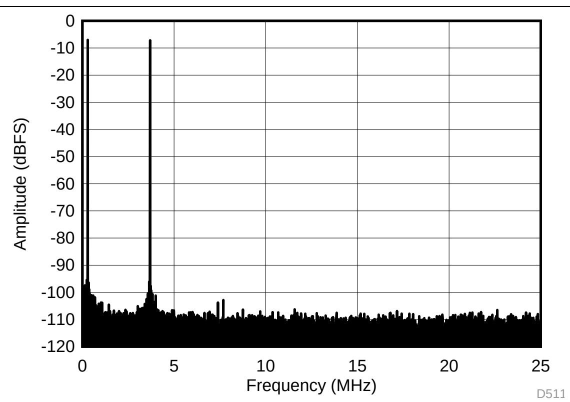
SFDR = 68 dBc, SNR = 68.2 dBFS, SINAD = 68 dBFS,
THD = 86 dBc, HD2 = 68 dBc, HD3 = 87 dBc

Figure 42. FFT for 450-MHz Input Signal (Dither On)



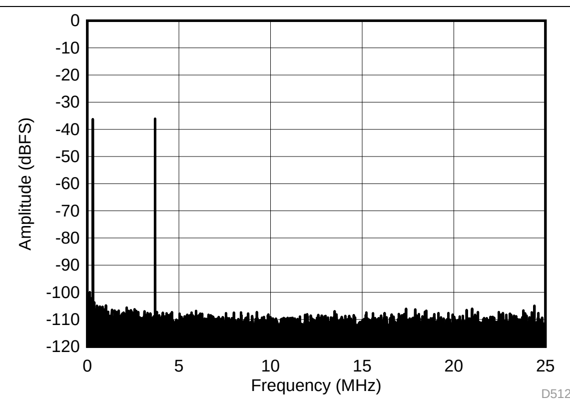
SFDR = 68 dBc, SNR = 68.5 dBFS, SINAD = 68.3 dBFS,
THD = 86 dBc, HD2 = 68 dBc, HD3 = 90 dBc

Figure 43. FFT for 450-MHz Input Signal (Dither Off)



f_{IN1} = 46.3 MHz, f_{IN2} = 50.3 MHz, IMD3 = 102 dBFS,
each tone at –7 dBFS

Figure 44. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

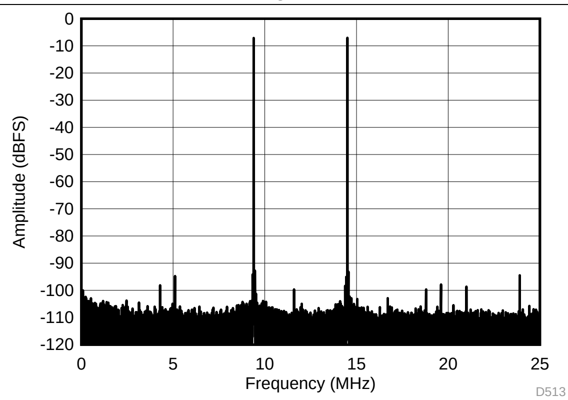


f_{IN1} = 46.3 MHz, f_{IN2} = 50.3 MHz, IMD3 = 110 dBFS,
each tone at –36 dBFS

Figure 45. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

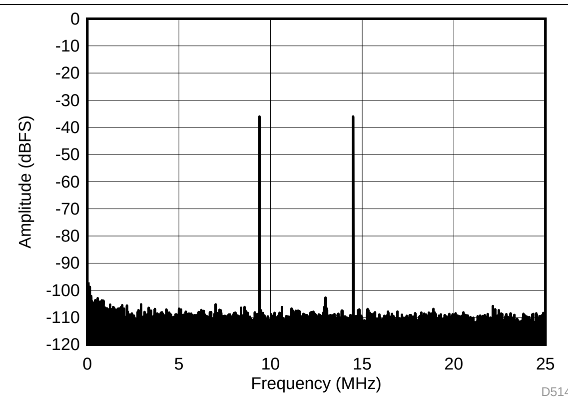
Typical Characteristics: ADC3442 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, IMD3 = 93 dBFS, each tone at –7 dBFS

Figure 46. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, IMD3 = 105 dBFS, each tone at –36 dBFS

Figure 47. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

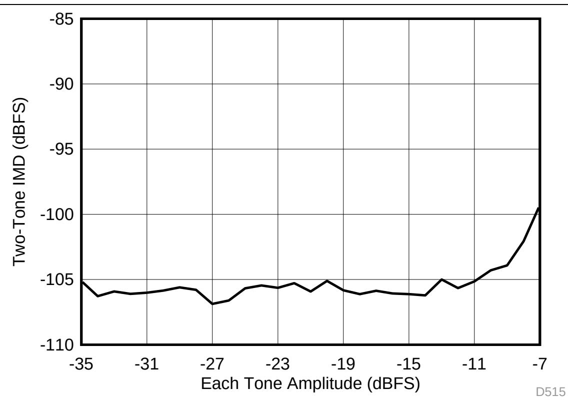


Figure 48. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

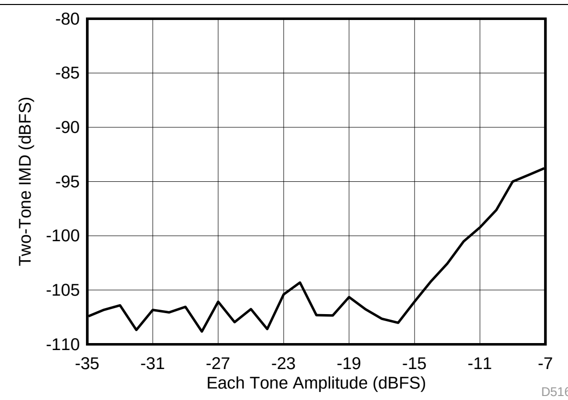


Figure 49. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

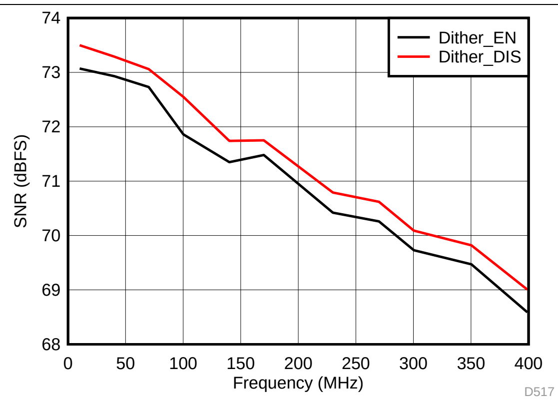


Figure 50. Signal-to-Noise Ratio vs Input Frequency

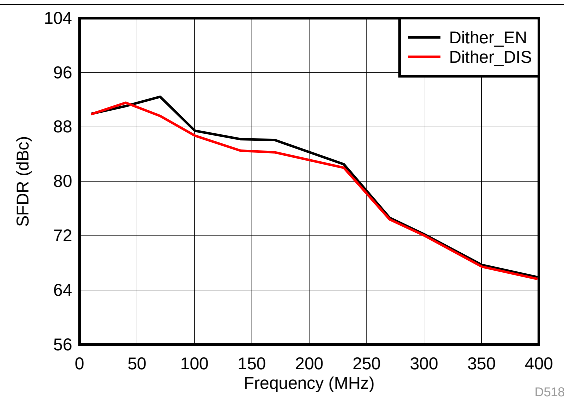


Figure 51. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC3442 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

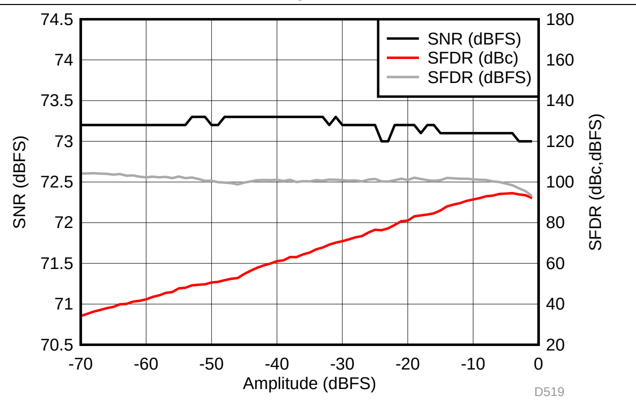


Figure 52. Performance vs Input Amplitude (30 MHz)

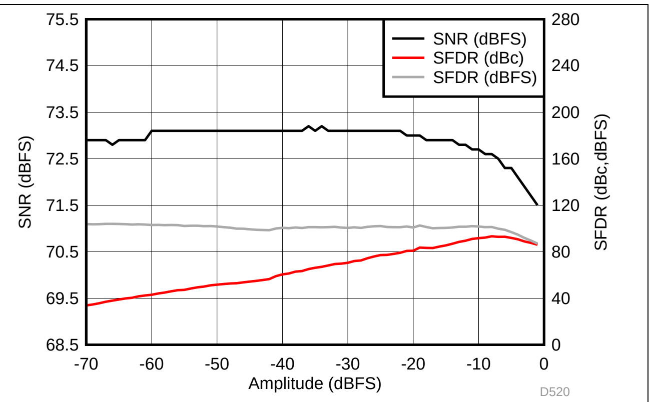


Figure 53. Performance vs Input Amplitude (170 MHz)

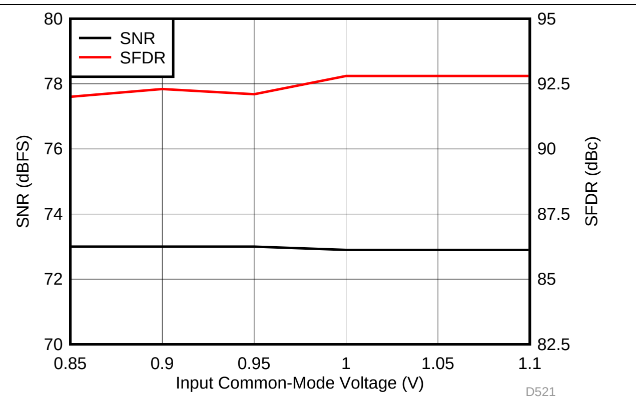


Figure 54. Performance vs Input Common-Mode Voltage (30 MHz)

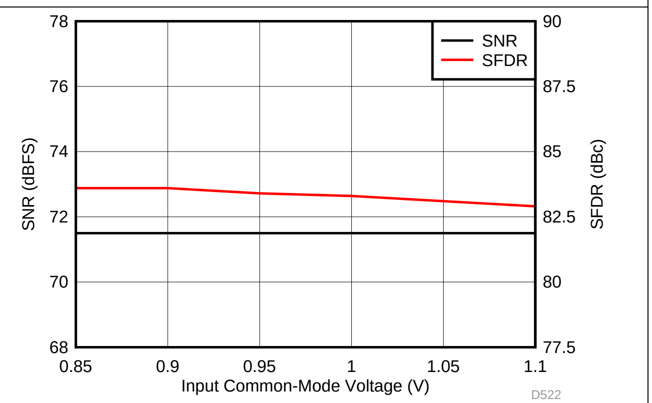


Figure 55. Performance vs Input Common-Mode Voltage (170 MHz)

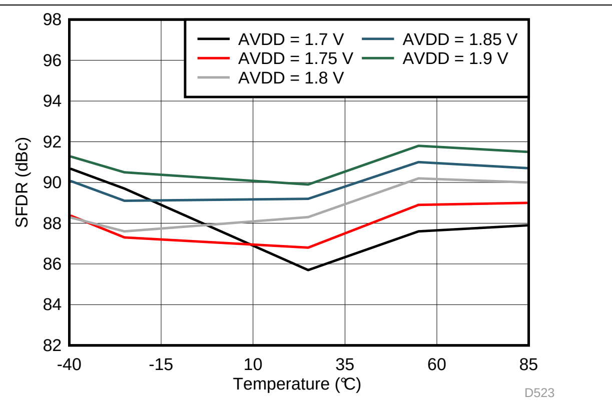


Figure 56. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (30 MHz)

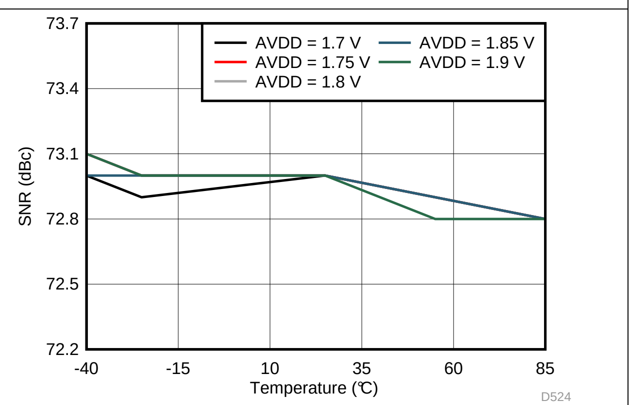


Figure 57. Signal-to-Noise Ratio vs AVDD Supply and Temperature (30 MHz)

Typical Characteristics: ADC3442 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

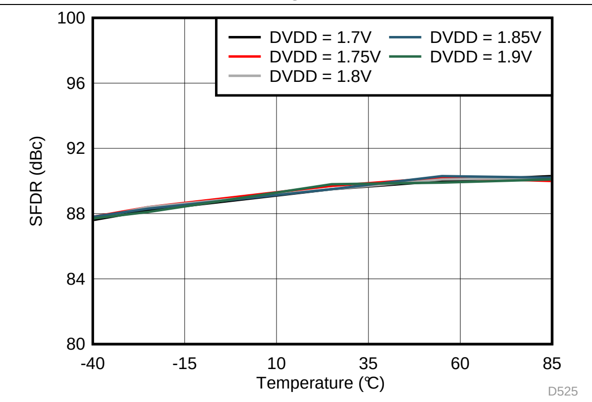


Figure 58. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)

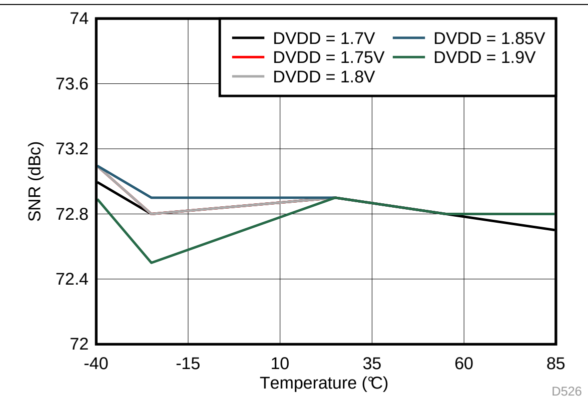


Figure 59. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)

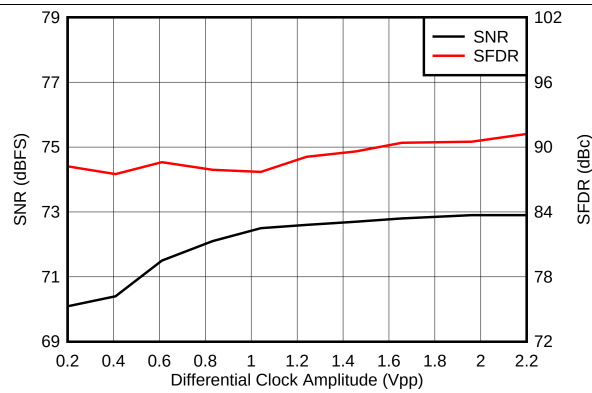


Figure 60. Performance vs Clock Amplitude (40 MHz)

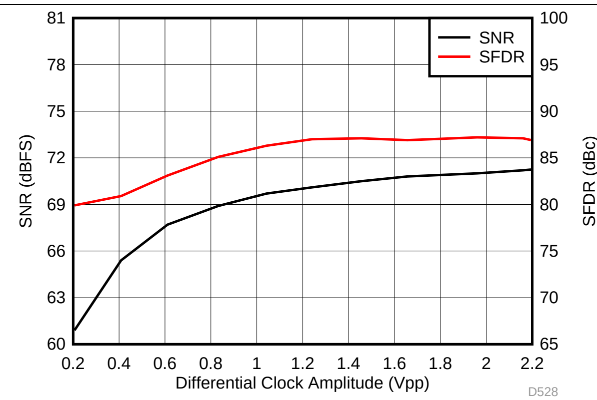


Figure 61. Performance vs Clock Amplitude (150 MHz)

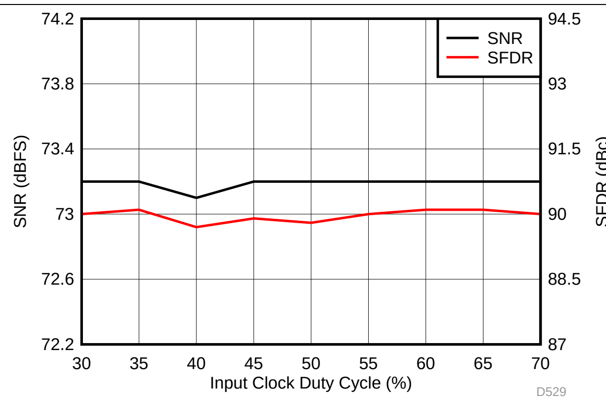


Figure 62. Performance vs Clock Duty Cycle (30 MHz)

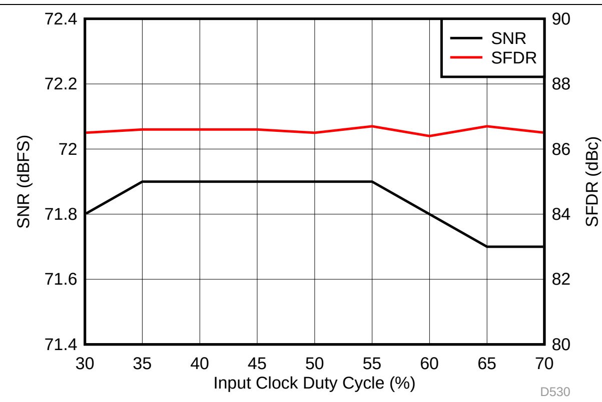
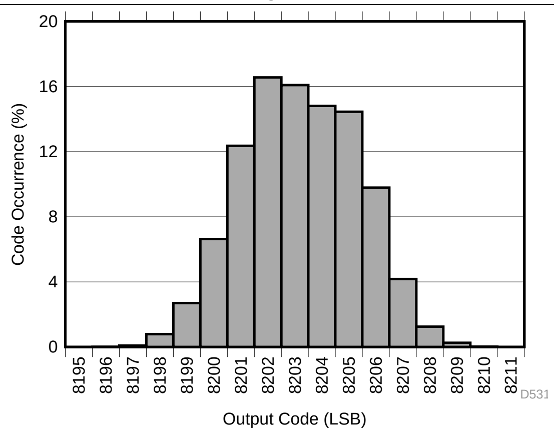


Figure 63. Performance vs Clock Duty Cycle (150 MHz)

Typical Characteristics: ADC3442 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



RMS noise = 1.3 LSBs

Figure 64. Idle Channel Histogram

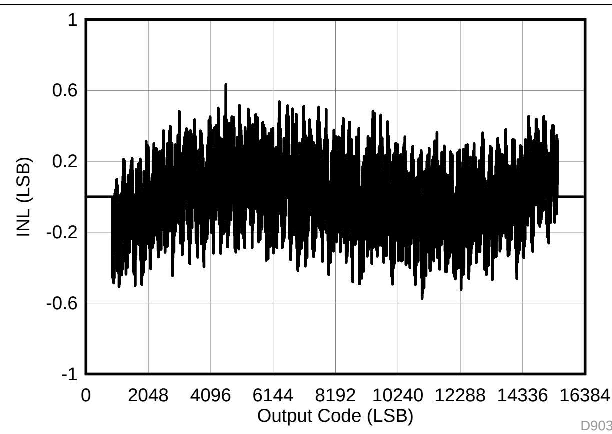


Figure 65. Integral Nonlinearity for 20-MHz Input

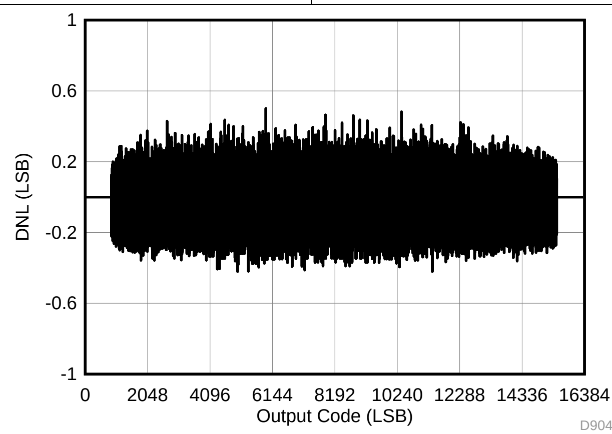
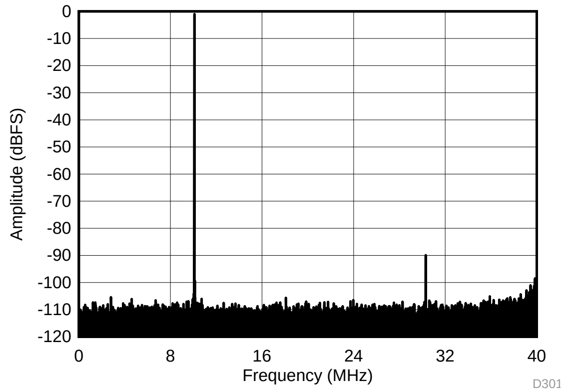


Figure 66. Differential Nonlinearity for 20-MHz Input

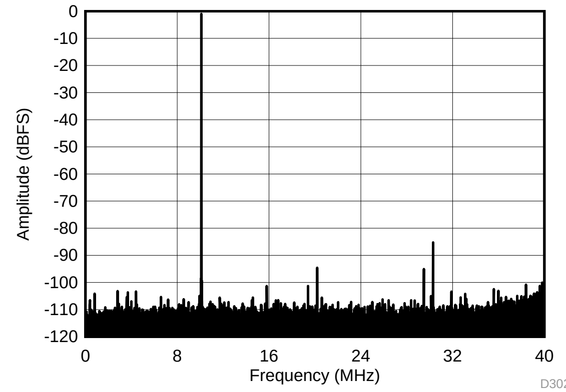
7.17 Typical Characteristics: ADC3443

typical values are at T_A = 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



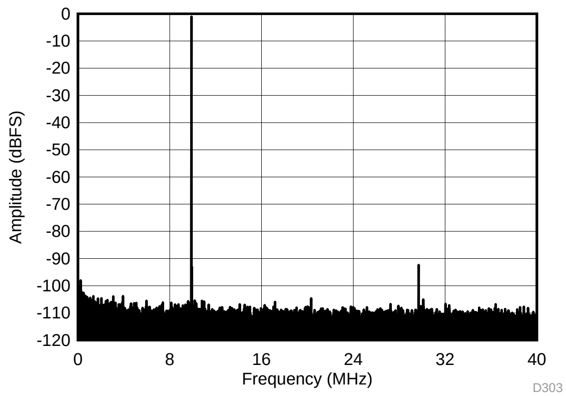
SFDR = 89 dBc, SNR = 73.1 dBFS, SINAD = 73 dBFS, THD = 89 dBc, HD2 = 110 dBc, HD3 = 89 dBc

Figure 67. FFT for 10-MHz Input Signal (Chopper On, Dither On)



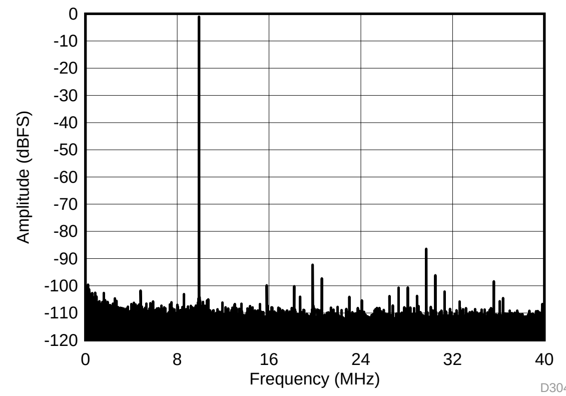
SFDR = 84 dBc, SNR = 73.2 dBFS, SINAD = 73.1 dBFS, THD = 83 dBc, HD2 = 94 dBc, HD3 = 84 dBc

Figure 68. FFT for 10-MHz Input Signal (Chopper On, Dither Off)



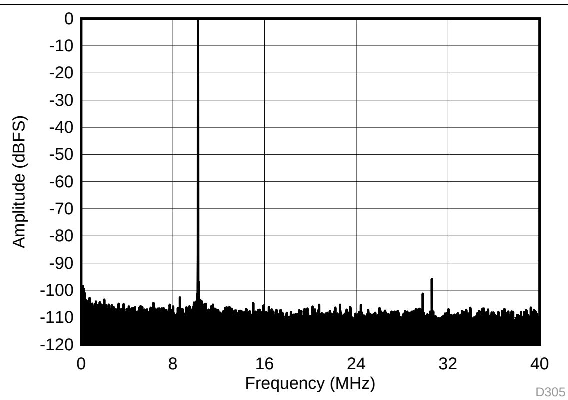
SFDR = 91 dBc, SNR = 72.9 dBFS, SINAD = 72.8 dBFS, THD = 91 dBc, HD2 = 110 dBc, HD3 = 91 dBc

Figure 69. FFT for 70-MHz Input Signal (Dither On)



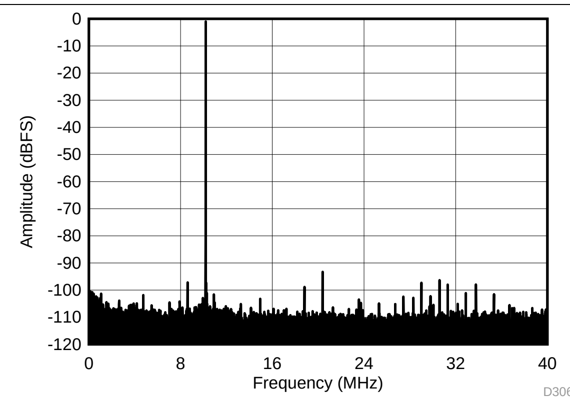
SFDR = 85 dBc, SNR = 73.1 dBFS, SINAD = 72.9 dBFS, THD = 84 dBc, HD2 = 91 dBc, HD3 = 85 dBc

Figure 70. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 95 dBc, SNR = 72.1 dBFS, SINAD = 71.9 dBFS, THD = 93 dBc, HD2 = 106 dBc, HD3 = 95 dBc

Figure 71. FFT for 170-MHz Input Signal (Dither On)

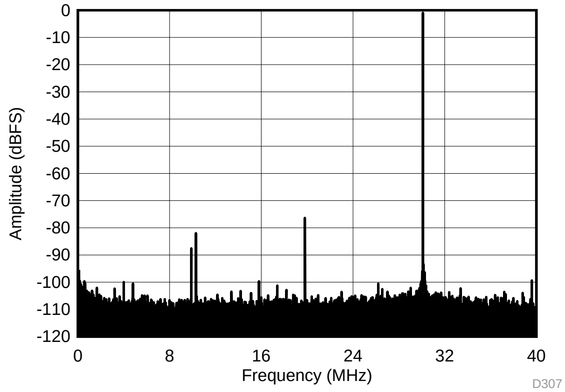


SFDR = 92 dBc, SNR = 72.4 dBFS, SINAD = 72.2 dBFS, THD = 88 dBc, HD2 = 92 dBc, HD3 = 95 dBc

Figure 72. FFT for 170-MHz Input Signal (Dither Off)

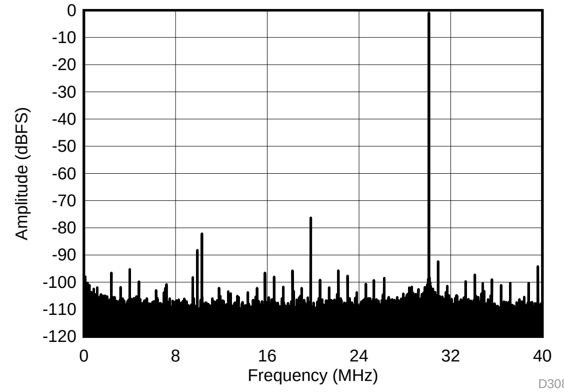
Typical Characteristics: ADC3443 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



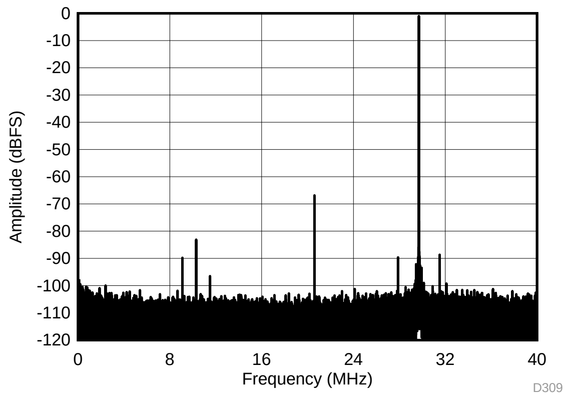
SFDR = 75 dBc, SNR = 70.5 dBFS, SINAD = 69.6 dBFS, THD = 74 dBc, HD2 = 75 dBc, HD3 = 81 dBc

Figure 73. FFT for 270-MHz Input Signal (Dither On)



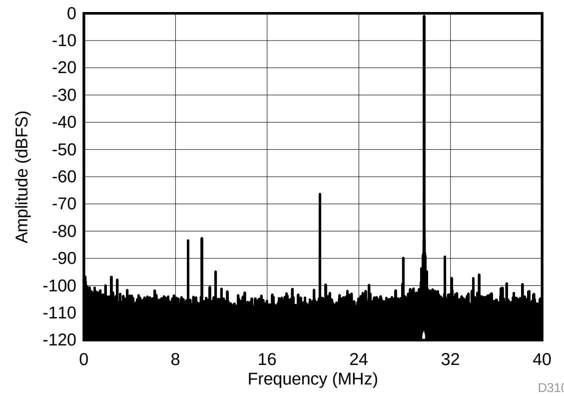
SFDR = 75 dBc, SNR = 71 dBFS, SINAD = 69.7 dBFS, THD = 74 dBc, HD2 = 75 dBc, HD3 = 81 dBc

Figure 74. FFT for 270-MHz Input Signal (Dither Off)



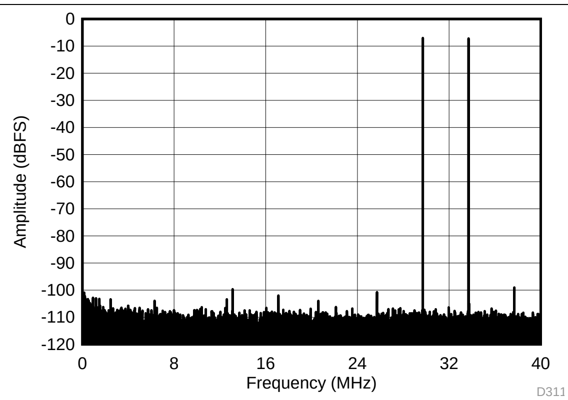
SFDR = 66 dBc, SNR = 68.4 dBFS, SINAD = 64.6 dBFS, THD = 66 dBc, HD2 = 66 dBc, HD3 = 89 dBc

Figure 75. FFT for 450-MHz Input Signal (Dither On)



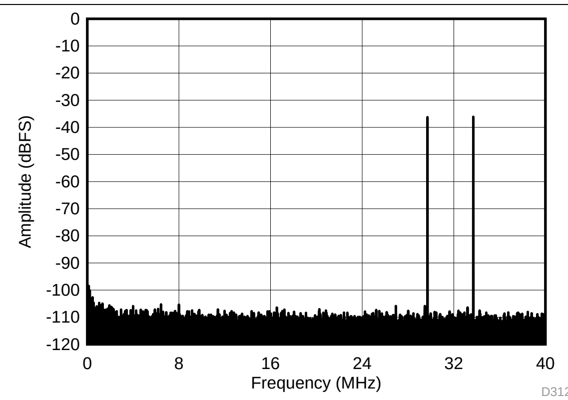
SFDR = 65 dBc, SNR = 68.7 dBFS, SINAD = 64.4 dBFS, THD = 65 dBc, HD2 = 65 dBc, HD3 = 82 dBc

Figure 76. FFT for 450-MHz Input Signal (Dither Off)



f_{IN1} = 46 MHz, f_{IN2} = 50 MHz, IMD3 = 99 dBFS, each tone at –7 dBFS

Figure 77. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

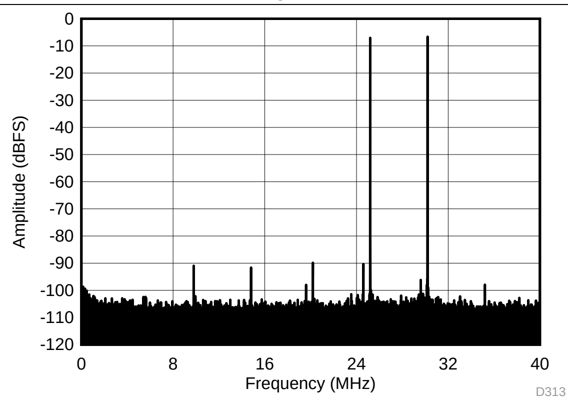


f_{IN1} = 46 MHz, f_{IN2} = 50 MHz, IMD3 = 105 dBFS, each tone at –36 dBFS

Figure 78. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

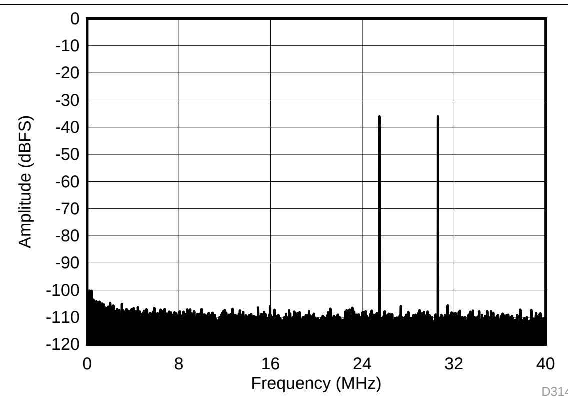
Typical Characteristics: ADC3443 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, IMD3 = 90 dBFS, each tone at –7 dBFS

Figure 79. FFT FOR Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, IMD3 = 106 dBFS, each tone at –36 dBFS

Figure 80. FFT FOR Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

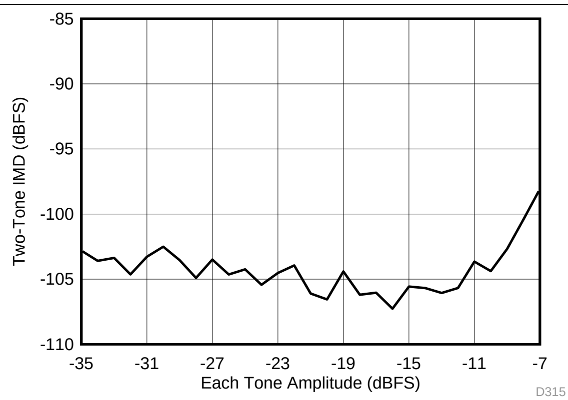


Figure 81. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

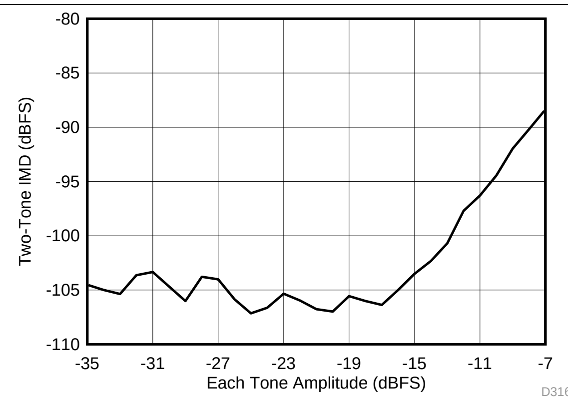


Figure 82. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

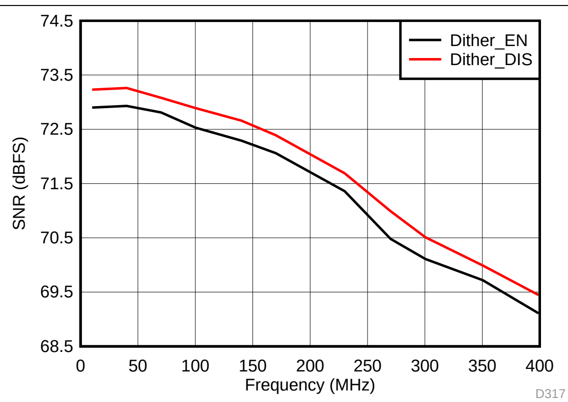


Figure 83. Signal-to-Noise Ratio vs Input Frequency

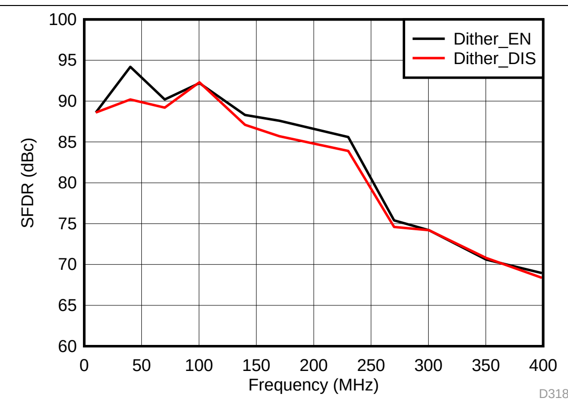


Figure 84. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC3443 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

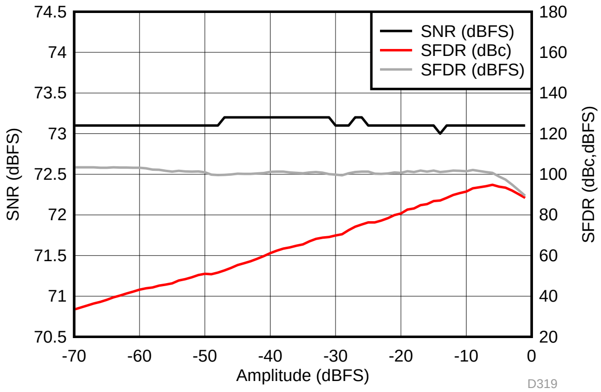


Figure 85. Performance vs Input Amplitude (30 MHz)

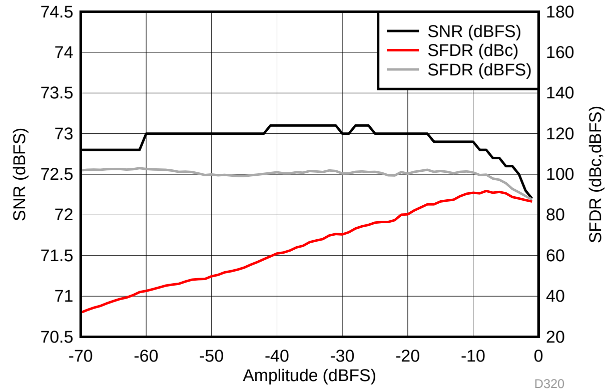


Figure 86. Performance vs Input Amplitude (170 MHz)

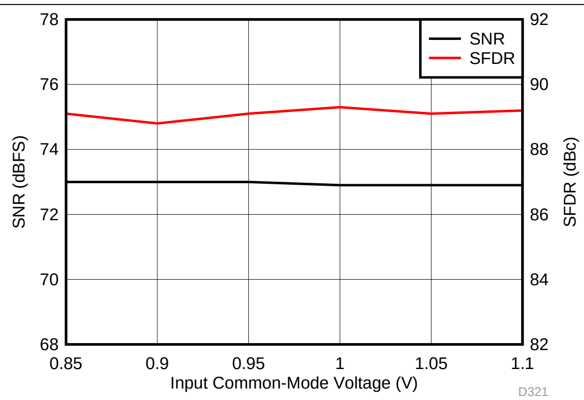


Figure 87. Performance vs Input Common-Mode Voltage (30 MHz)

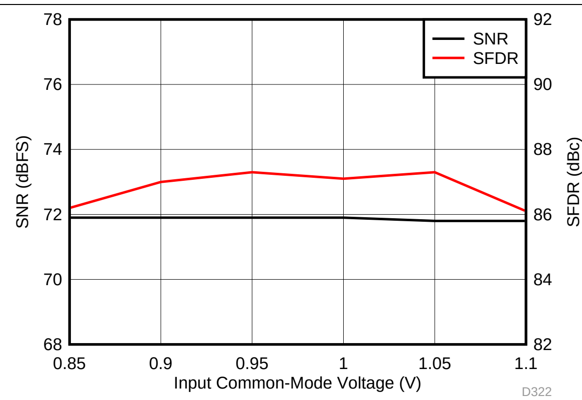


Figure 88. Performance vs Input Common-Mode Voltage (170 MHz)

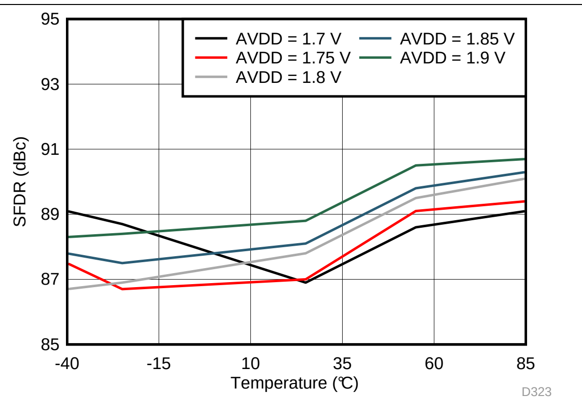


Figure 89. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (170 MHz)

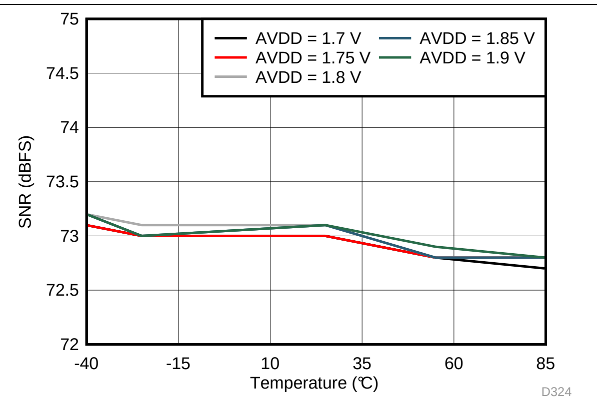


Figure 90. Signal-to-Noise Ratio vs AVDD Supply and Temperature (170 MHz)

Typical Characteristics: ADC3443 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

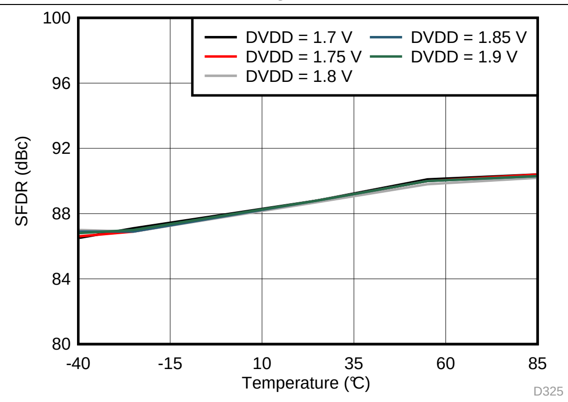


Figure 91. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (170 MHz)

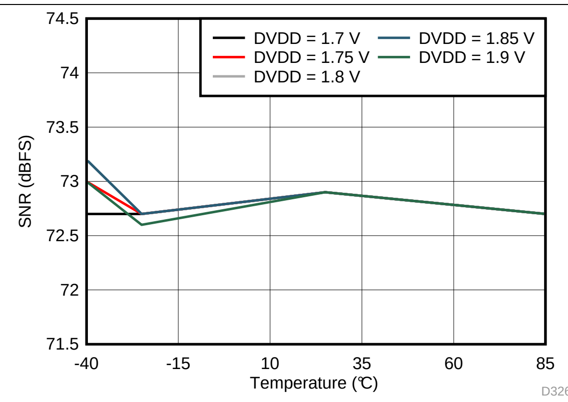


Figure 92. Signal-to-Noise Ratio vs DVDD Supply and Temperature (170 MHz)

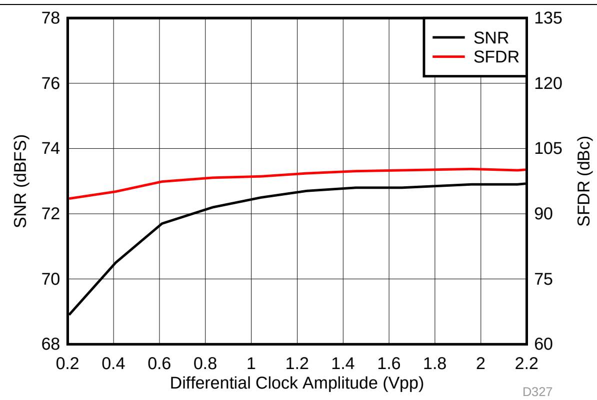


Figure 93. Performance vs Clock Amplitude (40 MHz)

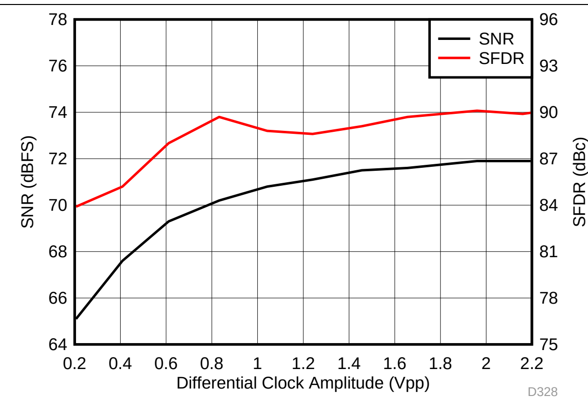


Figure 94. Performance vs Clock Amplitude (150 MHz)

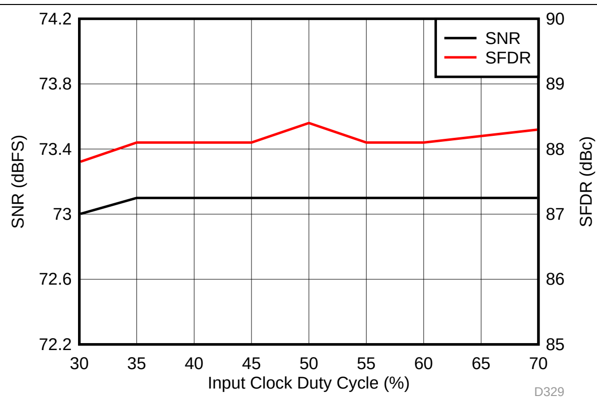


Figure 95. Performance vs Clock Duty cycle (30 MHz)

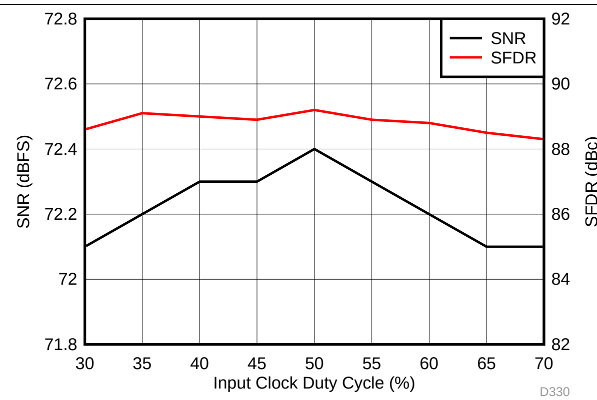
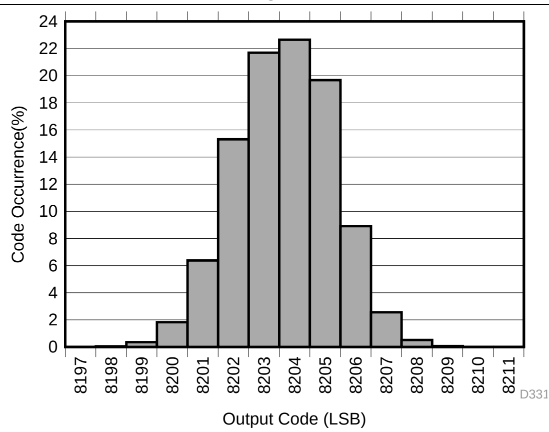


Figure 96. Performance vs Clock Duty Cycle (150 MHz)

Typical Characteristics: ADC3443 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



RMS noise = 1.28 LSBs

Figure 97. Idle Channel Histogram

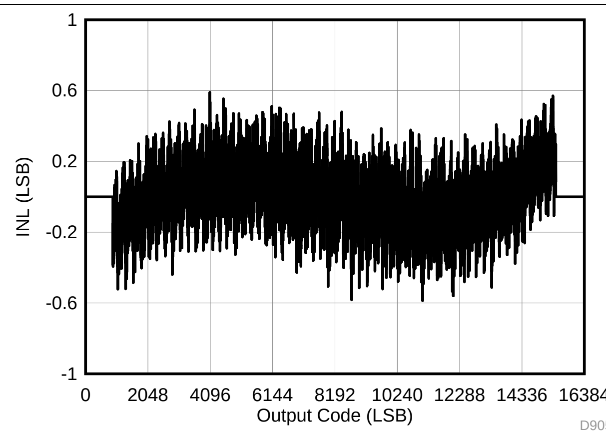


Figure 98. Integral Nonlinearity for 70-MHz Input

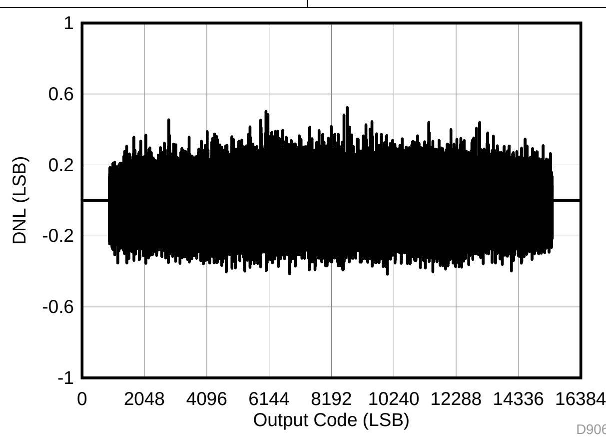
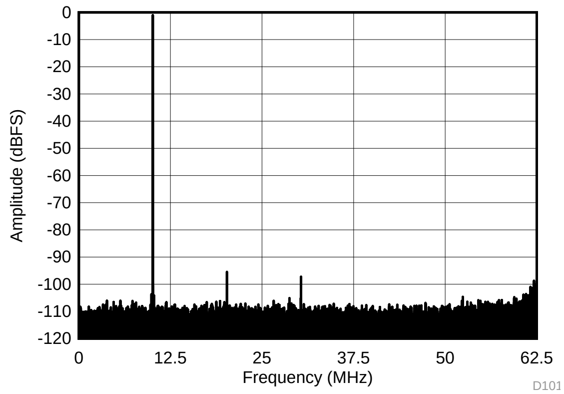


Figure 99. Differential Nonlinearity for 70-MHz Input

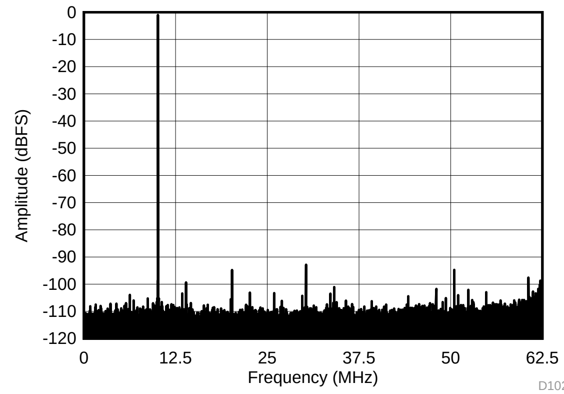
7.18 Typical Characteristics: ADC3444

typical values are at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



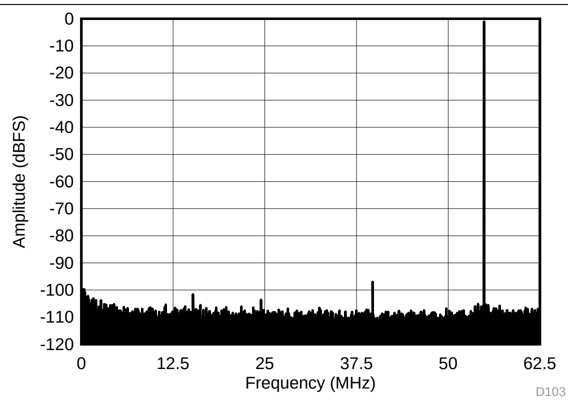
SFDR = 95 dBc, SNR = 72.7 dBFS, SINAD = 72.6 dBFS,
THD = 100 dBc, HD2 = 95 dBc, HD3 = 96 dBc

Figure 100. FFT for 10-MHz Input Signal (Chopper On, Dither On)



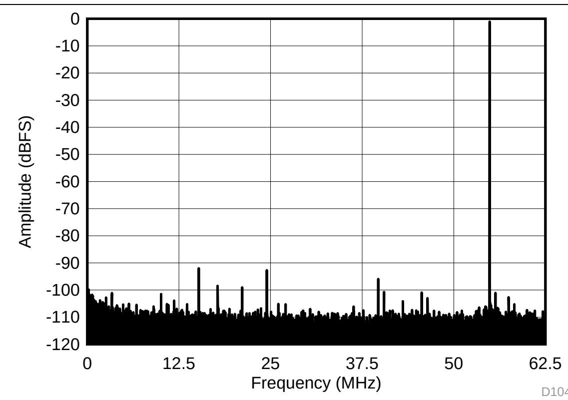
SFDR = 91.8 dBc, SNR = 73.1 dBFS, SINAD = 73 dBFS,
THD = 87 dBc, HD2 = 94 dBc, HD3 = 92 dBc

Figure 101. FFT for 10-MHz Input Signal (Chopper On, Dither Off)



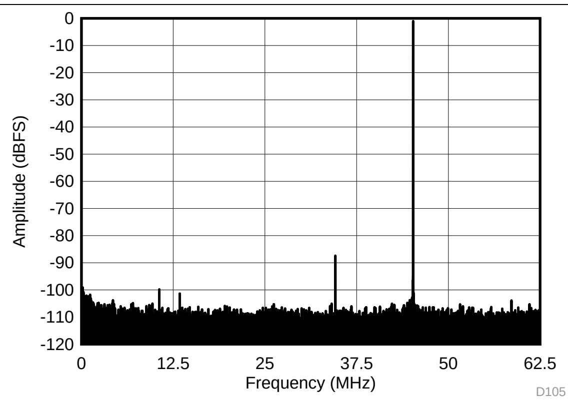
SFDR = 96 dBc, SNR = 72.5 dBFS, SINAD = 72.4 dBFS,
THD = 94 dBc, HD2 = 101 dBc, HD3 = 96 dBc

Figure 102. FFT for 70-MHz Input Signal (Dither On)



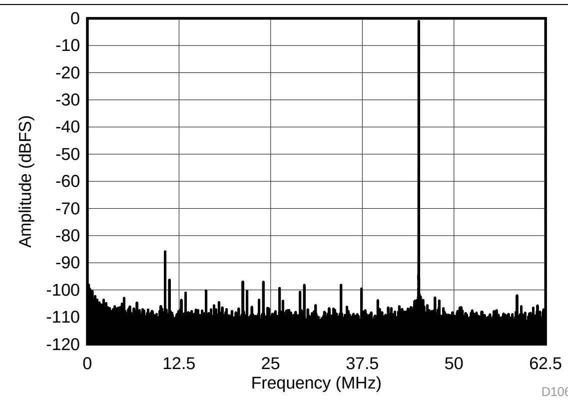
SFDR = 91 dBc, SNR = 73 dBFS, SINAD = 72.8 dBFS,
THD = 87 dBc, HD2 = 91 dBc, HD3 = 95 dBc

Figure 103. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 86 dBc, SNR = 71.7 dBFS, SINAD = 71.6 dBFS,
THD = 93 dBc, HD2 = 86 dBc, HD3 = 99 dBc

Figure 104. FFT for 170-MHz Input Signal (Dither On)

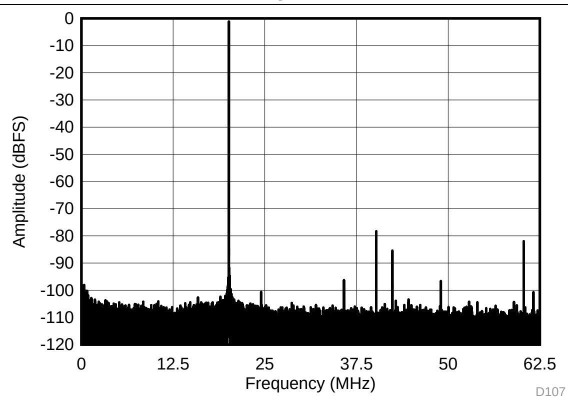


SFDR = 85 dBc, SNR = 72.3 dBFS, SINAD = 72.1 dBFS,
THD = 87 dBc, HD2 = 97 dBc, HD3 = 85 dBc

Figure 105. FFT for 170-MHz Input Signal (Dither Off)

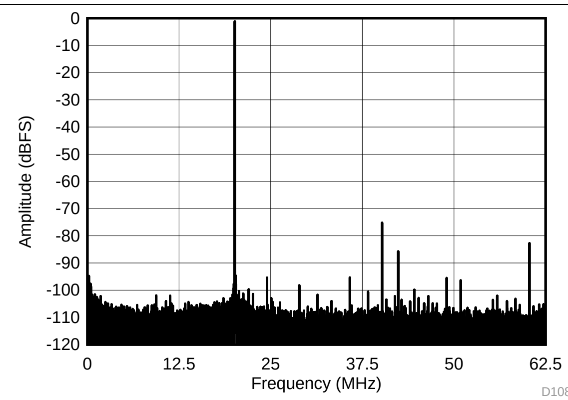
Typical Characteristics: ADC3444 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



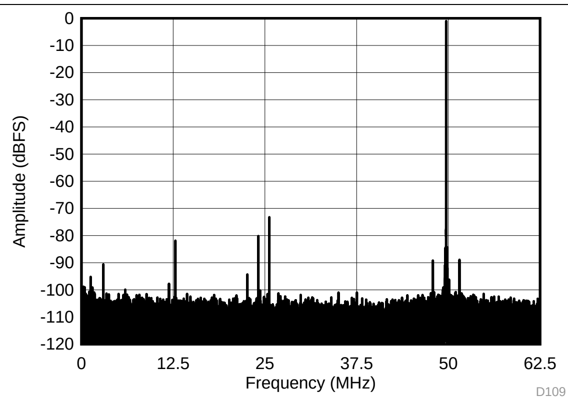
SFDR = 77 dBc, SNR = 70.4 dBFS, SINAD = 69.6 dBFS, THD = 75 dBc, HD2 = 77 dBc, HD3 = 81 dBc

Figure 106. FFT for 270-MHz Input Signal (Dither On)



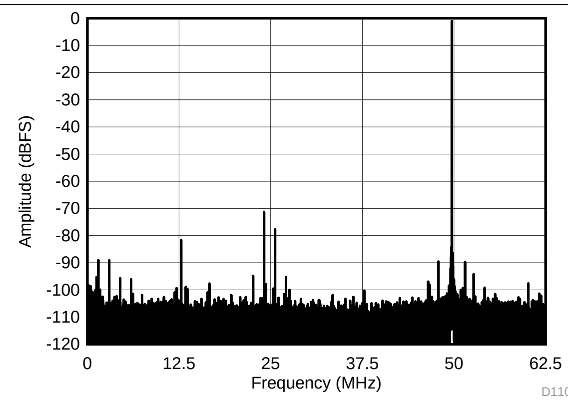
SFDR = 74 dBc, SNR = 71 dBFS, SINAD = 70.1 dBFS, THD = 75 dBc, HD2 = 76 dBc, HD3 = 82 dBc

Figure 107. FFT for 270-MHz Input Signal (Dither Off)



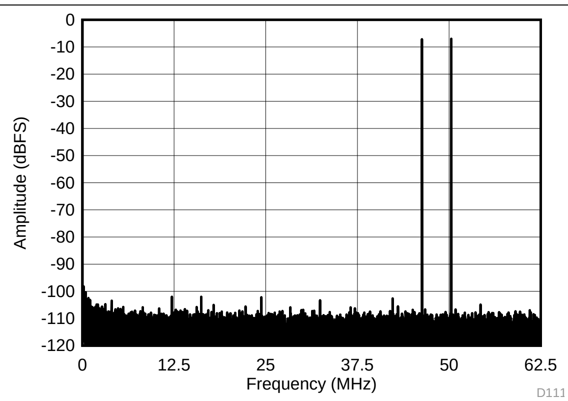
SFDR = 72 dBc, SNR = 68.2 dBFS, SINAD = 67.3 dBFS, THD = 74 dBc, HD2 = 72 dBc, HD3 = 79 dBc

Figure 108. FFT for 450-MHz Input Signal (Dither On)



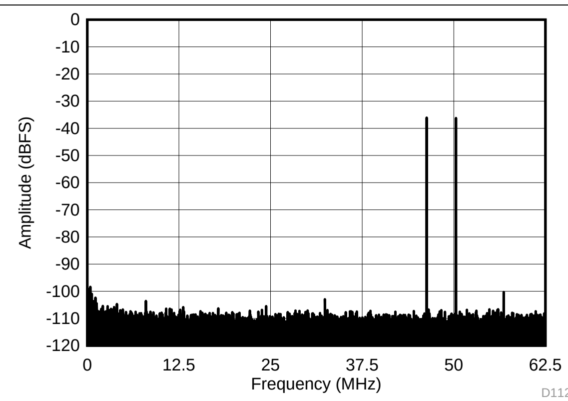
SFDR = 70 dBc, SNR = 68.9 dBFS, SINAD = 67.6 dBFS, THD = 73 dBc, HD2 = 77 dBc, HD3 = 70 dBc

Figure 109. FFT for 450-MHz Input Signal (Dither Off)



f_{IN1} = 46 MHz, f_{IN2} = 50 MHz, IMD3 = 102 dBFS, each tone at –7 dBFS

Figure 110. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

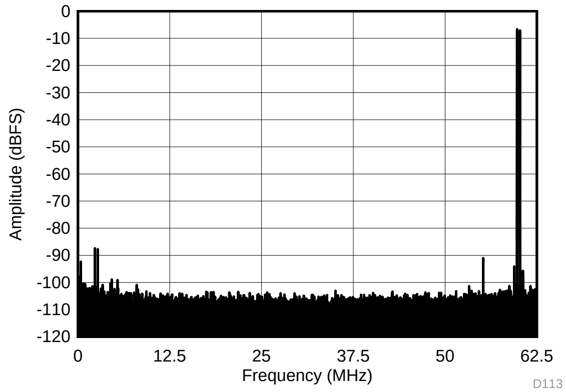


f_{IN1} = 46 MHz, f_{IN2} = 50 MHz, IMD3 = 100 dBFS, each tone at –36 dBFS

Figure 111. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

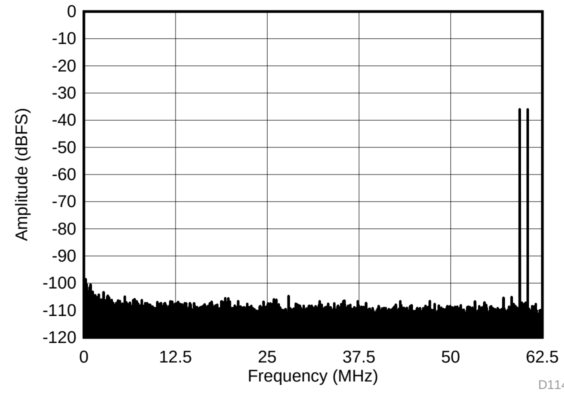
Typical Characteristics: ADC3444 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, IMD3 = 88 dBFS, each tone at –7 dBFS

Figure 112. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, IMD3 = 104 dBFS, each tone at –36 dBFS

Figure 113. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

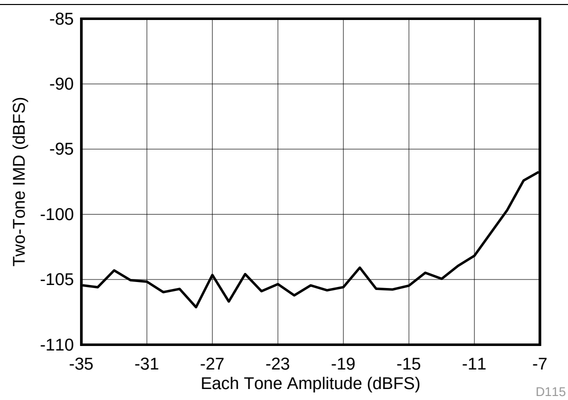


Figure 114. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

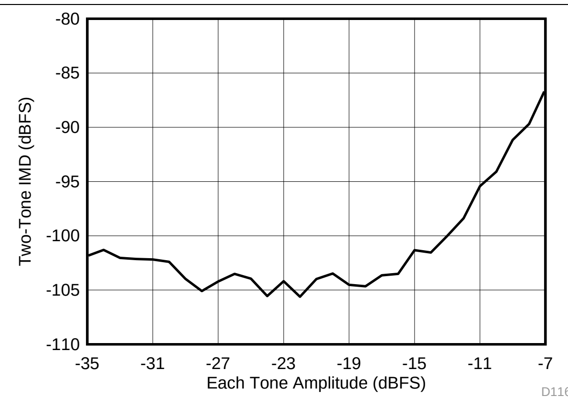


Figure 115. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

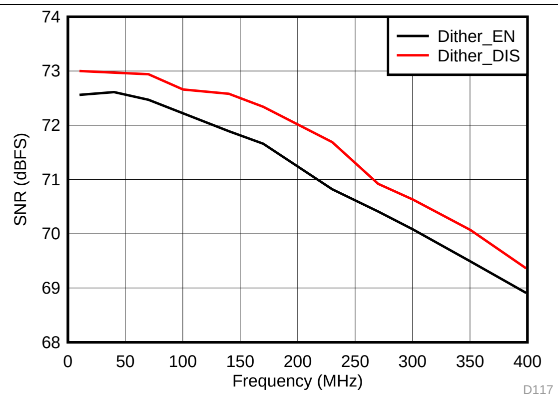


Figure 116. Signal-to-Noise Ratio vs Input Frequency

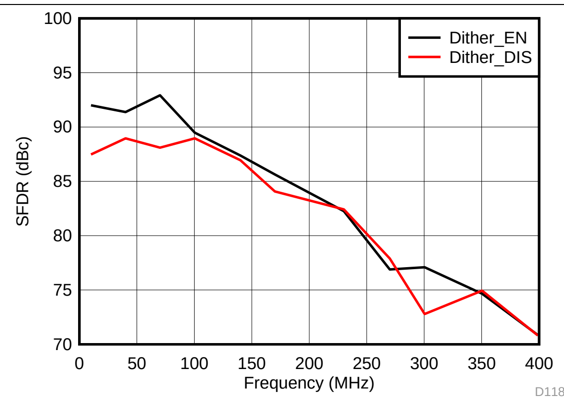


Figure 117. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC3444 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

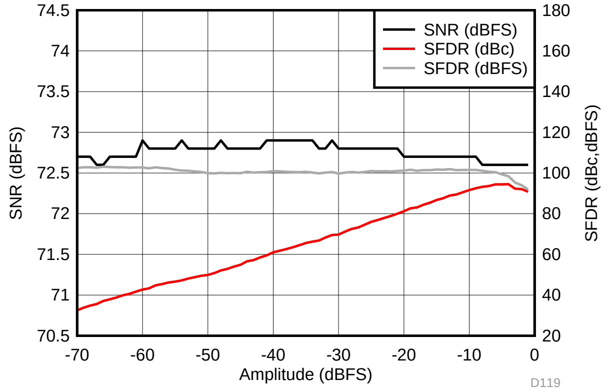


Figure 118. Performance vs Input Amplitude (30 MHz)

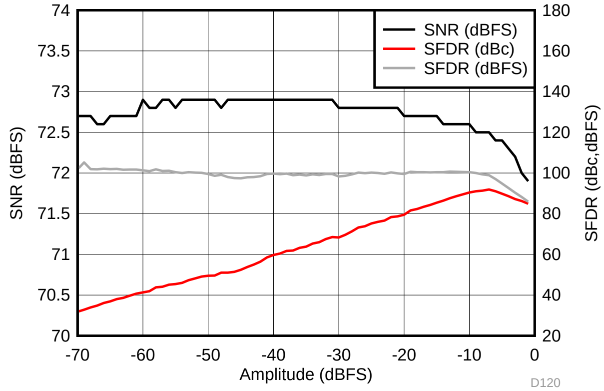


Figure 119. Performance vs Input Amplitude (170 MHz)

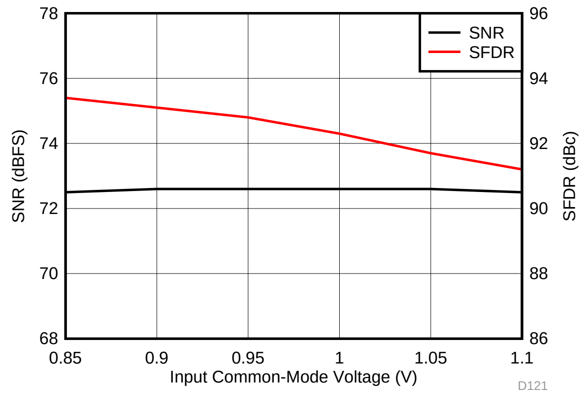


Figure 120. Performance vs Input Common-Mode Voltage (30 MHz)

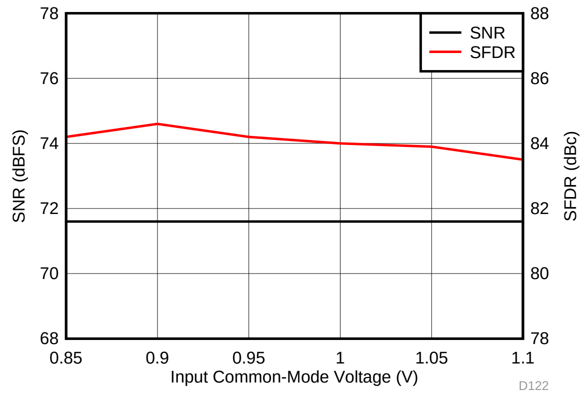


Figure 121. Performance vs Input Common-Mode Voltage (170 MHz)

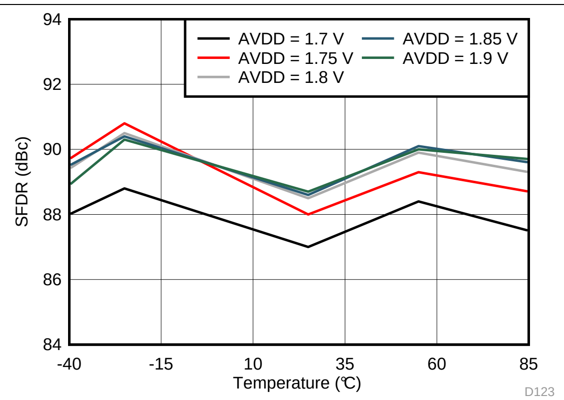


Figure 122. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (170 MHz)

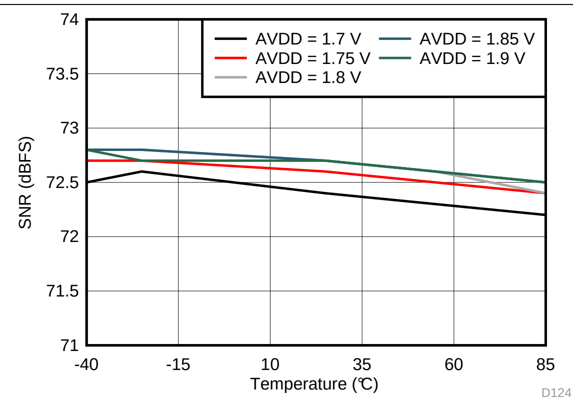


Figure 123. Signal-to-Noise Ratio vs AVDD Supply and Temperature (170 MHz)

Typical Characteristics: ADC3444 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

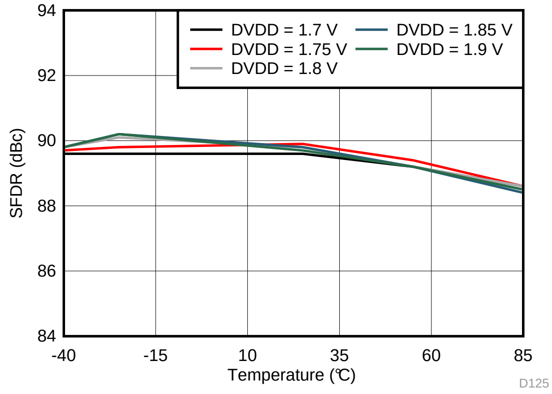


Figure 124. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (170 MHz)

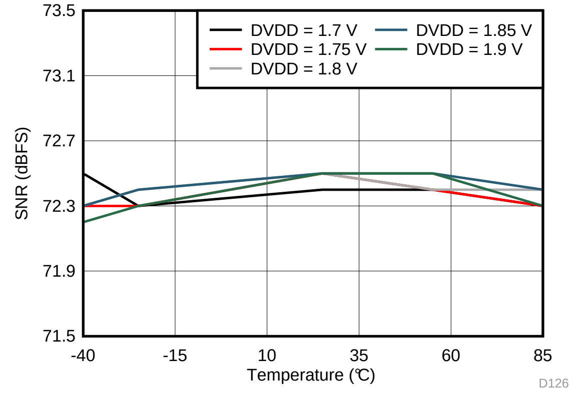


Figure 125. Signal-to-Noise Ratio vs DVDD Supply and Temperature (170 MHz)

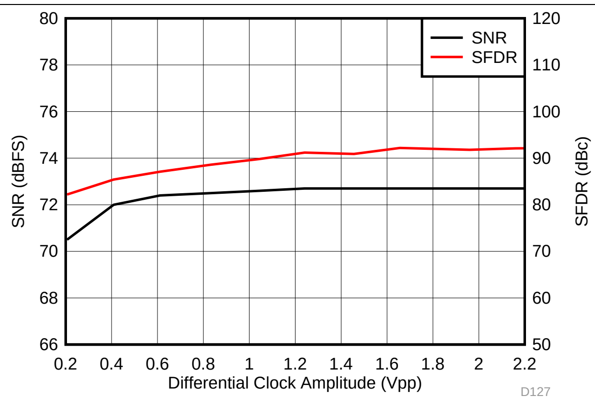


Figure 126. Performance vs Clock Amplitude (40 MHz)

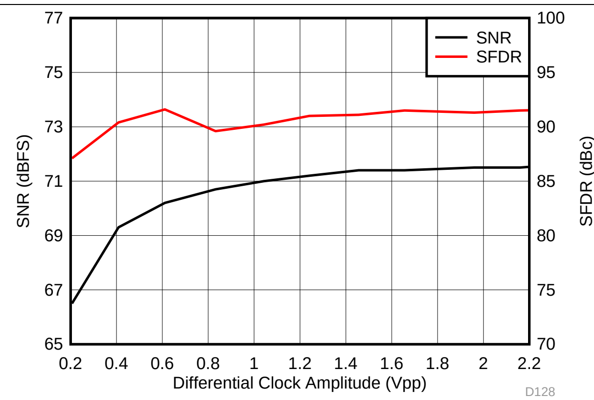


Figure 127. Performance vs Clock Amplitude (150 MHz)

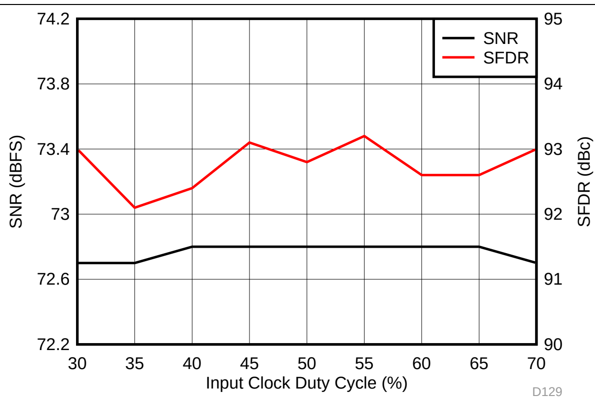


Figure 128. Performance vs Clock Duty Cycle (30 MHz)

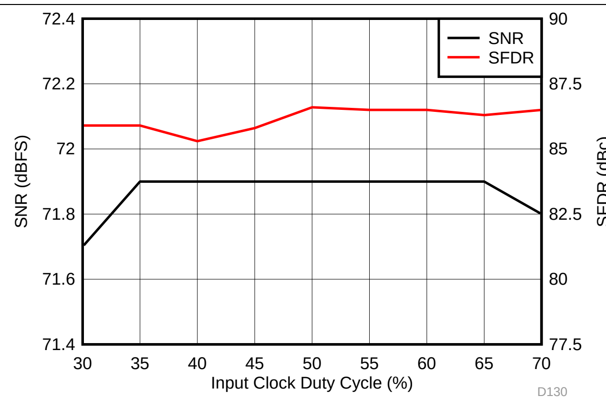


Figure 129. Performance vs Clock Duty Cycle (150 MHz)

Typical Characteristics: ADC3444 (continued)

typical values are at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)

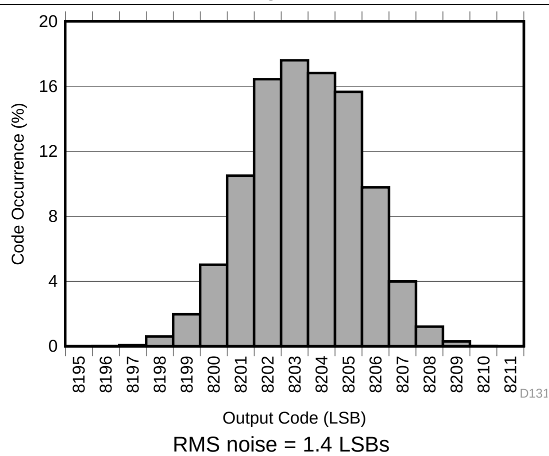


Figure 130. Idle Channel Histogram

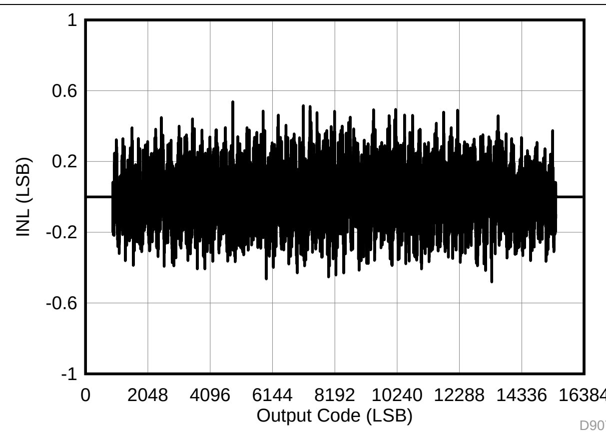


Figure 131. Integral Nonlinearity for 70-MHz Input

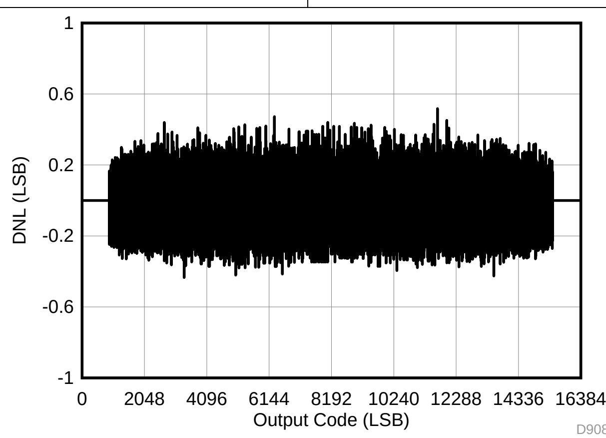
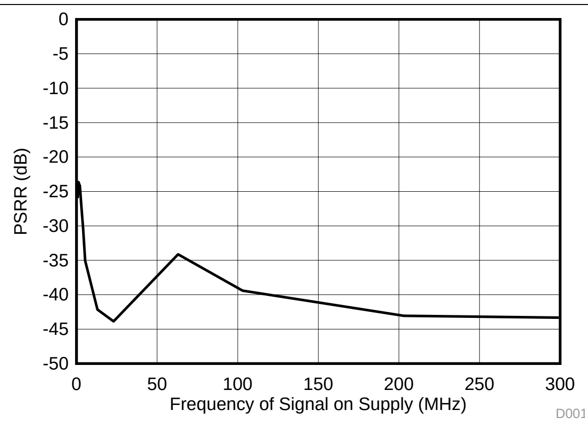


Figure 132. Differential Nonlinearity for 70-MHz Input

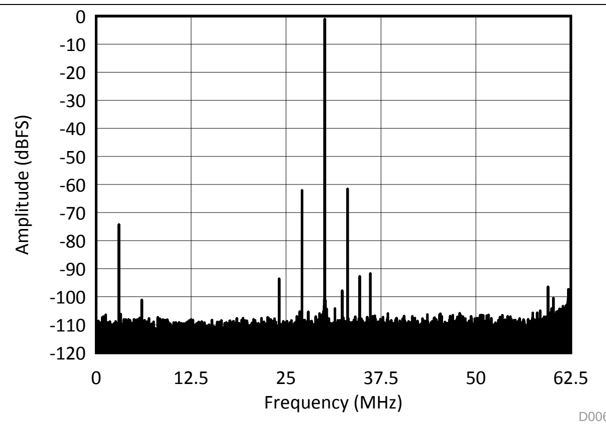
7.19 Typical Characteristics: Common

typical values are at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled, and dither on (unless otherwise noted)



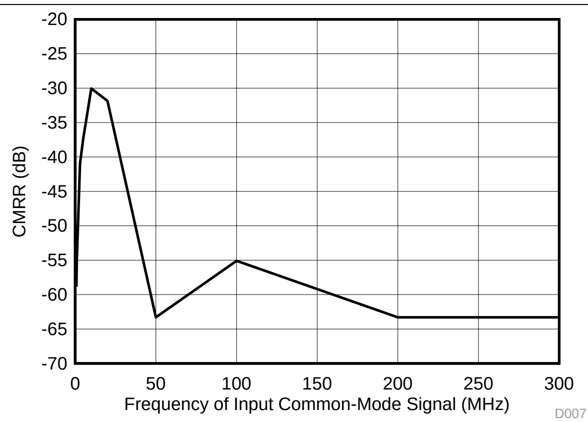
f_{IN} = 30 MHz, A_{IN} = –1 dBFS,
test signal amplitude = 50 mV_{PP}

Figure 133. Power-Supply Rejection Ratio vs Test Signal Frequency



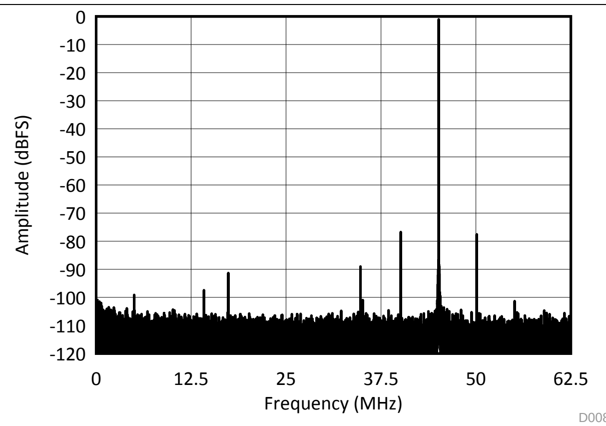
f_{IN} = 30.1 MHz, f_{PSRR} = 3 MHz, A_{PSRR} = 50 mV_{PP},
SINAD = 58.63 dBFS, SFDR = 61.57 dBc

Figure 134. Power-Supply Rejection Ratio Spectrum (Chopper On)



f_{IN} = 170 MHz, A_{IN} = –1 dBFS,
test signal amplitude = 50 mV_{PP}, input VCM = 0.95 V

Figure 135. Common-Mode Rejection Ratio vs Test Signal Frequency



f_{IN} = 170.1 MHz, f_{CMRR} = 5 MHz, A_{CMRR} = 50 mV_{PP},
SINAD = 69.66 dBFS, SFDR = 75.66 dBc

Figure 136. Common-Mode Rejection Ratio Spectrum

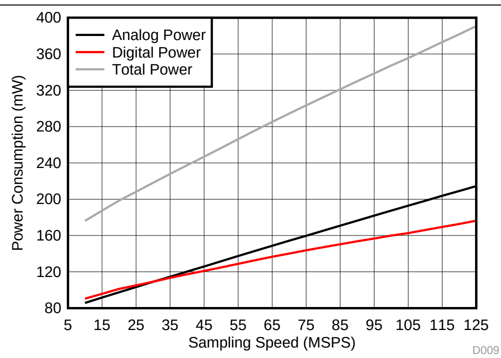


Figure 137. Power vs Sampling Frequency (Two-Wire Mode)

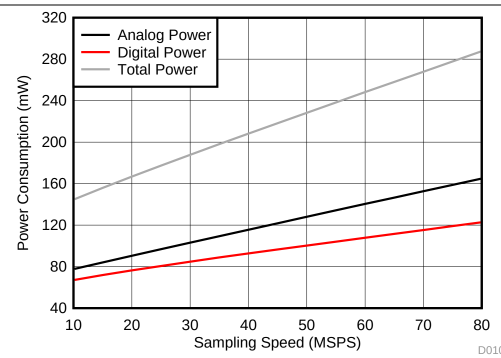


Figure 138. Power vs Sampling Frequency (One-Wire Mode)

7.20 Typical Characteristics: Contour

typical values are at T_A = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when is chopper enabled, and dither on (unless otherwise noted)

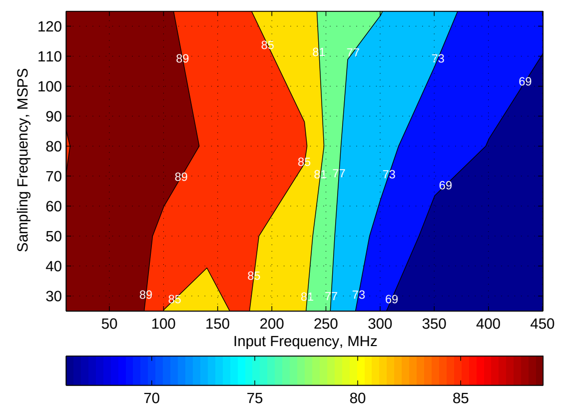


Figure 139. Spurious-Free Dynamic Range (SFDR)

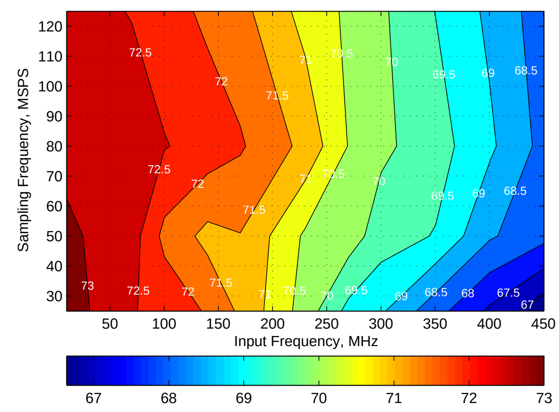


Figure 140. Signal-to-Noise Ratio (SNR)

8 Parameter Measurement Information

8.1 Timing Diagrams

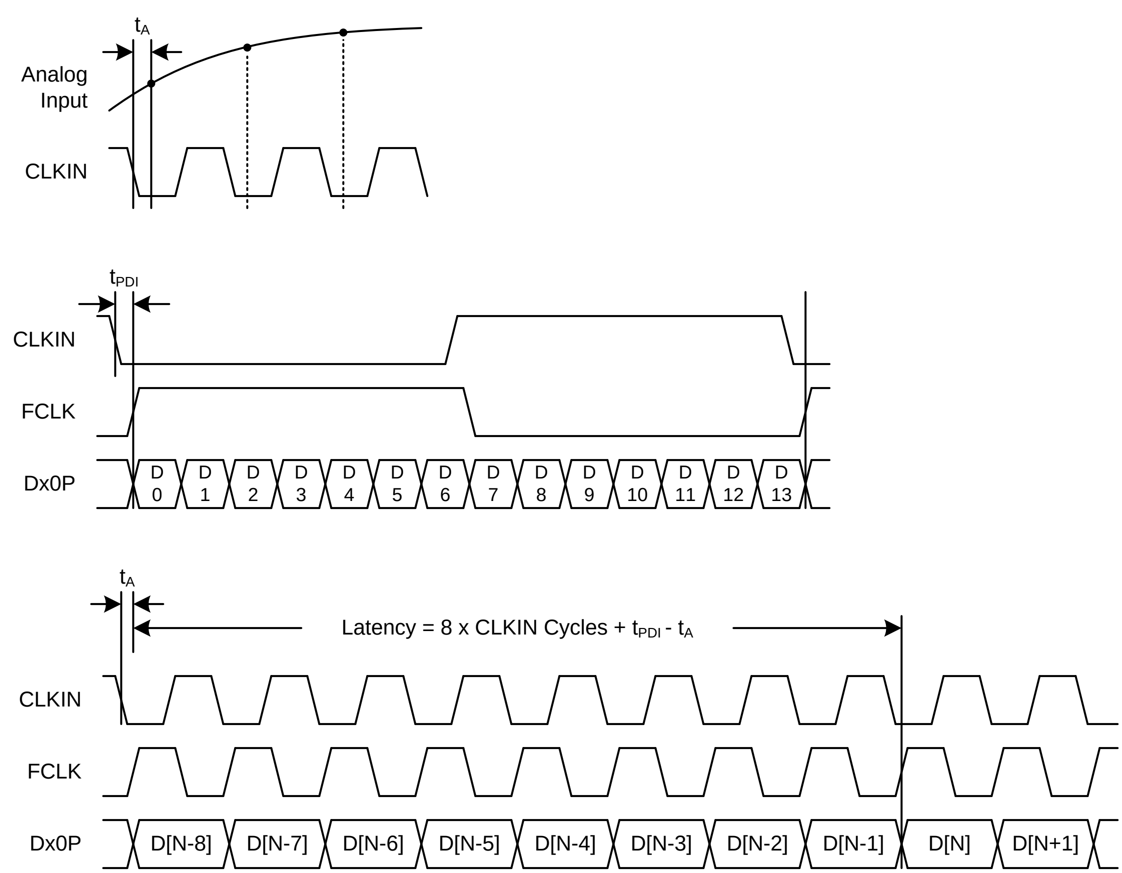
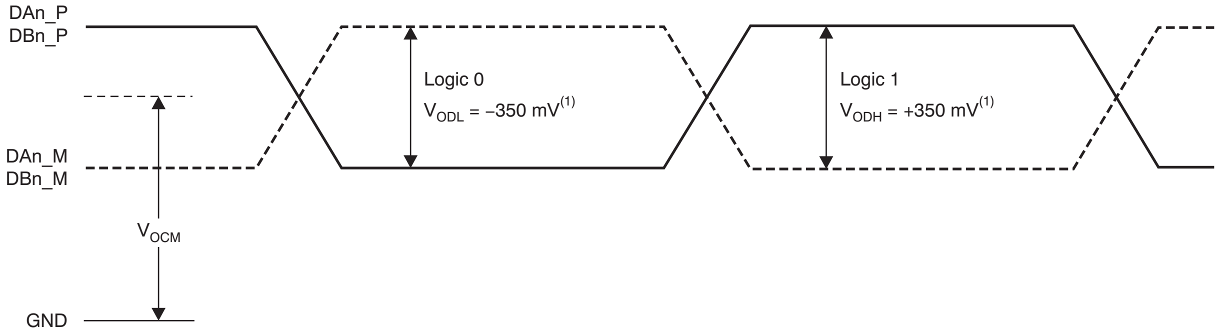


Figure 141. Latency Timing Diagram

Timing Diagrams (continued)



(1) With an external 100-Ω termination.

Figure 142. Serial LVDS Output Voltage Levels

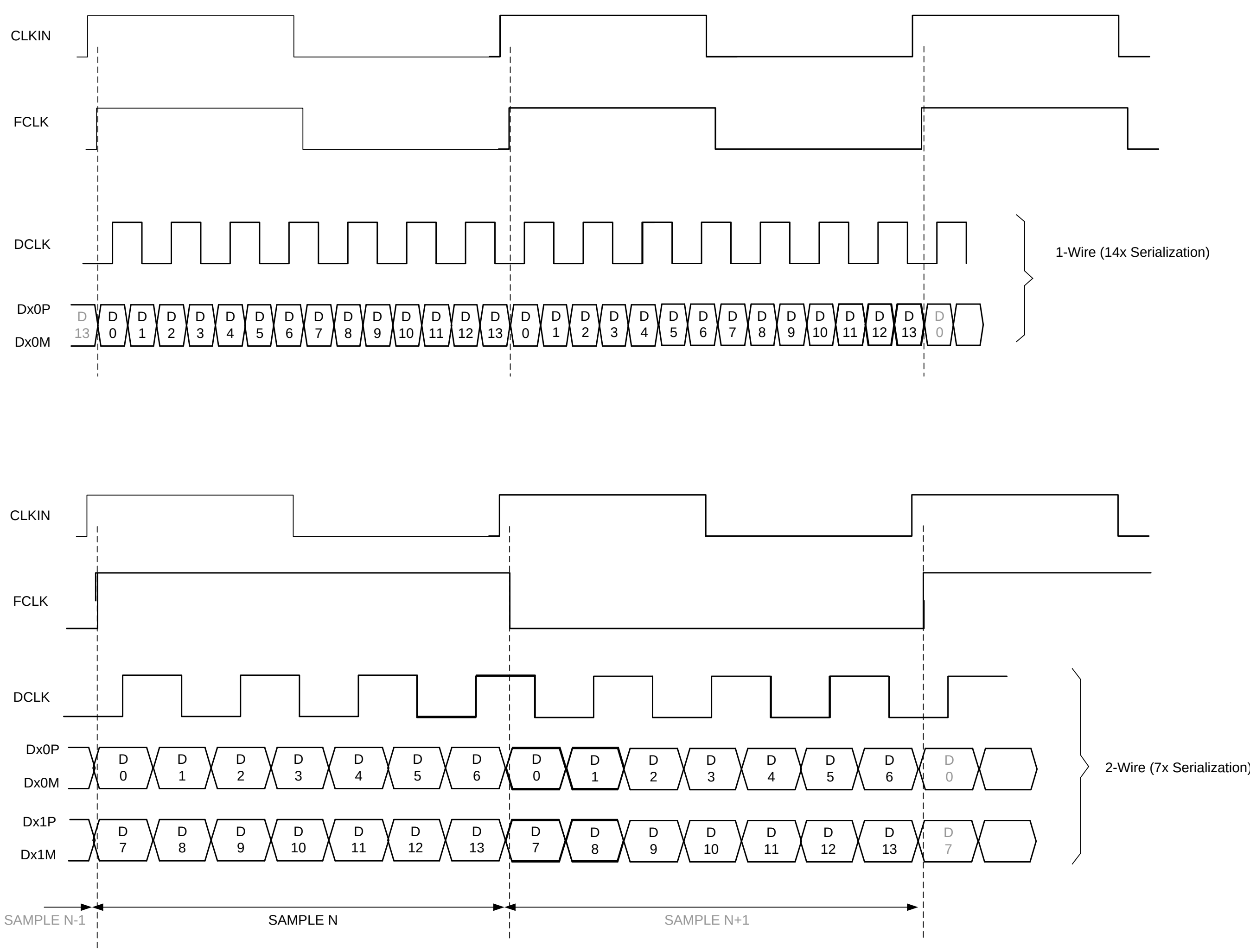


Figure 143. Output Timing Diagram

Timing Diagrams (continued)

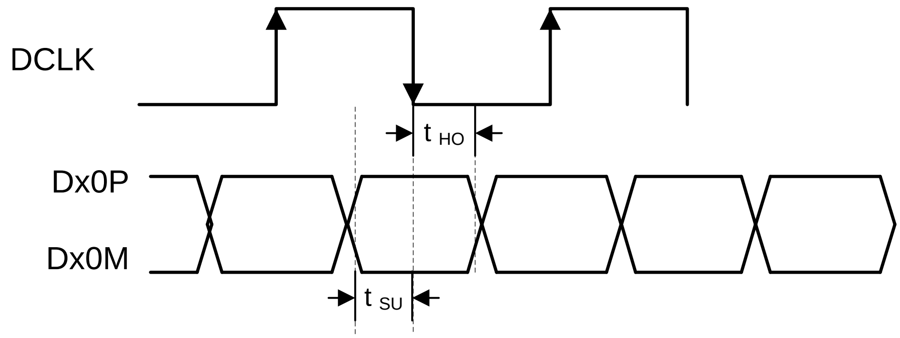


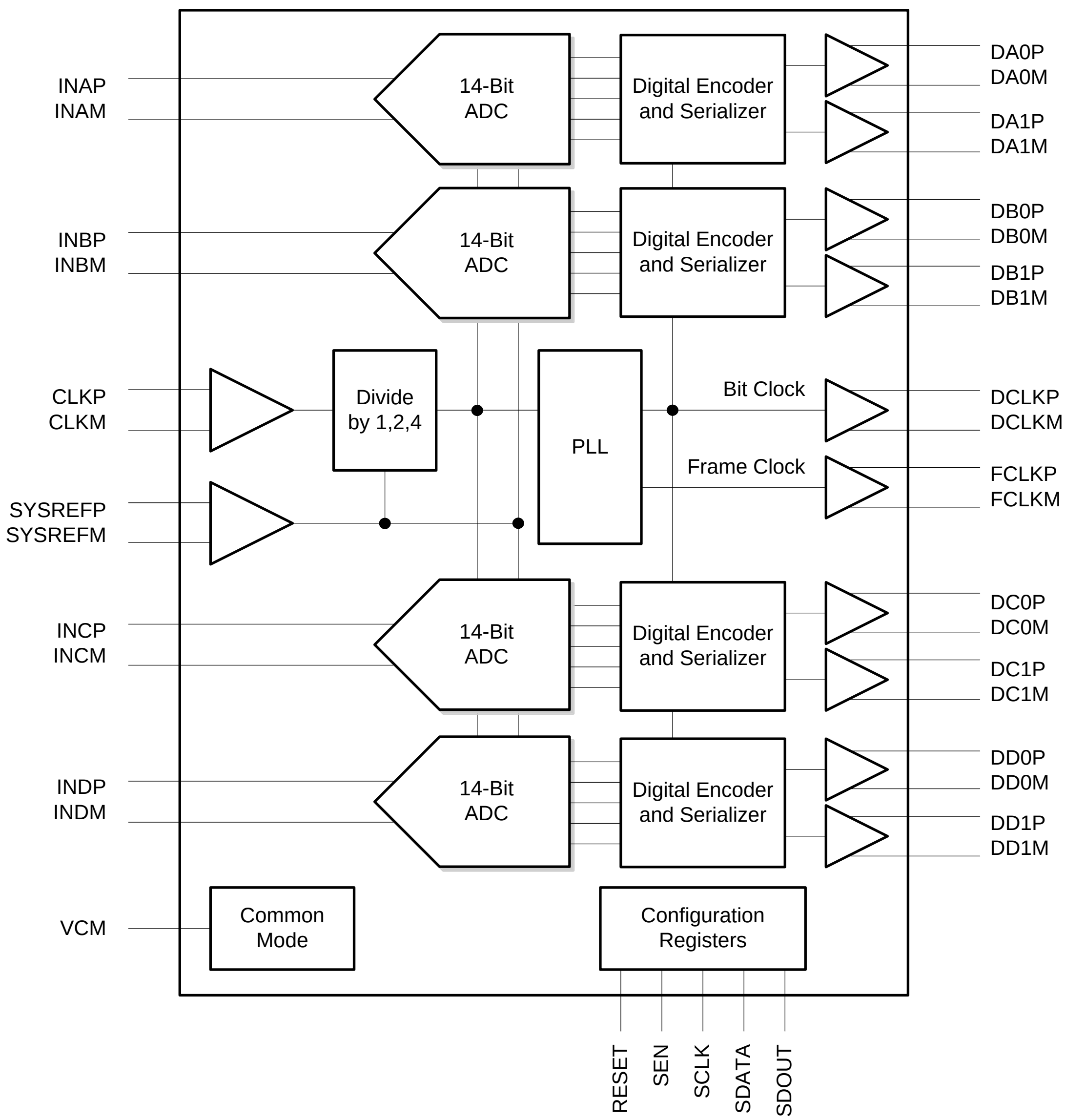
Figure 144. Setup and Hold Time

9 Detailed Description

9.1 Overview

The ADC344x devices are a high-linearity, ultra-low power, quad-channel, 14-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The ADC344x family supports serial LVDS interface in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 14-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

9.2 Functional Block Diagram



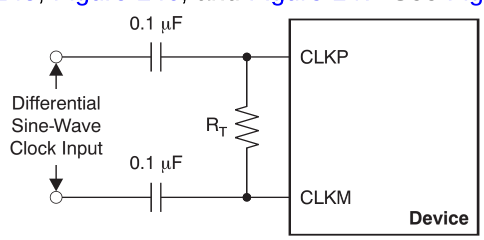
9.3 Feature Description

9.3.1 Analog Inputs

The ADC344x analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 540 MHz (50-Ω source driving 50-Ω termination between INP and INM).

9.3.2 Clock Input

The device clock inputs may be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-kΩ resistors. The ADC344x self-bias clock inputs may be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 145, Figure 146, and Figure 147. See Figure 148 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

Figure 145. Differential Sine-Wave Clock Driving Circuit

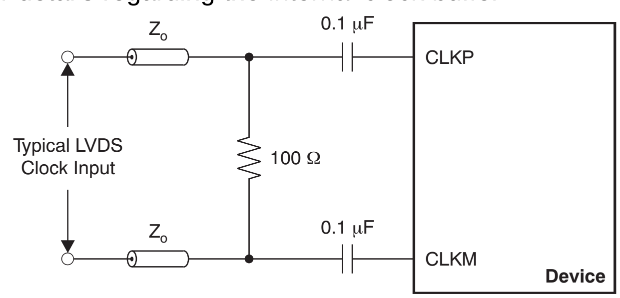


Figure 146. LVDS Clock Driving Circuit

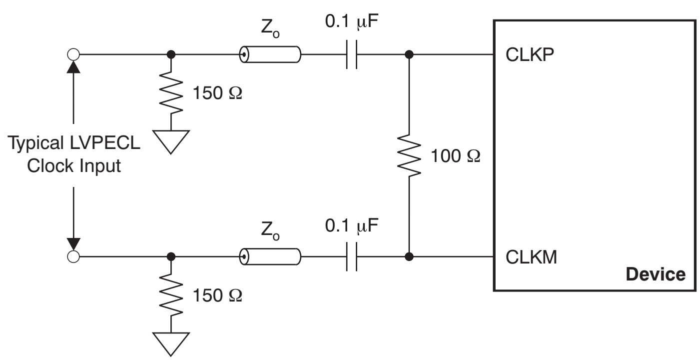
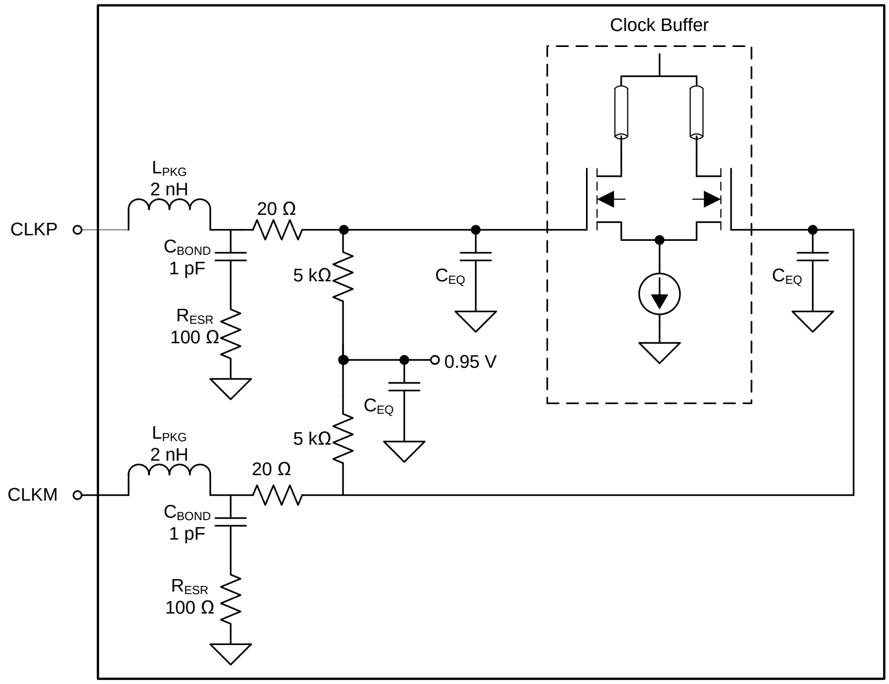


Figure 147. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 148. Internal Clock Buffer

A single-ended CMOS clock may be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 149. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with low jitter. Band-pass filtering of the clock source may help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

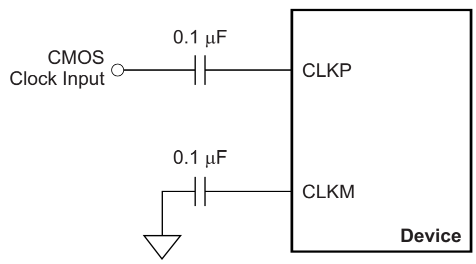


Figure 149. Single-Ended Clock Driving Circuit

9.3.2.1 Using the SYSREF Input

The ADC344x has a SYSREF input pin that can be used when the clock-divider feature is used. A logic low-to-high transition on the SYSREF pin aligns the falling edge of the divided clock with the next falling edge of the input clock, essentially resetting the phase of the divided clock, as shown in Figure 150. When multiple ADC344x devices are onboard and the clock divider option is used, the phase of the divided clock among the devices may not be the same. The phase of the divided clock in each device can be synchronized to the common sampling clock by using the SYSREF pins. SYSREF can applied as mono-shot or periodic waveform. When applied as periodic waveform, its period must be integer multiple of period of the divided clock. When not used, the SYSREFP and SYSREFM pins can be connected to AVDD and GND, respectively. Alternatively, the SYSREF buffer inside the device can be powered down using the PDN SYSREF register bit.

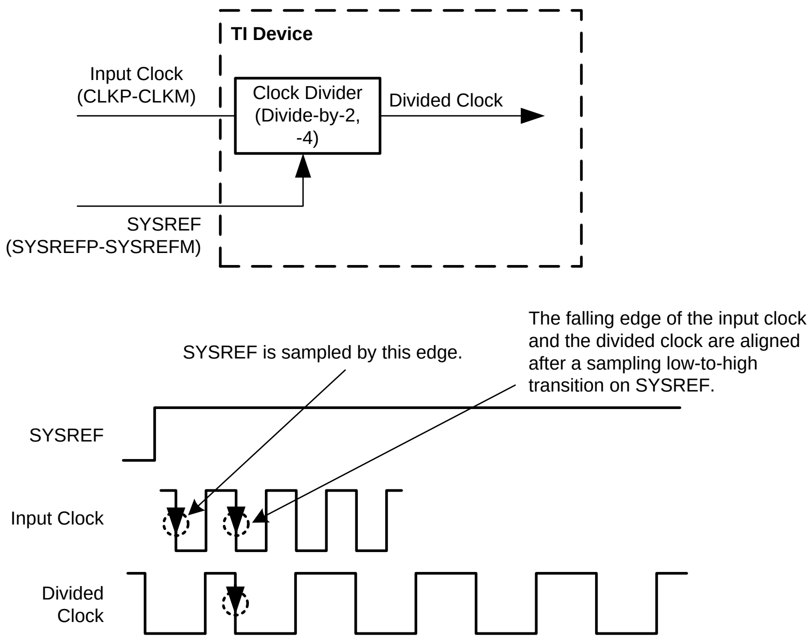


Figure 150. Using SYSREF for Synchronization

9.3.2.2 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors, as shown in Equation 1. Quantization noise (typically 86 dB for a 14-bit ADC) and thermal noise limit SNR at low input frequencies while the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{-\frac{SNR_{Quantizatoin\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ \ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation resulting from sample clock jitter may be calculated with Equation 2.

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter}) \quad (2)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (130 fs for the device) which is set by the noise of the clock input buffer and the external clock. T_{Jitter} may be calculated with Equation 3.

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (3)$$

External clock jitter may be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter. The devices have a typical thermal noise of 72.7 dBFS and internal aperture jitter of 130 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 151.

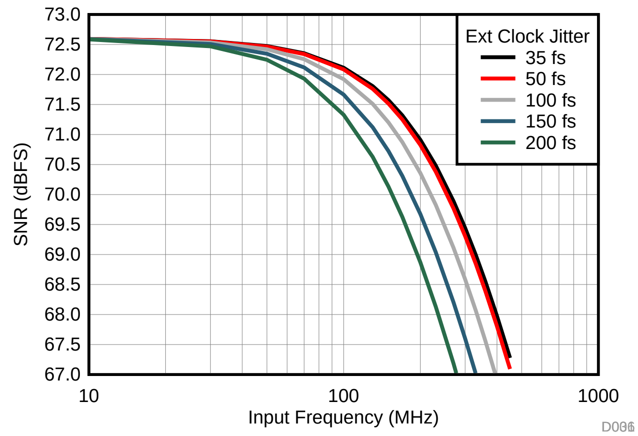


Figure 151. SNR vs Frequency for Different Clock Jitter

9.3.3 Digital Output Interface

The devices offer two different output format options, thus making interfacing to a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) easy. Each option may be easily programmed using the serial interface, as shown in Table 3. The output interface options are:

- One-wire, 1x frame clock, 14x serialization with the DDR bit clock
- Two-wire, 1x frame clock, 7x serialization with the DDR bit clock.

Table 3. Interface Rates

INTERFACE OPTIONS	SERIALIZATION	RECOMMENDED SAMPLING FREQUENCY (MSPS)		BIT CLOCK FREQUENCY (MHz)	FRAME CLOCK FREQUENCY (MHz)	SERIAL DATA RATE (Mbps)
		MINIMUM	MAXIMUM			
1-wire	14x	15 (1)	—	105	15	210
		—	80	560	80	1120
2-wire (default after reset)	7x	20 (1)	—	70	10	140
		—	125	437.5	62.5	875

(1) Use the LOW SPEED ENABLE register bits for low speed operation; see Table 20.

9.3.3.1 One-Wire Interface: 14x Serialization

In this interface option, the device outputs the data of each ADC serially on a single LVDS pair (one-wire). The data are available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the LSB. The data rate is 14x sample frequency (14x serialization).

9.3.3.2 Two-Wire Interface: 7x Serialization

The two-wire interface is recommended for sampling frequencies above 65 MSPS. The output data rate is 7x sample frequency because seven data bits are output every clock cycle on each differential pair. Each ADC sample is sent over the two wires with the seven MSBs on Dx1P, Dx1M and the seven LSBs on Dx0P, Dx0M, as shown in Figure 152.

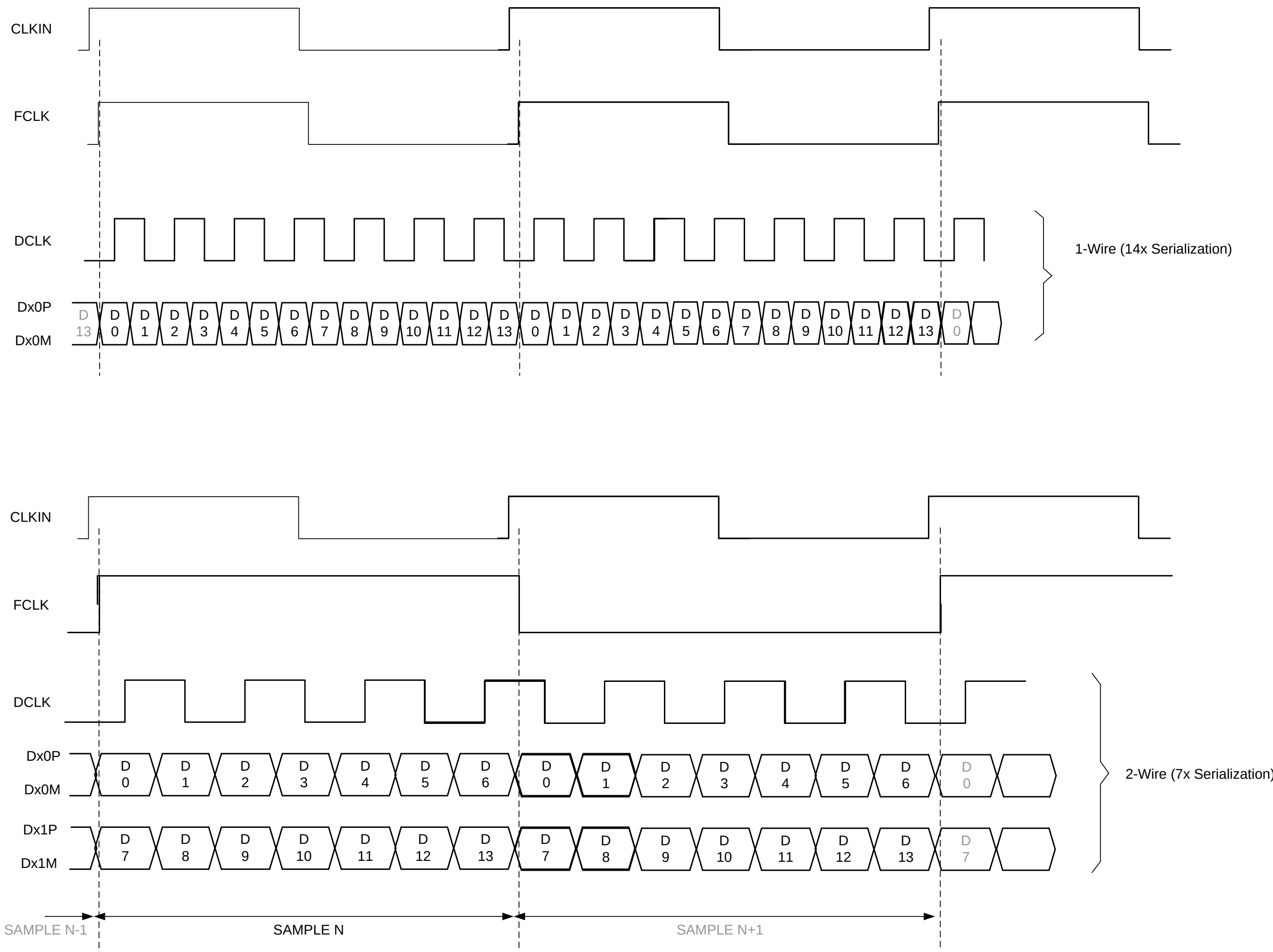


Figure 152. Output Timing Diagram

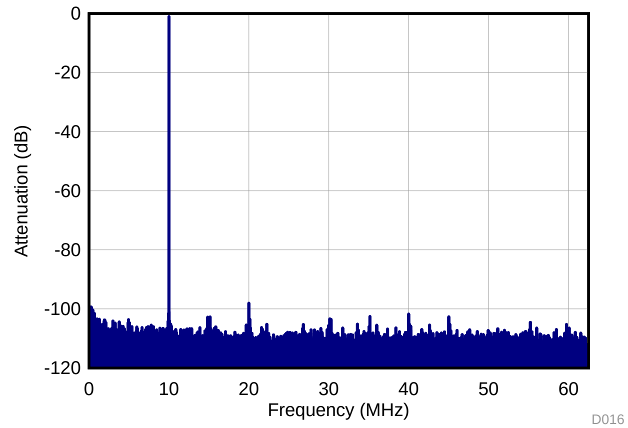
9.4 Device Functional Modes

9.4.1 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The clock divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider may be bypassed for operation with a 125-MHz clock while the divide-by-2 option supports a maximum input clock of 250 MHz and the divide-by-4 option provides a maximum input clock frequency of 500 MHz.

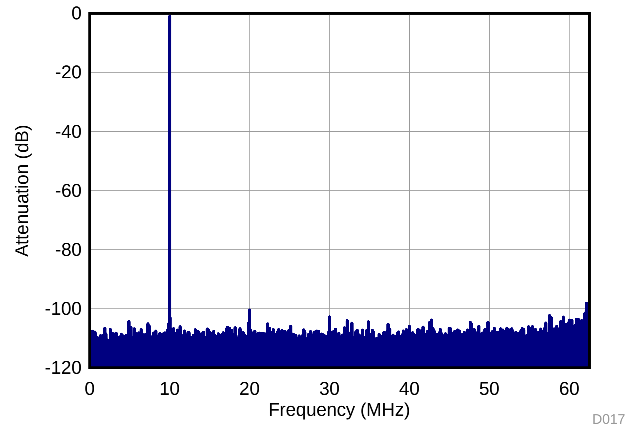
9.4.2 Chopper Functionality

The devices are equipped with an internal chopper front-end. Enabling the chopper function swaps the ADC noise spectrum by shifting the 1/f noise from dc to f_S / 2. Figure 153 shows the noise spectrum with the chopper off and Figure 154 shows the noise spectrum with the chopper on. This function is especially useful in applications requiring good ac performance at low input frequencies or in dc-coupled applications. The chopper may be enabled through SPI register writes and is recommended for input frequencies below 30 MHz. The chopper function creates a spur at f_S / 2 that must be filtered out digitally.



f_S = 125 MSPS, SNR = 72.7 dBFS,
f_{IN} = 10 MHz, SFDR = 94 dBc

Figure 153. Chopper Off



f_S = 125 MSPS, SNR = 72.7 dBFS,
f_{IN} = 10 MHz, SFDR = 94 dBc

Figure 154. Chopper On

9.4.3 Power-Down Control

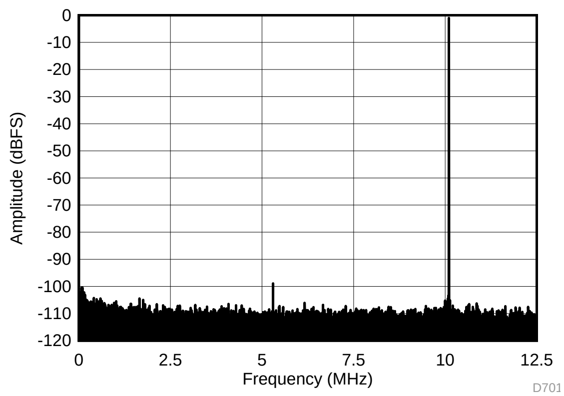
The ADC344x power-down functions may be controlled either through the parallel control pin (PDN) or through an SPI register setting (see register 15h). The PDN pin may also be configured through SPI to a global power-down or standby functionality, as shown in Table 4.

Table 4. Power-Down Modes

FUNCTION	POWER CONSUMPTION (mW)	WAKE-UP TIME (µs)
Global power-down	5	85
Standby	45	35

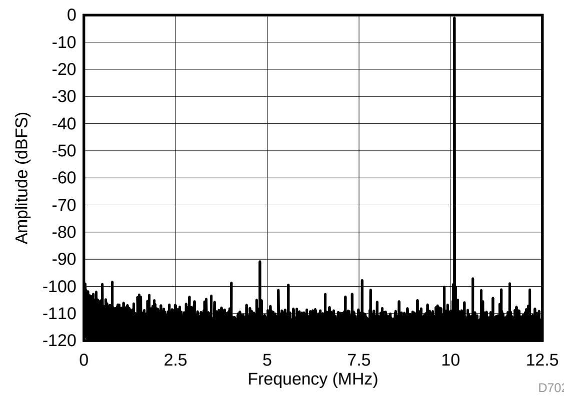
9.4.4 Internal Dither Algorithm

The ADC344x family uses an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm may be turned off by using the DIS DITH CHx registers bits. Figure 155 and Figure 156 show the effect of using dither algorithms.



SFDR = 98 dBc, SNR = 73.1 dBFS, SINAD = 73 dBFS,
THD = 97 dBc, HD2 = 110.0 dBc,
HD3 = 98 dBc, SFDR = 100 dBc (excluding HD2, HD3)

Figure 155. FFT for 10-MHz Input Signal (Dither On)



SFDR = 90 dBc, SNR = 73.5 dBFS, SINAD = 73.2 dBFS,
THD = 88 dBc, HD2 = 90 dBc,
HD3 = 100 dBc, SFDR = 92 dBc (excluding HD2, HD3)

Figure 156. FFT for 10-MHz Input Signal (Dither Off)

9.4.5 Summary of Performance Mode Registers

Table 5 lists the location, value, and functions of performance mode registers in the device.

Table 5. Performance Modes

MODE	LOCATION	FUNCTION
Special modes	Registers 139 (bit 3), 239 (bit 3), 439 (bit 3), and 539 (bit 3)	Always write 1 for best performance.
Disable dither	Registers 1 (bits 7-0), 134 (bits 5 and 3), 234 (bits 5 and 3), 434 (bits 5 and 3), and 534 (bits 5 and 3)	Disables the dither to improve SNR.
Disable chopper	Registers 122 (bit 1), 222 (bit 1), 422 (bit 1), and 522 (bit 1)	Disables the chopper (shifts the 1/f noise floor at dc).
High IF modes	Registers 11Dh (bit 1), 21Dh (bit 1), 41Dh (bit 1), 51Dh (bit 1), 308h (bits 7-6) and 608h (bits 7-6)	Improves HD3 by a couple of dB for IF > 100 MHz

9.5 Programming

The ADC344x device may be configured using a serial programming interface, as described in this section.

9.5.1 Serial Interface

The device has a set of internal registers that may be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data may be loaded in multiples of 24-bit words within a single active SEN pulse. The interface may function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

Programming (continued)

9.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in Figure 157. If required, the serial interface registers may be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) to high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.1.1.1 Serial Register Write

The device internal register may be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

Figure 157 and Table 6 show the timing requirements for the serial register write operation.

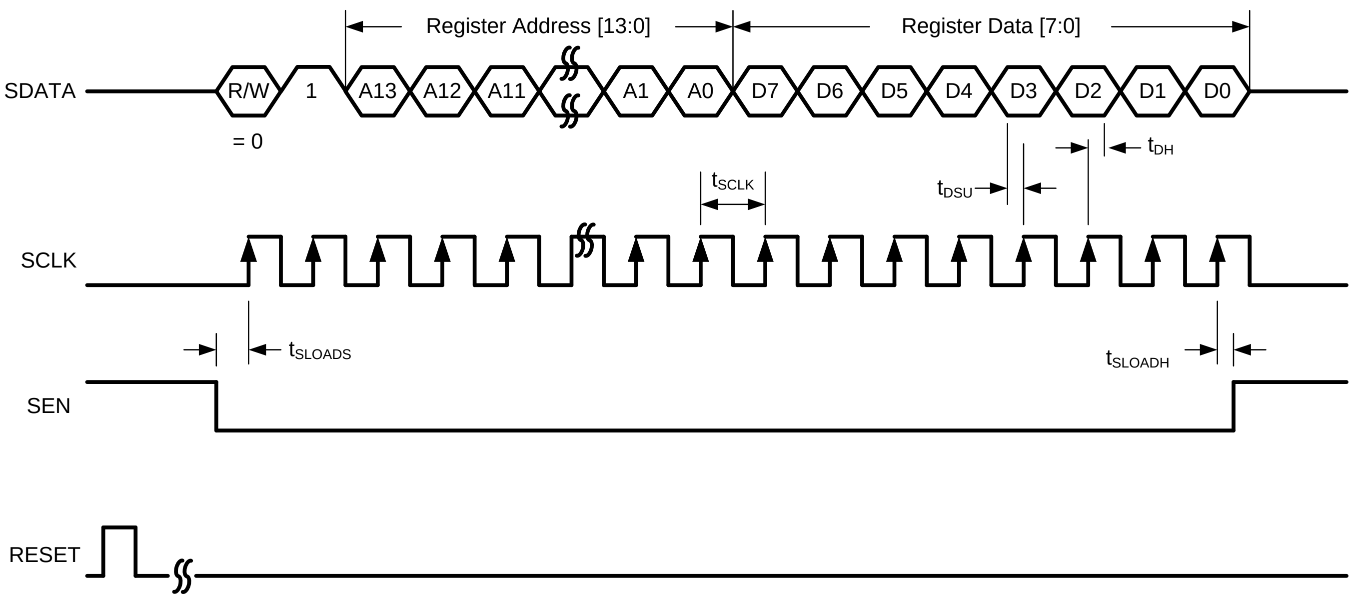


Figure 157. Serial Register Write Timing Diagram

Table 6. Serial Interface Timing(1)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, and AVDD = DVDD = 1.8 V, unless otherwise noted.

9.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers may be read back using the SDOUT pin. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller may latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 158 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 159.

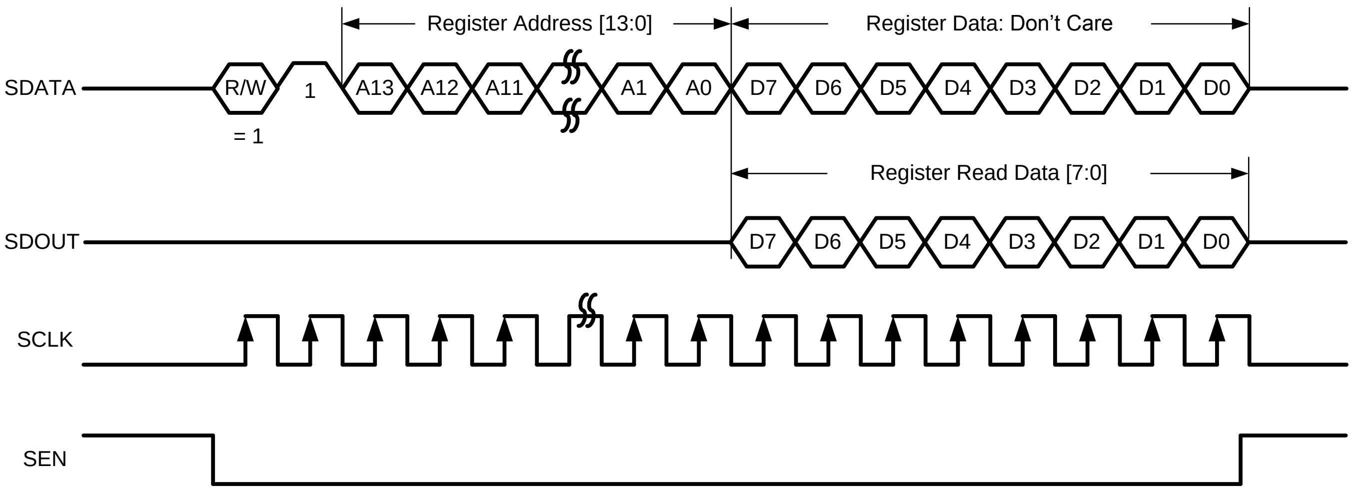


Figure 158. Serial Register Read Timing Diagram

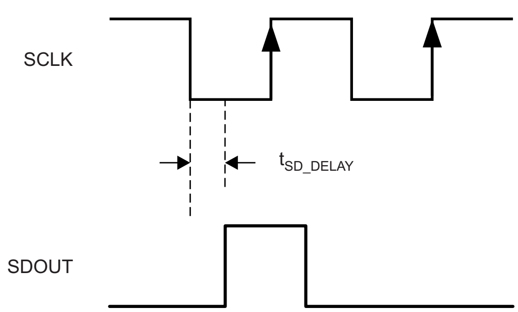


Figure 159. SDOUT Timing Diagram

9.5.2 ADC3441 Power-Up Requirements

Power-up begins with the application of AVDD and DVDD. The exact sequencing and ramp rate of AVDD and DVDD are not important as long as the parameters in Table 7 are met.

After power-up, the RESET pin must be pulsed high to reset the internal registers to the default values. Figure 160 and Table 7 show a power-up sequence.

During operation, the device registers can be restored to the default values by either pulsing the RESET pin high or by issuing a software reset via the SPI interface. A software reset can be issued by writing bit 0 of register 06h high. This bit is self-clearing.

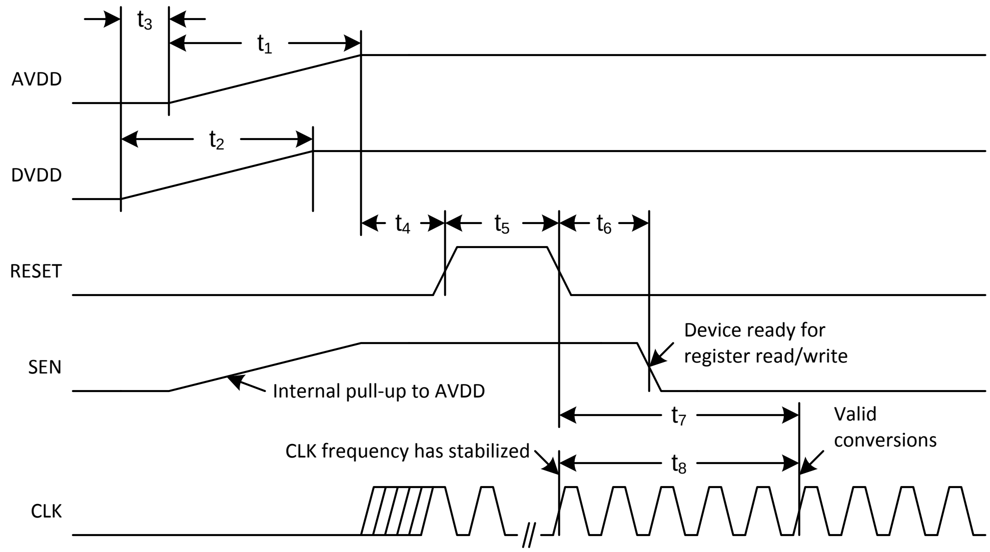


Figure 160. Power-Up Timing

Table 7. Power-Up Timing Table

		MIN	NOM	MAX	UNIT
t_1	AVDD supply power-up ramp time			10	ms
t_2	DVDD supply power-up ramp time			10	ms
t_3	AVDD to DVDD power-up delay	-10		10	ms
t_4	Device power-up to RESET assertion	1			ms
t_5	RESET assertion duration	10			ns
t_6	RESET deassertion to SEN assertion	10			µs
t_7	RESET deassertion to valid conversions	150			µs
t_8	CLK stable frequency to valid conversions	150			µs

After the power supplies are valid, enable the sample clock. The sampling clock can be enabled before or after reset, but conversions are not valid until at least a minimum time after reset and the time that the sample clock reaches a stable frequency, as shown in Table 7.

Before using samples from the device, a minimum register write sequence must be applied, as described in Table 8. Apply this register write sequence after any further application of the hardware or software reset.

Table 8. Required Register Writes after Power-up or Reset

ADDRESS	DATA	NOTE
139h	08h	Channel A - best performance default
439h	08h	Channel B - best performance default
539h	08h	Channel C - best performance default
239h	08h	Channel D - best performance default
137h	40h	ADC core latch reset
437h	40h	
537h	40h	
237h	40h	
137h	00h	
437h	00h	
537h	00h	
237h	00h	

These register writes configure the optimal settings for ADC performance and apply a reset to the internal latches inside the ADC core that are not part of the device reset function. After the register writes of Table 8 are written, any use-case-specific registers must be applied before using the conversion values.

9.6 Register Maps

Table 9. Register Map Summary

REGISTER ADDRESS, A[13:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
Register 01h	DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	
Register 03h	0	0	0	0	0	0	0	ODD EVEN
Register 04h	0	0	0	0	0	0	0	FLIP WIRE
Register 05h	0	0	0	0	0	0	0	1W-2W
Register 06h	0	0	0	0	0	0	TEST PATTERN EN	RESET
Register 07h	0	0	0	0	0	0	0	OVR ON LSB
Register 09h	0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
Register 0Ah	CHA TEST PATTERN				CHB TEST PATTERN			
Register 0Bh	CHC TEST PATTERN				CHD TEST PATTERN			
Register 13h	0	0	0	0	0	0	LOW SPEED ENABLE	
Register 0Eh	CUSTOM PATTERN[13:6]							
Register 0Fh	CUSTOM PATTERN[5:0]						0	0
Register 15h	CHA PDN	CHB PDN	CHC PDN	CHD PDN	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
Register 25h	LVDS SWING							
Register 27h	CLK DIV		0	0	0	0	0	0
Register 11Dh	0	0	0	0	0	0	HIGH IF MODE0	0
Register 122h	0	0	0	0	0	0	DIS CHOP CHA	0
Register 134h	0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
Register 139h	0	0	0	0	SP1 CHA	0	0	0
Register 21Dh	0	0	0	0	0	0	HIGH IF MODE1	0
Register 222h	0	0	0	0	0	0	DIS CHOP CHD	0
Register 234h	0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0
Register 239h	0	0	0	0	SP1 CHD	0	0	0
Register 308	HIGH IF MODE <5:4>		0	0	0	0	0	0
Register 41Dh	0	0	0	0	0	0	HIGH IF MODE2	0
Register 422h	0	0	0	0	0	0	DIS CHOP CHB	0
Register 434h	0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0
Register 439h	0	0	0	0	SP1 CHB	0	0	0
Register 51Dh	0	0	0	0	0	0	HIGH IF MODE3	0
Register 522h	0	0	0	0	0	0	DIS CHOP CHC	0
Register 534h	0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0
Register 539h	0	0	0	0	SP1 CHC	0	0	0
Register 608h	HIGH IF MODE <7:6>		0	0	0	0	0	0
Register 70Ah	0	0	0	0	0	0	0	PDN SYSREF

9.6.1 Serial Register Description

9.6.1.1 Register 01h (address = 01h)

Figure 161. Register 01h

7	6	5	4	3	2	1	0
DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 10. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIS DITH CHA	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 134h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
5-4	DIS DITH CHB	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
3-2	DIS DITH CHC	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 534h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
1-0	DIS DITH CHD	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 234h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.

9.6.1.2 Register 03h (address = 03h)

Figure 162. Register 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ODD EVEN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 11. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	ODD EVEN	R/W	0h	This bit selects the bit sequence on the output wires (in 2-wire mode only). 0 = Bits 0, 1, 2, and so forth appear on wire-0; bits 7, 8, 9, and so forth appear on wire-1. 1 = Bits 0, 2, 4, and so forth appear on wire-0; bits 1, 3, 5, and so forth appear on wire-1.

9.6.1.3 Register 04h (address = 04h)

Figure 163. Register 04h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FLIP WIRE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 12. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	FLIP WIRE	R/W	0h	This bit flips the data on the output wires. Valid only in two wire configuration. 0 = Default 1 = Data on output wires is flipped. Pin D0x becomes D1x, and vice versa.

9.6.1.4 Register 05h (address = 05h)

Figure 164. Register 05h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1W-2W
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 13. Register 05h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	1W-2W	R/W	0h	This bit transmits output data on either one or two wires. 0 = Output data are transmitted on two wires (Dx0P, Dx0M and Dx1P, Dx1M) 1 = Output data are transmitted on one wire (Dx0P, Dx0M). In this mode, the recommended f_S is less than 80 MSPS.

9.6.1.5 Register 06h (address = 06h)

Figure 165. Register 06h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PATTERN EN	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 14. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	TEST PATTERN EN	R/W	0h	Enables test pattern selection for the digital outputs. 0 = Normal output 1 = Test pattern output enabled
0	RESET	R/W	0h	Software reset applied. This bit resets all internal registers to the default values and self-clears to 0.

9.6.1.6 Register 07h (address = 07h)

Figure 166. Register 07h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	OVR ON LSB
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 15. Register 07h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	OVR ON LSB	R/W	0h	OVR information on the LSB bits. 0 = Output data bit 0 functions as the LSB of the 14-bit data 1 = Output data bit 0 carries the overrange (OVR) information.

9.6.1.7 Register 09h (address = 09h)

Figure 167. Register 09h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 16. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	ALIGN TEST PATTERN	R/W	0h	This bit aligns the test patterns across the outputs of both channels. 0 = Test patterns of both channels are free running 1 = Test patterns of both channels are aligned
0	DATA FORMAT	R/W	0h	Digital output data format. 0 = Twos complement 1 = Offset binary

9.6.1.8 Register 0Ah (address = 0Ah)

Figure 168. Register 0Ah

7	6	5	4	3	2	1	0
CHA TEST PATTERN				CHB TEST PATTERN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 17. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CHA TEST PATTERN	R/W	0h	These bits control the test pattern for channel A after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits 0110 = Deskew pattern: data are 2AAAh 1000 = PRBS pattern: data are a sequence of pseudo random numbers 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use
3-0	CHB TEST PATTERN	R/W	0h	These bits control the test pattern for channel B after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits 0110 = Deskew pattern: data are 2AAAh 1000 = PRBS pattern: data are a sequence of pseudo random numbers 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use

9.6.1.9 Register 0Bh (address = 0Bh)

Figure 169. Register 0Bh

7	6	5	4	3	2	1	0
CHC TEST PATTERN				CHD TEST PATTERN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 18. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CHC TEST PATTERN	R/W	0h	These bits control the test pattern for channel C after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits 0110 = Deskew pattern: data are 2AAAh 1000 = PRBS pattern: data are a sequence of pseudo random numbers 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use
3-0	CHD TEST PATTERN	R/W	0h	These bits control the test pattern for channel D after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 10101010101010 and 01010101010101 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits 0110 = Deskew pattern: data are 2AAAh 1000 = PRBS pattern: data are a sequence of pseudo random numbers 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399. Others = Do not use

9.6.1.10 Register 13h (address = 13h)

Figure 170. Register 13h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LOW SPEED ENABLE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 19. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1-0	LOW SPEED ENABLE	R/W	0h	Enables low speed operation in 1-wire and 2-wire mode. Depending upon sampling frequency, write this bit as per Table 20.

Table 20. LOW SPEED ENABLE Register Settings Across f_S

f_S, MSPS		REGISTER BIT LOW SPEED ENABLE	
MIN	MAX	1-WIRE MODE	2-WIRE MODE
25	125	00	00
20	25	00	10
15	20	10	Not supported

9.6.1.11 Register 0Eh (address = 0Eh)

Figure 171. Register 0Eh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[13:6]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 21. Register 0Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN[13:6]	R/W	0h	These bits set the 14-bit custom pattern (bits 13-6) for all channels.

9.6.1.12 Register 0Fh (address = 0Fh)

Figure 172. Register 0Fh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[5:0]						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 22. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	CUSTOM PATTERN[5:0]	R/W	0h	These bits set the 14-bit custom pattern (bits 5-0) for all channels.
1-0	0	W	0h	Must write 0.

9.6.1.13 Register 15h (address = 15h)

Figure 173. Register 15h

7	6	5	4	3	2	1	0
CHA PDN	CHB PDN	CHC PDN	CHD PDN	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 23. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
7	CHA PDN	W	0h	0 = Normal operation 1 = Power-down channel A
6	CHB PDN	R/W	0h	0 = Normal operation 1 = Power-down channel B
5	CHC PDN	R/W	0h	0 = Normal operation 1 = Power-down channel C
4	CHD PDN	W	0h	0 = Normal operation 1 = Power-down channel D
3	STANDBY	R/W	0h	ADCs of both channels enter standby. 0 = Normal operation 1 = Standby
2	GLOBAL PDN	R/W	0h	0 = Normal operation 1 = Global power-down
1	0	W	0h	Must write 0.
0	CONFIG PDN PIN	R/W	0h	This bit configures the PDN pin as either a global power-down or standby pin. 0 = Logic high voltage on PDN pin sends the device into global power-down 1 = Logic high voltage on PDN pin sends the device into standby

9.6.1.14 Register 25h (address = 25h)

Figure 174. Register 25h

7	6	5	4	3	2	1	0
LVDS SWING							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 24. Register 25h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LVDS SWING	R/W	0h	These bits control the swing of the LVDS outputs (including the data output, bit clock, and frame clock).

9.6.1.15 Register 27h (address = 27h)

Figure 175. Register 27h

7	6	5	4	3	2	1	0
CLK DIV		0	0	0	0	0	0
R/W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 25. Register 27h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CLK DIV	R/W	0h	Internal clock divider for the input sampling clock. 00 = Divide-by-1 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4
5-0	0	W	0h	Must write 0.

9.6.1.16 Register 11Dh (address = 11Dh)

Figure 176. Register 11Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 26. Register 11Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE0			Set the HIGH IF MODE[7:0] bits together to 1111. Improves HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

9.6.1.17 Register 122h (address = 122h)

Figure 177. Register 122h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHA	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 27. Register 122h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHA	R/W	0h	Disables the chopper. Set this bit to shift 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

9.6.1.18 Register 134h (address = 134h)

Figure 178. Register 134h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 28. Register 134h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHA	R/W	0h	Set this bit with bits 7 and 6 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHA	R/W	0h	Set this bit with bits 7 and 6 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

9.6.1.19 Register 139h (address = 139h)

Figure 179. Register 139h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHA	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 29. Register 139h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHA	R/W	0h	Special mode for best performance on channel A. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

9.6.1.20 Register 21Dh (address = 21Dh)

Figure 180. Register 21Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE1	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 30. Register 21Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE1			Set the HIGH IF MODE[7:0] bits together to 1111. Improves HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

9.6.1.21 Register 222h (address = 222h)

Figure 181. Register 222h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHD	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 31. Register 222h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHD	R/W	0h	Disables the chopper. Set this bit to shift 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

9.6.1.22 Register 234h (address = 234h)

Figure 182. Register 234h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 32. Register 234h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHD	R/W	0h	Set this bit with bits 1 and 0 of register 01h. 00 = Default 11 = Dither is disabled for channel D. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHD	R/W	0h	Set this bit with bits 1 and 0 of register 01h. 00 = Default 11 = Dither is disabled for channel D. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

9.6.1.23 Register 239h (address = 239h)

Figure 183. Register 239h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHD	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 239h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHD	R/W	0h	Special mode for best performance on channel D. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

9.6.1.24 Register 308h (address = 308h)

Figure 184. Register 308h

7	6	5	4	3	2	1	0
HIGH IF MODE<5:4>		0	0	0	0	0	0
W-0h		W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 308h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HIGH IF MODE<5:4>	W	0h	Set the HIGH IF MODE[7:0] bits together to FFh. Improves HD3 by a couple of dB for IF > 100 MHz.
5-0	0	W	0h	Must write 0.

9.6.1.25 Register 41Dh (address = 41Dh)

Figure 185. Register 41Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE2	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 35. Register 41Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE2			Set the HIGH IF MODE[7:0] bits together to FFh. Improves HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

9.6.1.26 Register 422h (address = 422h)

Figure 186. Register 422h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHB	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 36. Register 422h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHB	R/W	0h	Disables the chopper. Set this bit to shift 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

9.6.1.27 Register 434h (address = 434h)

Figure 187. Register 434h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 37. Register 434h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHB	R/W	0h	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHB	R/W	0h	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

9.6.1.28 Register 439h (address = 439h)

Figure 188. Register 439h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHB	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 38. Register 439h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHB	R/W	0h	Special mode for best performance on channel B. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

9.6.1.29 Register 51Dh (address = 51Dh)

Figure 189. Register 51Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE3	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 39. Register 51Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE3			Set the HIGH IF MODE[7:0] bits together to FFh. Improves HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

9.6.1.30 Register 522h (address = 522h)

Figure 190. Register 522h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHC	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 40. Register 522h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHC	R/W	0h	Disables the chopper. Set this bit to shift 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

9.6.1.31 Register 534h (address = 534h)

Figure 191. Register 534h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 41. Register 534h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHC	R/W	0h	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel C. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHC	R/W	0h	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel C. In this mode, SNR typically improves by 0.5 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

9.6.1.32 Register 539h (address = 539h)

Figure 192. Register 539h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHC	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 42. Register 539h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHC	R/W	0h	Special mode for best performance on channel C. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

9.6.1.33 Register 608h (address = 608h)

Figure 193. Register 608h

7	6	5	4	3	2	1	0
HIGH IF MODE<7:6>		0	0	0	0	0	0
W-0h		W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 43. Register 608h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HIGH IF MODE<7:6>			Set the HIGH IF MODE[7:0] bits together to FFh. Improves HD3 by a couple of dB for IF > 100 MHz.
5-0	0	W	0h	Must write 0.

9.6.1.34 Register 70Ah (address = 70Ah)

Figure 194. Register 70Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PDN SYSREF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 44. Register 70Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	PDN SYSREF	R/W	0h	If the SYSREF pins are not used in the system, the SYSREF buffer must be powered down by setting this bit. 0 = Normal operation 1 = Powers down the SYSREF buffer

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) may be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. While designing the dc driving circuits, the ADC input impedance must be considered. Figure 195 and Figure 196 show the impedance ($Z_{in} = R_{in} \parallel C_{in}$) across the ADC input pins.

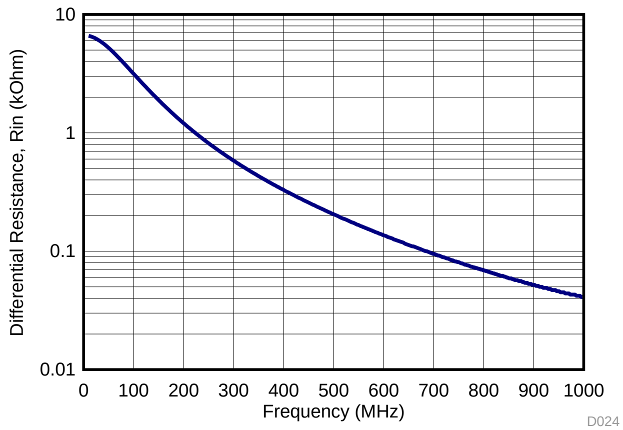


Figure 195. Differential Input Resistance, R_{IN}

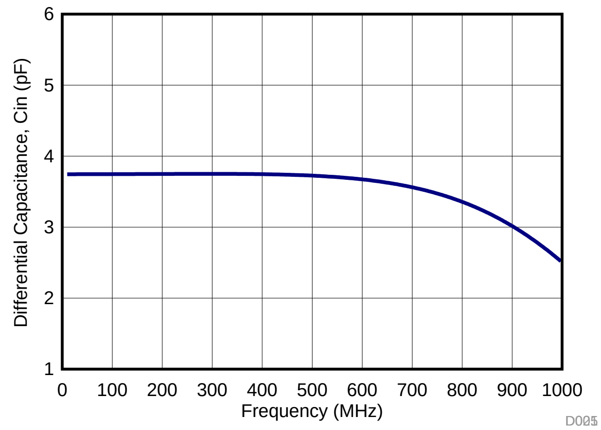


Figure 196. Differential Input Capacitance, C_{IN}

10.2 Typical Applications

10.2.1 Driving Circuit Design: Low Input Frequencies

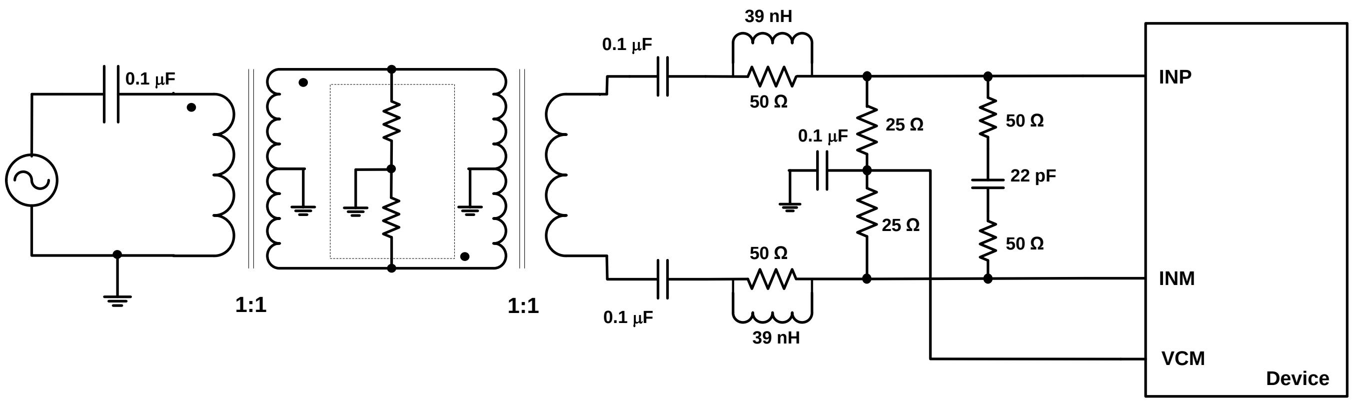


Figure 197. Driving Circuit for Low Input Frequencies

10.2.1.1 Design Requirements

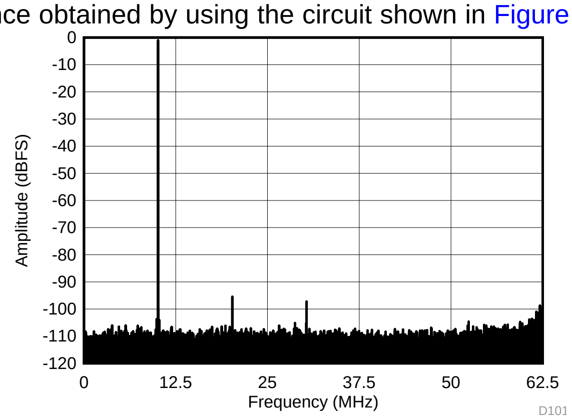
For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin may be kept to damp out ringing caused by package parasitic. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

10.2.1.2 Detailed Design Procedure

A typical application involving using two back-to-back coupled transformers is shown in Figure 197. The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used with the series inductor (39 nH), this combination helps absorb the sampling glitches. To improve phase and amplitude balance of first transformer, the termination resistors can be split between two transformers. For example, 25-Ω to 25-Ω termination across the secondary winding of the second transformer can be changed to 50-Ω to 50-Ω termination and another 50-Ω to 50-Ω resistor can be placed inside the dashed box between the transformers in Figure 197.

10.2.1.3 Application Curve

Figure 198 shows the performance obtained by using the circuit shown in Figure 197.



SFDR = 95 dBc, SNR = 72.7 dBFS, SINAD = 72.6 dBFS,
THD = 100 dBc, HD2 = 95 dBc, HD3 = 96 dBc

Figure 198. FFT for 10-MHz Input Signal (Chopper On, Dither On)

Typical Applications (continued)

10.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz

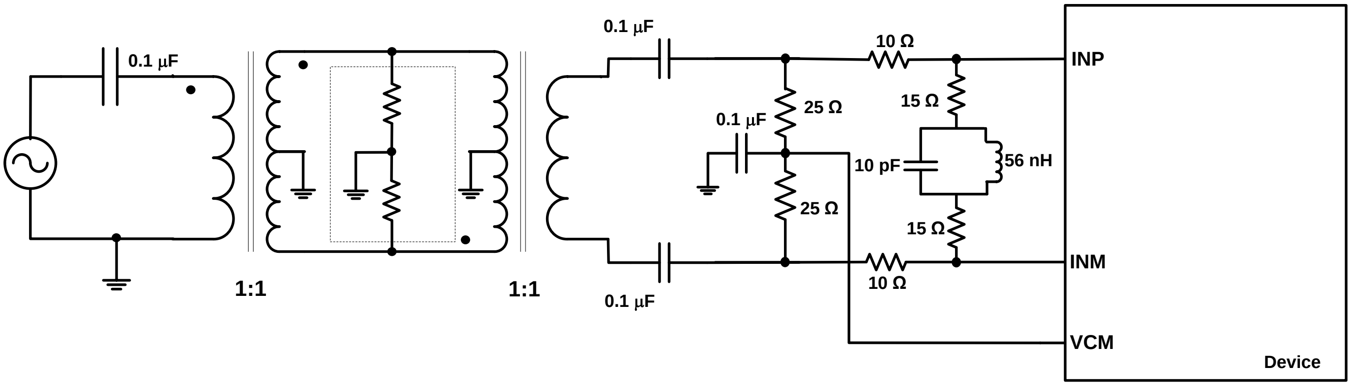


Figure 199. Driving Circuit for Mid-Range Input Frequencies (100 MHz < f_{IN} < 230 MHz)

10.2.2.1 Design Requirements

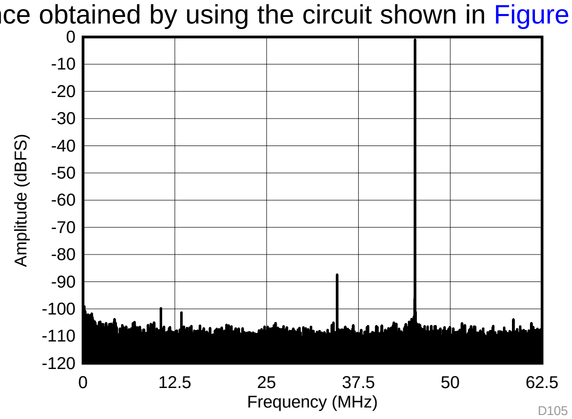
See the *Design Requirements* section for further details.

10.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit may be used to optimize performance, as shown in Figure 199.

10.2.2.3 Application Curve

Figure 200 shows the performance obtained by using the circuit shown in Figure 199.



SFDR = 86 dBc, SNR = 71.7 dBFS, SINAD = 71.6 dBFS,
THD = 93 dBc, HD2 = 86 dBc, HD3 = 99 dBc

Figure 200. FFT for 170-MHz Input Signal (Chopper Off, Dither On)

Typical Applications (continued)

10.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

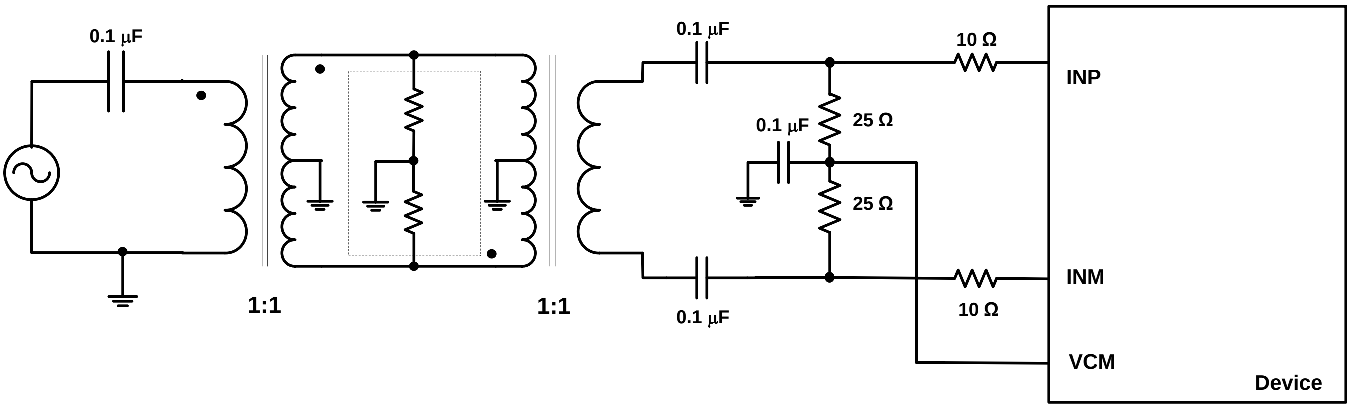


Figure 201. Driving Circuit for High Input Frequencies (f_{IN} > 230 MHz)

10.2.3.1 Design Requirements

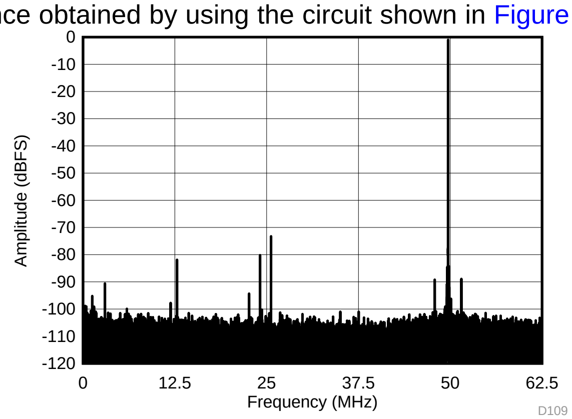
See the *Design Requirements* section for further details.

10.2.3.2 Detailed Design Procedure

For high input frequencies (> 230 MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of 10 Ω may be used as shown in Figure 201.

10.2.3.3 Application Curve

Figure 202 shows the performance obtained by using the circuit shown in Figure 201.



SFDR = 72 dBc, SNR = 68.2 dBFS, SINAD = 67.3 dBFS,
THD = 74 dBc, HD2 = 72 dBc, HD3 = 79 dBc

Figure 202. FFT for 450-MHz Input Signal (Chopper Off, Dither On)

11 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD may power up in any order. See Figure 160 for other power-up requirements.

12 Layout

12.1 Layout Guidelines

The ADC344x EVM layout may be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 203. Some important points to remember during laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pin out in opposite directions, as shown in the reference layout of Figure 203 as much as possible.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 203 as much as possible.
3. Keep digital outputs away from the analog inputs. When these digital outputs exit the pin out, the digital output traces must not be kept parallel to the analog input traces because this configuration may result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors may be kept close to the supply source.

12.2 Layout Example

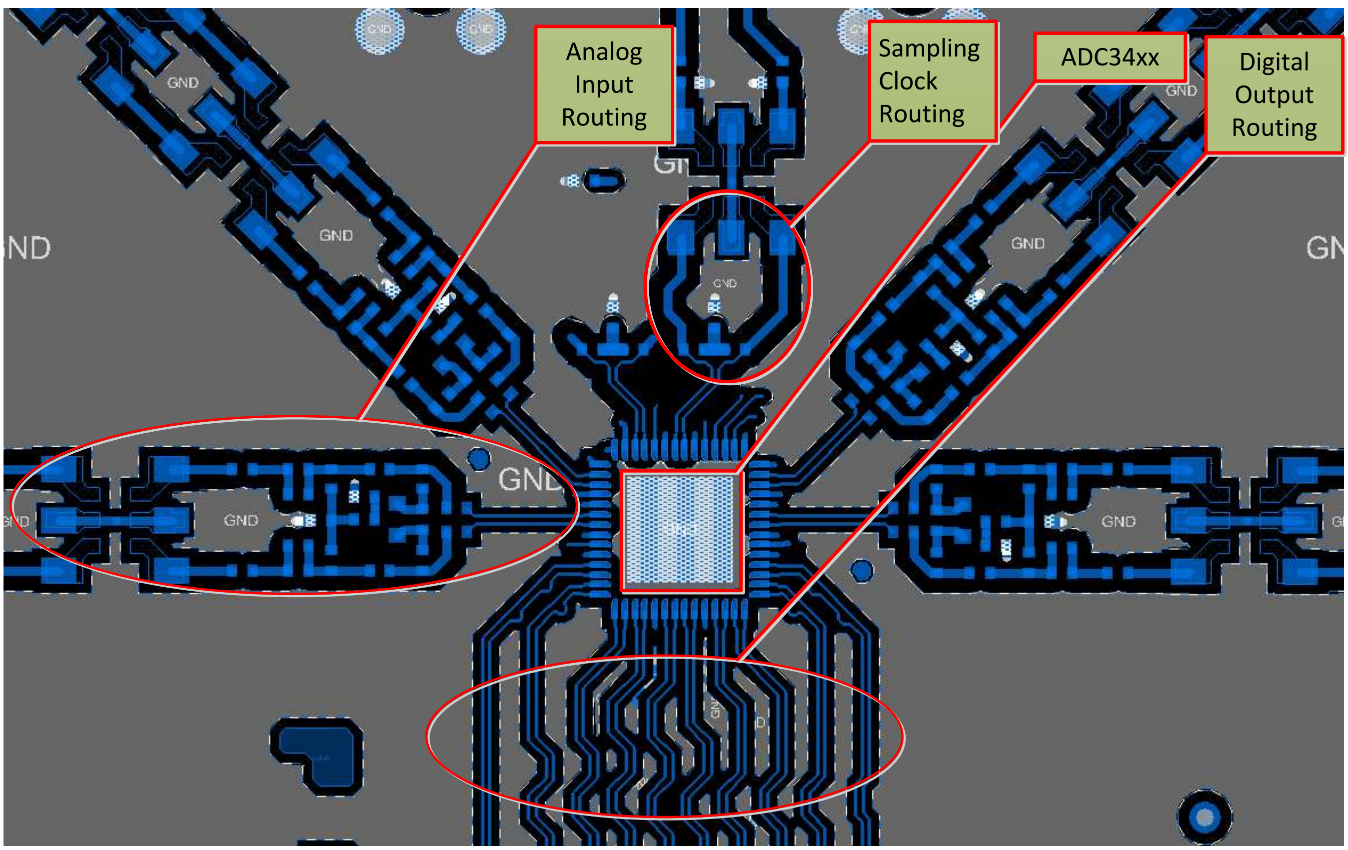


Figure 203. Typical Layout of the ADC344x Board

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 45. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADC3441	Click here	Click here	Click here	Click here	Click here
ADC3442	Click here	Click here	Click here	Click here	Click here
ADC3443	Click here	Click here	Click here	Click here	Click here
ADC3444	Click here	Click here	Click here	Click here	Click here

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC3441IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3441	Samples
ADC3441IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3441	Samples
ADC3442IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3442	Samples
ADC3442IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3442	Samples
ADC3443IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3443	Samples
ADC3443IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3443	Samples
ADC3444IRTQR	ACTIVE	QFN	RTQ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3444	Samples
ADC3444IRTQT	ACTIVE	QFN	RTQ	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ3444	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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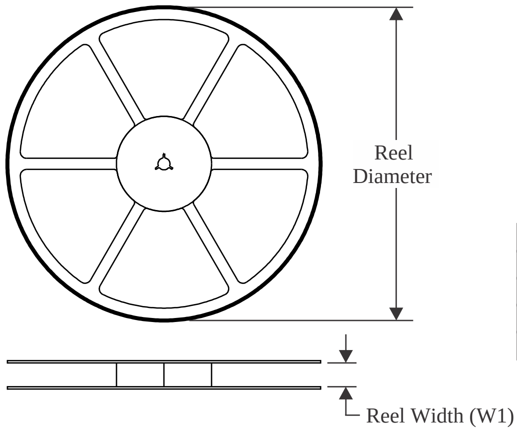
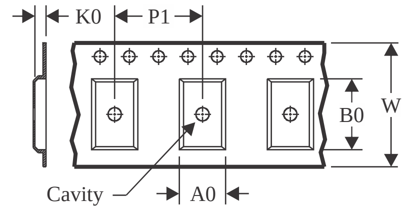
TAPE AND REEL INFORMATION

REEL DIMENSIONS

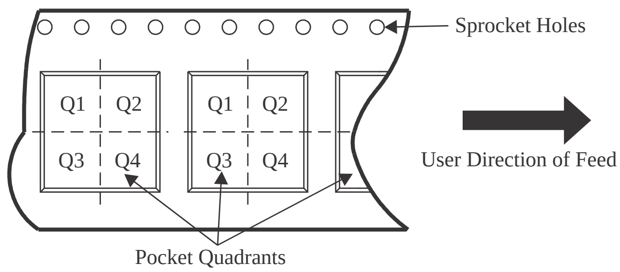


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

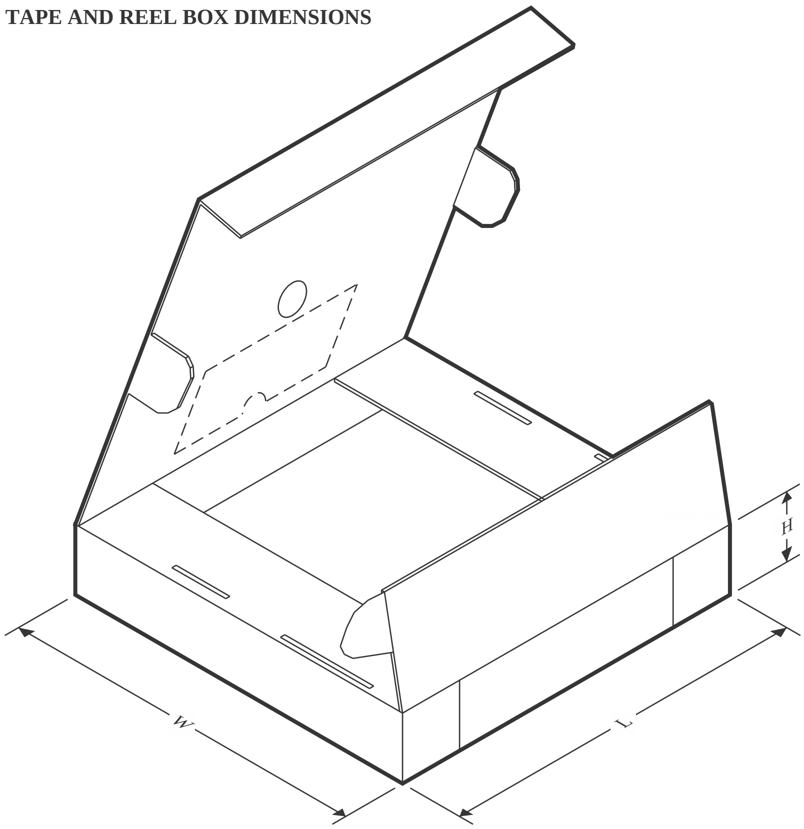
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC3441IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
ADC3442IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
ADC3443IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
ADC3444IRTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

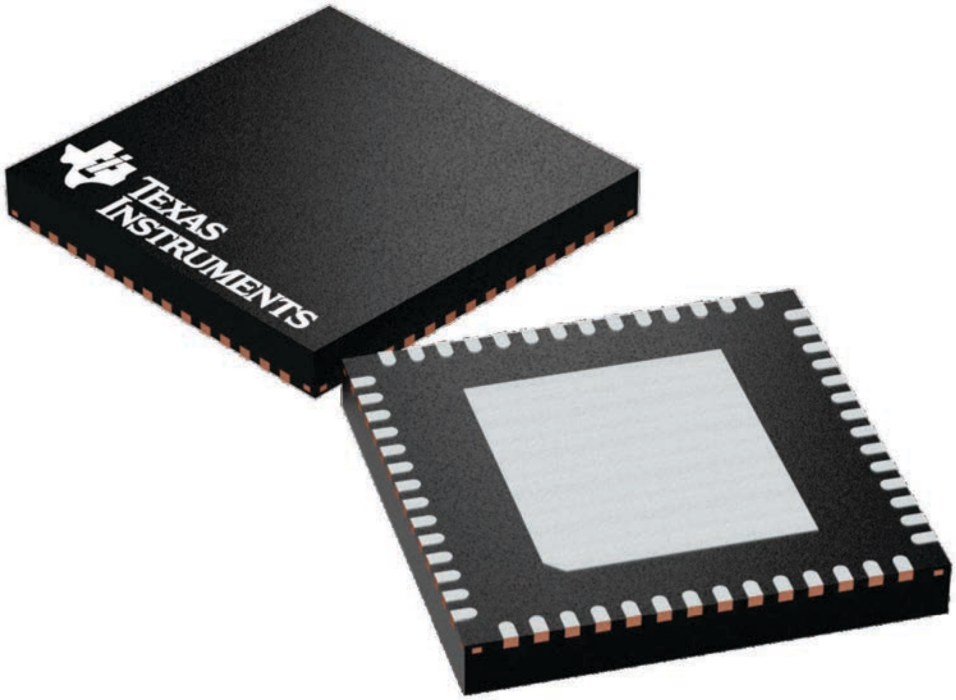
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC3441IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
ADC3442IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
ADC3443IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0
ADC3444IRTQR	QFN	RTQ	56	2000	350.0	350.0	43.0

RTQ 56

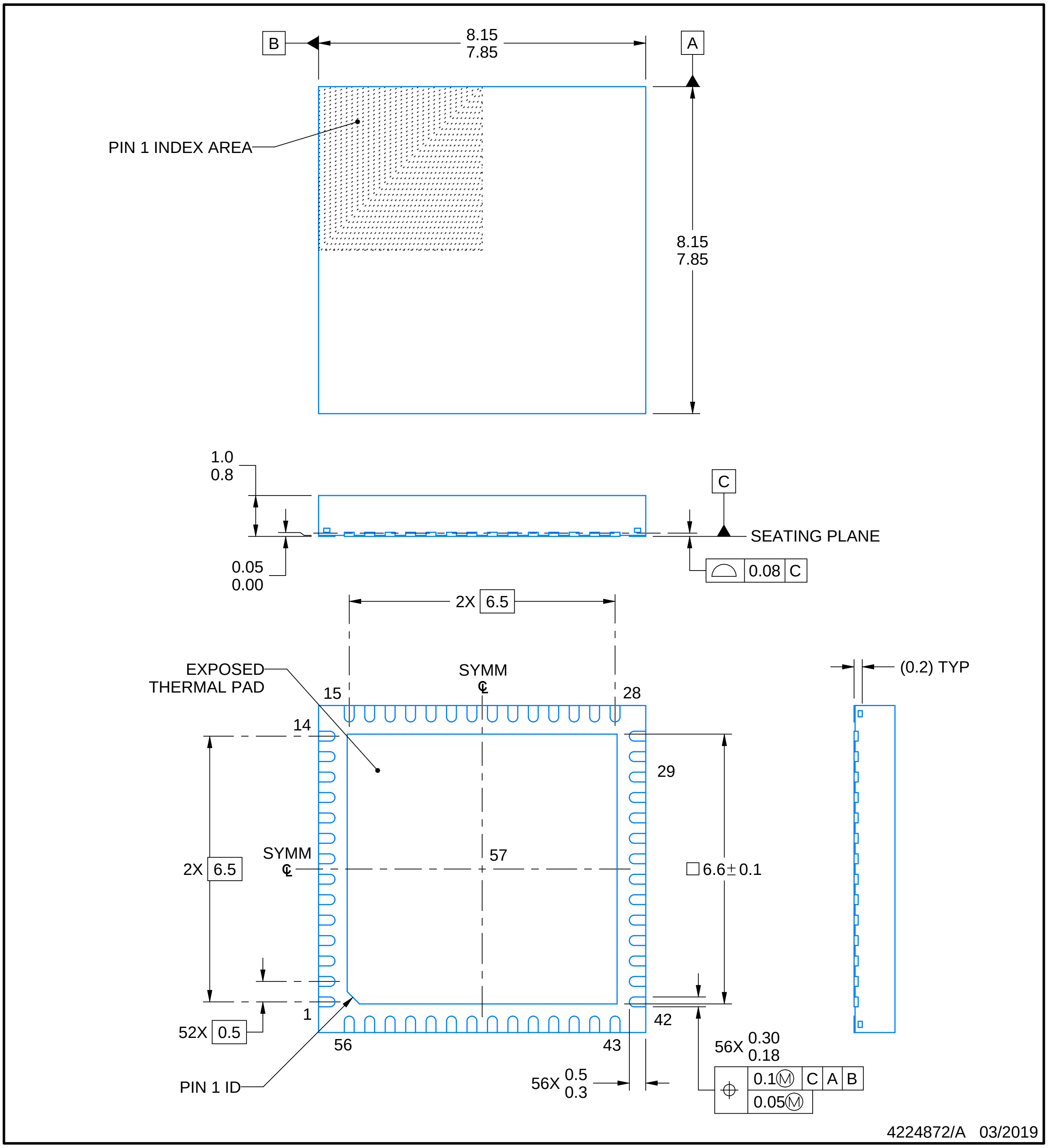
VQFN - 1 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

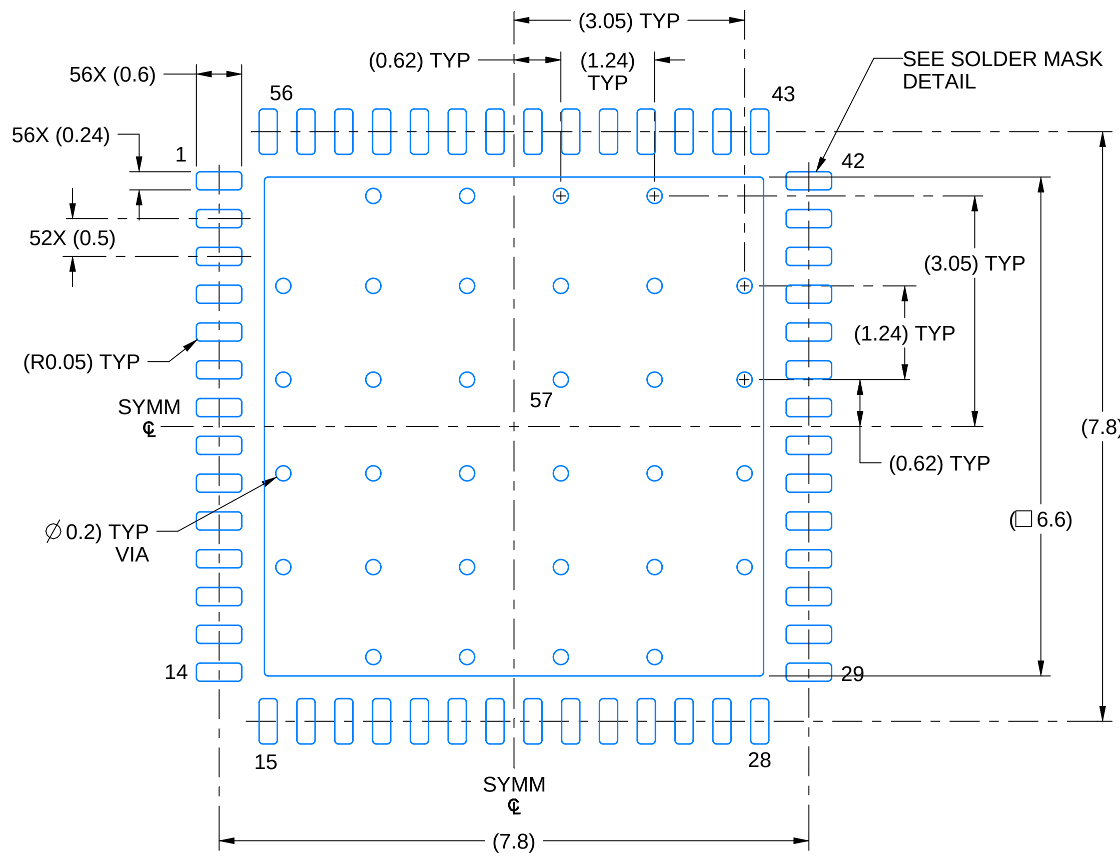


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

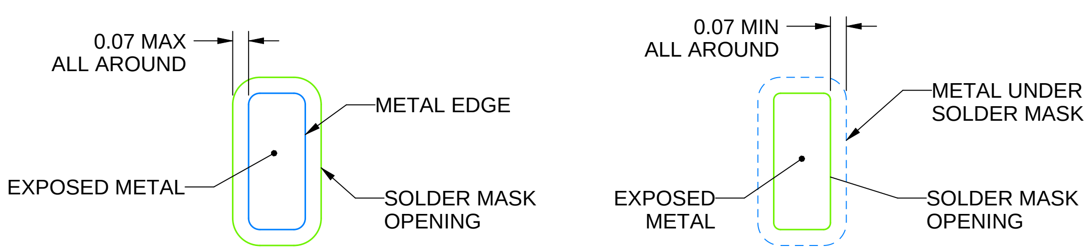


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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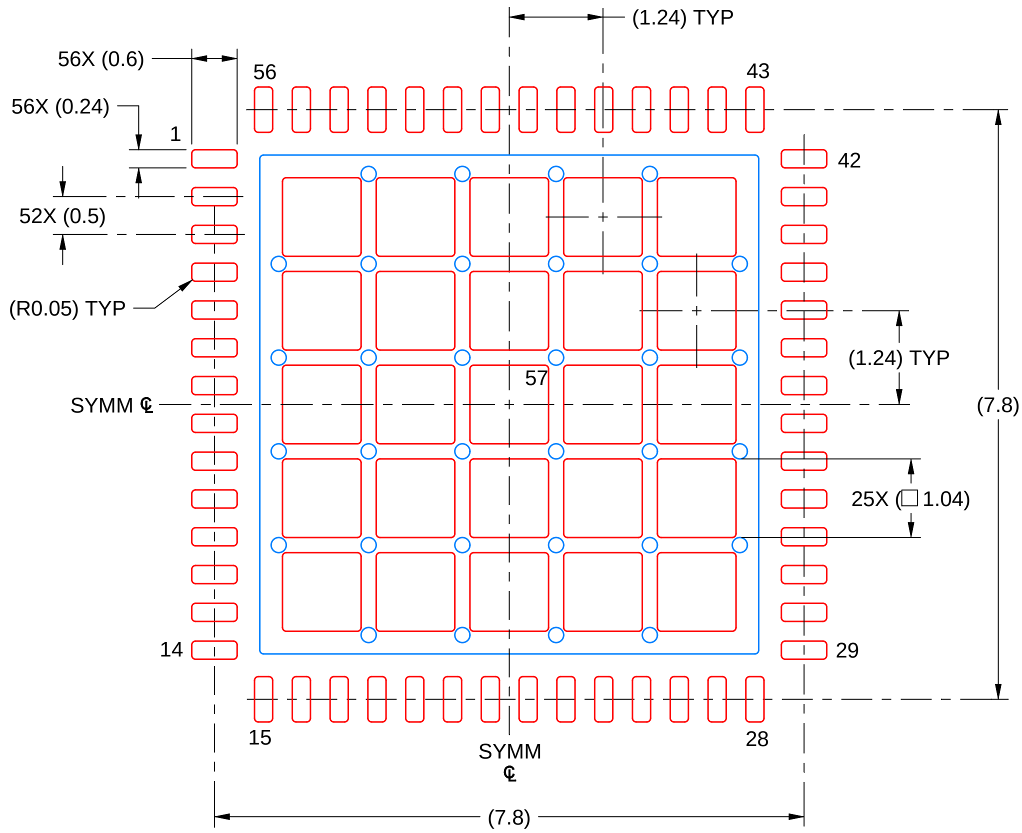
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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