

AMC1303x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With Internal Clock

1 Features

- Pin-compatible family optimized for shunt-resistor-based current measurements:
 - $\pm 50\text{mV}$ or $\pm 250\text{mV}$ input voltage ranges
 - Manchester-coded or uncoded bitstream options
 - 10MHz and 20MHz clock options
- Excellent DC performance:
 - Offset error: $\pm 50\mu\text{V}$ or $\pm 100\mu\text{V}$ (max)
 - Offset drift: $\pm 1\mu\text{V}/^\circ\text{C}$ (max)
 - Gain error: $\pm 0.2\%$ (max)
 - Gain drift: $\pm 40\text{ppm}/^\circ\text{C}$ (max)
- Transient immunity: 100kV/ μs (typ)
- System-level diagnostic features
- Safety-related certifications:
 - 7000V_{PK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
 - 5000V_{RMS} isolation for 1 minute per UL1577
 - CAN/CSA no. 5A-component acceptance service notice and IEC 62368-1 end equipment standard
- Fully specified over the extended industrial temperature range: -40°C to $+125^\circ\text{C}$

2 Applications

- Shunt-resistor-based current sensing and isolated voltage measurement in:
 - [Industrial motor drives](#)
 - [Photovoltaic inverters](#)
 - [Uninterruptible and isolated power supplies](#)
 - [Power factor correction circuits](#)

3 Description

The AMC1303 (AMC1303x0510, AMC1303x0520, AMC1303x2510, and AMC1303x2520) is a family of precision, isolated delta-sigma ($\Delta\Sigma$) modulators. The output is separated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000V_{PK} according to the DIN EN IEC 60747-17 (VDE 0884-17) and UL1577 standards, and supports a working voltage up to 1.5kV_{RMS}.

The input of the AMC1303 device is optimized for direct connection to shunt resistors or other, low-impedance signal sources. The small size, high DC accuracy, low temperature drift, and high common-mode transient immunity (CMTI) support accurate isolated current sensing in noisy high-voltage applications.

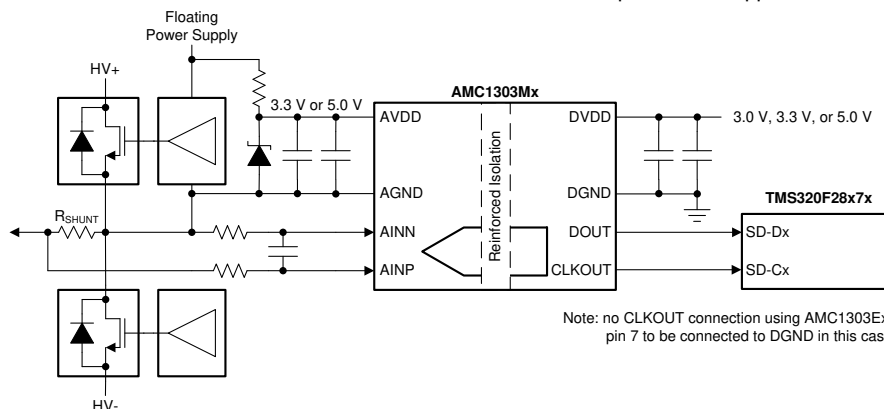
The output bitstream of the AMC1303 is synchronized to the internally generated clock and is Manchester coded (AMC1303Ex) or uncoded (AMC1303Mx). Combined with a digital low-pass filter (such as a Sinc-filter) the device achieves 85dB of dynamic range at an effective output data rate of 78kSPS.

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ |
|-------------|------------------------|-----------------------------|
| AMC1303x | DWV (SOIC, 8) | 5.85mm × 11.5mm |

(1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Schematic



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4 Device Comparison Table

| DEVICE | LINEAR INPUT VOLTAGE RANGE | DIFFERENTIAL INPUT RESISTANCE | DIGITAL OUTPUT INTERFACE | INTERNAL CLOCK FREQUENCY |
|------------------------------|----------------------------|-------------------------------|--------------------------|--------------------------|
| AMC1303E0510 | ±50mV | 4.9kΩ | Manchester-coded CMOS | 10MHz |
| AMC1303E2510 | ±250mV | 22kΩ | Manchester-coded CMOS | |
| AMC1303M0510 | ±50mV | 4.9kΩ | Uncoded CMOS | |
| AMC1303M2510 | ±250mV | 22kΩ | Uncoded CMOS | |
| AMC1303E0520 | ±50mV | 4.9kΩ | Manchester-coded CMOS | 20MHz |
| AMC1303E2520 | ±250mV | 22kΩ | Manchester-coded CMOS | |
| AMC1303M0520 | ±50mV | 4.9 kΩ | Uncoded CMOS | |
| AMC1303M2520 | ±250mV | 22kΩ | Uncoded CMOS | |
| AMC1303M2520F ⁽¹⁾ | ±250mV | 22kΩ | Uncoded CMOS | |

(1) Optimised for lower radiated emission

5 Pin Configuration and Functions

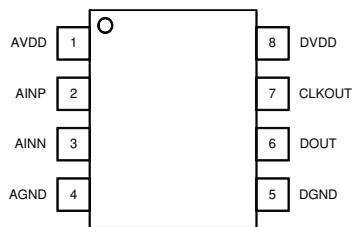


Figure 5-1. AMC1303Mx: DWV Package, 8-Pin SOIC (Top View)

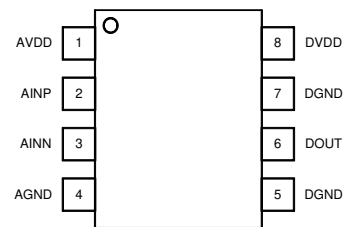


Figure 5-2. AMC1303Ex: DWV Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|--------|-----------|-----------|------|---|
| | AMC1303Mx | AMC1303Ex | | |
| AGND | 4 | 4 | — | Analog (high-side) ground reference. |
| AINN | 3 | 3 | I | Inverting analog input. |
| AINP | 2 | 2 | I | Noninverting analog input. |
| AVDD | 1 | 1 | — | Analog (high-side) power supply, 3.0V to 5.5V. See the Power Supply Recommendations section for decoupling recommendations. |
| CLKOUT | 7 | — | O | Modulator clock output, 10MHz (on AMC1303Mxx10) or 20MHz (on AMC1303Mxx20) nominal. |
| DGND | 5 | 5 | — | Digital (controller-side) ground reference. |
| DGND | — | 7 | — | Connect this pin to the controller-side ground for AMC1303Ex derivatives. |
| DOUT | 6 | 6 | O | Modulator bitstream output. This pin is a Manchester coded output for the AMC1303Ex derivatives. |
| DVDD | 8 | 8 | — | Digital (controller-side) power supply, 2.7V to 5.5V. See the Power Supply Recommendations section for decoupling recommendations. |

6 Specifications

6.1 Absolute Maximum Ratings

see ⁽¹⁾

| | MIN | MAX | UNIT |
|--|------------|------------|------|
| Supply voltage, AVDD to AGND or DVDD to DGND | -0.3 | 6.5 | V |
| Analog input voltage at AINP, AINN | AGND - 6 | AVDD + 0.5 | V |
| Digital output voltage at DOUT, CLKOUT | DGND - 0.5 | DVDD + 0.5 | V |
| Input current to any pin except supply pins | -10 | 10 | mA |
| Junction temperature, T _J | | 150 | °C |
| Storage temperature, T _{stg} | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 | |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------------|---|-----|-----|-----|------|
| AVDD | Analog (high-side) supply voltage (AVDD to AGND) | 3.0 | 5.0 | 5.5 | V |
| DVDD | Digital (controller-side) supply voltage (DVDD to DGND) | 2.7 | 3.3 | 5.5 | V |
| T _A | Operating ambient temperature | -40 | | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | AMC1303x | UNIT |
|-------------------------------|--|------------|------|
| | | DWV (SOIC) | |
| | | 8 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 112.2 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 47.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 60.0 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 23.1 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 60.0 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|-----------------------------------|-----|-----|-------|------|
| P _D | Maximum power dissipation (both sides) | AMC1303Exxx20, AVDD = DVDD = 5.5V | | | 89.65 | mW |
| | | AMC1303Mxxx20, AVDD = DVDD = 5.5V | | | 93.50 | |
| P _{D1} | Maximum power dissipation (high-side supply) | AMC1303xxx20, AVDD = 5.5V | | | 53.90 | mW |
| P _{D2} | Maximum power dissipation (low-side supply) | AMC1303Exxx20, DVDD = 5.5V | | | 35.75 | mW |
| | | AMC1303Mxxx20, DVDD = 5.5V | | | 39.60 | |

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|--|---|--|--------------------|------------------|
| GENERAL | | | | |
| CLR | External clearance ⁽¹⁾ | Shortest pin-to-pin distance through air | ≥ 8.5 | mm |
| CPG | External creepage ⁽¹⁾ | Shortest pin-to-pin distance across the package surface | ≥ 8.5 | mm |
| DTI | Distance through insulation | Minimum internal gap (internal clearance) of the double insulation (2 × 0.0105mm) | ≥ 0.021 | mm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | ≥ 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 300V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 600V _{RMS} | I-IV | |
| | | Rated mains voltage ≤ 1000V _{RMS} | I-III | |
| DIN EN IEC 60747-17 (VDE 0884-17)⁽²⁾ | | | | |
| V _{IORM} | Maximum repetitive peak isolation voltage | At ac voltage (bipolar) | 2121 | V _{PK} |
| V _{IOWM} | Maximum-rated isolation working voltage | At ac voltage (sine wave) | 1500 | V _{RMS} |
| | | At dc voltage | 2121 | V _{DC} |
| V _{IOTM} | Maximum transient isolation voltage | V _{TEST} = V _{IOTM} , t = 60s (qualification test) V _{TEST} = 1.2 × V _{IOTM} , t = 1s (100% production test) | 7000 | V _{PK} |
| V _{IMP} | Maximum impulse voltage ⁽³⁾ | Tested in air, 1.2/50μs waveform per IEC 62368-1 | 9800 | V _{PK} |
| V _{IOSM} | Maximum surge isolation voltage ⁽⁴⁾ | Tested in oil (qualification test), 1.2/50μs waveform per IEC 62368-1 | 12800 | V _{PK} |
| q _{pd} | Apparent charge ⁽⁵⁾ | Method a, after input/output safety test subgroup 2 / 3, V _{ini} = V _{IOTM} , t _{ini} = 60s, V _{pd(m)} = 1.2 × V _{IORM} = 2545V _{PK} , t _m = 10s | ≤ 5 | pC |
| | | Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60s, V _{pd(m)} = 1.6 × V _{IORM} = 3394V _{PK} , t _m = 10s | ≤ 5 | |
| | | Method b1, at routine test (100% production) and type test, V _{ini} = V _{IOTM} , t _{ini} = 1s, V _{pd(m)} = 1.875 × V _{IORM} = 3977V _{PK} , t _m = 1s | ≤ 5 | |
| C _{IO} | Barrier capacitance, input to output ⁽⁶⁾ | V _{IO} = 0.5V _{PP} at 1MHz | ~1 | pF |
| R _{IO} | Insulation resistance, input to output ⁽⁶⁾ | V _{IO} = 500V at T _A = 25°C | > 10 ¹² | Ω |
| | | V _{IO} = 500V at 100°C ≤ T _A ≤ 125°C | > 10 ¹¹ | Ω |
| | | V _{IO} = 500V at T _S = 150°C | > 10 ⁹ | Ω |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| UL1577 | | | | |
| V _{ISO} | Withstand isolation voltage | V _{TEST} = V _{ISO} , t = 60s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1s (100% production test) | 5000 | V _{RMS} |

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design and make sure the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings is specified by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

| VDE | UL |
|--|---|
| DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9 | Recognized under 1577 component recognition and CSA component acceptance NO 5 programs |
| Reinforced insulation | Single protection |
| Certificate number: 40040142 | File number: E181974 |

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|---|-----|-----|---------------------|------|
| I _S | Safety input, output, or supply current, see Figure 6-3 | R _{θJA} = 112.2°C/W, VDD1 = VDD2 = 5.5 V, T _J = 150°C, T _A = 25°C | | | 202.5 | mA |
| | | R _{θJA} = 112.2°C/W, VDD1 = VDD2 = 3.6 V, T _J = 150°C, T _A = 25°C | | | 309.4 | |
| P _S | Safety input, output, or total power, see Figure 6-4 | R _{θJA} = 112.2°C/W, T _J = 150°C, T _A = 25°C | | | 1114 ⁽¹⁾ | mW |
| T _S | Maximum safety temperature | | | | 150 | °C |

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where T_{J(max)} is the maximum junction temperature.

$P_S = I_S \times AVDD_{max} + I_S \times AVDD_{max}$, where AVDD_{max} is the maximum high-side supply voltage and DVDD_{max} is the maximum controller-side supply voltage.

6.9 Electrical Characteristics: AMC1303x05x

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $AVDD = 3.0\text{V}$ to 5.5V , $DVDD = 2.7\text{V}$ to 5.5V , $A_{INP} = -50\text{mV}$ to 50mV , $A_{INN} = \text{AGND}$, and sinc³ filter with $\text{OSR} = 256$ (unless otherwise noted); typical specifications are at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{V}$, and $DVDD = 3.3\text{V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|----------|---------------|------------|------------------------------|
| ANALOG INPUTS | | | | | | |
| V_{Clipping} | Differential input voltage before clipping output | $V_{\text{IN}} = A_{\text{INP}} - A_{\text{INN}}$ | | ± 64 | | mV |
| FSR | Specified linear differential full-scale | $V_{\text{IN}} = A_{\text{INP}} - A_{\text{INN}}$ | -50 | | 50 | mV |
| | Absolute common-mode input voltage ⁽¹⁾ | $(A_{\text{INP}} + A_{\text{INN}}) / 2$ to AGND | -2 | | AVDD | V |
| V_{CM} | Operating common-mode input voltage | $(A_{\text{INP}} + A_{\text{INN}}) / 2$ to AGND | -0.032 | | AVDD - 2.1 | V |
| V_{CMov} | Common-mode overvoltage detection level | $(A_{\text{INP}} + A_{\text{INN}}) / 2$ to AGND | AVDD - 2 | | | V |
| | Hysteresis of the common-mode overvoltage detection level | | | 90 | | mV |
| C_{IN} | Single-ended input capacitance | $A_{\text{INN}} = \text{AGND}$ | | 4 | | pF |
| C_{IND} | Differential input capacitance | | | 2 | | pF |
| R_{IN} | Single-ended input resistance | $A_{\text{INN}} = \text{AGND}$ | | 4.75 | | k Ω |
| R_{IND} | Differential input resistance | | | 4.9 | | k Ω |
| I_{IB} | Input bias current | $A_{\text{INP}} = A_{\text{INN}} = \text{AGND}$, $I_{\text{IB}} = I_{\text{IBP}} + I_{\text{IBN}}$ | -97 | -72 | -57 | μA |
| I_{IO} | Input offset current | | | ± 10 | | nA |
| CMTI | Common-mode transient immunity | | 50 | 100 | | kV/ μs |
| CMRR | Common-mode rejection ratio | $A_{\text{INP}} = A_{\text{INN}}$, $f_{\text{IN}} = 0\text{Hz}$, $V_{\text{CM min}} \leq V_{\text{IN}} \leq V_{\text{CM max}}$ | | -99 | | dB |
| | | $A_{\text{INP}} = A_{\text{INN}}$, f_{IN} from 0.1Hz to 50kHz, $V_{\text{CM min}} \leq V_{\text{IN}} \leq V_{\text{CM max}}$ | | -98 | | |
| PSRR | Power-supply rejection ratio | $A_{\text{INP}} = A_{\text{INN}} = \text{AGND}$, $3.0\text{V} \leq AVDD \leq 5.5\text{V}$, at dc | | -108 | | dB |
| | | $A_{\text{INP}} = A_{\text{INN}} = \text{AGND}$, $3.0\text{V} \leq AVDD \leq 5.5\text{V}$, 10kHz, 100mV ripple | | -107 | | |
| BW | Input bandwidth ⁽²⁾ | AMC1303x0510 | | 430 | | kHz |
| | | AMC1303x0520 | | 800 | | |
| DC ACCURACY | | | | | | |
| DNL | Differential nonlinearity | Resolution: 16 bits | -0.99 | | 0.99 | LSB |
| INL | Integral nonlinearity ⁽³⁾ | Resolution: 16 bits | -4 | ± 1 | 4 | LSB |
| E_{O} | Offset error | Initial, at $T_A = 25^\circ\text{C}$, $A_{\text{INP}} = A_{\text{INN}} = \text{AGND}$ | -50 | ± 2.5 | 50 | μV |
| TCE_{O} | Offset error thermal drift ⁽⁴⁾ | | -1 | ± 0.25 | 1 | $\mu\text{V}/^\circ\text{C}$ |
| E_{G} | Gain error | Initial, at $T_A = 25^\circ\text{C}$ | -0.2% | $\pm 0.005\%$ | 0.2% | |
| TCE_{G} | Gain error thermal drift ⁽⁵⁾ | | -40 | ± 20 | 40 | ppm/ $^\circ\text{C}$ |
| AC ACCURACY | | | | | | |
| SNR | Signal-to-noise ratio | AMC1303x0510, $f_{\text{IN}} = 35\text{Hz}$ | 81 | 84 | | dB |
| | | AMC1303x0520, $f_{\text{IN}} = 35\text{Hz}$ | 79 | 83 | | |
| THD | Total harmonic distortion | $f_{\text{IN}} = 35\text{Hz}$ | | -97 | -86 | dB |
| SFDR | Spurious-free dynamic range | AMC1303x0510, $f_{\text{IN}} = 35\text{Hz}$ | | 96 | | dB |
| | | AMC1303x0520, $f_{\text{IN}} = 35\text{Hz}$ | | 97 | | |

6.9 Electrical Characteristics: AMC1303x05x (continued)

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $AVDD = 3.0\text{V}$ to 5.5V , $DVDD = 2.7\text{V}$ to 5.5V , $A_{INP} = -50\text{mV}$ to 50mV , $A_{INN} = \text{AGND}$, and sinc³ filter with OSR = 256 (unless otherwise noted); typical specifications are at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{V}$, and $DVDD = 3.3\text{V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|--------------------------------|--|------------|-----|-----|------|
| DIGITAL OUTPUTS (CMOS Logic) | | | | | | |
| C_{LOAD} | Output load capacitance | | | 30 | | pF |
| V_{OH} | High-level output voltage | $I_{OH} = -20\mu\text{A}$ | DVDD – 0.1 | | | V |
| | | $I_{OH} = -4\text{mA}$ | DVDD – 0.4 | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 20\mu\text{A}$ | | | 0.1 | V |
| | | $I_{OL} = 4\text{mA}$ | | | 0.4 | |
| POWER SUPPLY | | | | | | |
| I_{AVDD} | High-side supply current | AMC1303x0510, $3.0\text{V} \leq AVDD \leq 3.6\text{V}$ | | 5.4 | 7.3 | mA |
| | | AMC1303x0510, $4.5\text{V} \leq AVDD \leq 5.5\text{V}$ | | 6.0 | 8.0 | |
| | | AMC1303x0520, $3.0\text{V} \leq AVDD \leq 3.6\text{V}$ | | 6.3 | 8.5 | |
| | | AMC1303x0520, $4.5\text{V} \leq AVDD \leq 5.5\text{V}$ | | 7.2 | 9.8 | |
| I_{DVDD} | Controller-side supply current | AMC1303E0510, $2.7\text{V} \leq DVDD \leq 3.6\text{V}$, $C_{LOAD} = 15\text{pF}$ | | 3.3 | 4.5 | mA |
| | | AMC1303E0510, $4.5\text{V} \leq DVDD \leq 5.5\text{V}$, $C_{LOAD} = 15\text{pF}$ | | 3.6 | 5.0 | |
| | | AMC1303M0510, $2.7\text{V} \leq DVDD \leq 3.6\text{V}$, $C_{LOAD} = 15\text{pF}$ | | 3.5 | 4.7 | |
| | | AMC1303M0510, $4.5\text{V} \leq DVDD \leq 5.5\text{V}$, $C_{LOAD} = 15\text{pF}$ | | 3.9 | 5.4 | |
| | | AMC1303E0520, $2.7\text{V} \leq DVDD \leq 3.6\text{V}$, $C_{LOAD} = 15\text{pF}$ | | 4.1 | 5.5 | |
| | | AMC1303E0520, $4.5\text{V} \leq DVDD \leq 5.5\text{V}$, $C_{LOAD} = 15\text{pF}$ | | 4.7 | 6.5 | |
| | | AMC1303M0520, $2.7\text{V} \leq DVDD \leq 3.6\text{V}$, $C_{LOAD} = 15\text{pF}$ | | 4.6 | 6.0 | |
| | | AMC1303M0520, $4.5\text{V} \leq DVDD \leq 5.5\text{V}$, $C_{LOAD} = 15\text{pF}$ | | 5.4 | 7.2 | |

- Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the [Absolute Maximum Ratings](#) table.
- This parameter is the –3dB, second-order, roll-off frequency of the integrated differential input amplifier to consider for antialiasing filter designs.
- Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.

- Offset error drift is calculated using the box method as described by the following equation:
$$TCE_o = \frac{\text{value}_{MAX} - \text{value}_{MIN}}{\text{TempRange}}$$
- Gain error drift is calculated using the box method as described by the following equation:
$$TCE_g(\text{ppm}) = \left(\frac{\text{value}_{MAX} - \text{value}_{MIN}}{\text{value} \times \text{TempRange}} \right) \times 10^6$$

6.10 Electrical Characteristics: AMC1303x25x

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $AVDD = 3.0\text{V}$ to 5.5V , $DVDD = 2.7\text{V}$ to 5.5V , $A\text{INP} = -250\text{mV}$ to 250mV , $A\text{INN} = \text{AGND}$, and sinc³ filter with $\text{OSR} = 256$ (unless otherwise noted); typical specifications are at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{V}$, and $DVDD = 3.3\text{V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|---|---|----------|---------|------------|--------|
| ANALOG INPUTS | | | | | | |
| V_{Clipping} | Differential input voltage before clipping output | $V_{\text{IN}} = A\text{INP} - A\text{INN}$ | | ±320 | | mV |
| FSR | Specified linear differential full-scale | $V_{\text{IN}} = A\text{INP} - A\text{INN}$ | -250 | | 250 | mV |
| | Absolute common-mode input voltage ⁽¹⁾ | $(A\text{INP} + A\text{INN}) / 2$ to AGND | -2 | | AVDD | V |
| V_{CM} | Operating common-mode input voltage | $(A\text{INP} + A\text{INN}) / 2$ to AGND | -0.16 | | AVDD - 2.1 | V |
| V_{CMov} | Common-mode overvoltage detection level | $(A\text{INP} + A\text{INN}) / 2$ to AGND | AVDD - 2 | | | V |
| | Hysteresis of common-mode overvoltage detection level | | | 90 | | mV |
| C_{IN} | Single-ended input capacitance | AINN = AGND | | 2 | | pF |
| C_{IND} | Differential input capacitance | | | 1 | | pF |
| R_{IN} | Single-ended input resistance | AINN = AGND | | 19 | | kΩ |
| R_{IND} | Differential input resistance | | | 22 | | kΩ |
| I_{IB} | Input bias current | $A\text{INP} = A\text{INN} = \text{AGND}$, $I_{\text{IB}} = I_{\text{IBP}} + I_{\text{IBN}}$ | -82 | -60 | -48 | μA |
| I_{IO} | Input offset current | | | ±5 | | nA |
| CMTI | Common-mode transient immunity | | 50 | 100 | | kV/μs |
| CMRR | Common-mode rejection ratio | $A\text{INP} = A\text{INN}$, $f_{\text{IN}} = 0\text{Hz}$, $V_{\text{CM min}} \leq V_{\text{IN}} \leq V_{\text{CM max}}$ | | -98 | | dB |
| | | $A\text{INP} = A\text{INN}$, f_{IN} from 0.1Hz to 50kHz, $V_{\text{CM min}} \leq V_{\text{IN}} \leq V_{\text{CM max}}$ | | -98 | | |
| PSRR | Power-supply rejection ratio | $A\text{INP} = A\text{INN} = \text{AGND}$, $3.0\text{V} \leq AVDD \leq 5.5\text{V}$, at dc | | -97 | | dB |
| | | $A\text{INP} = A\text{INN} = \text{AGND}$, $3.0\text{V} \leq AVDD \leq 5.5\text{V}$, 10kHz, 100mV ripple | | -94.5 | | |
| BW | Input bandwidth ⁽²⁾ | AMC1303x2510 | | 510 | | kHz |
| | | AMC1303x2520 | | 900 | | |
| DC ACCURACY | | | | | | |
| DNL | Differential nonlinearity | Resolution: 16 bits | -0.99 | | 0.99 | LSB |
| INL | Integral nonlinearity ⁽³⁾ | Resolution: 16 bits | -4 | ±1 | 4 | LSB |
| E_{O} | Offset error | Initial, at $T_A = 25^\circ\text{C}$, $A\text{INP} = A\text{INN} = \text{AGND}$ | -100 | ±4.5 | 100 | μV |
| TCE_{O} | Offset error thermal drift ⁽⁴⁾ | | -1 | ±0.15 | 1 | μV/°C |
| E_{G} | Gain error | Initial, at $T_A = 25^\circ\text{C}$ | -0.2% | -0.005% | 0.2% | |
| TCE_{G} | Gain error thermal drift ⁽⁵⁾ | | -40 | ±20 | 40 | ppm/°C |
| AC ACCURACY | | | | | | |
| SNR | Signal-to-noise ratio | AMC1303x2510, $f_{\text{IN}} = 35\text{Hz}$ | 85 | 87 | | dB |
| | | AMC1303x2520, $f_{\text{IN}} = 35\text{Hz}$ | 84.5 | 86.5 | | |
| THD | Total harmonic distortion | AMC1303x2510, $f_{\text{IN}} = 35\text{Hz}$ | | -97 | -86 | dB |
| | | AMC1303x2520, $f_{\text{IN}} = 35\text{Hz}$ | | -101 | -86 | |
| SFDR | Spurious-free dynamic range | $f_{\text{IN}} = 35\text{Hz}$ | | 98 | | dB |

6.10 Electrical Characteristics: AMC1303x25x (continued)

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $AVDD = 3.0\text{V}$ to 5.5V , $DVDD = 2.7\text{V}$ to 5.5V , $A_{INP} = -250\text{mV}$ to 250mV , $A_{INN} = \text{AGND}$, and sinc³ filter with $\text{OSR} = 256$ (unless otherwise noted); typical specifications are at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{V}$, and $DVDD = 3.3\text{V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|--------------------------------|---|------------|-----|-----|------|
| DIGITAL OUTPUTS (CMOS LOGIC) | | | | | | |
| C_{LOAD} | Output load capacitance | | | 30 | | pF |
| V_{OH} | High-level output voltage | $I_{\text{OH}} = -20\mu\text{A}$ | DVDD – 0.1 | | | V |
| | | $I_{\text{OH}} = -4\text{mA}$ | DVDD – 0.4 | | | |
| V_{OL} | Low-level output voltage | $I_{\text{OL}} = 20\mu\text{A}$ | | | 0.1 | V |
| | | $I_{\text{OL}} = 4\text{mA}$ | | | 0.4 | |
| POWER SUPPLY | | | | | | |
| I_{AVDD} | High-side supply current | AMC1303x2510, $3.0\text{V} \leq AVDD \leq 3.6\text{V}$ | | 5.4 | 7.3 | mA |
| | | AMC1303x2510, $4.5\text{V} \leq AVDD \leq 5.5\text{V}$ | | 6.0 | 8.0 | |
| | | AMC1303x2520, $3.0\text{V} \leq AVDD \leq 3.6\text{V}$ | | 6.3 | 8.5 | |
| | | AMC1303x2520, $4.5\text{V} \leq AVDD \leq 5.5\text{V}$ | | 7.2 | 9.8 | |
| I_{DVDD} | Controller-side supply current | AMC1303E2510, $2.7\text{V} \leq DVDD \leq 3.6\text{V}$, $C_{\text{LOAD}} = 15\text{pF}$ | | 3.3 | 4.5 | mA |
| | | AMC1303E2510, $4.5\text{V} \leq DVDD \leq 5.5\text{V}$, $C_{\text{LOAD}} = 15\text{pF}$ | | 3.6 | 5.0 | |
| | | AMC1303M2510, $2.7\text{V} \leq DVDD \leq 3.6\text{V}$, $C_{\text{LOAD}} = 15\text{pF}$ | | 3.5 | 4.7 | |
| | | AMC1303M2510, $4.5\text{V} \leq DVDD \leq 5.5\text{V}$, $C_{\text{LOAD}} = 15\text{pF}$ | | 3.9 | 5.4 | |
| | | AMC1303E2520, $2.7\text{V} \leq DVDD \leq 3.6\text{V}$, $C_{\text{LOAD}} = 15\text{pF}$ | | 4.1 | 5.5 | |
| | | AMC1303E2520, $4.5\text{V} \leq DVDD \leq 5.5\text{V}$, $C_{\text{LOAD}} = 15\text{pF}$ | | 4.7 | 6.5 | |
| | | AMC1303M2520, $2.7\text{V} \leq DVDD \leq 3.6\text{V}$, $C_{\text{LOAD}} = 15\text{pF}$ | | 4.6 | 6.0 | |
| | | AMC1303M2520, $4.5\text{V} \leq DVDD \leq 5.5\text{V}$, $C_{\text{LOAD}} = 15\text{pF}$ | | 5.4 | 7.2 | |

- Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the [Absolute Maximum Ratings](#) table.
- This parameter is the –3dB, second-order, roll-off frequency of the integrated differential input amplifier to consider for antialiasing filter designs.
- Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.

- Offset error drift is calculated using the box method as described by the following equation:

$$TCE_o = \frac{\text{value}_{\text{MAX}} - \text{value}_{\text{MIN}}}{\text{TempRange}}$$

- Gain error drift is calculated using the box method as described by the following equation:

$$TCE_g(\text{ppm}) = \left(\frac{\text{value}_{\text{MAX}} - \text{value}_{\text{MIN}}}{\text{value} \times \text{TempRange}} \right) \times 10^6$$

6.11 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|---|------|-----|------|------|
| f _{CLK} | Internal clock frequency, on the CLKOUT pin of the AMC1303Mx only | AMC1303Mxx10 | 9.6 | 10 | 10.4 | MHz |
| | | AMC1303Mxx20 | 19.2 | 20 | 20.8 | |
| | Internal clock duty cycle ⁽¹⁾ , on the CLKOUT pin of the AMC1303Mx only | | 45% | 50% | 55% | |
| t _h | DOUT hold time after rising edge of CLKOUT | AMC1303Mx, C _{LOAD} = 15pF | 7 | | | ns |
| t _d | DOUT delay time after rising edge of CLKOUT | AMC1303Mx, C _{LOAD} = 15pF | | | 15 | ns |
| t _r | DOUT, CLKOUT rise time | 10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C _{LOAD} = 15pF | | 0.8 | 3.5 | ns |
| | | 10% to 90%, 4.5V ≤ DVDD ≤ 5.5 V, C _{LOAD} = 15pF | | 1.8 | 3.9 | |
| t _f | DOUT, CLKOUT fall time | 90% to 10%, 2.7V ≤ DVDD ≤ 3.6V, C _{LOAD} = 15pF | | 0.8 | 3.5 | ns |
| | | 90% to 10%, 4.5V ≤ DVDD ≤ 5.5V, C _{LOAD} = 15pF | | 1.8 | 3.9 | |
| t _{ASTART} | Analog start-up time | AVDD step to 3.0V with DVDD ≥ 2.7V | | 0.5 | | ms |

(1) Duty cycle values are specified by design.

6.12 Timing Diagrams

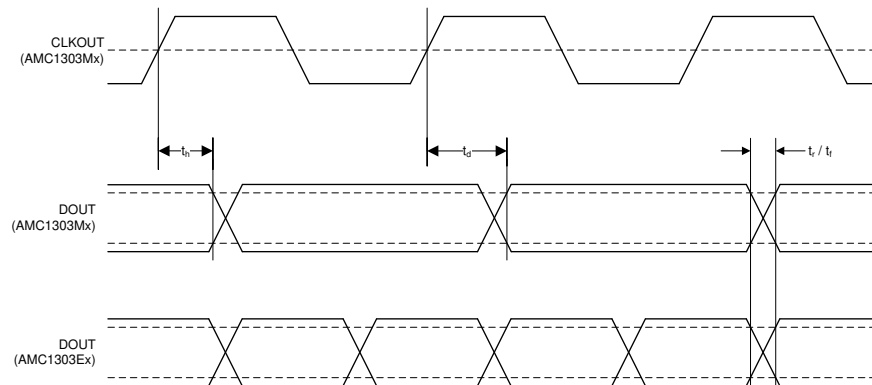


Figure 6-1. AMC1303Mx Digital Interface Timing

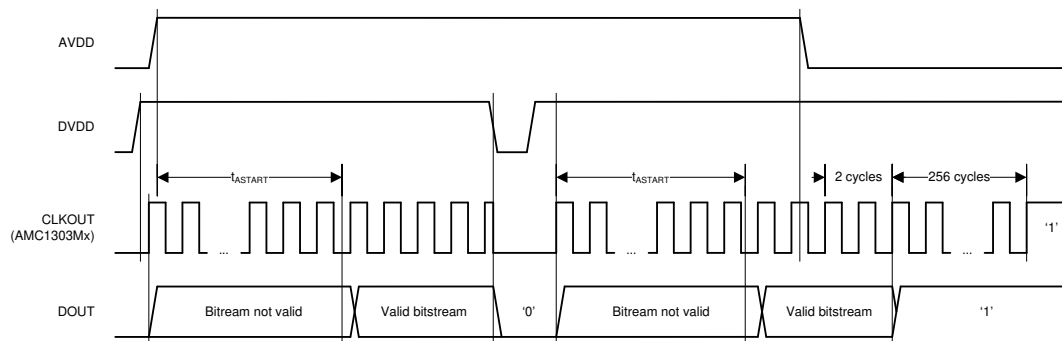


Figure 6-2. Digital Interface Start-Up Timing

6.13 Insulation Characteristics Curves

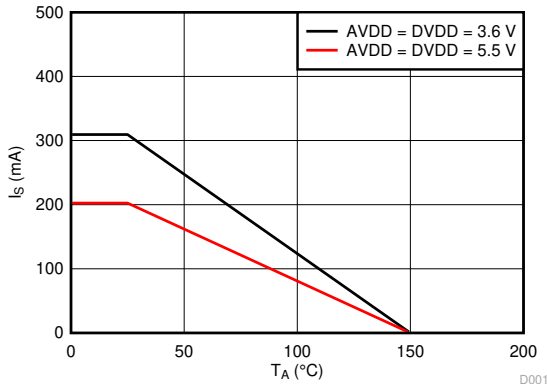


Figure 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE

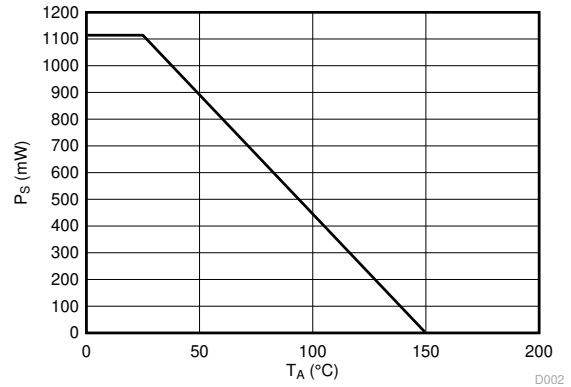
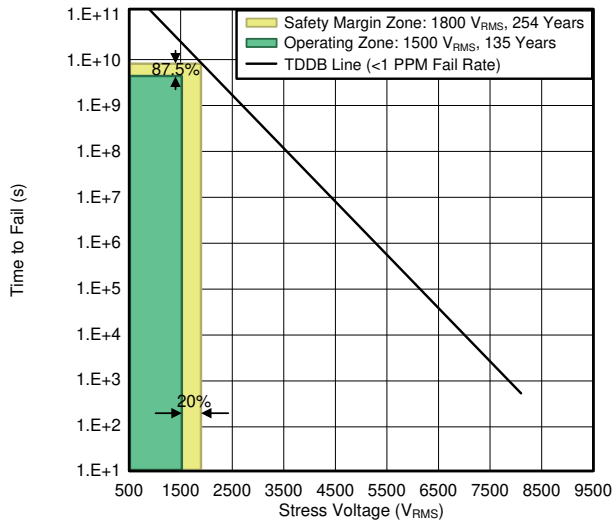


Figure 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V_{RMS}, operating lifetime = 135 years

Figure 6-5. Reinforced Isolation Capacitor Lifetime Projection

6.14 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $AV_{DD} = 5\text{V}$, $DV_{DD} = 3.3\text{V}$, $A_{INP} = -50\text{mV}$ to 50mV (AMC1303x05x) or -250mV to 250mV (AMC1303x25x), $A_{INN} = \text{AGND}$, and sinc³ filter with OSR = 256 (unless otherwise noted)

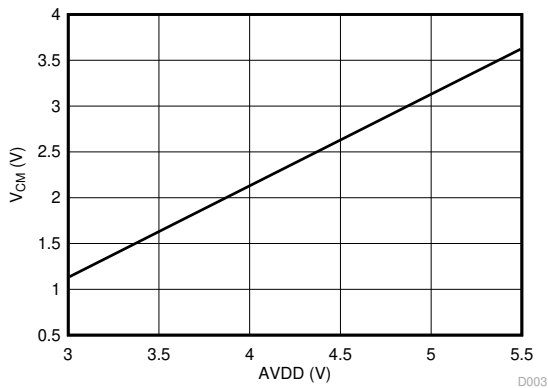


Figure 6-6. Maximum Operating Common-Mode Input Voltage vs High-Side Supply Voltage

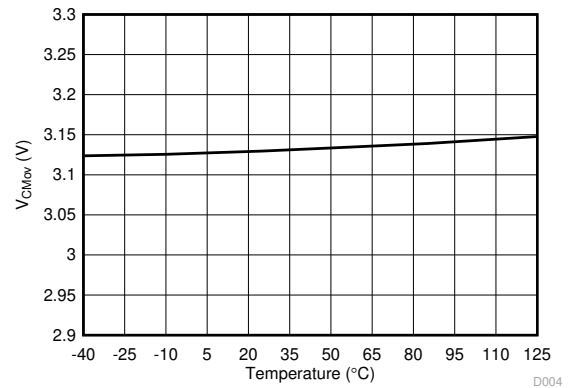


Figure 6-7. Common-Mode Overvoltage Detection Level vs Temperature

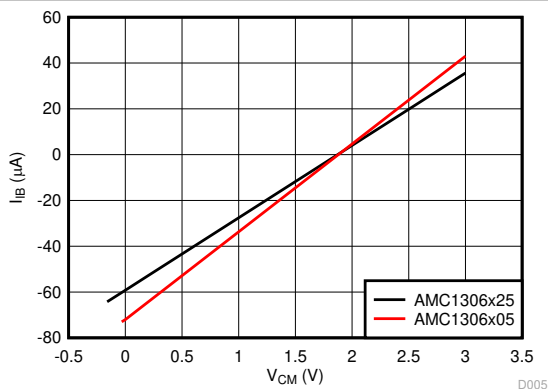


Figure 6-8. Input Bias Current vs Common-Mode Input Voltage

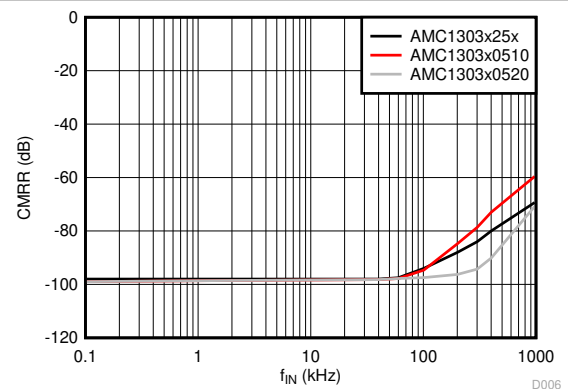


Figure 6-9. Common-Mode Rejection Ratio vs Input Signal Frequency

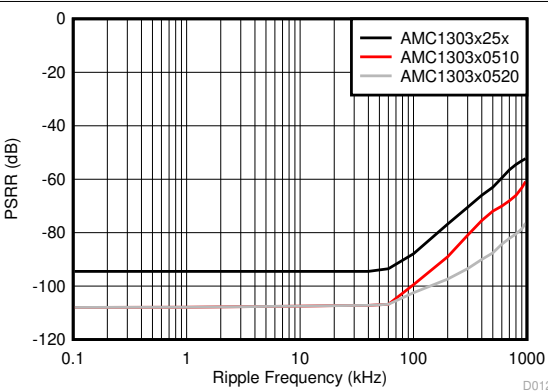


Figure 6-10. Power-Supply Rejection Ratio vs Ripple Frequency

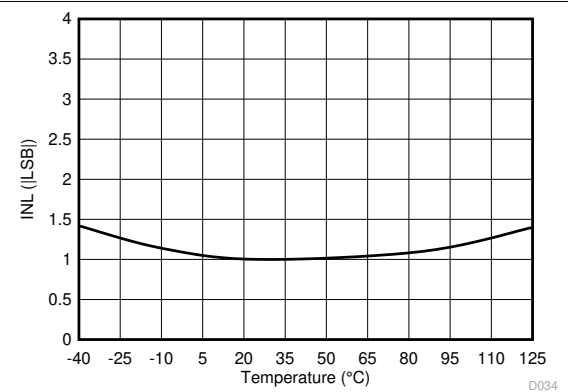


Figure 6-11. Integral Nonlinearity vs Temperature

6.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{V}$, $DVDD = 3.3\text{V}$, $AINP = -50\text{mV}$ to 50mV (AMC1303x05x) or -250mV to 250mV (AMC1303x25x), $AINN = AGND$, and sinc³ filter with OSR = 256 (unless otherwise noted)

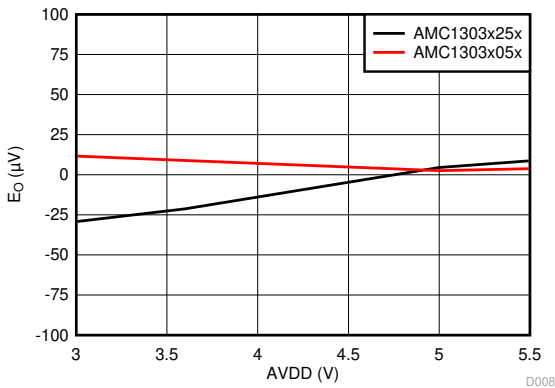


Figure 6-12. Offset Error vs High-Side Supply Voltage

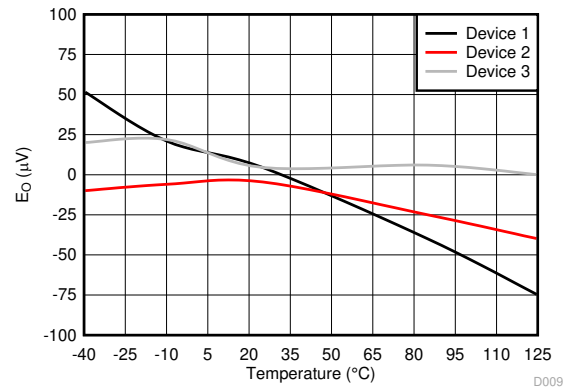


Figure 6-13. Offset Error vs Temperature

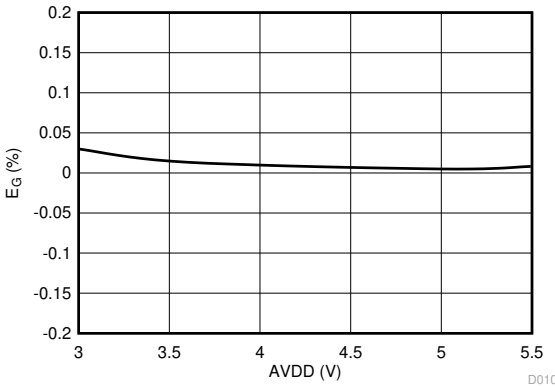


Figure 6-14. Gain Error vs High-Side Supply Voltage

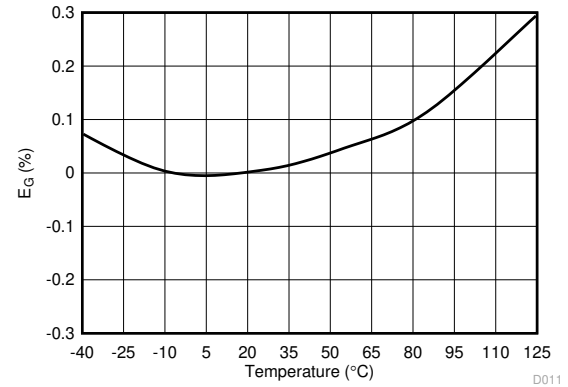


Figure 6-15. Gain Error vs Temperature

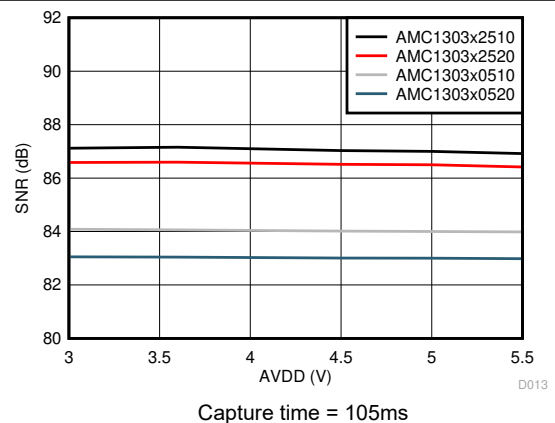


Figure 6-16. Signal-to-Noise Ratio vs High-Side Supply Voltage

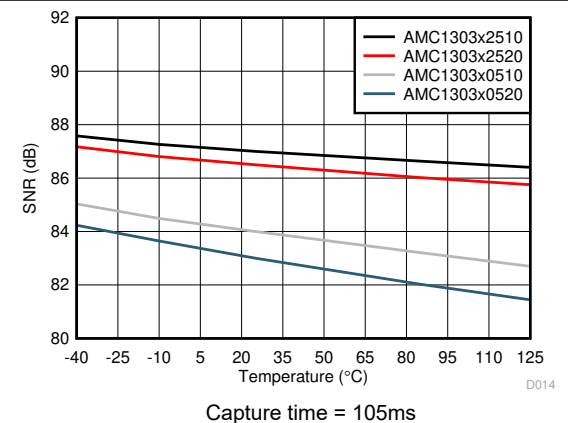


Figure 6-17. Signal-to-Noise Ratio vs Temperature

6.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $AV_{DD} = 5\text{V}$, $DV_{DD} = 3.3\text{V}$, $A_{INP} = -50\text{mV}$ to 50mV (AMC1303x05x) or -250mV to 250mV (AMC1303x25x), $A_{INN} = \text{AGND}$, and sinc³ filter with OSR = 256 (unless otherwise noted)

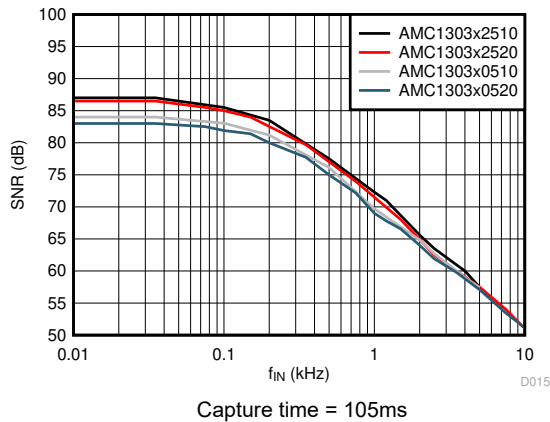


Figure 6-18. Signal-to-Noise Ratio vs Input Signal Frequency

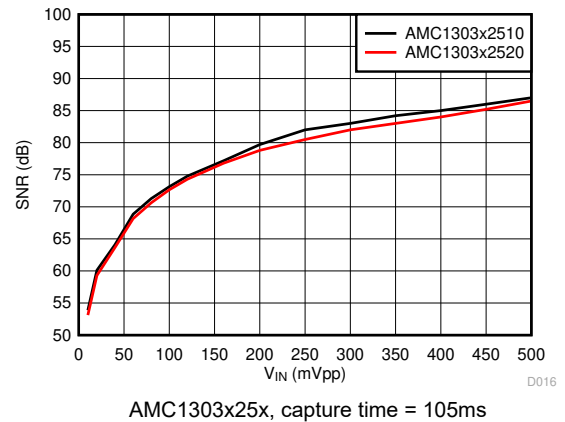


Figure 6-19. Signal-to-Noise Ratio vs Input Signal Amplitude

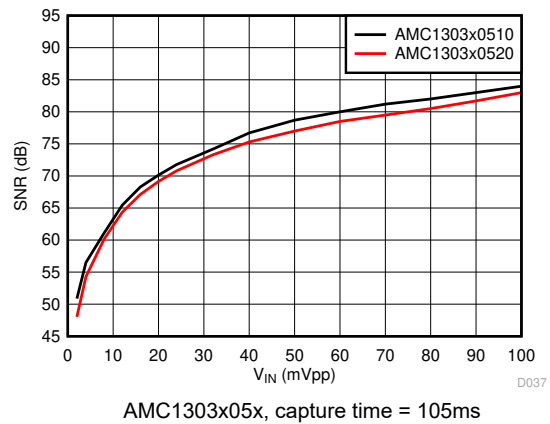


Figure 6-20. Signal-to-Noise Ratio vs Input Signal Amplitude

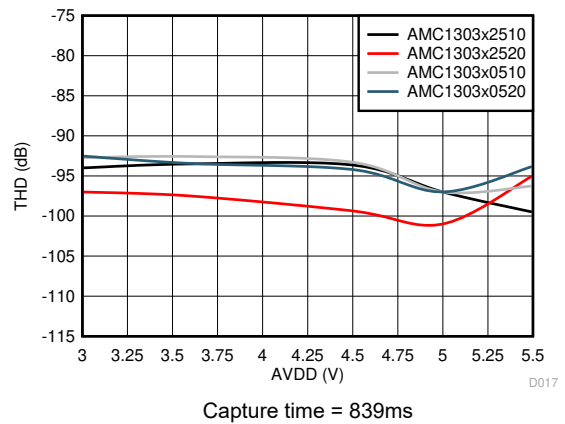


Figure 6-21. Total Harmonic Distortion vs High-Side Supply Voltage

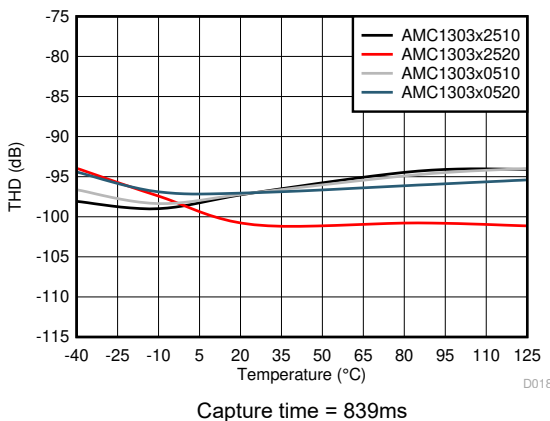


Figure 6-22. Total Harmonic Distortion vs Temperature

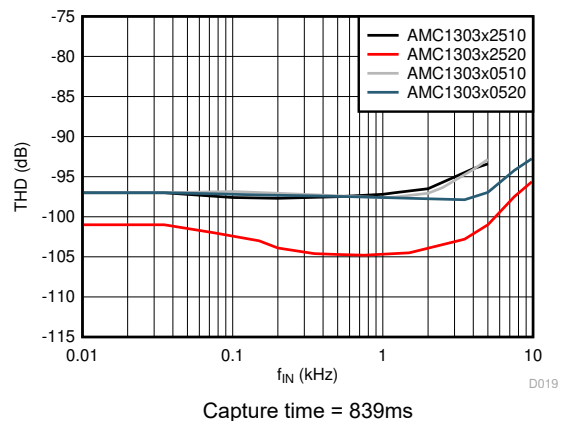
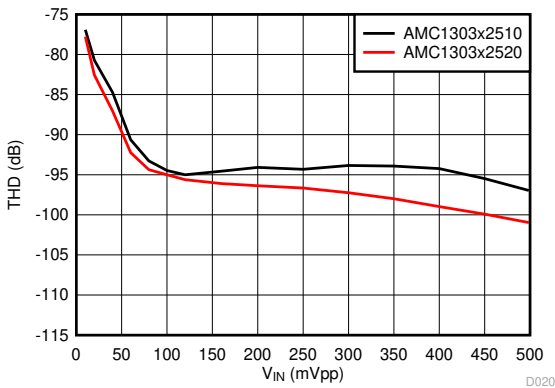


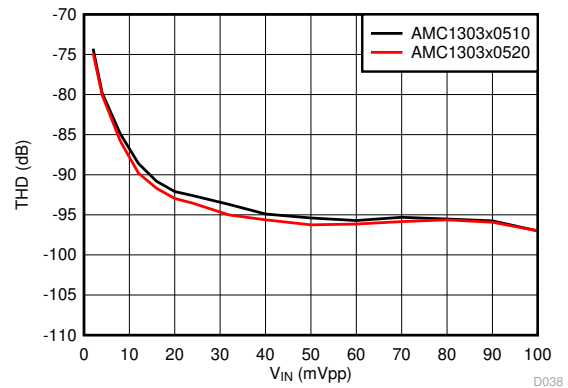
Figure 6-23. Total Harmonic Distortion vs Input Signal Frequency

6.14 Typical Characteristics (continued)

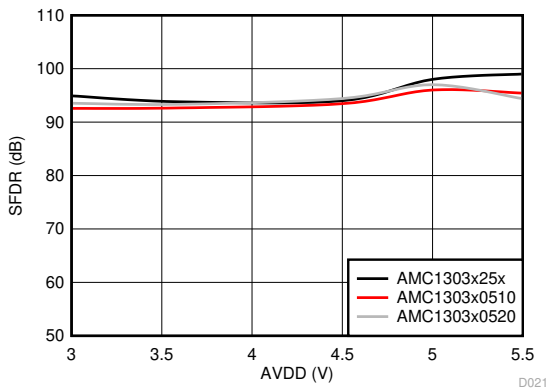
at $T_A = 25^\circ\text{C}$, $AV_{DD} = 5\text{V}$, $DV_{DD} = 3.3\text{V}$, $A_{INP} = -50\text{mV}$ to 50mV (AMC1303x05x) or -250mV to 250mV (AMC1303x25x), $A_{INN} = \text{AGND}$, and sinc³ filter with OSR = 256 (unless otherwise noted)



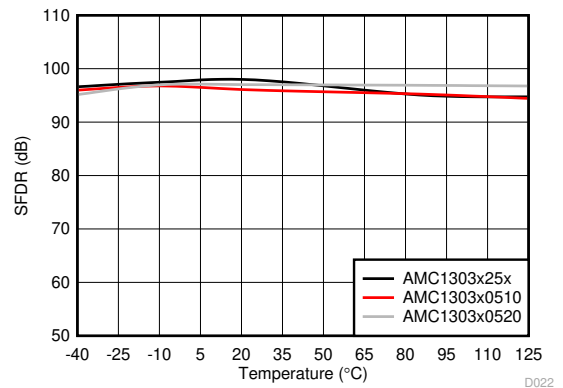
AMC1303x25x, capture time = 839ms
Figure 6-24. Total Harmonic Distortion vs Input Signal Amplitude



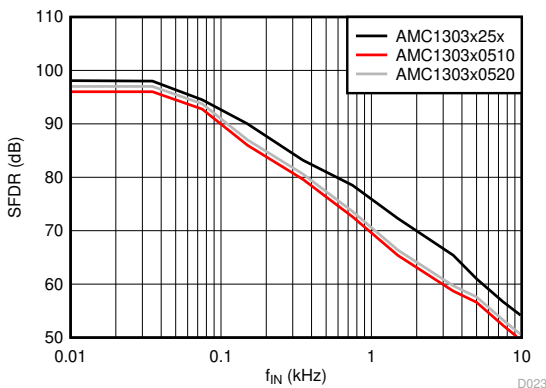
AMC1303x05x, capture time = 839ms
Figure 6-25. Total Harmonic Distortion vs Input Signal Amplitude



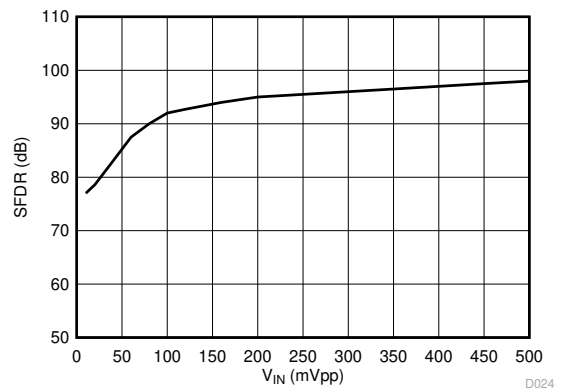
Capture time = 105ms
Figure 6-26. Spurious-Free Dynamic Range vs High-Side Supply Voltage



Capture time = 105ms
Figure 6-27. Spurious-Free Dynamic Range vs Temperature



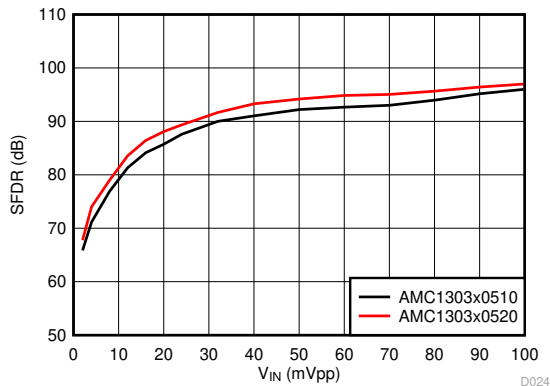
Capture time = 105ms
Figure 6-28. Spurious-Free Dynamic Range vs Input Signal Frequency



AMC1303x25x, capture time = 105ms
Figure 6-29. Spurious-Free Dynamic Range vs Input Signal Amplitude

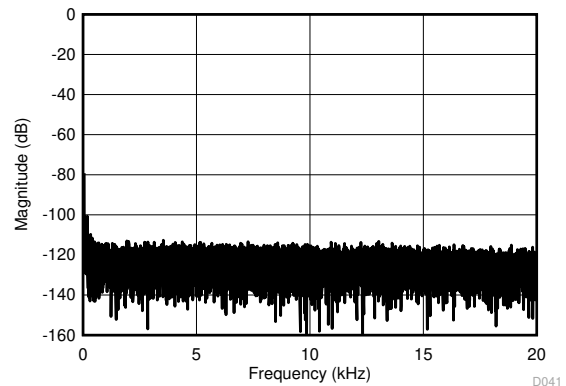
6.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $AV_{DD} = 5\text{V}$, $DV_{DD} = 3.3\text{V}$, $A_{INP} = -50\text{mV}$ to 50mV (AMC1303x05x) or -250mV to 250mV (AMC1303x25x), $A_{INN} = \text{AGND}$, and sinc³ filter with OSR = 256 (unless otherwise noted)



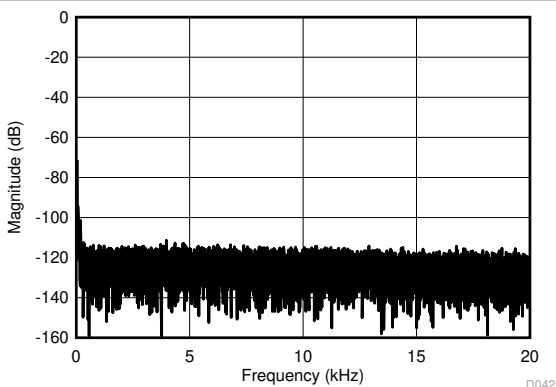
AMC1303x05x, capture time = 105ms

Figure 6-30. Spurious-Free Dynamic Range vs Input Signal Amplitude



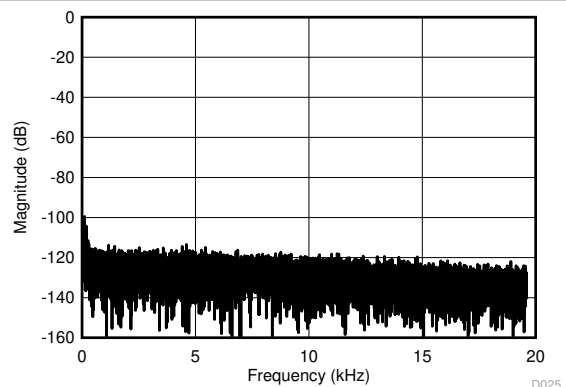
AMC1303x0510, capture time = 839ms, $V_{IN} = 100\text{mV}_{PP}$

Figure 6-31. Frequency Spectrum With 35Hz Input Signal



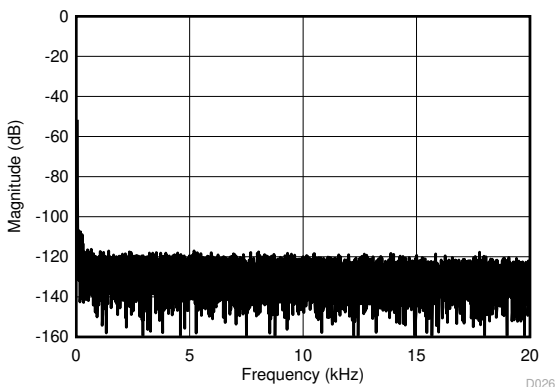
AMC1303x0520, capture time = 839ms, $V_{IN} = 100\text{mV}_{PP}$

Figure 6-32. Frequency Spectrum With 35Hz Input Signal



AMC1303x2510, capture time = 839ms, $V_{IN} = 500\text{mV}_{PP}$

Figure 6-33. Frequency Spectrum With 35Hz Input Signal



AMC1303x2520, capture time = 839ms, $V_{IN} = 500\text{mV}_{PP}$

Figure 6-34. Frequency Spectrum With 35Hz Input Signal

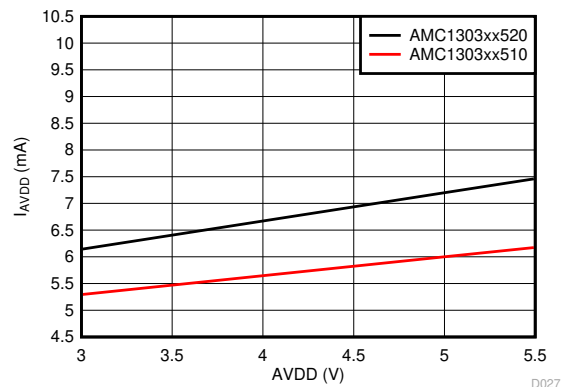


Figure 6-35. High-Side Supply Current vs High-Side Supply Voltage

6.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{V}$, $DVDD = 3.3\text{V}$, $AINP = -50\text{mV}$ to 50mV (AMC1303x05x) or -250mV to 250mV (AMC1303x25x), $AINN = \text{AGND}$, and sinc³ filter with $\text{OSR} = 256$ (unless otherwise noted)

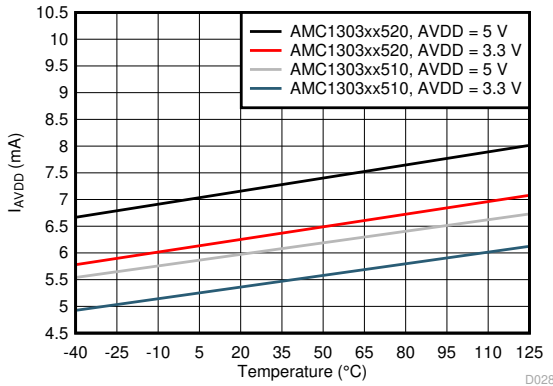


Figure 6-36. High-Side Supply Current vs Temperature

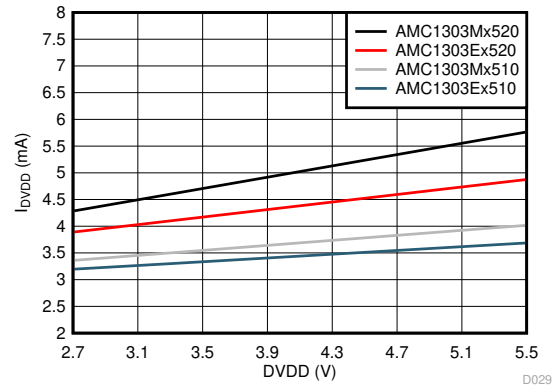


Figure 6-37. Controller-Side Supply Current vs Controller-Side Supply Voltage

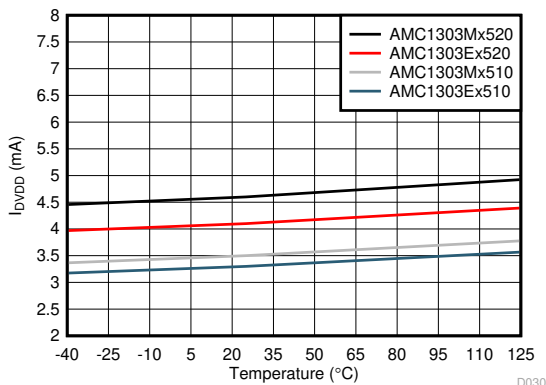


Figure 6-38. Controller-Side Supply Current vs Temperature

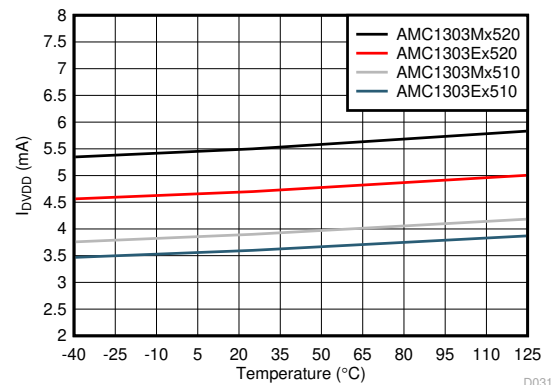


Figure 6-39. Controller-Side Supply Current vs Temperature

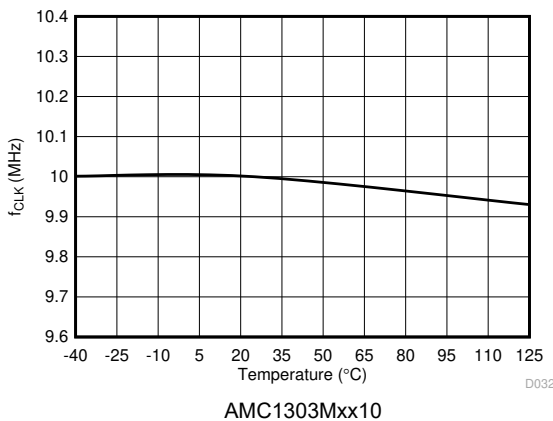


Figure 6-40. Output Clock Frequency vs Temperature

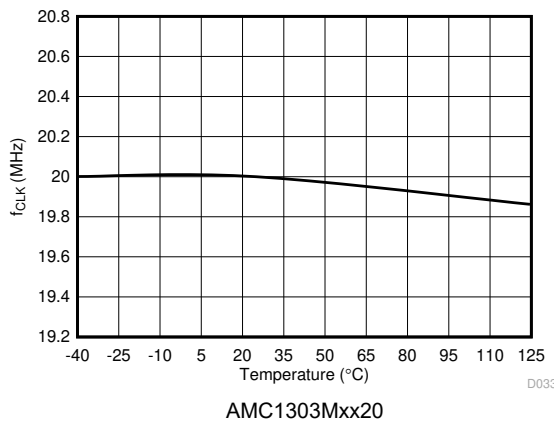


Figure 6-41. Output Clock Frequency vs Temperature

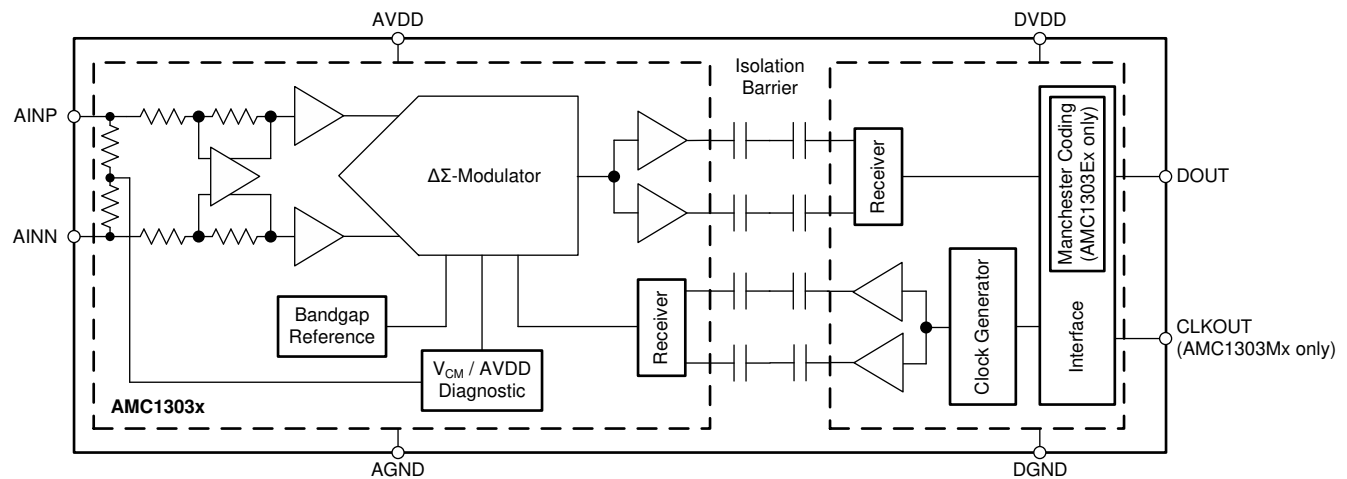
7 Detailed Description

7.1 Overview

The analog input stage of the AMC1303 is a fully differential amplifier feeding the switched-capacitor input of a second-order, delta-sigma ($\Delta\Sigma$) modulator stage that digitizes the input signal into a 1-bit output stream. The isolated data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the internally-generated clock at the CLKOUT pin (active on AMC1303Mx derivatives only) with a frequency as specified in the [Switching Characteristics](#) table. The time average of this serial bit-stream output is proportional to the analog input voltage.

The [Functional Block Diagram](#) section shows a detailed block diagram of the AMC1303. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The SiO₂-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application note](#), available for download at www.ti.com. The extended clock frequency of 20MHz on the AMC1303xxx20 supports faster control loops and higher performance levels compared to the other solutions available on the market.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The AMC1303 incorporates a front-end circuitry that contains a differential amplifier and sampling stage, followed by a $\Delta\Sigma$ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 for devices with a specified input voltage range of $\pm 250\text{mV}$ (for the AMC1303x25x), or to a factor of 20 in devices with a $\pm 50\text{mV}$ input voltage range (for the AMC1303x05x), resulting in a differential input resistance of $4.9\text{k}\Omega$ (for the AMC1303x05x) or $22\text{k}\Omega$ (for the AMC1303x25x).

For reduced offset and offset drift, the differential amplifier is chopper-stabilized with the switching frequency set at 625kHz . Figure 7-1 shows that the switching frequency generates a spur.

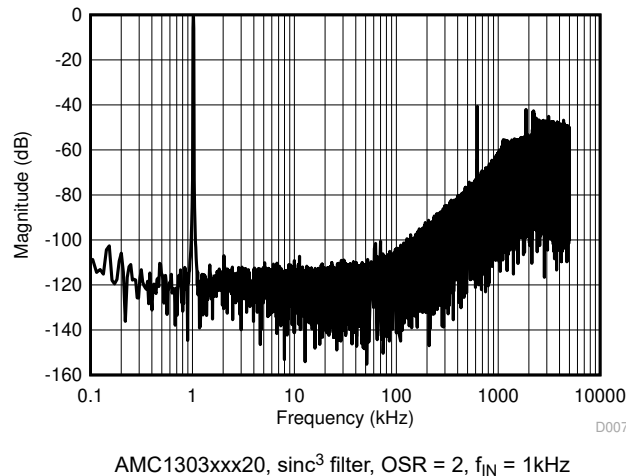


Figure 7-1. Quantization Noise Shaping

Consider the input resistance of the AMC1303 in designs with high-impedance signal sources that cause degradation of gain and offset specifications. The importance of this effect, however, depends on the desired system performance. Additionally, the input bias current caused by the internal common-mode voltage at the output of the differential amplifier causes an offset that is dependent on the actual amplitude of the input signal. See the *Isolated Voltage Sensing* section for more details on reducing these effects.

There are two restrictions on the analog input signals (AINP and AINN). First, if the input voltage exceeds the range $\text{AGND} - 6\text{V}$ to $\text{AVDD} + 0.5\text{V}$, limit the input current to 10mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are specified only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is $\pm 250\text{mV}$ (for the AMC1303x25x) or $\pm 50\text{mV}$ (for the AMC1303x05x), and within the specified input common-mode voltage range.

7.3.2 Modulator

The modulator implemented in the AMC1303 (such as the one conceptualized in Figure 7-2) is a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are subtracted, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is subtracted from the input signal V_{IN} and the output of the first integrator V_2 . Depending on the polarity of the resulting voltage V_4 , the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage V_5 , causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

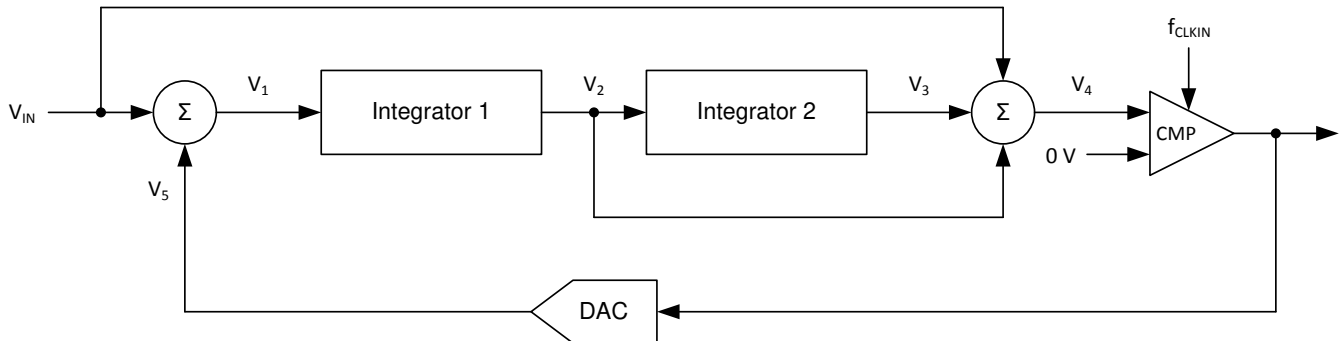


Figure 7-2. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies; see Figure 7-1. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families [TMS320F2807x](#) and [TMS320F2837x](#) offer a suitable programmable, hardwired filter structure called a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1303 family. Also, SD24_B converters on the [MSP430F677x](#) microcontrollers offer a path to directly access the integrated sinc-filters, thus offering a system-level solution for multichannel, isolated current sensing. An additional option using an appropriate application-specific device, such as the [AMC1210](#) (a four-channel digital sinc-filter). Alternatively, use a field-programmable gate array (FPGA) to implement the filter.

7.3.3 Isolation Channel Signal Transmission

The AMC1303 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the capacitive SiO₂-based isolation barrier. The transmitter modulates the bitstream at TX IN in Figure 7-3 with an internally generated, 480MHz carrier across the isolation barrier to represent a digital zero and sends a *no signal* to represent the digital one. The receiver demodulates the signal after advanced signal conditioning and produces the output. The symmetrical design of each isolation channel improves the CMTI performance and reduces the radiated emissions caused by the high-frequency carrier. Figure 7-3 shows a block diagram of an isolation channel integrated in the AMC1303.

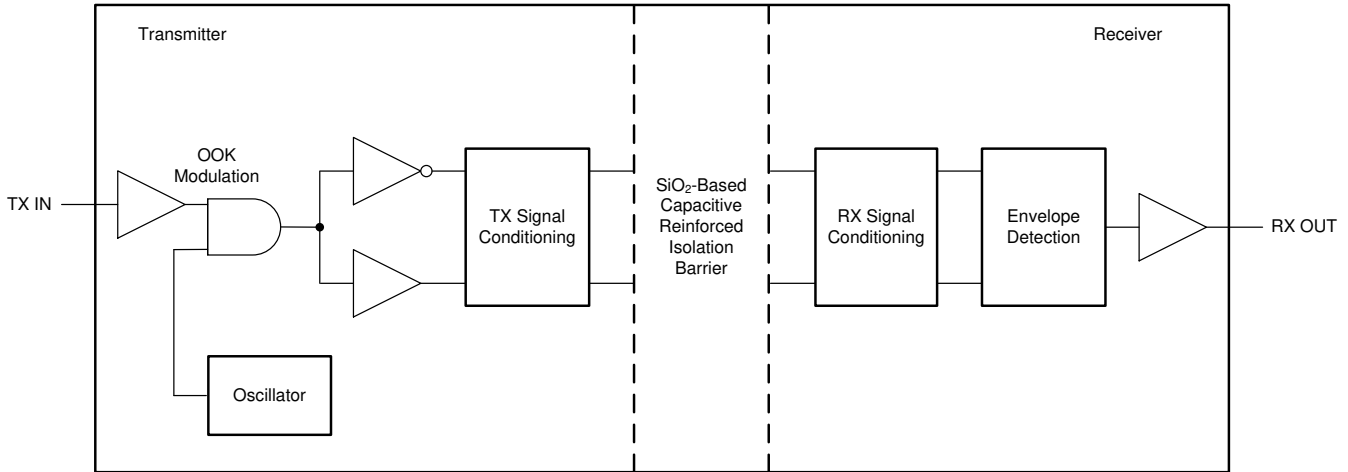


Figure 7-3. Block Diagram of an Isolation Channel

Figure 7-4 shows the concept of the on-off keying scheme.

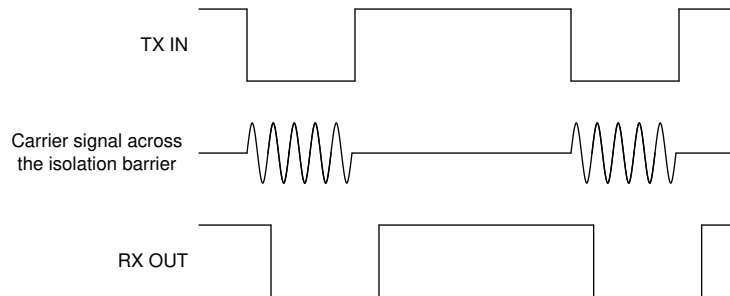


Figure 7-4. OOK-Based Modulation Scheme

7.3.4 Digital Output

A differential input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 250mV (for the AMC1303x25x) or 50 mV (for the AMC1303x05x) produces a stream of ones and zeros that are high 89.06% of the time. With 16 bits of resolution on the decimation filter, that percentage ideally corresponds to code 58368. A differential input of –250mV (–50mV for the AMC1303x05x) produces a stream of ones and zeros that are high 10.94% of the time and ideally results in code 7168 with a 16-bit resolution decimation filter. These input voltages are also the specified linear ranges of the different AMC1303 versions with performance as specified in this document. If the input voltage value exceeds these ranges, the output of the modulator shows nonlinear behavior where the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –320mV (–64mV for the AMC1303x05x) or with a stream of only ones with an input greater than or equal to 320mV (64mV for the AMC1303x05x). In this case, however, the AMC1303 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the [Fail-Safe Output](#) section for more details). [Figure 7-5](#) shows the input voltage versus the output modulator signal.

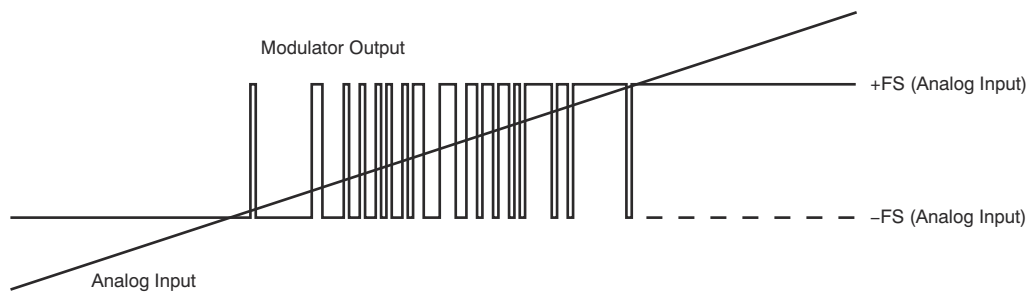


Figure 7-5. Analog Input versus AMC1303 Modulator Output

[Equation 1](#) calculates the density of ones in the output bitstream for any input voltage value (with the exception of a full-scale input signal, as described in the [Section 7.4.2](#) section):

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

The AMC1303 internally generates the clock signal required for the modulator. This clock is provided externally at the CLKOUT pin on AMC1303Mx devices only. For more details, see the [Switching Characteristics](#) section.

7.3.5 Manchester Coding Feature

The AMC1303Ex offers the IEEE 802.3-compliant Manchester-coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. A Manchester-coded bitstream is free of dc components. The Manchester coding combines the clock and data information using exclusive or (XOR) logical operation. [Figure 7-6](#) shows the resulting bitstream.

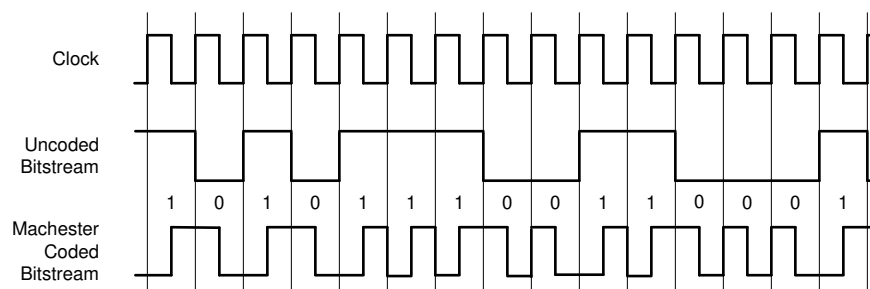


Figure 7-6. Manchester-Coded Output of the AMC1303Ex

7.4 Device Functional Modes

7.4.1 Fail-Safe Output

In the case of a missing high-side supply voltage AVDD, the output of the $\Delta\Sigma$ modulator is not defined and can cause a system malfunction. In systems with high safety requirements, this behavior is not acceptable. Therefore, the AMC1303 implements a fail-safe output function that pulls the DOUT and CLKOUT outputs (AMC1303Mx only) to a steady-state logic 1 in case of a missing AVDD; see [Figure 6-2](#).

Similarly, as also shown in [Figure 7-7](#), if the common-mode voltage of the input reaches or exceeds the specified common-mode overvoltage detection level V_{CMov} as defined in the [Electrical Characteristics](#) table, the AMC1303 generates a steady-state bitstream of logic 1's at the DOUT output.

In both cases, the steady-state logic 1 occurs on the DOUT output with a delay of two clock cycles after the event of either exceeded common-mode input voltage or missing AVDD. Another 256 clock cycles are required for the CLKOUT pin of the AMC1303Mx to be held at logic 1.

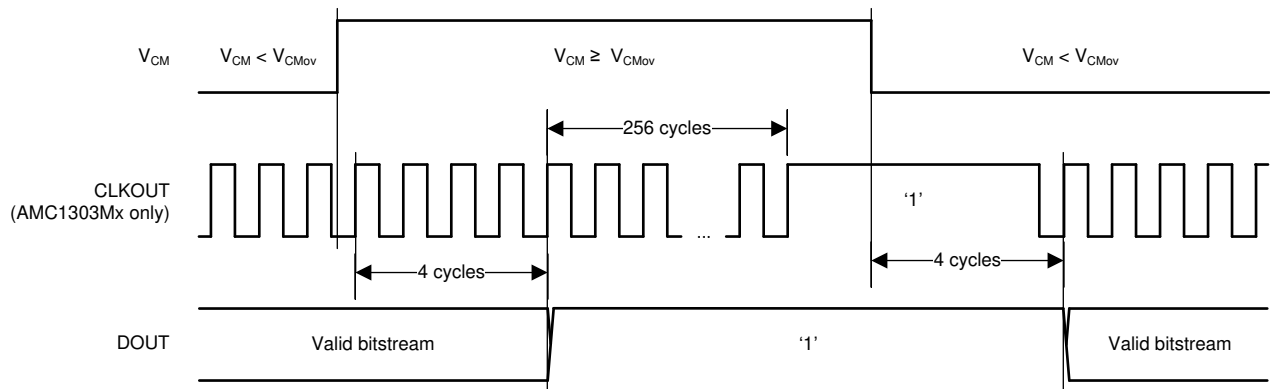


Figure 7-7. Fail-Safe Output of the AMC1303

7.4.2 Output Behavior in Case of a Full-Scale Input

When an input signal is applied to the AMC1303 that exceeds the clipping voltage ($|V_{IN}| \geq |V_{Clipping}|$), the AMC1303 outputs a bitstream as shown in [Figure 7-8](#). A zero or one is generated every 128th clock cycle depending on the actual polarity of the signal being sensed. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.

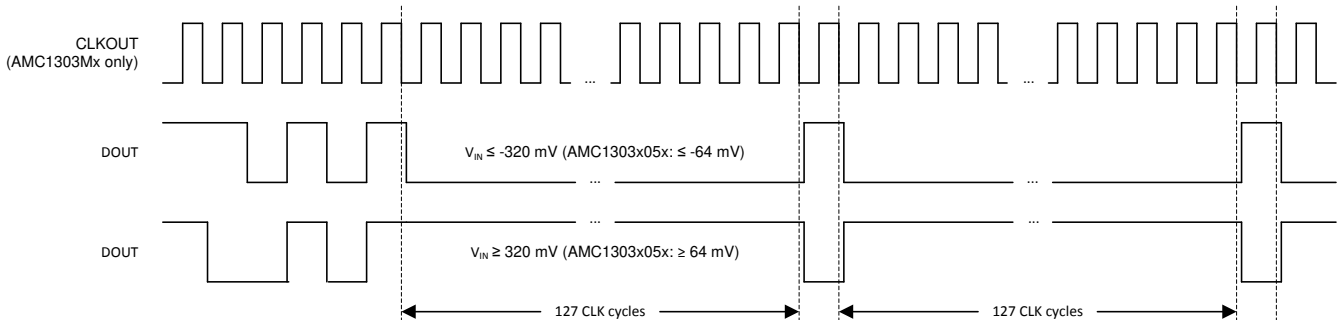


Figure 7-8. Overrange Output of the AMC1303

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, shown in Equation 2, built with minimal effort and hardware, is a sinc³-type filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is done with a sinc³ filter with an oversampling ratio (OSR) of 256 and an output word size of 16 bits.

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 8-1 shows the ENOB of the AMC1303 with different oversampling ratios. In this document, Equation 3 calculates this number from the SINAD by using the following equation:

$$\text{SINAD} = 1.76 + 6.02\text{dB} \times \text{ENOB} \quad (3)$$

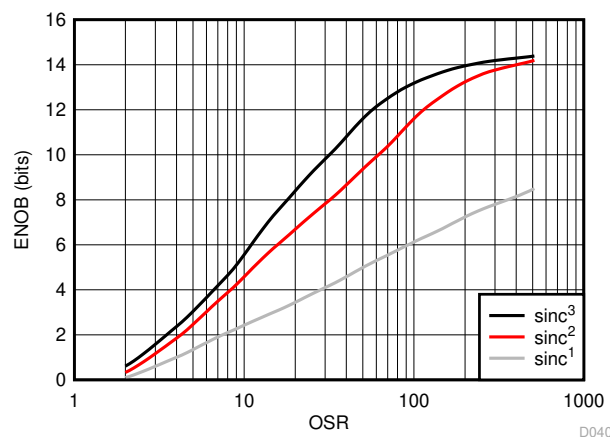


Figure 8-1. Measured Effective Number of Bits versus Oversampling Ratio

An example code for implementing a sinc³ filter in an FPGA is discussed in the [Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications](#) application note, available for download at www.ti.com.

8.2 Typical Applications

8.2.1 Frequency Inverter Application

Isolated $\Delta\Sigma$ modulators are widely used in frequency inverter designs because of the device high ac and dc performance. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), and other industrial applications.

Figure 8-2 shows a simplified schematic of the AMC1303Mx in a typical frequency inverter application as used in industrial motor drives with shunt resistors (R_{SHUNT}) used for current sensing. Depending on the system design, either all three or only two motor phase currents are sensed.

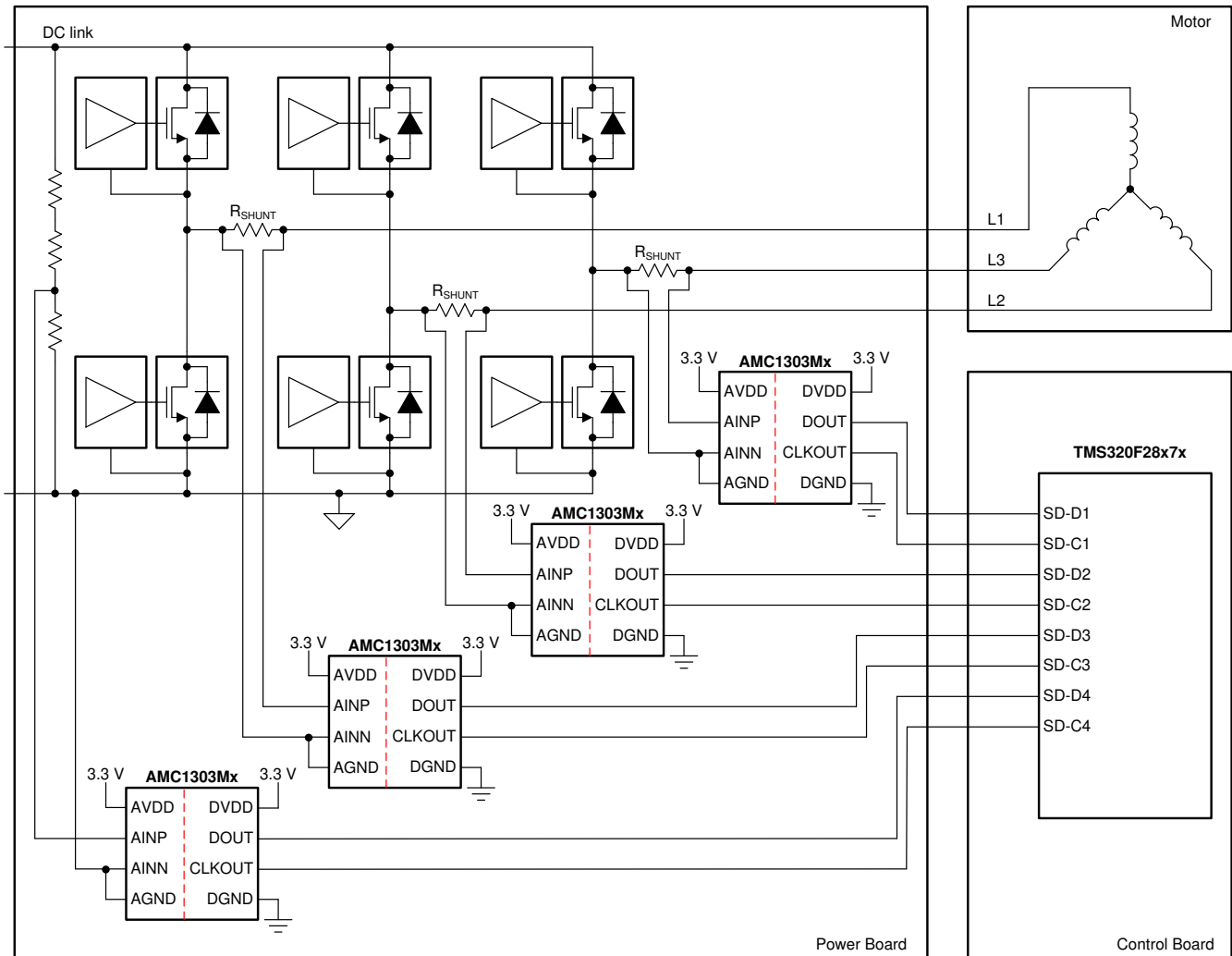


Figure 8-2. Simplified Diagram of the AMC1303Mx in a Frequency Inverter Application

Figure 8-3 shows how the Manchester-coded bitstream output of the AMC1303Ex minimizes the wiring efforts of the connection between the power and the control board. This bitstream output also allows the clock to be generated locally on the power board without the having to adjust the propagation delay time of each DOUT connection to fulfill the setup and hold time requirements of the microcontroller.

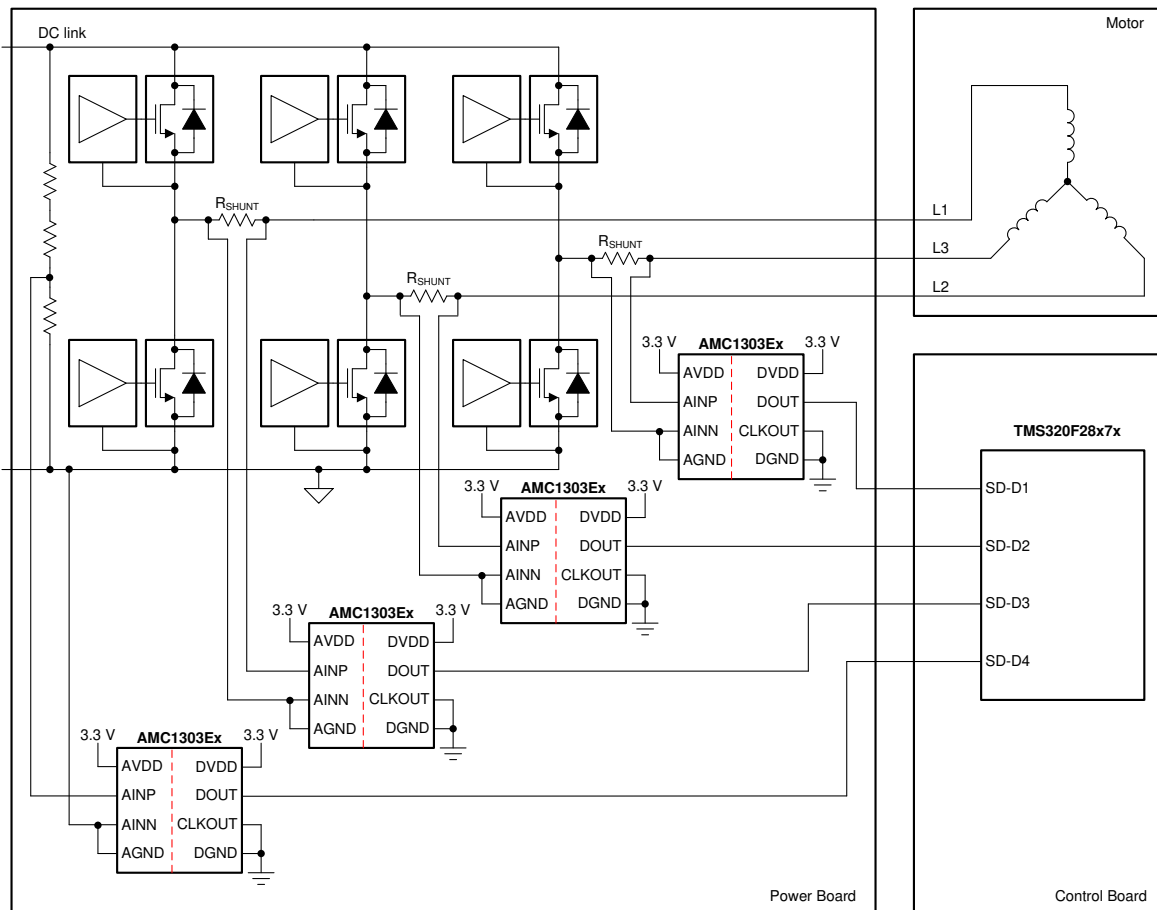


Figure 8-3. Simplified Diagram of the AMC1303Ex in a Frequency Inverter Application

In both examples shown previously, an additional fourth AMC1303 is used to support isolated voltage sensing of the dc link. This high voltage is reduced using a resistive divider and is sensed by the device across a smaller resistor. The value of this resistor degrades the performance of the measurement, as described in the [Isolated Voltage Sensing](#) section.

8.2.1.1 Design Requirements

Table 8-1 lists the parameters for the typical application in the [Frequency Inverter Application](#) section.

Table 8-1. Design Requirements

| PARAMETER | VALUE |
|---|---|
| High-side supply voltage | 3.3V or 5V |
| Low-side supply voltage | 3.3V or 5V |
| Voltage drop across the shunt for a linear response | AMC1303x25x: $\pm 250\text{mV}$ (maximum) |
| | AMC1303x05x: $\pm 50\text{mV}$ (maximum) |

8.2.1.2 Detailed Design Procedure

The high-side power supply (AVDD) for the AMC1303 device is derived from the power supply of the upper gate driver. Further details are provided in the [Power Supply Recommendations](#) section.

The floating ground reference (AGND) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1303 (AINN). If a four-pin shunt is used, the inputs of the device are connected to the inner leads and AGND is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT} :

- Make sure the voltage drop caused by the nominal current range does not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250\text{mV}$
- Make sure the voltage drop caused by the maximum allowed overcurrent does not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

The typically recommended RC filter in front of a $\Delta\Sigma$ modulator to improve signal-to-noise performance of the signal path is not required for the AMC1303. By design, the input bandwidth of the analog front-end of the device is limited as specified in the [Electrical Characteristics](#) table.

For modulator output bitstream filtering, use a device from TI's [TMS320F2807x](#) family of low-cost microcontrollers (MCUs) or [TMS320F2837x](#) family of dual-core MCUs. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one fast response path for overcurrent detection.

8.2.1.3 Application Curves

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter in case of a step-signal at the input of the modulator depends on the order; that is, a sinc³ filter requires three data updates for full settling (with $f_{DATA} = f_{CLK} / OSR$). Therefore, for overcurrent protection, sinc² filters with a lower OSR are a better choice. [Figure 8-4](#) and [Figure 8-5](#) compare the settling times of different filter orders.

The delay time of a sinc filter with a continuous signal is half the settling time.

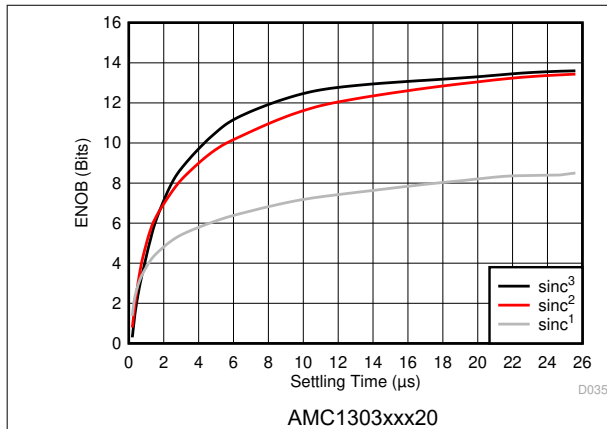


Figure 8-4. Measured Effective Number of Bits versus Settling Time

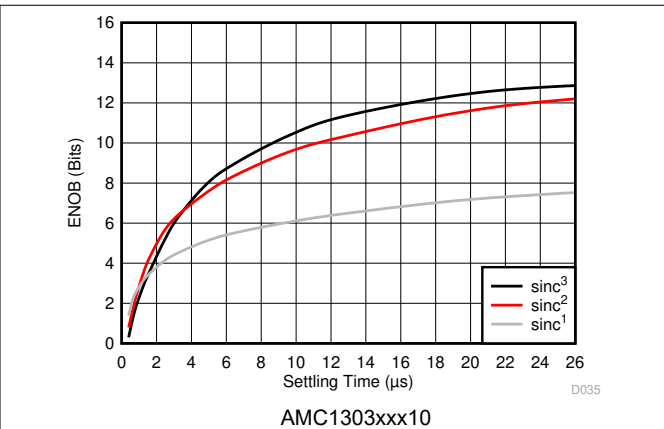


Figure 8-5. Measured Effective Number of Bits versus Settling Time

8.2.2 Isolated Voltage Sensing

The AMC1303 is optimized for usage in current-sensing applications using low-resistance shunts. However, the device is also suitable for isolated voltage-sensing applications as long as the effect of the input bias current is considered. For best performance, use the $\pm 250\text{mV}$ versions of the device (AMC1303x25xx) in this case.

Figure 8-6 shows a simplified circuit typically used in high-voltage-sensing applications. The high value resistors (R1 and R2) are used as voltage dividers and dominate the current value definition. The resistance of the sensing resistor R3 is chosen to meet the input voltage range of the AMC1303. This resistor and the differential input resistance of the AMC1303x25x is $22\text{k}\Omega$ also create a voltage divider that results in an additional gain error. With the assumption of R1, R2, and R_{IND} having a considerably higher value than R3, the resulting total gain error is estimated using Equation 4, with E_G being the gain error of the AMC1303.

$$|E_{\text{Gtot}}| = |E_G| + \frac{R3}{R_{\text{IN}}} \quad (4)$$

This gain error is minimized during the initial system-level gain calibration procedure.

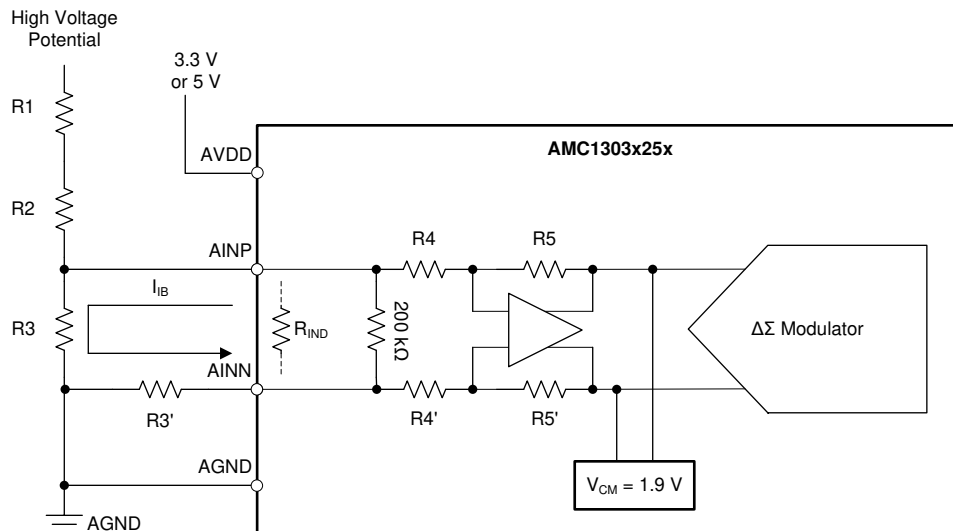


Figure 8-6. Using the AMC1303x25x for Isolated Voltage Sensing

8.2.2.1 Design Requirements

Table 8-2 lists the parameters for the typical application in the *Isolated Voltage Sensing* section.

Table 8-2. Design Requirements

| PARAMETER | VALUE |
|---|---|
| High-side supply voltage | 3.3V or 5V |
| Low-side supply voltage | 3.3V or 5V |
| Voltage drop across the resistor R3 for a linear response | AMC1303x25x: $\pm 250\text{mV}$ (maximum) |

8.2.2.2 Detailed Design Procedure

As indicated in Figure 8-6, the output of the integrated differential amplifier is internally biased to a common-mode voltage of 1.9V . This voltage results in a bias current I_B through the resistive network R4 and R5 (or R4' and R5') used for setting the gain of the amplifier. The value range of this current is specified in the *Electrical Characteristics* table. This bias current generates additional offset error that depends on the value of the resistor

R3. Because the value of this bias current depends on the actual common-mode amplitude of the input signal (as illustrated in Figure 8-7), the initial system offset calibration does not minimize the effect. Therefore, in systems with high accuracy requirements, use a series resistor at the negative input (AINN) of the AMC1303 with a value equal to the shunt resistor R3 (that is, $R3' = R3$ in Figure 8-6) to eliminate the effect of the bias current.

This additional series resistor ($R3'$) influences the gain error of the circuit. The effect is calculated using Equation 5 with $R5 = R5' = 50k\Omega$ and $R4 = R4' = 12.5k\Omega$ for the AMC1303x25x.

$$E_G(\%) = \left(1 - \frac{R4}{R4' + R3'} \right) \times 100\% \tag{5}$$

8.2.2.3 Application Curve

Figure 8-7 shows the dependency of the input bias current on the common-mode voltage at the input of the AMC1303x25x.

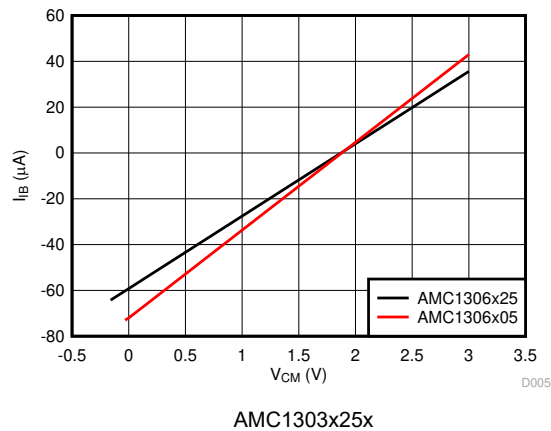


Figure 8-7. Input Current vs Input Common-Mode Voltage

8.2.3 Best Design Practices

Do not leave the inputs of the AMC1303 unconnected (floating) when the device is powered up. If both modulator inputs are left floating, the input bias current drives these inputs to the output common-mode voltage of the differential amplifier of approximately 1.9V. If that voltage is above the specified input common-mode range, the gain of the differential amplifier diminishes and the modulator outputs a bitstream resembling a zero differential input voltage.

8.3 Power Supply Recommendations

In a typical frequency-inverter application, the device high-side power supply (AVDD) is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, use a Zener diode to limit the voltage to 5V or 3.3V ($\pm 10\%$). Alternatively, use a low-cost, low-drop regulator (LDO), for example the LM317-N, to adjust the supply voltage level and minimize noise on the power-supply node. Use a 0.1 μ F, low-ESR decoupling capacitor to filter this power-supply path. Place this capacitor (C2 in Figure 8-8) as close as possible to the AVDD pin of the AMC1303 for best performance. Further, use an additional capacitor with a value in the range of 2.2 μ F to 10 μ F.

The floating ground reference (AGND) is derived from the end of the shunt resistor, which is connected to the negative input (AINN) of the device. If using a four-pin shunt, connect the inputs of the device to the sense terminals of the shunt. Route the ground connection as a separate trace to the shunt to minimize offset and improve accuracy.

To decouple the digital power supply on the controller side, use a 0.1 μ F and 2.2 μ F capacitor placed as close to the DVDD pin of the AMC1303 as possible.

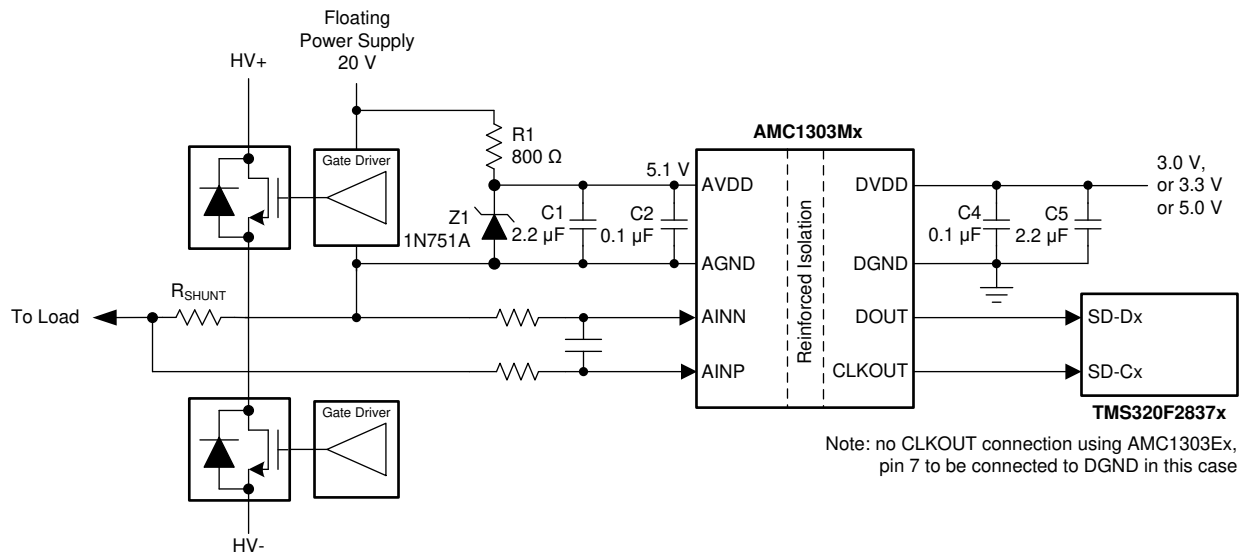


Figure 8-8. Decoupling the AMC1303

8.4 Layout

8.4.1 Layout Guidelines

Figure 8-9 shows a layout recommendation detailing the critical placement of the decoupling capacitors (as close as possible to the AMC1303). This figure also shows the placement of other components required by the device. For best performance, place the shunt resistor and the antialiasing filter components as close as possible to the AINP and AINN inputs of the AMC1303. Keep the layout of both connections symmetrical.

8.4.2 Layout Example

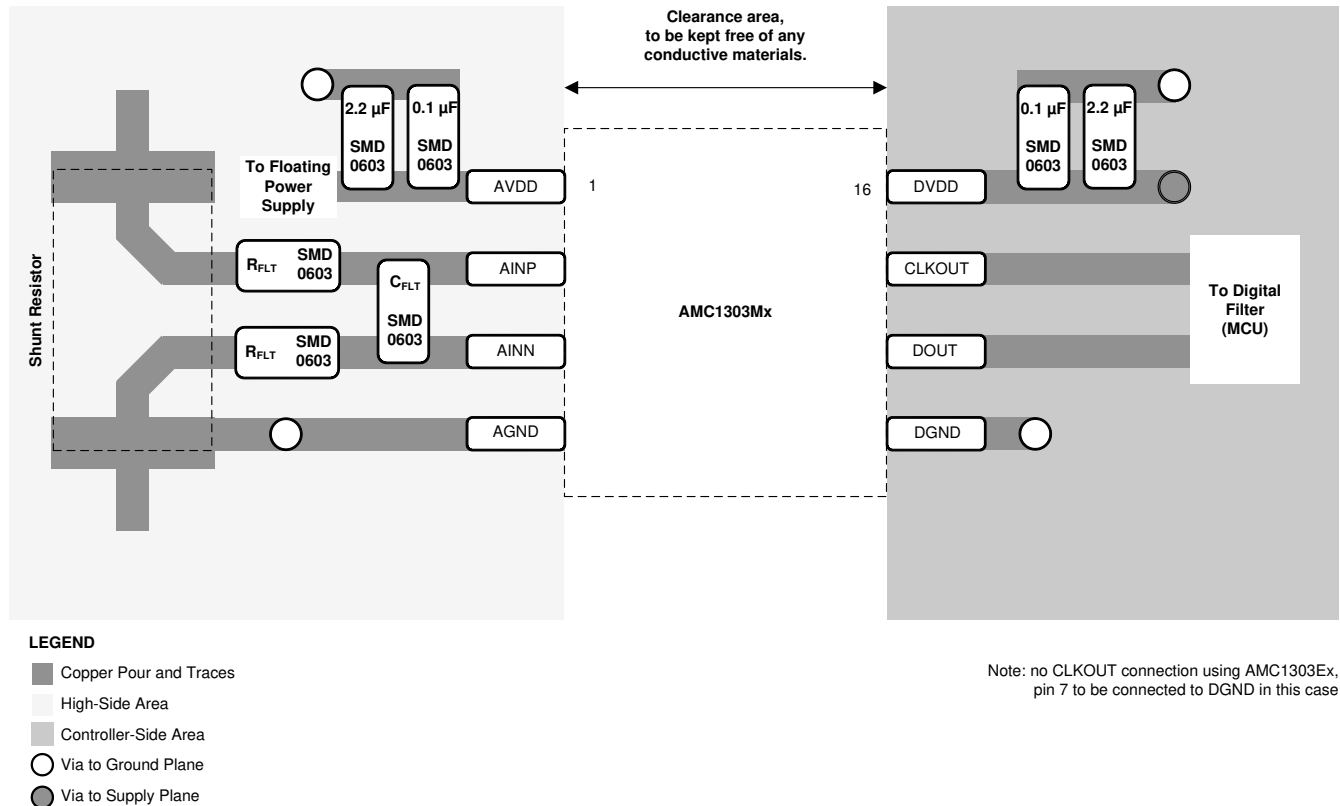


Figure 8-9. Recommended Layout of the AMC1303

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

9.1.1.1 Isolation Glossary

See the [Isolation Glossary](#)

9.2 Documentation Support

9.2.1 Related Documentation

- Texas Instruments, [AMC1210 Quad Digital Filter for 2nd-Order Delta-Sigma Modulator data sheet](#)
- Texas Instruments, [MSP430F677x Polyphase Metering SoCs data sheet](#)
- Texas Instruments, [TMS320F2807x Piccolo™ Microcontrollers data sheet](#)
- Texas Instruments, [TMS320F2837xD Dual-Core Delfino™ Microcontrollers data sheet](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application note](#)
- Texas Instruments, [Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications application note](#)

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.5 Trademarks

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (February 2020) to Revision D (October 2024) | Page |
|--|------|
| • Changed isolation standard from <i>DIN VDE V 0884-11 (VDE V 0884-11)</i> to <i>DIN EN IEC 60747-17 (VDE 0884-17)</i> and updated the <i>Insulation Specifications</i> and <i>Safety-Related Certifications</i> tables accordingly..... | 1 |
| • Added AMC1303M2520F device to Device Comparison Table | 3 |
| • Changed chopper frequency from $f_{CLK} / 32$ to fixed 625kHz..... | 21 |
| • Changed <i>Output Behavior in Case of a Full-Scale Input</i> section..... | 25 |

| Changes from Revision B (June 2018) to Revision C (February 2020) | Page |
|--|-------------|
| • Changed <i>Safety-related certifications</i> bullet in <i>Features</i> section: changed VDE certification revision from <i>DIN V VDE V 0884-10 (VDE V 0884-11)</i> to <i>DIN VDE V 0884-11</i> and changed <i>IEC 60950-1</i> , and <i>IEC 60065</i> to <i>IEC 62368-1</i> | 1 |
| • Changed <i>DIN V VDE V</i> to <i>DIN VDE V</i> in <i>Description</i> section | 1 |
| • Changed CLR and CPG values from ≥ 9 mm to ≥ 8.5 mm in <i>Insulation Specifications</i> table | 6 |
| • Changed <i>Insulation Specifications</i> table header row from <i>DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01</i> to <i>DIN VDE V 0884-11: 2017-01</i> | 6 |
| • Changed VDE certification details in <i>Safety-Related Certifications</i> table | 7 |
| • Changed <i>Safety Limiting Values</i> table format as per current standard | 7 |
| • Changed <i>Functional Block Diagram</i> to include input resistors used for VCM diagnostic..... | 20 |
| • Changed <i>Equation 3</i> and text reference in <i>Digital Filter Usage</i> section..... | 26 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| AMC1303E0510DWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303E051 | Samples |
| AMC1303E0510DWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303E051 | Samples |
| AMC1303E0520DWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303E052 | Samples |
| AMC1303E0520DWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303E052 | Samples |
| AMC1303E2510DWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303E251 | Samples |
| AMC1303E2510DWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303E251 | Samples |
| AMC1303E2520DWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303E252 | Samples |
| AMC1303E2520DWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303E252 | Samples |
| AMC1303M0510DWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303M051 | Samples |
| AMC1303M0510DWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303M051 | Samples |
| AMC1303M0520DWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303M052 | Samples |
| AMC1303M0520DWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303M052 | Samples |
| AMC1303M2510DWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303M251 | Samples |
| AMC1303M2510DWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303M251 | Samples |
| AMC1303M2520DWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303M252 | Samples |
| AMC1303M2520DWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1303M252 | Samples |
| AMC1303M2520FDWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | 40 to 125 | 303M252F | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

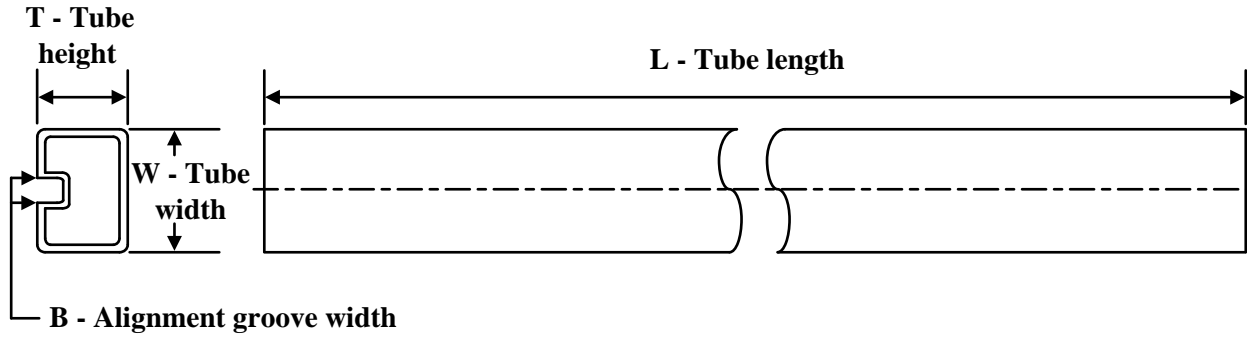

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| AMC1303E0510DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| AMC1303E0520DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| AMC1303E2510DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| AMC1303E2520DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| AMC1303M0510DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| AMC1303M0520DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| AMC1303M2510DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| AMC1303M2520DWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

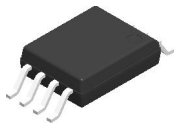

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| AMC1303E0510DWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| AMC1303E0520DWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| AMC1303E2510DWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| AMC1303E2520DWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| AMC1303M0510DWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| AMC1303M0520DWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| AMC1303M2510DWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| AMC1303M2520DWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

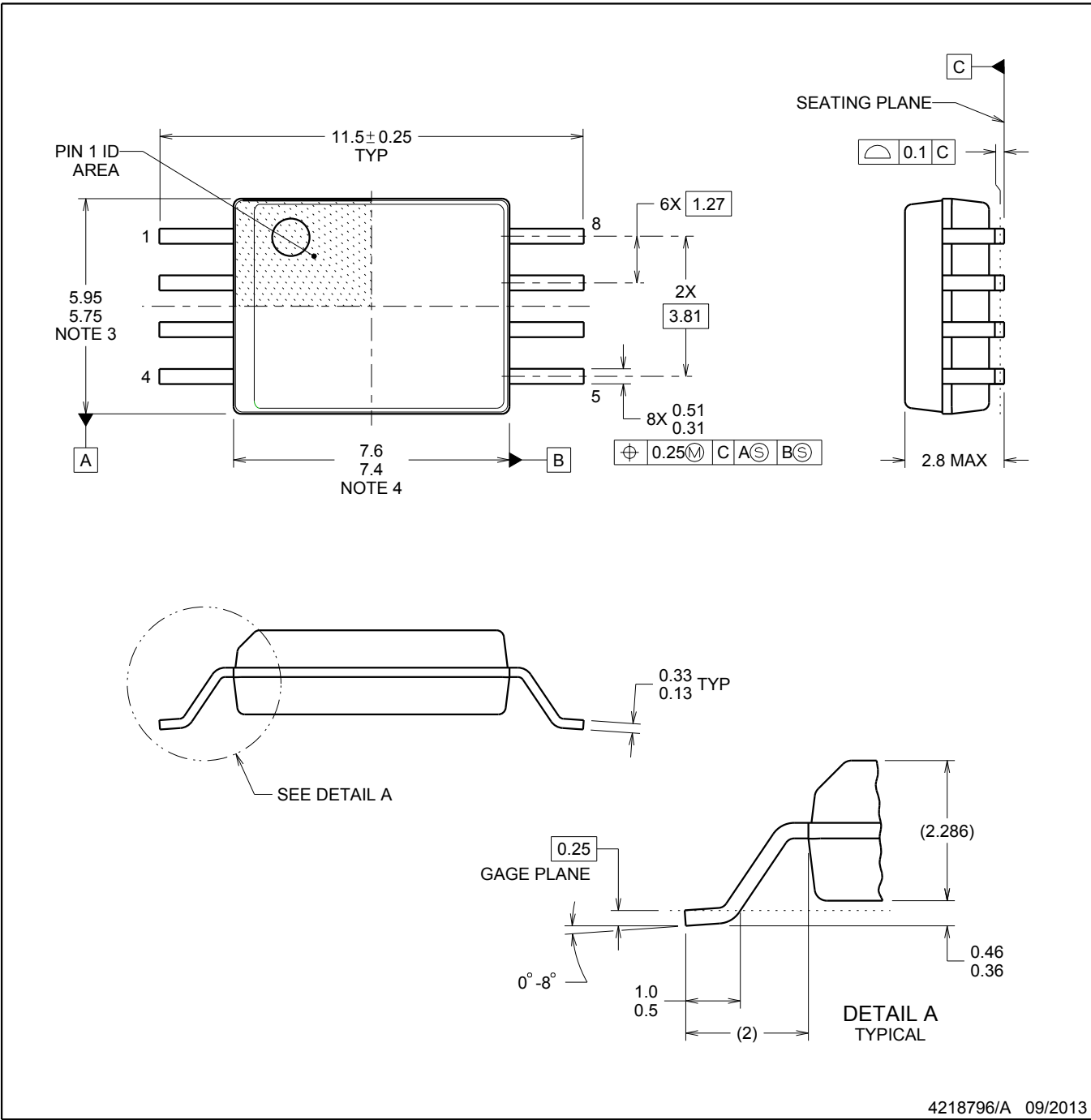
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| AMC1303E0510DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1303E0520DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1303E2510DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1303E2520DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1303M0510DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1303M0520DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1303M2510DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1303M2520DWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |



DWV0008A

SOIC - 2.8 mm max height

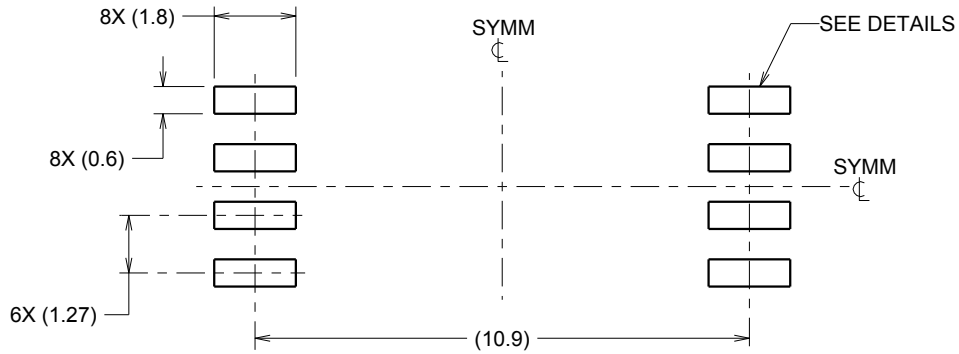
SOIC



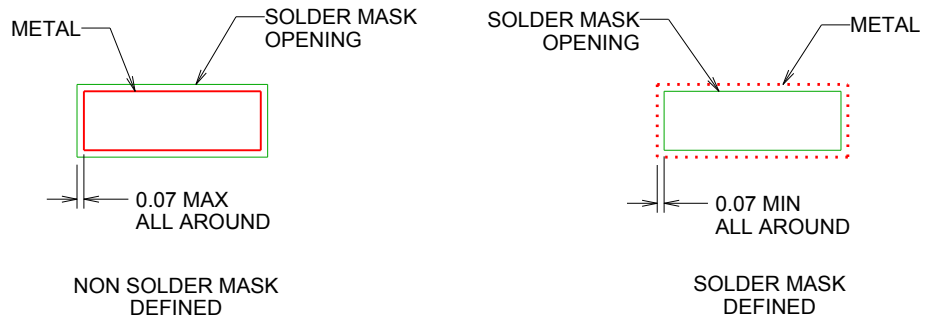
4218796/A 09/2013

NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

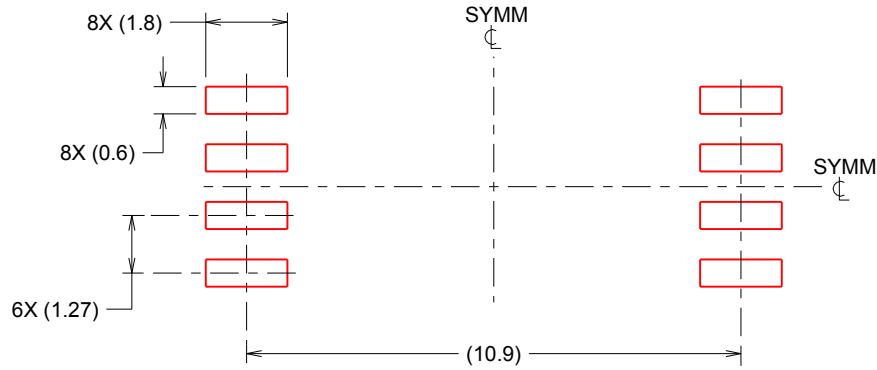


SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:6X

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NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.

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