BQ25620/BQ25622 I^2C Controlled 1-Cell, 3.5A, Maximum 18V Input, Buck Battery Charger with NVDC Power Path Management and OTG Output

1 Features

- High-efficiency, 1.5MHz, synchronous switching mode buck charger for single cell battery
  - >90% efficiency down to 25mA output current from 5V input
  - Charge termination from 10mA to 620mA, 10mA steps
  - Flexible JEITA profile for safe charging over temperature
- BATFET control to support shutdown, ship mode and full system reset
  - 1.5µA quiescent current in battery only mode
  - 0.15µA battery leakage current in ship mode
  - 0.1µA battery leakage current in shutdown
- Supports USB On-The-Go (OTG)
  - Boost mode supporting 3.84V to 9.6V output
  - >90% boost efficiency down to 100mA OTG current for 5V VBUS
- Supports a wide range of input sources
  - 3.9V to 18V wide input operating voltage range with 26V absolute maximum input voltage
  - Maximizes source power with input voltage regulation (VINDPM) and input current regulation (IINDPM)
  - VINDPM threshold automatically tracks battery voltage
- Efficient battery operation with 15mΩ BATFET
- Narrow VDC (NVDC) power path management
  - System instant-on with depleted or no battery
  - Battery supplement when adapter is fully loaded
- Flexible autonomous or I^2C-controlled modes
- Integrated 12-bit ADC for voltage, current, temperature monitoring
- High accuracy
  - ±0.5% charge voltage regulation
  - ±5% charge current regulation
  - ±5% input current regulation
- Safety
  - Thermal regulation and thermal shutdown
  - Input, system, battery overvoltage protection
  - Battery, converter overcurrent protection
  - Charging safety timer
- Safety-Related Certifications:
  - IEC 62368-1 CB Certification

2 Applications

- Tablet
- Gaming and Computer Accessories
- IP Camera, EPOS
- Portable Medical Equipment

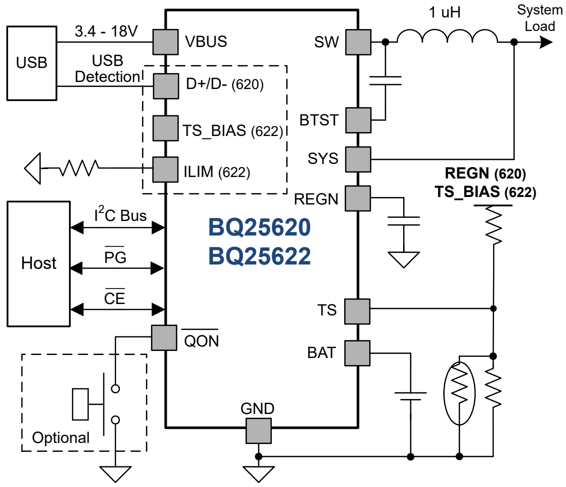
3 Description

The BQ25620 and BQ25622 are highly-integrated 3.5A switch-mode battery charge management and system power path management devices for single cell Li-Ion and Li-polymer batteries. The solution is highly integrated with built-in current sensing, loop compensation, input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. The devices use narrow VDC power path management, regulating the system slightly above the battery voltage without dropping below a configurable minimum system voltage. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time, extends battery life during discharging phase, and the ultra-low 0.15µA ship mode current extends battery shelf life. The I^2C serial interface with charging and system settings makes the BQ25620 and BQ25622 truly flexible solutions.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
BQ25620	RYK (WQFN 18)	2.50mm × 3.00mm
BQ25622	RYK (WQFN 18)	2.50mm × 3.00mm

(1) For all available packages, see Section 14.



BQ25620/2 Simplified Application Diagram

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4 Description (continued)

The BQ25620 supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant high voltage adapter. It sets the default input current limit based on the built-in D+/D- USB adapter detection interface. BQ25622 has an ILIM pin to set the default input current limit and a TS_BIAS pin for controlled thermistor bias. The device is compliant with USB 2.0 and USB 3.0 power specifications for input current and voltage regulation and meets USB On-the-Go (OTG) operation power rating specification with constant current limit up to 2.4A.

The power path management regulates the system slightly above battery voltage but does not drop below the programmable minimum system voltage. With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or input voltage limit is reached, the power path management automatically reduces the charge current. As the system load continues to increase, the battery starts to discharge until the system power requirement is met. This supplement mode prevents overloading the input source.

The BQ25620 and BQ25622 initiate and complete a charging cycle without host control. By sensing the battery voltage, it charges the battery in four different phases: trickle charge, pre-charge, constant current (CC) charge, and constant voltage (CV) charge. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset threshold and the battery voltage is higher than the recharge threshold. Termination is supported for all TS pin temperature zones.

The BQ25620 and BQ25622 provide various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer, and overvoltage and overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds the programmable threshold. The STAT output reports the charging status and any fault conditions. Other safety features include battery temperature sensing for charge mode and OTG boost mode, thermal shutdown and input UVLO and overvoltage protection. The $\overline{\text{PG}}$ output indicates if a good power source is present. The $\overline{\text{INT}}$ output notifies the host when a fault occurs or status changes.

The BQ25620 and BQ25622 are available in a 18-pin, 2.5mm × 3.0mm WQFN package.

5 Device Comparison

Table 5-1. Device Comparison

FUNCTION	BQ25611D	BQ25616	BQ25620	BQ25622
Input Voltage Range	4V - 13.5V	4V - 13.5V	3.9V - 18V	3.9V - 18V
Part Configuration	I2C	Standalone	I2C	I2C
Programmable Charge Voltage	3.5 - 4.3V (100mV per step); 4.3 - 4.52V (10mV per step)	4.1V / 4.2V / 4.35V	3.5 - 4.8V (10mV per step)	3.5 - 4.8V (10mV per step)
D+/D- USB Detection	Yes	Yes	Yes	No
ILIM Pin	No	Yes	No	Yes
TS Profile	JEITA	HOT/COLD	JEITA	JEITA
Quiescent Battery Current	9.5µA	9.5µA	1.5µA	1.5µA
OTG	Yes	Yes	Yes	Yes
OTG Current Limit	1.2A	1.2A	2.4A	2.4A
ADC	None	None	12-bit ADC	12-bit ADC
Package	4x4mm^2 QFN (24)	4x4mm^2 QFN (24)	2.5x3mm^2 QFN (18)	2.5x3mm^2 QFN (18)

6 Pin Configuration and Functions

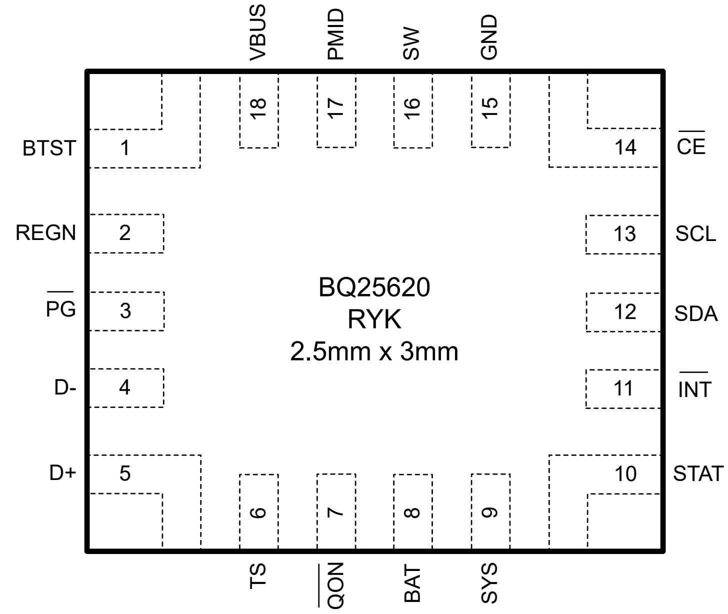


Figure 6-1. BQ25620 Pinout, 18-Pin WQFN Top View

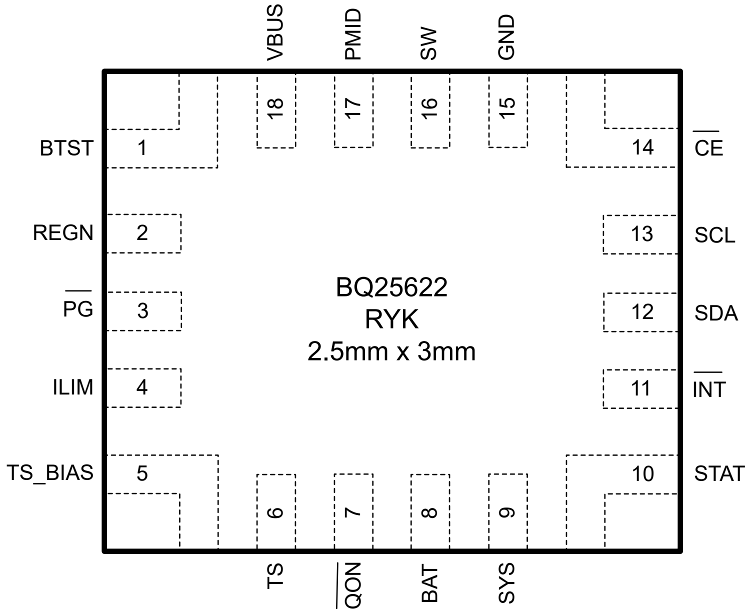


Figure 6-2. BQ25622 Pinout, 18-Pin WQFN Top View

Table 6-1. Pin Functions

NAME		NO.	TYPE[1]	DESCRIPTION
BQ25622	BQ25620			
BTST		1	P	**High Side Switching MOSFET Gate Driver Power Supply –** Connect a 10 V or higher rating, 47-nF ceramic capacitor between SW and BTST as the bootstrap capacitor for driving high side switching MOSFET (Q2).
REGN		2	P	**The Charger Internal Linear Regulator Output –** Internally, REGN is connected to the anode of the boost-strap diode. Connect a 10 V or higher rating, 4.7-µF ceramic capacitor from REGN to power ground, The capacitor should be placed close to the IC. The REGN LDO output is used for the internal MOSFETs gate driving voltage and for biasing the external TS pin thermistor in BQ25620.

Table 6-1. Pin Functions (continued)

NAME		NO.	TYPE(1)	DESCRIPTION
BQ25622	BQ25620			
$\overline{PG}$		3	DO	**Open Drain Active Low Power Good Indicator –** Connect to the pull up rail via 10-kΩ resistor. LOW indicates an input source of V_{VBUS_UVLO} < VBUS < V_{VBUS_OVP}. Failing poor source detection or triggering the sleep comparator (VBUS < VBAT + V_{SLEEP}) also causes $\overline{PG}$ to transition HIGH.
ILIM	D-	4	AIO	**Input Current Limit Setting Input Pin –** ILIM pin sets the input current limit as I_{INREG} = K_{ILIM} / R_{ILIM}, where R_{ILIM} is connected from ILIM pin to GND. The input current is limited to the lower of the two values set by ILIM pin and IINDPM register bits. The ILIM pin can also be used to monitor input current. The input current is proportional to the voltage on ILIM pin and can be calculated by I_{IN} = (K_{ILIM} x V_{ILIM}) / (R_{ILIM} x 0.8). The ILIM pin function is disabled when EN_EXTILIM bit is set to 0.
				Negative Line of the USB Data Line Pair – D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2.
TS_BIAS	D+	5	P	**Bias for the TS Resistor Voltage Divider –** Provides the bias voltage for the TS resistor voltage divider.
			AIO	**Positive Line of the USB Data Line Pair –** D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2.
TS		6	AI	**Temperature Qualification Voltage Input –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from TS pin bias reference (REGN in BQ25620, TS_BIAS in BQ25622) to TS, then to GND. Charge suspends when TS pin voltage is out of range. Recommend a 103AT-2 10-kΩ thermistor.
$\overline{QON}$		7	DI	**BATFET Enable or System Power Reset Control Input –** If the charger is in ship mode, a logic low on this pin with t_{SM_EXIT} duration forces the device to exit ship mode. If the charger is not in ship mode, a logic low on this pin with t_{QON_RST} initiates a full system power reset if either V_{VBUS} < V_{VBUS_UVLO} or BATFET_CTRL_WVBUS = 1. $\overline{QON}$ has no effect during shutdown mode. The pin contains an internal pull-up to maintain default high logic.
BAT		8	P	**The Battery Charging Power Connection –** Connect to the positive terminal of the battery pack. The internal BATFET is connected between SYS and BAT.
SYS		9	P	**The Charger Output Voltage to System –**The Buck converter output connection point to the system. The internal BATFET is connected between SYS and BAT.
STAT		10	DO	**Open Drain Charge Status Output –** It indicates various charger operations. Connect to the pull up rail via 10-kΩ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. Setting DIS_STAT = 1 disables the STAT pin function, causing the pin to be pulled HIGH. Leave floating if unused.
$\overline{INT}$		11	DO	**Open Drain Interrupt Output. –** Connect to the pull up rail via 10-kΩ resistor. The $\overline{INT}$ pin sends an active low, 256-µs pulse to the host to report the charger device status and faults.
SDA		12	DIO	**I^2C Interface Data –** Connect SDA to the logic rail through a 10-kΩ resistor.
SCL		13	DI	**I^2C Interface Clock –** Connect SCL to the logic rail through a 10-kΩ resistor.
$\overline{CE}$		14	DI	**Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin must be pulled HIGH or LOW, do not leave floating.
GND		15	P	**Ground Return**
SW		16	P	**Switching Node Connecting to Output Inductor –** Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 47-nF bootstrap capacitor from SW to BTST.
PMID		17	P	**HSFET Drain Connection –** Internally PMID is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET.
VBUS		18	P	**Charger Input Voltage –** The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source.

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VBUS (converter not switching)	–2	26	V
	PMID (converter not switching)	–0.3	26	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SW	–2 (50ns)	21	V
	BTST (when converter switching)	–0.3	27	V
	$\overline{\text{CE}}$, STAT, SCL, SDA, $\overline{\text{INT}}$, REGN, $\overline{\text{QON}}$	–0.3	6	V
	D+, D-, ILIM, $\overline{\text{PG}}$, TS, TS_BIAS	–0.3	6	V
Output Sink Current	$\overline{\text{INT}}$, STAT, $\overline{\text{PG}}$		6	mA
Differential Voltage	BTST-SW	–0.3	6	V
	PMID-VBUS	–0.3	6	V
	SYS-BAT	–0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	3.9		18	V
V_{BAT}	Battery voltage			4.8	V
I_{VBUS}	Input current			3.2	A
I_{SW}	Output current (SW)			3.5	A
I_{BAT}	Fast charging current			3.5	A
	RMS discharge current (continuously)			6	A
	Peak discharge current (up to 50ms)			10	A
I_{REGN}	Maximum REGN Current			20	mA
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C
L_{SW}	Inductor for the switching regulator	0.68		2.2	µH
C_{VBUS}	VBUS capacitor (without de-rating)	1			µF
C_{PMID}	PMID capacitor (without de-rating)	10			µF
C_{SYS}	SYS capacitor (without de-rating)	20		500	µF

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C_{BAT}	BAT capacitor (without de-rating)	10			µF

7.4 Thermal Information

THERMAL METRIC[1]		BQ25620, BQ25622	UNIT
		RYK (QFN)	
		18 pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Quiescent battery current (BAT, SYS, SW) when the charger is in the battery only mode, BATFET is enabled, ADC is disabled	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, system is powered by battery. -40 °C < T_J < 60 °C		1.5	3	µA
$I_{Q\_BAT\_ADC}$	Quiescent battery current (BAT, SYS, SW) when the charger is in the battery only mode, BATFET is enabled, ADC is enabled	VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC enabled, system is powered by battery. -40 °C < T_J < 60 °C		260		µA
$I_{Q\_BAT\_SD}$	Quiescent battery current (BAT) when the charger is in shutdown mode, BATFET is disabled, ADC is disabled	VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in shutdown mode, ADC disabled, T_J < 60 °C		0.1	0.2	µA
$I_{Q\_BAT\_SHIP}$	Quiescent battery current (BAT) when the charger is in ship mode, BATFET is disabled, ADC is disabled	VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in ship mode, ADC disabled, T_J < 60 °C		0.15	0.5	µA
I_{Q_VBUS}	Quiescent input current (VBUS)	VBUS = 5V, VBAT = 4V, charge disabled, converter switching, ISYS = 0A, PFM enabled		450		µA
$I_{Q\_VBUS\_HIZ}$	Quiescent input current (VBUS) in HIZ	VBUS = 5V, VBAT = 4V, HIZ mode, ADC disabled		5	20	µA
		VBUS = 15V, VBAT = 4V, HIZ mode, ADC disabled		20	35	µA
I_{Q_OTG}	Quiescent battery current (BAT, SYS, SW) in boost OTG mode	VBAT = 4.2V, VBUS = 5V, OTG mode enabled, converter switching, PFM enabled, I_{VBUS} = 0A, TS float, TS_IGNORE = 1		250		µA
VBUS / VBAT SUPPLY						
V_{VBUS_OP}	VBUS operating range		3.9		18	V
V_{VBUS_UVLO}	VBUS falling to turn off I2C, no battery	VBUS falling	3.0	3.15	3.3	V

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery	VBUS rising	3.2	3.35	3.5	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 0	6.1	6.4	6.7	V
V_{VBUS_OVPZ}	VBUS overvoltage falling hreshold	VBUS rising, VBUS_OVP = 0	5.8	6.0	6.2	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising, VBUS_OVP = 1	18.2	18.5	18.8	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS falling, VBUS_OVP = 1	17.4	17.7	18.0	V
V_{SLEEP}	Enter Sleep mode threshold	(VBUS - VBAT), VBUS falling	9	45	85	mV
V_{SLEEPZ}	Exit Sleep mode threshold	(VBUS - VBAT), VBUS rising	115	220	340	mV
V_{BAT_UVLOZ}	BAT voltage for active I2C, turn on BATFET, no VBUS	VBAT rising	2.3	2.4	2.5	V
V_{BAT_UVLO}	BAT voltage to turnoff I2C, turn off BATFET, no VBUS	VBAT falling, VBAT_UVLO = 0	2.1	2.2	2.3	V
		VBAT falling, VBAT_UVLO = 1	1.7	1.8	1.9	V
V_{BAT_OTG}	BAT voltage rising threshold to enable OTG mode	VBAT rising, VBAT_OTG_MIN = 0	2.9	3.0	3.1	V
		VBAT rising, VBAT_OTG_MIN = 1	2.5	2.6	2.7	V
V_{BAT_OTGZ}	BAT voltage falling threshold to disable OTG mode	VBAT falling, VBAT_OTG_MIN = 0	2.7	2.8	2.9	V
		VBAT falling, VBAT_OTG_MIN = 1	2.3	2.4	2.5	V
$V_{POORSRC}$	Bad adapter detection threshold	VBUS falling	3.6	3.7	3.75	V
$I_{POORSRC}$	Bad adapter detection current source			10		mA
POWER-PATH MANAGEMENT						
$V_{SYS\_REG\_ACC}$	Typical system voltage regulation	ISYS = 0A, VBAT > VSYSMIN, Charge Disabled. Offset above VBAT		50		mV
		ISYS = 0A, V_{BAT} < VSYSMIN, Charge Disabled. Offset above VSYSMIN		230		mV
V_{SYSMIN_RNG}	VSYSMIN register range		2.56		3.84	V
$V_{SYSMIN\_REG\_STEP}$	VSYSMIN register step size			80		mV
$V_{SYSMIN\_REG\_ACC}$	Minimum DC system voltage output	ISYS = 0A, V_{BAT} < VSYSMIN = B00h (3.52V), Charge Disabled	3.52	3.75		V
V_{SYS_SHORT}	VSYS short voltage falling threshold to enter forced PFM			0.9		V
V_{SYS_SHORTZ}	VSYS short voltage rising threshold to exit forced PFM			1.1		V
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3.50		4.80	V
V_{REG_STEP}	Typical charge voltage step			10		mV
V_{REG_ACC}	Charge voltage accuracy	T_J = 25°C	–0.3		0.3	%
		T_J = –10°C - 85°C	–0.4		0.4	%
I_{CHG_RANGE}	Typical charge current regulation range		0.08		3.52	A
I_{CHG_STEP}	Typical charge current regulation step			80		mA
I_{CHG_ACC}	Charge current accuracy	VBAT = 3.1V or 3.8V, ICHG = 1760mA, T_J = –10°C - 85°C	–5		5	%
		VBAT = 3.1V or 3.8V, ICHG = 1040mA, T_J = –10°C - 85°C	–5.5		5.5	%
		VBAT = 3.1V or 3.8V, ICHG = 320mA, T_J = –10°C - 85°C	–5.5		5.5	%

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PRECHG_RANGE}	Typical pre-charge current range		20		620	mA
I_{PRECHG_STEP}	Typical pre-charge current step			20		mA
I_{PRECHG_ACC}	Pre-charge current accuracy when V_{BAT} below V_{SYSMIN} setting	VBAT = 2.5V, IPRECHG = 500mA, T_J = –10°C - 85°C	–12		12	%
		VBAT = 2.5V, IPRECHG = 200mA, T_J = –10°C - 85°C	–12		12	%
		VBAT = 2.5V, IPRECHG = 100mA, T_J = –10°C - 85°C	–15		15	%
I_{TERM_RANGE}	Typical termination current range		10		620	mA
I_{TERM_STEP}	Typical termination current step			10		mA
I_{TERM_ACC}	Termination current accuracy	ITERM = 20mA, T_J = –10°C - 85°C	–60		60	%
		ITERM = 100mA, T_J = –10°C - 85°C	–15		15	%
		ITERM = 300mA, T_J = –10°C - 85°C	–13		13	%
V_{BAT_SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising		2.25		V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling, VBAT_UVLO=0		2.05		V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling, VBAT_UVLO=1		1.85		V
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < V_{BAT_SHORTZ}, ITRICKLE = 0	15	25	35	mA
		VBAT < V_{BAT_SHORTZ}, ITRICKLE = 1	62	82	102	mA
V_{BAT_LOWVZ}	Battery voltage rising threshold	Transition from pre-charge to fast charge	2.9	3.0	3.1	V
V_{BAT_LOWV}	Battery voltage falling threshold	Transition from fast charge to pre-charge	2.7	2.8	2.9	V
V_{RECHG}	Battery recharge threshold below V_{REG}	VBAT falling, VRECHG = 0		100		mV
		VBAT falling, VRECHG = 1		200		mV
I_{PMID_LOAD}	PMID discharge load current		20	30		mA
I_{BAT_LOAD}	Battery discharge load current		20	30		mA
I_{SYS_LOAD}	System discharge load current		20	30		mA
BATFET						
R_{BATFET}	MOSFET on resistance from SYS to BAT			15	25	mΩ
BATTERY PROTECTIONS						
V_{BAT_OVP}	Battery overvoltage rising threshold	As percentage of VREG	103	104	105	%
V_{BAT_OVPZ}	Battery overvoltage falling threshold	As percentage of VREG	101	102	103	%
I_{BATFET_OCP}	BATFET over-current rising threshold		6			A
I_{BAT_PK}	Battery discharging peak current rising threshold	IBAT_PK = 00	1.5			A
		IBAT_PK = 01	3			A
		IBAT_PK = 10	6			A
		IBAT_PK = 11	12			A
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		3.8		16.8	V
V_{INDPM_STEP}	Typical input voltage regulation step			40		mV

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM=4.6V	–4		4	%
		VINDPM=8V	–3		3	%
		VINDPM=16V	–2		2	%
$V_{INDPM\_BAT\_TRACK}$	Battery tracking VINDPM accuracy	VBAT = 3.9V, VINDPM_BAT_TRACK=1, VINDPM = 4V	4.15	4.3	4.45	V
I_{INDPM_RANGE}	Typical input current regulation range		0.04		3.2	A
I_{INDPM_STEP}	Typical input current regulation step			20		mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500mA, VBUS=5V	450	475	500	mA
		IINDPM = 900mA, VBUS=5V	810	855	900	mA
		IINDPM = 1500mA, VBUS=5V	1350	1425	1500	mA
K_{ILIM}	ILIM Pin Scale Factor, IINREG = K_{ILIM} / R_{ILIM}	INREG = 1.6 A	2250	2500	2750	AΩ
D+ / D- DETECTION						
$V_{D+D-\_0p6V\_SRC}$	D+/D- voltage source (600 mV)	1 mA load on D+/D-	400	600	800	mV
I_{D+D-_LKG}	Leakage current into D+/D-	HiZ mode	–1		1	µA
V_{D+D-_2p8}	D+/D- comparator threshold for non-standard adapter		2.55		2.85	V
V_{D+D-_2p0}	D+/D- comparator threshold for non-standard adapter		1.85		2.15	V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 1		120		°C
		TREG = 0		60		°C
T_{SHUT}	Thermal Shutdown Rising Threshold	Temperature Increasing		140		°C
T_{SHUT_HYS}	Thermal Shutdown Falling Hysteresis	Temperature Decreasing by T_{SHUT_HYS}		30		°C
THERMISTOR COMPARATORS (CHARGE MODE)						
V_{TS_COLD}	TS pin rising voltage threshold for TH1 comparator to transition from TS_COOL to TS_COLD. Charge suspended above this voltage.	As Percentage to TS pin bias reference (-5°C w/ 103AT), TS_TH1_TH2_TH3 = 100, 101, 110	75.0	75.5	76.0	%
		As Percentage to TS pin bias reference (0°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 010, 011, 111	72.8	73.3	73.8	%
V_{TS_COLDZ}	TS pin falling voltage threshold for TH1 comparator to transition from TS_COLD to TS_COOL. TS_COOL charge settings resume below this voltage.	As Percentage to TS pin bias reference (-2.5°C w/ 103AT), TS_TH1_TH2_TH3 = 100, 101, 110	73.9	74.4	74.9	%
		As Percentage to TS pin bias reference (2.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 010, 011, 111	71.7	72.2	72.7	%

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TS_COOL}	TS pin rising voltage threshold for TH2 comparator to transition from TS_PRECOOL to TS_COOL. TS_COOL charging settings used above this voltage.	As Percentage to TS pin bias reference (5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 100	70.6	71.1	71.6	%
		As Percentage to TS pin bias reference (10°C w/ 103AT), TS_TH1_TH2_TH3 = 001, 101, 110, 111	67.9	68.4	68.9	%
		As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH1_TH2_TH3 = 010	65.0	65.5	66.0	%
		As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH1_TH2_TH3 = 011	61.9	62.4	62.9	%
V_{TS_COOLZ}	TS pin falling voltage threshold for TH2 comparator to transition from TS_COOL to TS_PRECOOL. TS_PRECOOL charging settings resume below this voltage.	As Percentage to TS pin bias reference (7.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 100	69.3	69.8	70.3	%
		As Percentage to TS pin bias reference (12.5°C w/ 103AT), TS_TH1_TH2_TH3 = 001, 101, 110, 111	66.6	67.1	67.6	%
		As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH1_TH2_TH3 = 010	63.7	64.2	64.7	%
		As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH1_TH2_TH3 = 011	60.6	61.1	61.6	%
$V_{TS\_PRECOOL}$	TS pin rising voltage threshold for TH3 comparator to transition from TS_NORMAL to TS_PRECOOL. TS_PRECOOL charge settings used above this voltage.	As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 100, 101	65.0	65.5	66.0	%
		As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH1_TH2_TH3 = 010, 011, 110, 111	61.9	62.4	62.9	%
$V_{TS\_PRECOOLZ}$	TS pin falling voltage threshold for TH3 comparator to transition from TS_PRECOOL to TS_NORMAL. Normal charging resumes below this voltage.	As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 100, 101	63.7	64.2	64.7	%
		As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH1_TH2_TH3 = 010, 011, 110, 111	60.6	61.1	61.6	%
$V_{TS\_PREWARM}$	TS pin falling voltage threshold for TH4 comparator to transition from TS_NORMAL to TS_PREWARM. TS_PREWARM charging settings used below this voltage.	As Percentage to TS pin bias reference (35°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 100, 101	51.5	52.0	52.5	%
		As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH4_TH5_TH6 = 011, 110, 111	47.9	48.4	48.9	%
$V_{TS\_PREWARMZ}$	TS pin rising voltage threshold for TH4 comparator to transition from TS_PREWARM to TS_NORMAL. Normal charging resumes above this voltage.	As Percentage to TS pin bias reference (32.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 100, 101	53.3	53.8	54.3	%
		As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4_TH5_TH6 = 011, 110, 111	49.2	49.7	50.2	%

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TS_WARM}	TS pin falling voltage threshold for TH5 comparator to transition from TS_PREWARM to TS_WARM. TS_WARM charging settings used below this voltage.	As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 100	47.9	48.4	48.9	%
		As Percentage to TS pin bias reference (45°C w/ 103AT), TS_TH4_TH5_TH6 = 001, 101, 110	44.3	44.8	45.3	%
		As Percentage to TS pin bias reference (50°C w/ 103AT), TS_TH4_TH5_TH6 = 010, 111	40.7	41.2	41.7	%
		As Percentage to TS pin bias reference (55°C w/ 103AT), TS_TH4_TH5_TH6 = 011	37.2	37.7	38.2	%
V_{TS_WARMZ}	TS pin rising voltage threshold for TH5 comparator to transition from TS_WARM to TS_PREWARM. TS_PREWARM charging settings resume above this voltage.	As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 100	49.2	49.7	50.2	%
		As Percentage to TS pin bias reference (42.5°C w/ 103AT), TS_TH4_TH5_TH6 = 001, 101, 110	45.6	46.1	46.6	%
		As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH4_TH5_TH6 = 010, 111	42.0	42.5	43.0	%
		As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_TH4_TH5_TH6 = 011	38.5	39	39.5	%
V_{TS_HOT}	TS pin falling voltage threshold for TH6 comparator to transition from TS_WARM to TS_HOT. Charging is suspended below this voltage.	As Percentage to TS pin bias reference (50°C w/ 103AT), TS_TH4_TH5_TH6 = 100 or 101	40.7	41.2	41.7	%
		As Percentage to TS pin bias reference (60°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 011, 110 or 111	33.9	34.4	34.9	%
V_{TS_HOTZ}	TS pin rising voltage threshold for TH6 comparator to transition from TS_HOT to TS_WARM. TS_WARM charging settings resume above this voltage.	As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH4_TH5_TH6 = 100 or 101	42.0	42.5	43.0	%
		As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 011, 110 or 111	35.2	35.7	36.2	%
THERMISTOR COMPARATORS (OTG MODE)						
$V_{TS\_OTG\_COLD}$	TS pin rising voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_COLD. OTG suspended above this voltage.	As Percentage to TS pin bias reference (–20°C w/ 103AT), TS_TH_OTG_COLD = 0	79.5	80.0	80.5	%
		As Percentage to TS pin bias reference (–10°C w/ 103AT), TS_TH_OTG_COLD = 1	76.6	77.1	77.6	%
$V_{TS\_OTG\_COLDZ}$	TS pin falling voltage threshold to transition from TS_OTG_COLD to TS_OTG_NORMAL. OTG resumes below this voltage.	As Percentage to TS pin bias reference (–15°C w/ 103AT), TS_TH_OTG_COLD = 0	78.2	78.7	79.2	%
		As Percentage to TS pin bias reference (–5°C w/ 103AT), TS_TH_OTG_COLD = 1	75.0	75.5	76.5	%

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TS\_OTG\_HOT}$	TS pin falling voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_HOT. OTG suspended below this voltage.	As Percentage to TS pin bias reference (55°C w/ 103AT), TS_OTG_HOT = 00	37.2	37.7	38.2	%
		As Percentage to TS pin bias reference (60°C w/ 103AT), TS_OTG_HOT = 01	33.9	34.4	34.9	%
		As Percentage to TS pin bias reference (65°C w/ 103AT), TS_OTG_HOT = 10	30.8	31.3	31.8	%
$V_{TS\_OTG\_HOTZ}$	TS pin rising voltage threshold to transition from TS_OTG_HOT to TS_OTG_NORMAL. OTG resumes above this threshold.	As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_OTG_HOT = 00	38.5	39.0	39.5	%
		As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_OTG_HOT = 01	35.2	35.7	36.2	%
		As Percentage to TS pin bias reference (62.5°C w/ 103AT), TS_OTG_HOT = 10	32.0	32.5	33.0	%
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency	1.35	1.5	1.65	MHz
MOSFET TURN-ON RESISTANCE						
R_{Q1_ON}	VBUS to PMID on resistance	T_j = –40°C-85°C		26	34	mΩ
R_{Q2_ON}	Buck high-side switching MOSFET turn on resistance between PMID and SW	T_j = –40°C-85°C		55	78	mΩ
R_{Q3_ON}	Buck low-side switching MOSFET turn on resistance between SW and PGND	T_j = –40°C-85°C		60	90	mΩ
OTG MODE CONVERTER						
V_{OTG_RANGE}	Typical OTG mode voltage regulation range		3.8		9.6	V
V_{OTG_STEP}	Typical OTG mode voltage regulation step			80		mV
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 9V	–2		2	%
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 5V	–3		3	%
I_{OTG_RANGE}	Typical OTG mode current regulation range		0.1		2.4	A
I_{OTG_STEP}	Typical OTG mode current regulation step			20		mA
I_{OTG_ACC}	OTG mode current regulation accuracy	IOTG = 1.8A	–3		3	%
		IOTG = 1.5A	–5		5	%
		IOTG = 0.5A	–10		10	%
V_{OTG_UVP}	OTG mode undervoltage falling threshold at PMID			3.4		V
$V_{OTG\_VBUS\_OVP}$	OTG mode overvoltage rising threshold at VBUS		10.5	11.0	11.5	V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.4	4.6		V
		V_{VBUS} = 9V, I_{REGN} = 20mA	4.8	5.0	5.2	V
V_{REGNZ_OK}	REGN not good falling threshold	Converter switching		3.2		V
		Converter not switching		2.3		V
I_{REGN_LIM}	REGN LDO current limit	V_{VBUS} = 5V, VREGN = 4.3V	20			mA

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{TS\_BIAS\_FAULT}$	Rising threshold to transition from TSBIAS good condition to fault condition	REGN=5V; ISINK applied on TS_BIAS pin	2.5	4.5	8	mA
$I_{TS\_BIAS\_FAULTZ}$	Falling threshold to transition from TSBIAS fault condition to good condition	REGN=5V; ISINK applied on TS_BIAS pin	2	3.85	7	mA
ADC MEASUREMENT ACCURACY AND PERFORMANCE						
t_{ADC_CONV}	Conversion-time, Each Measurement	ADC_SAMPLE = 00		24		ms
		ADC_SAMPLE = 01		12		ms
		ADC_SAMPLE = 10		6		ms
		ADC_SAMPLE = 11		3		ms
ADC_{RES}	Effective Resolution	ADC_SAMPLE = 00	11	12		bits
		ADC_SAMPLE = 01	10	11		bits
		ADC_SAMPLE = 10	9	10		bits
		ADC_SAMPLE = 11	8	9		bits
ADC MEASUREMENT RANGE AND LSB						
IBUS_ADC	ADC Bus Current Reading (both forward and OTG)	Range	–4		4	A
		LSB		2		mA
VBUS_ADC	ADC VBUS Voltage Reading	Range	0		18.00	V
		LSB		3.97		mV
VPMID_ADC	ADC PMID Voltage Reading	Range	0		18.00	V
		LSB		3.97		mV
VBAT_ADC	ADC BAT Voltage Reading	Range	0		5.572	V
		LSB		1.99		mV
VSYS_ADC	ADC SYS Voltage Reading	Range	0		5.572	V
		LSB		1.99		mV
IBAT_ADC	ADC BAT Current Reading	Range	-7.5		4.0	A
		LSB		4		mA
TS_ADC	ADC TS Voltage Reading	Range as a percent of REGN (–40 °C to 85 °C for 103AT)	20.9		83.2	%
	ADC TS Voltage Reading	LSB		0.0961		%
TDIE_ADC	ADC Die Temperature Reading	Range	–40		140	°C
		LSB		0.5		°C
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL		0.78			V
V_{IL}	Input low threshold level, SDA and SCL				0.42	V
V_{OL_SDA}	Output low threshold level	Sink current = 5mA, 1.2V VDD			0.3	V
I_{BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA
C_{BUS}	Capacitive load for each bus line				400	pF
LOGIC OUTPUT PIN ($\overline{INT}$, $\overline{PG}$, STAT)						
V_{OL}	Output low threshold level	Sink current = 5mA			0.3	V
I_{OUT_BIAS}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC INPUT PIN ($\overline{CE}$, $\overline{QON}$)						
V_{IH_CE}	Input high threshold level, /CE		0.78			V

7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

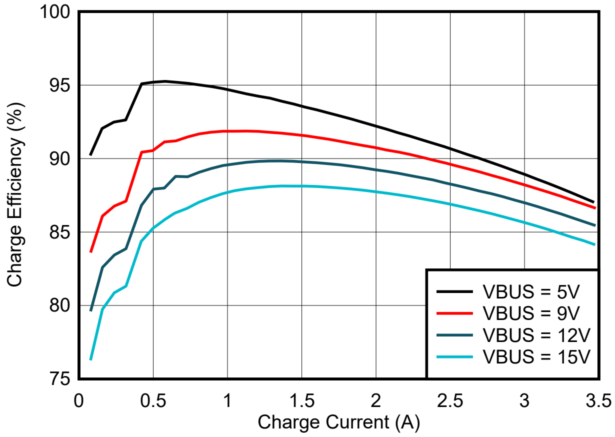
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL_CE}	Input low threshold level, /CE				0.4	V
$I_{IN\_BIAS\_CE}$	High-level leakage current, /CE	Pull up rail 1.8V			1	µA
V_{IH_QON}	Input high threshold level, /QON		1.3			V
V_{IL_QON}	Input low threshold level, /QON				0.4	V
V_{QON}	Internal /QON pull up	/QON is pulled up internally		5		V
R_{QON}	Internal /QON pull up resistance			250		kΩ

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VBUS / VBAT POWER UP						
t_{VBUS_OVP}	VBUS OVP deglitch time to set VBUS_OVP_STAT and VBUS_OVP_FLAG			200		µs
$t_{POORSRC}$	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{TOP_OFF}	Typical top-off timer accuracy	TOPOFF_TMR = 01	12	17	21	min
		TOPOFF_TMR = 10	24	35	41	min
		TOPOFF_TMR = 11	36	52	61	min
t_{SAFETY_TRKCHG}	Charge safety timer accuracy in trickle charge		0.85	1.25	1.35	hr
t_{SAFETY_PRECHG}	Charge safety timer accuracy in pre-charge	PRECHG_TMR = 0	1.75	2.5	2.75	hr
		PRECHG_TMR = 1	0.43	0.62	0.68	hr
t_{SAFETY}	Charge safety timer accuracy in fast charge	CHG_TMR = 0	10.5	14.5	15.5	hr
		CHG_TMR = 1	21.0	28	31	hr
BATFET CONTROL						
t_{BATFET_DLY}	Time after writing to BATFET_CTRL before BATFET turned off for ship mode or shutdown	BATFET_DLY = 1		12.5		s
		BATFET_DLY = 0		25		ms
t_{SM_EXIT}	Deglitch time for $\overline{\text{QON}}$ to be pulled low in order to exit from Ship Mode		0.55	0.8	0.93	s
t_{QON_RST}	Time $\overline{\text{QON}}$ is held low to initiate system power reset		9.0	12.5	14.5	s
t_{BATFET_RST}	Duration that BATFET is disabled during system power reset			430		ms
I2C INTERFACE						
f_{SCL}	SCL clock frequency	See Serial Interface section for more details.			1.0	MHz
DIGITAL CLOCK AND WATCHDOG						
t_{LP_WDT}	Watchdog Reset time (EN_HIZ = 1, WATCHDOG = 11)		100	200		s
t_{WDT}	Watchdog Reset time (EN_HIZ = 0, WATCHDOG = 11)		136	200		s

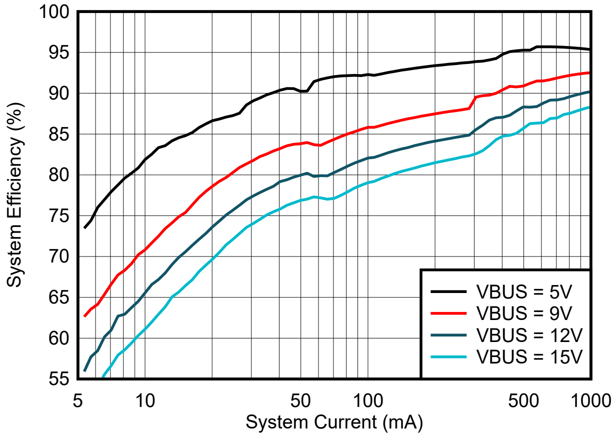
7.7 Typical Characteristics

C_{VBUS} = 1μF, C_{PMID}= 10μF, C_{SYS}= 20μF, C_{BAT}= 1μF, L= 1μH (unless otherwise specified)



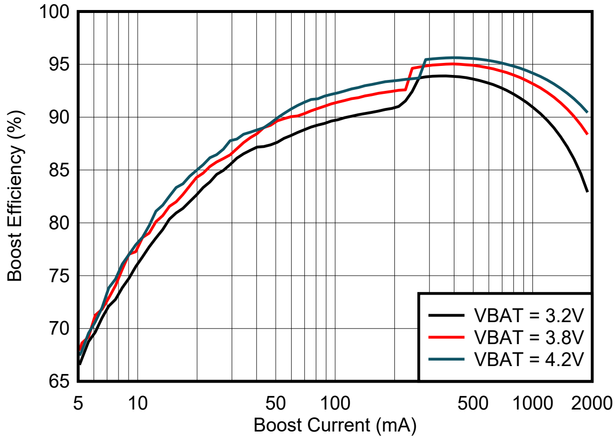
VBAT = 3.8 DCR = 15mΩ

Figure 7-1. Charge Efficiency vs. Charge Current



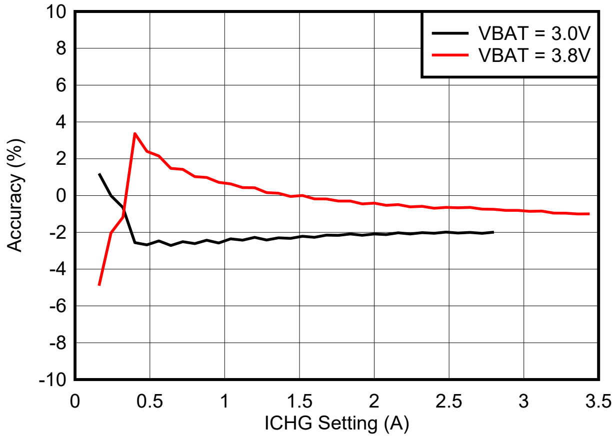
VSYSMIN = 3.52V DCR = 15mΩ

Figure 7-2. System Light Load Efficiency vs. System Current



VOTG = 5.04V DCR = 15mΩ

Figure 7-3. Boost Mode Efficiency vs. Boost Output Current



VBUS = 5V

Figure 7-4. Charge Current Accuracy vs. ICHG Setting

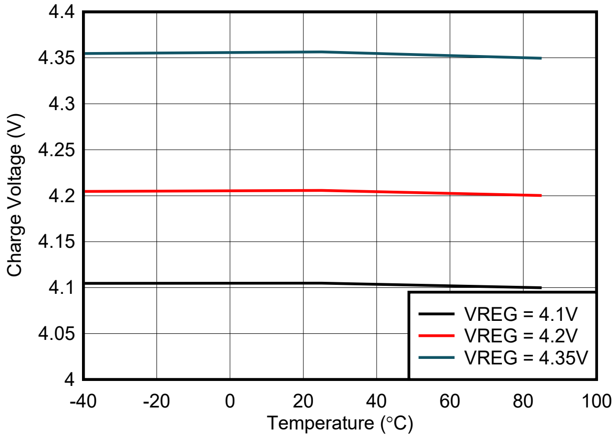
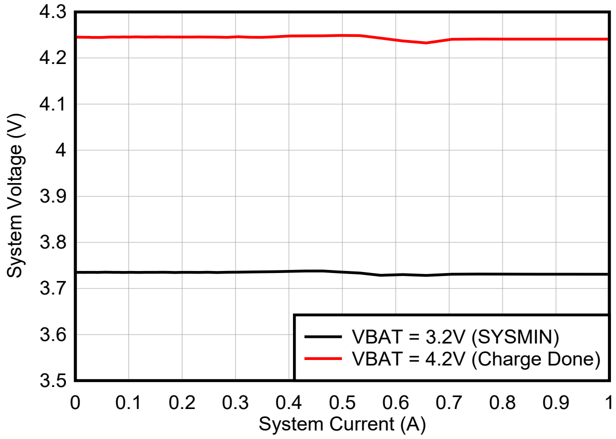


Figure 7-5. Charge Voltage Accuracy vs. VREG Setting



VBUS = 12V

Figure 7-6. System Load Regulation for SYSMIN and After Charge Done

7.7 Typical Characteristics (continued)

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS}= 20µF, C_{BAT}= 1µF, L= 1µH (unless otherwise specified)

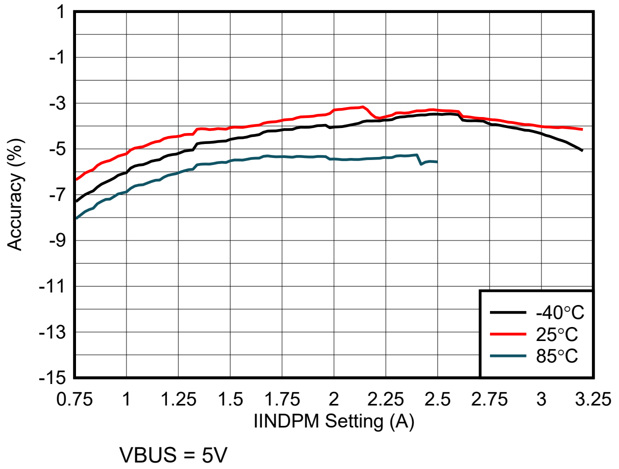


Figure 7-7. Input Current Regulation Accuracy vs. IINDPM Setting

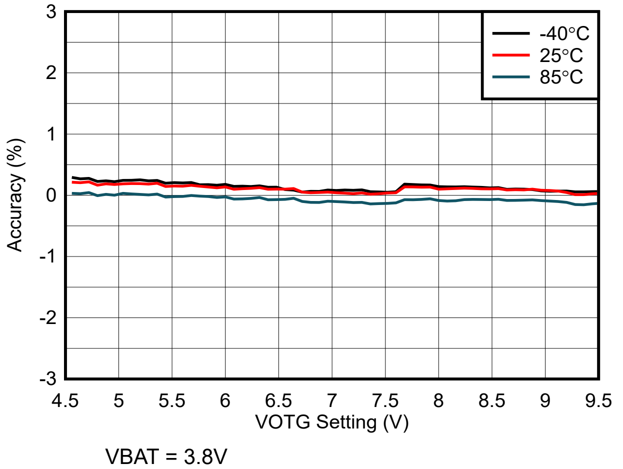


Figure 7-8. Boost Voltage Regulation vs VOTG Setting

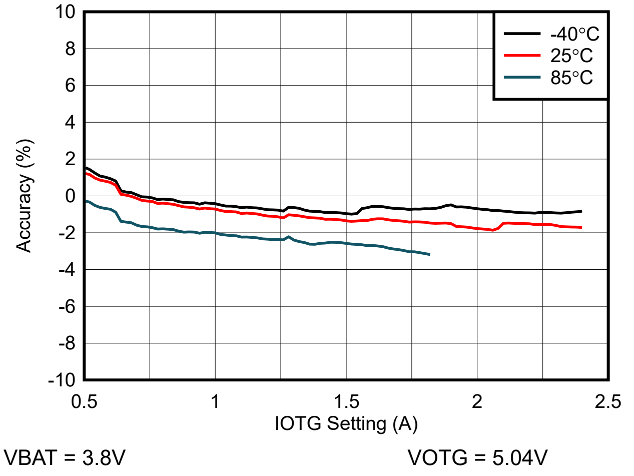


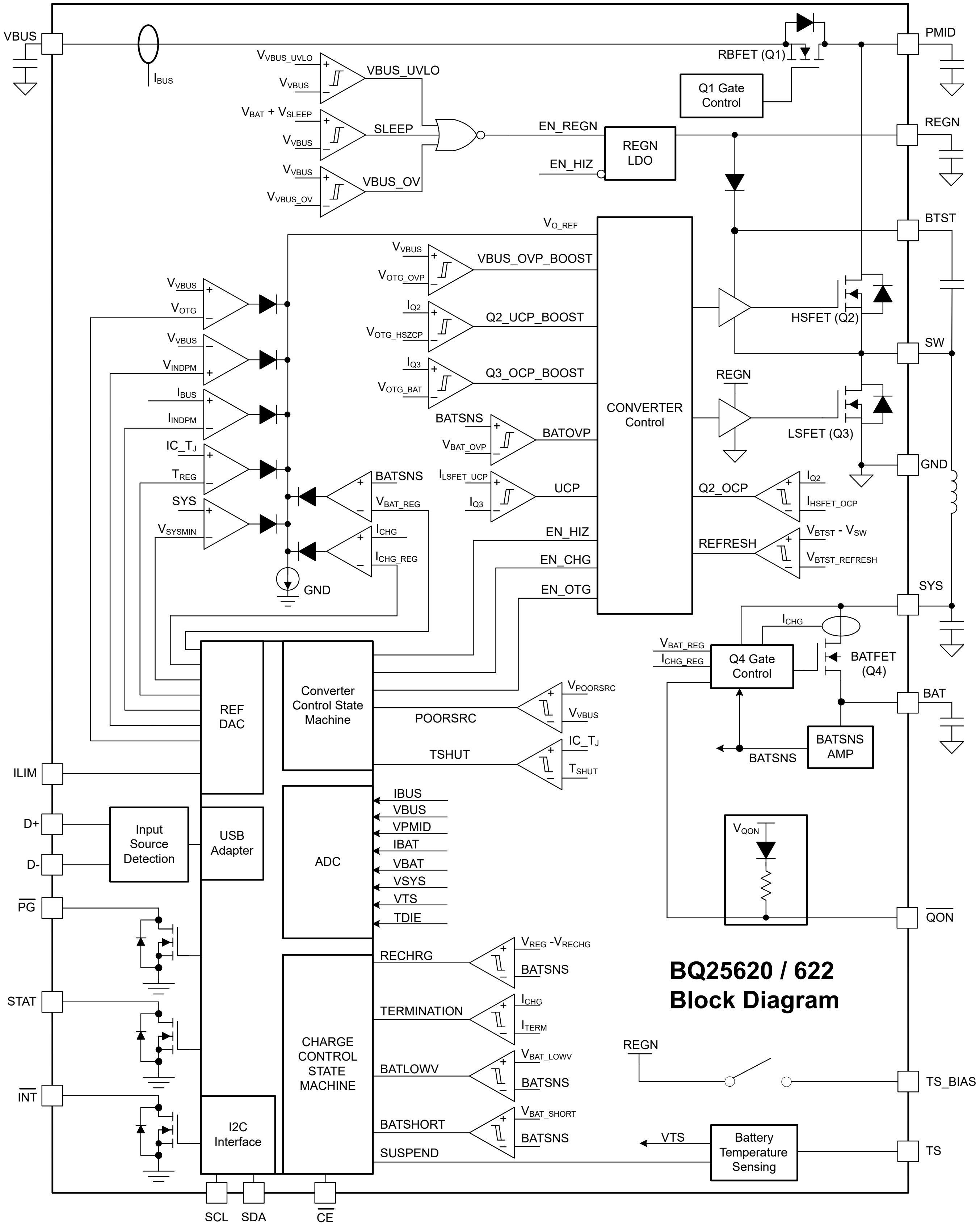
Figure 7-9. Boost Current Regulation Accuracy vs. IOTG Setting

8 Detailed Description

8.1 Overview

The BQ25620 and BQ25622 are highly-integrated 3.5-A switch-mode battery chargers for single-cell Li-ion and Li-polymer batteries. The device includes input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), battery FET (BATFET, Q4), and bootstrap diode for the high-side gate driver.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-On-Reset (POR)

The BQ25620 and BQ25622 power internal bias circuits from the higher voltage of VBUS and BAT. When either voltage rises above its undervoltage lockout (UVLO) threshold, all registers are reset to their POR values and the I^2C interface is enabled for communication. A non-maskable $\overline{\text{INT}}$ pulse is generated, after which the host can access all of the registers.

8.3.2 Device Power Up from Battery

If only the battery is present and the VBAT is above depletion threshold (V_{BAT_UVLOZ}), the BQ25620 and BQ25622 perform a power-on reset then turns on the BATFET to connect the battery to system. The REGN LDO output remains off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

8.3.3 Device Power Up from Input Source

When a valid input source is plugged in with $VBAT < V_{BAT\_UVLOZ}$, the BQ25620 and BQ25622 perform a power-on reset then checks the input source voltage to turn on the REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. REGN LDO power up (Section 8.3.3.1)
2. Poor source qualification (Section 8.3.3.2)
3. Input source type detection using D+/D– to set input current limit (IINDPM) register and input source type (Section 8.3.3.3)
4. Input voltage limit threshold setting (Section 8.3.3.5)
5. Converter power-up (Section 8.3.3.6)

8.3.3.1 REGN LDO Power Up

The REGN LDO regulator supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- VBUS above V_{VBUS_UVLOZ}
- VBUS above $V_{BAT} + V_{SLEEPZ}$
- EN_HIZ = 0
- After 220-ms delay is completed

If any one of the above conditions is not valid, the REGN LDO and the converter power stage remain off with the converter disabled. In this state, the battery supplies power to the system.

8.3.3.2 Poor Source Qualification

After the REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to move forward to the next power on steps.

1. VBUS voltage below V_{VBUS_OVP}
2. VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$

Once these conditions are met, the device proceeds to input source type detection.

8.3.3.3 D+/D– Detection Sets Input Current Limit (BQ25620 Only)

After the REGN LDO is powered, the adapter has been qualified as a good source, and AUTO_INDET_EN bit = 1 (POR default), BQ25620 runs input source detection through D+/D– lines to detect USB Battery Charging Specification 1.2 (BC1.2) input sources (CDP / SDP / DCP) and non-standard adapters. If DCP is detected, BQ25620 runs HVDCP detection if either EN_9V or EN_12V is 1. The detection algorithm runs automatically each time that VBUS is plugged in, updating the IINDPM according to Table 8-2. If AUTO_INDET_EN = 0, the detection algorithm is not run and IINDPM remains unchanged. The host can force the detection algorithm to run and update IINDPM by setting FORCE_INDET to 1.

The USB BC1.2 is able to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

The secondary detection is used to distinguish two types of charging ports (CDP and DCP). Most of the time, a CDP requires the portable device (such as smart phone, tablet) to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port reverts back to SDP even though the D+/D– detection indicates CDP.

Upon the completion of input source type detection, the following registers are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. VBUS_STAT bits are updated to indicate the detected input source type

After detection completes, the host can over-write the IINDPM register to change the input current limit if needed.

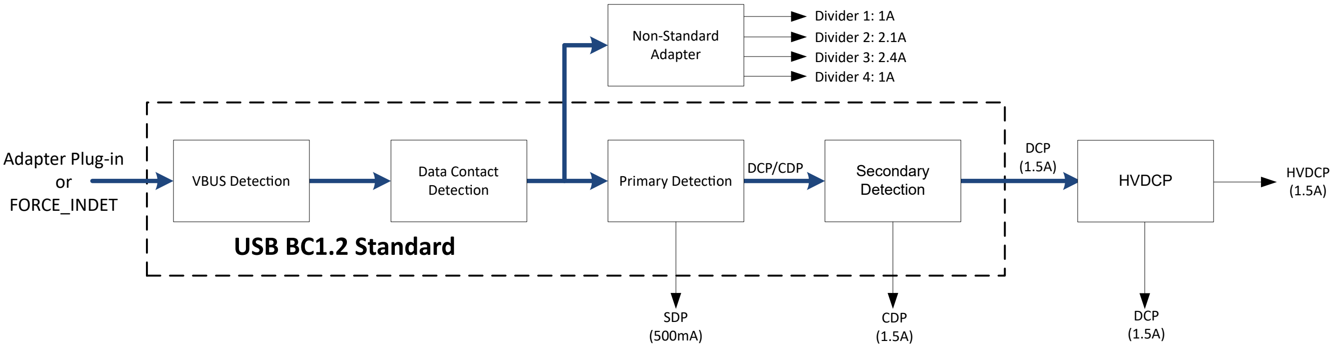


Figure 8-1. D+/D– Detection Flow

If DCP is detected (VBUS_STAT = 011), BQ25620 turns on $V_{D+D-\_0p6V\_SRC}$ on D+ if EN_DCP_BIAS is set to 1. Setting EN_DCP_BIAS to 0 while VBUS_STAT = 011 disables the $V_{D+D-\_0p6V\_SRC}$ on D+ pin, and setting EN_DCP_BIAS to 1 while VBUS_STAT = 011 enables the $V_{D+D-\_0p6V\_SRC}$ on D+ pin. The EN_HIZ bit has priority over EN_DCP_BIAS.

High Voltage Dedicated Charging Port (HVDCP) is used to negotiate either 9V or 12V from the power source if BC1.2 DCP support is detected.

In order to remain in 9V or 12V HVDCP, BQ25620 must maintain a bias on D+ and D-, resulting in higher quiescent current. The host may remove this bias and associated quiescent current by setting EN_9V and EN_12V to 0 at any time. Setting EN_9V and EN_12V to 0 when an HVDCP adapter is providing either 9V or 12V causes the adapter to revert to 5V DCP operation.

The non-standard detection is used to distinguish vendor specific adapters based on their unique dividers on the D+/D- pins. Comparators detect the voltage applied on each pin and determine the input current limit according to Table 8-1.

Table 8-1. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT (A)
Divider 1	V_{D+} within V_{D+D-_2p0}	V_{D-} within V_{D+D-_2p8}	1
Divider 2	V_{D+} within V_{D+D-_2p8}	V_{D-} within V_{D+D-_2p0}	2.1
Divider 3	V_{D+} within V_{D+D-_2p8}	V_{D-} within V_{D+D-_2p8}	2.4

Table 8-2. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINLIM)	VBUS_STAT
USB SDP (USB500)	500 mA	0x1

Table 8-2. Input Current Limit Setting from D+/D– Detection (continued)

D+/D– DETECTION	INPUT CURRENT LIMIT (IINLIM)	VBUS_STAT
USB CDP	1.5 A	0x2
USB DCP	1.5 A	0x3
Divider 1	1 A	0x5
Divider 2	2.1 A	0x5
Divider 3	2.4 A	0x5
HVDCP	1.5 A	0x6
Unknown 5-V Adapter	500mA	0x4

8.3.3.4 ILIM Pin (BQ25622 Only)

The ILIM pin clamps the input current limit to IINREG = K_{ILIM} / R_{ILIM}, where R_{ILIM} is connected from the ILIM pin to GND. The ILIM pin can be used to limit the input current limit from 100 mA - 3.2 A. The input current is limited to the lower of the two values set by the ILIM pin and IINDPM register bits. The ILIM pin can also be used to monitor input current. The input current is proportional to the voltage on the ILIM pin and can be calculated by IIN = (K_{ILIM} x V_{ILIM}) / (R_{ILIM} x 0.8). The ILIM pin function is disabled when the EN_EXTILIM bit is set to 0.

An RC filter in parallel with R_{ILIM} is required when the input current setting on the ILIM pin is either:

- below 400 mA or
- above 2 A when using a 2.2-µH inductor

The value for the RC filter is 1.2 kΩ and 330 nF, respectively.

8.3.3.5 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The BQ25620 and BQ25622 support a wide range of input voltage limit (3.8 V – 16.8 V). Its POR default VINDPM threshold is set at 4.6 V. The BQ25620 and BQ25622 also support dynamic VINDPM tracking, which tracks the battery voltage to ensure a sufficient margin between input and battery voltages for proper operation of the buck converter. This function is enabled via the VINDPM_BAT_TRACK register bit. When enabled, the actual input voltage limit is the higher of the VINDPM register or $V_{INDPM\_BAT\_TRACK}$ (VBAT + 400-mV typical offset.)

8.3.3.6 Converter Power-Up

After the input current and voltage limits are set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, the BATFET turns off. Otherwise, the BATFET stays on to charge the battery. Converter startup requires the following conditions:

- VBUS has passed poor source qualification (refer to Section 8.3.3.2)
- VBUS > V_{BAT} + V_{SLEEPZ}
- $V_{VBUS} < V_{VBUS\_OVP}$
- EN_HIZ = 0
- $V_{SYS} < V_{SYS\_OVP}$
- $T_J < T_{SHUT}$

The BQ25620 and BQ25622 provide soft start when the system rail is ramped up by setting IINDPM to its lowest programmable value and stepping up through each available setting until reaching the value set by IINDPM register. Concurrently, the system short protection limits the output current to approximately 0.5 A when the system rail is below V_{SYS_SHORT}.

The device uses a highly efficient 1.5-MHz, fixed frequency pulse width modulated (PWM) step-down switching regulator. The internally compensated feedback loop keep tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to pulse frequency modulation (PFM) control at light load condition. The PFM_FWD_DIS and PFM_OTG_DIS bits can be used to disable the PFM operation in buck and boost respectively.

8.3.4 Power Path Management

The BQ25620 and BQ25622 accommodate a wide range of input sources from a USB, wall adapter, wireless charger, to car charger. They provide automatic power path selection to supply the system from an input source, battery, or both.

8.3.4.1 Narrow VDC Architecture

The BQ25620 and BQ25622 use the Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by VSYSMIN register setting. Even with a fully depleted battery, the system is regulated to the minimum system voltage. If charging is enabled, the BATFET operates in linear mode (LDO mode). The default minimum system voltage at POR is 3.52 V.

As the battery voltage rises above the minimum system voltage, the BATFET is turned fully on. When battery charging is disabled and V_{BAT} is above the minimum system voltage setting, or charging is terminated, the system is regulated 50 mV (typical) above battery voltage.

8.3.4.2 Dynamic Power Management

To meet the USB maximum current limit and avoid overloading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When the input source is overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage by V_{SUPP}, the device automatically enters the supplement mode where the BATFET turns on and the battery starts discharging so that the system is supported from both the input source and battery.

8.3.4.3 High Impedance Mode

The host may place the BQ25620 and BQ25622 into high impedance mode by writing EN_HIZ = 1. In high impedance mode, RBFET (Q1), HSFET (Q2) and LSFET (Q3) are turned off. The RBFET and HSFET block current flow to and from VBUS, putting the VBUS pin into a high impedance state. The BATFET (Q4) is turned on to connect the BAT to SYS. During high impedance mode, REGN is disabled and the digital clock is slowed to conserve power.

8.3.5 Battery Charging Management

The BQ25620 and BQ25622 charge a 1-cell Li-Ion battery with up to a 3.5-A charge current. The 15-mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

8.3.5.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit = 1 and $\overline{\text{CE}}$ pin is LOW), the BQ25620 and BQ25622 autonomously complete a charging cycle without host involvement. The device default charging parameters are listed in Table 8-3. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table 8-3. Charging Parameter Default Setting

	VREG	VRECHG	ITRICKLE	IPRECHG	ICHG	ITERM	TOPOFF TIMER
BQ25620	4.2 V	VREG - 100 mV	20 mA	100 mA	1040 mA	60 mA	Disabled
BQ25622	4.2 V	VREG - 100 mV	20 mA	100 mA	1040 mA	60 mA	Disabled

A new charge cycle starts when the following conditions are valid:

- Converter starts per the conditions in Section 8.3.3.6
- EN_CHG = 1
- $\overline{\text{CE}}$ pin is low

- No thermistor fault on TS
- No safety timer fault

The BQ25620 and BQ25622 automatically terminate the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM or thermal regulation. When a fully charged battery is discharged below VRECHG, the device automatically starts a new charging cycle. After charging terminates, toggling $\overline{CE}$ pin or EN_CHG bit also initiates a new charging cycle.

The STAT output indicates the charging status. Refer to Section 8.3.8.3 for details of STAT pin operation. In addition, the status register (CHG_STAT) indicates the different charging phases: 00-charging disabled or terminated, 01-constant current, 10 constant voltage, 11-topoff charging.

8.3.5.2 Battery Charging Profile

The BQ25620 and BQ25622 charge the battery in five phases: trickle charge, pre-charge, constant current, constant voltage and an optional top-off charging phase. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

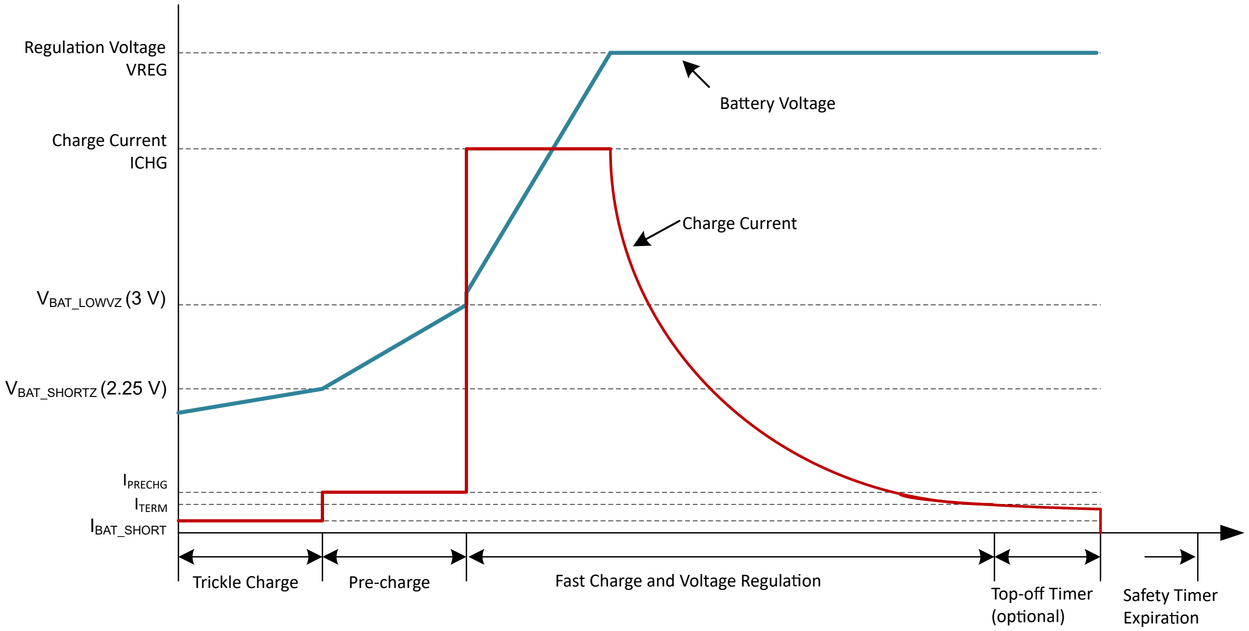


Figure 8-2. Battery Charging Profile

8.3.5.3 Charging Termination

The BQ25620 and BQ25622 terminate a charge cycle when the battery voltage is above recharge threshold, the converter is in constant-voltage regulation and the current is below ITERM. Because constant-voltage regulation is required for termination, the BQ25620 and BQ25622 do not terminate while IINDPM, VINDPM or thermal regulation loops are active. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and the BATFET can turn on again to engage supplement mode. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents, due to the comparator offset, the actual termination current may be 10 mA to 20 mA higher than the termination target. In order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The top-off timer follows safety timer constraints, such that if the safety timers suspend, so does the top-off timer. Similarly, if the safety timers count at half-clock rate, so does the top-off timer. Refer to Section 8.3.5.5 for the list of conditions. The host can read CHG_STAT to find out the termination status.

Top-off timer gets reset by any of the following conditions:

1. Charging cycle stop and restart (toggle CE pin, toggle EN_CHG bit, charged battery falls below recharge threshold or adapter removed and replugged)
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in after is detected by the charger. Programming a top-off timer value after termination has no effect unless a recharge cycle is initiated. CHG_FLAG is set to 1 when entering top-off timer segment and again when the top-off timer expires.

8.3.5.4 Thermistor Qualification

The BQ25620 and BQ25622 provide a single thermistor input for battery temperature monitoring. The TS pin input of the battery temperature can be ignored by the charger if TS_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS to always be valid for charging mode and OTG mode, and TS_STAT always reports 000. The TS pin may be left floating if TS_IGNORE is set to 1.

When TS_IGNORE=1, the TS_ADC channel is disabled, with TS_ADC_DIS forced to 1; Attempting to write to 0 is ignored.

When TS_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information according to the configurable profile described in Section 8.3.5.4.1. When the battery temperature crosses from one temperature range to another, TS_STAT is updated accordingly, and the charger sets the FLAG bit for the newly-entered temperature range. If TS_MASK is set to 0, any change to TS_STAT, including a transition to TS_NORMAL, generates an $\overline{\text{INT}}$ pulse.

8.3.5.4.1 Advanced Temperature Profile in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges. As battery technology continues to evolve, battery manufacturers have released temperature safety specifications that extend beyond the JEITA standard. The BQ25620 and BQ25622 feature a highly flexible temperature-based charging profile to meet these advanced specifications while remaining backwards compatible with the original JEITA standard. Figure 8-3 shows the programmability for charger behavior under different battery temperature (TS) operating regions.

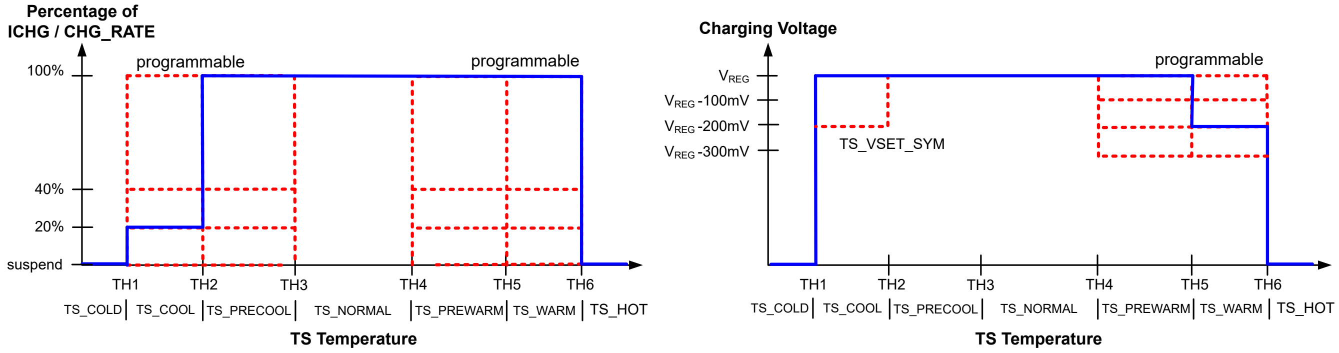


Figure 8-3. TS Charging Values

Charging safety timer is adjusted within the temperature zones to reflect changes to the charging current. When IPRECHG and ICHG are reduced to 20% or 40% in the cool or warm temperature zones, the charging safety timer counts at half rate. If charging is suspended, the safety timer is suspended, the STAT pin blinks and CHG_STAT is set to 00 (not charging or charge terminated.)

8.3.5.4.2 TS Pin Thermistor Configuration

The typical TS resistor network is illustrated below.

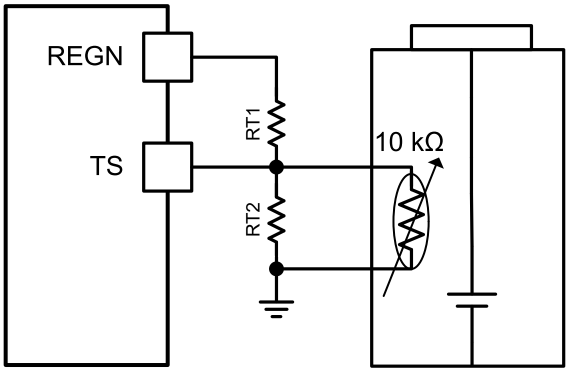


Figure 8-4. TS Resistor Network

The value of RT1 and RT2 are determined from the resistance of the thermistor at 0 and 60ºC (RTH_{0degC} and RTH_{60degC}) and the corresponding voltage thresholds V_{TS_0degC} and V_{TS_60degC} (expressed as percentage of REGN with value between 0 and 1). For the most accurate thermistor curve fitting, use the rising threshold for V_{TS_COLD} at 0ºC and the falling threshold for V_{TS_HOT} at 60ºC, regardless of the actual register settings for TS_TH1_TH2_TH3 and TS_TH4_TH5_TH6.

$$RT2 = \frac{RTH_{0degC} \times RTH_{60degC} \times \left(\frac{1}{V_{TS\_0degC}} - \frac{1}{V_{TS\_60degC}}\right)}{RTH_{60degC} \times \left(\frac{1}{V_{TS\_60degC}} - 1\right) - RTH_{0degC} \times \left(\frac{1}{V_{TS\_0degC}} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{TS\_0degC}} - 1}{\frac{1}{R_{T2}} + \frac{1}{RTH_{0degC}}} \quad (2)$$

Assuming a 103AT NTC thermistor on the battery pack, the RT1 and RT2 are calculated to be 5.32 kΩ and 30.1 kΩ respectively.

8.3.5.4.3 Cold/Hot Temperature Window in OTG Mode

For battery protection during boost OTG, BQ25620 and BQ25622 monitor the battery temperature to be within the TS_TH_OTG_COLD to TS_TH_OTG_HOT register settings. For a 103AT NTC thermistor with RT1 of 5.3 kΩ and RT2 of 31.1 kΩ, TS_TH_OTG_COLD default is -10°C and TS_TH_OTG_HOT default is 60°C. When temperature is outside of this range, the OTG mode is suspended with REGN remaining on. In addition, VBUS_STAT bits are set to 000, TS_STAT is set to 001 (TS_OTG_COLD) or 010 (TS_OTG_HOT), and TS_FLAG is set. Once the battery temperature returns to normal temperature, the boost OTG is restarted and TS_STAT returns to 000 (TS_NORMAL).

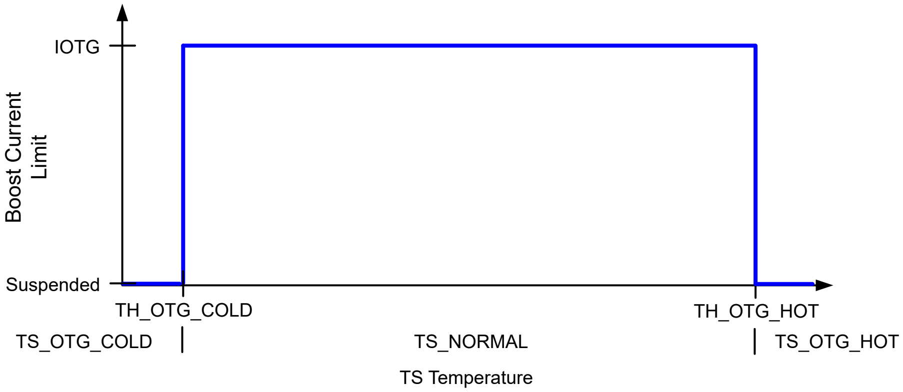


Figure 8-5. TS Pin Thermistor Sense Threshold in Boost Mode

8.3.5.4.4 JEITA Charge Rate Scaling

The TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM and TS_ISET_WARM cool and warm charge current fold backs are based on a 1C charging rate. The 1C rate is the battery capacity in mA-hours divided by 1 hour, so that a 500 mA-hour battery would have a 1C charging rate of 500 mA. The same battery would have a 2C charging rate of 1,000 mA. In order to convert the charging foldback, the host must set the CHG_RATE register to the C rate for the battery. This scales the foldback accordingly.

When TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM or TS_ISET_WARM is set to either 00 (suspend) or 11 (unchanged), the CHG_RATE setting has no effect. A summary is provided in Table 8-4.

Table 8-4. ICHG Fold Back

TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM or TS_ISET_WARM	CHG_RATE	FOLD-BACK CURRENT AS PERCENTAGE OF ICHG
00	Any	0% (Suspended)
01 (20%)	00 (1C)	20%
	01 (2C)	10%
	10 (4C)	5%
	11 (6C)	3.3%
10 (40%)	00 (1C)	40%
	01 (2C)	20%
	10 (4C)	10%
	11 (6C)	6.6%
11	Any	100%

8.3.5.4.5 TS_BIAS Pin (*BQ25622 Only*)

The The BQ25622 has the TS_BIAS pin to isolate the battery temperature sensing thermistor and associated resistor-divider from REGN. The 103AT thermistor with typical resistor-divider network requires about 400 µA to bias. The BQ25622 provides the TS_BIAS pin, which is internally connected to the REGN LDO via a back-to-back MOSFET switch. When no temperature measurement is being taken, the switch is disabled to disconnect the thermistor and resistor-divider from the REGN LDO, saving the 400-µA bias current from being expended unnecessarily.

The TS_BIAS pin has short-circuit protection. If a short is detected on the TS_BIAS pin, the switch is disabled to disconnect the short from REGN. If this condition occurs, TS_STAT register is set to 0x3. Charging and OTG modes are suspended until the short is removed.

8.3.5.5 Charging Safety Timers

The BQ25620 and BQ25622 have three built-in safety timers to prevent extended charging cycle due to abnormal battery conditions. The fast charge safety timer and pre-charge safety timers are set through I^2C CHG_TMR and PRECHG_TMR fields, respectively. The trickle charge timer is fixed at 1 hour.

The trickle charging, pre-charging and fast charging safety timers can be disabled by setting EN_SAFETY_TMRS = 0. EN_SAFETY_TMRS can be enabled anytime regardless of which charging stage the charger is in. Each timer starts to count as soon as the following two conditions are simultaneously true: EN_SAFETY_TMRS=1 and the corresponding charging stage is active.

When either the fast charging, trickle charging or pre-charging safety timer expires, the SAFETY_TMR_STAT and SAFETY_TMR_FLAG bits are set to 1.

Events that cause a reduction in charging current also cause the charging safety timer to count at half-clock rate if TMR2X_EN bit is set.

During faults which suspend charging, the charge, pre-charge and trickle safety timers are also suspended, regardless of the state of the TMR2X_EN bit. Once the fault goes away, charging resumes and the safety timer resumes from where it stopped.

The charging safety timer and the charging termination can be disabled at the same time. Under this condition, the charging keeps running until it is disabled by the host.

8.3.6 USB On-The-Go (OTG)

8.3.6.1 Boost OTG Mode

BQ25620 and BQ25622 support boost converter operation to deliver power from the battery to VBUS. The output voltage and maximum current are set in the VOTG and IOTG registers, respectively. VBUS_STAT is set to 111 upon a successful entry into boost OTG. The boost operation is enabled when the following conditions are met:

1. BAT above V_{BAT_OTG}
2. VBUS less than V_{BAT}+V_{SLEEP}
3. Boost mode operation is enabled (EN_OTG = 1)
4. $V_{TS\_OTG\_HOT} < V_{TS} < V_{TS\_OTG\_COLD}$
5. $V_{REGN} > V_{REGN\_OK}$
6. 30 ms delay after EN_OTG = 1
7. Boost mode regulation voltage in REG0x0C is greater than 105% of battery voltage.

8.3.7 Integrated 12-Bit ADC for Monitoring

The BQ25620 and BQ25622 provide an integrated 12-bit ADC for the host to monitor various system parameters.

To enable the ADC, the ADC_EN bit must be set to ‘1’. The ADC is disabled by default (ADC_EN = 0) to conserve power. The ADC is allowed to operate if either VBUS > $V_{POORSRC}$ or VBAT > V_{BAT_LOWV} is valid. If ADC_EN is set to ‘1’ before VBUS or VBAT reach their respective valid thresholds, then ADC_EN stays '0'. The host can enable the ADC during HIZ mode by setting ADC_EN = 1.

At battery only condition, if the TS_ADC channel is enabled, the ADC only operates when the battery voltage is higher than 3.2 V (the minimal value to turn on REGN), otherwise, the ADC operates when the battery voltage is higher than V_{BAT_LOWV}.

The ADC_DONE_STAT, ADC_DONE_FLAG bits are set when a conversion is complete in one-shot mode only. During continuous conversion mode, the ADC_DONE_STAT, ADC_DONE_FLAG bits have no meaning and remain at 0. In one-shot mode, the ADC_EN bit is set to 0 at the completion of the conversion, at the same time as the ADC_DONE_FLAG bit is set. In continuous mode, the ADC_EN bit remains at 1 until the user disables the ADC by setting it to 0.

8.3.8 Status Outputs ($\overline{\text{PG}}$, STAT, $\overline{\text{INT}}$)

8.3.8.1 $\overline{\text{PG}}$ Pin Power Good Indicator

The $\overline{\text{PG}}$ pin goes LOW to indicate a good input source when:

- V_{VBUS} is above V_{VBUS_UVLOZ}
- V_{VBUS} is above battery (not in sleep)
- V_{VBUS} is below V_{VBUS_OVP} threshold
- V_{VBUS} is above $V_{POORSRC}$ when $I_{POORSRC}$ current is applied (not a poor source)

8.3.8.2 Interrupts and Status, Flag and Mask Bits

The device incorporates an interrupt pin ($\overline{\text{INT}}$) to inform a host microcontroller of status changes without requiring microcontroller polling. Each reported event has a status field, a flag bit and a mask bit. The status field reports the status at the time that it is read. The flag bit is latched and, once set to 1, will remain at 1 until the host reads the bit, which will clear it to 0. The mask bit determines whether or not an interrupt pulse will be generated when the flag bit is set.

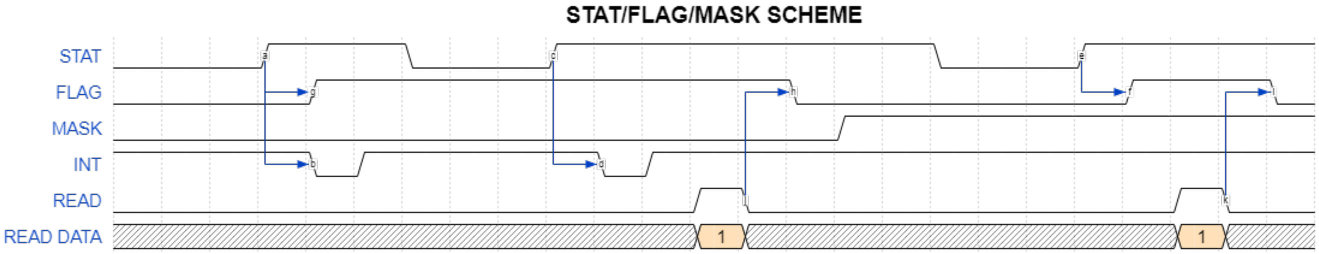


Figure 8-6. Relationship Between STAT, FLAG, and MASK

The flag bit is set upon certain transitions of the status field. These transitions also generate an $\overline{\text{INT}}$ pulse if the associated mask bit is set to 0. Because the $\overline{\text{INT}}$ is generated from the status field transition and not the flag bit, an $\overline{\text{INT}}$ pulse is sent to the host even if the associated flag is already set to 1 when the status transition occurs. Details of this behavior are shown in Figure 8-6.

The default behavior is to generate a 256-μs $\overline{\text{INT}}$ pulse when any flag bit is set to 1. These pulses may be masked out on a flag-by-flag basis by setting a flag's mask bit to 1. Setting the mask bit does not affect the transition of the flag bit from 0 to 1, only the generation of the 256-μs $\overline{\text{INT}}$ pulse.

8.3.8.3 Charging Status Indicator (STAT)

The BQ25620 and BQ25622 indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. The STAT pin function can be disabled via the DIS_STAT bit.

Table 8-5. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Not charging, no fault detected. (Includes charging complete, Charge Disabled, no adapter present, in OTG mode.)	HIGH
Charge suspend	Blinking at 1 Hz

8.3.8.4 Interrupt to Host ($\overline{\text{INT}}$)

In many applications, the host does not continually poll the charger status registers. Instead, the INT pin may be used to notify the host of a status change with a 256-μs $\overline{\text{INT}}$ pulse. Upon receiving the interrupt pulse, the host may read the flag registers (Charger_Flag_X and FAULT_Flag_X) to determine the event that caused the interrupt, and for each flagged event, read the corresponding status registers (Charger_Status_X and FAULT_Status_X) to determine the current state. Once set to 1, the flag bits remain latched at 1 until they are read by the host, which clears them. The status bits, however, are updated whenever there is a change to status and always represent the current state of the system.

All of the $\overline{\text{INT}}$ events can be masked off to prevent $\overline{\text{INT}}$ pulses from being sent out when they occur, with the exception of the initial power-up interrupt. Interrupt events are masked by setting their mask bit in registers (Charger_Mask_X and FAULT_Mask_X). Events always cause the corresponding flag bit to be set to 1, regardless of whether or not the interrupt pulse has been masked.

8.3.9 BATFET Control

The BQ25620 and BQ25622 have an integrated, bi-directionally blocking BATFET that can be turned off to remove leakage current from the battery to the system. The BATFET is controlled by the BATFET_CTRL register bits, and supports shutdown mode, ship mode and system power reset.

Table 8-6. BATFET Control Modes

MODE	BATFET	I^2C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 1	EXIT
Normal	On	Active	N/A	N/A	N/A	N/A

Table 8-6. BATFET Control Modes (continued)

MODE	BATFET	I^2C	ENTRY, NO ADAPTER	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 0	ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 1	EXIT
Ship mode	Off	Off	Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY and enters ship mode.	Writing BATFET_CTRL = 10 has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters ship mode. Writing BATFET_CTRL = 00 before adapter is removed aborts ship mode.	Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters ship mode. Writing BATFET_CTRL = 00 before adapter is removed turns BATFET on and aborts ship mode.	$\overline{\text{QON}}$ or adapter plug-in
System reset	On to Off to On	Active	Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding $\overline{\text{QON}}$ low for t_{QON_RST} initiates immediate reset (BATFET_DLY is not applied.)	Writing BATFET_CTRL = 11 is ignored and BATFET_CTRL resets to 00. Holding $\overline{\text{QON}}$ low for t_{QON_RST} is ignored.	Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding $\overline{\text{QON}}$ low for t_{QON_RST} initiates immediate reset. Converter is placed in HIZ during system reset and exits HIZ when system reset completes.	N/A
Shutdown mode	Off	Off	Writing BATFET_CTRL = 01 turns off BATFET after BATFET_DLY and enters shutdown.	Writing BATFET_CTRL = 01 with adapter present is ignored, regardless of BATFET_CTRL_WVBUS setting, and BATFET_CTRL is reset to 00.		Adapter plug-in

8.3.9.1 Shutdown Mode

For the lowest battery leakage current, the host can shut down the BQ25620 and BQ25622 by setting the register bits BATFET_CTRL to 01. In this mode, the BATFET is turned off to prevent the battery from powering the system, the I^2C is disabled and the charger is totally shut down. The BQ25620 and BQ25622 can only be woken up by plugging in an adapter. When the adapter is plugged in, the BQ25620 and BQ25622 start back up with all register settings in their POR default.

After the host sets BATFET_CTRL to 01, the BATFET turns off after waiting either 20 ms or 10 s as configured by BATFET_DLY register bit. Shutdown mode can only be entered when $V_{VBUS} < V_{VBUS\_UVLO}$, regardless of the BATFET_CTRL_WVBUS setting, which has no effect on shutdown mode entry. If the host writes BATFET_CTRL = 01 with $V_{VBUS} > V_{VBUS\_UVLOZ}$, the request is ignored and the BATFET_CTRL bits are set back to 00.

If the host writes BATFET_CTRL to 01 while boost OTG, the BQ25620 and BQ25622 first exit from boost OTG by setting EN_OTG = 0 and then enters shutdown mode.

$\overline{\text{QON}}$ has no effect during shutdown mode. The internal pull-up on the $\overline{\text{QON}}$ pin is disabled during shutdown to prevent leakage through the pin.

8.3.9.2 Ship Mode

The host may place the BQ25620 and BQ25622 into ship mode by setting BATFET_CTRL = 10. In ship mode, the BATFET is turned off to prevent the battery from powering the system, and the I^2C is disabled. Ship mode has slightly higher quiescent current than shutdown mode, but $\overline{\text{QON}}$ may be used to exit from ship mode. The BQ25620 and BQ25622 are taken out of ship mode by either of these methods:

- Pulling the $\overline{\text{QON}}$ pin low for t_{SM_EXIT}
- $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter plug-in)

When the BQ25620 and BQ25622 exit from ship mode, the registers are reset to their POR values.

Ship mode is only entered when the adapter is not present. Setting BATFET_CTRL = 10 while $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter present) either disables the BATFET or has no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

When BATFET_CTRL_WVBUS is set to 0 and $V_{VBUS} > V_{VBUS\_UVLO}$ (adapter present), setting BATFET_CTRL = 10 has no immediate effect. If the adapter is removed while BATFET_CTRL is set to 10, then the BATFET is disabled and the device enters ship mode. The BATFET turns off either after t_{BATFET_DLY} or when the adapter is removed, whichever comes later.

When BATFET_CTRL_WVBUS is set to 1 and $V_{VBUS} > V_{VBUS\_UVLO}$ (adapter present), setting BATFET_CTRL = 10 turns off the BATFET after t_{BATFET_DLY}. The converter continues to run while the adapter is present, supplying SYS power from the adapter. If the adapter is removed while BATFET_CTRL is set to 10, the BQ25620 and BQ25622 enters ship mode. Ship mode is entered either after t_{BATFET_DLY} or when the adapter is removed, whichever comes later.

8.3.9.3 System Power Reset

The BATFET functions as a load switch between battery and system when the converter is not running. By changing the state of BATFET from on to off, systems connected to SYS can be power cycled. Any of the following conditions initiates a system power reset:

- BATFET_CTRL_WVBUS = 1 and $\overline{\text{QON}}$ is pulled low for tQON_RST
- BATFET_CTRL_WVBUS = 1 and BATFET_CTRL = 11
- BATFET_CTRL_WVBUS = 0 and VBUS < V_{VBUS_UVLO} simultaneously with $\overline{\text{QON}}$ pulled low for tQON_RST
- BATFET_CTRL_WVBUS = 0 and VBUS < V_{VBUS_UVLO} and BATFET_CTRL = 11

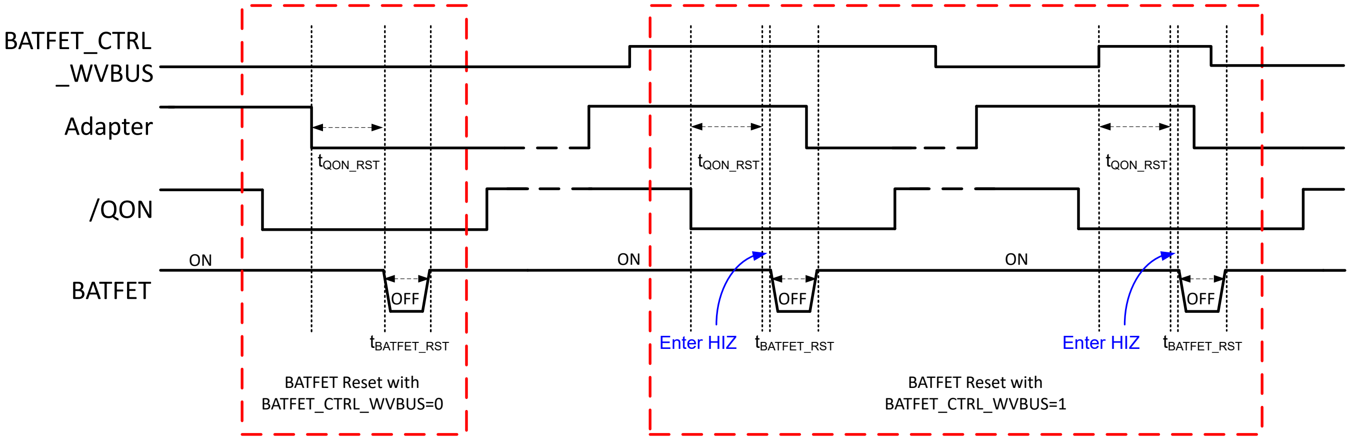


Figure 8-7. System Power Reset Timing

When BATFET_CTRL_WVBUS is set to 1, system power reset proceeds if either BATFET_CTRL is set to 11 or $\overline{\text{QON}}$ is pulled low for t_{QON_RST}, regardless of whether VBUS is present or not . There is a delay of t_{BATFET_DLY} before initiating the system power reset. If $\overline{\text{QON}}$ is pulled low, there is no delay after the tQON_RST completes, regardless of BATFET_DLY setting.

The system power reset can be initiated from the battery only condition, from OTG mode or from the forward charging mode with adapter present. If the system power is reset when the charger is in boost OTG mode, the boost OTG mode is first stopped by setting EN_OTG = 0.

8.3.10 Protections

8.3.10.1 Voltage and Current Monitoring in Battery Only and HIZ Modes

The BQ25620 monitors a reduced set of voltages and currents when operating from battery without an adapter or when operating from battery in high impedance mode.

8.3.10.1.1 Battery Undervoltage Lockout

In battery-only mode, the BQ25620 disables the BATFET if V_{BAT} falls below V_{BAT_UVLO}, separating the system from the battery. I^{2}C is disabled as well. Upon exit from the undervoltage lockout condition when either V_{BAT} rises above V_{BAT_UVLOZ} or V_{VBUS} rises above V_{VBUS_UVLOZ}, I^{2}C will be re-enabled and the registers are reset to their POR values.

8.3.10.1.2 Battery Overcurrent Protection

The BQ25620 has a two-level battery overcurrent protection. The I_{BAT_PK} threshold is set by IBAT_PK and provides a fast (100 µs) protection for the battery discharging. I_{BATFET_OCP} provides a slower (50 ms), fixed-threshold protection for the BATFET. If the battery discharge current becomes higher than either threshold for its protection timer, the BAT_FAULT_STAT and BAT_FAULT_FLAG fault register bits are set to 1, and the BATFET enters hiccup mode with 100-ms off-time and ~1% on-time. The BAT_FAULT_STAT will return to 0 once the BATFET is disabled for the hiccup mode. Once the BATFET is turned back on, the I_{BAT_PK} and I_{BATFET_OCP} thresholds are re-evaluated. In boost OTG mode, if the battery discharging current is higher than either I_{BAT_PK} or I_{BATFET_OCP} for their respective protection timers, the charger exits OTG mode by clearing the EN_OTG bit.

8.3.10.2 Voltage and Current Monitoring in Buck Mode

8.3.10.2.1 Input Overvoltage

If VBUS voltage rises above V_{VBUS_OVP}, the converter stops switching to protect the internal power MOSFETs and I_{PMID_LOAD} discharge current is applied to bring down VBUS voltage. VBUS_FAULT_FLAG and VBUS_FAULT_STAT are set to 1. When VBUS falls back below V_{VBUS_OVPZ}, VBUS_OVP_STAT will transition to 0 and the converter will resume switching.

8.3.10.2.2 System Overvoltage Protection (SYSOVP)

When VSYS rises above the V_{SYS_OVP} threshold (around 250 mV above VBAT when not charging) in forward converter operation, the converter stops switching to limit voltage overshoot and applies I_{SYS_LOAD} to pull down the system voltage. VSYS_FAULT_FLAG and VSYS_FAULT_STAT are set to 1. Once VSYS drops below V_{SYS_OVP}, the converter resumes switching, the 30 mA discharge current is removed and VSYS_FAULT_STAT transitions to 0.

8.3.10.2.3 Forward Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In forward mode, if the current through Q2 exceeds I_{HSFET_OCP}, the converter will immediately turn off the high-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

8.3.10.2.4 System Short

When the SYS voltage falls below V_{SYS_SHORT}, the charger enters PFM operation to limit the output current to approximately 0.5 A or less. SYS_FAULT_STAT and SYS_FAULT_FLAG bits are set to 1. If V_{SYS} rises above V_{SYS_SHORTZ}, the converter exits forced PFM mode, and the SYS_FAULT_STAT bit is set to 0.

8.3.10.2.5 Battery Overvoltage Protection (BATOVP)

When V_{BAT} transitions above V_{BAT_OVP}, the BQ25620 disables charging by disabling the BATFET and applies I_{BAT_LOAD} current source to discharge excess BAT voltage. If battery voltage remains above the threshold , BAT_FAULT_FLAG is set to 1 and BAT_FAULT_STAT transitions to 1. Once V_{BAT} falls below V_{BAT_OVPZ}, charging resumes and BAT_FAULT_STAT transitions back to 0.

8.3.10.2.6 Sleep and Poor Source Comparators

The sleep comparator is used to suspend the converter if the adapter voltage is insufficient to maintain buck converter operation while charging the battery. If V_{VBUS} falls below V_{BAT} + V_{SLEEP} , the converter stops switching, the $\overline{PG}$ pin transitions high, and VBUS_FAULT_STAT and VBUS_FAULT_FLAG are set to 1. If V_{VBUS} rises back above V_{BAT} + V_{SLEEPZ} , the converter restarts, and the $\overline{PG}$ pin transitions low.

If V_{VBUS} falls below $V_{POORSRC}$, the converter stops switching and the $\overline{PG}$ pin transitions high (if not already suspended and high due to the sleep comparator), and the VBUS_STAT transitions to 000 and the device transitions to battery-only mode. If V_{VBUS} rises above $V_{POORSRC}$, it is a new adapter attach, and poor source qualification will be run in addition to D+/D- detection if enabled. VBUS_STAT and the $\overline{PG}$ pin state will be determined by the adapter attach sequence as outlined in Section 8.3.3.

8.3.10.3 Voltage and Current Monitoring in Boost Mode

BQ25620 closely monitors VBUS, SYS and BAT voltages, as well as VBUS, BAT and LSFET currents to ensure safe boost mode operation.

8.3.10.3.1 Boost Mode Overvoltage Protection

During OTG operation, BQ25620 uses two comparators to sense output overvoltage at VBUS and PMID. If either VBUS or PMID voltage rises above their OVP threshholds, the converter stops switching and attempts to discharge the voltage.

If the OVP condition persists (200 µs), OTG_FAULT_FLAG is set to 1, OTG_FAULT_STAT transitions to 1 and the converter powers down into a fault condition.

8.3.10.3.2 Boost Mode Duty Cycle Protection

After an initial startup blanking period, BQ25620 monitors the PMID voltage during boost OTG mode to ensure that PMID voltage remains sufficiently above VSYS to maintain the minimum duty cycle. If V_{PMID} falls below V_{BOOST_DUTY} (105% V_{SYS} typical), the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

8.3.10.3.3 Boost Mode PMID Undervoltage Protection

During boost OTG mode, BQ25620 converter monitors PMID for undervoltage. If the PMID voltage falls below V_{OTG_UVP}, the converter stops and enters hiccup mode.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

8.3.10.3.4 Boost Mode Battery Undervoltage

If V_{BAT} falls below V_{BAT_OTGZ} during OTG mode, the charger exits OTG mode by setting EN_OTG = 0, and BAT_FAULT_STAT and BAT_FAULT_FLAG are set to 1. Setting EN_OTG = 1 while $V_{BAT} < V_{BAT\_OTG}$ will not enter OTG and the EN_OTG bit will be cleared to 0. When the battery is charged above V_{BAT_OTG}, OTG mode may be entered by setting EN_OTG = 1.

8.3.10.3.5 Boost Converter Cycle-by-Cycle Current Limit

The converter has cycle-by-cycle peak overcurrent protection in the switching MOSFETs. In OTG mode, if the current through Q3 exceeds I_{LSFET_OCP}, the converter will immediately turn off the low-side gate drive for the remainder of the switching cycle. Normal switching resumes on the next switching cycle.

8.3.10.3.6 Boost Mode SYS Short

If VSYS falls below VSYS_SHORT in boost OTG mode, BQ25620 immediately stops the boost converter, enters hiccup mode, and sets SYS_FAULT_FLAG to 1.

If the boost converter cannot recover from hiccup mode, EN_OTG bit is cleared and the device exits boost mode. The host may attempt to restart boost OTG mode by setting EN_OTG = 1.

8.3.10.4 Thermal Regulation and Thermal Shutdown

8.3.10.4.1 Thermal Protection in Buck Mode

The BQ25620 monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in buck mode. When the internal junction temperature exceeds the T_{REG} thermal regulation limit (TREG register configuration), the device lowers the charging current. During thermal regulation, the safety timer runs at half the clock rate, and the TREG_FLAG and TREG_STAT bits are set to 1. Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET and converter are re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

8.3.10.4.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT}, the boost mode is disabled by setting EN_OTG bit low and BATFET is turned off, and TSHUT_FLAG is set to 1. When IC junction temperature is below T_{SHUT} - T_{SHUT_HYS}, the BATFET is enabled automatically to allow system to restore and the host can re-enable EN_OTG bit to recover.

8.3.10.4.3 Thermal Protection in Battery-Only Mode

The BQ25620 monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in battery-only mode. The device has thermal shutdown to turn off the BATFET when IC junction temperature exceeds T_{SHUT}. The fault bit TSHUT_FLAG is set to 1 and TSHUT_STAT transitions to 1. The BATFET is re-enabled when IC temperature is T_{SHUT_HYS} below T_{SHUT}, and TSHUT_STAT transitions to 0.

8.4 Device Functional Modes

8.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an $\overline{\text{INT}}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck converter continues to operate to supply system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog expires, the device returns to default mode. The ICHG value is divided in half when the watchdog timer expires, and a number of other fields are reset to their POR default values as shown in the notes column of the register tables in Section 8.6. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an $\overline{\text{INT}}$ is asserted low to alert the host (unless masked by WD_MASK).

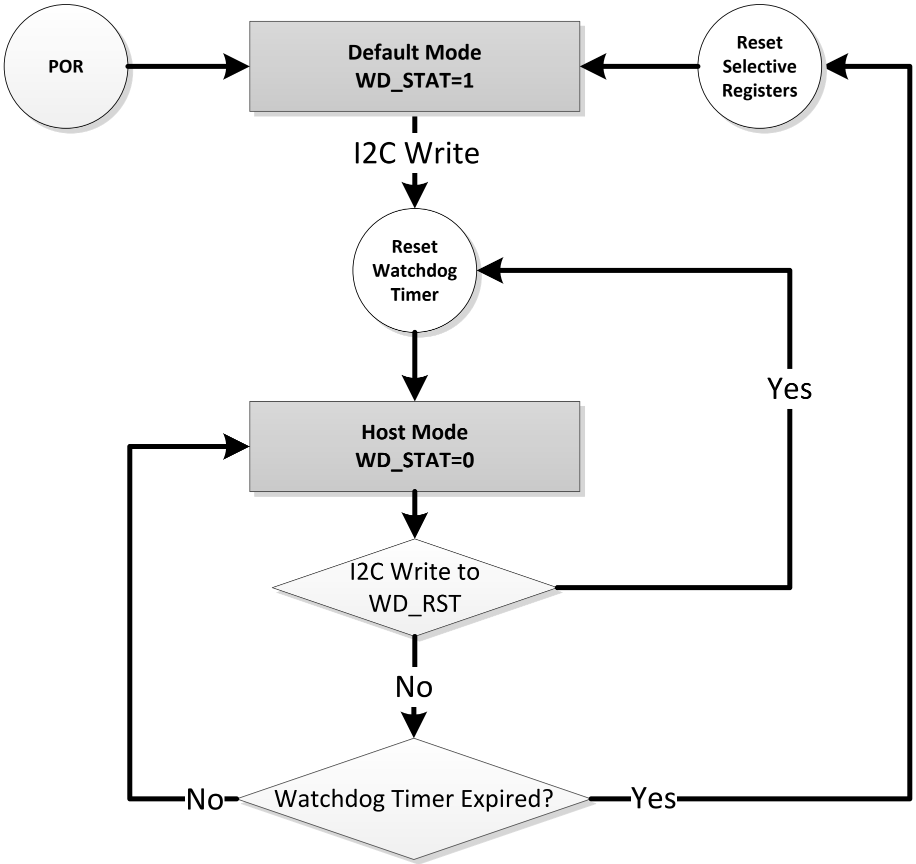


Figure 8-8. Watchdog Timer Flow Chart

8.4.2 Register Bit Reset

Beside a register reset by the watchdog timer in default mode, the register and the timer can be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit goes back from 1 to 0 automatically.

8.5 Programming

8.5.1 Serial Interface

The BQ25620 and BQ25622 uses an I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL).

The device has 7-bit I^2C address 0x6B, receiving control inputs from a host device such as a micro-controller or digital signal processor through register addresses 0x02 – 0x38. The host device initiates all transfers and the charger responds. Register reads outside of these addresses return 0xFF. When the bus is free, both SDA and SCL lines are HIGH.

The I^2C interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s) and fast mode plus (up to 1 Mbits/s.) These lines are pulled up to a reference voltage via pull-up resistor. The device I^2C detection thresholds support a communication reference voltage from 1.2 V to 5 V.

Due to the ultra low I_Q when the device operates in low power mode, it is necessary ensure a minimum of 128μs between a START command and any subsequent START command on the I^2C bus. The recommended minimum t_{buf} (bus free time between a STOP and START condition) depends on the I^2C mode:

- Standard mode (100 kbits/s):
  - No additional requirements
- Fast mode (400 kbits/s):
  - Increase I^2C t_{buf} to at least 80 μs
  - If using repeated start commands, ensure I^2C tsu:STA is at least 80 μs
- Fast mode plus (1 Mbits/s):
  - Increase I^2C t_{buf} to at least 120 μs
  - If using repeated start commands, ensure I^2C tsu:STA is at least 120 μs

These recommendations assume a successful I^2C transaction. It is also necessary to ensure a minimum 128μs time between two START commands in the case of a NACK.

8.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

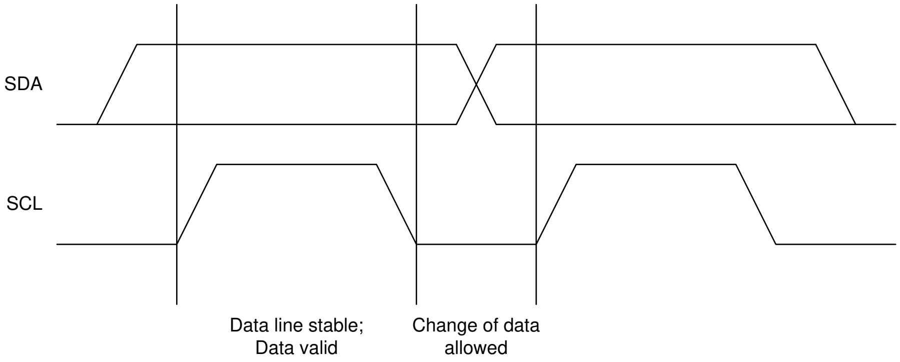


Figure 8-9. Bit Transfer on the I^2C Bus

8.5.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

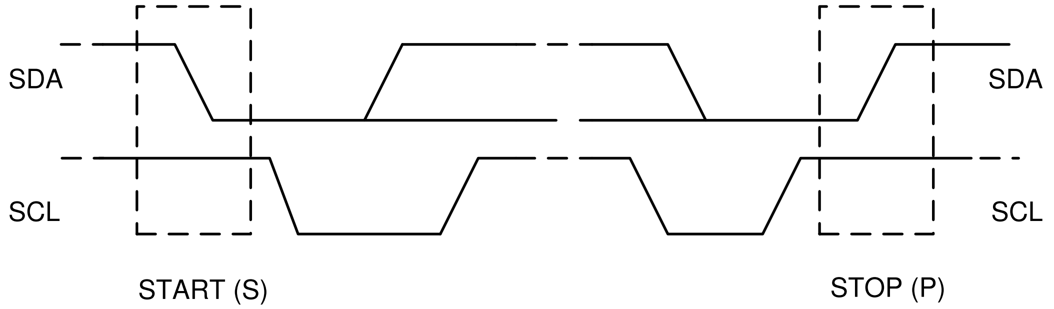


Figure 8-10. START and STOP Conditions on the I^{2}C Bus

8.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

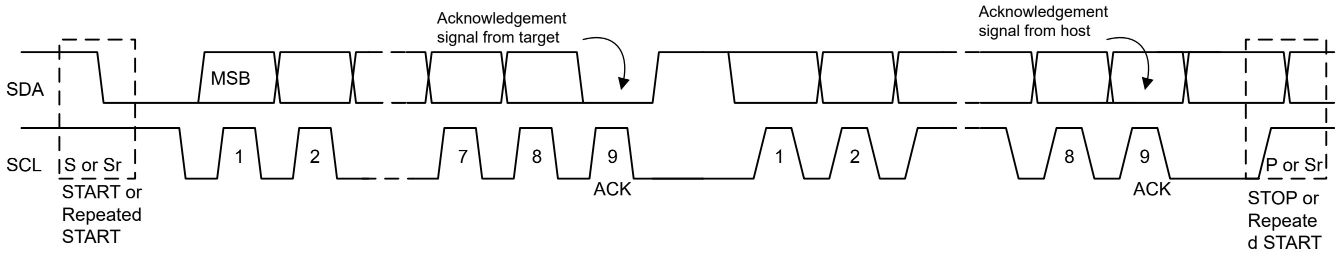


Figure 8-11. Data Transfer on the I^{2}C Bus

8.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the target to signal the host that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The host releases the SDA line during the acknowledge clock pulse so the target can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.5.1.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 011' (0x6B).

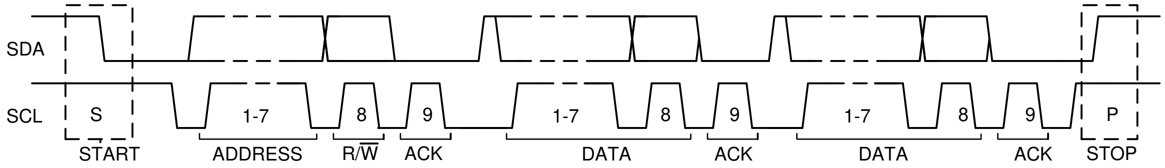


Figure 8-12. Complete Data Transfer on the I^{2}C Bus

8.5.1.6 Single Write and Read

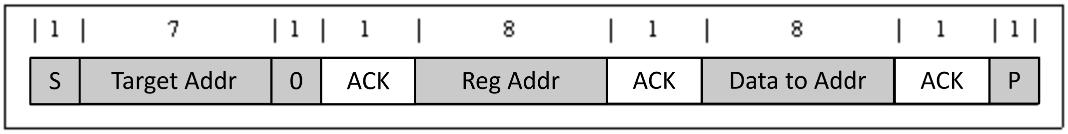


Figure 8-13. Single Write

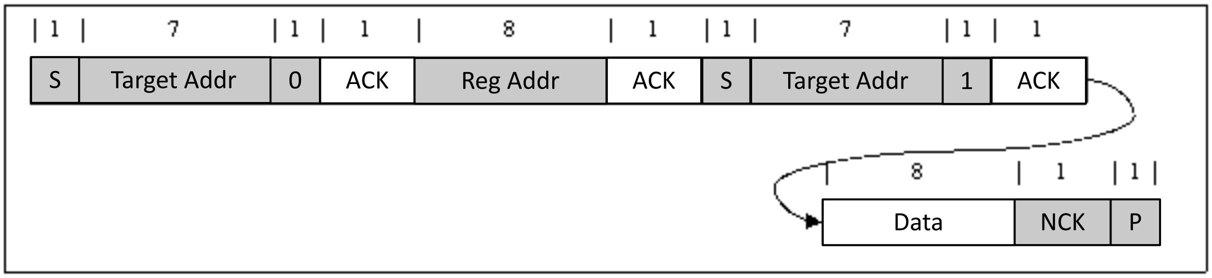


Figure 8-14. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

8.5.1.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map may be read in a single operation with a 39-byte read that starts at register address 0x01.

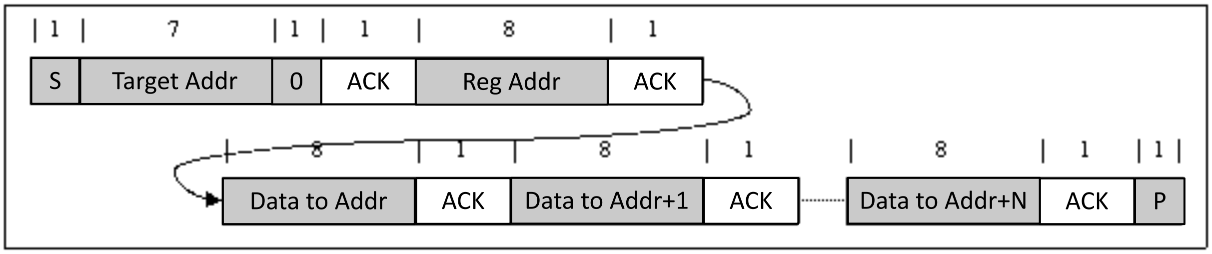


Figure 8-15. Multi-Write

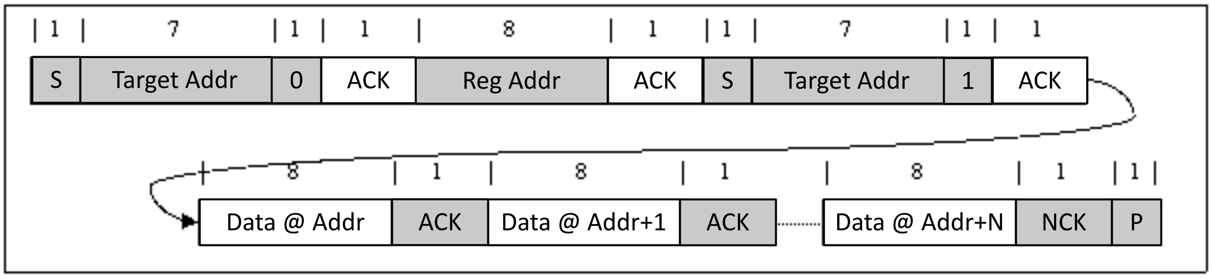


Figure 8-16. Multi-Read

8.6 Register Maps

I^{2}C Device Address: 0x6B.

8.6.1 Register Programming

The BQ25620 and BQ25622 contain 8-bit and 16-bit registers. When writing to 16-bit registers, I^{2}C transactions follow the little endian format, starting at the address of the least significant byte and writing both register bytes in a single 16-bit transaction.

8.6.2 BQ25620 Registers

Table 8-7 lists the memory-mapped registers for the BQ25620 registers. All register offset addresses not listed in Table 8-7 should be considered as reserved locations and the register contents should not be modified.

Table 8-7. BQ25620 Registers

Address	Acronym	Register Name	Section
2h	REG0x02_Charge_Current_Limit	Charge Current Limit	Go
4h	REG0x04_Charge_Voltage_Limit	Charge Voltage Limit	Go
6h	REG0x06_Input_Current_Limit	Input Current Limit	Go
8h	REG0x08_Input_Voltage_Limit	Input Voltage Limit	Go
Ah	REG0x0A_IOTG_regulation	IOTG regulation	Go
Ch	REG0x0C_VOTG_regulation	VOTG regulation	Go
Eh	REG0x0E_Minimal_System_Voltage	Minimal System Voltage	Go
10h	REG0x10_Pre-charge_Control	Pre-charge Control	Go
12h	REG0x12_Termination_Control	Termination Control	Go
14h	REG0x14_Charge_Control_0	Charge Control 0	Go
15h	REG0x15_Charge_Timer_Control	Charge Timer Control	Go
16h	REG0x16_Charger_Control_1	Charger Control 1	Go
17h	REG0x17_Charger_Control_2	Charger Control 2	Go
18h	REG0x18_Charger_Control_3	Charger Control 3	Go
19h	REG0x19_Charger_Control_4	Charger Control 4	Go
1Ah	REG0x1A_NTC_Control_0	NTC Control 0	Go
1Bh	REG0x1B_NTC_Control_1	NTC Control 1	Go
1Ch	REG0x1C_NTC_Control_2	NTC Control 2	Go
1Dh	REG0x1D_Charger_Status_0	Charger Status 0	Go
1Eh	REG0x1E_Charger_Status_1	Charger Status 1	Go
1Fh	REG0x1F_FAULT_Status_0	FAULT Status 0	Go
20h	REG0x20_Charger_Flag_0	Charger Flag 0	Go
21h	REG0x21_Charger_Flag_1	Charger Flag 1	Go
22h	REG0x22_FAULT_Flag_0	FAULT Flag 0	Go
23h	REG0x23_Charger_Mask_0	Charger Mask 0	Go
24h	REG0x24_Charger_Mask_1	Charger Mask 1	Go
25h	REG0x25_FAULT_Mask_0	FAULT Mask 0	Go
26h	REG0x26_ADC_Control	ADC Control	Go
27h	REG0x27_ADC_Function_Disable_0	ADC Function Disable 0	Go
28h	REG0x28_IBUS_ADC	IBUS ADC	Go
2Ah	REG0x2A_IBAT_ADC	IBAT ADC	Go
2Ch	REG0x2C_VBUS_ADC	VBUS ADC	Go
2Eh	REG0x2E_VPMID_ADC	VPMID ADC	Go
30h	REG0x30_VBAT_ADC	VBAT ADC	Go
32h	REG0x32_VSYS_ADC	VSYS ADC	Go
34h	REG0x34_TS_ADC	TS ADC	Go
36h	REG0x36_TDIE_ADC	TDIE ADC	Go
38h	REG0x38_Part_Information	Part Information	Go

Complex bit access types are encoded to fit into small table cells. Table 8-8 shows the codes that are used for access types in this section.

Table 8-8. BQ25620 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

8.6.2.1 REG0x02_Charge_Current_Limit Register (Address = 2h) [Reset = 0340h]

REG0x02_Charge_Current_Limit is shown in Figure 8-17 and described in Table 8-9.

Return to the Summary Table.

Charge Current Limit

Figure 8-17. REG0x02_Charge_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				ICHG			
R-0h				R/W-Dh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ICHG		RESERVED					
R/W-Dh		R-0h					

Table 8-9. REG0x02_Charge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:6	ICHG	R/W	Dh	Charge Current Regulation Limit: This 16-bit register follows the little-endian convention. ICHG[5:2] falls in REG0x03[3:0], and ICHG[1:0] falls in REG0x02[7:6]. POR: 1040mA (Dh) Range: 80mA-3520mA (1h-2Ch) Clamped Low Clamped High Bit Step: 80mA (1h) NOTE: When Q4_FULLON=1, this register has a minimum value of 160mA
5:0	RESERVED	R	0h	Reserved

8.6.2.2 REG0x04_Charge_Voltage_Limit Register (Address = 4h) [Reset = 0D20h]

REG0x04_Charge_Voltage_Limit is shown in Figure 8-18 and described in Table 8-10.

Return to the Summary Table.

Charge Voltage Limit

Figure 8-18. REG0x04_Charge_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED				VREG			
R-0h				R/W-1A4h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VREG					RESERVED		
R/W-1A4h					R-0h		

Figure 8-18. REG0x04_Charge_Voltage_Limit Register (continued)

Table 8-10. REG0x04_Charge_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:3	VREG	R/W	1A4h	Battery Voltage Regulation Limit: This 16-bit register follows the little-endian convention. VREG[8:5] falls in REG0x05[3:0], and VREG[4:0] falls in REG0x04[7:3]. POR: 4200mV (1A4h) Range: 3500mV-4800mV (15Eh-1E0h) Clamped Low Clamped High Bit Step: 10mV
2:0	RESERVED	R	0h	Reserved

8.6.2.3 REG0x06_Input_Current_Limit Register (Address = 6h) [Reset = 0A00h]

REG0x06_Input_Current_Limit is shown in Figure 8-19 and described in Table 8-11.

Return to the Summary Table.

Input Current Limit

Figure 8-19. REG0x06_Input_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED				IINDPM			
R-0h				R/W-A0h			

7	6	5	4	3	2	1	0
IINDPM				RESERVED			
R/W-A0h				R-0h			

Table 8-11. REG0x06_Input_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:4	IINDPM	R/W	A0h	Input Current Regulation Limit: This 16-bit register follows the little-endian convention. IINDPM[7:4] falls in REG0x07[3:0], and IINDPM[3:0] falls in REG0x06[7:4]. BQ25620: Based on D+/D- detection results: USB SDP = 500mA USB CDP = 1.5A USB DCP = 1.5A USB HVDCP = 1.5A Unknown Adapter = 500mA Non-Standard Adapter = 1A/2.1A/2.4A POR: 3200mA (A0h) Range: 100mA-3200mA (5h-A0h) Clamped Low Clamped High Bit Step: 20mA When the adapter is removed, IINDPM is reset to its POR value of 3.2 A.
3:0	RESERVED	R	0h	Reserved

8.6.2.4 REG0x08_Input_Voltage_Limit Register (Address = 8h) [Reset = 0E60h]

REG0x08_Input_Voltage_Limit is shown in Figure 8-20 and described in Table 8-12.

Return to the Summary Table.

Input Voltage Limit

Figure 8-20. REG0x08_Input_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED		VINDPM					
R-0h		R/W-73h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VINDPM			RESERVED				
R/W-73h			R-0h				

Table 8-12. REG0x08_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0h	Reserved
13:5	VINDPM	R/W	73h	Absolute Input Voltage Regulation Limit: This 16-bit register follows the little-endian convention. VINDPM[8:3] falls in REG0x09[5:0], and VINDPM[2:0] falls in REG0x08[7:5]. POR: 4600mV (73h) Range: 3800mV-16800mV (5Fh-1A4h) Clamped Low Clamped High Bit Step: 40mV
4:0	RESERVED	R	0h	Reserved

8.6.2.5 REG0x0A_IOTG_regulation Register (Address = Ah) [Reset = 0320h]

REG0x0A_IOTG_regulation is shown in Figure 8-21 and described in Table 8-13.

Return to the Summary Table.

IOTG regulation

Figure 8-21. REG0x0A_IOTG_regulation Register

15	14	13	12	11	10	9	8
RESERVED				IOTG			
R-0h				R/W-32h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IOTG				RESERVED			
R/W-32h				R-0h			

Table 8-13. REG0x0A_IOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:4	IOTG	R/W	32h	OTG mode current regulation limit: This 16-bit register follows the little-endian convention. IOTG[7:4] falls in REG0x0B[3:0], and IOTG[3:0] falls in REG0x0A[7:4]. POR: 1000mA (32h) Range: 100mA-2400mA (5h-78h) Clamped Low Clamped High Bit Step: 20mA
3:0	RESERVED	R	0h	Reserved

8.6.2.6 REG0x0C_VOTG_regulation Register (Address = Ch) [Reset = 0FC0h]

REG0x0C_VOTG_regulation is shown in Figure 8-22 and described in Table 8-14.

Return to the Summary Table.

VOTG regulation

Figure 8-22. REG0x0C_VOTG_regulation Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">VOTG</td></tr>
<tr><td colspan="3">R-0h</td><td colspan="5">R/W-3Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">VOTG</td><td colspan="6">RESERVED</td></tr>
<tr><td colspan="2">R/W-3Fh</td><td colspan="6">R-0h</td></tr>
</table>

Table 8-14. REG0x0C_VOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:6	VOTG	R/W	3Fh	OTG mode regulation voltage: This 16-bit register follows the little-endian convention. VOTG[6:2] falls in REG0x0D[4:0], and VOTG[1:0] falls in REG0x0C[7:6]. POR: 5040mV (3Fh) Range: 3840mV-9600mV (30h-78h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0h	Reserved

8.6.2.7 REG0x0E_Minimal_System_Voltage Register (Address = Eh) [Reset = 0B00h]

REG0x0E_Minimal_System_Voltage is shown in Figure 8-23 and described in Table 8-15.

Return to the Summary Table.

Minimal System Voltage

Figure 8-23. REG0x0E_Minimal_System_Voltage Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">VSYSMIN</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R/W-2Ch</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">VSYSMIN</td><td colspan="6">RESERVED</td></tr>
<tr><td colspan="2">R/W-2Ch</td><td colspan="6">R-0h</td></tr>
</table>

Table 8-15. REG0x0E_Minimal_System_Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:6	VSYSMIN	R/W	2Ch	Minimal System Voltage: This 16-bit register follows the little-endian convention. VSYSMIN[5:2] falls in REG0x0F[3:0], and VSYSMIN[1:0] falls in REG0x0E[7:6]. POR: 3520mV (2Ch) Range: 2560mV-3840mV (20h-30h) Clamped Low Clamped High Bit Step: 80mV
5:0	RESERVED	R	0h	Reserved

8.6.2.8 REG0x10_Pre-charge_Control Register (Address = 10h) [Reset = 0050h]

REG0x10_Pre-charge_Control is shown in Figure 8-24 and described in Table 8-16.

Return to the Summary Table.

Pre-charge Control

Figure 8-24. REG0x10_Pre-charge_Control Register

15	14	13	12	11	10	9	8
RESERVED							IPRECHG
R-0h							R/W-5h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPRECHG				RESERVED			
R/W-5h				R-0h			

Table 8-16. REG0x10_Pre-charge_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0h	Reserved
8:4	IPRECHG	R/W	5h	Pre-charge current regulation limit: This 16-bit register follows the little-endian convention. IPRECHG[4] falls in REG0x11[0], and IPRECHG[3:0] falls in REG0x10[7:4] POR: 100mA (5h) Range: 20mA-620mA (1h-1Fh) Clamped Low Bit Step: 20mA (1h) NOTE: When Q4_FULLON=1, this register has a minimum value of 80mA
3:0	RESERVED	R	0h	Reserved

8.6.2.9 REG0x12_Termination_Control Register (Address = 12h) [Reset = 0030h]

REG0x12_Termination_Control is shown in Figure 8-25 and described in Table 8-17.

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Termination Control

Figure 8-25. REG0x12_Termination_Control Register

15	14	13	12	11	10	9	8
RESERVED							ITERM
R-0h							R/W-6h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ITERM					RESERVED		
R/W-6h					R-0h		

Table 8-17. REG0x12_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0h	Reserved
8:3	ITERM	R/W	6h	Termination Current Threshold: This 16-bit register follows the little-endian convention. ITERM[5] falls in REG0x13[0], and ITERM[4:0] falls in REG0x12[7:3]. POR: 60mA (6h) Range: 10mA-620mA (1h-3Eh) Clamped Low Bit Step: 10mA (1h) NOTE: When Q4_FULLON=1, this register has a minimum value of 120mA, so Reset value becomes 120mA in this case

Table 8-17. REG0x12_Termination_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	RESERVED	R	0h	Reserved

8.6.2.10 REG0x14_Charge_Control_0 Register (Address = 14h) [Reset = 06h]

REG0x14_Charge_Control_0 is shown in Figure 8-26 and described in Table 8-18.

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Charge Control 0

Figure 8-26. REG0x14_Charge_Control_0 Register

7	6	5	4	3	2	1	0
Q1_FULLON	Q4_FULLON	ITRICKLE	TOPOFF_TMR		EN_TERM	VINDPM_BAT_TRACK	VRECHG
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-1h	R/W-1h	R/W-0h

Table 8-18. REG0x14_Charge_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Q1_FULLON	R/W	0h	Forces RBFET (Q1) into low resistance state (26 mΩ) , regardless of IINDPM setting. 0h = RBFET RDSON determined by IINDPM setting (default) 1h = RBFET RDSON is always 26 mΩ
6	Q4_FULLON	R/W	0h	Forces BATFET (Q4) into low resistance state (15 mΩ), regardless of ICHG setting. (Only applies when VBAT > VSYSMIN. Otherwise BATFET operates in linear mode.) 0h = BATFET RDSON determined by charge current (default) 1h = BATFET RDSON is always 15 mΩ
5	ITRICKLE	R/W	0h	Trickle charging current setting: 0b = 20mA (default) 1b = 80mA
4:3	TOPOFF_TMR	R/W	0h	Top-off timer control: 0h = Disabled (default) 1h = 17 mins 2h = 35 mins 3h = 52 mins
2	EN_TERM	R/W	1h	Enable termination 0h = Disable 1h = Enable (default)
1	VINDPM_BAT_TRACK	R/W	1h	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of the VINDPM register value and VBAT + VINDPM_BAT_TRACK. 0h = Disable function (VINDPM set by register) 1h = VBAT + 400 mV (default)
0	VRECHG	R/W	0h	Battery Recharge Threshold Offset (Below VREG) 0h = 100mV (default) 1h = 200mV

8.6.2.11 REG0x15_Charge_Timer_Control Register (Address = 15h) [Reset = 5Ch]

REG0x15_Charge_Timer_Control is shown in Figure 8-27 and described in Table 8-19.

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Charge Timer Control

Figure 8-27. REG0x15_Charge_Timer_Control Register

7	6	5	4	3	2	1	0
DIS_STAT	EN_AUTO_INDET	FORCE_INDET	EN_DCP_BIAS	TMR2X_EN	EN_SAFETY_TMRS	PRECHG_TMR	CHG_TMR
R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

Figure 8-27. REG0x15_Charge_Timer_Control Register (continued)

Table 8-19. REG0x15_Charge_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_STAT	R/W	0h	Disable the STAT pin output 0h = Enable (default) 1h = Disable
6	EN_AUTO_INDET	R/W	1h	Automatic D+/D- Detection Enable 0h = Disable DPDM detection when VBUS is plugged-in 1h = Enable DPDM detection when VBUS is plugged-in (default)
5	FORCE_INDET	R/W	0h	Force D+/D- detection 0h = Do not force DPDM detection (default) 1h = Force DPDM algorithm, when DPDM detection is done, this bit is reset to 0
4	EN_DCP_BIAS	R/W	1h	Enable 600 mV bias on D+ pin whenever DCP is detected by BC1.2 detection algorithm (VBUS_STAT = 011b.) 0h = Disable 600 mV bias on D+ pin 1h = Enable 600 mV bias on D+ pin if DCP detected
3	TMR2X_EN	R/W	1h	2X charging timer control 0h = Trickle charge, pre-charge and fast charge timer not slowed by 2X during input DPM or thermal regulation. 1h = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default)
2	EN_SAFETY_TMRS	R/W	1h	Enable fast charge, pre-charge and trickle charge timers 0h = Disable 1h = Enable (default)
1	PRECHG_TMR	R/W	0h	Pre-charge safety timer setting 0h = 2.5 hrs (default) 1h = 0.62 hrs
0	CHG_TMR	R/W	0h	Fast charge safety timer setting 0h = 14.5 hrs (default) 1h = 28 hrs

8.6.2.12 REG0x16_Charger_Control_1 Register (Address = 16h) [Reset = A1h]

REG0x16_Charger_Control_1 is shown in Figure 8-28 and described in Table 8-20.

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Charger Control 1

Figure 8-28. REG0x16_Charger_Control_1 Register

7	6	5	4	3	2	1	0
EN_AUTO_IBATDIS	FORCE_IBATDIS	EN_CHG	EN_HIZ	FORCE_PMID_DIS	WD_RST	WATCHDOG	
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	

Table 8-20. REG0x16_Charger_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_AUTO_IBATDIS	R/W	1h	Enable the auto battery discharging during the battery OVP fault 0h = The charger does NOT apply a discharging current on BAT during battery OVP triggered 1h = The charger does apply a discharging current on BAT during battery OVP triggered (default)
6	FORCE_IBATDIS	R/W	0h	Force a battery discharging current (~30mA) 0h = IDLE (default) 1h = Force the charger to apply a discharging current on BAT
5	EN_CHG	R/W	1h	Charger enable configuration 0h = Charge Disable 1h = Charge Enable (default)

Table 8-20. REG0x16_Charger_Control_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EN_HIZ	R/W	0h	Enable HIZ mode. 0h = Disable (default) 1h = Enable
3	FORCE_PMID_DIS	R/W	0h	Force a PMID discharge current (~30mA.) 0h = Disable (default) 1h = Enable
2	WD_RST	R/W	0h	I2C watch dog timer reset 0h = Normal (default) 1h = Reset (this bit goes back to 0 after timer reset)
1:0	WATCHDOG	R/W	1h	Watchdog timer setting 0h = Disable 1h = 50s (default) 2h = 100s 3h = 200s

8.6.2.13 REG0x17_Charger_Control_2 Register (Address = 17h) [Reset = 4Fh]

REG0x17_Charger_Control_2 is shown in Figure 8-29 and described in Table 8-21.

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Charger Control 2

Figure 8-29. REG0x17_Charger_Control_2 Register

7	6	5	4	3	2	1	0
REG_RST	TREG	SET_CONV_FREQ		SET_CONV_STRN		RESERVED	VBUS_OVP
R/W-0h	R/W-1h	R/W-0h		R/W-3h		R-0h	R/W-1h

Table 8-21. REG0x17_Charger_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REG_RST	R/W	0h	Reset registers to default values and reset timer Value resets to 0 after reset completes. 0h = Not reset (default) 1h = Reset
6	TREG	R/W	1h	Thermal regulation thresholds. 0h = 60C 1h = 120C (default)
5:4	SET_CONV_FREQ	R/W	0h	Adjust switching frequency of the converter 0h = Nominal, 1.5 MHz (default) 1h = -10%, 1.35 MHz 2h = +10%, 1.65 MHz 3h = RESERVED
3:2	SET_CONV_STRN	R/W	3h	Adjust the high side and low side drive strength of the converter to adjust efficiency versus EMI. 0h = weak 1h = normal 2h = RESERVED 3h = strong
1	RESERVED	R	0h	Reserved
0	VBUS_OVP	R/W	1h	Sets VBUS overvoltage protection threshold 0h = 6.3 V 1h = 18.5 V

8.6.2.14 REG0x18_Charger_Control_3 Register (Address = 18h) [Reset = 04h]

REG0x18_Charger_Control_3 is shown in Figure 8-30 and described in Table 8-22.

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Charger Control 3

Figure 8-30. REG0x18_Charger_Control_3 Register

7	6	5	4	3	2	1	0
RESERVED	EN_OTG	PFM_OTG_DIS	PFM_FWD_DIS	BATFET_CTRL_WVBUS	BATFET_DLY	BATFET_CTRL	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	

Table 8-22. REG0x18_Charger_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	EN_OTG	R/W	0h	OTG mode control 0b = OTG Disable (default) 1b = OTG Enable
5	PFM_OTG_DIS	R/W	0h	Disable PFM in OTG boost mode 0h = Enable (Default) 1h = Disable
4	PFM_FWD_DIS	R/W	0h	Disable PFM in forward buck mode 0h = Enable (Default) 1h = Disable
3	BATFET_CTRL_WVBUS	R/W	0h	Optionally allows BATFET off or system power reset with adapter present. 0h = 0x0 1h = 0x1
2	BATFET_DLY	R/W	1h	Delay time added to the taking action in bits [1:0] of the BATFET_CTRL 0h = Add 25 ms delay time 1h = Add 12.5s delay time (default)
1:0	BATFET_CTRL	R/W	0h	BATFET control The control logic of the BATFET to force the device enter different modes. 0h = Normal (default) 1h = Shutdown Mode 2h = Ship Mode 3h = System Power Reset

8.6.2.15 REG0x19_Charger_Control_4 Register (Address = 19h) [Reset = C0h]

REG0x19_Charger_Control_4 is shown in Figure 8-31 and described in Table 8-23.

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Charger Control 4

Figure 8-31. REG0x19_Charger_Control_4 Register

7	6	5	4	3	2	1	0
IBAT_PK		VBAT_UVLO	VBAT_OTG_MIN	EN_9V	EN_12V_or_EN_EXTILIM	CHG_RATE	
R/W-3h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 8-23. REG0x19_Charger_Control_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	IBAT_PK	R/W	3h	Battery discharging peak current protection threshold setting 0h = 1.5A 1h = 3A 2h = 6A 3h = 12A (default)

Table 8-23. REG0x19_Charger_Control_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	VBAT_UVLO	R/W	0h	Select the VBAT_UVLO falling threshold and VBAT_SHORT threshold 0h = VBAT_UVLO 2.2V, VBAT_SHORT 2.05V (default) 1h = VBAT_UVLO 1.8V, VBAT_SHORT 1.85V
4	VBAT_OTG_MIN	R/W	0h	Select the minimal battery voltage to start the OTG mode 0h = 3V rising / 2.8 falling (default) 1h = 2.6V rising / 2.4 falling
3	EN_9V	R/W	0h	**BQ25620: Enable 9V adapter detection** Host has to set EN_12V=EN_9V=0, followed by proper setting of EN_12V and EN_9V to start a detection. After successful 9V detection, if EN_9V is set to 0, charger starts a 12V detection (if EN_12V=1), or releases D+/D- bias and goes back to DCP (if EN_12V=0). 0b = Disabled (default) 1b = Enabled **BQ25622: RESERVED with default 0**
2	EN_12V_or_EN_EXTILIM	R/W	0h	**BQ25620: Enable 12V adapter detection** If EN_12V = EN_9V = 1, charger attempts 12V negotiation first. If 12V is detected, charger skips 9V negotiation. Host has to set EN_12V = EN_9V = 0, followed by proper setting of EN_12V and EN_9V to start a negotiation. After successful 12V negotiation, if EN_12V is set to 0 and EN_9V stays at 1, charger starts 9V negotiation. 0b = Disabled (default) 1b = Enabled **BQ25622:** Enable the external ILIM pin input current regulation 0b = Disabled 1b = Enabled (default)
1:0	CHG_RATE	R/W	0h	The charge rate definition for the fast charge stage. The charging current fold back value is equal to ICHG register setting times the fold back ratio, then divided by the charge rate. 0h = 1C (default) 1h = 2C 2h = 4C 3h = 6C

8.6.2.16 REG0x1A_NTC_Control_0 Register (Address = 1Ah) [Reset = 3Dh]

REG0x1A_NTC_Control_0 is shown in Figure 8-32 and described in Table 8-24.

Return to the Summary Table.

NTC Control 0

Figure 8-32. REG0x1A_NTC_Control_0 Register

7	6	5	4	3	2	1	0
TS_IGNORE	TS_TH_OTG_HOT		TS_TH_OTG_COLD	TS_ISET_WARM		TS_ISET_COOL	
R/W-0h	R/W-1h		R/W-1h	R/W-3h		R/W-1h	

Table 8-24. REG0x1A_NTC_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TS_IGNORE	R/W	0h	Ignore the TS feedback: the charger considers the TS is always good to allow charging and OTG modes, TS_STAT reports TS_NORMAL condition. 0h = Not ignore (Default) 1h = Ignore

Table 8-24. REG0x1A_NTC_Control_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	TS_TH_OTG_HOT	R/W	1h	OTG Mode TS_HOT rising temperature threshold to transition from normal operation into suspended OTG mode when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. 0h = 55°C 1h = 60°C (default) 2h = 65°C 3h = Disable
4	TS_TH_OTG_COLD	R/W	1h	OTG Mode TS_COLD falling temperature threshold to transition from normal operation into suspended OTG mode when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. 0h = -20°C 1h = -10°C (default)
3:2	TS_ISET_WARM	R/W	3h	TS_WARM Current Setting 0h = Charge Suspend 1h = Set ICHG to 20% 2h = Set ICHG to 40% 3h = ICHG unchanged (default)
1:0	TS_ISET_COOL	R/W	1h	TS_COOL Current Setting 0h = Charge Suspend 1h = Set ICHG to 20% (default) 2h = Set ICHG to 40% 3h = ICHG unchanged

8.6.2.17 REG0x1B_NTC_Control_1 Register (Address = 1Bh) [Reset = 25h]

REG0x1B_NTC_Control_1 is shown in Figure 8-33 and described in Table 8-25.

Return to the Summary Table.

NTC Control 1

Figure 8-33. REG0x1B_NTC_Control_1 Register

7	6	5	4	3	2	1	0
TS_TH1_TH2_TH3			TS_TH4_TH5_TH6			TS_VSET_WARM	
R/W-1h			R/W-1h			R/W-1h	

Table 8-25. REG0x1B_NTC_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	TS_TH1_TH2_TH3	R/W	1h	TH1, TH2 and TH3 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. 0h = TH1 is 0°C, TH2 is 5°C, TH3 is 15°C 1h = TH1 is 0°C, TH2 is 10°C, TH3 is 15°C (default) 2h = TH1 is 0°C, TH2 is 15°C, TH3 is 20°C 3h = TH1 is 0°C, TH2 is 20°C, TH3 20°C 4h = TH1 is -5°C, TH2 is 5°C, TH3 is 15°C 5h = TH1 is -5°C, TH2 is 10°C, TH3 is 15°C 6h = TH1 is -5°C, TH2 is 10°C, TH3 is 20°C 7h = TH1 is 0°C, TH2 is 10°C, TH3 is 20°C
4:2	TS_TH4_TH5_TH6	R/W	1h	TH4, TH5 and TH6 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. 0h = TH4 is 35°C, TH5 is 40°C, TH6 is 60°C 1h = TH4 is 35°C, TH5 is 45°C, TH6 is 60°C (default) 2h = TH4 is 35°C, TH5 is 50°C, TH6 is 60°C 3h = TH4 is 40°C, TH5 is 55°C, TH6 is 60°C 4h = TH4 is 35°C, TH5 is 40°C, TH6 is 50°C 5h = TH4 is 35°C, TH5 is 45°C, TH6 is 50°C 6h = TH4 is 40°C, TH5 is 45°C, TH6 is 60°C 7h = TH4 is 40°C, TH5 is 50°C, TH6 is 60°C

Table 8-25. REG0x1B_NTC_Control_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	TS_VSET_WARM	R/W	1h	TS_WARM Voltage Setting 0h = Set VREG to VREG-300mV 1h = Set VREG to VREG-200mV (default) 2h = Set VREG to VREG-100mV 3h = VREG unchanged

8.6.2.18 REG0x1C_NTC_Control_2 Register (Address = 1Ch) [Reset = 3Fh]

REG0x1C_NTC_Control_2 is shown in Figure 8-34 and described in Table 8-26.

Return to the Summary Table.

NTC Control 2

Figure 8-34. REG0x1C_NTC_Control_2 Register

7	6	5	4	3	2	1	0
RESERVED	TS_VSET_SYM	TS_VSET_PREWARM		TS_ISET_PREWARM		TS_ISET_PRECOOL	
R-0h	R/W-0h	R/W-3h		R/W-3h		R/W-3h	

Table 8-26. REG0x1C_NTC_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	TS_VSET_SYM	R/W	0h	When this bit is set to 0, the voltage regulation for TS_PRECOOL and TS_COOL is unchanged. When this bit is set to 1, TS_PRECOOL uses the TS_VSET_PREWARM setting of TS_PREWARM and TS_COOL uses the TS_VSET_WARM setting of TS_WARM . 0h = VREG unchanged (default) 1h = TS_COOLx matches TS_WARMx
5:4	TS_VSET_PREWARM	R/W	3h	Advanced temperature profile voltage setting for TS_PREWARM (TH4 - TH5) 0h = Set VREG to VREG-300mV 1h = Set VREG to VREG-200mV 2h = Set VREG to VREG-100mV 3h = VREG unchanged (default)
3:2	TS_ISET_PREWARM	R/W	3h	Advanced temperature profile current setting for TS_PREWARM zone(TH4 - TH5) 0h = Charge Suspend 1h = Set ICHG to 20% 2h = Set ICHG to 40% 3h = ICHG unchanged (default)
1:0	TS_ISET_PRECOOL	R/W	3h	Advanced temperature profile current setting for TS_PRECOOL zone (TH2 - TH3) 0h = Charge Suspend 1h = Set ICHG to 20% 2h = Set ICHG to 40% 3h = ICHG unchanged (default)

8.6.2.19 REG0x1D_Charger_Status_0 Register (Address = 1Dh) [Reset = 00h]

REG0x1D_Charger_Status_0 is shown in Figure 8-35 and described in Table 8-27.

Return to the Summary Table.

Charger Status 0

Figure 8-35. REG0x1D_Charger_Status_0 Register

7	6	5	4	3	2	1	0
RESERVED	ADC_DONE_STAT	TREG_STAT	VSYS_STAT	IINDPM_STAT	VINDPM_STAT	SAFETY_TMR_STAT	WD_STAT

Figure 8-35. REG0x1D_Charger_Status_0 Register (continued)

R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-27. REG0x1D_Charger_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	ADC_DONE_STAT	R	0h	ADC Conversion Status (in one-shot mode only) Note: Always reads 0 in continuous mode 0h = Conversion not complete 1h = Conversion complete
5	TREG_STAT	R	0h	IC Thermal regulation status 0h = Normal 1h = Device in thermal regulation
4	VSYS_STAT	R	0h	VSYS Regulation Status (forward mode) 0h = Not in VSYSMIN regulation (BAT>VSYSMIN) 1h = In VSYSMIN regulation (BAT<VSYSMIN)
3	IINDPM_STAT	R	0h	In forward mode, indicates that either IINDPM regulation is active or ILIM pin regulation is active In OTG mode, indicates that IOTG regulation is active 0h = Normal 1h = In IINDPM/ILIM regulation or IOTG regulation
2	VINDPM_STAT	R	0h	VINDPM status (forward mode) or VOTG status (OTG mode, backup mode) 0h = Normal 1h = In VINDPM regulation or VOTG regulation
1	SAFETY_TMR_STAT	R	0h	Fast charge, trickle charge and pre-charge timer status 0h = Normal 1h = Safety timer expired
0	WD_STAT	R	0h	I2C watch dog timer status 0h = Normal 1h = WD timer expired

8.6.2.20 REG0x1E_Charger_Status_1 Register (Address = 1Eh) [Reset = 00h]

REG0x1E_Charger_Status_1 is shown in Figure 8-36 and described in Table 8-28.

Return to the Summary Table.

Charger Status 1

Figure 8-36. REG0x1E_Charger_Status_1 Register

7	6	5	4	3	2	1	0
RESERVED			CHG_STAT		VBUS_STAT		
R-0h			R-0h		R-0h		

Table 8-28. REG0x1E_Charger_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4:3	CHG_STAT	R	0h	Charge Status bits 0h = Not Charging or Charge Terminated 1h = Trickle Charge, Pre-charge or Fast charge (CC mode) 2h = Taper Charge (CV mode) 3h = Top-off Timer Active Charging

Table 8-28. REG0x1E_Charger_Status_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	VBUS_STAT	R	0h	VBUS status bits BQ25620: 000b = No qualified adapter, or EN_AUTO_INDET = 0. 001b = USB SDP Adapter (500mA) 010b = USB CDP Adapter (1.5A) 011b = USB DCP Adapter (1.5A) 100b = Unknown Adapter (500mA) 101b = Non-Standard Adapter (1A/2.1A/2.4A) 110b = HVDCP adapter (1.5A) 111b = In boost OTG mode BQ25622: 100b = Unknown Adapter (default IINDPM setting)

8.6.2.21 REG0x1F_FAULT_Status_0 Register (Address = 1Fh) [Reset = 00h]

REG0x1F_FAULT_Status_0 is shown in Figure 8-37 and described in Table 8-29.

Return to the Summary Table.

FAULT Status 0

Figure 8-37. REG0x1F_FAULT_Status_0 Register

7	6	5	4	3	2	1	0
VBUS_FAULT_STAT	BAT_FAULT_STAT	SYS_FAULT_STAT	OTG_FAULT_STAT	TSHUT_STAT	TS_STAT		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		

Table 8-29. REG0x1F_FAULT_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_STAT	R	0h	VBUS fault status, VBUS OVP and sleep comparator 0h = Normal 1h = Device not switching due to over voltage protection or sleep comparator
6	BAT_FAULT_STAT	R	0h	BAT fault status, IBAT OCP and VBAT OVP 0h = Normal 1h = Device in battery over current protection or battery overvoltage protection
5	SYS_FAULT_STAT	R	0h	VSYS under voltage and over voltage status 0h = Normal 1h = SYS in SYS short circuit or over voltage
4	OTG_FAULT_STAT	R	0h	Reverse-current or undervoltage or overvoltage fault detected at PMID or VBUS during boost OTG 0h = Normal 1h = Reverse-current fault or PMID or VBUS in over voltage or under voltage during OTG
3	TSHUT_STAT	R	0h	IC temperature shutdown status 0h = Normal 1h = Device in thermal shutdown protection
2:0	TS_STAT	R	0h	The TS temperature zone. 0h = TS_NORMAL 1h = TS_COLD or TS_OTG_COLD or TS resistor string power rail is not available. 2h = TS_HOT or TS_OTG_HOT 3h = TS_COOL 4h = TS_WARM 5h = TS_PRECOOL 6h = TS_PREWARM 7h = TS pin bias reference fault

8.6.2.22 REG0x20_Charger_Flag_0 Register (Address = 20h) [Reset = 00h]

REG0x20_Charger_Flag_0 is shown in Figure 8-38 and described in Table 8-30.

Return to the Summary Table.

Charger Flag 0

Figure 8-38. REG0x20_Charger_Flag_0 Register

7	6	5	4	3	2	1	0
RESERVED	ADC_DONE_FLAG	TREG_FLAG	VSYS_FLAG	IINDPM_FLAG	VINDPM_FLAG	SAFETY_TMR_FLAG	WD_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-30. REG0x20_Charger_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	ADC_DONE_FLAG	R	0h	ADC conversion flag (only in one-shot mode) 0h = Conversion not completed 1h = Conversion completed
5	TREG_FLAG	R	0h	IC Thermal regulation flag 0h = Normal 1h = TREG signal rising threshold detected
4	VSYS_FLAG	R	0h	VSYS min regulation flag 0h = Normal 1h = Entered or existed VSYS min regulation
3	IINDPM_FLAG	R	0h	Indicates that either the IINDPM regulation loop, ILIM pin regulation or IOTG regulation loop has been entered. 0h = Normal 1h = IINDPM, ILIM or IOTG regulation signal rising edge detected
2	VINDPM_FLAG	R	0h	VINDPM or VOTG flag 0h = Normal 1h = VINDPM or VOTG regulation signal rising edge detected
1	SAFETY_TMR_FLAG	R	0h	Fast charge, trickle charge and pre-charge timer flag 0h = Normal 1h = Fast charge timer expired rising edge detected
0	WD_FLAG	R	0h	I2C watchdog timer flag 0h = Normal 1h = WD timer signal rising edge detected

8.6.2.23 REG0x21_Charger_Flag_1 Register (Address = 21h) [Reset = 00h]

REG0x21_Charger_Flag_1 is shown in Figure 8-39 and described in Table 8-31.

Return to the Summary Table.

Charger Flag 1

Figure 8-39. REG0x21_Charger_Flag_1 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>CHG_FLAG</td><td colspan="2">RESERVED</td><td>VBUS_FLAG</td></tr>
<tr><td colspan="4">R-0h</td><td>R-0h</td><td colspan="2">R-0h</td><td>R-0h</td></tr>
</table>

Table 8-31. REG0x21_Charger_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	CHG_FLAG	R	0h	Charge status flag 0h = Normal 1h = Charge status changed

Table 8-31. REG0x21_Charger_Flag_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:1	RESERVED	R	0h	Reserved
0	VBUS_FLAG	R	0h	VBUS status flag 0h = Normal 1h = VBUS status changed

8.6.2.24 REG0x22_FAULT_Flag_0 Register (Address = 22h) [Reset = 00h]

REG0x22_FAULT_Flag_0 is shown in Figure 8-40 and described in Table 8-32.

Return to the Summary Table.

FAULT Flag 0

Figure 8-40. REG0x22_FAULT_Flag_0 Register

7	6	5	4	3	2	1	0
VBUS_FAULT_FLAG	BAT_FAULT_FLAG	SYS_FAULT_FLAG	OTG_FAULT_FLAG	TSHUT_FLAG	RESERVED		TS_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		R-0h

Table 8-32. REG0x22_FAULT_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_FLAG	R	0h	VBUS over-voltage or sleep flag 0h = Normal 1h = Entered VBUS OVP or sleep
6	BAT_FAULT_FLAG	R	0h	IBAT over-current and VBAT over-voltage flag 0h = Normal 1h = Entered battery discharged OCP or VBAT OVP
5	SYS_FAULT_FLAG	R	0h	VSYS over voltage and SYS short flag 0h = Normal 1h = Stopped switching due to system over-voltage or SYS short fault
4	OTG_FAULT_FLAG	R	0h	OTG PMID and VBUS reverse-current, under voltage and over voltage flag 0h = Normal 1h = Stopped OTG due to reverse-current fault, PMID under voltage or over voltage fault
3	TSHUT_FLAG	R	0h	IC thermal shutdown flag 0h = Normal 1h = TS shutdown signal rising threshold detected
2:1	RESERVED	R	0h	Reserved
0	TS_FLAG	R	0h	TS status flag 0h = Normal 1h = A change to TS status was detected

8.6.2.25 REG0x23_Charger_Mask_0 Register (Address = 23h) [Reset = 00h]

REG0x23_Charger_Mask_0 is shown in Figure 8-41 and described in Table 8-33.

Return to the Summary Table.

Charger Mask 0

Figure 8-41. REG0x23_Charger_Mask_0 Register

7	6	5	4	3	2	1	0
RESERVED	ADC_DONE_MASK	TREG_MASK	VSYS_MASK	IINDPM_MASK	VINDPM_MASK	SAFETY_TMR_MASK	WD_MASK
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-33. REG0x23_Charger_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	ADC_DONE_MASK	R/W	0h	ADC conversion mask flag (only in one-shot mode) 0h = ADC conversion done does produce $\overline{\text{INT}}$ pulse 1h = ADC conversion done does not produce $\overline{\text{INT}}$ pulse
5	TREG_MASK	R/W	0h	IC thermal regulation mask flag 0h = Entering TREG does produce $\overline{\text{INT}}$ 1h = Entering TREG does not produce $\overline{\text{INT}}$
4	VSYS_MASK	R/W	0h	VSYS min regulation mask flag 0h = Enter or exit VSYSMIN regulation does produce $\overline{\text{INT}}$ pulse 1h = Enter or exit VSYSMIN regulation does not produce $\overline{\text{INT}}$ pulse
3	IINDPM_MASK	R/W	0h	IINDPM, ILIM or IOTG mask 0h = Enter IINDPM, ILIM or IOTG does produce $\overline{\text{INT}}$ pulse 1h = Enter IINDPM, ILIM or IOTG does not produce $\overline{\text{INT}}$ pulse
2	VINDPM_MASK	R/W	0h	VINDPM or VOTG mask 0h = Enter VINDPM or VOTG does produce $\overline{\text{INT}}$ pulse 1h = Enter VINDPM or VOTG does not produce $\overline{\text{INT}}$ pulse
1	SAFETY_TMR_MASK	R/W	0h	Fast charge, trickle charge and pre-charge timer mask flag 0h = Fast charge, trickle charge or pre-charge timer expiration does produce $\overline{\text{INT}}$ 1h = Fast charge, trickle charge or pre-charge timer expiration does not produce $\overline{\text{INT}}$
0	WD_MASK	R/W	0h	I2C watch dog timer mask 0h = I2C watch dog timer expired does produce $\overline{\text{INT}}$ pulse 1h = I2C watch dog timer expired does not produce $\overline{\text{INT}}$ pulse

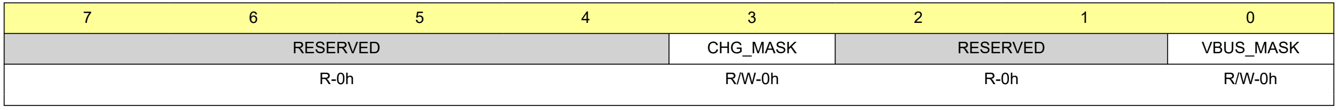
8.6.2.26 REG0x24_Charger_Mask_1 Register (Address = 24h) [Reset = 00h]

REG0x24_Charger_Mask_1 is shown in Figure 8-42 and described in Table 8-34.

Return to the Summary Table.

Charger Mask 1

Figure 8-42. REG0x24_Charger_Mask_1 Register



7	6	5	4	3	2	1	0
RESERVED				CHG_MASK	RESERVED		VBUS_MASK
R-0h				R/W-0h	R-0h		R/W-0h

Table 8-34. REG0x24_Charger_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	CHG_MASK	R/W	0h	Charge status mask flag 0h = Charging status change does produce $\overline{\text{INT}}$ 1h = Charging status change does not produce $\overline{\text{INT}}$
2:1	RESERVED	R	0h	Reserved
0	VBUS_MASK	R/W	0h	VBUS status mask flag 0h = VBUS status change does produce $\overline{\text{INT}}$ 1h = VBUS status change does not produce $\overline{\text{INT}}$

8.6.2.27 REG0x25_FAULT_Mask_0 Register (Address = 25h) [Reset = 00h]

REG0x25_FAULT_Mask_0 is shown in Figure 8-43 and described in Table 8-35.

Return to the Summary Table.

FAULT Mask 0

Figure 8-43. REG0x25_FAULT_Mask_0 Register

7	6	5	4	3	2	1	0
VBUS_FAULT_MASK	BAT_FAULT_MASK	SYS_FAULT_MASK	OTG_FAULT_MASK	TSHUT_MASK	RESERVED		TS_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h

Table 8-35. REG0x25_FAULT_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS_FAULT_MASK	R/W	0h	VBUS over-voltage and sleep comparator mask flag 0h = Entering VBUS OVP or sleep does produce $\overline{\text{INT}}$ 1h = Entering VBUS OVP or sleep does not produce $\overline{\text{INT}}$
6	BAT_FAULT_MASK	R/W	0h	IBAT over current and VBAT overvoltage mask flag 0h = IBAT OCP fault or VBAT OVP fault does produce $\overline{\text{INT}}$ 1h = Neither IBAT OCP fault nor VBAT OVP fault produces $\overline{\text{INT}}$
5	SYS_FAULT_MASK	R/W	0h	SYS over voltage and SYS short mask 0h = System over-voltage or SYS short fault does produce $\overline{\text{INT}}$ 1h = Neither system over voltage nor SYS short fault produces $\overline{\text{INT}}$
4	OTG_FAULT_MASK	R/W	0h	OTG VBUS and PMID reverse-current, under voltage and over voltage mask 0h = OTG VBUS or PMID reverse-current, under voltage fault or over voltage fault does produce $\overline{\text{INT}}$ 1h = Neither reverse-current fault, OTG PMID or VBUS under voltage nor over voltage fault produces $\overline{\text{INT}}$
3	TSHUT_MASK	R/W	0h	IC thermal shutdown mask flag 0h = TSHUT does produce $\overline{\text{INT}}$ 1h = TSHUT does not produce $\overline{\text{INT}}$
2:1	RESERVED	R	0h	
0	TS_MASK	R/W	0h	Temperature charging profile interrupt mask 0h = A change to TS temperature zone does produce $\overline{\text{INT}}$ 1h = A change to the TS temperature zone does not produce $\overline{\text{INT}}$

8.6.2.28 REG0x26_ADC_Control Register (Address = 26h) [Reset = 30h]

REG0x26_ADC_Control is shown in Figure 8-44 and described in Table 8-36.

Return to the Summary Table.

ADC Control

Figure 8-44. REG0x26_ADC_Control Register

7	6	5	4	3	2	1	0
ADC_EN	ADC_RATE	ADC_SAMPLE		ADC_AVG	ADC_AVG_INIT	RESERVED	
R/W-0h	R/W-0h	R/W-3h		R/W-0h	R/W-0h	R-0h	

Table 8-36. REG0x26_ADC_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_EN	R/W	0h	ADC Control The registers POR to all 0 's, then after that always retain the last measurement, and never clear. 0h = Disable (default) 1h = Enable
6	ADC_RATE	R/W	0h	ADC conversion rate control 0h = Continuous conversion (default) 1h = One shot conversion

Table 8-36. REG0x26_ADC_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	ADC_SAMPLE	R/W	3h	ADC sample speed 0h = 12 bit effective resolution 1h = 11 bit effective resolution 2h = 10 bit effective resolution 3h = 9 bit effective resolution (default)
3	ADC_AVG	R/W	0h	ADC average control 0h = Single value (default) 1h = Running average
2	ADC_AVG_INIT	R/W	0h	ADC average initial value control 0h = Start average using the existing register value (default) 1h = Start average using a new ADC conversion
1:0	RESERVED	R	0h	Reserved

8.6.2.29 REG0x27_ADC_Function_Disable_0 Register (Address = 27h) [Reset = 00h]

REG0x27_ADC_Function_Disable_0 is shown in Figure 8-45 and described in Table 8-37.

Return to the Summary Table.

ADC Function Disable 0

Figure 8-45. REG0x27_ADC_Function_Disable_0 Register

7	6	5	4	3	2	1	0
IBUS_ADC_DIS	IBAT_ADC_DIS	VBUS_ADC_DIS	VBAT_ADC_DIS	VSYS_ADC_DIS	TS_ADC_DIS	TDIE_ADC_DIS	VPMID_ADC_DIS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-37. REG0x27_ADC_Function_Disable_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IBUS_ADC_DIS	R/W	0h	IBUS ADC control 0h = Enable (Default) 1h = Disable
6	IBAT_ADC_DIS	R/W	0h	IBAT ADC control 0h = Enable (Default) 1h = Disable
5	VBUS_ADC_DIS	R/W	0h	VBUS ADC control 0h = Enable (Default) 1h = Disable
4	VBAT_ADC_DIS	R/W	0h	VBAT ADC control 0h = Enable (Default) 1h = Disable
3	VSYS_ADC_DIS	R/W	0h	VSYS ADC control 0h = Enable (Default) 1h = Disable
2	TS_ADC_DIS	R/W	0h	TS ADC control 0h = Enable (Default) 1h = Disable
1	TDIE_ADC_DIS	R/W	0h	TDIE ADC control 0h = Enable (Default) 1h = Disable
0	VPMID_ADC_DIS	R/W	0h	VPMID ADC control 0h = Enable (Default) 1h = Disable

8.6.2.30 REG0x28_IBUS_ADC Register (Address = 28h) [Reset = 0000h]

REG0x28_IBUS_ADC is shown in Figure 8-46 and described in Table 8-38.

Return to the Summary Table.

IBUS ADC

Figure 8-46. REG0x28_IBUS_ADC Register

15	14	13	12	11	10	9	8
IBUS_ADC							
R-0h							
7	6	5	4	3	2	1	0
IBUS_ADC							RESERVED
R-0h							R-0h

Table 8-38. REG0x28_IBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	IBUS_ADC	R	0h	IBUS ADC reading Reported in 2 's Complement. When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value. POR: 0mA (0h) Format: 2s Complement Range: -4000mA-4000mA (7830h-7FFFh), (0h-7D0h) Clamped Low Clamped High Bit Step: 2mA
0	RESERVED	R	0h	Reserved

8.6.2.31 REG0x2A_IBAT_ADC Register (Address = 2Ah) [Reset = 0000h]

REG0x2A_IBAT_ADC is shown in Figure 8-47 and described in Table 8-39.

Return to the Summary Table.

IBAT ADC

Figure 8-47. REG0x2A_IBAT_ADC Register

15	14	13	12	11	10	9	8
IBAT_ADC							
R-0h							
7	6	5	4	3	2	1	0
IBAT_ADC						RESERVED	
R-0h						R-0h	

Table 8-39. REG0x2A_IBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	IBAT_ADC	R	0h	IBAT ADC reading Reported in 2 's Complement. The IBAT ADC reports positive value for the battery charging current, and negative value for the battery discharging current. The IBAT ADC resets to zero when EN_CHG=0. POR: 0mA (0h) Format: 2s Complement Range: -7500mA-4000mA (38ADh-3FFFh), (0h-3E8h) Clamped Low Clamped High Bit Step: 4mA The IBAT ADC current can only be positive or zero in forward mode, and negative or zero in battery-only mode. If polarity of battery current changes from charging to discharging or vice-versa during the ADC measurement, the conversion is aborted and the register reports code 0x8000 (which is code 0x2000 for IBAT_ADC field)
1:0	RESERVED	R	0h	Reserved

8.6.2.32 REG0x2C_VBUS_ADC Register (Address = 2Ch) [Reset = 0000h]

REG0x2C_VBUS_ADC is shown in Figure 8-48 and described in Table 8-40.

Return to the Summary Table.

VBUS ADC

Figure 8-48. REG0x2C_VBUS_ADC Register

15	14	13	12	11	10	9	8
RESERVED	VBUS_ADC						
R-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBUS_ADC						RESERVED	
R-0h						R-0h	

Table 8-40. REG0x2C_VBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14:2	VBUS_ADC	R	0h	VBUS ADC reading POR: 0mV (0h) Range: 0mV-18000mV (0h-11B6h) Clamped High Bit Step: 3.97mV
1:0	RESERVED	R	0h	Reserved

8.6.2.33 REG0x2E_VPMID_ADC Register (Address = 2Eh) [Reset = 0000h]

REG0x2E_VPMID_ADC is shown in Figure 8-49 and described in Table 8-41.

Return to the Summary Table.

VPMID ADC

Figure 8-49. REG0x2E_VPMID_ADC Register

15	14	13	12	11	10	9	8
RESERVED	VPMID_ADC						
R-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Figure 8-49. REG0x2E_VPMID_ADC Register (continued)

VPMID_ADC	RESERVED
R-0h	R-0h

Table 8-41. REG0x2E_VPMID_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14:2	VPMID_ADC	R	0h	VPMID ADC reading POR: 0mV (0h) Range: 0mV-18000mV (0h-11B6h) Clamped High Bit Step: 3.97mV
1:0	RESERVED	R	0h	Reserved

8.6.2.34 REG0x30_VBAT_ADC Register (Address = 30h) [Reset = 0000h]

REG0x30_VBAT_ADC is shown in Figure 8-50 and described in Table 8-42.

Return to the Summary Table.

VBAT ADC

Figure 8-50. REG0x30_VBAT_ADC Register

15	14	13	12	11	10	9	8
RESERVED			VBAT_ADC				
R-0h			R-0h				
7	6	5	4	3	2	1	0
VBAT_ADC							RESERVED
R-0h							R-0h

Table 8-42. REG0x30_VBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:1	VBAT_ADC	R	0h	VBAT ADC reading POR: 0mV (0h) Range: 0mV-5572mV (0h-AF0h) Clamped High Bit Step: 1.99mV
0	RESERVED	R	0h	Reserved

8.6.2.35 REG0x32_VSYS_ADC Register (Address = 32h) [Reset = 0000h]

REG0x32_VSYS_ADC is shown in Figure 8-51 and described in Table 8-43.

Return to the Summary Table.

VSYS ADC

Figure 8-51. REG0x32_VSYS_ADC Register

15	14	13	12	11	10	9	8
RESERVED			VSYS_ADC				
R-0h			R-0h				
7	6	5	4	3	2	1	0
VSYS_ADC							RESERVED
R-0h							R-0h

Table 8-43. REG0x32_VSYS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:1	VSYS_ADC	R	0h	VSYS ADC reading POR: 0mV (0h) Range: 0mV-5572mV (0h-AF0h) Clamped High Bit Step: 1.99mV
0	RESERVED	R	0h	Reserved

8.6.2.36 REG0x34_TS_ADC Register (Address = 34h) [Reset = 0000h]

REG0x34_TS_ADC is shown in Figure 8-52 and described in Table 8-44.

Return to the Summary Table.

TS ADC

Figure 8-52. REG0x34_TS_ADC Register

15	14	13	12	11	10	9	8
RESERVED				TS_ADC			
R-0h				R-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_ADC							
R-0h							

Table 8-44. REG0x34_TS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved
11:0	TS_ADC	R	0h	TS ADC reading as TS pin voltage in percentage of bias reference. Valid with TS pin bias reference active. POR: 0%(0h) Range: 0% - 98.3103% (0h-3FFh) Clamped High Bit Step: 0.0961%

8.6.2.37 REG0x36_TDIE_ADC Register (Address = 36h) [Reset = 0000h]

REG0x36_TDIE_ADC is shown in Figure 8-53 and described in Table 8-45.

Return to the Summary Table.

TDIE ADC

Figure 8-53. REG0x36_TDIE_ADC Register

15	14	13	12	11	10	9	8
RESERVED				TDIE_ADC			
R-0h				R-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDIE_ADC							
R-0h							

Table 8-45. REG0x36_TDIE_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0h	Reserved

Table 8-45. REG0x36_TDIE_ADC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	TDIE_ADC	R	0h	TDIE ADC reading Reported in 2 's Complement. POR: 0°C(0h) Format: 2s Complement Range: -40°C - 140°C (FB0h-118h) Clamped Low Clamped High Bit Step: 0.5°C

8.6.2.38 REG0x38_Part_Information Register (Address = 38h) [Reset = 02h]

REG0x38_Part_Information is shown in Figure 8-54 and described in Table 8-46.

Return to the Summary Table.

Part Information

Figure 8-54. REG0x38_Part_Information Register

7	6	5	4	3	2	1	0
RESERVED		PN			DEV_REV		
R-0h		R-0h			R-2h		

Table 8-46. REG0x38_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:3	PN	R	0h	Device Part number All the other options are reserved 0h = BQ25620 1h = BQ25622
2:0	DEV_REV	R	2h	Device Revision

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the device configured as an I^2C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphone and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application

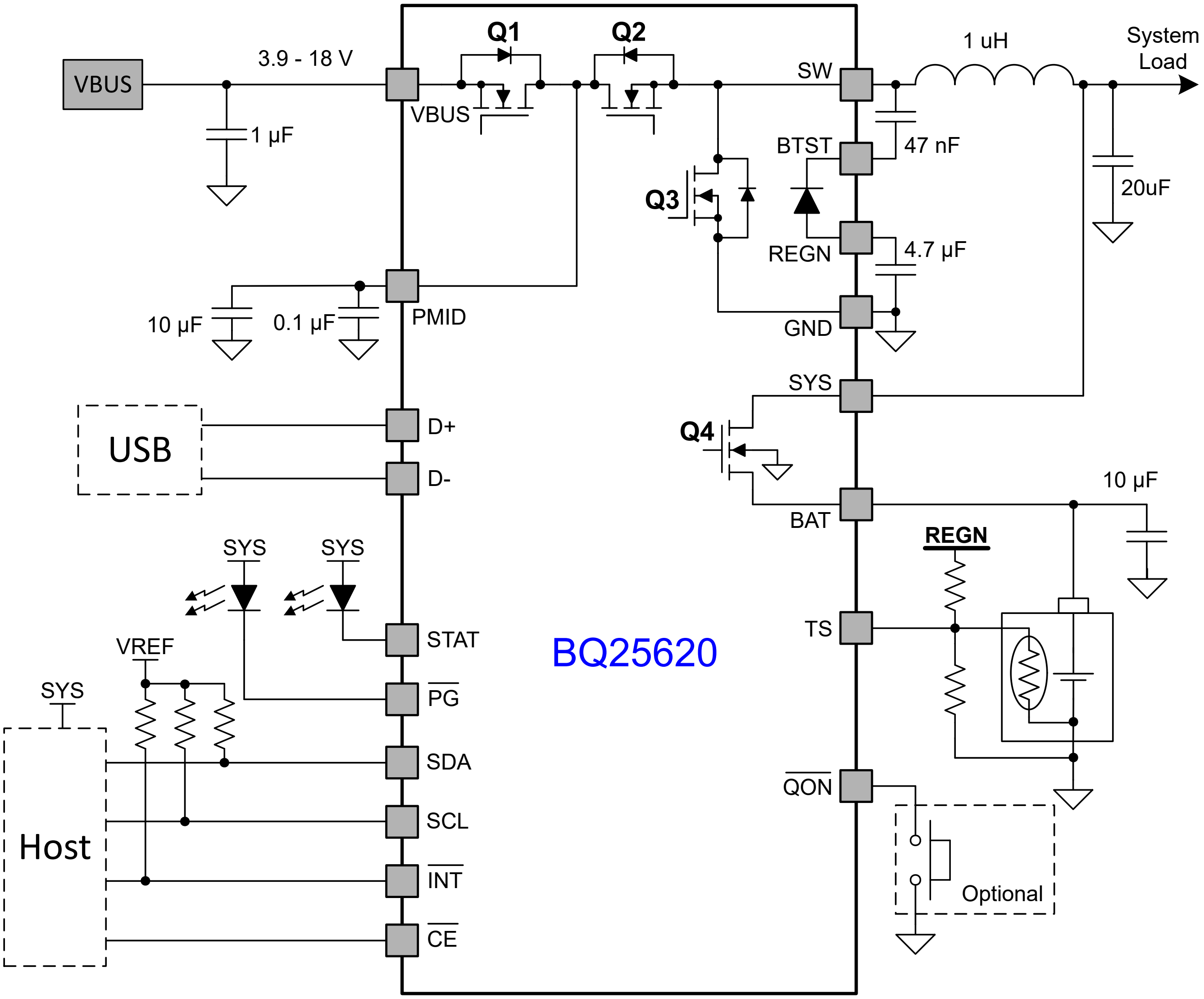


Figure 9-1. BQ25620 Application Diagram

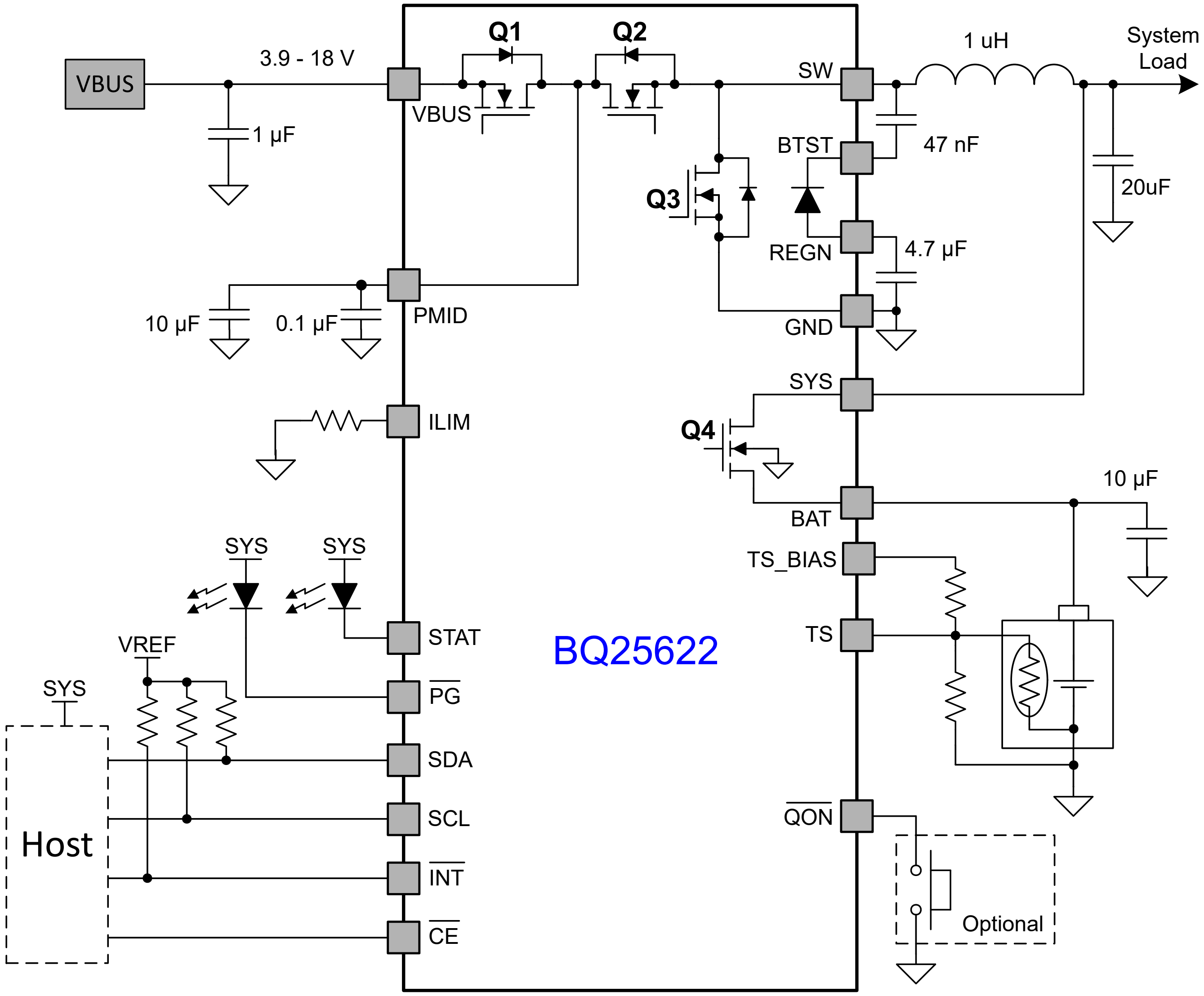


Figure 9-2. BQ25622 Application Diagram

9.2.1 Design Requirements

Table 9-1. Design Requirements

PARAMETER	VALUE
VBUS range	3.9 -18.0 V
Input current limit (REG0x06-0x07)	3200 mA
Fast charge current (REG0x02-0x03)	3040 mA
Minimum system voltage (REG0x0E-0x0F)	3520 mV
Battery regulation voltage (REG0x04-0x05)	4200 mV

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (3)$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \tag{4}$$

The maximum inductor ripple current occurs when the duty cycle (D) is approximately 0.5. Usually inductor ripple is designed between 20% and 40% of the maximum charging current as a trade-off between inductor size and efficiency.

9.2.2.2 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{Cin} occurs where the duty cycle is closest to 50% and can be estimated using Equation 5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{5}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET (PMID) and source of the low-side MOSFET (GND). Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15 V input voltage. 10-μF ceramic capacitor is suggested for typical of 3.5A charging current.

9.2.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. Equation 6 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{6}$$

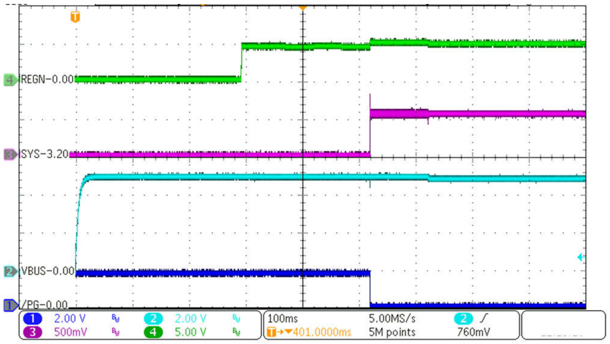
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_{SYS} = \frac{V_{SYS}}{8 \times L \times C_{SYS} \times f_{SW}^2}\left(1 - \frac{V_{SYS}}{V_{VBUS}}\right) \tag{7}$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

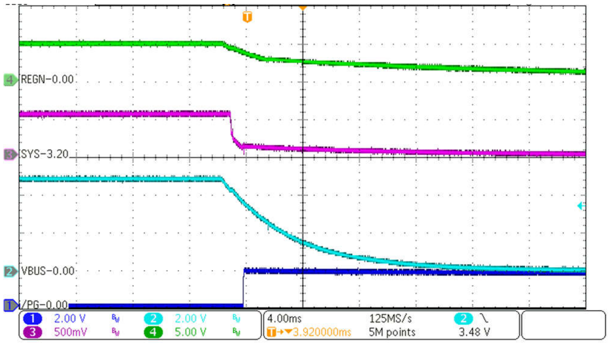
The charger device has internal loop compensation optimized for ≥ 10-μF ceramic output capacitor. The preferred ceramic capacitor is 10-V rating, X7R or X5R.

9.2.3 Application Curves



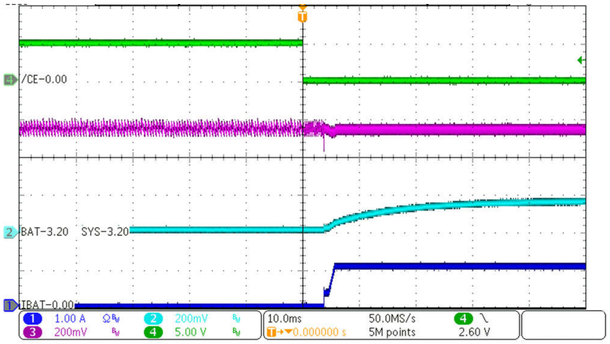
V_{VBUS} = 5 V V_{BAT} = 3.2 V
I_{CHG} = 1 A

Figure 9-3. Power-Up with Charge Enabled



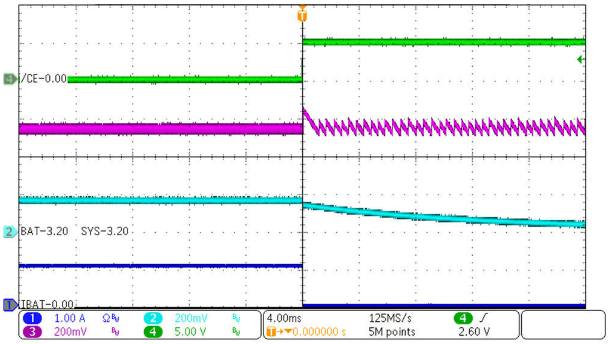
V_{VBUS} = 5 V V_{BAT} = 3.2 V
I_{CHG} = 1 A

Figure 9-4. Power-Down



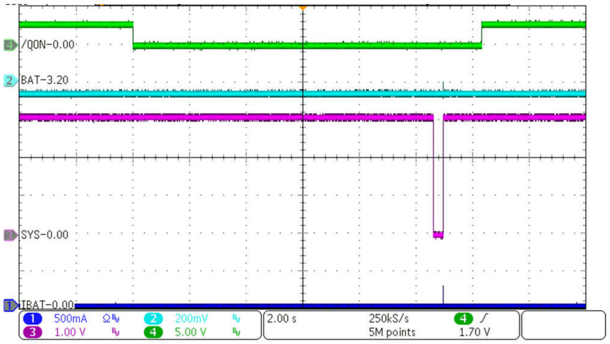
V_{VBUS} = 5 V V_{BAT} = 3.2 V
I_{CHG} = 1 A

Figure 9-5. Charge Enable



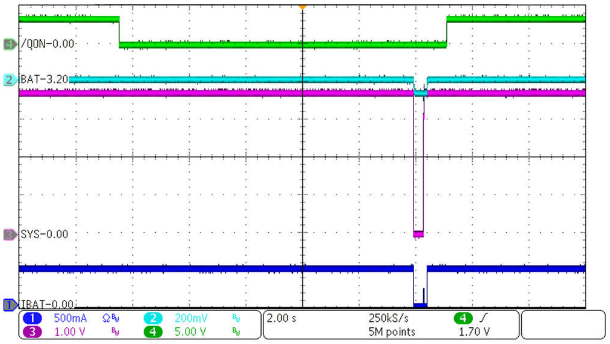
V_{VBUS} = 5 V V_{BAT} = 3.2 V
I_{CHG} = 1 A

Figure 9-6. Charge Disable



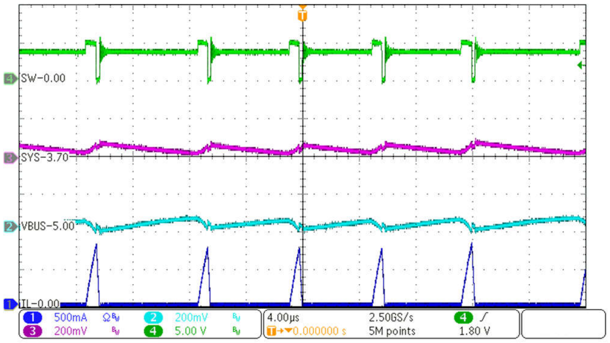
V_{BAT} = 3.2 V

Figure 9-7. System Reset by QON without VBUS Present



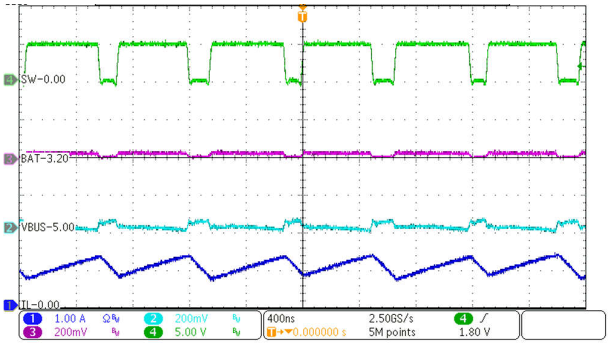
V_{VBUS} = 5 V V_{BAT} = 3.2 V
I_{CHG} = 480mA

Figure 9-8. System Reset by QON with VBUS Present



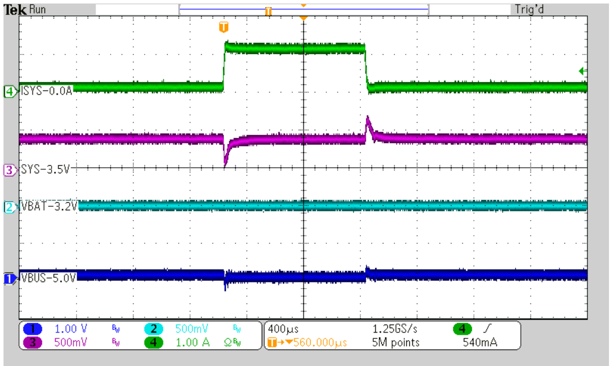
V_{VBUS} = 5 V
V_{BAT} = 3.2 V
I_{SYS} = 50 mA
Charge Disabled

Figure 9-9. PFM Switching in Buck Mode



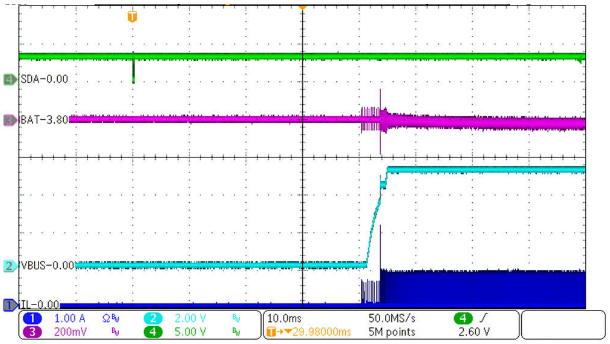
V_{VBUS} = 5 V
V_{VBAT} = 3.2 V
I_{CHG} = 1 A

Figure 9-10. PWM Switching in Buck Mode



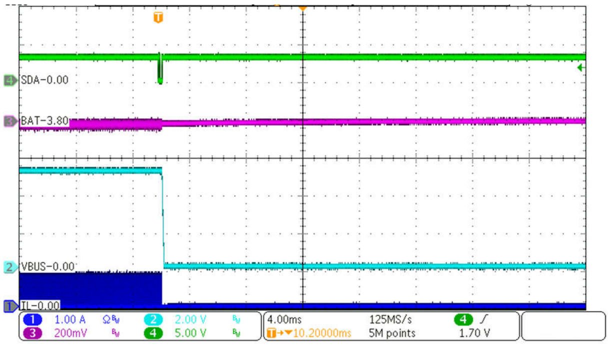
V_{VBUS} = 5 V
V_{BAT} = 3.2 V
I_{SYS} from 0 A to 1 A
Charge Disabled

Figure 9-11. System Load Transient



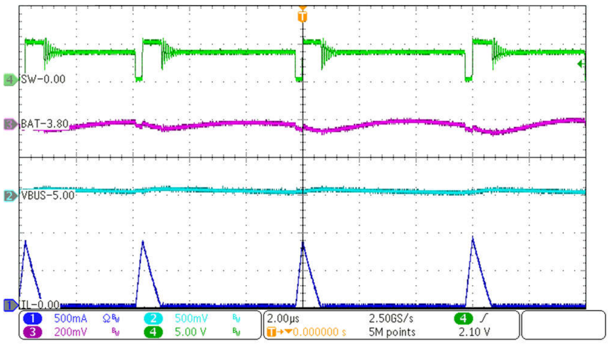
V_{BAT} = 3.8 V
V_{BOOST} = 5.04 V
I_{BOOST} = 100 mA

Figure 9-12. Boost Mode Power Up



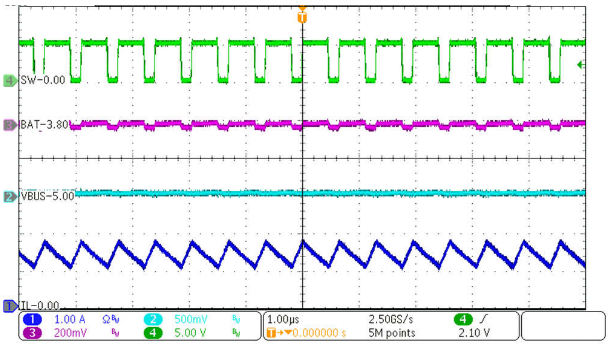
V_{BAT} = 3.8 V
V_{BOOST} = 5.04V
I_{BOOST} = 100 mA

Figure 9-13. Boost Mode Power Down



V_{BAT} = 3.8 V
V_{BOOST} = 5.04V
I_{BOOST}= 50 mA

Figure 9-14. PFM Switching in Boost Mode

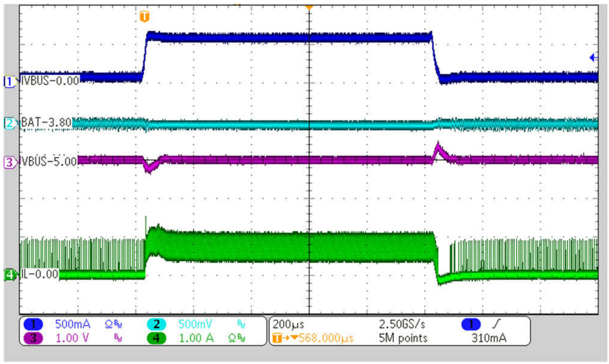


V_{BAT} = 3.8 V

V_{BOOST} = 5.04V

I_{BOOST}= 1 A

Figure 9-15. PWM Switching in Boost Mode



V_{BAT} = 3.8 V

V_{BOOST} = 5.04 V

I_{BOOST} from 0 A to 0.5 A

Figure 9-16. Boost Mode Load Transient

10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 18.0 V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for lowest switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 11-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. For lowest switching noise during forward/charge mode, place the decoupling capacitor CPMID1 and then bulk capacitor CPMID2 positive terminals as close as possible to PMID pin. Place the capacitor ground terminal close to the GND pin using the shortest copper trace connection or GND plane on the same layer as the IC. See Figure 11-2.
2. For lowest switching noise during reverse/OTG mode, place the CSYS1 and CSYS2 output capacitors' positive terminals near the SYS pin. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC. See Figure 11-2.
3. Since REGN powers the internal gate drivers, place the CREGN capacitor positive terminal close to REGN pin to minimize switching noise. The capacitor's ground terminal must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC. See Figure 11-2.
4. Place the CVBUS and CBAT capacitors positive terminals as close to the VBUS and BAT pins as possible. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC. See Figure 11-2.
5. Place the inductor input pin near the positive terminal of the SYS pin capacitors. Due to the PMID capacitor placement requirements, the inductor's switching node terminal must be via'd down with multiple via's to a second internal layer with a wide trace that returns to the SW pin with multiple vias. See Figure 11-3. Using multiple vias ensures that the via's additional resistance is negligible compared to the inductor's dc resistance and therefore does not impact efficiency. The vias additional series inductance is negligible compared to the inductor's inductance.
6. Place the BTST capacitor on the opposite side from the IC using vias to connect to the BTST pin and SW node. See Figure 11-4.
7. A separate analog GND plane for non-power related resistors and capacitors is not required if those components are placed away from the power components traces and planes.
8. Ensure that the I2C SDA and SCL lines are routed away from the SW node.

Additionally, it is important that the PCB footprint and solder mask for the BQ25620 cover the entire length of each of the pins. GND, SW, PMID, SYS and BAT pins extend further into the package than the other pins. Using the entire length of these pins reduces parasitic resistance and increases thermal conductivity from the package into the board.

11.2 Layout Example

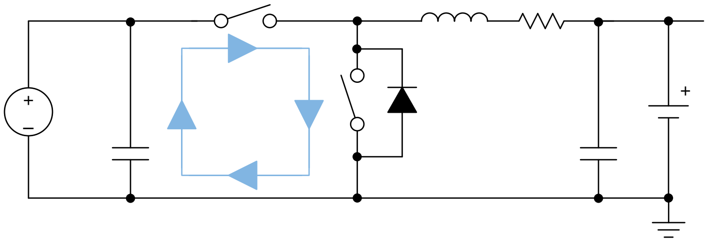


Figure 11-1. High Frequency Current Path

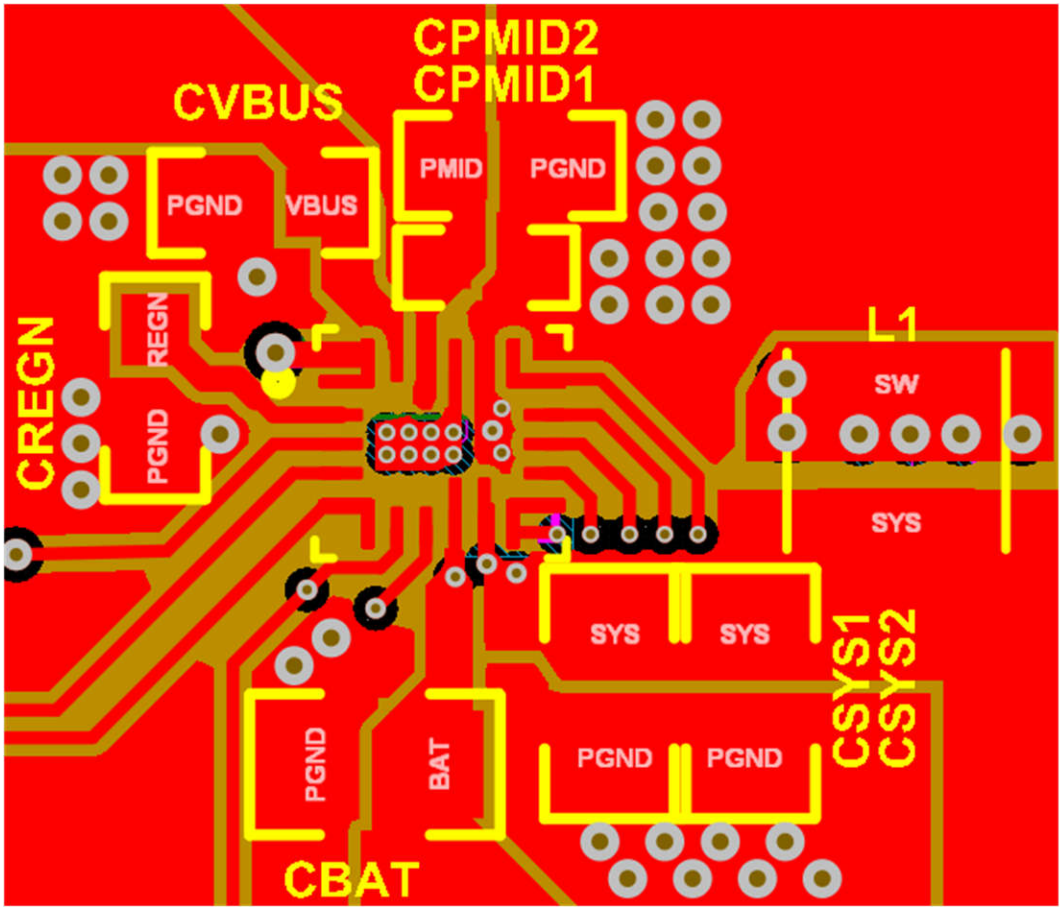


Figure 11-2. Layout Example: Top Layer (red) and All PGND Internal Layer 2 (brown)

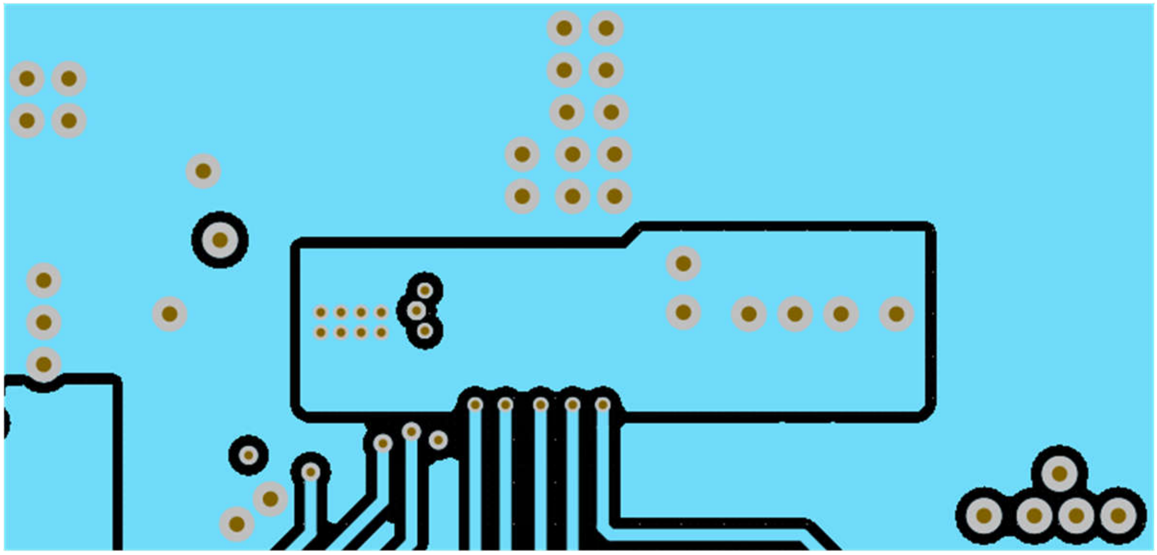


Figure 11-3. Layout Example: Inner Layer 3 (AGND pour; SW node pour; signal routing)

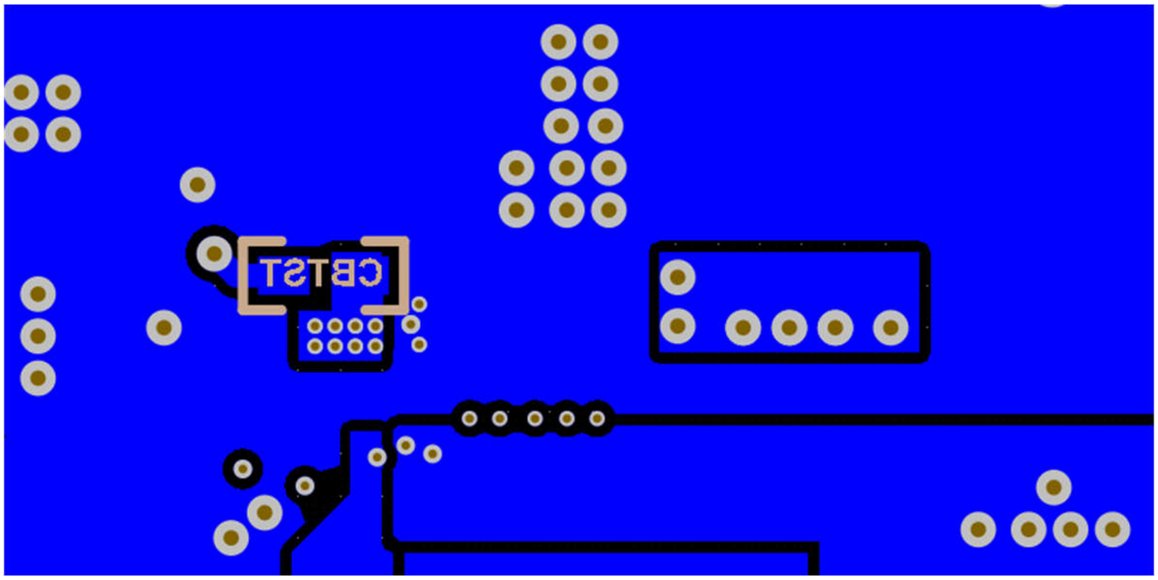


Figure 11-4. Layout Example: Bottom Layer X-Ray From Top (PGND pour; BTST capacitor; redundant SW, SYS and BAT pours)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *BQ25601 and BQ25601D (PWR877) Evaluation Module User's Guide*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2024) to Revision C (February 2024)	Page
• Changed T_{TOP_OFF} Typical and Maximum Limit.	16
• Changed T_{SAFETY_TRKCHG} Typical and Maximum Limit.	16
• Changed T_{SAFETY_PRECHG} Typical and Maximum Limit.	16
• Changed T_{SAFETY} Typical and Maximum Limit.	16
• Changed T_{BATEFT_DLY} Typical Value.	16
• Changed T_{SM_EXIT} Typical and Maximum Limit.	16
• Changed T_{QON_RST} Typical and Maximum Limit.	16
• Changed T_{BATEFT_RST} Typical Value.	16
• Changed T_{LP_WDT} Typical Value.	16
• Changed T_{WDT} Typical Value.	16
• Changed recommended values of RT1 and RT2 in Section 8.3.5.4.2	26
• Added I^2C timing requirements for fast mode and fast mode plus in Section 8.5.1	37
• Changed TOPOFF_TMR values in Charge_Control_0 Register Description, PRECHG_TMR and CHG_TMR values in Charge_Timer_Control Register Description, and WATCHDOG values in Charger_Control_1 Register Description.	40
• Updated behavior of IBAT_ADC in IBAT_ADC Register Description.	40

Changes from Revision A (October 2022) to Revision B (January 2024)	Page
• Added IEC 62368-1 CB Certification.	1
• Changed BQ25620/2 Simplified Application Diagram.	1
• Changed constant current limit from 3.2 A to 2.4 A in Section 4	3
• Changed OTG Current Limit from 3.2 A to 2.4 A for BQ25620/22 in Table 5-1	4
• Changed t_{RST} to t_{QON_RST} in $\overline{QON}$ pin description.	5
• Added Maximum limit to $V_{POORSRC}$	8
• Updated V_{TS_COLD}, V_{TS_COLDZ}, V_{TS_COOL}, V_{TS_COOLZ}, V_{TS_WARM}, V_{TS_WARMZ}, V_{TS_HOT}, and V_{TS_HOTZ}. Updated I_{OTG_RANGE}. Updated VBUS_ADC, VPMID_ADC, and TDIE_ADC.	8
• Changed IBAT_ADC LSB from 2mA to 4mA.	8
• Removed typical specs for $t_{VBUS\_OVP\_PROP}$, $T_{POORSRC\_RETRY}$, $t_{POORSRC\_RESTART}$, t_{VBUS_PD}, t_{TERM_DGL}, t_{RECHG_DGL}	16
• Clarified register conditions for T_{TOP_OFF} specifications.	16
• Clarified behavior of JEITA Charge Rate Scaling.	28
• Deleted *When the charger enters HIZ mode, the ADC is disabled.* from Section 8.3.7	29
• Added Section 8.3.8.2	29
• Added Section 8.3.10	33
• Changed IOTG from 3200mA and A0h to 2400mA and 78h in REG0x0A_IOTG_Regulation Register Field Descriptions.	40
• Changed VBUS_ADC from 19850mV and 1388h to 18000mV and 11B6h in REG0x2C_VBUS_ADC Register Field Descriptions.	40
• Changed VPMID_ADC from 19850mV and 1388h to 18000mV and 11B6h in REG0x2E_VPMID_ADC Register Field Descriptions.	40
• Changed TDIE_ADC from 150°C and 12Ch to 140°C and 118h in REG0x36_TDIE_ADC Register Field Descriptions.	40
• Changed Q1_FULLON, BATFET_CTRL_WVBUS bit access type from R to RW and TDIE_ADC bit access type from RW to R.	40
• Changed register fields and descriptions for REG0x02_Charge_Current_Limit register, REG0x10_Pre-charge_Control register, and REG0x12_Termination_Control register	40

- Changed Figure 9-11 69

Changes from Revision * (September 2022) to Revision A (October 2022) **Page**

- Changed BQ25622 from Preview to Production Data.. 1

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25620RYKR	ACTIVE	WQFN-HR	RYK	18	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	BQ620	Samples
BQ25622RYKR	ACTIVE	WQFN-HR	RYK	18	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	BQ622	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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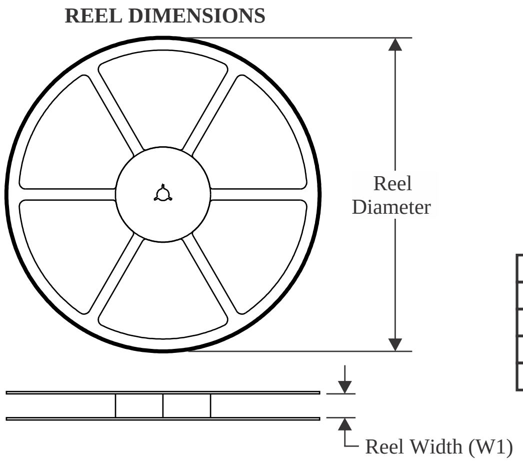
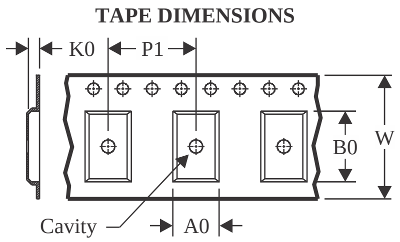
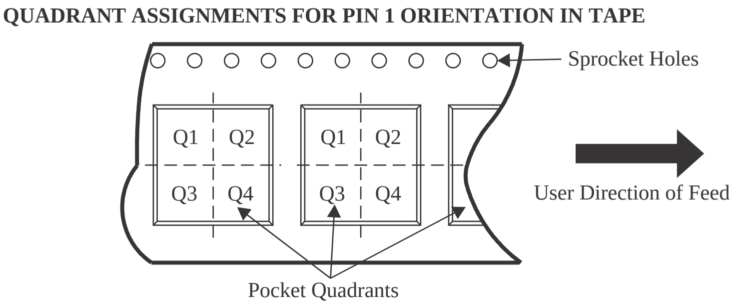
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





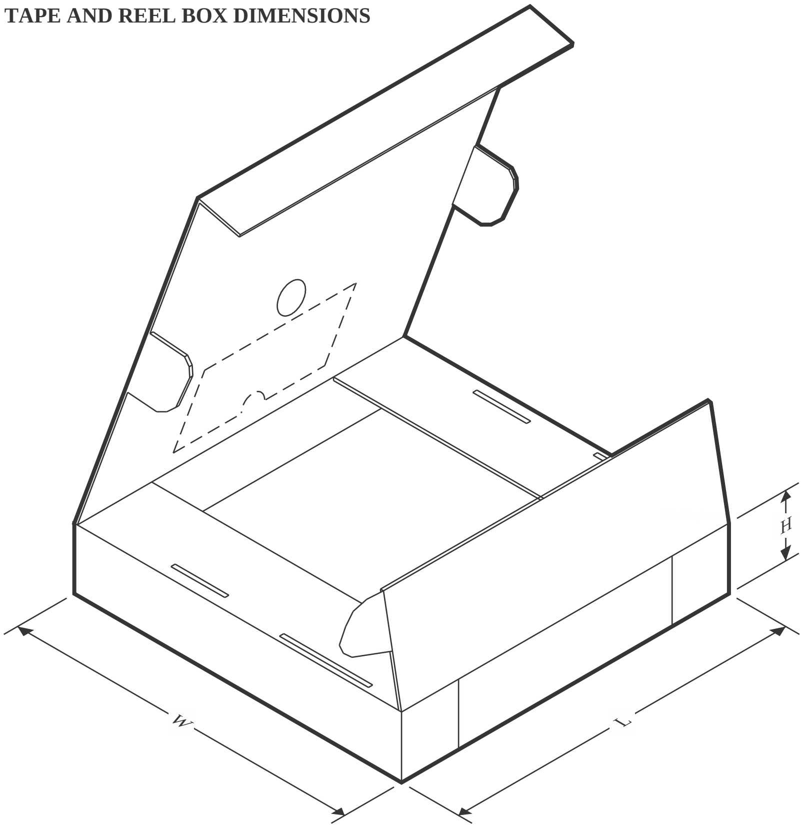
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25622RYKR	WQFN-HR	RYK	18	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

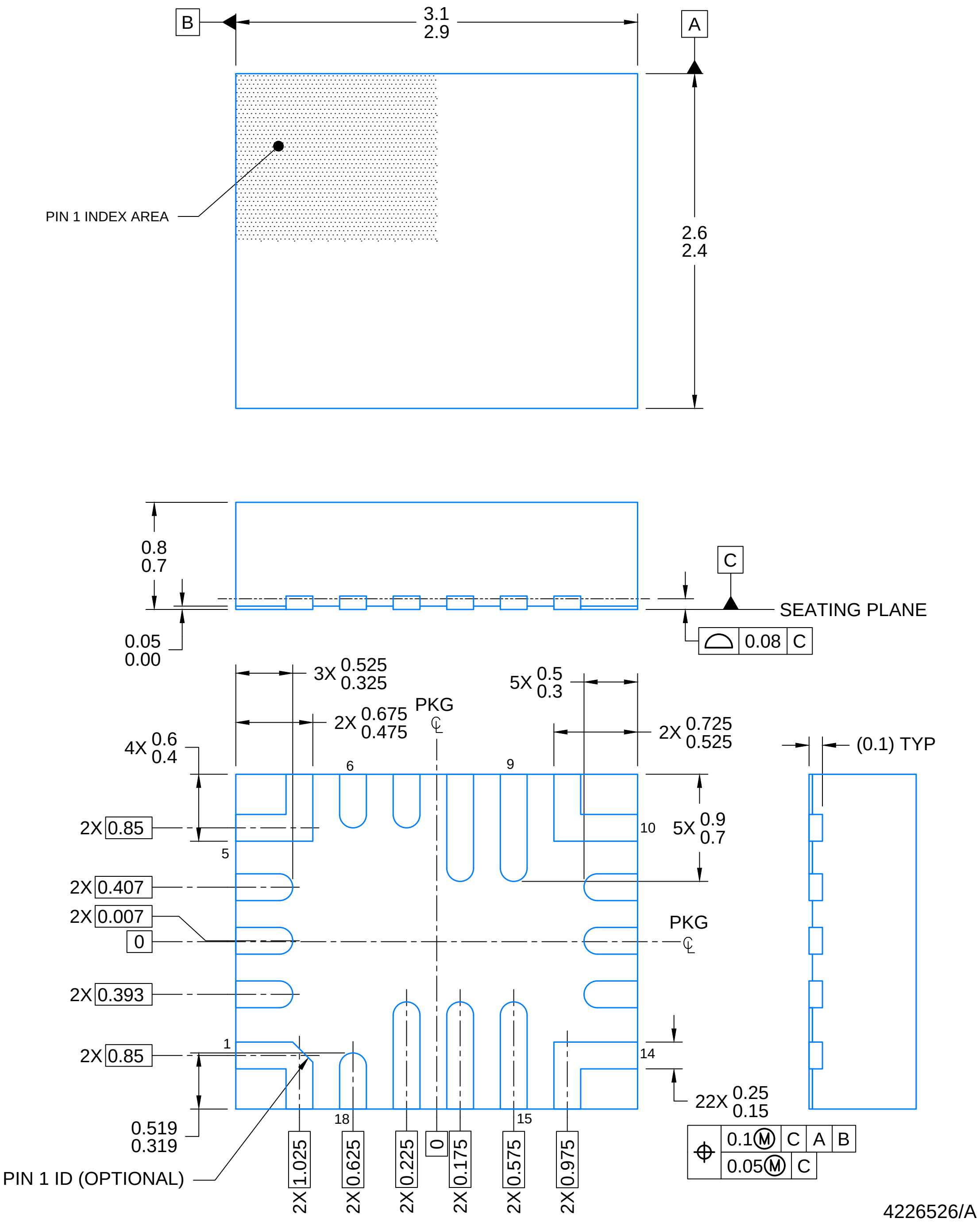
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25622RYKR	WQFN-HR	RYK	18	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RYK0018A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



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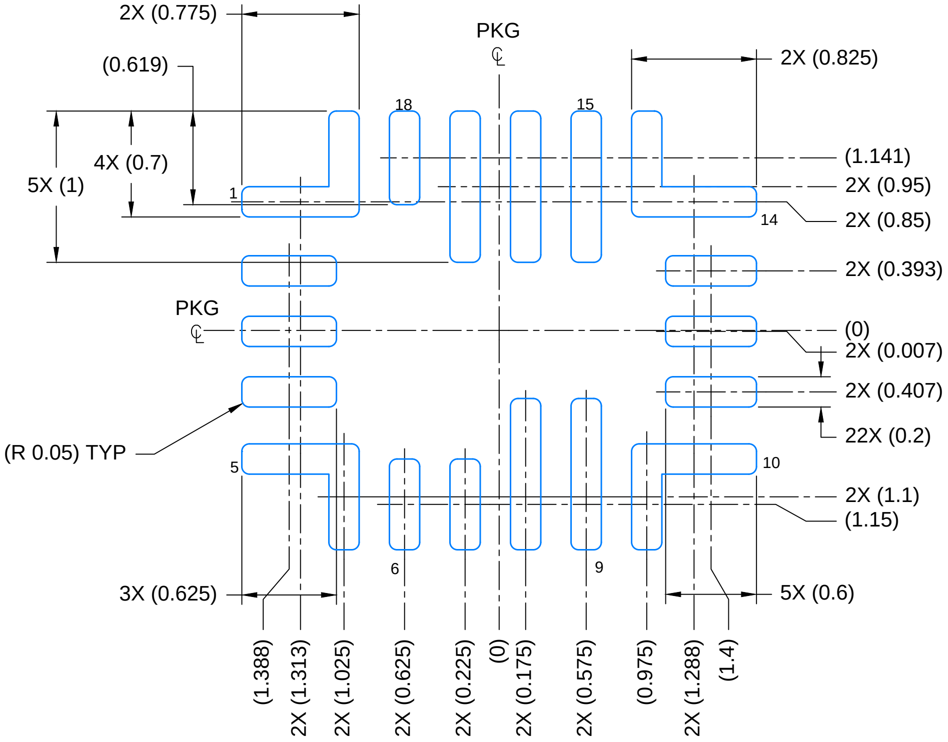
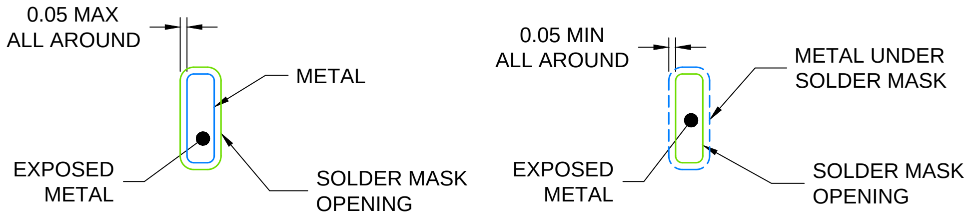
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



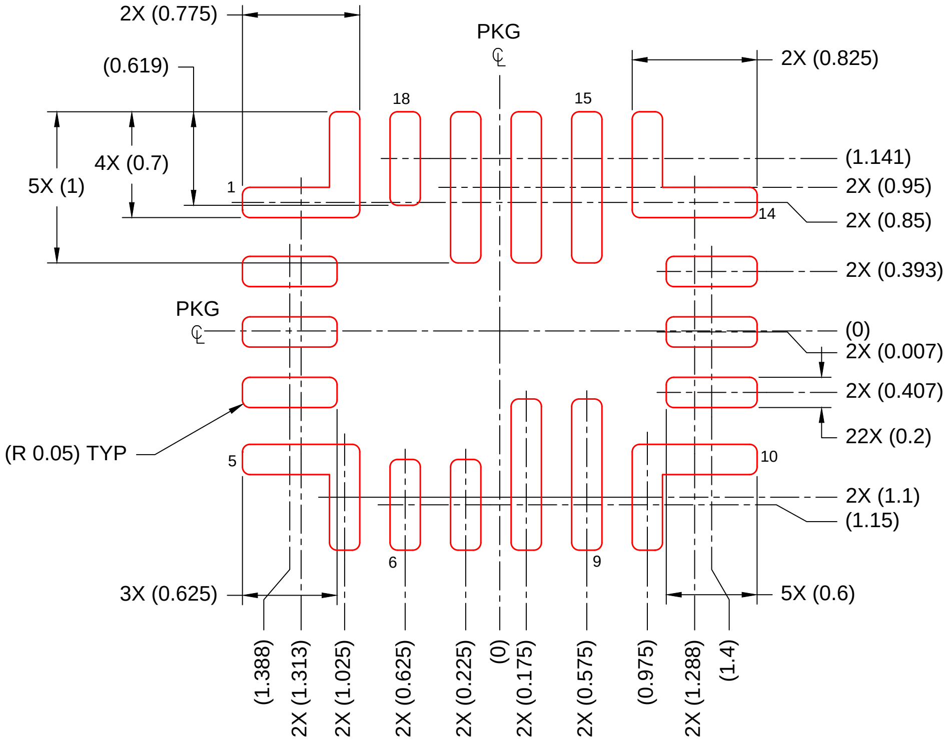
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 20X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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