

# BQ29209-Q1 Voltage Protection with Automatic Cell Balance for 2-Series Cell Li-Ion Batteries

## 1 Features

- 2-series cell secondary protection
- Automatic cell imbalance correction with external enable control
  - $\pm 30$ -mV enable, 0-mV disable thresholds typical
- External capacitor-controlled delay timer
- External resistor-controlled cell balance current
- Low power consumption  $I_{CC} < 3 \mu\text{A}$  typical ( $V_{CELL(ALL)} < V_{PROTECT}$ )
- Internal cell balancing handles current up to 15 mA
- External cell balancing mode supported
- High-accuracy overvoltage protection:
  - $\pm 25$  mV with  $T_A = 0^\circ\text{C}$  to  $60^\circ\text{C}$
- Fixed overvoltage protection threshold: 4.30 V
- Small 8L DRB package
- [Functional Safety-Capable](#)
  - [Documentation available to aid functional safety system design](#)
- Automotive-qualified AEC Q100 grade two

## 2 Applications

- 2<sup>nd</sup> level protection in li-ion battery packs
  - Emergency call (eCall)
  - Netbook computers
  - Power tools
  - Portable equipment and instrumentation
  - Battery backup systems

## 3 Description

The BQ29209-Q1 device is a secondary overvoltage protection IC for 2-series cell lithium-ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit and automatic cell imbalance correction.

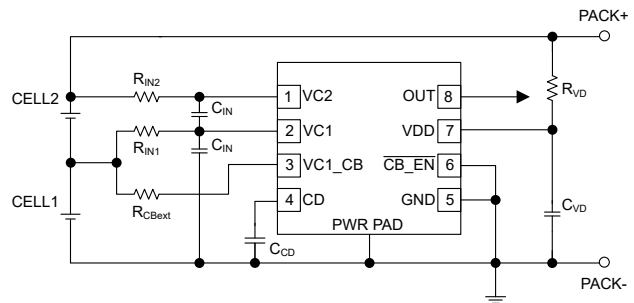
The voltage of each cell in a 2-series cell battery pack is compared to a factory programmed internal reference voltage. If either cell reaches an overvoltage condition, the OUT pin changes from low to high state.

The BQ29209-Q1 can perform automatic voltage-based cell imbalance correction. Balancing can start when the cell voltages are different by nominally 30 mV or more and stops when the difference is nominally 0 mV. Cell balancing is enabled and disabled by the  $\overline{\text{CB\_EN}}$  pin.

### Device Information

PART NUMBER <sup>(1)</sup>	PACKAGE	BODY SIZE (NOM)
BQ29209-Q1	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision C (December 2018) to Revision D (September 2020) Page

- Added the functional safety capable information..... 1

### Changes from Revision B (November 2018) to Revision C (December 2018) Page

- Added a clarification regarding operation if GND is not connected first in sequence..... 8

### Changes from Revision A (March 2016) to Revision B (November 2018) Page

- Changed component names in the *Simplified Schematic* ..... 1
- Changed a component name in *Recommended Operating Conditions* ..... 4
- Added the value of internal cell balancing switch resistances to *Electrical Characteristics* ..... 4
- Changed resistor names ..... 6
- Added [Figure 8-2](#) to clarify the cell balancing description; updated the equations ..... 9
- Changed values and component names in [Figure 9-1](#) ..... 12
- Changed component names and values used in the design example ..... 12
- Changed external cell balancing figure, equations, and description..... 13

### Changes from Revision \* (June 2015) to Revision A (March 2016) Page

- Changed resistor  $R_{VD}$  location, added PACK+ and PACK– in the *Simplified Schematic* ..... 1
- Deleted the Lead Temperature (soldering) from the [Section 7.1](#) table ..... 3
- Changed resistor  $R_{VD}$  location in [Figure 9-1](#) ..... 12
- Added title to [Table 9-1](#) ..... 12
- Changed resistor  $R_{VD}$  location, added PACK+ and PACK– in [Figure 9-3](#) ..... 13

## 5 Device Options

$T_A$	PART NUMBER	OVP
-40°C to +105°C	BQ29209-Q1	4.3 V

## 6 Pin Configuration and Functions

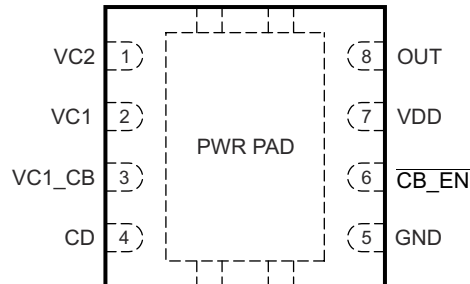


Figure 6-1. DRB Package 8-Pin VSON Top View

### Pin Functions

PIN		DESCRIPTION
NAME	NO.	
CB_EN	6	Cell balance enable
CD	4	Connection to external capacitor for programmable delay time
GND	5	Ground pin
OUT	8	Output
Thermal Pad	PWR PAD	GND pin to be connected to the PWRPAD on the printed circuit board for proper operation
VC1	2	Sense voltage input for bottom cell
VC1_CB	3	Cell balance input for bottom cell
VC2	1	Sense voltage input for top cell
VDD	7	Power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range, $V_{MAX}$	VDD–GND	-0.3	16	V
Input voltage range, $V_{IN}$	VC2–GND, VC1–GND	-0.3	16	V
	VC2–VC1, CD–GND	-0.3	8	V
	CB_EN–GND	-0.3	16	V
Output voltage range, $V_{OUT}$	OUT–GND	-0.3	16	V
Continuous total power dissipation, $P_{TOT}$		See <a href="#">Section 7.4</a> .		
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

		VALUE	UNIT		
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>			
		Charged-device model (CDM), per AEC Q100-011	All pins	±2000	V
			Corner pins (VC2, CD, OUT, and GND)	±500	
		±750			

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4		10	V
Input voltage range	VC2–VC1, VC1–GND	0		5	V
Delay time capacitance, t <sub>d(CD)</sub>	C <sub>CD</sub> (See Figure 9-1.)		0.1		μF
Voltage monitor filter resistance	R <sub>IN</sub> (See Figure 9-1.)	100	1K		Ω
Voltage monitor filter capacitance	C <sub>IN</sub> (See Figure 9-1.)	0.01	0.1		μF
Supply voltage filter resistance	R <sub>VD</sub> (See Figure 9-1.)		100	1K	Ω
Supply voltage filter capacitance	C <sub>VD</sub> (See Figure 9-1.)		0.1		μF
Cell balance resistance	R <sub>CBext</sub> (See Figure 9-1 and Section 8.3.1.)	100		4.7K	Ω
Operating ambient temperature range, T <sub>A</sub>		–40		105	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		BQ29209-Q1			UNIT
		DRB			
		8 PINS			
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	50.5			°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	25.1			°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	19.3			°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.7			°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	18.9			°C/W
R <sub>θJC(bot)</sub>	Junction-to-case(bottom) thermal resistance	5.2			°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

Typical values stated where T<sub>A</sub> = 25°C and VDD = 7.2 V. Minimum and maximum values stated where T<sub>A</sub> = –40°C to 105°C and VDD = 4 V to 10 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V <sub>PROTECT</sub>	Overvoltage detection voltage					4.3		V
V <sub>HYS</sub>	Overvoltage detection hysteresis				200	300	400	mV
V <sub>OA</sub>	Overvoltage detection accuracy	T <sub>A</sub> = 25°C			–10		10	mV
V <sub>OA_DRIFT</sub>	Overvoltage threshold temperature drift	T <sub>A</sub> = 0°C to 60°C			–0.4		0.4	mV/°C
		T <sub>A</sub> = –40°C to 110°C			–0.6		0.6	
X <sub>DELAY</sub>	Overvoltage delay time scale factor	T <sub>A</sub> = 0°C to 60°C Note: Does not include external capacitor variation.			6	9	12	s/μF
		T <sub>A</sub> = –40°C to 110°C Note: Does not include external capacitor variation.			5.5	9	13.5	

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 7.2\text{ V}$ . Minimum and maximum values stated where  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  and  $V_{DD} = 4\text{ V}$  to  $10\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$X_{\text{DELAY\_CTM}}$ <sup>(1)</sup>	Overvoltage delay time scale factor in Customer Test Mode			0.08		s/ $\mu\text{F}$
$I_{\text{CD(CHG)}}$	Overvoltage detection charging current			150		nA
$I_{\text{CD(DSG)}}$	Overvoltage detection discharging current			60		$\mu\text{A}$
$V_{\text{CD}}$	Overvoltage detection external capacitor comparator threshold			1.2		V
$I_{\text{CC}}$	Supply current	$(V_{\text{C2}} - V_{\text{C1}}) = (V_{\text{C1}} - \text{GND}) = 3.5\text{ V}$ (See <a href="#">Figure 8-5.</a> )		3	6	$\mu\text{A}$
$V_{\text{OUT}}$	OUT pin drive voltage	$(V_{\text{C2}} - V_{\text{C1}})$ or $(V_{\text{C1}} - \text{GND}) > V_{\text{PROTECT}}$ , $V_{\text{DD}} = 10\text{ V}$ , $I_{\text{OH}} = 0$	6	8.25	9.5	V
		$(V_{\text{C2}} - V_{\text{C1}})$ or $(V_{\text{C1}} - \text{GND}) = V_{\text{PROTECT}}$ , $V_{\text{DD}} = V_{\text{PROTECT}}$ , $I_{\text{OH}} = -100\ \mu\text{A}$ , $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$	1.75	2.5		V
		$(V_{\text{C2}} - V_{\text{C1}})$ and $(V_{\text{C1}} - \text{GND}) < V_{\text{PROTECT}}$ , $I_{\text{OL}} = 100\ \mu\text{A}$ , $T_A = 25^\circ\text{C}$			200	mV
		$(V_{\text{C2}} - V_{\text{C1}})$ and $(V_{\text{C1}} - \text{GND}) < V_{\text{PROTECT}}$ , $I_{\text{OL}} = 0\ \mu\text{A}$ , $T_A = 25^\circ\text{C}$		0	10	mV
		$V_{\text{C2}} = V_{\text{C1}} = V_{\text{DD}} = 4\text{ V}$ , $I_{\text{OL}} = 100\ \mu\text{A}$			200	mV
$I_{\text{OH}}$	High-level output current	OUT = 1.75 V, $(V_{\text{C2}} - V_{\text{C1}})$ or $(V_{\text{C1}} - \text{GND}) = V_{\text{PROTECT}}$ , $V_{\text{DD}} = V_{\text{PROTECT}}$ to 10 V, $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$	-100			$\mu\text{A}$
$I_{\text{OL}}$	Low-level output current	OUT = 0.05 V, $(V_{\text{C2}} - V_{\text{C1}})$ or $(V_{\text{C1}} - \text{GND}) < V_{\text{PROTECT}}$ , $V_{\text{DD}} = V_{\text{PROTECT}}$ to 10 V, $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$	30		85	$\mu\text{A}$
$I_{\text{OH\_ZV}}$	High-level short-circuit output current	OUT = 0 V, $(V_{\text{C2}} - V_{\text{C1}}) = (V_{\text{C1}} - \text{GND}) = V_{\text{PROTECT}}$ , $V_{\text{DD}} = 4$ to 10 V			-8	mA
$I_{\text{IN}}$	Input current at VCx pins	Measured at VC1, $(V_{\text{C2}} - V_{\text{C1}}) = (V_{\text{C1}} - \text{GND}) = 3.5\text{ V}$ , $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$ (See <a href="#">Figure 8-5.</a> )	-0.2		0.2	$\mu\text{A}$
		Measured at VC2, $(V_{\text{C2}} - V_{\text{C1}}) = (V_{\text{C1}} - \text{GND}) = 3.5\text{ V}$ , $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$ (See <a href="#">Figure 8-5.</a> )			2.5	$\mu\text{A}$
$V_{\text{MM\_DET\_ON}}$	Cell mismatch detection threshold for turning ON	$(V_{\text{C2}} - V_{\text{C1}})$ versus $(V_{\text{C1}} - \text{GND})$ and vice-versa when cell balancing is enabled. $V_{\text{C2}} = V_{\text{DD}} = 7.6\text{ V}$	17	30	45	mV
$V_{\text{MM\_DET\_OFF}}$	Cell mismatch detection threshold for turning OFF	Delta between $(V_{\text{C2}} - V_{\text{C1}})$ and $(V_{\text{C1}} - \text{GND})$ when cell balancing is disabled. $V_{\text{C2}} = V_{\text{DD}} = 7.6\text{ V}$	-9	0	9	mV
$V_{\text{CB\_EN\_ON}}$	Cell balance enable ON threshold	Active LOW pin at $\overline{\text{CB\_EN}}$			1	V
$V_{\text{CB\_EN\_OFF}}$	Cell balance enable OFF threshold	Active HIGH at $\overline{\text{CB\_EN}}$	2.2			V
$I_{\text{CB\_EN}}$	Cell balance enable ON input current	$\overline{\text{CB\_EN}} = \text{GND}$ (See <a href="#">Figure 8-6.</a> )			0.2	$\mu\text{A}$
$R_{\text{CB1int}}$	Internal cell balance switch resistance	$\overline{\text{CB\_EN}} = \text{GND}$		300		$\Omega$
$R_{\text{CB2int}}$	Internal cell balance switch resistance	$\overline{\text{CB\_EN}} = \text{GND}$		235		$\Omega$

(1) Specified by design. Not 100% tested in production.

## 7.6 Recommended Cell Balancing Configurations

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $(VC2-VC1), (VC1-GND) = 3.8\text{ V}$ . Minimum and maximum values stated where  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$ ,  $VDD = 4\text{ V}$  to  $10\text{ V}$ , and  $(VC2-VC1), (VC1-GND) = 3\text{ V}$  to  $4.2\text{ V}$ . All values assume recommended supply voltage filter resistance  $R_{VD}$  of  $100\ \Omega$  and 5% accurate or better cell balance resistor  $R_{CBext}$ .

		MIN	NOM	MAX	UNIT
$I_{CB}$	Cell balance input current				mA
	$R_{CBext} = 4700\ \Omega$	0.5	0.75	1	
	$R_{CBext} = 2200\ \Omega$	1	1.5	2	
	$R_{CBext} = 910\ \Omega$	2	3	4	
	$R_{CBext} = 560\ \Omega$	3	4.5	6	
	$R_{CBext} = 360\ \Omega$	3.5	6	8.5	
	$R_{CBext} = 240\ \Omega$	4	7.5	11	
$R_{CBext} = 120\ \Omega$	5	10	15		

## 7.7 Typical Characteristics

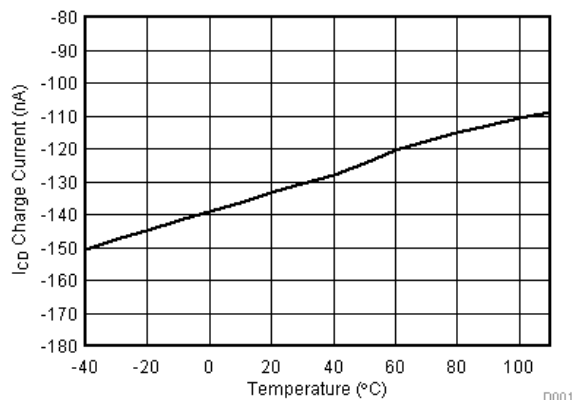


Figure 7-1.  $I_{CD}$  Charge Current

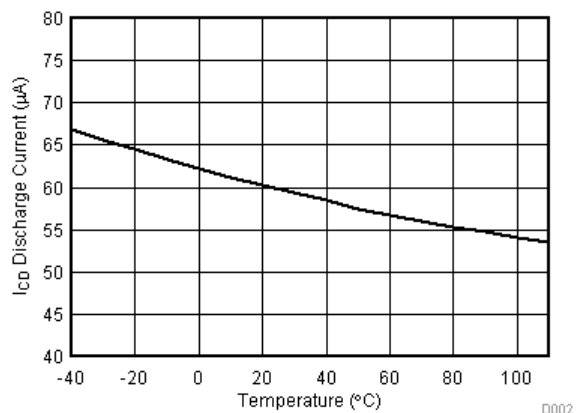


Figure 7-2.  $I_{CD}$  Discharge Current

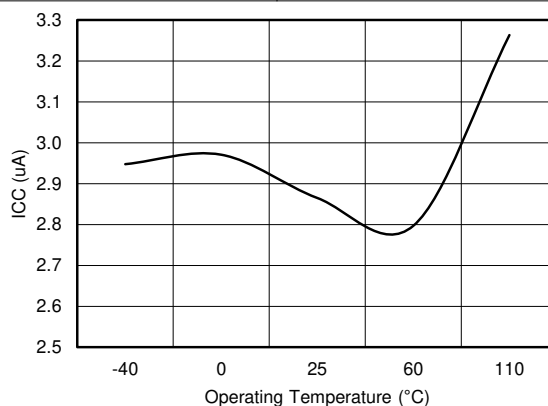


Figure 7-3. Average  $I_{CC}$  During Normal Operation Across Operational Temperature

## 8 Detailed Description

### 8.1 Overview

The BQ29209-Q1 provides overvoltage protection and cell balancing for 2-series cell lithium-ion battery packs.

#### 8.1.1 Voltage Protection

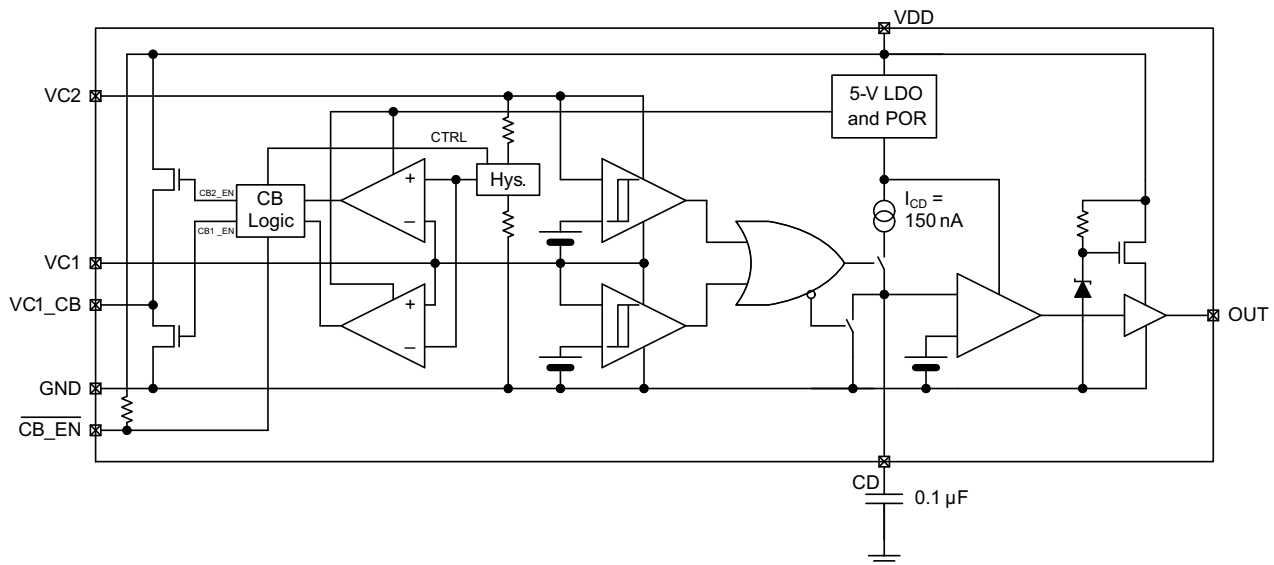
Each cell voltage is continuously compared to a factory configured internal reference threshold. If either cell reaches an overvoltage condition, the BQ29209-Q1 device starts a timer that provides a delay proportional to the capacitance on the CD pin. Upon expiration of the internal timer, the OUT pin changes from a low to high state.

#### 8.1.2 Cell Balancing

If enabled, the BQ29209-Q1 performs automatic cell-balance correction where the two cells are automatically corrected for voltage imbalance by loading the cell with the higher voltage with a small balancing current. When the cells are measured to be equal within nominally 0 mV, the load current is removed. It will be re-applied if the imbalance exceeds nominally 30 mV. The cell mismatch correction circuitry is enabled by pulling the  $\overline{\text{CB\_EN}}$  pin low, and disabled when  $\overline{\text{CB\_EN}}$  is pulled to greater than 2.2 V, for example, VDD.

If the internal cell balancing current of up to 15 mA is insufficient, the BQ29209-Q1 may be configured via external circuitry to support much higher external cell balancing current.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Protection (OUT) Timing

Sizing the external capacitor is based on the desired delay time as follows:

$$C_{CD} = \frac{t_d}{X_{DELAY}}$$

Where  $t_d$  is the desired delay time and  $X_{DELAY}$  is the overvoltage delay time scale factor, expressed in seconds per microfarad.  $X_{DELAY}$  is nominally 9 s/ $\mu\text{F}$ . For example, if a nominal delay of 3 seconds is desired, use a  $C_{CD}$  capacitor that is 3 s / 9 s/ $\mu\text{F}$  = 0.33  $\mu\text{F}$ .

The delay time is calculated as follows:

$$t_d = C_{CD} \times X_{DELAY}$$

If the cell overvoltage condition is removed before the external capacitor reaches the reference voltage, the internal current source is disabled and an internal discharge block is employed to discharge the external capacitor down to 0 V. In this instance, the OUT pin remains in a low state.

### 8.3.2 Cell Voltage > $V_{\text{PROTECT}}$

When one or both of the cell voltages rises above  $V_{\text{PROTECT}}$ , the internal comparator is tripped, and the delay begins to count to  $t_d$ . If the input remains above  $V_{\text{PROTECT}}$  for the duration of  $t_d$ , the BQ29209-Q1 output changes from a low to a high state, by means of an internal pull-up network, to a regulated voltage of no more than 9.5 V when  $I_{\text{OH}} = 0$  mA.

The external delay capacitor should charge up to no more than the internal LDO voltage (approximately 5 V typically), and will fully discharge in approximately under 100 ms when the overvoltage condition is removed.

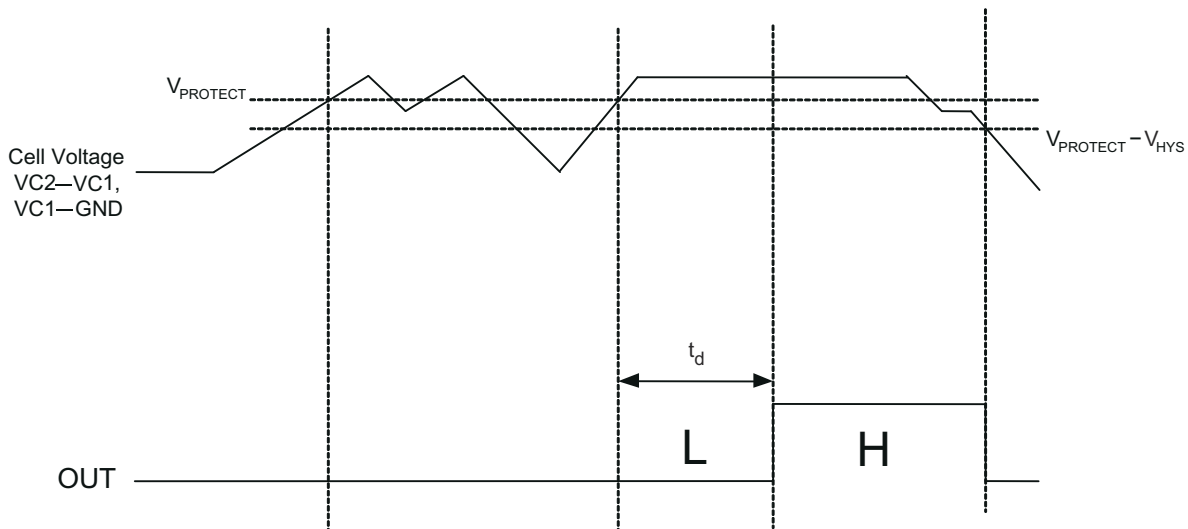


Figure 8-1. Timing for Overvoltage Sensing

### 8.3.3 Cell Connection Sequence

#### Note

Before connecting the cells, populate the overvoltage delay timing capacitor,  $C_{\text{CD}}$ .

The recommended cell connection sequence begins from the bottom of the stack, as follows:

1. GND
2. VC1
3. VC2

While not advised, connecting the cells in a sequence other than that described above does not result in errant activity on the OUT pin. For example:

1. GND
2. VC2 or VC1
3. Remaining VCx pin

#### Note

Using any cell connection sequence that does not connect GND first may result in increased leakage current drawn by the VDD pin.

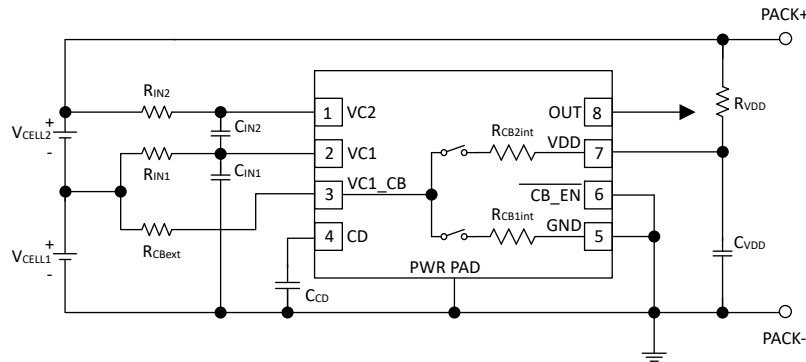
### 8.3.4 Cell Balance Enable Control

To avoid prematurely discharging the cells, it is recommended to turn off (pull high) the active-low Cell Balance Enable Control pin at lower state-of-charge (SOC) levels.



### 8.3.5 Cell Balance Configuration

The following cell balancing details relate to [Figure 8-2](#).



**Figure 8-2. Simplified Schematic for Cell Balancing Description**

The cell balancing current may be calculated as follows:

For Cell 1 balancing current,  $I_{CB1}$ :

$$I_{CB1} = \frac{V_{CELL1}}{R_{CBext} + R_{CB1int}} \quad (1)$$

For Cell 2 balancing current,  $I_{CB2}$ :

$$I_{CB2} = \frac{V_{CELL2}}{R_{CBext} + R_{CB2int} + R_{VDD}} \quad (2)$$

Where:

$R_{CBext}$  = resistor connected between the top of Cell 1 and the VC1\_CB pin

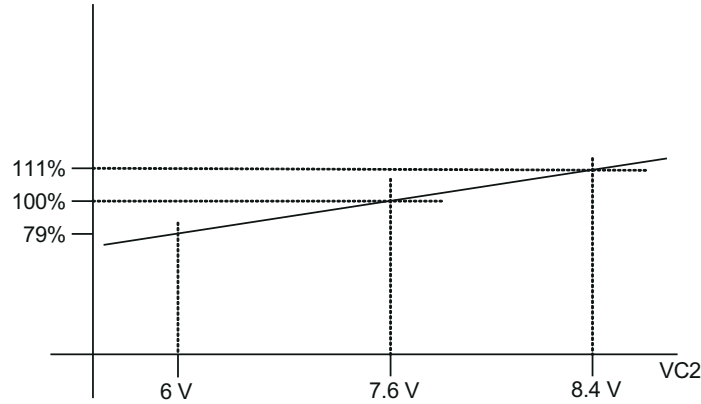
$R_{IN1}$  = resistor connected between the top of Cell 1 and the VC1 pin

$R_{IN2}$  = resistor connected between the top of Cell 2 and the VC2 pin

$R_{VDD}$  = resistor connected between the top of Cell 2 and the VDD pin

### 8.3.6 Cell Imbalance Auto-Detection (Via Cell Voltage)

The  $V_{MM\_DET\_ON}$  and  $V_{MM\_DET\_OFF}$  specifications are calibrated where  $VDD = VC2 = 7.6\text{ V}$  and  $VC1 = 3.8\text{ V}$ . The recommended range of cell balancing is  $VC2$  and  $VDD$  between  $6.0\text{ V}$  and  $8.4\text{ V}$ , and  $VC1$  between  $3\text{ V}$  and  $4.2\text{ V}$ . Below  $VDD = 6\text{ V}$ , it is recommended to pull  $CB\_EN$  high to disable the cell balancing function.



**Figure 8-3.  $V_{MM\_DET\_ON}$  and  $V_{MM\_DET\_OFF}$  Threshold**

### 8.3.7 Customer Test Mode

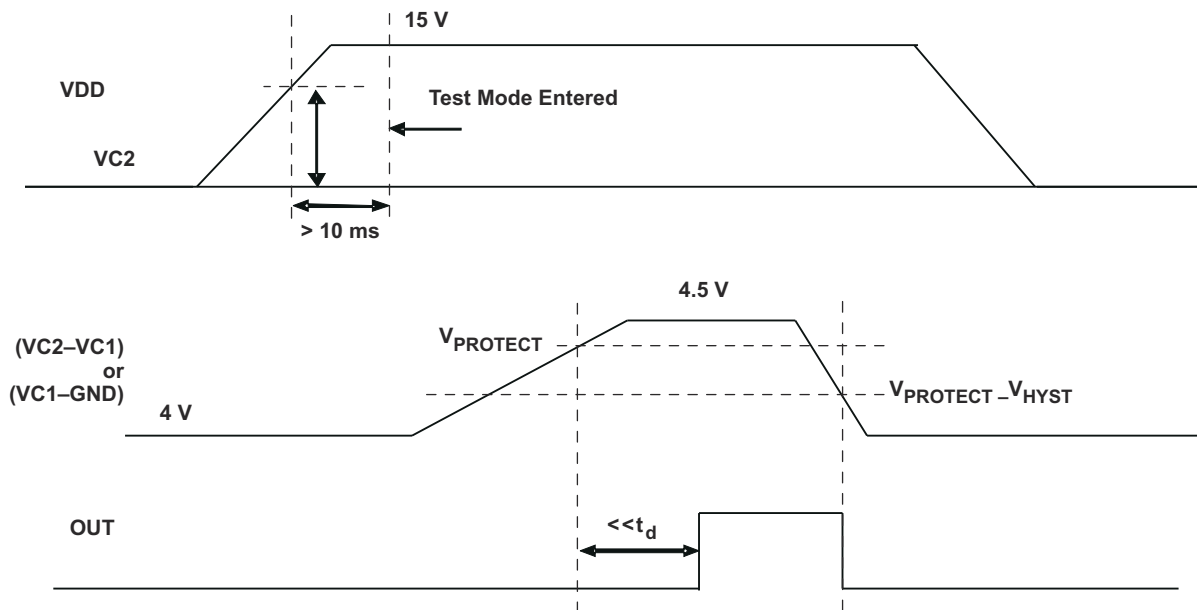
Customer Test Mode (CTM) helps to greatly reduce the overvoltage detection delay time and enable quicker customer production testing. This mode is intended for quick-pass board-level verification tests, and, as such, individual cell overvoltage levels may deviate slightly from the specifications ( $V_{PROTECT}$ ,  $V_{OA}$ ). If accurate overvoltage thresholds are to be tested, use the standard delay settings that are intended for normal use.

To enter CTM, VDD should be set to approximately 9.5 V higher than VC2. When CTM is entered, the device switches from the normal overvoltage delay time scale factor,  $X_{DELAY}$ , to a significantly reduced factor of approximately 0.08, thereby reducing the delay time during an overvoltage condition.

**CAUTION**

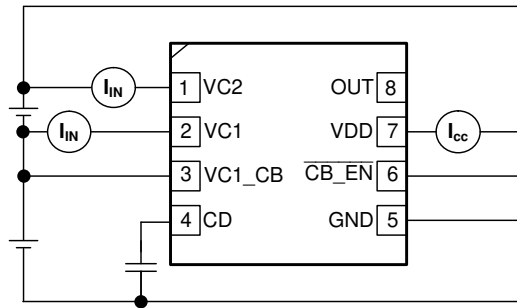
Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also, avoid exceeding absolute maximum voltages for the individual cell voltages (VC1–GND) and (VC2–VC1). Stressing the pins beyond the rated limits may cause permanent damage to the device.

To exit CTM, power off the device and then power it back on.

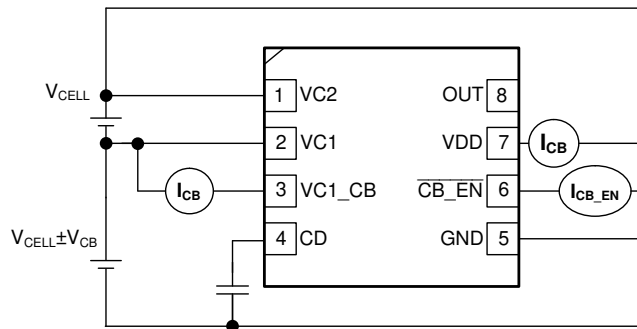


**Figure 8-4. Voltage Test Limits**

### 8.3.8 Test Conditions



**Figure 8-5.  $I_{CC}$ ,  $I_{IN}$  Measurement**



**Figure 8-6.  $I_{CB}$  Measurement**

## 8.4 Device Functional Modes

This device monitors the voltage of the cells connected to the VCx pins and depending on these voltages and the overall battery voltage at VDD the device enters different operating modes.

### 8.4.1 NORMAL Mode

The device is operating in NORMAL mode when the cell voltage range is between the over-charge detection threshold ( $V_{PROTECT}$ ) and the minimum supply voltage.

If this condition is satisfied, the device turns OFF the OUT pin.

### 8.4.2 PROTECTION Mode

The device is operating in PROTECTION mode when the cell over voltage protection feature has been triggered. See [Section 8.3.2](#) for more details on this feature.

If this condition is satisfied, the device turns ON the OUT pin.

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The BQ29209-Q1 is designed to be used in 2-series Li-Ion battery packs and with the option to include voltage-based cell balancing. The number of parallel cells or the overall capacity of the battery only affects the cell balancing circuit due to the level of potential imbalance that needs to be corrected.

## 9.2 Typical Applications

### 9.2.1 Battery Connection

Figure 9-1 shows the configuration for the 2-series cell battery connection with cell balancing enabled.

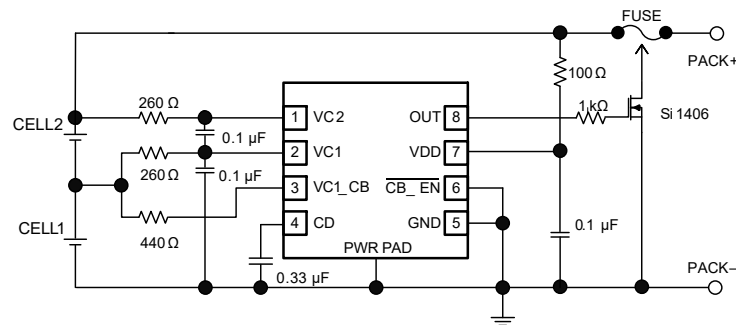


Figure 9-1. 2-Series Cell Configuration

#### 9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE at $T_A = 25^\circ\text{C}$
Input voltage range	4 V to 10 V
Overvoltage Protection (OVT)	4.3 V
Overvoltage detection delay time	3 s
Overvoltage detection delay timer capacitor	0.33 $\mu\text{F}$
Cell Balancing Enabled	Yes
Cell Balancing Current, $I_{CB1}$ and $I_{CB2}$	5 mA (targeted at a nominal cell voltage of 3.8 V)
Cell Balancing Resistors, $R_{CBext}$ , $R_{IN1}$ , $R_{IN2}$ and $R_{VD}$	$R_{CBext} = 440\ \Omega$ , $R_{IN1} = 260\ \Omega$ , $R_{IN2} = 260\ \Omega$ , $R_{VD} = 100\ \Omega$

#### 9.2.1.2 Detailed Design Procedure

The BQ29209-Q1 has limited features but there are some key calculations to be made when selecting external component values.

- Calculate the required  $C_{CD}$  capacitor value for the voltage protection delay time. Care should be taken to evaluate the tolerances of the capacitor and the BQ29209-Q1 to ensure system specifications are met.
- Calculate the cell balancing resistor values to provide a suitable level of balancing current that will, at a minimum, counter act an increase in imbalance during normal operation of the battery. Care should be taken to ensure any connectivity resistance is also considered as this will also reduce the balancing current level.

### 9.2.1.3 Application Curve

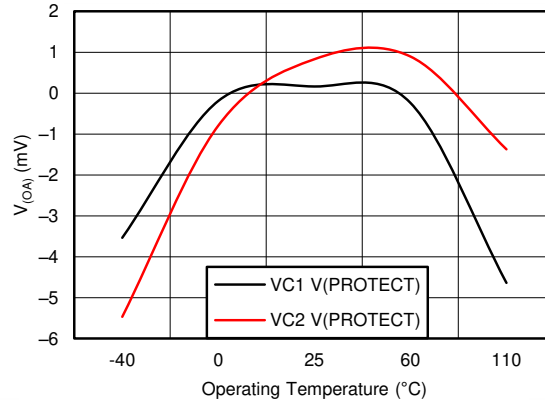


Figure 9-2. Average  $V_{\text{PROTECT}}$  Accuracy ( $V_{\text{OA}}$ ) Across Operation Temperature

## 9.3 System Example

### 9.3.1 External Cell Balancing

Higher cell balancing currents can be supported by means of a simple external network, as shown in Figure 9-3.

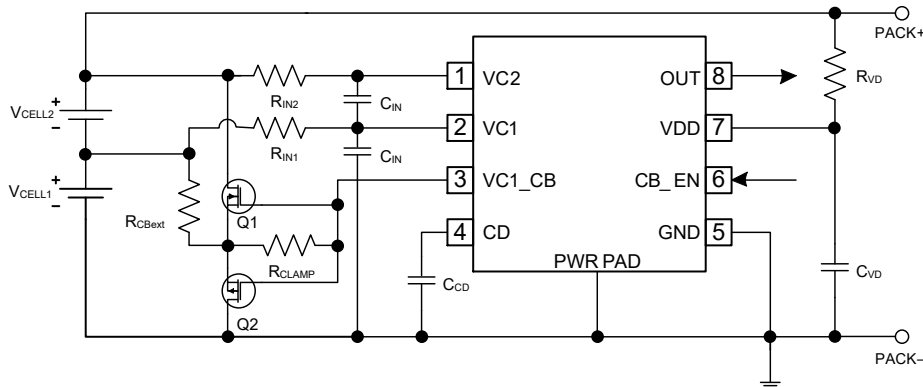


Figure 9-3. External Cell Balancing Configuration

The VC1\_CB pin is tri-stated when cell balancing is disabled, is driven low by the internal logic to enable balancing on CELL1, and is driven high by the internal logic to enable balancing on CELL2.  $R_{\text{CLAMP}}$  ensures that both Q1 and Q2 remain off when balancing is disabled, and should be sized above 2 k $\Omega$  to prevent excessive internal device current when the balancing network is activated. If  $R_{\text{CLAMP}}$  is too small, then the gate-source voltage required to enable the external FETs cannot be achieved.  $R_{\text{CBext}}$  determines the value of the balancing current, and is dependent on the voltage of the balanced cell and the specific Q1 and Q2 transistors used in the design (due to the transistors operating in saturation mode during balancing). The balancing currents (assuming the current through  $R_{\text{CLAMP}}$  is not significant) are given as follows:

$$I_{CB1} = \frac{(V_{CELL1} - V_{SG\_Q2})}{R_{CBext}} \quad (3)$$

$$I_{CB2} = \frac{(V_{CELL2} - V_{GS\_Q1})}{R_{CBext}} \quad (4)$$

## 10 Power Supply Recommendations

The recommended power supply for this device is a maximum 10-V operation on the VDD input pin.


## 11 Layout


### 11.1 Layout Guidelines

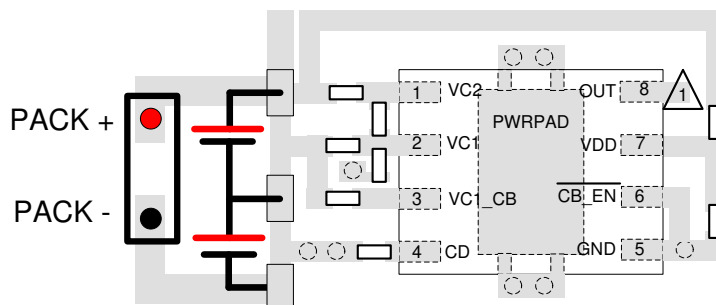
The following are the recommended layout guidelines:

1. Ensure the input filters to the VC1 and VC2 pins are as close to the IC as possible to improve noise immunity.
2. If the OUT pin is used to control a high current path, for example: to blow a chemical fuse, then care should be taken to ensure the high current path creates minimal interference of the BQ29209-Q1 voltage sense inputs.
3. The input RC filter on the VDD pin should be close to the terminal of the IC.

### 11.2 Layout Example

 Additional circuitry required based on usage of the OUT pin

 Via connects between two layers



## 12 Device and Documentation Support

### 12.1 Documentation Support

For additional information, see the following related document:

- [BQ29209-Q1 Functional Safety FIT Rate, FMD, and Pin FMA Application Report](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29209TDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	209Q1	<a href="#">Samples</a>
BQ29209TDRBTQ1	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	209Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF BQ29209-Q1 :**

- Catalog: [BQ29209](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29209TDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29209TDRBTQ1	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29209TDRBRQ1	SON	DRB	8	3000	346.0	346.0	33.0
BQ29209TDRBTQ1	SON	DRB	8	250	210.0	185.0	35.0

**DRB 8**

**GENERIC PACKAGE VIEW**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203482/L

DRB0008B



# PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
81% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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