

## CD74AC238 3-Line to 8-Line Decoder/Demultiplexer

### 1 Features

- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply voltage
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporates three enable inputs to simplify cascading and/or data reception
- Balanced propagation delays
- $\pm 24\text{mA}$  output drive current
  - Fanout to 15 F devices
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

### 2 Description

The CD74AC238 decoder/demultiplexer is designed for high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding.

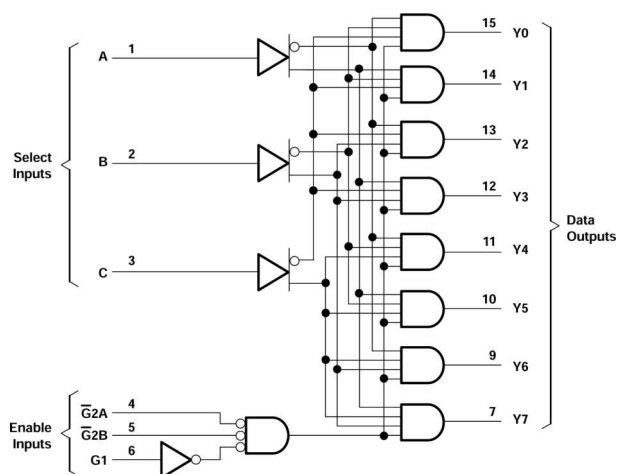
#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
CD74AC238	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.40mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

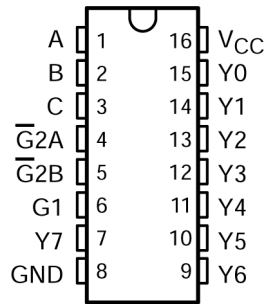
(3) The body size (length × width) is a nominal value and does not include pins.



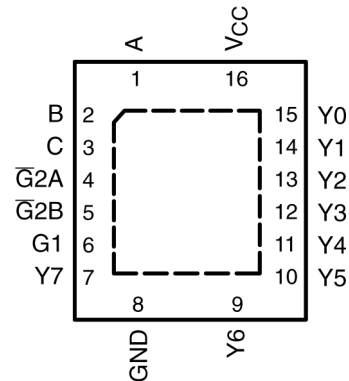
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### 3 Pin Configuration and Functions



**Figure 3-1. CD74AC238 D or PW Package; 16-Pin SOIC or TSSOP (Top View)**



**Figure 3-2. CD74AC238 BQB Package, 16-Pin WQFN (Top View)**

**Table 3-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
C	3	I	Input C
$\overline{G2A}$	4	I	Strobe Input 2A, active low
$\overline{G2B}$	5	I	Strobe Input 2B, active low
G1	6	I	Strobe Input
Y7	7	O	Output 7
GND	8	G	Ground
Y6	9	O	Output 6
Y5	10	O	Output 5
Y4	11	O	Output 4
Y3	12	O	Output 3
Y2	13	O	Output 2
Y1	14	O	Output 1
Y0	15	O	Output 0
V <sub>CC</sub>	16	P	Positive Supply
Thermal Pad <sup>(2)</sup>		—	Thermal Pad

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) BQB package only

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6	V
I <sub>IK</sub> <sup>(2)</sup>	Input clamp current	(V <sub>I</sub> < 0 V or V <sub>I</sub> > V <sub>CC</sub> )		±20 mA
I <sub>OK</sub> <sup>(2)</sup>	Output clamp current	(V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub> )		±50 mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> > 0 V or V <sub>O</sub> < V <sub>CC</sub> )		±50 mA
Continuous current through V <sub>CC</sub> or GND				±200 mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		T <sub>A</sub> = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.5 V	1.2	1.2	1.2	1.2		V
		V <sub>CC</sub> = 3 V	2.1	2.1	2.1			
		V <sub>CC</sub> = 5.5 V	3.85	3.85	3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.5 V		0.3	0.3	0.3		V
		V <sub>CC</sub> = 3 V		0.9	0.9	0.9		
		V <sub>CC</sub> = 5.5 V		1.65	1.65	1.65		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		-24	-24	-24		mA
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		24	24	24		mA
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.5 V to 3 V		50	50	50		ns/V
		V <sub>CC</sub> = 3.6 V to 5.5 V		20	20	20		

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	CD74AC238			UNIT
	BQB (WQFN)	D (SOIC)	PW (TSSOP)	
	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	83.9	106.6	126.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25 °C		-55°C to 125°C		-40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	1.5 V	1.4	1.4	1.4			V	
			3 V	2.9	2.9	2.9				
			4.5 V	4.4	4.4	4.4				
		I <sub>OH</sub> = -4 mA	3 V	2.58	2.4	2.48				
			4.5 V	3.94	3.7	3.8				
			5.5 V		3.85					
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	1.5 V	0.1	0.1	0.1		V		
			3 V	0.1	0.1	0.1				
			4.5 V	0.1	0.1	0.1				
		I <sub>OL</sub> = 12 mA	3 V	0.36	0.5	0.44				
			4.5 V	0.36	0.5	0.44				
			5.5 V		1.65					
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		5.5 V	±0.1	±1	±1		μA		
			I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	8	160	80	μA	
C <sub>i</sub>				10	10	10		pF		

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

## 4.6 Switching Characteristics, V<sub>CC</sub> = 1.5 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 1.5 V, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A, B, C	Any Y	187		170		ns
t <sub>PHL</sub>			187		170		
t <sub>PLH</sub>	G1	Any Y	208		189		ns
t <sub>PHL</sub>			208		189		
t <sub>PLH</sub>	G2A, G2B	Any Y	149		135		ns
t <sub>PHL</sub>			149		135		

#### 4.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A, B, C	Any Y	5.3	21	5.4	19.1	ns
$t_{PHL}$			5.3	21	5.4	19.1	
$t_{PLH}$	G1	Any Y	5.8	23.2	6	21.1	ns
$t_{PHL}$			5.8	23.2	6	21.1	
$t_{PLH}$	$\overline{G}2A, \overline{G}2B$	Any Y	4.2	16.7	4.3	15.2	ns
$t_{PHL}$			4.2	16.7	4.3	15.2	

#### 4.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

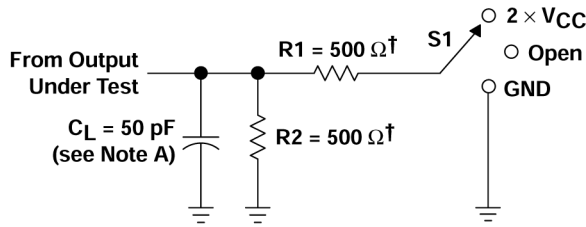
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A, B, C	Any Y	3.8	15	3.9	13.6	ns
$t_{PHL}$			3.8	15	3.9	13.6	
$t_{PLH}$	G1	Any Y	4.2	16.6	4.3	15.1	ns
$t_{PHL}$			4.2	16.6	4.3	15.1	
$t_{PLH}$	G2A, G2B	Any Y	3	11.9	3.1	10.7	ns
$t_{PHL}$			3	11.9	3.1	10.7	

#### 4.9 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

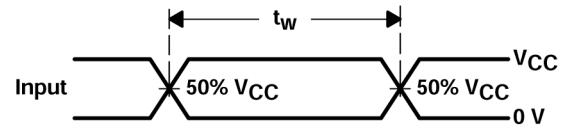
PARAMETER		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	110	pF

## 5 Parameter Measurement Information

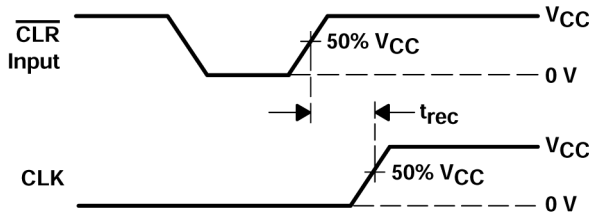


† When  $V_{CC} = 1.5\text{ V}$ ,  $R1 = R2 = 1\text{ k}\Omega$

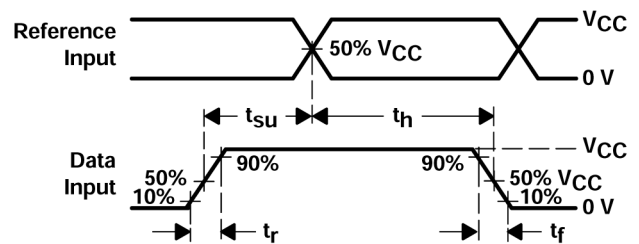
LOAD CIRCUIT



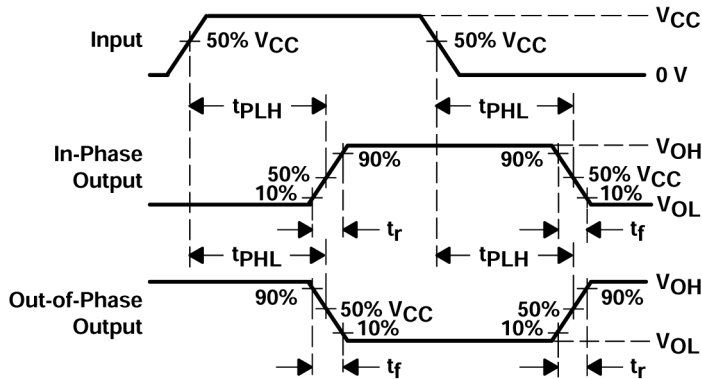
VOLTAGE WAVEFORMS  
PULSE DURATION



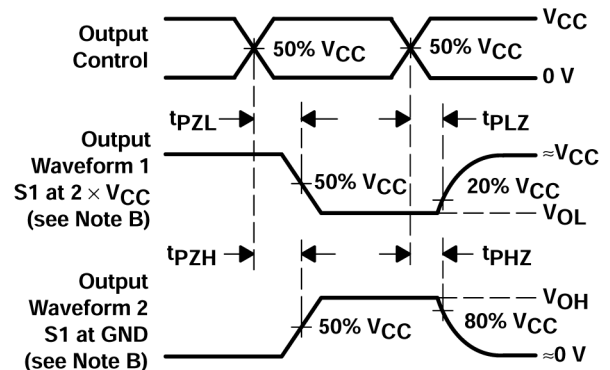
VOLTAGE WAVEFORMS  
RECOVERY TIME



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS  
OUTPUT ENABLE AND DISABLE TIMES

- $C_L$  includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ . Phase relationships between waveforms are arbitrary.
- For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
- $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



## 6 Detailed Description

### 6.1 Overview

When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications (see Application Information).

### 6.2 Functional Block Diagram

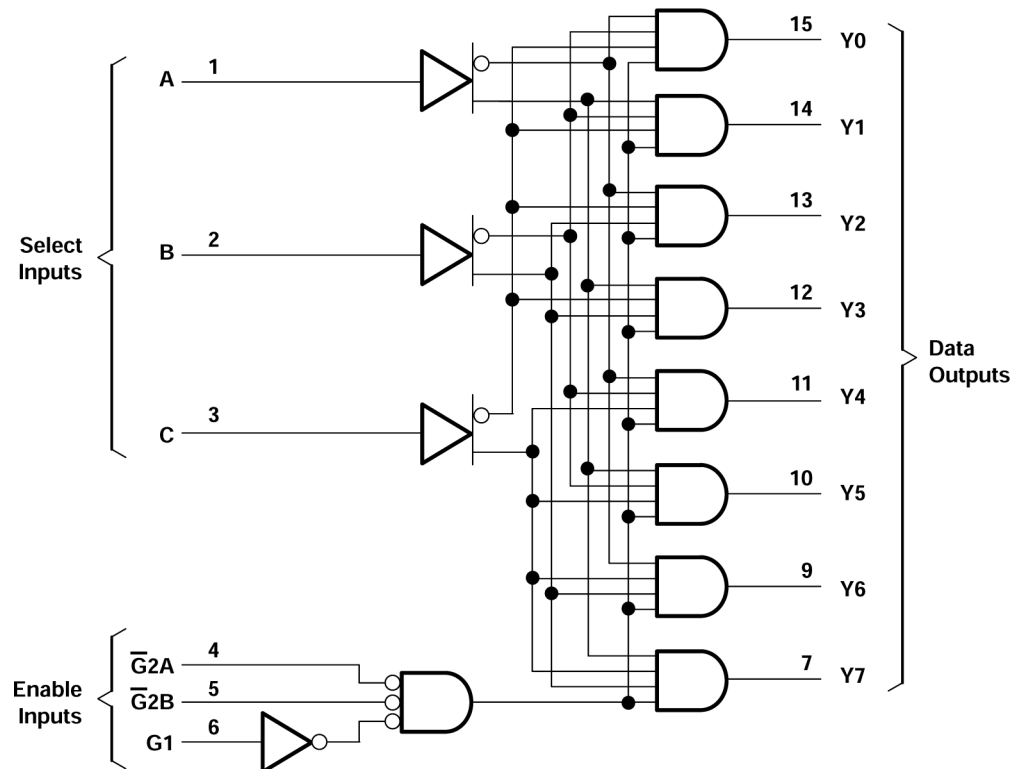


Figure 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

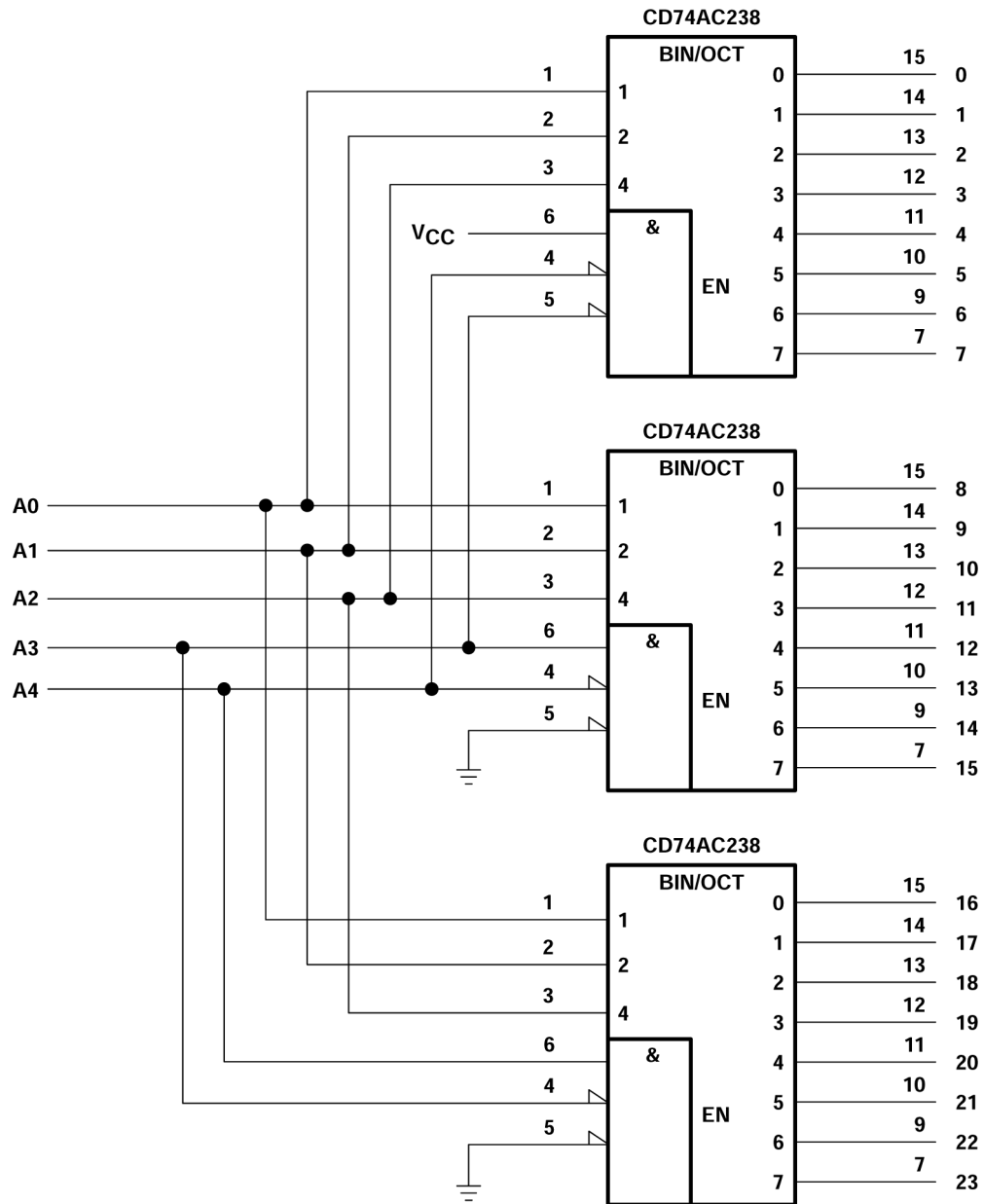
Table 6-1. Function Table

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L

**Table 6-1. Function Table (continued)**

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

## 7 Application Information



**Figure 7-1. 24-Bit Decoding Scheme**

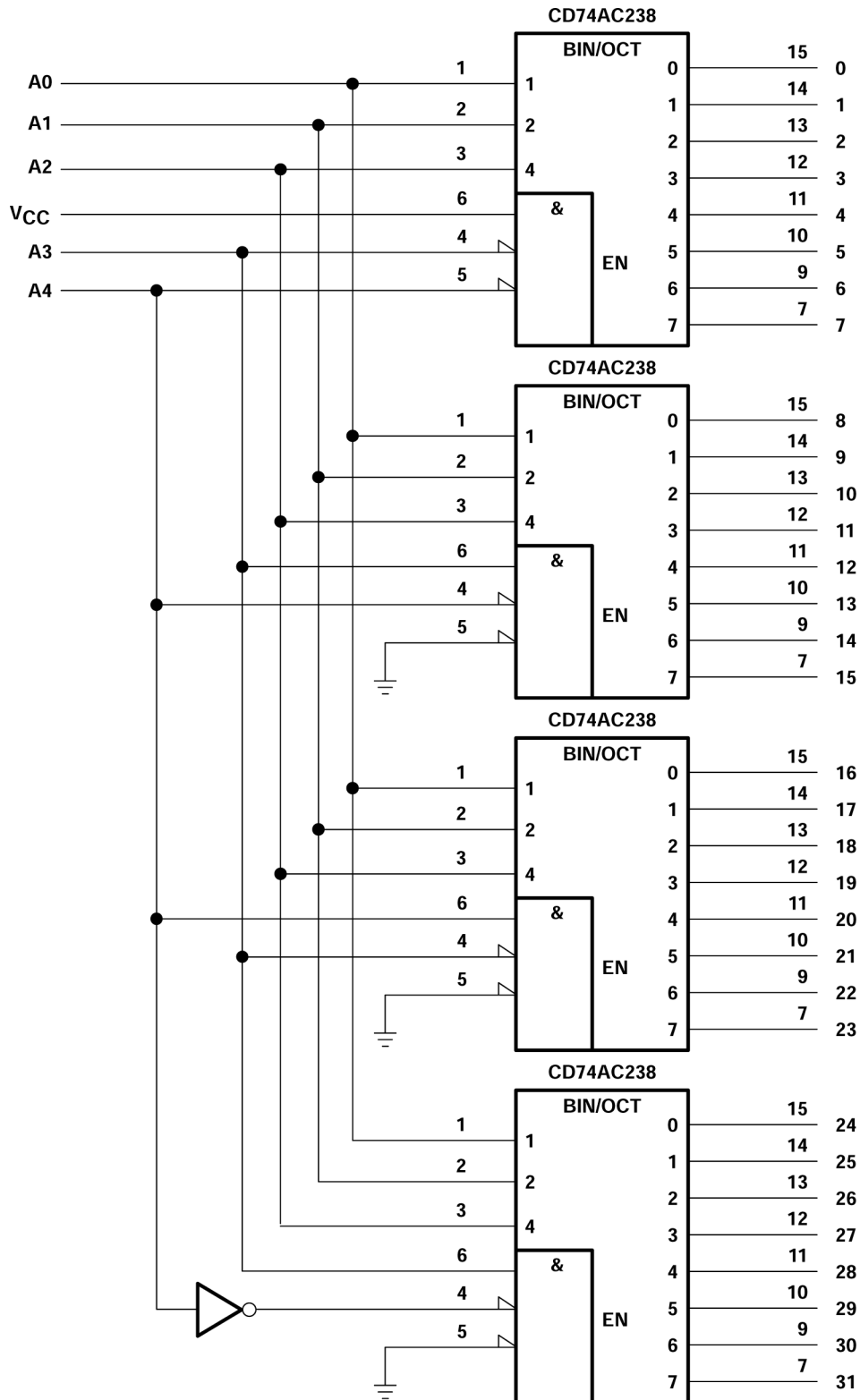


Figure 7-2. 32-Bit Decoding Scheme

## 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu\text{F}$  and  $1\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 7.2 Layout

### 7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 7.2.2 Layout Example

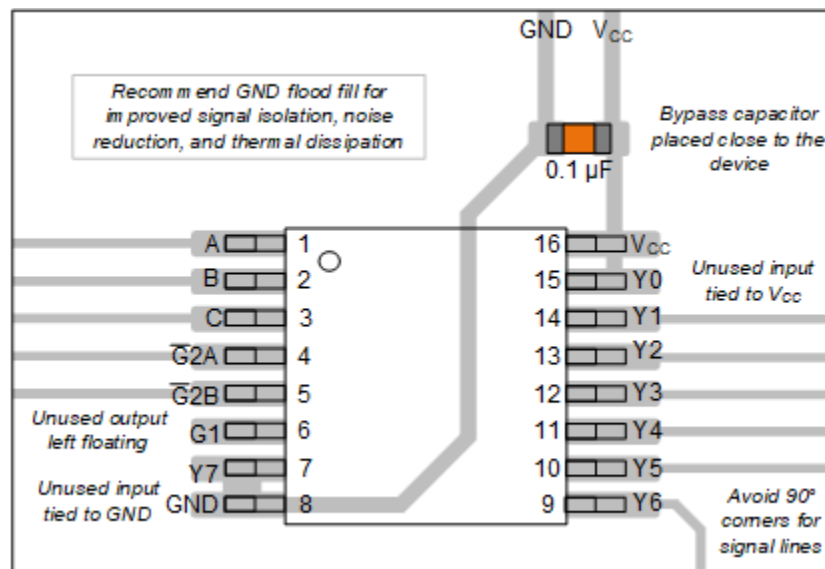


Figure 7-3. Example Layout for the CD74AC238

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC238	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

Changes from Revision A (April 2024) to Revision B (July 2024)	Page
• Added BQB and PW packages to <i>Package Information</i> table, <i>Pin Configuration and Functions</i> section, and <i>Thermal Information</i> table.....	1
• Changed M package to D package throughout data sheet.....	1

Changes from Revision * (February 2003) to Revision A (April 2024)	Page
• Added <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , Application and Implementation section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Updated RθJA values: M = 73 to 106.6, all values in °C/W .....	5

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC238BQBR	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC238	<a href="#">Samples</a>
CD74AC238M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC238M	<a href="#">Samples</a>
CD74AC238PWR	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	AC238	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC238BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
CD74AC238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74AC238PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC238BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
CD74AC238M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74AC238PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## GENERIC PACKAGE VIEW

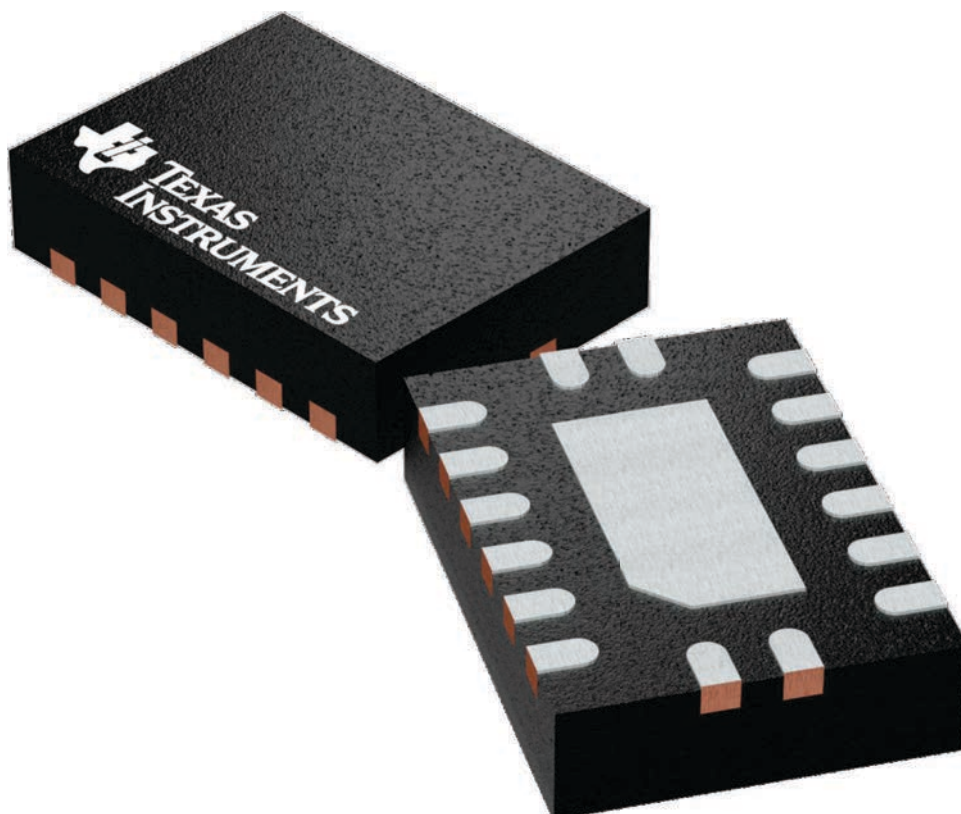
**BQB 16**

**WQFN - 0.8 mm max height**

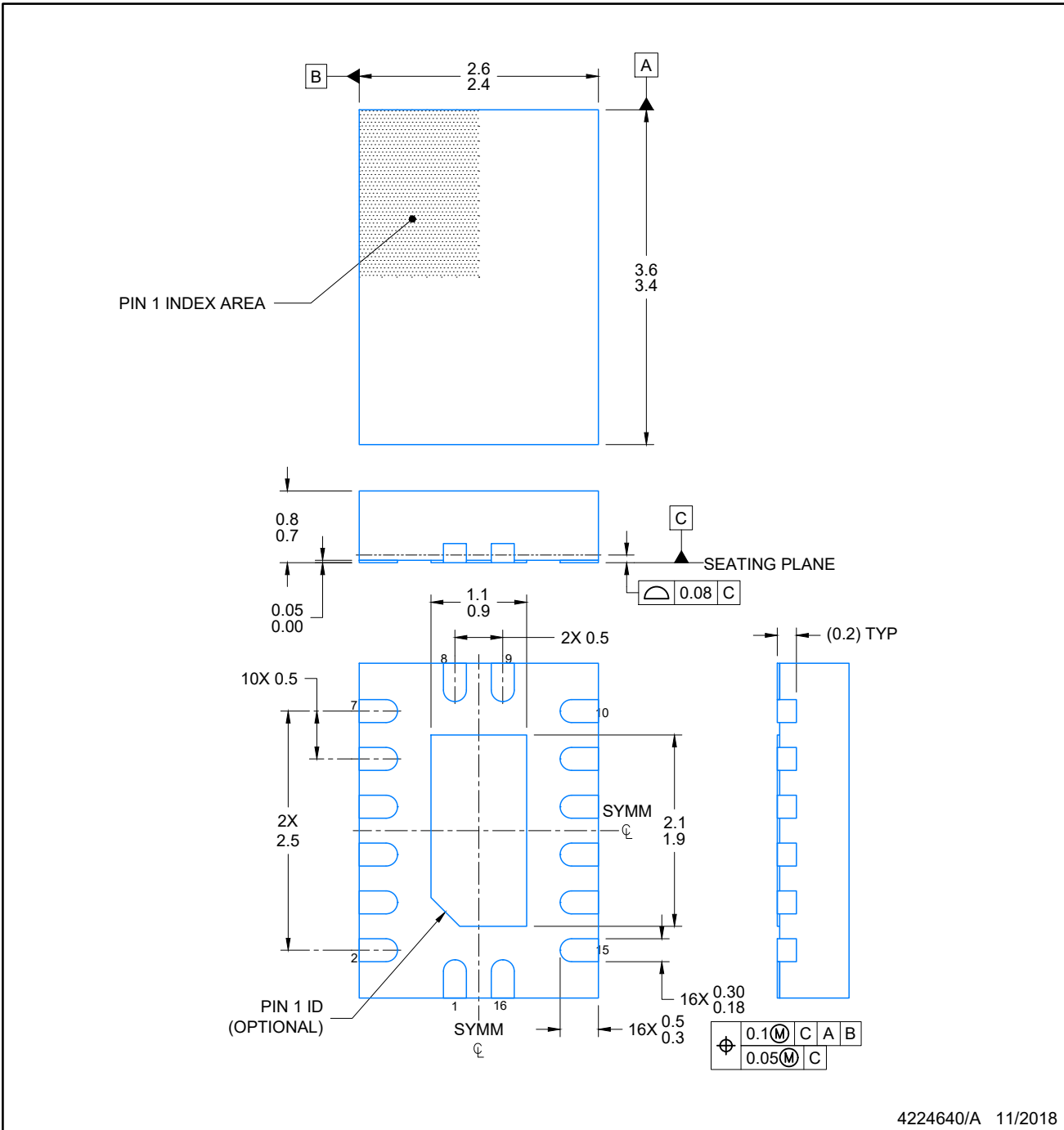
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226161/A



NOTES:

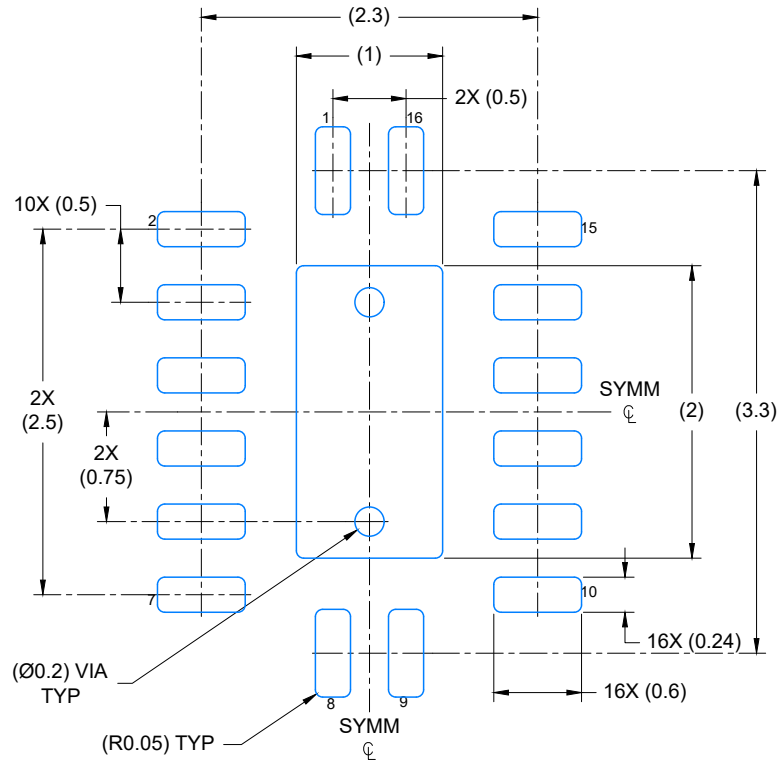
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

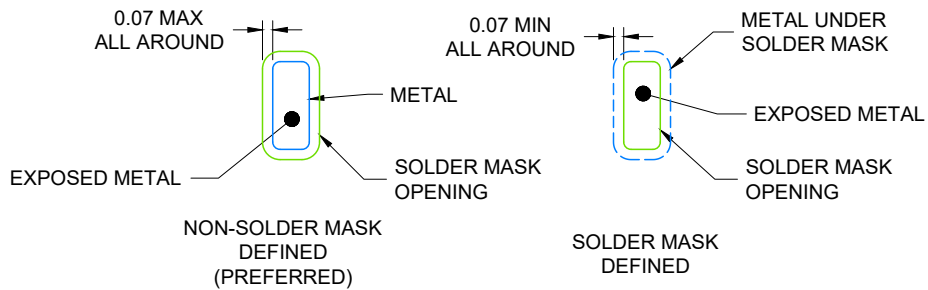
WQFN - 0.8 mm max height

BQB0016A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

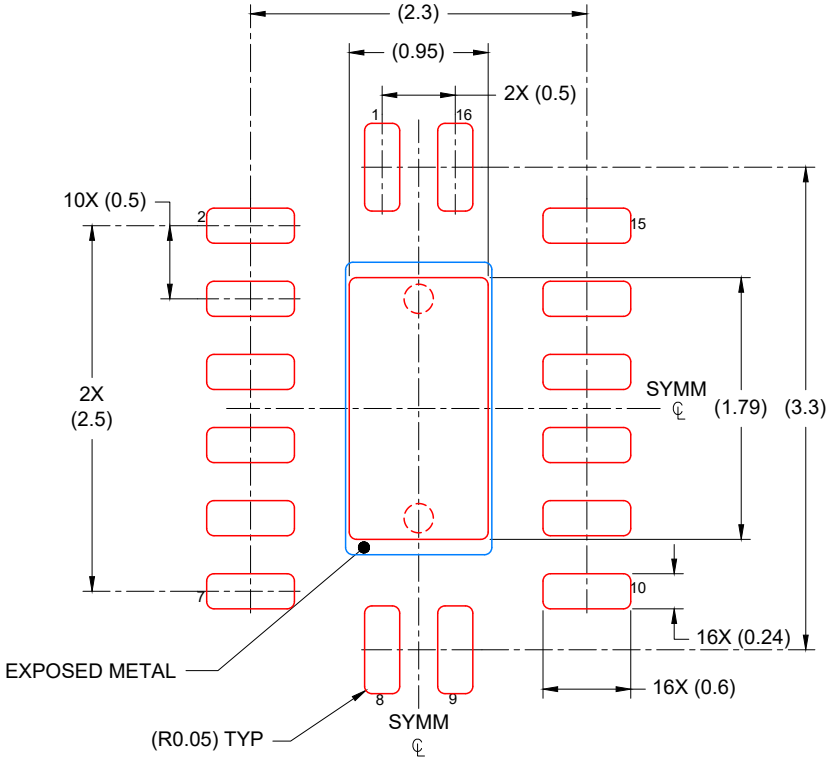
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**EXAMPLE STENCIL DESIGN**

**BQB0016A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 85% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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