

# CSD18533KCS 60V N-Channel NexFET™ Power MOSFET

## 1 Features

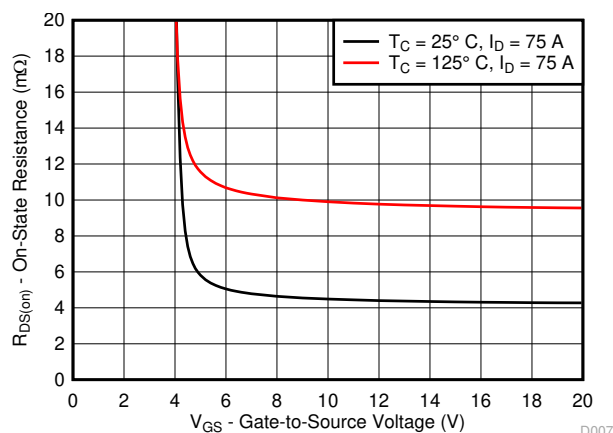
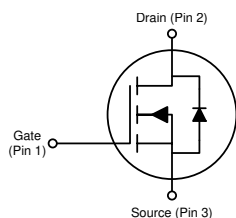
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Low thermal resistance
- Avalanche rated
- Logic level
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- TO-220 plastic package

## 2 Applications

- DC-DC conversion
- Secondary side synchronous rectifier
- Motor control

## 3 Description

This 60V, 5.0mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



**$R_{DS(on)}$  vs  $V_{GS}$**

## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-source voltage	60		V
$Q_g$	Gate charge total (10V)	28		nC
$Q_{gd}$	Gate charge gate-to-drain	3.9		nC
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{V}$	6.9	mΩ
		$V_{GS} = 10\text{V}$	5.0	mΩ
$V_{GS(th)}$	Threshold voltage	1.9		V

## Ordering Information<sup>(1)</sup>

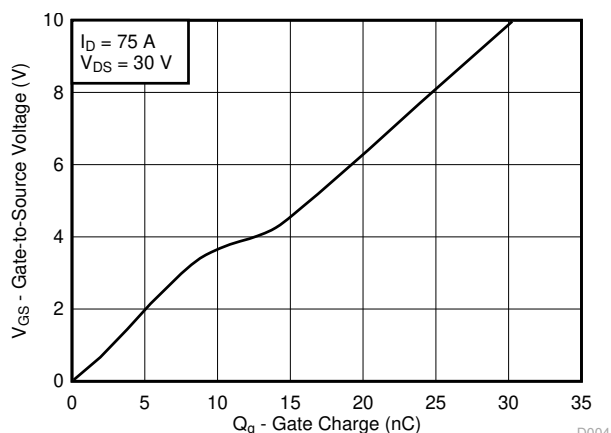
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18533KCS	50	Tube	TO-220 Plastic Package	Tube

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-source voltage	60	V
$V_{GS}$	Gate-to-source voltage	±20	V
$I_D$	Continuous drain current (package limited)	100	A
	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	118	
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	84	
$I_{DM}$	Pulsed drain current <sup>(1)</sup>	294	A
$P_D$	Power dissipation	192	W
$T_J$ , $T_{stg}$	Operating junction, Storage temperature	-55 to 175	°C
$E_{AS}$	Avalanche energy, single pulse $I_D = 52\text{A}$ , $L = 0.1\text{mH}$ , $R_G = 25\Omega$	135	mJ

- (1) Max  $R_{\theta JC} = 0.8^\circ\text{C/W}$ , pulse duration  $\leq 100\mu\text{s}$ , duty cycle  $\leq 1\%$



**Gate Charge**



## Table of Contents

<b>1 Features</b> .....	1	5.1 Third-Party Products Disclaimer.....	7
<b>2 Applications</b> .....	1	5.2 Receiving Notification of Documentation Updates.....	7
<b>3 Description</b> .....	1	5.3 Support Resources.....	7
<b>4 Specifications</b> .....	3	5.4 Trademarks.....	7
4.1 Electrical Characteristics.....	3	5.5 Electrostatic Discharge Caution.....	7
4.2 Thermal Information.....	3	5.6 Glossary.....	7
4.3 Typical MOSFET Characteristics.....	4	<b>6 Revision History</b> .....	8
<b>5 Device and Documentation Support</b> .....	7	<b>7 Mechanical, Packaging, and Orderable Information</b> ....	9

---

## 4 Specifications

### 4.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0V, I_D = 250\mu A$	60			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0V, V_{DS} = 48V$			1	$\mu A$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0V, V_{GS} = 20V$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.5	1.9	2.3	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5V, I_D = 75A$		6.9	9.0	m $\Omega$
		$V_{GS} = 10V, I_D = 75A$		5.0	6.3	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 30V, I_D = 75A$		150		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0V, V_{DS} = 30V, f = 1MHz$		2420	3025	pF
$C_{oss}$	Output capacitance			300	375	pF
$C_{rss}$	Reverse transfer capacitance			7	9.1	pF
$R_G$	Series gate resistance			1.4	2.8	$\Omega$
$Q_g$	Gate charge total (4.5V)	$V_{DS} = 30V, I_D = 75A$		14	17	nC
$Q_g$	Gate charge total (10V)			28	34	nC
$Q_{gd}$	Gate charge gate-to-drain			3.9		nC
$Q_{gs}$	Gate charge gate-to-source			9.4		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			4.6		nC
$Q_{oss}$	Output charge		$V_{DS} = 30V, V_{GS} = 0V$		31	
$t_{d(on)}$	Turn on delay time	$V_{DS} = 30V, V_{GS} = 10V,$ $I_{DS} = 75A, R_G = 0\Omega$		5.7		ns
$t_r$	Rise time			4.8		ns
$t_{d(off)}$	Turn off delay time			13		ns
$t_f$	Fall time			3.2		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 75A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 30V, I_F = 75A,$ $di/dt = 300A/\mu s$		97		nC
$t_{rr}$	Reverse recovery time			49		ns

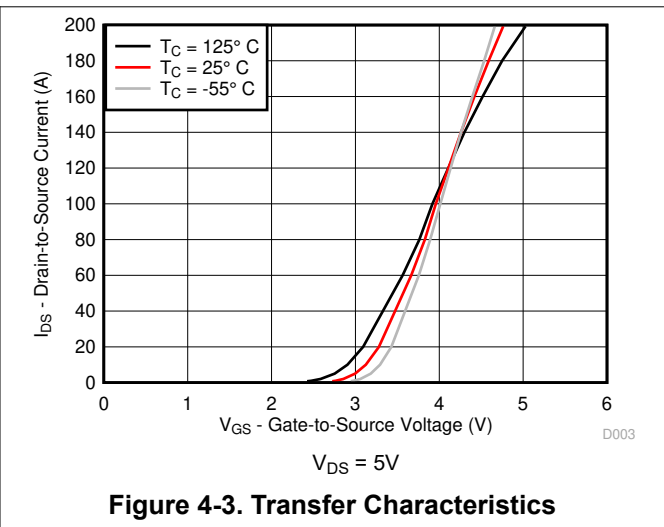
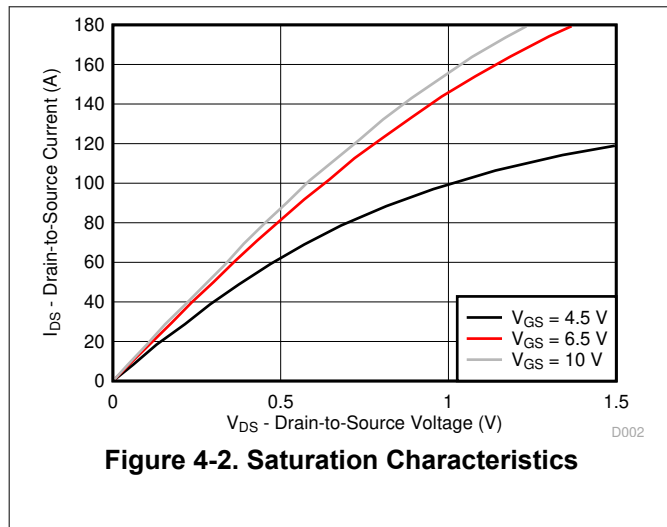
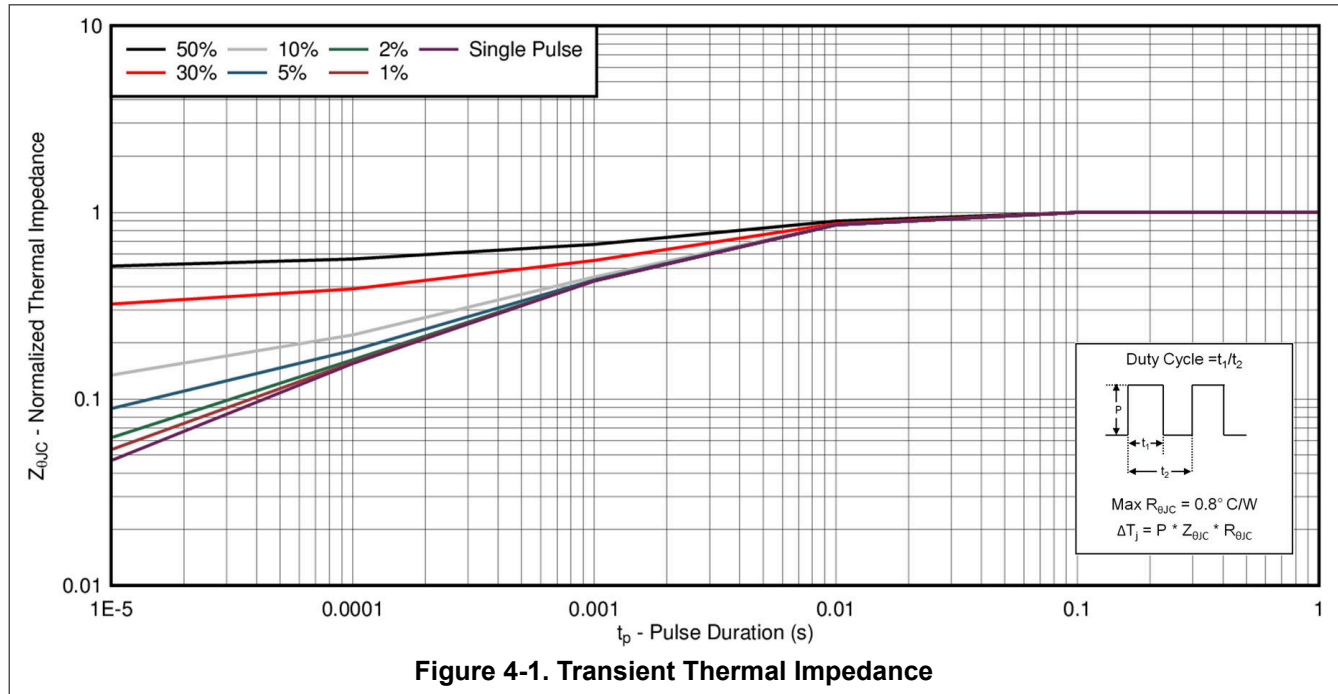
### 4.2 Thermal Information

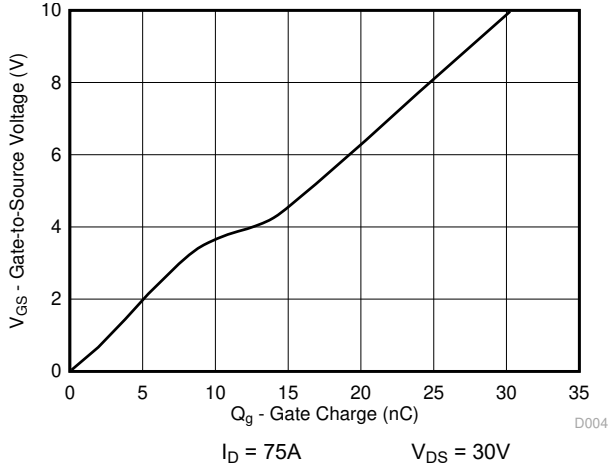
( $T_A = 25^\circ\text{C}$  unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C}/\text{W}$

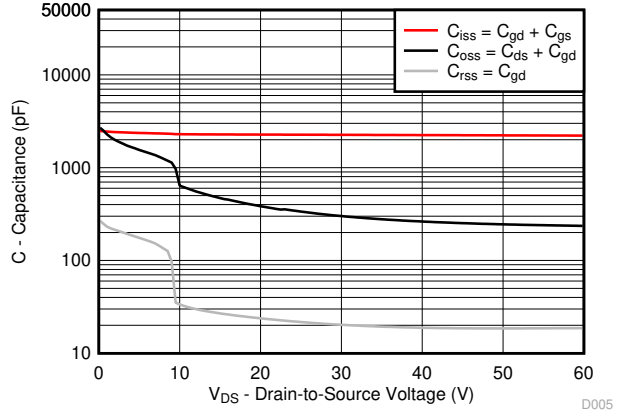
### 4.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

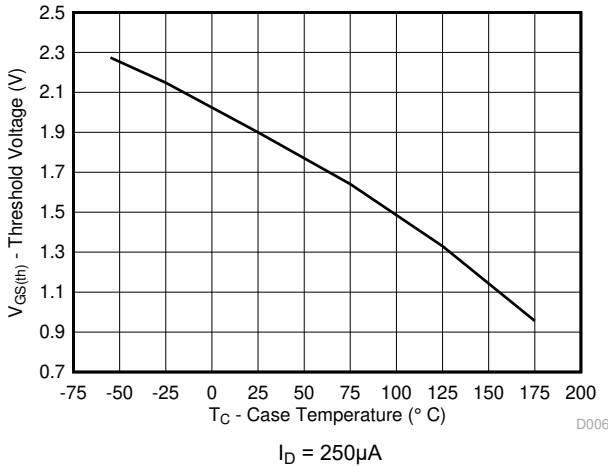




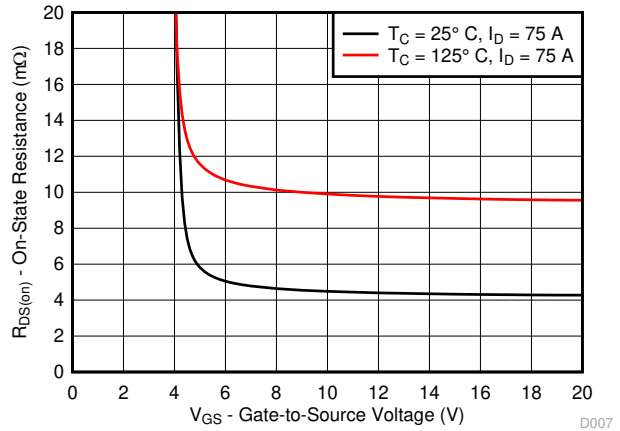
**Figure 4-4. Gate Charge**



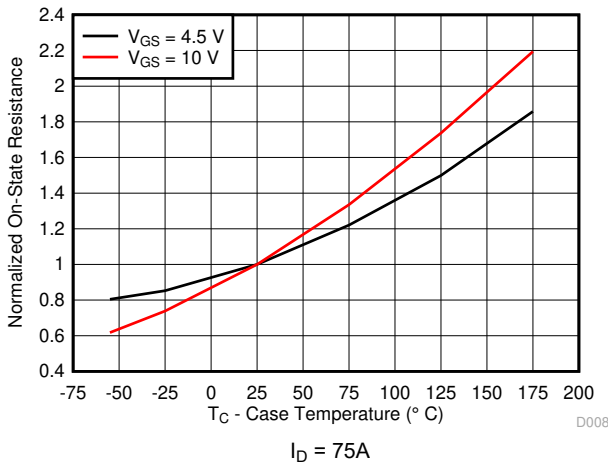
**Figure 4-5. Capacitance**



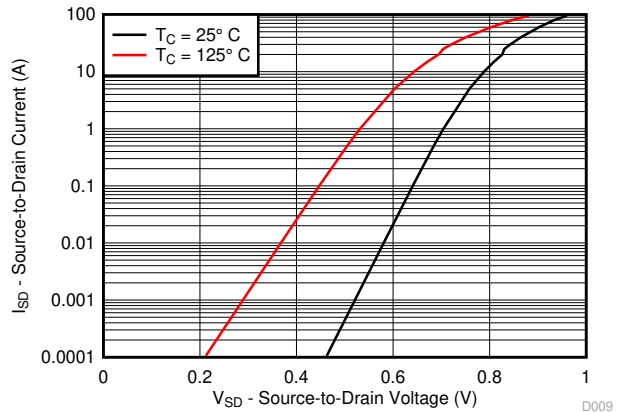
**Figure 4-6. Threshold Voltage vs Temperature**



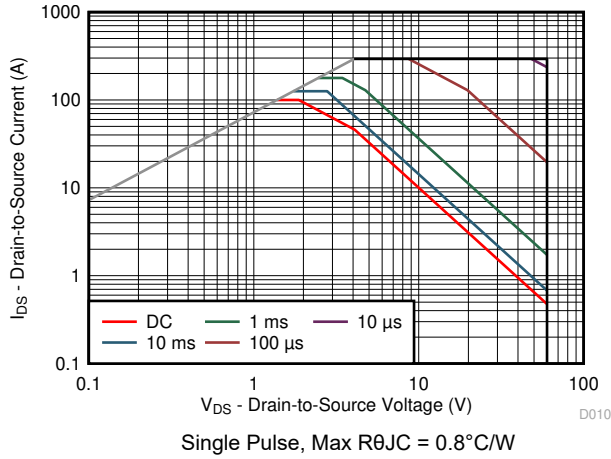
**Figure 4-7. On-State Resistance vs Gate-to-Source Voltage**



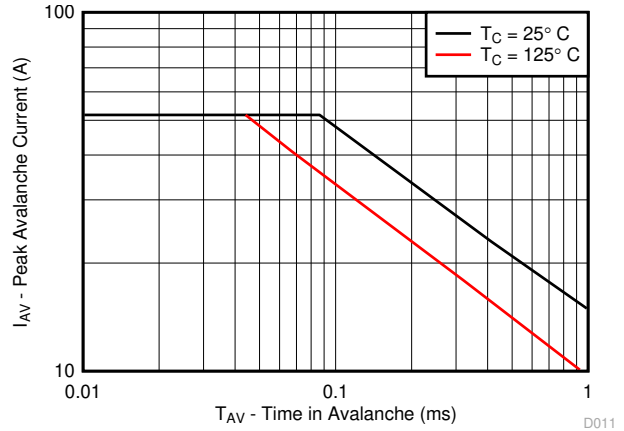
**Figure 4-8. Normalized On-State Resistance vs Temperature**



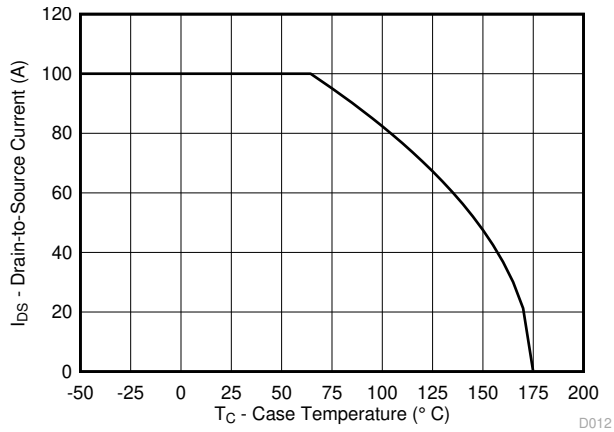
**Figure 4-9. Typical Diode Forward Voltage**



**Figure 4-10. Maximum Safe Operating Area**



**Figure 4-11. Single Pulse Unclamped Inductive Switching**



**Figure 4-12. Maximum Drain Current vs Temperature**

## 5 Device and Documentation Support

### 5.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 5.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 5.4 Trademarks

NexFET™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 5.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 5.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

---

### Changes from Revision C (June 2015) to Revision D (March 2024) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- 

### Changes from Revision B (April 2014) to Revision C (June 2015) Page

- Updated Pulsed Drain Current ..... 1
  - Updated pulsed current conditions ..... 1
  - Updated [Figure 4-1](#) .....4
  - Updated SOA in [Figure 4-10](#) ..... 4
- 

### Changes from Revision A (January 2013) to Revision B (April 2014) Page

- Updated document title to include part number ..... 1
  - Updated part description ..... 1
  - Increased currents to reflect increase in max temperature ..... 1
  - Increased max power to reflect increase in max temperature ..... 1
  - Increased max temperature to 175°C ..... 1
  - Updated [Figure 4-6](#) to extend to 175°C .....4
  - Updated [Figure 4-8](#) to extend to 175°C .....4
  - Updated [Figure 4-12](#) to extend to 175°C .....4
- 

### Changes from Revision \* (September 2012) to Revision A (January 2013) Page

- Changed  $Q_{g(th)}$ , Gate Charge at  $V_{th}$  value From: 7.3 To: 4.6..... 3
-



## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18533KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD18533KCS	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CSD18533KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD18533KCS	KCS	TO-220	3	50	532	34.1	700	9.6



# EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE:15X

4222214/B 08/2018

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated