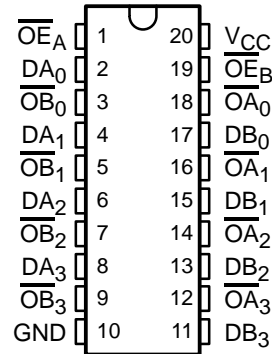


CY54FCT240T, CY74FCT240T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

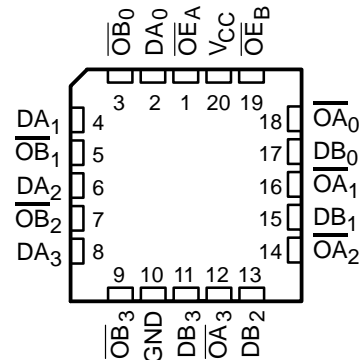
SCCS017A – MAY 1994 – REVISED OCTOBER 2001

- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT240T
 - 48-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT240T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

CY54FCT240T . . . D PACKAGE
CY74FCT240T . . . Q OR SO PACKAGE
(TOP VIEW)



CY54FCT240T . . . L PACKAGE
(TOP VIEW)



description

The 'FCT240T devices are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts, while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT240T, CY74FCT240T
8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

SCCS017A – MAY 1994 – REVISED OCTOBER 2001

ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – SO	Tube	4.3	CY74FCT240CTSOC	FCT240C
		Tape and reel	4.3	CY74FCT240CTSUCT	
	QSOP – Q	Tape and reel	4.3	CY74FCT240CTQCT	FCT240C
	SOIC – SO	Tube	4.8	CY74FCT240ATSOC	FCT240A
		Tape and reel	4.8	CY74FCT240ATSUCT	
	QSOP – Q	Tape and reel	4.8	CY74FCT240ATQCT	FCT240A
	SOIC – SO	Tube	8	CY74FCT240TSOC	FCT240
Tape and reel		8	CY74FCT240TSUCT		
QSOP – Q	Tape and reel	8	CY74FCT240TQCT	FCT240	
-55°C to 125°C	CDIP – D	Tube	4.7	CY54FCT240CTDMB	
	CDIP – D	Tube	5.1	CY54FCT240ATDMB	
	LCC – L	Tube	5.1	CY54FCT240ATLMB	
	CDIP – D	Tube	9	CY54FCT240TDMB	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

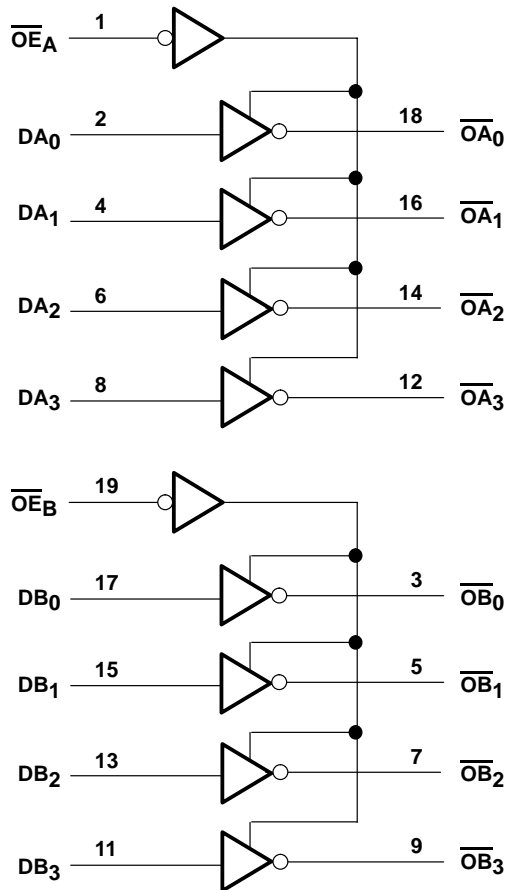
FUNCTION TABLE

INPUTS			OUTPUT O
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	H
L	L	H	L
H	H	X	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state



logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	-0.5 V to 7 V
DC input voltage range	-0.5 V to 7 V
DC output voltage range	-0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, T_A	-65°C to 135°C
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

CY54FCT240T, CY74FCT240T
8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

SCCS017A – MAY 1994 – REVISED OCTOBER 2001

recommended operating conditions (see Note 2)

	CY54FCT240T			CY74FCT240T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-12			-32	mA
I _{OL} Low-level output current			48			64	mA
T _A Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



CY54FCT240T, CY74FCT240T
8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

SCCS017A – MAY 1994 – REVISED OCTOBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT240T		CY74FCT240T		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
V _{IK}	V _{CC} = 4.5 V, I _{IN} = -18 mA	-0.7	-1.2			V	
	V _{CC} = 4.75 V, I _{IN} = -18 mA				-0.7 -1.2		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.3			V	
	V _{CC} = 4.75 V	I _{OH} = -32 mA			2		
		I _{OH} = -15 mA			2.4		3.3
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA	0.3	0.55			V	
	V _{CC} = 4.75 V, I _{OL} = 64 mA				0.3 0.55		
V _{hys}	All inputs	0.2			0.2	V	
I _I	V _{CC} = 5.5 V, V _{IN} = V _{CC}			5		μA	
	V _{CC} = 5.25 V, V _{IN} = V _{CC}				5		
I _{IH}	V _{CC} = 5.5 V, V _{IN} = 2.7 V			±1		μA	
	V _{CC} = 5.25 V, V _{IN} = 2.7 V				±1		
I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V			±1		μA	
	V _{CC} = 5.25 V, V _{IN} = 0.5 V				±1		
I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 2.7 V			10		μA	
	V _{CC} = 5.25 V, V _{OUT} = 2.7 V				10		
I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = 0.5 V			-10		μA	
	V _{CC} = 5.25 V, V _{OUT} = 0.5 V				-10		
I _{OS} ‡	V _{CC} = 5.5 V, V _{OUT} = 0 V	-60	-120	-225		mA	
	V _{CC} = 5.25 V, V _{OUT} = 0 V				-60 -120 -225		
I _{off}	V _{CC} = 0 V, V _{OUT} = 4.5 V			±1		μA	
I _{CC}	V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V	0.1	0.2			mA	
	V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V				0.1 0.2		
ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open	0.5	2			mA	
	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open				0.5 2		
I _{CCD} ¶	V _{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	0.06	0.12			mA/ MHz	
	V _{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V				0.06 0.12		

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



CY54FCT240T, CY74FCT240T
8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

SCCS017A – MAY 1994 – REVISED OCTOBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS		CY54FCT240T		CY74FCT240T		UNIT		
			MIN	TYP†	MAX	MIN		TYP†	MAX
I _C #	V _{CC} = 5.5 V, Outputs open, OE _A = OE _B = GND	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	0.7	1.4		mA		
			V _{IN} = 3.4 V or GND	1	2.4				
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} = 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	1.3	2.6				
			V _{IN} = 3.4 V or GND	3.3	10.6				
	V _{CC} = 5.25 V, Outputs open, OE _A = OE _B = GND	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V			0.7		1.4	
			V _{IN} = 3.4 V or GND			1		2.4	
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} = 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V			1.3	2.6		
			V _{IN} = 3.4 V or GND			3.3	10.6		
C _i				5	10		5	10	pF
C _o				9	12		9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



CY54FCT240T, CY74FCT240T
8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

SCCS017A – MAY 1994 – REVISED OCTOBER 2001

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT240T		CY54FCT240AT		CY54FCT240CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	\bar{O}	1.5	9	1.5	5.1	1.5	4.7	ns
t _{PHL}			1.5	9	1.5	5.1	1.5	4.7	
t _{PZH}	\overline{OE}	\bar{O}	1.5	10.5	1.5	6.5	1.5	5.7	ns
t _{PZL}			1.5	10.5	1.5	6.5	1.5	5.7	
t _{PHZ}	\overline{OE}	\bar{O}	1.5	10	1.5	5.9	1.5	4.6	ns
t _{PLZ}			1.5	10	1.5	5.9	1.5	4.6	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT240T		CY74FCT240AT		CY74FCT240CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	\bar{O}	1.5	8	1.5	4.8	1.5	4.3	ns
t _{PHL}			1.5	8	1.5	4.8	1.5	4.3	
t _{PZH}	\overline{OE}	\bar{O}	1.5	10	1.5	6.2	1.5	5	ns
t _{PZL}			1.5	10	1.5	6.2	1.5	5	
t _{PHZ}	\overline{OE}	\bar{O}	1.5	9.5	1.5	5.6	1.5	4.5	ns
t _{PLZ}			1.5	9.5	1.5	5.6	1.5	4.5	



CY54FCT240T, CY74FCT240T
8-BIT BUFFERS/LINE DRIVERS
WITH 3-STATE OUTPUTS

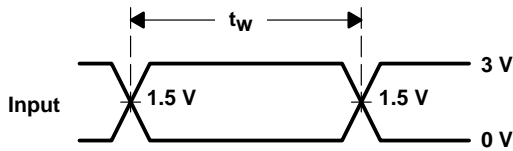
SCCS017A – MAY 1994 – REVISED OCTOBER 2001

PARAMETER MEASUREMENT INFORMATION

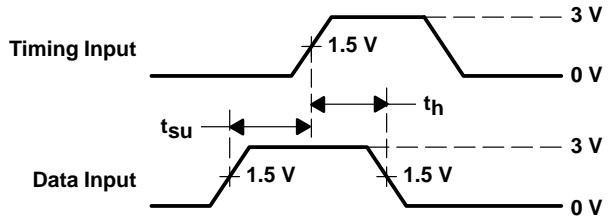


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

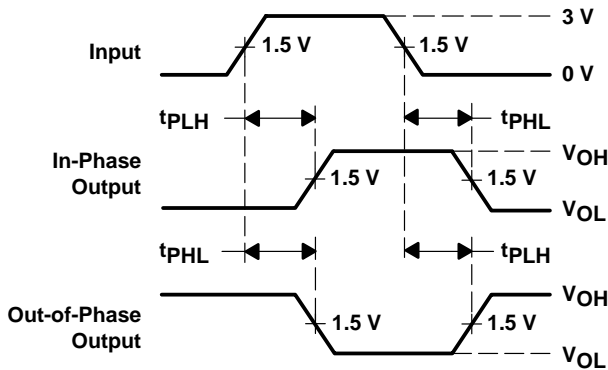
LOAD CIRCUIT FOR 3-STATE OUTPUTS



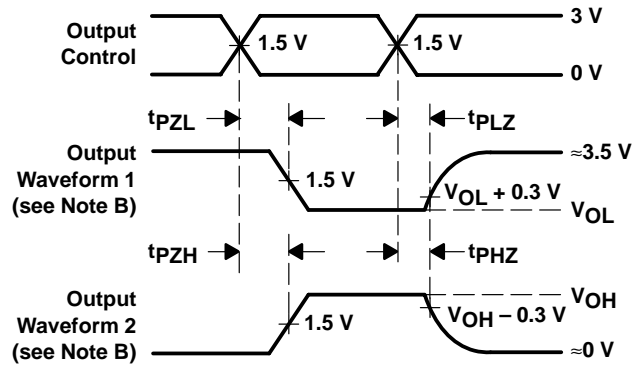
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9220301M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9220301M2A CY54FCT 244TLMB	Samples
5962-9220301MRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220301MR A CY54FCT244TDMB	Samples
5962-9220301MSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220301MS A CY54FCT244TW	Samples
5962-9220302M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9220302M2A CY54FCT 244ATLMB	Samples
5962-9220302MRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220302MR A CY54FCT244ATDM B	Samples
5962-9220302MSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220302MS A CY54FCT244ATW	Samples
5962-9220303M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9220303M2A	Samples
5962-9220303MRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220303MR A CY54FCT244CTDM B	Samples
5962-9221301MRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9221301MR A	Samples
5962-9221303M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9221303M2A CY54FCT 240ATLMB	Samples
5962-9221303MRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9221303MR A CY54FCT240ATDM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										B	
5962-9221305MRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9221305MR A	Samples
CY54FCT240ATDMB	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9221303MR A CY54FCT240ATDM B	Samples
CY54FCT240ATLMB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9221303M2A CY54FCT 240ATLMB	Samples
CY54FCT244ATDMB	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220302MR A CY54FCT244ATDM B	Samples
CY54FCT244ATLMB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9220302M2A CY54FCT 244ATLMB	Samples
CY54FCT244ATW	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220302MS A CY54FCT244ATW	Samples
CY54FCT244CTDMB	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220303MR A CY54FCT244CTDM B	Samples
CY54FCT244TDMB	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220301MR A CY54FCT244TDMB	Samples
CY54FCT244TLMB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9220301M2A CY54FCT 244TLMB	Samples
CY54FCT244TW	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9220301MS A CY54FCT244TW	Samples
CY74FCT240ATQCT	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT240A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT240ATSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240A	Samples
CY74FCT240ATSOCT	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240A	Samples
CY74FCT240TQCT	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT240	Samples
CY74FCT240TSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240	Samples
CY74FCT240TSOCT	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT240	Samples
CY74FCT244ATPC	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	CY74FCT244ATPC	Samples
CY74FCT244ATQCT	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244A	Samples
CY74FCT244ATQCTE4	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244A	Samples
CY74FCT244ATSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A	Samples
CY74FCT244ATSOCT	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244A	Samples
CY74FCT244CTQCT	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244C	Samples
CY74FCT244CTSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244C	Samples
CY74FCT244DTSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D	Samples
CY74FCT244DTSOCT	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244D	Samples
CY74FCT244TQCT	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT244	Samples
CY74FCT244TSOC	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244	Samples
CY74FCT244TSOCT	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT244	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT240ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT240ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT240TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT240TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT244ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT244CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244DTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT244TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT244TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT240ATQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT240ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT240TQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT240TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT244ATQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT244ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT244CTQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT244DTSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT244TQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT244TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9220301M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9220301MSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-9220302M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9220302MSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-9220303M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9221303M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT240ATLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT244ATLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT244ATW	W	CFP	20	25	506.98	26.16	6220	NA
CY54FCT244TLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT244TW	W	CFP	20	25	506.98	26.16	6220	NA
CY74FCT240ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT240TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244ATPC	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT244ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244DTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT244TSOC	DW	SOIC	20	25	507	12.83	5080	6.6

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated