INA332
INA2332

SBOS216B – SEPTEMBER 2001 - REVISED OCTOBER 2006

Low-Power, Single-Supply, CMOS INSTRUMENTATION AMPLIFIERS

FEATURES

- DESIGNED FOR LOW COST
- HIGH GAIN ACCURACY: G = 5, 0.07%, 2ppm/°C
- GAIN SET WITH EXT. RESISTORS FOR > 5V/V
- HIGH CMRR: 73dB DC, 50dB at 45kHz
- LOW BIAS CURRENT: 0.5pA
- BANDWIDTH, SLEW RATE: 2.0MHz, 5V/μs
- RAIL-TO-RAIL OUTPUT SWING: (V+) – 0.02V
- WIDE TEMPERATURE RANGE: –55°C to +125°C
- LOW QUIESCENT CURRENT: 490μA max/chan
- SHUTDOWN: 0.01μA
- MSOP-8 SINGLE AND TSSOP-14 DUAL PACKAGES

APPLICATIONS

- INDUSTRIAL SENSOR AMPLIFIERS: Bridge, RTD, Thermocouple, Position
- PHYSIOLOGICAL AMPLIFIERS: ECG, EEG, EMG
- A/D CONVERTER SIGNAL CONDITIONING
- DIFFERENTIAL LINE RECEIVERS WITH GAIN
- FIELD UTILITY METERS
- PCMCIA CARDS
- AUDIO AMPLIFIERS
- COMMUNICATION SYSTEMS
- TEST EQUIPMENT
- AUTOMOTIVE INSTRUMENTATION

DESCRIPTION

The INA332 and INA2332 are rail-to-rail output, low-power CMOS instrumentation amplifiers that offer wide range, single-supply, and bipolar-supply operation. Using a special manufacturing flow, the INA332 family provides the lowest cost available, while still achieving low-noise amplification of differential signals with low quiescent current of 415μA (dropping to 0.01μA when shut down). Returning to normal operation within microseconds, this INA can be used for battery or multichannel applications.

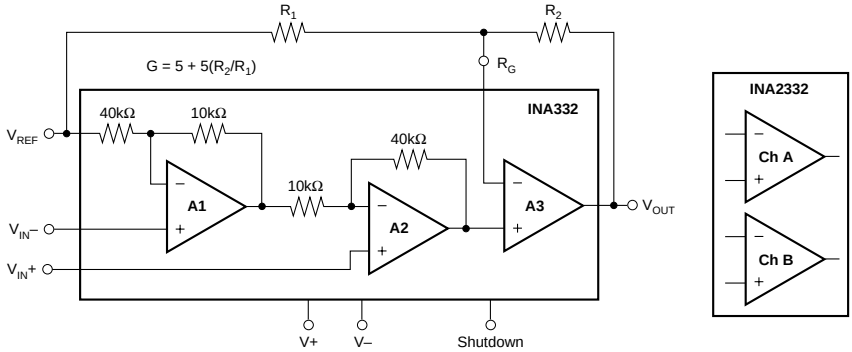
Configured internally in a gain of 5V/V, the INA332 offers flexibility in higher gains by choosing external resistors.

The INA332 rejects line noise and its harmonics because common-mode error remains low even at higher frequencies.

High bandwidth and slew rate make the INA332 ideal for directly driving sampling Analog-to-Digital (A/D) converters as well as general-purpose applications.

With high precision, low cost, and small packages, the INA332 outperforms discrete designs.

Additionally, because they are specified for a wide temperature range of –55°C to +125°C, the INA332 family can be used in demanding environments.



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	7.5V
Signal Input Terminals, Voltage[2]	(V–) – 0.5V to (V+) + 0.5V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

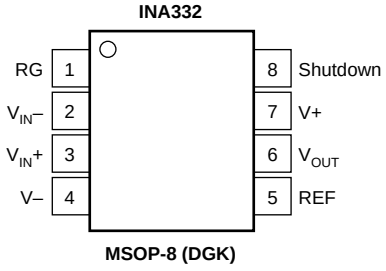
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	TEMPERATURE RANGE	SPECIFIED PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Single						
INA332AIDGK	MSOP-8	DGK	–55°C to +125°C	B32	INA332AIDGKT	Tape and Reel, 250
"	"	"	"	"	INA332AIDGKR	Tape and Reel, 2500
Dual						
INA2332AIPW	TSSOP-14	PW	–55°C to +125°C	2332A	INA2332AIPWT	Tape and Reel, 250
"	"	"	"	"	INA2332AIPWR	Tape and Reel, 2500

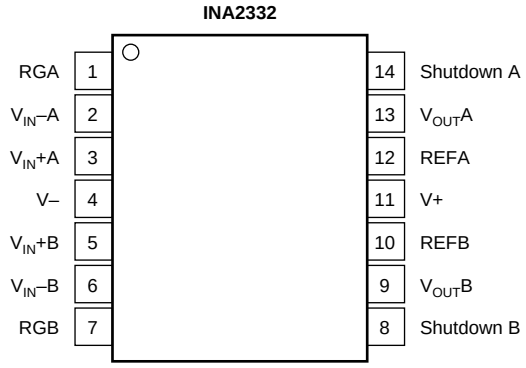
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View



MSOP-8 (DGK)



Dual, TSSOP-14 (PW)

ELECTRICAL CHARACTERISTICS: V_S = +2.7V TO +5.5V

BOLDFACE limits apply over the specified temperature range, **T_A = –55°C TO +125°C**

At T_A = +25°C, R_L = 10kΩ, G = 25, and V_{CM} = V_S/2, unless otherwise noted.

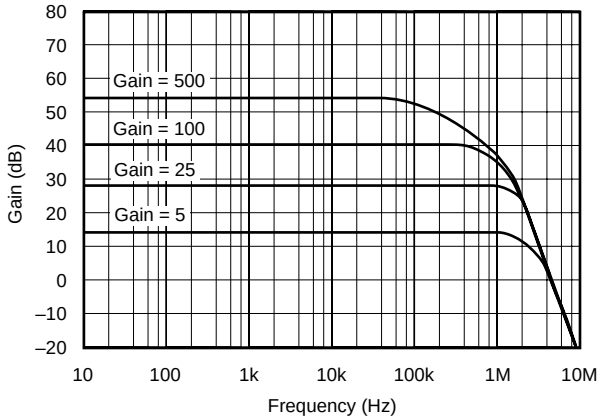
PARAMETER		CONDITION	INA332AIDGK INA2332AIPW MIN	TYP	MAX	UNITS
INPUT						
Input Offset Voltage, RTI		V_S = +5V		±2	±8	mV
Over Temperature	**V_{OS}**				**±9**	**mV**
Temperature Coefficient	**dV_{OS}/dT**			**±5**		**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +5.5V		±50	±250	µV/V
Over Temperature					**±260**	**µV/V**
Long-Term Stability				±0.4		µV/month
Input Impedance				10^{13} || 3		Ω || pF
Input Common-Mode Range		V_S = 2.7V	0.35		1.5	V
		V_S = 5V	0.55		3.8	V
Common-Mode Rejection	CMRR	V_S = 5V, V_{CM} = 0.55V to 3.8V	60	73		dB
Over Temperature		**V_S = 5V, V_{CM} = 0.55V to 3.8V**	**60**			**dB**
		V_S = 2.7V, V_{CM} = 0.35V to 1.5V		73		dB
Crosstalk, Dual				114		dB
INPUT BIAS CURRENT		V_{CM} = V_S/2				
Bias Current	I_B			±0.5	±10	pA
Offset Current	I_{OS}			±0.5	±10	pA
NOISE, RTI		R_S = 0Ω				
Voltage Noise: f = 10Hz	e_N			280		nV/√Hz
f = 100Hz				96		nV/√Hz
f = 1kHz				46		nV/√Hz
f = 0.1Hz to 10Hz				7		µVp-p
Current Noise: f = 1kHz	i_N			0.5		fA/√Hz
GAIN[1]						
Gain Equation, Externally Set		G > 5		G = 5 + 5(R_2/R_1)		
Range of Gain			5		1000	V/V
Gain Error				±0.07	±0.4	%
vs Temperature		**G = 5**		**±2**	**±10**	**ppm/°C**
Nonlinearity		G = 25, V_S = 5V, V_O = 0.05 to 4.95		±0.001	±0.010	% of FS
Over Temperature				**±0.002**	**±0.015**	**% of FS**
OUTPUT						
Output Voltage Swing from Rail[2]		G ≥ 10	50	25		mV
Over Temperature			**50**			**mV**
Capacitance Load Drive			See Typical Characteristics[3]			pF
Short-Circuit Current	I_{SC}			+48/–32		mA
FREQUENCY RESPONSE						
Bandwidth, –3dB	BW	G = 25		2.0		MHz
Slew Rate	SR	V_S = 5V, G = 25		5		V/µs
Settling Time, 0.1%	t_S	G = 25, C_L = 100pF, V_O = 2V step		1.7		µs
0.01%				2.5		µs
Overload Recovery		50% Input Overload G = 25		2		µs
POWER SUPPLY						
Specified Voltage Range			+2.7		+5.5	V
Operating Voltage Range				+2.5 to +5.5		V
Quiescent Current per Channel	I_Q	V_{SD} > 2.5[4]		415	490	µA
Over Temperature					**600**	**µA**
Shutdown Quiescent Current/Chan	I_{SD}	V_{SD} < 0.8[4]		0.01	1	µA
TEMPERATURE RANGE						
Specified/Operating Range			–55		+125	°C
Storage Range			–65		+150	°C
Thermal Resistance	θ_{JA}	MSOP-8, TSSOP-14 Surface Mount		150		°C/W

NOTES: (1) Does not include errors from external gain setting resistors.
(2) Output voltage swings are measured between the output and power-supply rails. Output swings to rail only if G ≥ 10. Output does not swing to positive rail if gain is less than 10.
(3) See typical characteristic curve, *Percent Overshoot vs Load Capacitance*.
(4) See typical characteristic curve, *Shutdown Voltage vs Supply Voltage*.

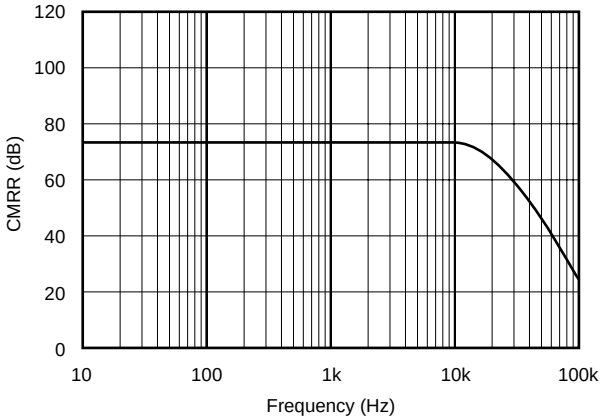
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

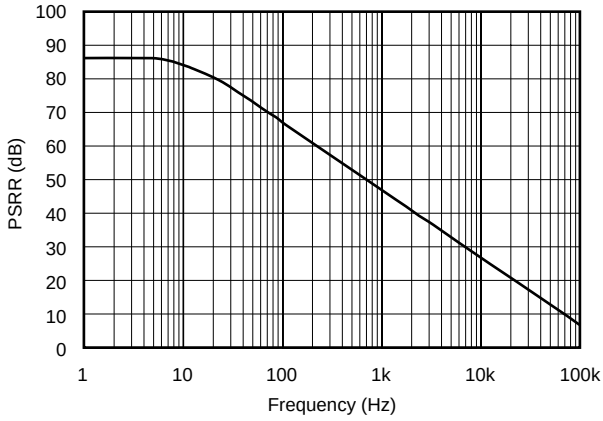
GAIN vs FREQUENCY



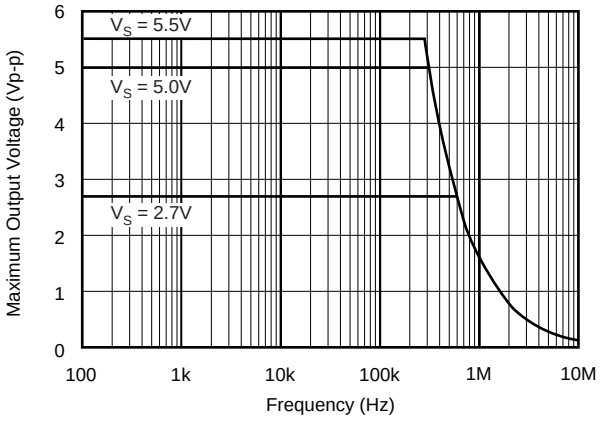
COMMON-MODE REJECTION RATIO vs FREQUENCY



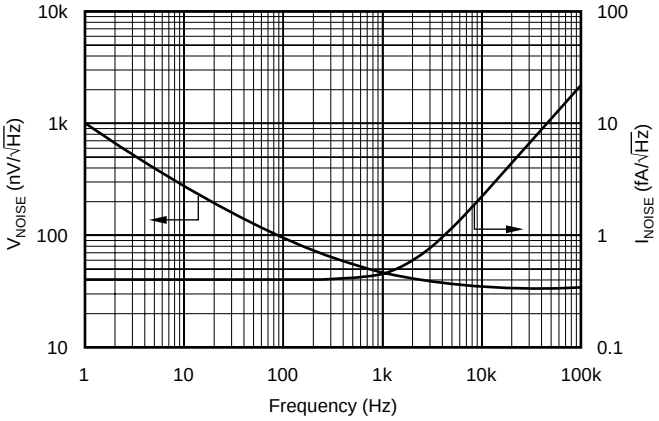
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



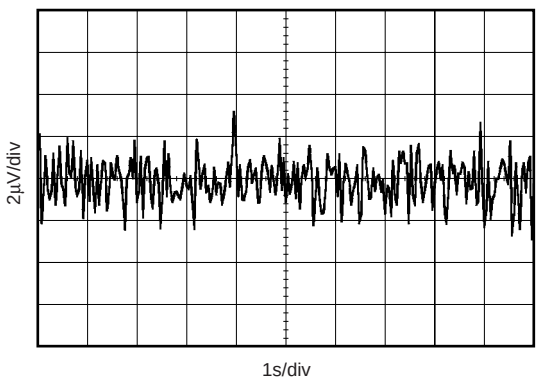
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



NOISE vs FREQUENCY



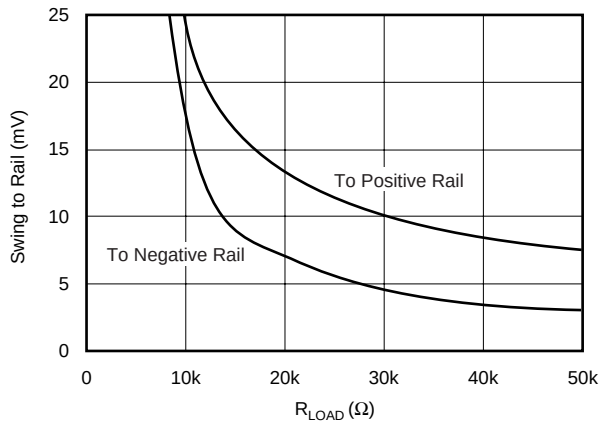
0.1Hz TO 10Hz VOLTAGE NOISE



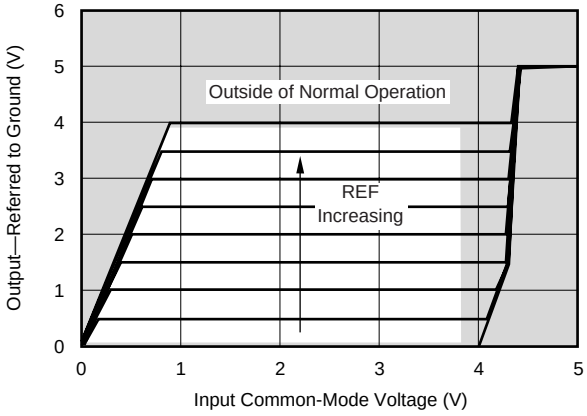
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

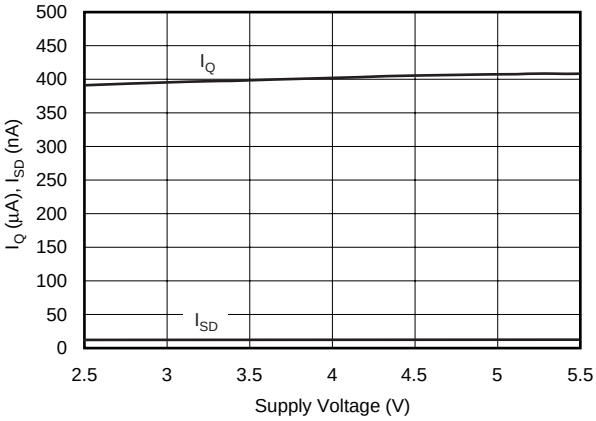
OUTPUT SWING vs LOAD RESISTANCE



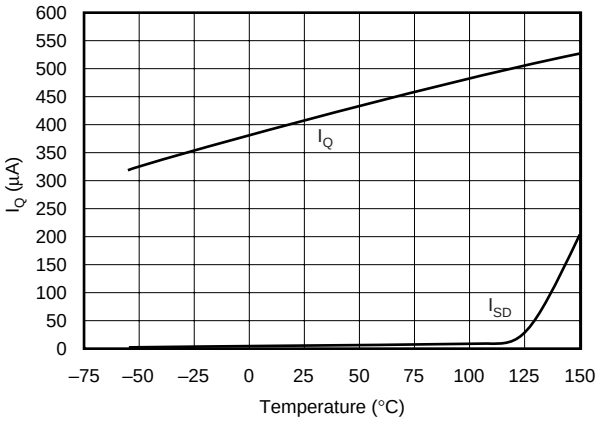
COMMON-MODE INPUT RANGE vs REFERENCE VOLTAGE



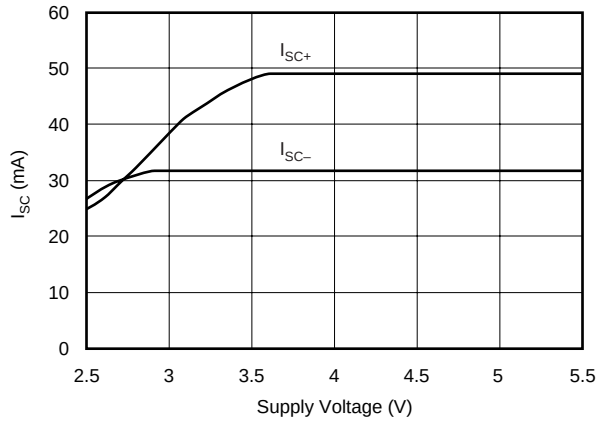
QUIESCENT CURRENT AND SHUTDOWN CURRENT vs POWER SUPPLY



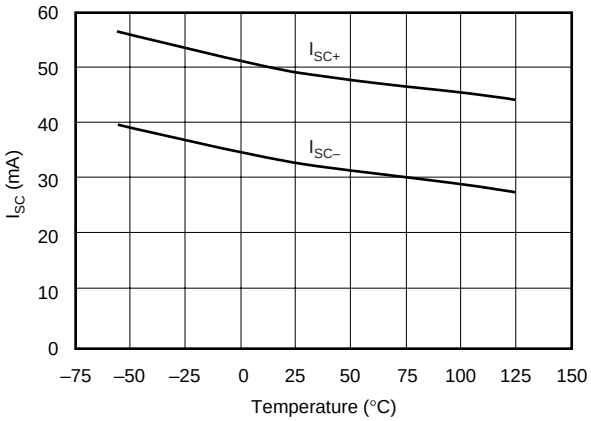
QUIESCENT CURRENT AND SHUTDOWN CURRENT vs TEMPERATURE



SHORT-CIRCUIT CURRENT vs POWER SUPPLY



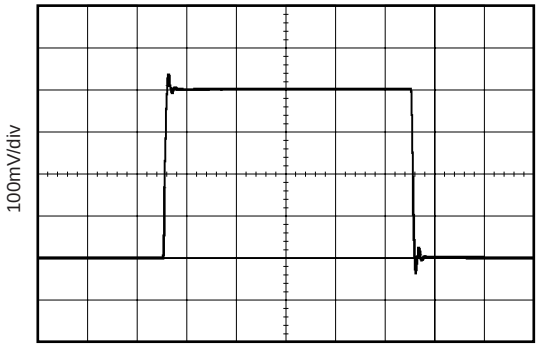
SHORT-CIRCUIT CURRENT vs TEMPERATURE



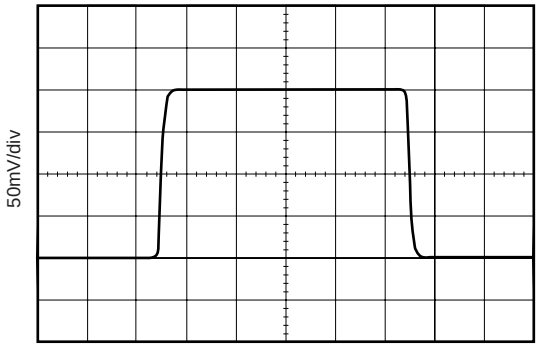
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

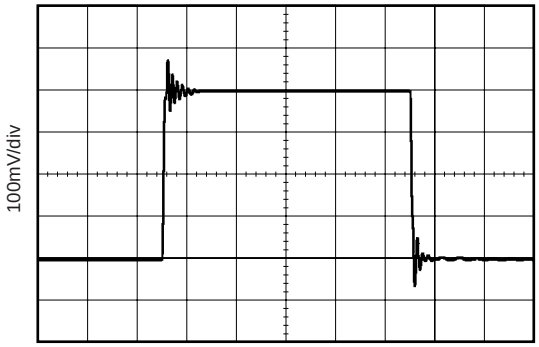
SMALL-SIGNAL STEP RESPONSE (G = 5)



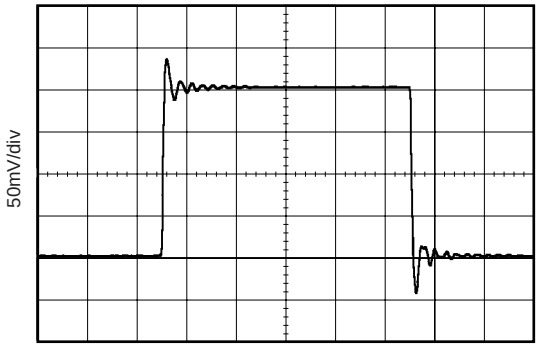
SMALL-SIGNAL STEP RESPONSE (G = 100)



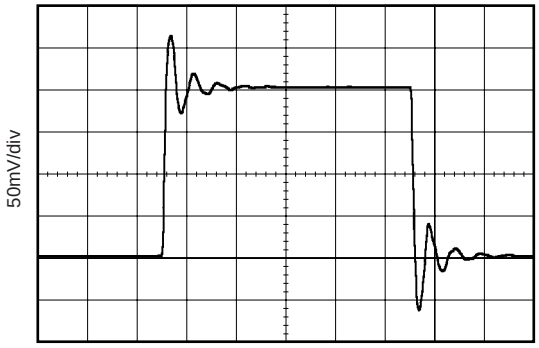
SMALL-SIGNAL STEP RESPONSE
(G = 5, C_L = 1000pF)



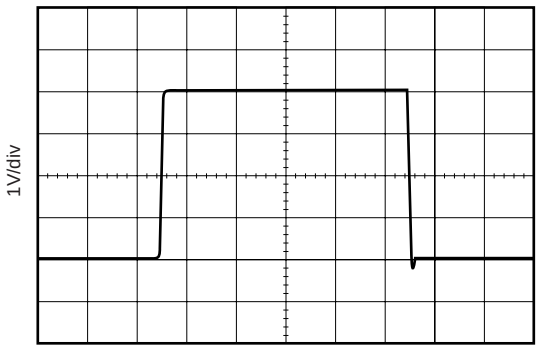
SMALL-SIGNAL STEP RESPONSE
(G = 100, C_L = 1000pF)



SMALL-SIGNAL STEP RESPONSE
(G = 100, C_L = 4700pF)



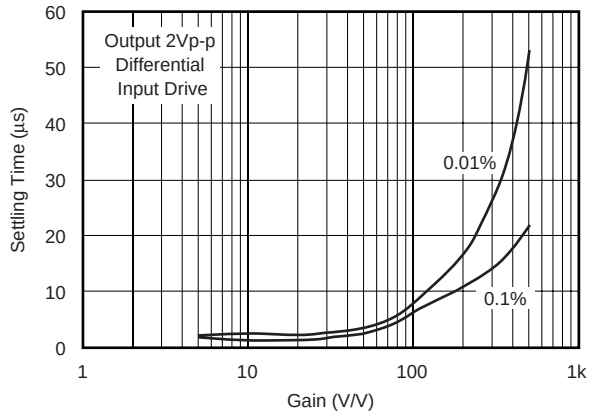
LARGE-SIGNAL STEP RESPONSE (G = 25)



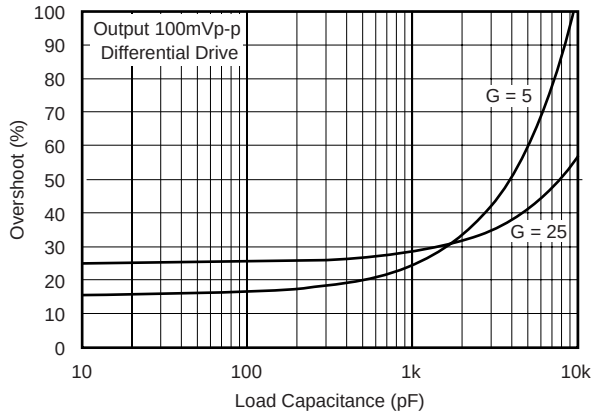
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

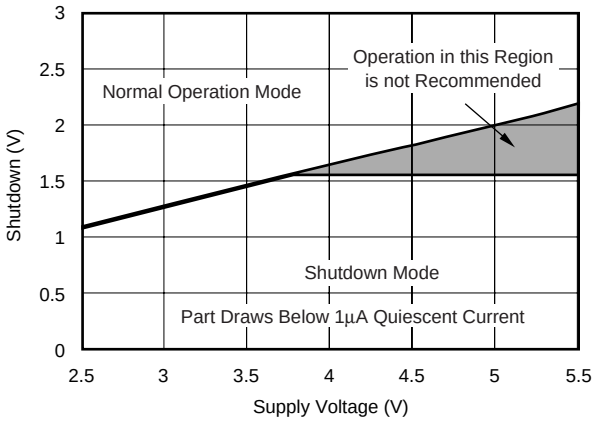
SETTLING TIME vs GAIN



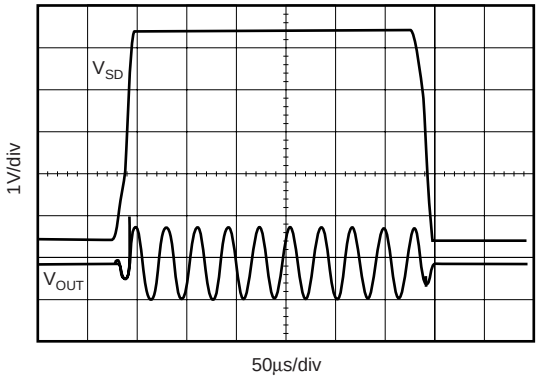
PERCENT OVERSHOOT vs LOAD CAPACITANCE



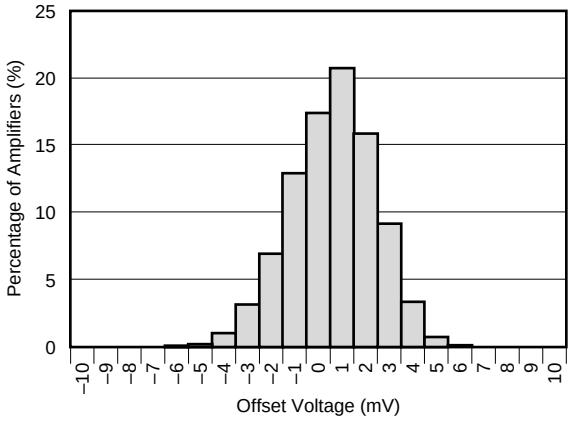
SHUTDOWN VOLTAGE vs SUPPLY VOLTAGE



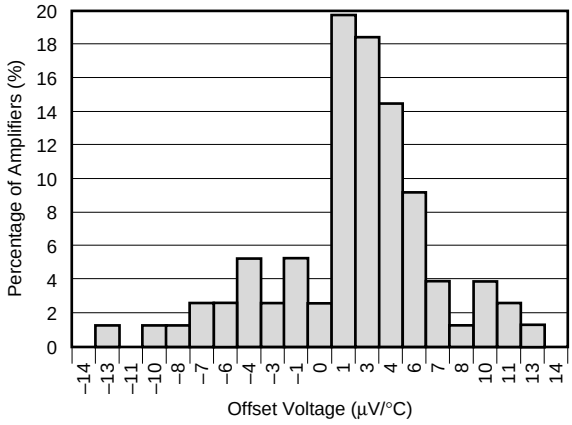
SHUTDOWN TRANSIENT BEHAVIOR



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



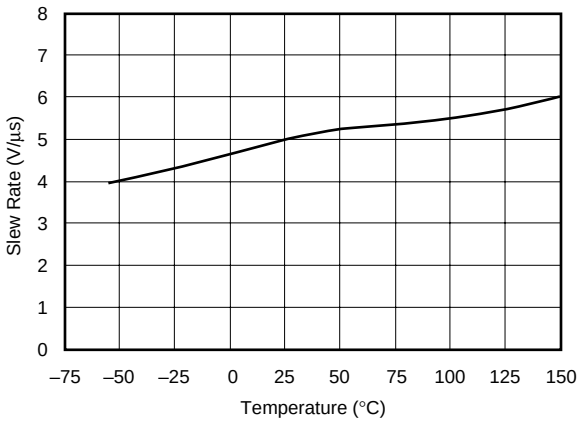
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



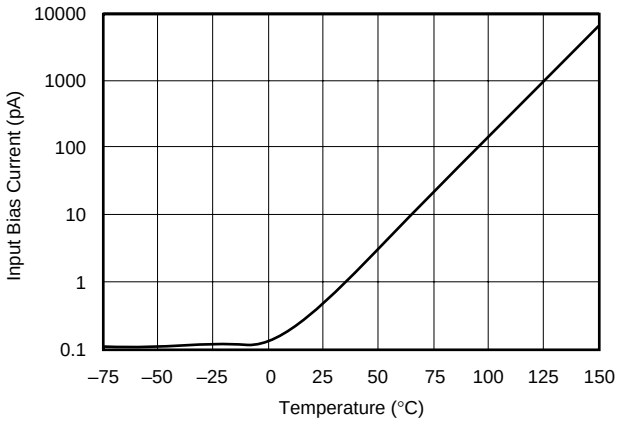
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = 5V, V_{CM} = V_S/2, R_L = 10kΩ, and C_L = 100pF, unless otherwise noted.

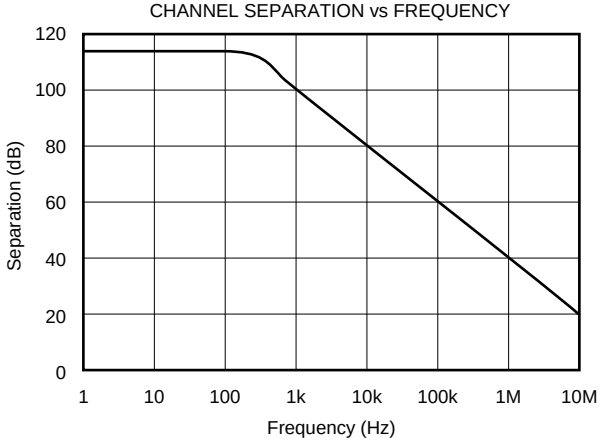
SLEW RATE vs TEMPERATURE



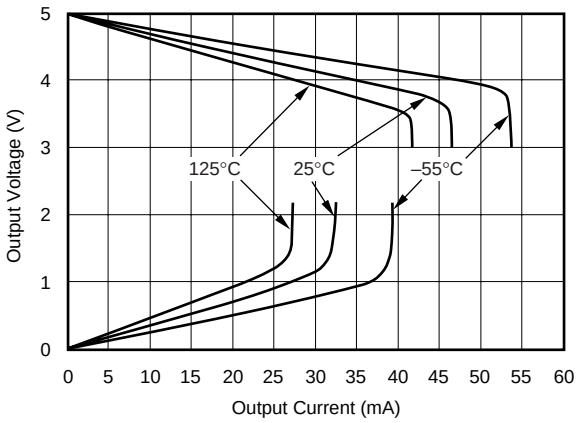
INPUT BIAS CURRENT vs TEMPERATURE



CHANNEL SEPARATION vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

The INA332 is a modified version of the classic *two op amp* instrumentation amplifier, with an additional gain amplifier.

Figure 1 shows the basic connections for the operation of the INA332 and INA2332. The power supply should be capacitively decoupled with 0.1µF capacitors as close to the INA332 as possible for noisy or high-impedance applications.

The output is referred to the reference terminal, which must be at least 1.2V below the positive supply rail.

OPERATING VOLTAGE

The INA332 family is fully specified over a supply range of +2.7V to +5.5V, with key parameters tested over the temperature range of –55°C to +125°C. Parameters that vary significantly with operating conditions, such as load conditions or temperature, are shown in the Typical Characteristics.

The INA332 may be operated on a single supply. Figure 2 shows a bridge amplifier circuit operated from a single +5V supply. The bridge provides a small differential voltage riding on an input common-mode voltage.

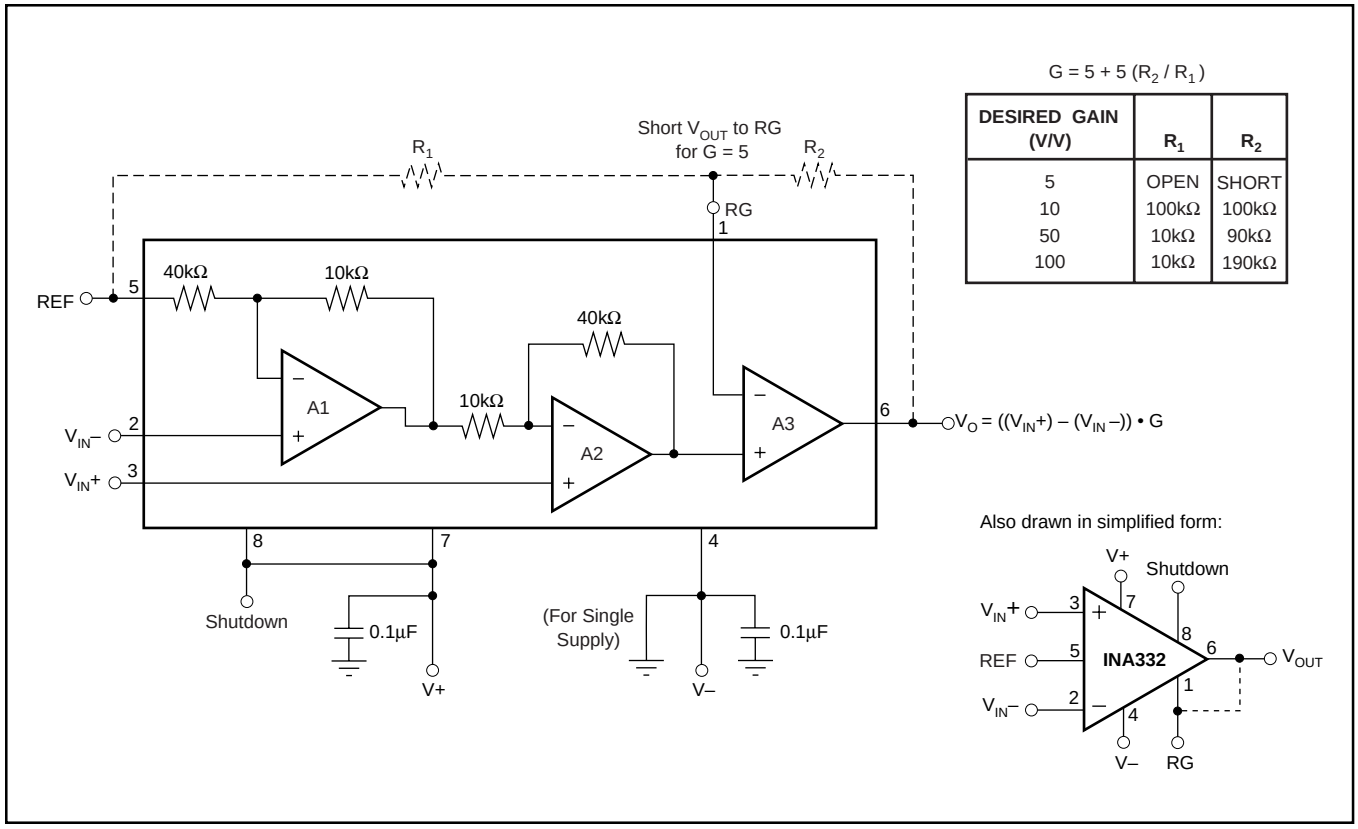


FIGURE 1. Basic Connections.

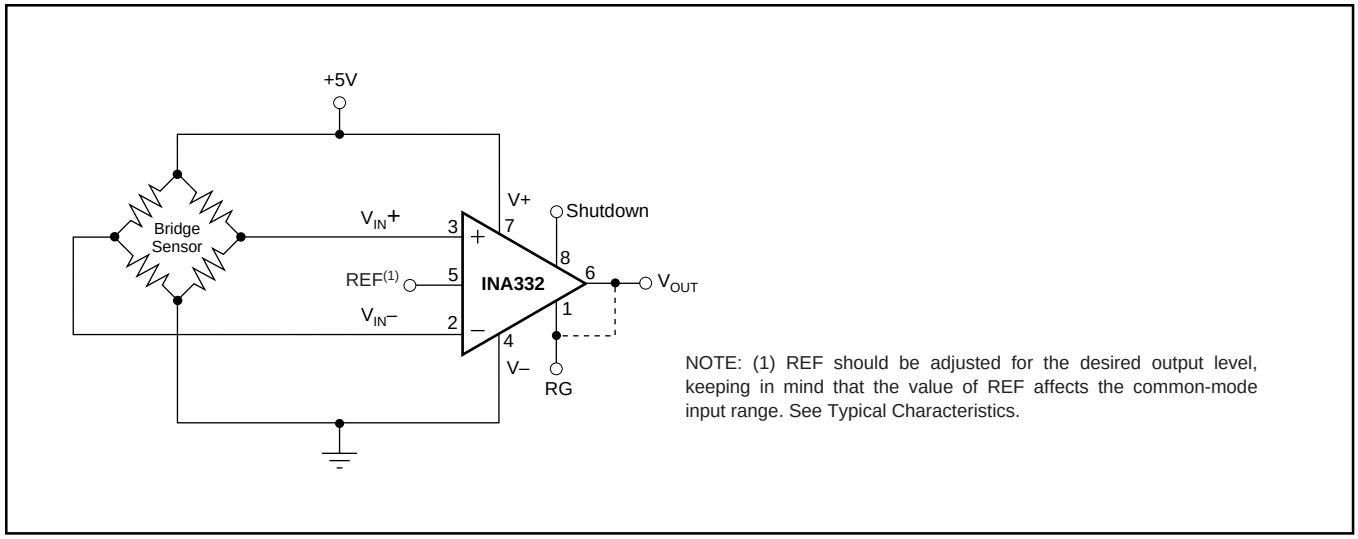


FIGURE 2. Single-Supply Bridge Amplifier.

SETTING THE GAIN

The ratio of R_2 to R_1, or the impedance between pins 1, 5, and 6, determines the gain of the INA332. With an internally set gain of 5, the INA332 can be programmed for gains greater than 5 according to the following equation:

$$G = 5 + 5\ (R_2/R_1)$$

The INA332 is designed to provide accurate gain, with gain error less than 0.4%. Setting gain with matching TC resistors will minimize gain drift. Errors from external resistors will add directly to the error, and may become dominant error sources.

COMMON-MODE INPUT RANGE

The upper limit of the common-mode input range is set by the common-mode input range of the second amplifier, A2, to 1.2V below positive supply. Under most conditions, the amplifier operates beyond this point with reduced performance. The lower limit of the input range is bounded by the output swing of amplifier A1, and is a function of the reference voltage according to the following equation:

$$V_{OA1} = 5/4\ V_{CM} - 1/4\ V_{REF}$$

(See typical characteristic curve, *Common-Mode Input Range vs Reference Voltage*).

REFERENCE

The reference terminal defines the zero output voltage level. In setting the reference voltage, the common-mode input of A3 should be considered according to the following equation:

$$V_{OA2} = V_{REF} + 5\ (V_{IN}+ - V_{IN}-)$$

For ensured operation, V_{OA2} should be less than $V_{DD} - 1.2V$.

The reference pin requires a low-impedance connection. As little as 160Ω in series with the reference pin will degrade the CMRR to 50dB. The reference pin may be used to compensate for the offset voltage (see the *Offset Trimming* section). The reference voltage level also influences the common-mode input range (see the *Common-Mode Input Range* section).

INPUT BIAS CURRENT RETURN

With a high input impedance of $10^{13}\Omega$, the INA332 is ideal for use with high-impedance sources. The input bias current of less than 10pA makes the INA332 nearly independent of input impedance and ideal for low-power applications.

For proper operation, a path must be provided for input bias currents for both inputs. Without input bias current paths, the inputs will *float* to a potential that exceeds common-mode range and the input amplifier will saturate. Figure 3 shows how bias current path can be provided in the cases of microphone applications, thermistor applications, ground returns, and dc-coupled resistive bridge applications.

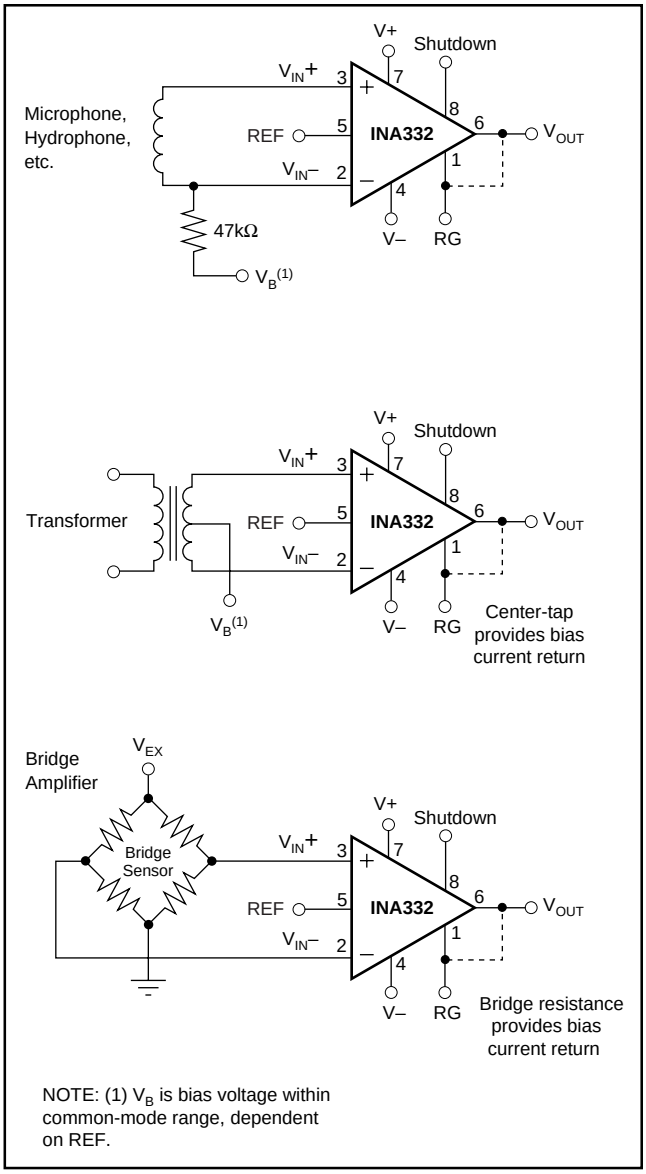


FIGURE 3. Providing an Input Common-Mode Path.

When differential source impedance is low, the bias current return path can be connected to one input. With higher source impedance, two equal resistors will provide a balanced input. The advantages are lower input offset voltage due to bias current flowing through the source impedance and better high-frequency gain.

SHUTDOWN MODE

The shutdown pin of the INA332 is nominally connected to V+. When the pin is pulled below 0.8V on a 5V supply, the INA332 goes into sleep mode within nanoseconds. For actual shutdown threshold, see typical characteristic curve, *Shutdown Voltage vs Supply Voltage*. Drawing less than 2µA of current, and returning from sleep mode in microseconds, the shutdown feature is useful for portable applications. Once in sleep mode, the amplifier has high output impedance, making the INA332 suitable for multiplexing.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output for gains of 10 or greater. For resistive loads greater than 10kΩ, the output voltage can swing to within 25mV of the supply rail while maintaining low gain error. For heavier loads and over temperature, see the typical characteristic curve, *Output Voltage Swing vs Output Current*. The INA332's low output impedance at high frequencies makes it suitable for directly driving Capacitive-Input A/D converters, as shown in Figure 4.

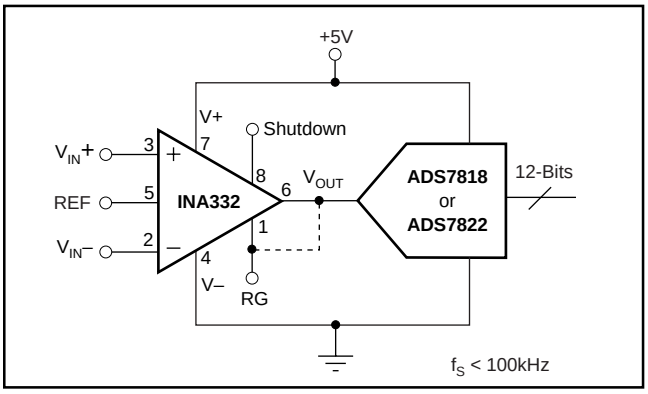


FIGURE 4. INA332 Directly Drives Capacitive-Input, High-Speed A/D Converter.

OUTPUT BUFFERING

The INA332 is optimized for a load impedance of 10kΩ or greater. For higher output current the INA332 can be buffered using the OPA340, as shown in Figure 5. The OPA340 can swing within 50mV of the supply rail, driving a 600Ω load. The OPA340 is available in the tiny MSOP-8 package.

OFFSET TRIMMING

The INA332 is laser trimmed for low offset voltage. In the event that external offset adjustment is required, the offset can be adjusted by applying a correction voltage to the reference terminal. Figure 6 shows an optional circuit for trimming offset voltage. The voltage applied to the REF terminal is added to the output signal. The gain from REF to V_{OUT} is +1. An op amp buffer is used to provide low impedance at the REF terminal to preserve good common-mode rejection.

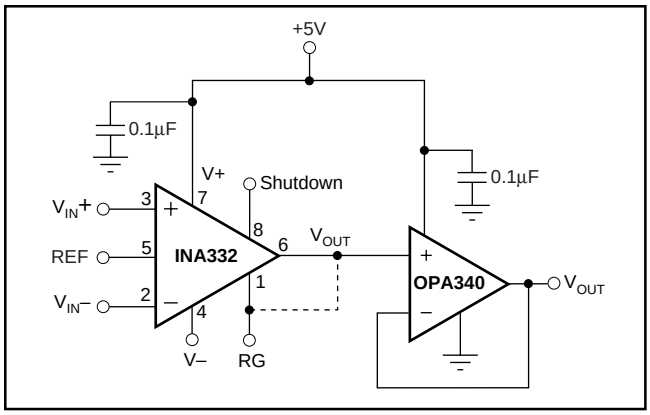


FIGURE 5. Output Buffering Circuit. Able to drive loads as low as 600Ω.

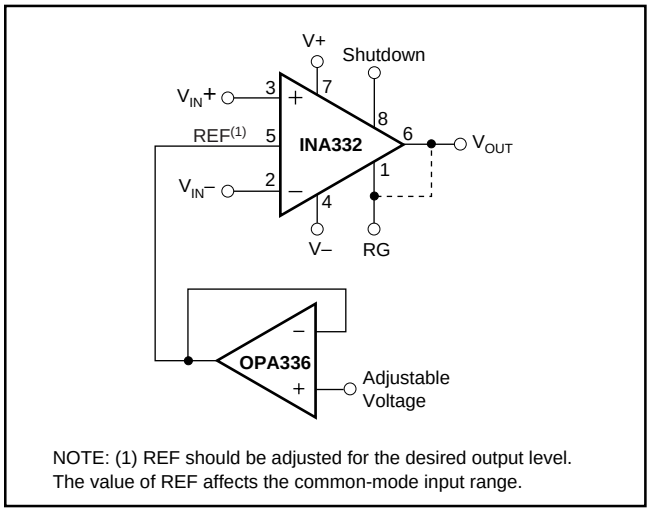


FIGURE 6. Optional Offset Trimming Voltage.

INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current through the input pins is limited to 10mA. This is easily accomplished with input resistor R_{LIM}, as shown in Figure 7. Many input signals are inherently current-limited to less than 10mA; therefore, a limiting resistor is not required.

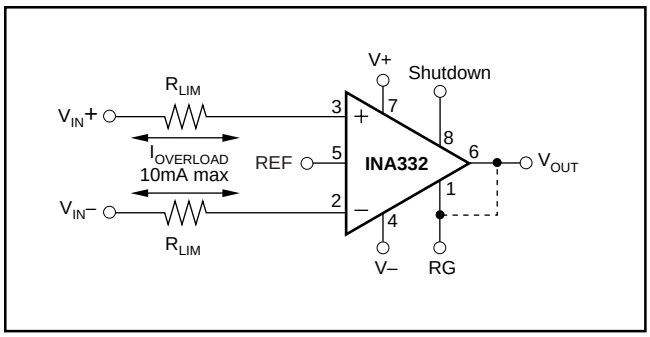


FIGURE 7. Sample Output Buffering Circuit.

OFFSET VOLTAGE ERROR CALCULATION

The offset voltage (V_{OS}) of the INA332AIDGK is specified at a maximum of 500µV with a +5V power supply and the common-mode voltage at V_S/2. Additional specifications for power-supply rejection and common-mode rejection are provided to allow the user to easily calculate worst-case expected offset under the conditions of a given application.

Power-Supply Rejection Ratio (PSRR) is specified in µV/V. For the INA332, worst case PSRR is 200µV/V, which means for each volt of change in power supply, the offset may shift up to 200µV. Common-Mode Rejection Ratio (CMRR) is specified in dB, which can be converted to µV/V using the following equation:

$$\text{CMRR (in } \mu V/V) = 10^{[(\text{CMRR in dB})/-20]} \bullet 10^6$$

For the INA332, the worst case CMRR over the specified common-mode range is 60dB (at G = 25) or about 30µV/V This means that for every volt of change in common-mode, the offset will shift less than 30µV.

These numbers can be used to calculate excursions from the specified offset voltage under different application conditions. For example, an application might configure the amplifier with a 3.3V supply with 1V common-mode. This configuration varies from the specified configuration, representing a 1.7V variation in power supply (5V in the offset specification versus 3.3V in the application) and a 0.65V variation in common-mode voltage from the specified V_S/2.

Calculation of the worst-case expected offset would be as follows:

Adjusted V_{OS} = Maximum specified V_{OS} +
(power-supply variation) • PSRR +
(common-mode variation) • CMRR

V_{OS} = 0.5mV + (1.7V • 200µV) + (0.65V • 30µV)
= ±0.860mV

However, the typical value will be smaller, as seen in the Typical Characteristics.

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 8. This capacitor compensates for the zero created by the feedback network impedance and the INA332's RG-pin input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks. Also, R_X and C_L can be added to reduce high-frequency noise.

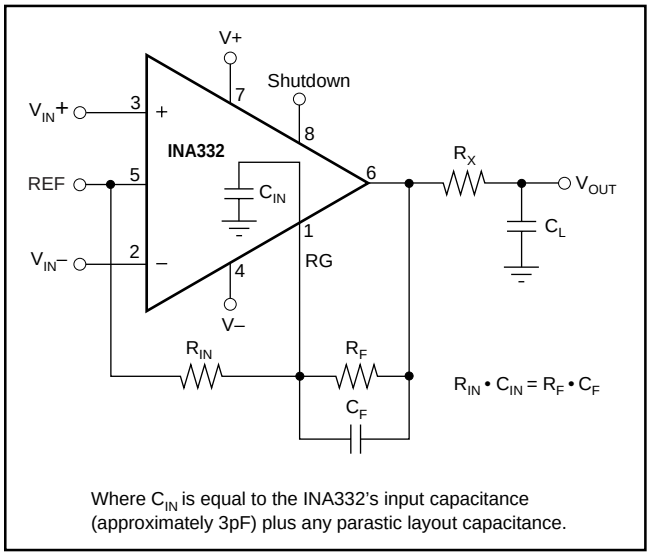


FIGURE 8. Feedback Capacitor Improves Dynamic Performance.

It is suggested that a variable capacitor be used for the feedback capacitor since input capacitance may vary between instrumentation amplifiers, and layout capacitance is difficult to determine. For the circuit shown in Figure 8, the value of the variable feedback capacitor should be chosen by the following equation:

$$R_{IN} \bullet C_{IN} = R_F \bullet C_F$$

Where C_{IN} is equal to the INA332's RG-pin input capacitance (typically 3pF) plus the layout capacitance. The capacitor can be varied until optimum performance is obtained.

APPLICATION CIRCUITS

MEDICAL ECG APPLICATIONS

Figure 9 shows the INA332 configured to serve as a low-cost ECG amplifier, suitable for moderate accuracy heart-rate applications such as fitness equipment. The input signals are obtained from the left and right arms of the patient. The common-mode voltage is set by two 2MΩ resistors. This potential through a buffer provides optional right leg drive. Filtering can be modified to suit application needs by changing the capacitor value of the output filter.

LOW-POWER, SINGLE-SUPPLY DATA ACQUISITION SYSTEMS

Refer to Figure 4 to see the INA332 configured to drive an ADS7818. Functioning at frequencies of up to 500kHz, the INA332 is ideal for low-power data acquisition.

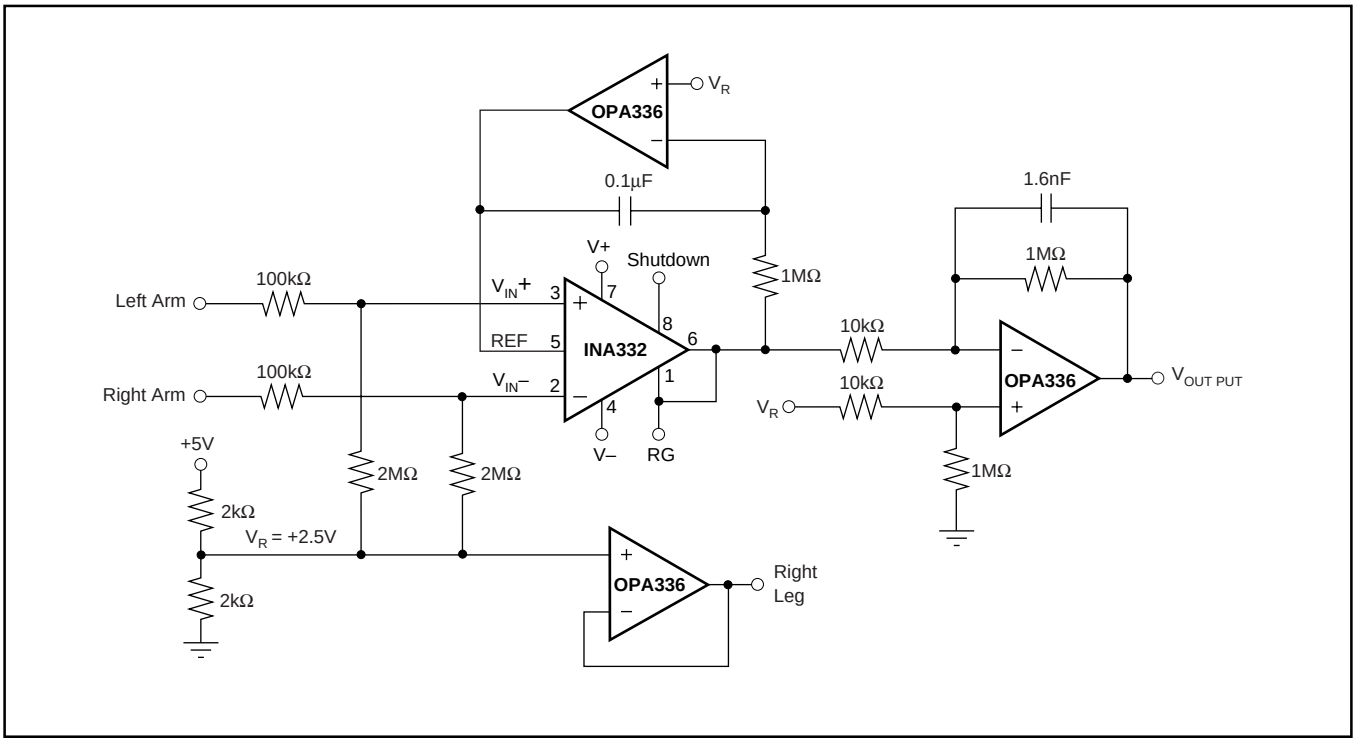


FIGURE 9. Simplified ECG Circuit for Medical Applications.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA2332AIPWR	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	INA 2332A	Samples
INA2332AIPWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	INA 2332A	Samples
INA2332AIPWTG4	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	INA 2332A	Samples
INA332AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | SN | NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	B32	Samples
INA332AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-55 to 125	B32	Samples
INA332AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | SN | NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	B32	Samples
INA332AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-55 to 125	B32	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

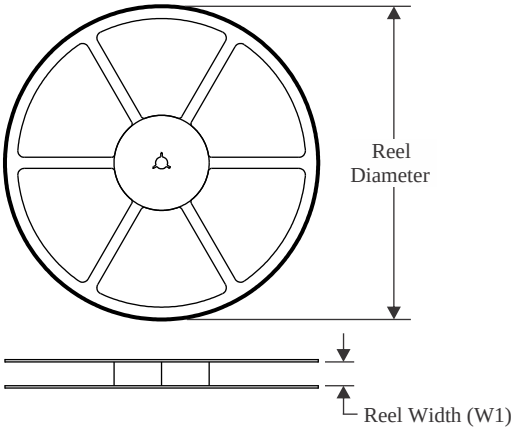
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

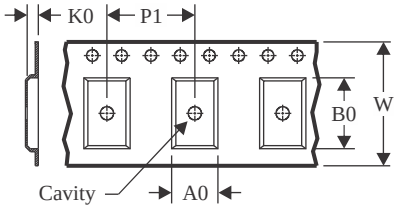
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

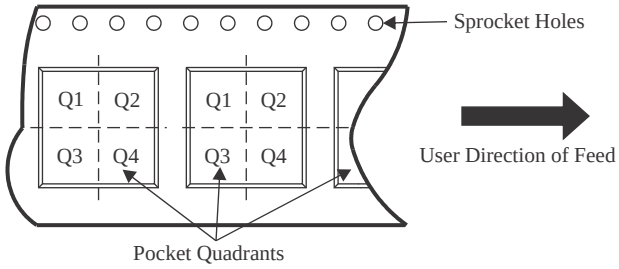


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

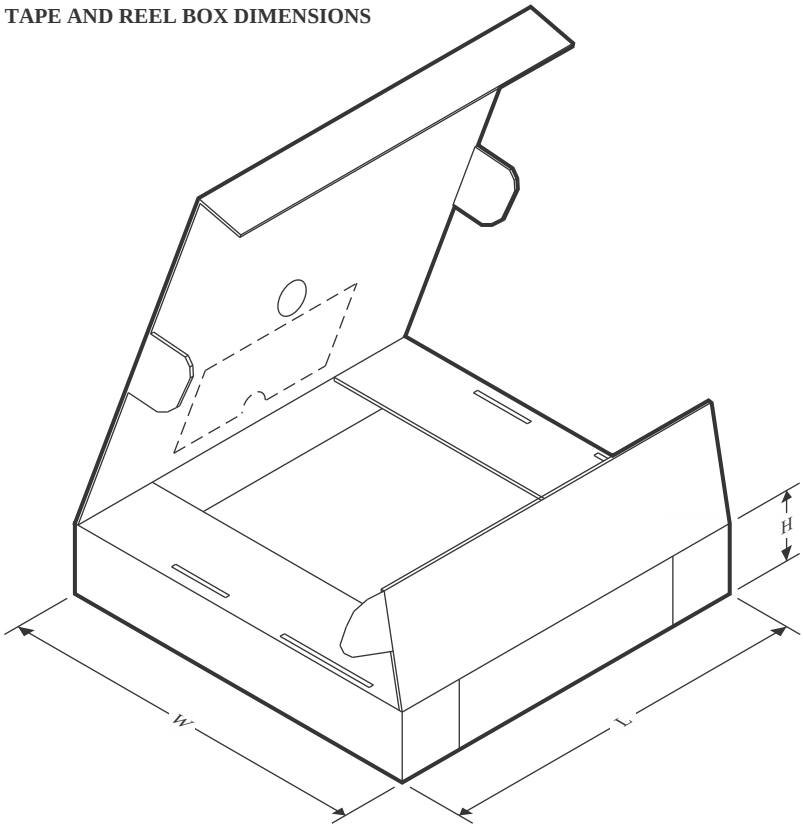
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2332AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA2332AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

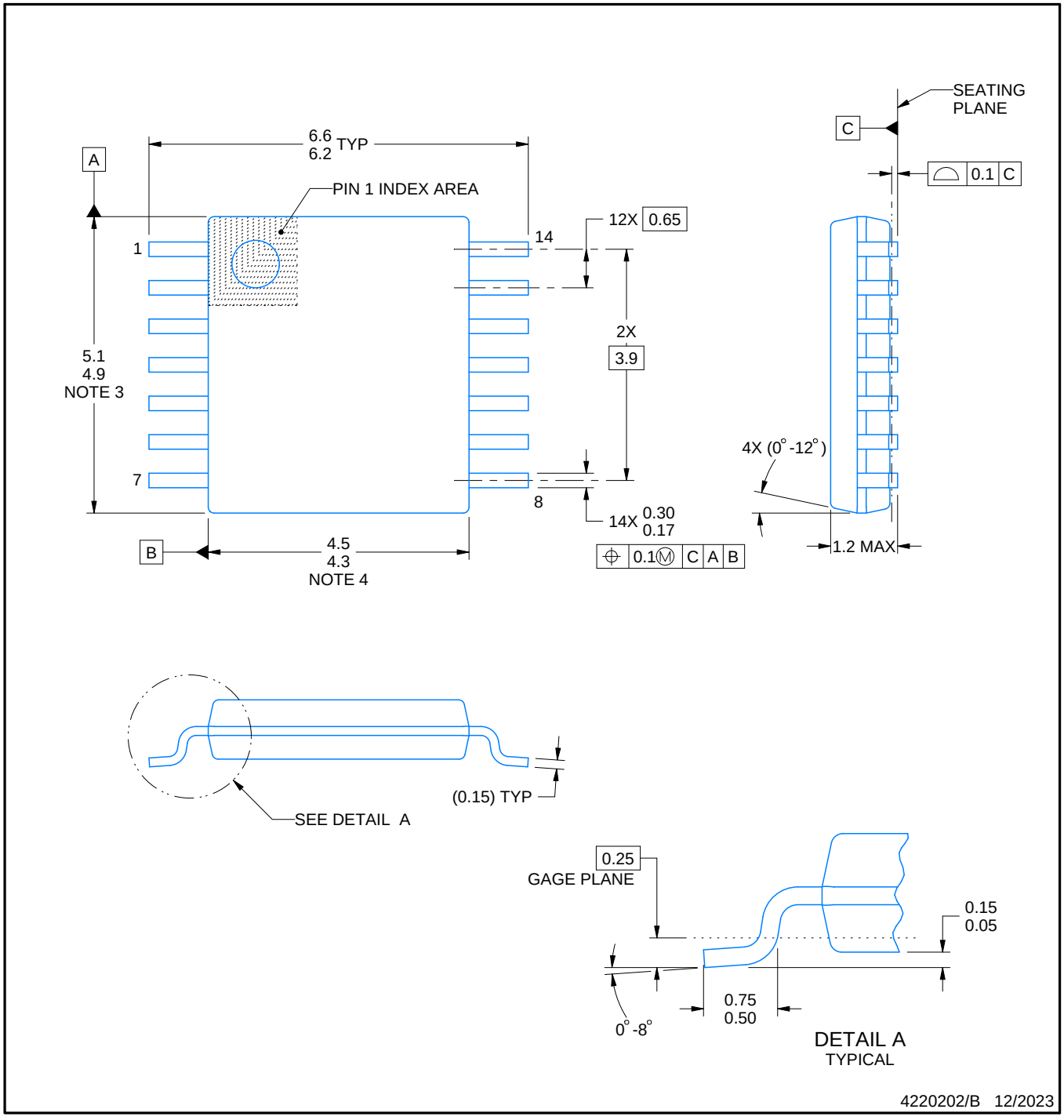
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2332AIPWR	TSSOP	PW	14	2500	367.0	367.0	35.0
INA2332AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

PACKAGE OUTLINE

PW0014A

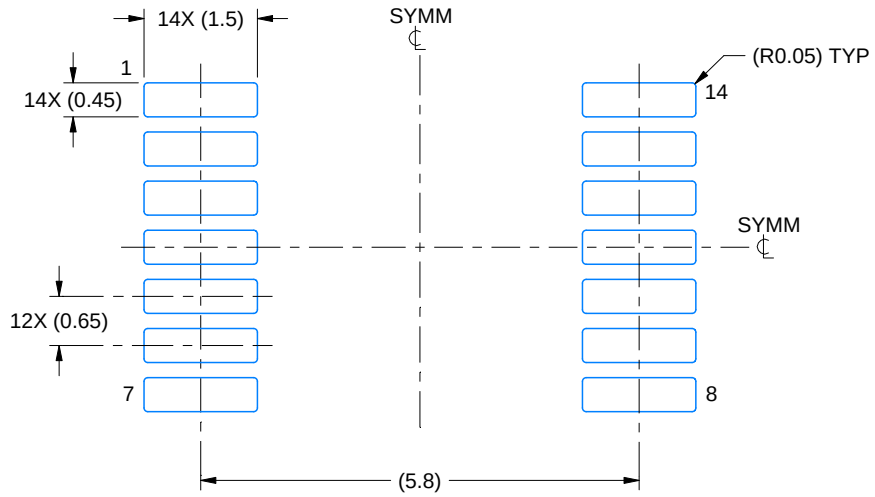
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

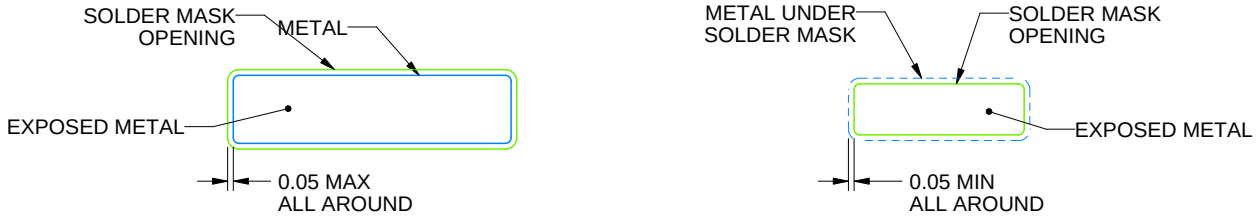


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

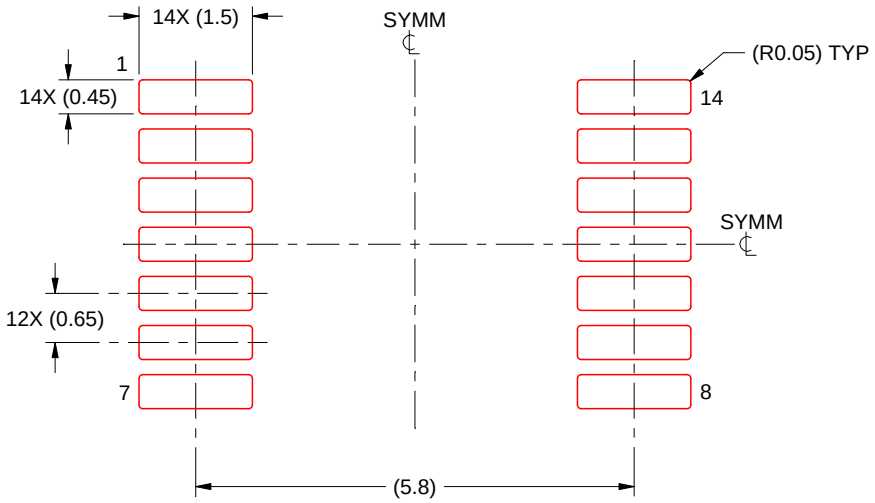


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

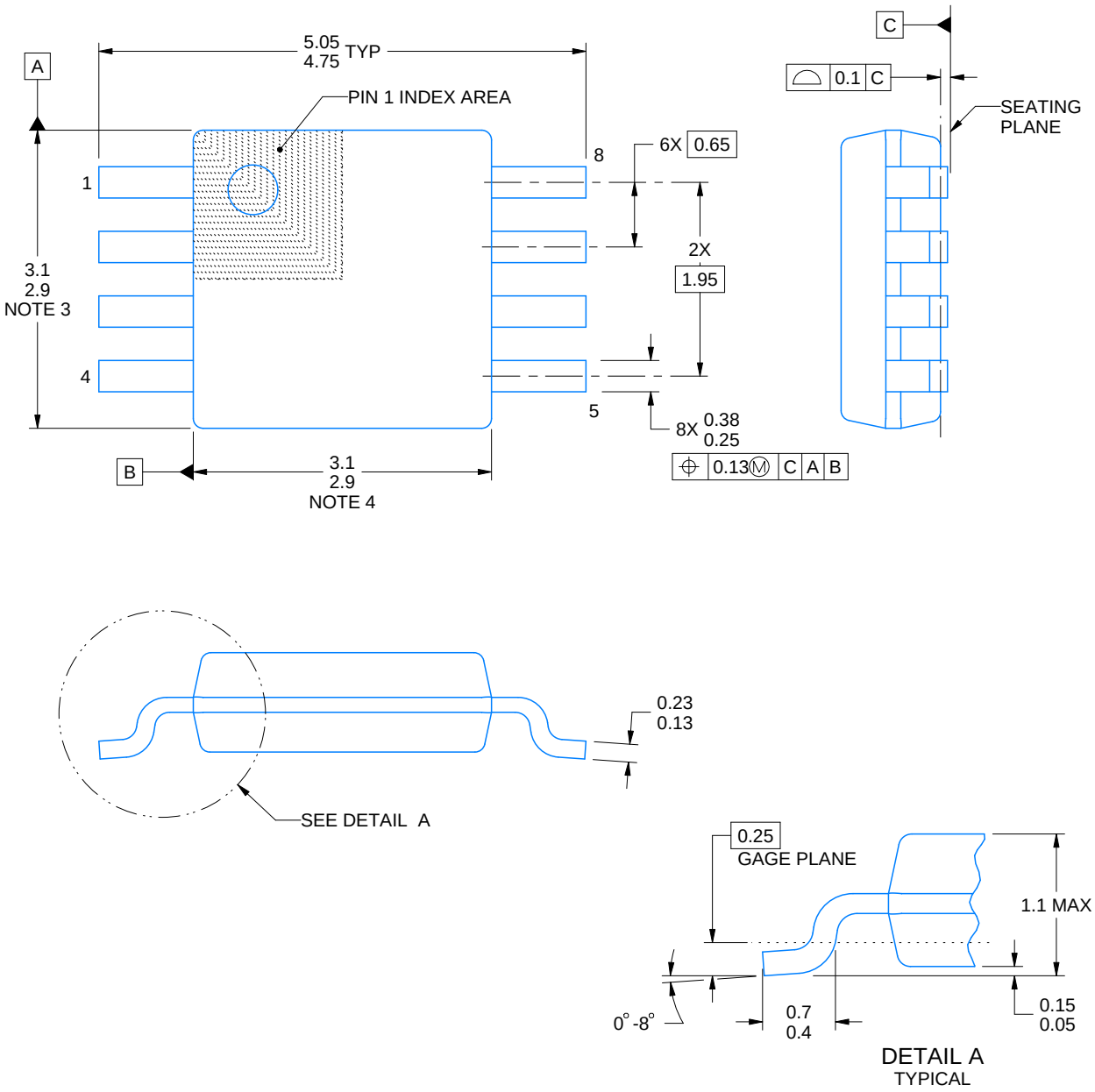
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

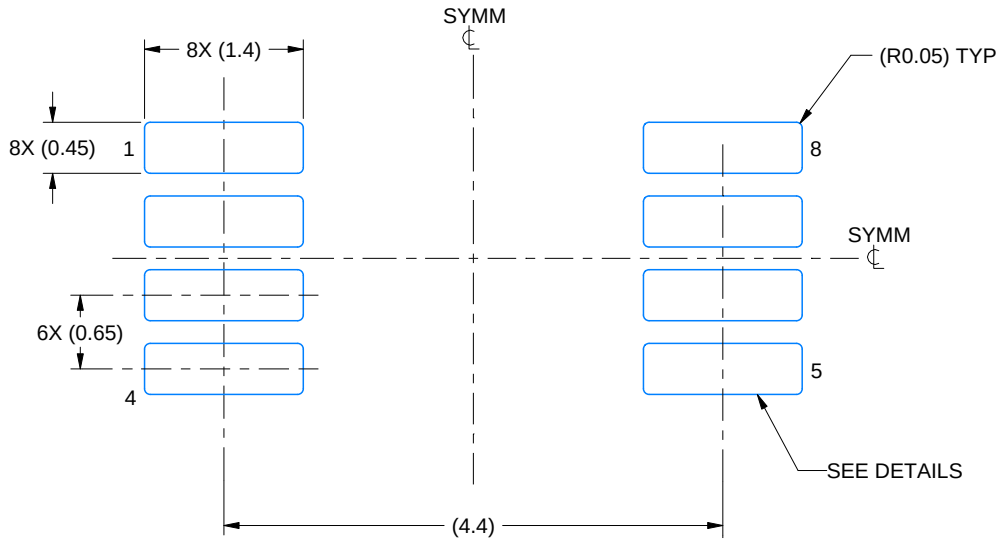
SMALL OUTLINE PACKAGE



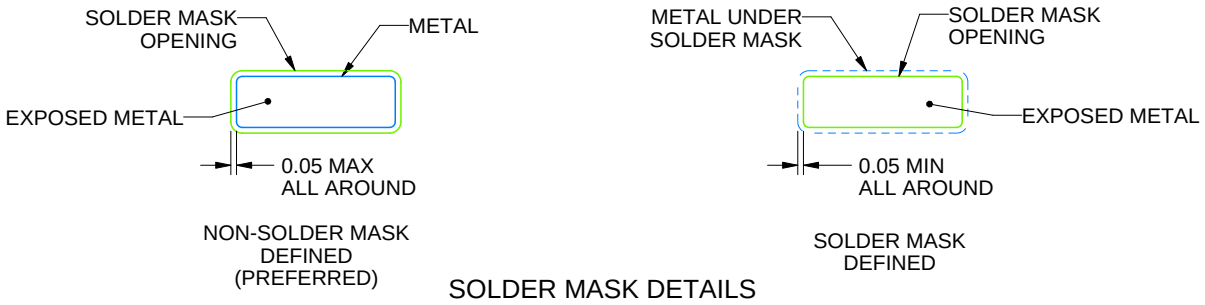
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

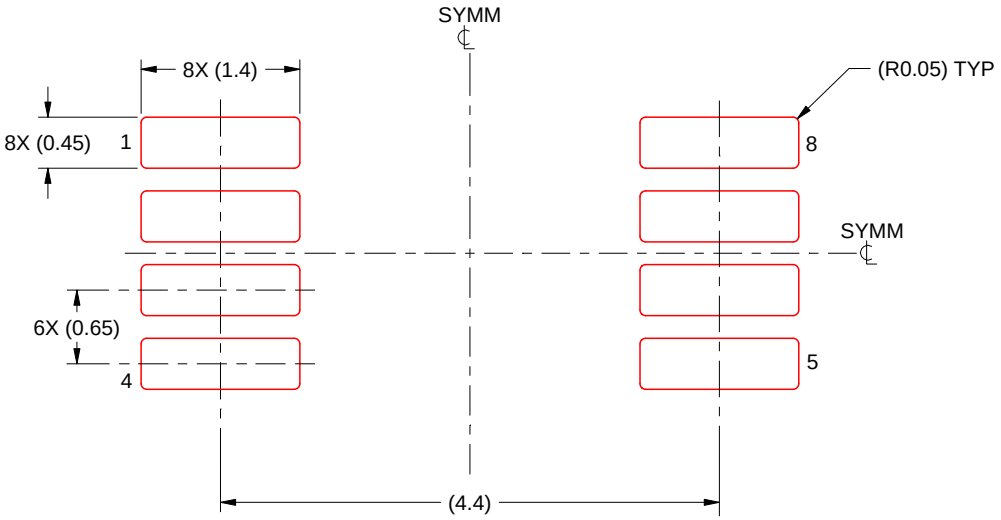


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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