

# LM93 Hardware Monitor with Integrated Fan Control for Server Management

Check for Samples: [LM93](#)

## 1 Introduction

### 1.1 Features

- 8-bit  $\Sigma\Delta$  ADC
- Monitors 16 Power Supplies
- Monitors 2 Remote Thermal Diodes
- Internal Ambient Temperature Sensing
- Programmable Autonomous Fan Control Based on Temperature Readings with Fan Boost Support
- Fan Control Based on 13-step Lookup Table
- Temperature Reading Digital Filter
- 1.0°C Digital Temperature Sensor Resolution
- 0.5°C Temperature Resolution for Fan Control
- 2 PWM Fan Speed Control Outputs
- 4 Fan Tachometer Inputs
- Dual Processor Thermal Throttling (PROCHOT) Monitoring
- Dual Dynamic VID Monitoring (6 VIDs per Processor)
- 8 General Purpose I/Os:
  - 4 Can be Configured as Fan Tachometer Inputs
  - 2 Can be Configured to Connect to THERMTRIP from a Processor
  - 2 are Standard GPIOs that Could be Used to Monitor IERR Signal
- 2 General Purpose Inputs that Can be Used to Monitor SCSI Termination Signals
- Limit Register Comparisons of All Monitored Values
- 2-wire, SMBus 2.0 Compliant, Serial Digital Interface
  - Supports Byte/block Read and Write
  - Configurable Slave Address (Tri-level Pin Selects 1 of 3 Possible Addresses)
- 2.5V Reference Voltage Output
- 56-pin TSSOP Package
- XOR-tree Test Mode
- Key Specifications
  - Voltage Measurement Accuracy  $\pm 2\%$  FS (max)
  - Resolution 8-bits, 1°C
  - Temperature Sensor Accuracy  $\pm 3^\circ\text{C}$  (max)
  - Temperature Range:
    - LM93 Operational 0°C to +85°C
    - Remote Temp Accuracy 0°C to +125°C
  - Power Supply Voltage +3.0V to +3.6V
  - Power Supply Current 0.9 mA

### 1.2 Applications

- Servers
- Workstations
- Multi-Microprocessor Based Equipment

### 1.3 Description

The LM93, hardware monitor, has a two wire digital interface compatible with SMBus 2.0. Using an 8-bit  $\Sigma\Delta$  ADC, the LM93 measures the temperature of two remote diode connected transistors as well as its own die and 16 power supply voltages.

To set fan speed, the LM93 has two PWM outputs that are each controlled by up to four temperature zones. The fan-control algorithm is lookup table based. The LM93 includes a digital filter that can be invoked to smooth temperature readings for better control of fan speed. The LM93 has four tachometer inputs to measure fan speed. Limit and status registers for all measured values are included.



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The LM93 builds upon the functionality of previous motherboard management ASICs and uses some of the LM85's features (i.e. smart tachometer mode). It also adds measurement and control support for dynamic V<sub>ccp</sub> monitoring and PROCHOT. It is designed to monitor a dual processor Xeon class motherboard with a minimum of external components.

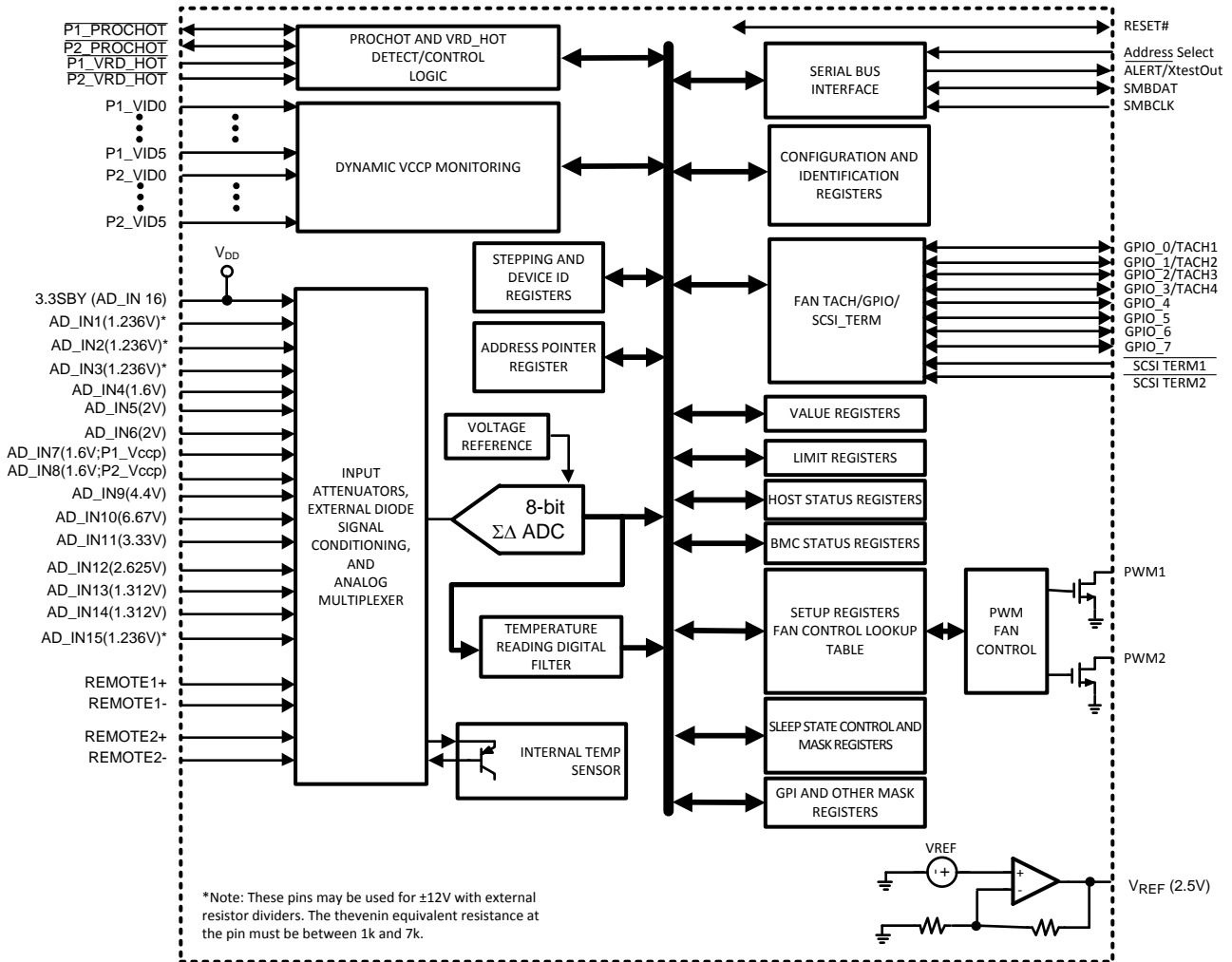


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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## 2 Device Information

### 2.1 Block Diagram



### 2.2 Application

Baseboard management of a Dual processor server. Two LM93s may be required to manage a quad processor baseboard. The block diagram of LM93 hardware is illustrated below. The hardware implementation is a single chip ASIC solution.

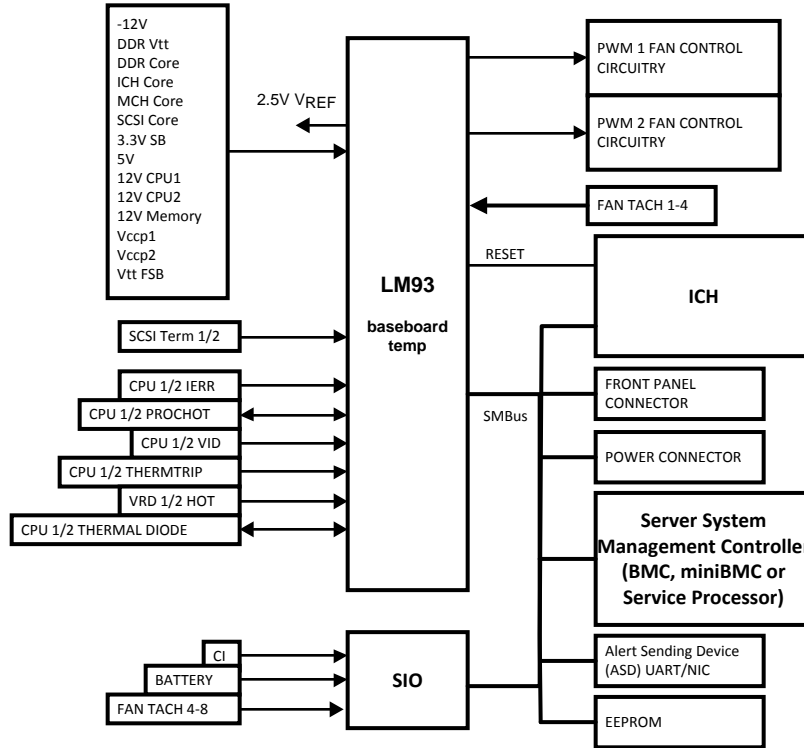


Figure 2-1. 2 Way Xeon Server Management

### 2.3 Connection Diagram

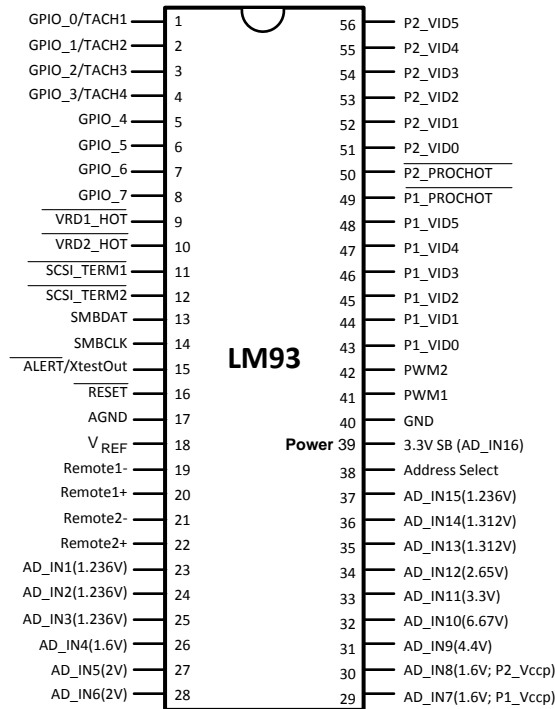


Figure 2-2. 56 Pin TSSOP Package DGG0056A Top View

**Table 2-1. Pin Descriptions<sup>(1)</sup>**

| Symbol                              | Pin # | Type                                          | Function                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------------------------------|-------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO_0/TACH1                        | 1     | Digital I/O (Open-Drain)                      | Can be configured as fan tach input or a general purpose open-drain digital I/O.                                                                                                                                                                                                                                                                                                                                       |
| GPIO_1/TACH2                        | 2     | Digital I/O (Open-Drain)                      | Can be configured as fan tach input or a general purpose open-drain digital I/O.                                                                                                                                                                                                                                                                                                                                       |
| GPIO_2/TACH3                        | 3     | Digital I/O (Open-Drain)                      | Can be configured as fan tach input or a general purpose open-drain digital I/O.                                                                                                                                                                                                                                                                                                                                       |
| GPIO_3/TACH4                        | 4     | Digital I/O (Open-Drain)                      | Can be configured as fan tach input or a general purpose open-drain digital I/O..                                                                                                                                                                                                                                                                                                                                      |
| GPIO_4 /<br>P1_THERMTRIP            | 5     | Digital I/O (Open-Drain)                      | A general purpose open-drain digital I/O. Can be configured to monitor a CPU's THERMTRIP signal to mask other errors.                                                                                                                                                                                                                                                                                                  |
| GPIO_5 /<br>P2_THERMTRIP            | 6     | Digital I/O (Open-Drain)                      | A general purpose open-drain digital I/O. Can be configured to monitor a CPU's THERMTRIP signal to mask other errors.                                                                                                                                                                                                                                                                                                  |
| GPIO_6                              | 7     | Digital I/O (Open-Drain)                      | Can be used to detect the state of CPU1 $\overline{\text{IERR}}$ or a general purpose open-drain digital I/O                                                                                                                                                                                                                                                                                                           |
| GPIO_7                              | 8     | Digital I/O (Open-Drain)                      | Can be used to detect the state of CPU2 $\overline{\text{IERR}}$ or a general purpose open-drain digital I/O                                                                                                                                                                                                                                                                                                           |
| $\overline{\text{VRD1\_HOT}}$       | 9     | Digital Input                                 | CPU1 voltage regulator $\overline{\text{HOT}}$                                                                                                                                                                                                                                                                                                                                                                         |
| $\overline{\text{VRD2\_HOT}}$       | 10    | Digital Input                                 | CPU2 voltage regulator $\overline{\text{HOT}}$                                                                                                                                                                                                                                                                                                                                                                         |
| $\overline{\text{SCSI\_TERM1}}$     | 11    | Digital Input                                 | SCSI Channel 1 termination fuse. Could also be used as a general purpose input to trigger an error event.                                                                                                                                                                                                                                                                                                              |
| $\overline{\text{SCSI\_TERM2}}$     | 12    | Digital Input                                 | SCSI Channel 2 termination fuse. Could also be used as a general purpose input to trigger an error event.                                                                                                                                                                                                                                                                                                              |
| SMBDAT                              | 13    | Digital I/O (Open-Drain)                      | Bidirectional System Management Bus Data. Output configured as 5V tolerant open-drain. SMBus 2.0 compliant.                                                                                                                                                                                                                                                                                                            |
| SMBCLK                              | 14    | Digital Input                                 | System Management Bus Clock. Driven by an open-drain output, and is 5V tolerant. SMBus 2.0 Compliant.                                                                                                                                                                                                                                                                                                                  |
| $\overline{\text{ALERT}}$ /XtestOut | 15    | Digital Output (Open-Drain)                   | Open-drain $\overline{\text{ALERT}}$ output used in an interrupt driven system to signal that an error event has occurred. Masked error events do not activate the $\overline{\text{ALERT}}$ output. When in XOR tree test mode, functions as XOR Tree output.                                                                                                                                                         |
| $\overline{\text{RESET}}$           | 16    | Digital I/O (Open-Drain)                      | Open-drain reset output when power is first applied to the LM93. Used as a reset for devices powered by 3.3V stand-by. After reset, this pin becomes a reset input. See <a href="#">RESET INPUT/OUTPUT</a> for more information.                                                                                                                                                                                       |
| AGND                                | 17    | GROUND Input                                  | Analog Ground                                                                                                                                                                                                                                                                                                                                                                                                          |
| V <sub>REF</sub>                    | 18    | Analog Output                                 | 2.5V used for external ADC reference, or as a V <sub>REF</sub> reference voltage                                                                                                                                                                                                                                                                                                                                       |
| REMOTE1-                            | 19    | Remote Thermal Diode_1- Input (CPU 1 THERMDC) | This is the negative input (current sink) from the CPU1 thermal diode. Connected to THERMDC pin of Pentium processor or the emitter of a diode connected MMBT3904 NPN transistor. Serves as the negative input into the A/D for thermal diode voltage measurements. A 100 pF capacitor is optional and can be connected between REMOTE1- and REMOTE1+.                                                                 |
| REMOTE1+                            | 20    | Remote Thermal Diode_1+ I/O (CPU1 THERMDA)    | This is a positive connection to the CPU1 thermal diode. Serves as the positive input into the A/D for thermal diode voltage measurements. It also serves as a current source output that forward biases the thermal diode. Connected to THERMDA pin of Pentium processor or the base of a diode connected MMBT3904 NPN transistor. A 100 pF capacitor is optional and can be connected between REMOTE1- and REMOTE1+. |
| REMOTE2-                            | 21    | Remote Thermal Diode_2 - Input (CPU2 THERMDC) | This is the negative input (current sink) from the CPU2 thermal diode. Connected to THERMDC pin of Pentium processor or the emitter of a diode connected MMBT3904 NPN transistor. Serves as the negative input into the A/D for thermal diode voltage measurements. A 100 pF capacitor is optional and can be connected between REMOTE2- and REMOTE2+.                                                                 |
| REMOTE2+                            | 22    | Remote Thermal Diode_2 + I/O (CPU2 THERMDA)   | This is a positive connection to the CPU2 thermal diode. Serves as the positive input into the A/D for thermal diode voltage measurements. It also serves as a current source output that forward biases the thermal diode. Connected to THERMDA pin of Pentium processor or the base of a diode connected MMBT3904 NPN transistor. A 100 pF capacitor is optional and can be connected between REMOTE2- and REMOTE2+. |
| AD_IN1                              | 23    | Analog Input (+12V1)                          | Analog Input for +12V Rail 1 monitoring, for CPU1 voltage regulator. External attenuation resistors required such that 12V is attenuated to 0.927V.                                                                                                                                                                                                                                                                    |

(1) The overscore indicates the signal is active low ("Not").

**Table 2-1. Pin Descriptions<sup>(1)</sup> (continued)**

| Symbol           | Pin # | Type                                         | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------------------|-------|----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AD_IN2           | 24    | Analog Input (+12V2)                         | Analog Input for +12V Rail 2 monitoring, for CPU2 voltage regulator. External attenuation resistors required such that 12V is attenuated to 0.927V.                                                                                                                                                                                                                                                                                                                                                                               |
| AD_IN3           | 25    | Analog Input (+12V3)                         | Analog Input for +12V Rail 3, for Memory/3GIO slots. External attenuation resistors required such that 12V is attenuated to 0.927V.                                                                                                                                                                                                                                                                                                                                                                                               |
| AD_IN4           | 26    | Analog Input (FSB_Vtt)                       | Analog input for 1.2V monitoring                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| AD_IN5           | 27    | Analog Input (3GIO / PXH / MCH_Core)         | Analog input for 1.5V monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| AD_IN6           | 28    | Analog Input (ICH_Core)                      | Analog input for 1.5V monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| AD_IN7 (P1_Vccp) | 29    | Analog Input (CPU1_Vccp)                     | Analog input for +Vccp (processor voltage) monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| AD_IN8 (P2_Vccp) | 30    | Analog Input (CPU2_Vccp)                     | Analog input for +Vccp (processor voltage) monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| AD_IN9           | 31    | Analog Input (+3.3V)                         | Analog input for +3.3V monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| AD_IN10          | 32    | Analog Input (+5V)                           | Analog input for +5V monitoring silver box supply monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| AD_IN11          | 33    | Analog Input (SCSI_Core)                     | Analog input for +2.5V monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| AD_IN12          | 34    | Analog Input (Mem_Core)                      | Analog input for +1.969V monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| AD_IN13          | 35    | Analog Input (Mem_Vtt)                       | Analog input for +0.984V monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| AD_IN14          | 36    | Analog Input (Gbit_Core)                     | Analog input for +0.984V S/B monitoring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| AD_IN15          | 37    | Analog Input (-12V)                          | Analog input for -12V monitoring. External resistors required to scale to positive level. Full scale reading at 1.236V.                                                                                                                                                                                                                                                                                                                                                                                                           |
| Address Select   | 38    | 3 level analog input                         | This input selects the lower two bits of the LM93 SMBus slave address.                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| AD_IN16          | 39    | POWER (V <sub>DD</sub> ) +3.3V standby power | V <sub>DD</sub> power input for LM93. Generally this is connected to +3.3V standby power. The LM93 can be powered by +3.3V if monitoring in low power states is not required, but power should be applied to this input before any other pins. This pin also serves as the analog input to monitor the 3.3V stand-by (SB) voltage. It is necessary to bypass this pin with a 0.1 $\mu$ F in parallel with 100 pF. A bulk capacitance of 10 $\mu$ F should be in the near vicinity. The 100 pF should be closest to the power pin. |
| GND              | 40    | GROUND                                       | Digital Ground. Digital ground and analog ground need to be tied together at the chip then both taken to a low noise system ground. A voltage difference between analog and digital ground may cause erroneous results.                                                                                                                                                                                                                                                                                                           |
| PWM1             | 41    | Digital Output (Open-Drain)                  | Fan control output 1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| PWM2             | 42    | Digital Output (Open-Drain)                  | Fan control output 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| P1_VID0          | 43    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P1_VID1          | 44    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P1_VID2          | 45    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P1_VID3          | 46    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P1_VID4          | 47    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P1_VID5          | 48    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P1_PROCHOT       | 49    | Digital I/O (Open-Drain)                     | Connected to CPU1 $\overline{\text{PROCHOT}}$ (processor hot) signal through a bidirectional level shifter.                                                                                                                                                                                                                                                                                                                                                                                                                       |
| P2_PROCHOT       | 50    | Digital I/O (Open-Drain)                     | Connected to CPU2 $\overline{\text{PROCHOT}}$ (processor hot) signal through a bi-directional level shifter.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| P2_VID0          | 51    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P2_VID1          | 52    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P2_VID2          | 53    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| P2_VID3          | 54    | Digital Input                                | Voltage Identification signal from the processor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

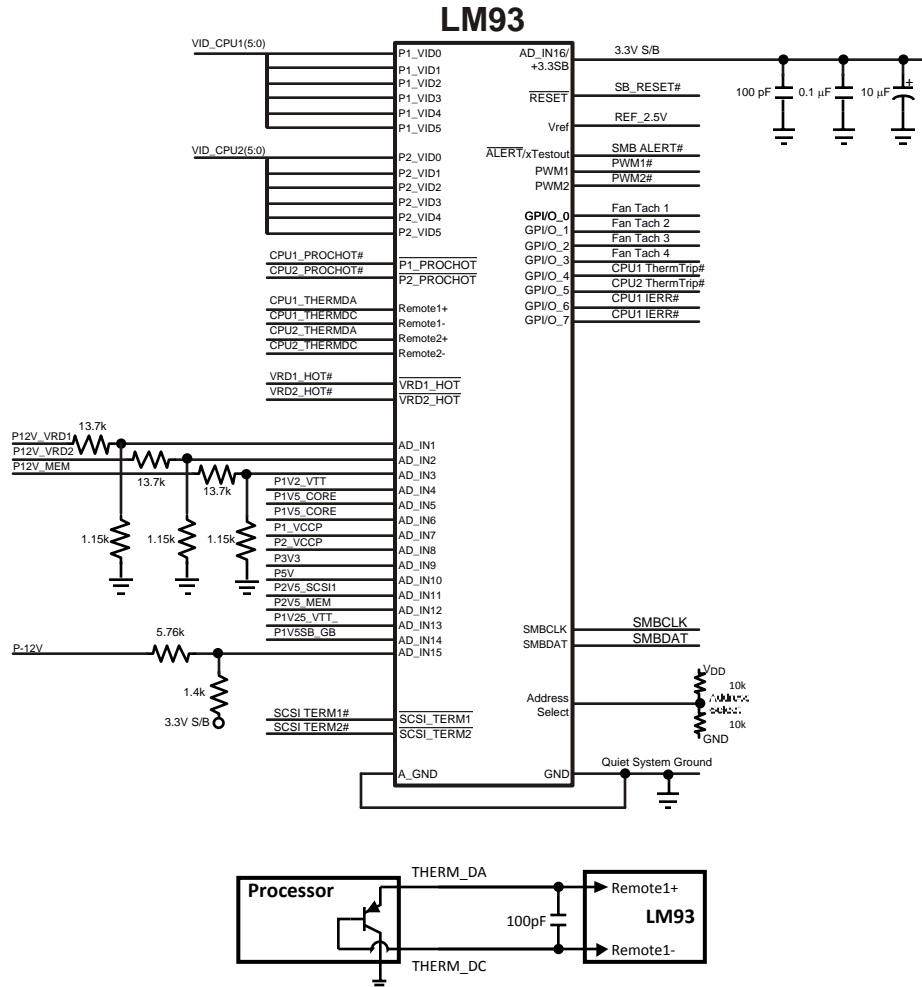
**Table 2-1. Pin Descriptions<sup>(1)</sup> (continued)**

| Symbol  | Pin # | Type          | Function                                          |
|---------|-------|---------------|---------------------------------------------------|
| P2_VID4 | 55    | Digital Input | Voltage Identification signal from the processor. |
| P2_VID5 | 56    | Digital Input | Voltage Identification signal from the processor. |

**Table 2-2. Server Terminology**

|                           |                                                                                                                                   |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| A/D                       | Analog to Digital Converter                                                                                                       |
| ACPI                      | Advanced Configuration and Power Interface                                                                                        |
| $\overline{\text{ALERT}}$ | SMBus signal to bus master that an event occurred that has been flagged for attention.                                            |
| ASF                       | Alert Standard Format                                                                                                             |
| BMC                       | Baseboard Micro-Controller                                                                                                        |
| BW                        | Bandwidth                                                                                                                         |
| DIMM                      | Dual inline memory module                                                                                                         |
| DP                        | Dual-processor                                                                                                                    |
| ECC                       | Error checking and correcting                                                                                                     |
| FRU                       | Field replaceable unit                                                                                                            |
| FSB                       | Front side bus                                                                                                                    |
| FW                        | Firmware                                                                                                                          |
| Gb                        | Gigabit                                                                                                                           |
| GB                        | Gigabyte                                                                                                                          |
| Gbe                       | Gigabit Ethernet                                                                                                                  |
| GPIO                      | General purpose I/O                                                                                                               |
| HW                        | Hardware                                                                                                                          |
| I <sup>2</sup> C          | Inter integrated circuit (bus)                                                                                                    |
| LAN                       | Local area network                                                                                                                |
| LVDS                      | Low-Voltage Differential Signaling                                                                                                |
| Mb                        | Megabit                                                                                                                           |
| MB                        | Megabyte                                                                                                                          |
| MP                        | Multi-processor                                                                                                                   |
| MTBF                      | Mean time between failures                                                                                                        |
| MTTR                      | Mean time to repair                                                                                                               |
| NIC                       | Network Interface Card (Ethernet Card)                                                                                            |
| OS                        | Operating system                                                                                                                  |
| P/S                       | Power Supply                                                                                                                      |
| PCI                       | PCI Local Bus                                                                                                                     |
| PDB                       | Power Distribution Board                                                                                                          |
| POR                       | Power On Reset                                                                                                                    |
| PS                        | Power Supply                                                                                                                      |
| SMBCLK and SMBDAT         | These signals comprise the SMBus interface (data and clock) See the <a href="#">SMBus Interface</a> section for more information. |
| VRD                       | Voltage Regulator Down - regulates Vccp voltage for a CPU                                                                         |

## 2.4 Recommended Implementation



**Note:** 100 pF cap is optional and should be placed close to the LM93, if used. The maximum capacitance between these pins is 300 pF.



### 3 Functional Description

The LM93 provides 16 channels of voltage monitoring, two remote thermal diode monitors, an onboard ambient temperature sensor, 2 PROCHOT monitors, 4 fan tachometers, 8 GPIOs, THERMTRIP monitor for masking error events, 2 SCSI\_TERM inputs, and all the associated limit registers on a single chip, which communicates to the rest of the baseboard over the System Management Bus (SMBus).

Readings from both the external thermal diodes and the internal temperature sensor are made available as an 8-bit two's-complement digital byte with the LSB representing 1°C.

All but 4 of the analog inputs include internal scaling resistors. External scaling resistors are required for measuring  $\pm 12V$ . The inputs are converted to 8-bit digital values such that a nominal voltage appears at  $\frac{3}{4}$  scale for positive voltages and  $\frac{1}{4}$  scale for negative voltages. The analog inputs are intended to be connected to both baseboard resident VRDs and to standard voltage rails supplied by a SSI compliant power supply.

The LM93 provides a number of internal registers, which are detailed in the [Registers](#) section of this document.

#### 3.1 MONITORING CYCLE TIME

When the LM93 is powered up, it cycles through each temperature measurement followed by the analog voltages in sequence, and it continuously loops through the sequence. The total monitoring cycle time is not more than 100 ms, as this is the time period that most external micro-controllers require to read the register values.

Each measured value is compared to values stored in the limit registers. When the measured value violates the programmed limit, a corresponding status bit in the B\_ and H\_Error Status Registers is set.

The PROCHOT and dynamic VID/V<sub>ccp</sub> monitoring is performed independently of the analog and temperature monitoring cycle.

#### 3.2 $\Sigma\Delta$ A/D INHERENT AVERAGING

The  $\Sigma\Delta$  A/D architecture filters the input signal. During one conversion many samples are taken of the input voltage and these samples are effectively averaged to give the final result. The output of the  $\Sigma\Delta$  A/D is the average value of the signal during the sampling interval. For a voltage measurement, the samples are accumulated for 1.5 ms. For a temperature measurement, the samples are accumulated for 8.4 ms.

#### 3.3 TEMPERATURE MONITORING

The LM93 remote diode target is the embedded thermal diode found in a Xeon class processor. In some cases instead of using the embedded thermal diode, found on the Xeon processor, a diode connected 2N3904 transistor type can also be used. An example of this would be a MMBT3904 with its collector and base tied to the thermal diode REMOTE+ pin and the emitter tied to the thermal diode REMOTE- pin. Since the MMBT3904 is a surface mount device and has very small thermal mass, it measures the board temperature where it is mounted. The non-ideality and series resistance varies for different diodes. Since the LM93 is optimized for the Xeon processor, when measuring a 2N3904 transistor an offset in the error band of approximately -4°C may be observed. This can be corrected for by programming the appropriate Zone Adjustment Offset register.

The LM93 acquires temperature data from three different sources:

2 external diodes (embedded in a processor or discrete)

1 internal diode (internal to the LM93)

In addition to these three temperatures, a fourth temperature can be externally written into the LM93 from the SMBus. This value can be used to control fans, or compared against limits, etc. The temperature value registers are located at addresses 50h–53h. The temperature sources are referred to as “zones” for convenience:

| Zone   | Description                                   |
|--------|-----------------------------------------------|
| Zone 1 | Processor 1 remote diode (REMOTE1+, REMOTE1-) |
| Zone 2 | Processor 2 remote diode (REMOTE2+, REMOTE2-) |
| Zone 3 | Internal LM93 on-chip sensor                  |
| Zone 4 | External Digital Sensor written in from SMBus |

### 3.3.1 Temperature Data Format

Most of the temperature data for the LM93 is represented in a common format. The format is an 8-bit, two's complement byte with the LSB equal to 1.0 °C. This applies to temperature measurements as well as any temperature limit registers and some configuration registers. Some fan control configuration registers use four bits and have a binary format, please see the [Fan Control](#) configuration register descriptions for further details on this 4-bit format.

| Temperature <sup>(1)</sup> | Binary    | Hex |
|----------------------------|-----------|-----|
| +125°C                     | 0111 1101 | 7Dh |
| +25°C                      | 0001 1001 | 19h |
| +1.0°C                     | 0000 0001 | 01h |
| 0°C                        | 0000 0000 | 00h |
| -1.0°C                     | 1111 1111 | FFh |
| -25°C                      | 1110 0111 | E7h |
| -55°C                      | 1100 1001 | C9h |
| -127°C                     | 1000 0001 | 81h |

(1) **Note:** A value of 80h has a special meaning in the limit registers. It means that the temperature channel is masked. In addition, temperature readings of 80h indicate thermal diode faults.

### 3.3.2 Thermal Diode Fault Status

The LM93 provides for indications of a fault (open or short circuit) with the remote thermal diodes. Before a remote diode conversion is updated, the status of the remote diode is checked for an open or short circuit condition. If such a fault condition occurs, a status bit is set in the status register. A short circuit is defined as the input pins being connected to each other. When an open or short circuit is detected, the corresponding temperature register is set to 80h.

## 3.4 VOLTAGE MONITORING

The LM93 contains inputs for monitoring voltages. Scaling is such that the correct value refers to approximately 3/4 scale or 192 decimal on all inputs except the  $\pm 12V$ . Input voltages are converted by an 8-bit Delta-Sigma ( $\Delta\Sigma$ ) A/D. The Delta-Sigma A/D architecture provides inherent filtering and spike smoothing of the analog input signal.

The  $\pm 12V$  inputs must be scaled externally. A full scale reading is achieved when 1.236V is applied to these inputs. For optimum performance the +12V should be scaled to provide a nominal  $\frac{3}{4}$  full scale reading, while the -12V should be scaled to provide a nominal  $\frac{1}{4}$  scale reading. The thevenin resistance at the pin should be kept between 1 k $\Omega$  and 7 k $\Omega$ .

The -12V monitoring is particularly challenging. It is required that an external offset voltage and external resistors be used to bring the -12V rail into the positive input voltage region of the A/D input. It is suggested that the supply rail for the LM93 device be used as the offset voltage. This voltage is usually derived from the P/S 5V stand-by voltage rail via a  $\pm 1\%$  accurate linear regulator. In this fashion we can always assume that the offset voltage is present when the -12V rail is present as the system cannot be turned on without the 3.3V stand-by voltage being present.

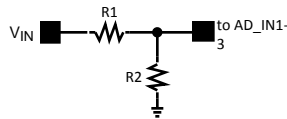
**Table 3-1. Voltage vs Register Reading**

| Pin     | Normal Use | Nominal Voltage <sup>(1)</sup> | Register Reading at Nominal Voltage | Maximum Voltage | Register Reading at Maximum Voltage | Minimum Voltage | Register Reading at Minimum Voltage | Absolute Maximum Range        |
|---------|------------|--------------------------------|-------------------------------------|-----------------|-------------------------------------|-----------------|-------------------------------------|-------------------------------|
| AD_IN1  | +12V1      | 0.927V                         | C0h                                 | 1.236V          | FFh                                 | 0V              | 00h                                 | -0.3V to ( $V_{DD} + 0.05V$ ) |
| AD_IN2  | +12V2      | 0.927V                         | C0h                                 | 1.236V          | FFh                                 | 0V              | 00h                                 | -0.3V to ( $V_{DD} + 0.05V$ ) |
| AD_IN3  | +12V3      | 0.927V                         | C0h                                 | 1.236V          | FFh                                 | 0V              | 00h                                 | -0.3V to ( $V_{DD} + 0.05V$ ) |
| AD_IN4  | FSB_Vtt    | 1.20V                          | C0h                                 | 1.60V           | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN5  | 3GIO       | 1.5V                           | C0h                                 | 2V              | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN6  | ICH_Core   | 1.5V                           | C0h                                 | 2V              | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN7  | Vccp1      | 1.20V                          | C0h                                 | 1.60V           | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN8  | Vccp2      | 1.20V                          | C0h                                 | 1.60V           | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN9  | +3.3V      | 3.30V                          | C0h                                 | 4.40V           | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN10 | +5V        | 5.0V                           | C0h                                 | 6.667V          | FAh                                 | 0V              | 00h                                 | -0.3V to +6.5V                |
| AD_IN11 | SCSI_Core  | 2.5V                           | C0h                                 | 3.333V          | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN12 | Mem_Core   | 1.969V                         | C0h                                 | 2.625V          | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN13 | Mem_Vtt    | 0.984V                         | C0h                                 | 1.312V          | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN14 | Gbit_Core  | 0.984V                         | C0h                                 | 1.312V          | FFh                                 | 0V              | 00h                                 | -0.3V to +6.0V                |
| AD_IN15 | -12V       | 0.309V                         | 40h                                 | 1.236V          | FFh                                 | 0V              | 00h                                 | -0.3V to ( $V_{DD} + 0.05V$ ) |
| AD_IN16 | +3.3V S/B  | 3.3V                           | C0h                                 | 3.6V            | D1h                                 | 3.0V            | A Eh                                | -0.3V to +6.0V                |

(1) **Application Note:** The nominal voltages listed in this table are only typical values. Voltage rails with different nominal voltages can be monitored, but the register reading at the nominal value is no longer C0h. For example, a Mem\_Core rail at 2.5V nominal could be monitored with AD\_IN12, or a Mem\_Vtt rail at 1.2V could be monitored with AD\_IN13.

### 3.5 RECOMMENDED EXTERNAL SCALING RESISTORS FOR +12V POWER RAILS

The +12V inputs require external scaling resistors. The resistors need to scale 12V down to 0.927V.



**Figure 3-1. Required External Scaling Resistors for +12V Power Input**

To calculate the required ratio of R1 to R2 use this equation:

$$\frac{R1}{R2} = \frac{12}{0.927} - 1 = 11.04498 \quad (1)$$

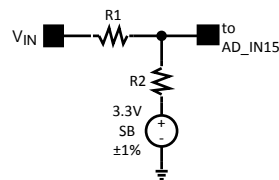
It is recommended that the equivalent thevenin resistance of the divider be between 1k and 7k to minimize errors caused by leakage currents at extreme temperatures. The best values for the resistors are: R1=13.7 kΩ and R2=1.15 kΩ. This yields a ratio of 11.94498, which has a +0.27% deviation from the theoretical. It is also recommended that the resistors have ±1% tolerance or better.

Each LSB in the voltage value registers has a weight of  $12V / 192 = 62.5$  mV. To calculate the actual voltage of the +12V power input, use the following equation:

$$V_{IN} = (8\text{-bit value register code}) \times (62.5 \text{ mV}) \quad (2)$$

### 3.6 RECOMMENDED EXTERNAL SCALING CIRCUIT FOR -12V POWER INPUT

The -12V input requires external resistors to level shift the nominal input voltage of -12V to +0.309V.



**Figure 3-2. Required External Level Shifting Resistors for -12V Power Input**

The +3.3V standby voltage is used as a reference for the level shifting. Therefore, the tolerance of this voltage directly effects the accuracy of the -12V reading. To minimize ratio errors, a tolerance of better than ±1% should be used. It is recommended that the equivalent thevenin resistance of the divider is between 1k and 7k to minimize errors caused by leakage currents at extreme temperatures. To calculate the ratio of R1 to R2 use this equation:

$$\frac{R1}{R2} = \frac{(V_{IN} - V_{REF})}{(AD\_IN - V_{REF})} - 1 \quad (3)$$

where  $V_{IN}$  is the nominal input voltage of -12V,  $V_{REF}$  is the reference voltage of +3.3V and AD\_IN is the voltage required at the AD input for a ¼ scale reading or 0.309V.

Therefore, for this case:

$$\frac{R1}{R2} = \frac{(-12 - 3.3)}{(0.309 - 3.3)} - 1 = 4.11535 \quad (4)$$

Using standard 1% resistor values for R1 of 5.76 kΩ and R2 of 1.4 kΩ yields an R1 to R2 ratio of 4.1143.

The input voltage  $V_{IN}$  can be calculated using the value register reading (VR) using this equation:

$$V_{IN} = \frac{R1}{R2} \left( \left( \frac{VR}{256} \right) - 3.3V \right) + 3.3V$$

$$= (24.69 \text{ mV} \times VR) - 13.5771V$$

(5)

The table below summarizes the theoretical voltage values for value register readings near -12V.

| Value Register | V <sub>IN</sub> | % Δ from -12V |
|----------------|-----------------|---------------|
| 15             | -13.2068        | -10.0563      |
| 16             | -13.1821        | -9.8505       |
| 17             | -13.1574        | -9.6448       |
| 18             | -13.1327        | -9.4390       |
| 19             | -13.1080        | -9.2332       |
| 20             | -13.0833        | -9.0275       |
| 21             | -13.0586        | -8.8217       |
| 22             | -13.0339        | -8.6159       |
| 23             | -13.0092        | -8.4101       |
| 24             | -12.9845        | -8.2044       |
| 25             | -12.9598        | -7.9986       |
| 26             | -12.9351        | -7.7928       |
| 27             | -12.9104        | -7.5871       |
| 28             | -12.8858        | -7.3813       |
| 29             | -12.8611        | -7.1755       |
| 30             | -12.8364        | -6.9698       |
| 31             | -12.8117        | -6.7640       |
| 32             | -12.7870        | -6.5582       |
| 33             | -12.7623        | -6.3524       |
| 34             | -12.7376        | -6.1467       |
| 35             | -12.7129        | -5.9409       |
| 36             | -12.6882        | -5.7351       |
| 37             | -12.6635        | -5.5294       |
| 38             | -12.6388        | -5.3236       |
| 39             | -12.6141        | -5.1178       |
| 40             | -12.5894        | -4.9121       |
| 41             | -12.5648        | -4.7063       |
| 42             | -12.5401        | -4.5005       |
| 43             | -12.5154        | -4.2947       |
| 44             | -12.4907        | -4.0890       |
| 45             | -12.4660        | -3.8832       |
| 46             | -12.4413        | -3.6774       |
| 47             | -12.4166        | -3.4717       |
| 48             | -12.3919        | -3.2659       |
| 49             | -12.3672        | -3.0601       |
| 50             | -12.3425        | -2.8544       |
| 51             | -12.3178        | -2.6486       |
| 52             | -12.2931        | -2.4428       |
| 53             | -12.2684        | -2.2370       |
| 54             | -12.2438        | -2.0313       |
| 55             | -12.2191        | -1.8255       |
| 56             | -12.1944        | -1.6197       |

| Value Register | V <sub>IN</sub> | % Δ from -12V |
|----------------|-----------------|---------------|
| 57             | -12.1697        | -1.4140       |
| 58             | -12.1450        | -1.2082       |
| 59             | -12.1203        | -1.0024       |
| 60             | -12.0956        | -0.7967       |
| 61             | -12.0709        | -0.5909       |
| 62             | -12.0462        | -0.3851       |
| 63             | -12.0215        | -0.1793       |
| 64             | -11.9968        | 0.0264        |
| 65             | -11.9721        | 0.2322        |
| 66             | -11.9474        | 0.4380        |
| 67             | -11.9228        | 0.6437        |
| 68             | -11.8981        | 0.8495        |
| 69             | -11.8734        | 1.0553        |
| 70             | -11.8487        | 1.2610        |
| 71             | -11.8240        | 1.4668        |
| 72             | -11.7993        | 1.6726        |
| 73             | -11.7746        | 1.8784        |
| 74             | -11.7499        | 2.0841        |
| 75             | -11.7252        | 2.2899        |
| 76             | -11.7005        | 2.4957        |
| 77             | -11.6758        | 2.7014        |
| 78             | -11.6511        | 2.9072        |
| 79             | -11.6264        | 3.1130        |
| 80             | -11.6018        | 3.3188        |
| 81             | -11.5771        | 3.5245        |
| 82             | -11.5524        | 3.7303        |
| 83             | -11.5277        | 3.9361        |
| 84             | -11.5030        | 4.1418        |
| 85             | -11.4783        | 4.3476        |
| 86             | -11.4536        | 4.5534        |
| 87             | -11.4289        | 4.7591        |
| 88             | -11.4042        | 4.9649        |
| 89             | -11.3795        | 5.1707        |
| 90             | -11.3548        | 5.3765        |
| 91             | -11.3301        | 5.5822        |
| 92             | -11.3054        | 5.7880        |
| 93             | -11.2807        | 5.9938        |
| 94             | -11.2561        | 6.1995        |
| 95             | -11.2314        | 6.4053        |
| 96             | -11.2067        | 6.6111        |
| 97             | -11.1820        | 6.8168        |
| 98             | -11.1573        | 7.0226        |
| 99             | -11.1326        | 7.2284        |
| 100            | -11.1079        | 7.4342        |
| 101            | -11.0832        | 7.6399        |
| 102            | -11.0585        | 7.8457        |
| 103            | -11.0338        | 8.0515        |
| 104            | -11.0091        | 8.2572        |
| 105            | -10.9844        | 8.4630        |

| Value Register | V <sub>IN</sub> | % Δ from -12V |
|----------------|-----------------|---------------|
| 106            | -10.9597        | 8.6688        |
| 107            | -10.9351        | 8.8745        |
| 108            | -10.9104        | 9.0803        |
| 109            | -10.8857        | 9.2861        |
| 110            | -10.8610        | 9.4919        |
| 111            | -10.8363        | 9.6976        |
| 112            | -10.8116        | 9.9034        |
| 113            | -10.7869        | 10.1092       |

### 3.7 DYNAMIC V<sub>CCP</sub> MONITORING USING VID

The AD\_IN7 (CPU1 V<sub>CCP</sub>) and AD\_IN8 (CPU2 V<sub>CCP</sub>) inputs are dynamically monitored using the P1\_VIDx and P2\_VIDx inputs to determine the limits. The dynamic comparisons operate independently of the static comparisons which use the statically programmed limits.

According to the VRM/VRD 10 specification when a VID signal is ramping to a new value, it steps by one LSB at a time, and one step occurs every 5 μs. In worse case, up to 20 steps may occur at once over 100 μs. The V<sub>CCP</sub> voltage from the VRD has to settle to the new value within 50 μs of the last VID change. The LM93 expects that the VID changes will not occur more frequently than every 5 μs.

The VID signal can be changed by the processor under program control, by internal thermal events or by external control, like force  $\overline{\text{PROCHOT}}$ .

The reference voltages selected by each value of the 6 bit VID can be found in the VRM/VRD 10 spec. Transient VID values caused by line-to-line skew are ignored by the LM93. See the VRM/VRD 10 spec for the worst case line-to-line skew.

The LM93 averages the VID values over a sampling window to determine the average voltage that the VID input was indicating during the sampling window. At the completion of a voltage conversion cycle the LM93 performs limit comparisons based on average VID values and not instantaneous values. The upper limit is determined by adding the upper limit offset to the average voltage indicated by VID. The lower limit is determined by subtracting the lower limit offset from average voltage indicated by VID. If the AD\_IN7 (or AD\_IN8) voltage falls outside the upper and lower limits, an error event is generated. Dynamic and static comparisons are performed once every 100 ms. The averaging time interval is 1.5 ms.

If at any time during the V<sub>CCP</sub> sampling window, the VID code indicates that the VRD should turn off its output, the dynamic V<sub>CCP</sub> checking is disabled for that sample.

The comparison accuracy is ±25 mV, therefore the comparison limits must be set to include this error. Since the V<sub>CCP</sub> voltage may be in the process of settling to a new value (due to a VID change), this settling should be taken into account when setting the upper and lower limit offsets.

The LM93 has a limitation on the upper limit voltage for dynamic V<sub>CCP</sub> checking. The upper limit cannot exceed 1.5875V. If the sum of the voltage indicated by VID and the upper offset voltage exceed 1.5875, the upper limit checking is disabled.

### 3.8 V<sub>REF</sub> OUTPUT

V<sub>REF</sub> is a fixed voltage to be used by an external VRD or as a voltage reference input for the BMC A/D inputs. V<sub>REF</sub> is 2.5V ±1%. There is internal current limit protection for the V<sub>REF</sub> output in case it gets shorted to supply or ground accidentally.

### 3.9 $\overline{\text{PROCHOT}}$ BACKGROUND INFORMATION

$\overline{\text{PROCHOT}}$  is an output from a processor that indicates that the processor has reached a predetermined temperature trip point. At this trip point the processor can be programmed to lower its internal operating frequency and/or lower its supply voltage by changing the value of the 6 bit VID that it supplies to the VRD. The final VID setting and the rate at which it transitions to the new VID is programmable within the processor.

If  $\overline{\text{PROCHOT}}$  is 100% throttled, it does not mean that the CPU is not executing, but it may mean that the CPU is about to encounter a thermal trip if the processor temperature continues to rise.

$\overline{\text{PROCHOT}}$  is also an input to some processors so that an external controller can force a thermal throttle based on external events.

$\overline{\text{PROCHOT}}$  is no longer asserted by the processor when the temperature drops below the predefined thermal trip point.

Oscillation around the trip point is avoided by the processor by requiring that the temperature be above/below the trip point for a predetermined period of time. A counter inside the processor is used to track this time and it has to be incremented to a max count for an above temperature trip and decremented to zero when below the trip temperature setting, to remove the trip.

The minimum time for  $\overline{\text{PROCHOT}}$  assertion is time dependant on the FSB frequency. The minimum time that the processor asserts  $\overline{\text{PROCHOT}}$  is estimated to be 187  $\mu\text{s}$ .

### 3.10 $\overline{\text{PROCHOT}}$ MONITORING

$\overline{\text{PROCHOT}}$  monitoring applies to both the  $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$  inputs. Both inputs are monitored in the same fashion, but the following description discusses a single monitor. ( $\overline{\text{Px\_PROCHOT}}$  represents both  $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$ ).

$\overline{\text{PROCHOT}}$  monitoring is meant to achieve two goals. One goal is to measure the percentage of time that  $\overline{\text{PROCHOT}}$  is asserted over a programmable time period. The result of this measurement can be read from an 8-bit register where one LSB equals 1/256th of the  $\overline{\text{PROCHOT}}$  Time Interval (0.39%). The second goal is to have a status register that indicates, as a coarse percentage, the amount of time a processor has been throttled. This second goal is required in order to communicate information over the NIC using ASF, i.e. status can be sent, not values.

To achieve the first goal, the  $\overline{\text{PROCHOT}}$  input is monitored over a period of time as defined by the  $\overline{\text{PROCHOT}}$  Time Interval Register. At the end of each time period, the 8-bit measurement is transferred to the Current  $\overline{\text{Px\_PROCHOT}}$  register. Also at the end of each measurement period, the Current  $\overline{\text{Px\_PROCHOT}}$  register value is moved to the Average  $\overline{\text{Px\_PROCHOT}}$  register by adding the new value to the old value and dividing the result by 2. Note that the value that is averaged into the Average  $\overline{\text{Px\_PROCHOT}}$  register is not the new measurement but rather the previous measurement. If the SMBus writes to the Current  $\overline{\text{P1\_PROCHOT}}$  (or Current  $\overline{\text{P2\_PROCHOT}}$ ) register, the capture cycle restarts for both monitoring channels ( $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$ ). Also note, that a strict average of two 8-bit values may result in Average  $\overline{\text{Px\_PROCHOT}}$  reflecting a value that is one LSB lower than the Current  $\overline{\text{Px\_PROCHOT}}$  in steady state.

It should be noted that the 8-bit result has a positive bias of one half of an LSB. This is necessary because a value of 00h represents that  $\overline{\text{Px\_PROCHOT}}$  was not asserted at all during the sampling window. Any amount of throttling results in a reading of 01h.

The following table demonstrates the mapping for the 8-bit result:



| 8-Bit Result | Percentage Thottled         |
|--------------|-----------------------------|
| 0            | Exactly 0%                  |
| 1            | Between 0% and 0.39%        |
| 2            | Between 0.39% and 0.78%     |
| ~            | ~                           |
| n            | Between (n-1)/256 and n/256 |
| ~            | ~                           |
| 253          | Between 98.4% and 98.8%     |
| 254          | Between 98.8% and 99.2%     |
| 255          | Greater than 99.2%          |

To achieve the second goal, the LM93 has several comparators that compare the measured percentage reading against several fixed and 1 variable value. The variable value is user programmable.

The result of these comparisons generates several error status bits described in the following table:

| Status Description                               | Comparison Formula                                        |
|--------------------------------------------------|-----------------------------------------------------------|
| 100% Throttle                                    | PROCHOT was never de-asserted during monitoring interval. |
| Greater than or equal to 75% and less than 100%  | $193 \leq \text{measured value and not } 100\%$           |
| Greater than or equal to 50% and less than 75%   | $129 \leq \text{measured value} < 193$                    |
| Greater than or equal to 25% and less than 50%   | $65 \leq \text{measured value} < 129$                     |
| Greater than or equal to 12.5% and less than 25% | $33 \leq \text{measured value} < 65$                      |
| Greater than 0% and less than 12.5%              | $0 < \text{measured value} < 33$                          |
| Greater than 0%                                  | $0 < \text{measured value}$                               |
| Greater than user limit                          | $\text{user limit} < \text{measured value}$               |

These status bits are reflected in the  $\overline{\text{PROCHOT}}$  Error Status Registers. Each of the  $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$  inputs is monitored independently, and each has its own set of status registers.

In S3 and S4/5 sleep states, the  $\overline{\text{PROCHOT}}$  Monitoring function does not run. The Current  $\overline{\text{Px\_PROCHOT}}$  registers are reset to 00h and the Average  $\overline{\text{Px\_PROCHOT}}$  registers hold their current state. Once the sleep state changes back to S0, the monitoring function is restarted. After the first  $\overline{\text{PROCHOT}}$  measurement has been made, the measurement is written directly into the Current and Average  $\overline{\text{Px\_PROCHOT}}$  registers without performing any averaging. Averaging returns to normal on the second measurement.

### 3.11 $\overline{\text{PROCHOT}}$ OUTPUT CONTROL

In some cases, it is necessary for the LM93 to drive the  $\overline{\text{Px\_PROCHOT}}$  outputs low. There are several conditions that cause this to happen.

The LM93 can be told to logically short the two  $\overline{\text{PROCHOT}}$  inputs together. When this is done, the LM93 monitors each of the  $\overline{\text{Px\_PROCHOT}}$  inputs. If any external device asserts one of the  $\overline{\text{PROCHOT}}$  signals, the LM93 responds by asserting the other  $\overline{\text{PROCHOT}}$  signal until the first  $\overline{\text{PROCHOT}}$  signal is de-asserted. This feature should never be enabled if the  $\overline{\text{PROCHOT}}$  signals are already being shorted by another means.

Whenever one of the  $\overline{\text{VRDx\_HOT}}$  inputs is asserted, the corresponding  $\overline{\text{Px\_PROCHOT}}$  pins are asserted by the LM93. The response time is less than 10  $\mu\text{s}$ . When the  $\overline{\text{VRDx\_HOT}}$  input is de-asserted, the  $\overline{\text{Px\_PROCHOT}}$  pin is no longer asserted by the LM93. If the LM93 is configured to short the  $\overline{\text{PROCHOT}}$  signals together, it always asserts them together whenever either of the  $\overline{\text{VRDx\_HOT}}$  inputs is asserted.

Software can manually program the LM93 to drive a PWM type signal onto  $\overline{\text{P1\_PROCHOT}}$  or  $\overline{\text{P2\_PROCHOT}}$ . This is done via the  $\overline{\text{PROCHOT}}$  Override register. See the description of this register for more details. Once again, if the LM93 is configured to short the  $\overline{\text{PROCHOT}}$  signals together, it always asserts them together whenever this function is enabled.

### 3.12 FAN SPEED MEASUREMENT

The fan tach circuitry measures the period of the fan pulses by enabling a counter for two periods of the fan tach signal. The accumulated count is proportional to the fan tach period and inversely proportional to the fan speed. All four fan tach signals are measured within 1 second.

Fans in general do not over-speed if run from the correct voltage, so the failure condition of interest is under speed due to electrical or mechanical failure. For this reason only low-speed limits are programmed into the limit registers for the fans. It should be noted that, since fan period rather than speed is being measured, a fan tach error event occurs when the measurement *exceeds* the limit value.

### 3.13 SMART FAN SPEED MEASUREMENT

If a fan is driven using a low-side drive PWM, the tachometer output of the fan is corrupted. The LM93 includes smart tachometer circuitry that allows an accurate tachometer reading to be achieved despite the signal corruption. In smart tach mode all four signals are measured within 4 seconds.

A smart tach capture cycle works according to the following steps:

1. Both PWM outputs are synchronized such that they activate simultaneously.
2. Both PWM output active times are extended for up to 50 ms.
3. The number of tach signal periods during the 50 ms interval are tracked:
  - (a) If less than 1 period is sensed during the 50 ms extension the result returned is 3FFh.
  - (b) After one period occurs the count for that period is memorized.
  - (c) If during the 50 ms interval 2 periods do not occur, the tach value reported is the 1 period count multiplied by 2.
  - (d) If 2 periods do occur, the 2 period count is loaded into the value register and the 50 ms PWM extension is terminated.

The lowest two bits in each of the Fan Tach value registers are reserved. The smart tach feature takes advantage of these bits. In normal tach mode, these bits return 00. In smart tach mode the two bits determine the accuracy level of the reading. 11 is most accurate (2 periods used) and 10 is the least accurate (1 period used). If less than 1 period occurred during the measurement cycle, the lower two bits are set to 10.

In smart fan tach mode, the TACH\_EDGE field is honored in the LM93 Status/Control register. If only one edge type is active, the measurement always uses that edge type (rising or falling). If both are active, the measurement uses whichever edge type occurs first.

Typically the minimum RPM captured by smart fan tach mode is 900 RPM for a fan that produces two pulses per revolution at about 50% duty cycle.

### 3.14 Inputs/Outputs

Besides all the pins associated with sensor inputs the LM93 has several pins that are assigned for other specific functions.

### 3.14.1 $\overline{\text{ALERT}}$ OUTPUT

The  $\overline{\text{ALERT}}$  output is an active-low open drain output signal. The  $\overline{\text{ALERT}}$  output is used to signal a micro-controller that one or more sensors have crossed their corresponding limit thresholds. This is generally not a fatal event unless the micro-controller decides it to be.

If enabled, the  $\overline{\text{ALERT}}$  output is asserted whenever any bit in any BMC Error Status register is set (with the exception of the fixed  $\overline{\text{PROCHOT}}$  threshold bits). By definition, when  $\overline{\text{ALERT}}$  is enabled, it always matches the inverse of the BMC\_ERR bit in the LM93 Status/Control register. When the  $\overline{\text{ALERT}}$  output is disabled, an alert event can still be determined by reading the state of the BMC\_ERR bit.

The  $\overline{\text{ALERT}}$  functions like an interrupt. The LM93 does not support the SMBus ARA (Alert Response Address) protocol.

$\overline{\text{ALERT}}$  is only de-asserted when there are no error status bits set in any BMC Error Status registers. Alternatively, software can disable the  $\overline{\text{ALERT}}$  output to cause it to de-assert. The  $\overline{\text{ALERT}}$  output re-asserts once enabled if any BMC Error Status register bits are still set.

Further information on how the  $\overline{\text{ALERT}}$  output behaves can be found in [MASKING, ERROR STATUS AND ALERT](#).

### 3.14.2 $\overline{\text{RESET}}$ INPUT/OUTPUT

This pin acts as an active low reset output when power is applied to the LM93. It is asserted when the LM93 first sees a voltage that exceeds the internal POR level on its +3.3V S/B  $V_{DD}$  input. The internal registers of the LM93 are reset to their defaults when power is applied.

After this reset has completed, the  $\overline{\text{RESET}}$  pin becomes an input. When an external device asserts  $\overline{\text{RESET}}$ , the LM93 clears the LOCK bit in the LM93 Configuration register. This feature allows critical registers to be locked and provides a controlled mechanism to unlock them.

Asserting  $\overline{\text{RESET}}$  externally causes the Sleep State Control register to be automatically set to S4/5. This causes several error events to be masked according to the S4/5 masking definitions. Refer to the [Register Descriptions](#) for more information.

### 3.14.3 PWM1 AND PWM2 OUTPUTS

The PWM outputs are used to control the speed of fans. The output signal duty cycle can automatically be controlled by the temperature of one or more temperature zones. It is also influenced by various other inputs and registers. See [FAN CONTROL](#) for further information on the behavior of the PWM outputs.

### 3.14.4 $\overline{\text{SCSI\_TERMx}}$ INPUTS

These inputs can be used to monitor the status of the electronic fuse on each of the SCSI channels. In prior implementations the reference voltage out to the terminators was measured. When LVDS SCSI was introduced this reference voltage could take on multiple voltage levels depending on the mode of the SCSI bus. Also when the SCSI terminators were disabled, the  $V_{REF}$  voltage could not be ensured. Monitoring individual terminators was also pin intensive. All of these issues caused problems that were difficult to work around so moving to monitoring the fuse was selected as the solution.

These inputs do not have to be used for monitoring SCSI fuses. Assertion of the  $\overline{\text{SCSI\_TERMx}}$  inputs to a Low sets the associated bits the status registers. Therefore, any active low signal could be connected to these pins to generate an error event.

### 3.14.5 *VRD1\_HOT AND VRD2\_HOT INPUTS*

These inputs monitor the thermal sensor associated with each processor VRD on a baseboard. When one of the inputs is activated, it indicates that the VRD has exceeded a predetermined temperature threshold. The LM93 responds by gradually increasing the duty cycle of any PWM outputs that are bound to the corresponding processor and setting the appropriate error status bits. The corresponding  $\overline{\text{PROCHOT}}$  signal is also asserted. See the [FAN CONTROL](#) and the [PROCHOT OUTPUT CONTROL](#) for more information.

### 3.14.6 *GPIO PINS*

The LM93 has 8 GPIO pins that can act as either as inputs or outputs. Each can be configured and controlled independently. When acting as an input the pin can be masked to prevent it from setting a corresponding bit in the GPI Error status registers.

### 3.14.7 *FAN TACH INPUTS*

The fan inputs are Schmitt-Trigger digital inputs. Schmitt-trigger input circuitry is included to accommodate slow rise and fall times typical of fan tachometer outputs.

The maximum input signal range is 0V to +6.0V, even when  $V_{DD}$  is less than 5V. In the event that these inputs are supplied from fan outputs, which exceed 0V to +6.0V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range, thereby preventing damage to the LM93.

Hot plugging fans can involve spikes on the Tach signals of up to 12V so diode protection or other circuitry is required. For “Hot Plug” fans, external clamp diodes may be required for signal conditioning.

## 3.15 *SMBus Interface*

The SMBus is used to communicate with the LM93. The LM93 provides the means to monitor power supplies for fan status and power failures. LM93 is designed to be tolerant to 5V signalling. Necessary pull-ups are located on the baseboard. Care should be taken to ensure that only one pull-up is used for each SMBus signal. For proper operation, the SMBus slave addresses of all devices attached to the bus must comply with those listed in this document. The SMBus interface obeys the SMBus 2.0 protocols and signaling levels.

The SMBus interface of the LM93 does not load down the SMBus if no power is applied to the LM93. This allows a module containing the LM93 to be powered down and replaced, if necessary.

### 3.15.1 *SMBUS ADDRESSING*

Each time the LM93 is powered up, it latches the assigned SMBus slave address (determined by ADDR\_SEL) during the first valid SMBus transaction in which the first five bits of the targeted slave address match those of the LM93 slave address. Once the address has been latched, the LM93 continues to use that address for all future transactions until power is lost.

The address select input detects three different voltage levels and allows for up to 3 devices to exist in a system. The address assignment is as follows:

| Address Select Pin (ADDR_SEL) | Slave Address Assignment |
|-------------------------------|--------------------------|
| High                          | 01011 01                 |
| $V_{DD}/2$                    | 01011 10                 |
| Low                           | 01011 00                 |

### 3.15.2 DIGITAL NOISE EFFECT ON SMBUS COMMUNICATION

Noise coupling into the digital lines (greater than 150mV), overshoot greater than  $V_{DD}$  and undershoot less than GND, may prevent successful SMBus communication with the LM93. SMBus No Acknowledge (NACK) is the most common symptom, causing unnecessary traffic on the bus. Although, the SMBus maximum frequency of communication is rather low (100 kHz max), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed circuit board traces. The LM93 includes on chip low-pass filtering of the SMBCLK and SMBDAT signals to make it more noise immune. Minimize noise coupling by keeping digital traces out of switching baseboard areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SMBDAT and SMBCLK lines.

### 3.15.3 GENERAL SMBUS TIMING

The SMBus 2.0 specification defines specific conditions for different types of read and write operations but in general the SMBus protocol operates as follows:

The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SMBDAT while the serial clock line SMBCLK remains high. This indicates that a data stream follows. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits. This consists of a 7-bit slave address (MSB first) plus a R/W bit, which determines the direction of the data transfer, i.e. whether data is written to or read from the slave device (0 = write, 1 = read).

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0 then the master writes to the slave device. If the R/W bit is a 1 the master reads from the slave device.

Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge bit. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.

If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction, such as telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written.

Since data can flow in only one direction as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it is necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will allow the data line to go high during the 10th clock pulse to assert a STOP condition. In READ mode, the slave drives the data not the master. For the bit in question, the slave is looking for an acknowledge and the master doesn't drive low. This is known as 'No Acknowledge'. The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Note, a repeated START may be given only between a write and read operation that are in succession.

### 3.15.4 SMBUS ERROR SAFETY FEATURES

To provide a more robust SMBus interface, the LM93 incorporates a timeout feature for both SMBCLK and SMBDAT. If either signal is low for a long period of time (see [SMBus AC Characteristics](#)), the LM93 SMBus state machine reverts to the idle state and waits for a START signal. Large block transfers of all zeros should be avoided if the SMBCLK is operating at a very low frequency to avoid accidental timeouts. Pulling the Reset pin low does not reset the SMBus state machine. If the LM93 SMBDAT pin is low during a system reset, the LM93's state machine timeouts and resets automatically. If the LM93's SMBDAT pin is high during a system reset, the first assertion of a start by the master resets the LM93's interface state machine.

Although it is a violation of the SMBus specification, in some cases a START or STOP signal occurs in the middle of a byte transfer instead of coming after an acknowledge bit. If this occurs, only a partial byte was transferred. If a byte was being written, it is aborted and the partial byte is not committed. If a byte was being read from a read-to-clear register, the register is not cleared.

### 3.15.5 SERIAL INTERFACE PROTOCOLS

The LM93 contains volatile registers, the registers occupy address locations from 00h to EFh.

Data can be read and written as a single byte, a word, or as a block of several bytes. The LM93 supports the following SMBus/I<sup>2</sup>C transactions/protocols:

- Send Byte
- Write Byte
- Write Word
- SMBus Write Block
- I<sup>2</sup>C Block Write
- Read Byte
- Read Word
- SMBus Read Block
- SMBus Block-Write Block-Read Process Call
- I<sup>2</sup>C Block Read

In addition to these transactions the LM93 supports a few extra items and also has some behavior that must be defined beyond the SMBus 2.0 specification. No other SMBus 2.0 transactions are supported (PEC, ARA etc.).

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the LM93 are discussed below. The following abbreviations are used in the diagrams:

- S — START
- P — STOP
- R — READ
- W — WRITE
- A — ACKNOWLEDGE
- /A — NO ACKNOWLEDGE

### 3.15.5.1 Address Incrementing

The established base address does not increment. Repeatedly reading without re-establishing a new base address returns data from the same address each time. I<sup>2</sup>C read transactions can use this information and skip reestablishing the base address, when only one master is used. One exception to this rule exists when a block write and block read is used to emulate a block write/read process call. This is detailed later, see the [Block Write/Read Process Call](#) description.

### 3.15.5.2 Block Command Code Summary

Block command codes control the block read and write operations of the LM93 as summarized in the following table:

| Command Code Name   | Value | Description                                                |
|---------------------|-------|------------------------------------------------------------|
| Block Write Command | F0h   | SMBus Block Write Command Code                             |
| Block Read Command  | F1h   | SMBus Block Write/Read Process Call                        |
| Fixed Block 0       | F2h   | Fixed Block Read Command Code: address 40h, size 8 bytes   |
| Fixed Block 1       | F3h   | Fixed Block Read Command Code: address 48h, size 8 bytes   |
| Fixed Block 2       | F4h   | Fixed Block Read Command Code: address 50h, size 6 bytes   |
| Fixed Block 3       | F5h   | Fixed Block Read Command Code: address 56h, size 16 bytes  |
| Fixed Block 4       | F6h   | Fixed Block Read Command Code: address 67h, size 4 bytes   |
| Fixed Block 5       | F7h   | Fixed Block Read Command Code: address 6Eh, size 8 bytes   |
| Fixed Block 6       | F8h   | Fixed Block Read Command Code: address 78h, size 12 bytes  |
| Fixed Block 7       | F9h   | Fixed Block Read Command Code: address 90h, size 32 bytes  |
| Fixed Block 8       | FAh   | Fixed Block Read Command Code: address B4h, size 8 bytes   |
| Fixed Block 9       | FBh   | Fixed Block Read Command Code: address C8h, size 8 bytes   |
| Fixed Block 10      | FCh   | Fixed Block Read Command Code: address D00h, size 16 bytes |
| Fixed Block 11      | FDh   | Fixed Block Read Command Code: address E5h, size 9 bytes   |

### 3.15.5.3 Write Operations

The LM93 supports the following SMBus write protocols.

#### 3.15.5.3.1 Write Byte

In this operation the master device sends an address byte and one data byte to the slave device, as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a command code (register address).
5. The slave asserts ACK.



6. The master sends the data byte.
7. The slave asserts ACK.
8. The master asserts a STOP condition to end the transaction.

|   |               |   |   |                  |   |           |   |   |
|---|---------------|---|---|------------------|---|-----------|---|---|
| 1 | 2             |   | 3 | 4                | 5 | 6         | 7 | 8 |
| S | Slave Address | W | A | Register Address | A | Data Byte | A | P |

### 3.15.5.3.2 Write Word

In this operation the master device sends an address byte and two data bytes to the slave device, as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a command code (register address).
5. The slave asserts ACK.
6. The master sends the low data byte.
7. The slave asserts ACK.
8. The master sends the high data byte.
9. The slave asserts ACK.
10. The master asserts a STOP condition to end the transaction.

|   |               |   |   |                  |   |               |   |                |   |    |
|---|---------------|---|---|------------------|---|---------------|---|----------------|---|----|
| 1 | 2             |   | 3 | 4                | 5 | 6             | 7 | 8              | 9 | 10 |
| S | Slave Address | W | A | Register Address | A | Data Byte Low | A | Data Byte High | A | P  |

### 3.15.5.3.3 SMBus Write Block to Any Address

The start address for a block write is embedded in this transaction. In this operation the master sends a block of data to the slave as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a command code that tells the slave device to expect a block write. The LM93 command code for a block write is F0h.
5. The slave asserts ACK.
6. The master sends a byte that tells the slave device how many data bytes it will send (N). The SMBus specification allows a maximum of 32 data bytes to be sent in a block write.
7. The slave asserts ACK.
8. The master sends data byte 1, the starting address of the block write.
9. The slave asserts ACK after each data byte.
10. The master sends data byte 2.
11. The slave asserts ACK.
12. The master continues to send data bytes and the slave asserts ACK for each byte.
13. The master asserts a STOP condition to end the transaction.



|   |               |   |   |                           |   |                |   |                             |   |             |    |  |             |   |    |
|---|---------------|---|---|---------------------------|---|----------------|---|-----------------------------|---|-------------|----|--|-------------|---|----|
| 1 | 2             |   | 3 | 4                         | 5 | 6              | 7 | 8                           | 9 | 10          | 11 |  | 12          |   | 13 |
| S | Slave Address | W | A | Command F0h (Block Write) | A | Byte Count (N) | A | Data Byte 1 (Start Address) | A | Data Byte 2 | A  |  | Data Byte N | A | P  |

**Special Notes**

1. Any attempts to write to bytes beyond normal address space are acknowledged by the LM93 but are ignored.
2. Block writes do not wrap from address FFh back to 00h the address remains at FFh.
3. The Byte Count field is ignored by the LM93. The master device may send more or less bytes and the LM93 accepts them.
4. The SMBus specification requires that block writes never exceed 32 data bytes. Meeting this requirement means that only 31 actual data bytes can be sent (the register address counts as one byte). The LM93 does not care if this requirement is met.

**3.15.5.3.4 *FC* Block Write**

In this transaction the master sends a block of data to the LM93 as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends the starting address of the block write.
5. The slave asserts ACK after each data byte.
6. The master sends data byte 1.
7. The slave asserts ACK.
8. The master continues to send data bytes and the slave asserts ACK for each byte.
9. The master asserts a STOP condition to end the transaction

|   |               |   |   |                  |   |             |   |  |             |   |   |
|---|---------------|---|---|------------------|---|-------------|---|--|-------------|---|---|
| 1 | 2             |   | 3 | 4                | 5 | 6           | 7 |  | 8           |   | 9 |
| S | Slave Address | W | A | Register Address | A | Data Byte 1 | A |  | Data Byte N | A | P |

**Special Notes:**

1. Any attempts to write to bytes beyond normal address space are acknowledged by the LM93 but are ignored.
2. Block writes do not wrap from address FFh back to 00h the address remains at FFh.

**3.15.5.4 Read Operations**

The LM93 uses the following SMBus read protocols.

**3.15.5.4.1 Read Byte**

In the LM93, the read byte protocol is used to read a single byte of data from a register. In this operation the master device receives a single byte from a slave device, as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a register address.
5. The slave asserts an ACK.
6. The master sends a Repeated START.

7. The master sends the slave address followed by the read bit (high).
8. The slave asserts an ACK.
9. The master receives a data byte and asserts a NACK.
10. The master asserts a STOP condition and the transaction ends.

|   |               |   |   |                  |   |   |               |   |   |           |    |    |
|---|---------------|---|---|------------------|---|---|---------------|---|---|-----------|----|----|
| 1 | 2             |   | 3 | 4                | 5 | 6 | 7             |   | 8 | 9         |    | 10 |
| S | Slave Address | W | A | Register Address | A | S | Slave Address | R | A | Data Byte | /A | P  |

#### 3.15.5.4.2 Read Word

In the LM93, the read word protocol is used to read two bytes of data from a register or two consecutive registers. In this operation the master device reads two bytes from a slave device, as follows:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a register address.
5. The slave asserts an ACK.
6. The master sends a Repeated START.
7. The master sends the slave address followed by the read bit (high).
8. The slave asserts an ACK.
9. The master receives the Low data byte and asserts an ACK.
10. The master receives the High data byte and asserts a NACK.
11. The master asserts a STOP condition and the transaction ends.

|   |               |   |   |                  |   |   |               |   |   |               |   |                |    |    |
|---|---------------|---|---|------------------|---|---|---------------|---|---|---------------|---|----------------|----|----|
| 1 | 2             |   | 3 | 4                | 5 | 6 | 7             |   | 8 | 9             |   | 10             |    | 11 |
| S | Slave Address | W | A | Register Address | A | S | Slave Address | R | A | Data Byte Low | A | Data Byte High | /A | P  |

#### 3.15.5.4.3 SMBus Block-Write Block-Read Process Call

This transaction is used to read a block of data from the LM93. Below is the sequence of events that occur in this transaction:

1. The master device asserts a START condition.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK.
4. The master sends a command code that tells the slave device to expect a block read (F1h) and the slave asserts ACK.
5. The master sends the Byte Count for this write which is 2 and the slave asserts ACK.
6. The master sends the Start Register Address for the block read and the slave asserts the ACK.
7. The master sends the Byte Count (1-32) for the block read processes call and the slave asserts ACK.
8. The master asserts a repeat START condition.
9. The master sends the 7-bit slave address followed by the read bit (high).
10. The slave asserts ACK.
11. The master receives a byte count data byte that tells it how many data bytes will received. This field reflects the number of bytes requested by the Byte Count transmitted to the LM93. The SMBus specification allows a maximum of 32 data bytes to be received in a block read. Then master asserts ACK.

12. The master receives byte 1 and then asserts ACK.
13. The master receives byte 2 and then asserts ACK.
14. The master receives N-3 data bytes, and asserts ACK for each one.
15. The master receives data byte N and asserts a NACK.
16. The master asserts a STOP condition to end the transaction.

|   |                        |   |   |                               |   |                 |   |                        |   |                        |   |    |               |   |    |  |
|---|------------------------|---|---|-------------------------------|---|-----------------|---|------------------------|---|------------------------|---|----|---------------|---|----|--|
| 1 | 2                      |   | 3 | 4                             |   | 5               |   | 6                      |   | 7                      |   | 8  | 9             |   | 10 |  |
| S | Slave Address          | W | A | Block Read Command Code (F1h) | A | Byte Count (2h) | A | Start Register Address | A | Byte Count (1–20h) (N) | A | S  | Slave Address | R | A  |  |
|   | 11                     |   |   | 12                            |   | 13              |   | 14                     |   | 15                     |   | 15 | 16            |   |    |  |
|   | Byte Count (1–20h) (N) |   | A | Data Byte 1                   | A | Data Byte 2     | A |                        |   | Data Byte N            |   | /A | P             |   |    |  |

**Special Notes:**

1. The LM93 returns 00h when address locations outside of normal address space are read.
2. Block reads do not wrap around from address FFh to 00h
3. If the master acknowledges more bytes than it requested, the LM93 continues to supply data until the master does not acknowledge a byte.
4. If the master does not acknowledge a byte to prematurely abort a block read, the LM93 gets off the bus to allow the master to issue a STOP signal.

**3.15.5.4.4 Simulated SMBus Block-Write Block-Read Process Call**

Alternatively, if the master cannot support an SMBus Block-Write Block-Read process call, it can be emulated by two transactions (a block write followed by a block read). This should only be done in a single master system, since in a dual master system collisions can occur that corrupt the data and transaction. Below is the sequence of events for these transactions:

1. The master issues a START to start this transaction.
2. The master sends the 7-bit slave address followed by a write bit (low).
3. The slave asserts the ACK.
4. The master sends the Block Read command code (F1h) and the slave asserts the ACK.
5. The master sends the Byte Count (2h) for this transaction and the slave asserts the ACK.
6. The master sends the Start Register Address and the slave asserts the ACK.
7. The master sends the Byte Count (1-20h) for the Block-Read Process Call and the slave asserts the ACK.
8. The master sends a STOP to end this transaction.
9. The master sends a START to start this transaction.
10. The master sends the 7-bit slave address followed by a write bit (low) and the slave asserts the ACK.
11. The master sends the Block Read Command code (F1h) and the slave asserts the ACK.
12. The master sends a repeat START.
13. The master sends the 7-bit slave address followed by a read bit (high) and the slave asserts the ACK.
14. The master receives Byte Count (this matches the size sent by the master in step 7) and asserts the ACK.
15. The master receives Data Byte 1 and asserts the ACK.
16. The master receives Data Byte 2 and asserts the ACK.
17. The master receives N-3 data bytes, and asserts ACK for each one.

18. The master receives the last data byte and asserts a NACK.
19. The master issues a STOP to end this transaction.

|   |                               |   |    |                               |   |                 |   |                        |   |                        |   |             |   |               |             |    |    |
|---|-------------------------------|---|----|-------------------------------|---|-----------------|---|------------------------|---|------------------------|---|-------------|---|---------------|-------------|----|----|
| 1 | 2                             |   | 3  | 4                             |   | 5               |   | 6                      |   | 7                      |   | 8           | 9 | 10            |             |    |    |
| S | Slave Address                 | W | A  | Block Read Command Code (F1h) | A | Byte Count (2h) | A | Start Register Address | A | Byte Count (1–20h) (N) | A | P           | S | Slave Address | W           | A  |    |
|   | 11                            |   | 12 | 13                            |   |                 |   | 14                     |   | 15                     |   | 16          |   |               |             | 17 | 16 |
|   | Block Read Command Code (F1h) | A | S  | Slave Address                 | R | A               |   | Byte Count (1–20h) (N) | A | Data Byte 1            | A | Data Byte 2 | A |               | Data Byte N | /A | P  |

#### Special Notes:

1. Steps 9 through 19 can be repeated to read another block of data. The address auto-increments such that the next block starts where the last block left off. The size returned by the LM93 is the same each time.
2. The LM93 returns 00h when address locations outside of normal address space are read.
3. Block reads do not wrap around from address FFh to 00h
4. If the master acknowledges more bytes than it requested, the LM93 continues to supply data until the master does not acknowledge a byte.
5. If the master does not acknowledge a byte to prematurely abort a block read, the LM93 gets off the bus to allow the master to issue a STOP signal.
6. After a block read is finished, the base address of the LM93 is updated to point to the byte just beyond the last byte read.

#### 3.15.5.4.5 SMBus Fixed Address Block Reads

Block reads can be performed from pre-defined addresses. A special command code has been reserved for each pre-defined address. See the [Block Command Code Summary](#) for more details on the command codes. Below is the sequence of events that occur for this type of block read:

1. The master sends a START to start this transaction.
2. The master sends the 7-bit slave address followed by a write bit (low).
3. The slave asserts an ACK.
4. The master sends a Fixed Block Command Code (F2h-FDh) and the slave asserts an ACK.
5. The master sends a repeated START.
6. The master sends the 7-bit slave address followed by a read bit (high).
7. The slave asserts an ACK.
8. The master receives the Byte Count (depends on the Fixed Block Command Code used) and asserts an ACK.
9. The master receives the first data byte and asserts an ACK.
10. The master continues to receive data bytes and asserting an ACK.
11. The master receives the last data byte.
12. The master asserts a NACK.
13. The master issues a STOP to end this transaction.

|   |               |   |   |                                    |   |   |               |   |   |                |   |             |   |    |             |    |    |
|---|---------------|---|---|------------------------------------|---|---|---------------|---|---|----------------|---|-------------|---|----|-------------|----|----|
| 1 | 2             |   | 3 | 4                                  |   | 5 | 6             |   | 7 | 8              |   | 9           |   | 10 | 11          | 12 | 13 |
| S | Slave Address | W | A | Fixed Block Command Code (F2h–FDh) | A | S | Slave Address | R | A | Byte Count (N) | A | Data Byte 1 | A |    | Data Byte N | /A | P  |

**Special Notes:**

1. The LM93 returns 00h when address locations outside of normal address space are read.
2. Block reads do not wrap around from address FFh to 00h.
3. If the master acknowledges more bytes that it requested, the LM93 continues to supply data until the master does not acknowledge a byte.
4. If the master does not acknowledge a byte to prematurely abort a block read, the LM93 gets off the bus to allow the master to issue a STOP signal.

**3.15.5.4.6 I<sup>2</sup>C Block Reads**

The LM93 supports I<sup>2</sup>C block reads. The following sequence of events occur in this transaction:

1. The master sends a START to start this transaction .
2. The master send 7-bit slave address followed by a write bit (low).
3. The slave asserts an ACK.
4. The master sends the register address and the slave asserts an ACK.
5. The master sends a repeated START.
6. The master sends the 7-bit slave address followed by a read bit (high).
7. The slave asserts an ACK.
8. The master receives Data Byte 1 and asserts an ACK.
9. The master continues to receive bytes and asserting an ACK for each byte received.
10. The master receives the last byte.
11. The master asserts a NACK.
12. The master issues a STOP.

|   |               |   |   |                  |   |   |               |   |   |             |   |             |   |    |             |    |   |
|---|---------------|---|---|------------------|---|---|---------------|---|---|-------------|---|-------------|---|----|-------------|----|---|
| 1 | 2             |   | 3 | 4                |   | 5 | 6             |   | 7 | 8           |   | 9           |   | 10 | 11          | 12 |   |
| S | Slave Address | W | A | Register Address | A | S | Slave Address | R | A | Data Byte 1 | A | Data Byte 2 | A |    | Data Byte N | /A | P |

**Special Notes:**

1. The LM93 returns 00h when address locations outside of normal address space are read.
2. Block reads do not wrap around from address FFh to 00h.
3. If the master acknowledges more bytes that it requested, the LM93 continues to supply data until the master does not acknowledge a byte.
4. If the master does not acknowledge a byte to prematurely abort a block read, the LM93 gets off the bus to allow the master to issue a STOP signal.

**3.15.6 READING AND WRITING 16-BIT REGISTERS**

Whenever the low byte of a 16-bit register is read, the high byte is frozen. After the high byte is read, it is unfrozen. This ensures that the entire 16-bit value is read properly and the high byte matches with the low byte. If the low byte of a different 16-bit register is read, the currently frozen high byte is unfrozen and the high byte of the new 16-bit register is frozen. In a system with two SMBus masters, it is very important that only one master reads any 16-bit registers at a time. One possible method to achieve this would involve using 16-bit SMBus reads (instead of two separate 8-bit reads) to read 16-bit registers.

Whenever the low byte of a 16-bit register is written, the write is buffered and does not take effect until the corresponding high byte is written. If the low byte of a different 16-bit register is written, the previously buffered low byte of the first register is discarded. If a device attempts to write the high byte of a 16-bit register, and the corresponding low byte was not written (or was discarded), then the LM93 will NACK the byte.

### 3.16 Using The LM93

#### 3.16.1 POWER ON

The LM93 generates a power on reset signal on  $\overline{\text{RESET}}$  when power is applied for the first time to the part.

#### 3.16.2 RESETS

Upon power up, the  $\overline{\text{RESET}}$  output is asserted when the voltage on the power supply crosses the power-on-reset threshold level (see [Electrical Specifications](#)). The  $\overline{\text{RESET}}$  output is open-drain and should be used with an external pull-up resistor connected to  $V_{DD}$ . Once the power on reset has completed, the  $\overline{\text{RESET}}$  pin becomes an input and when asserted causes the LOCK bit in the LM93 Configuration register to be cleared. In addition, assertion of  $\overline{\text{RESET}}$  causes the sleep control register to be automatically set to S4/S5. This causes several error events to be masked according to the S4/S5 masking definitions.

| Register Types              | Power On Reset | External Reset |
|-----------------------------|----------------|----------------|
| Factory regs                | x              |                |
| BMC Error Status regs       | x              |                |
| Host Error Status regs      | x              |                |
| Value regs                  |                |                |
| Limit regs                  | x              |                |
| Setup regs                  | x              |                |
| LM93 Configuration Lock Bit | x              | x              |
| LM93 Configuration GMSK Bit | x (reset)      | x (set)        |
| Sleep Mask                  | x              |                |
| Sleep State Control         |                | x              |
| Other Mask regs             | x              |                |

All other registers are not effected by power on reset or external reset.

#### 3.16.3 ADDRESS SELECTION

LM93 is designed to be used primarily in dual processor server systems that may require only one monitoring device.

If multiple LM93 devices are implemented in a system, they must have unique SMBus slave addresses. See the [SMBUS ADDRESSING](#) for more information.

The board designer may apply a 10 k $\Omega$  pull-down and/or pull-up resistors to ground and/or to 3.3V SB  $V_{DD}$  on the ADDR\_SEL pin. The LM93 is designed to work with resistors of 5% tolerance for the case where two resistors are required. Upon the first SMBus communication to the part, the LM93 assigns itself an SMBus address according to the ADDR\_SEL input.

| Address Select               | Board Implementation                                          | SMBus Address |
|------------------------------|---------------------------------------------------------------|---------------|
| less-than 10% of $V_{DD}$    | Pulled to ground through a 10 k $\Omega$ resistor             | 0101,100b     |
| $\approx V_{DD}/2$           | 10 k $\Omega$ (5%) Resistor to 3.3V SB $V_{DD}$ and to Ground | 0101,110b     |
| greater-than 90% of $V_{DD}$ | Pulled to 3.3V SB $V_{DD}$ through a 10 k $\Omega$ resistor   | 0101,101b     |

### 3.16.4 DEVICE SETUP

BIOS executes the following steps to configure the registers in the LM93. All steps may not be necessary if default values are acceptable.

Set limits and parameters (not necessarily in this order):

- Set up Fan control
- Set up PWM temperature bindings
- Set fan tach limits
- Set fan boost temperature and hysteresis
- Set the VRD\_HOT and PROCHOT PWM ramp control rate
- Enable Smart Tach Mode and Tachometer Input to PWM binding (required with direct PWM drive of fans)
- Set the temperature absolute limits
- Set the temperature hysteresis values
- Set temperature filtered or unfiltered usage
- Set the Zone Adjustment Offset temperature
- Set the PROCHOT override and time interval values
- Set the PROCHOT user limit
- Enable THERMTRIP masking of error events (if GPIO4 and GPIO5 are used as THERMTRIP inputs)
- Set voltage sensor limits and hysteresis
- Set the Dynamic Vccp offset limits
- Set the Sleep State control and mask registers
- Set Other Mask Registers (GPI Error, VRDx\_HOT, SCSI\_TERM, and dynamic Vccp limit checking)
- Set start bit to select user values and unmask error events
- Set the sleep state to 0
- Set Lock bit to lock the limit and parameter registers (optional)

### 3.16.5 ROUND ROBIN VOLTAGE/TEMPERATURE CONVERSION CYCLE

The LM93 monitoring function is started as soon as the part is powered up. The LM93 performs a “round robin” sampling of the inputs, in the order shown below. Each cycle of the round robin is completed in less than 100 ms.

The results of the sampling and conversions can be found in the value registers and are available at any time.

| Channel # | Input       | Typical Assignment                  |
|-----------|-------------|-------------------------------------|
| 1         | Temp Zone 1 | Remote Diode 1 Temp Reading         |
| 2         | Temp Zone 2 | Remote Diode 2 Temp Reading         |
| 3         | Temp Zone 3 | Internal Temperature Reading        |
| 4         | AIN1        | +12V1                               |
| 5         | AIN2        | +12V2                               |
| 6         | AIN3        | +12V3                               |
| 7         | AIN4        | FSB_Vtt                             |
| 8         | AIN5        | 3GIO/PXH/MCH_Core                   |
| 9         | AIN6        | ICH_Core                            |
| 10        | AIN7        | CPU_1Vccp                           |
| 11        | AIN8        | CPU2_Vccp                           |
| 12        | AIN9        | 3.3V                                |
| 13        | AIN10       | +5V                                 |
| 14        | AIN11       | SCSI_Core                           |
| 15        | AIN12       | Mem_Core                            |
| 16        | AIN13       | Mem_Vtt                             |
| 17        | AIN14       | GBIT_Core                           |
| 18        | AIN15       | -12V                                |
| 19        | AIN16       | 3.3V SB V <sub>DD</sub> Supply Rail |

### 3.16.6 ERROR STATUS REGISTERS

The LM93 contains several error status registers for the BMC side, and duplicated error status registers for the Host side. These registers are used to reflect the state of all the possible error conditions that the LM93 monitors.

The BMC/Host Error Status registers hold a set bit until the event is cleared by software, even if the condition causing the error event goes away.

To clear a bit in the Error Status registers, a '1' has to be written to the specific bit that is required to be cleared. If the event that caused the error is no longer active then the bit is cleared.

Clearing a bit in a BMC Error Status register does not clear the corresponding bit in the Host Error Status register or vice versa.

#### 3.16.6.1 ASF Mode

In order for the LM93 part to act as a legacy sensor (6.1.2 of ASF spec DSP0114 rev 2) and to easily bolt up to the SMBus of an ASF capable NIC chip, the treatment of the Error Status registers needs to change.

The LM93 can be placed into ASF mode by setting the appropriate bit in the LM93 Status/Control register. Once this bit is set, the BMC Error Status registers become read-to-clear. Writing a '1' to clear a particular bit is also allowed in ASF mode. The Host Error Status registers are not effected by ASF mode.

### 3.16.7 MASKING, ERROR STATUS AND ALERT

Masking is always applied to bits in the HOST and BMC Error Status registers. If an event is masked, the corresponding error bit in the HOST or BMC Error Status registers is prevented from ever being set. As a result, this prevents the event from ever causing ALERT to be asserted. Masking an event does not clear its associated Error Status bit if it is currently set.

Voltage errors are masked by writing a high voltage limit value of FFh. This is the default high limit for all voltages.



Temperature errors are masked by writing a high temperature limit value of 80h. This is the default high limit for all temperatures. Masking a temperature channel masks both temperature errors and diode fault errors.

The GPI Mask register allows GPI errors to be masked. Any bits that are set in this register mask events for the corresponding GPIO\_x pin.

User  $\overline{\text{PROCHOT}}$  status is not really an error but it can be used to notify the user of processor throttling past a preset USER limit. A user limit of FFh acts as the mask for this register. Error bits associated with the predefined  $\overline{\text{PROCHOT}}$  thresholds cannot be masked. It is important to note though, that these error bits do not cause BMC\_ERR, HOST\_ERR, or  $\overline{\text{ALERT}}$  to be asserted under any condition.

Fan tach errors are masked if the tach limit for the given tach is set to FFh .

$\overline{\text{SCSI\_TERMx}}$  errors and  $\overline{\text{VRDx\_HOT}}$  errors can be masked by setting the appropriate bit in the VRD THERMTRIP and  $\overline{\text{SCSI\_TERM}}$  Error Mask register.

When the LM93 powers up, the  $\overline{\text{ALERT}}$  output is disabled. The  $\overline{\text{ALERT}}$  output can be enabled by setting the ALERT\_EN bit in the LM93 Configuration register.

In addition the manual masking options, the LM93 also masks some errors depending on the sleep state of the system. The sleep state of the system is communicated to the LM93 by writing to the Sleep State Control register. Some types of error events are always masked in certain sleep modes. Some types of error events are optionally masked in certain sleep modes if their sleep mask register bit is set. Refer to the [Register Descriptions](#) for more information.

### 3.16.8 LAYOUT AND GROUNDING

Analog components such as voltage dividers should be physically located as close as possible to the LM93.

The LM93 bypass capacitors, the parallel combination of 100 pF, 10  $\mu\text{F}$  (electrolytic or tantalum) and 0.1  $\mu\text{F}$  (ceramic) bypass capacitors must be connected between power pin (pin 39) and ground, and should be located as close as possible to the LM93. The 100 pF capacitor should be placed closest to the power pin.

### 3.16.9 THERMAL DIODE APPLICATION

To measure temperature external to the LM93, we need to use a remote discrete diode to sense the temperature of external objects or ambient air. Remember that the temperature of a discrete diode is effected, and often dominated, by the temperature of its leads.

Most silicon diodes do not lend themselves well to this application. It is recommended that a MMBT3904 transistor type base emitter junction be used with the collector tied to the base.

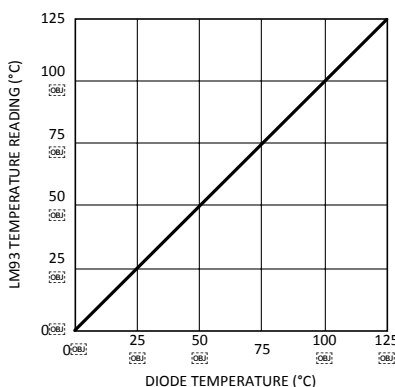


Figure 3-3. Thermal Diode Temperature vs. LM93 Temperature Reading

### 3.16.9.1 Accuracy Effects of Diode Non-Ideality Factor

The technique used in today's remote temperature sensors is to measure the change in  $V_{BE}$  at two different operating points of a diode. For a bias current ratio of N:1, this difference is given as:

$$\Delta V_{BE} = \eta \frac{kT}{q} \ln(N)$$

where:

- $\eta$  is the non-ideality factor of the process the diode is manufactured on,
- $q$  is the electron charge,
- $k$  is the Boltzmann's constant,
- $N$  is the current ratio,
- $T$  is the absolute temperature in °K. (6)

The temperature sensor then measures  $\Delta V_{BE}$  and converts to digital data. In this equation,  $k$  and  $q$  are well defined universal constants, and  $N$  is a parameter controlled by the temperature sensor. The only other parameter is  $\eta$ , which depends on the diode that is used for measurement. Since  $\Delta V_{BE}$  is proportional to both  $\eta$  and  $T$ , the variations in  $\eta$  cannot be distinguished from variations in temperature. Since the non-ideality factor is not controlled by the temperature sensor, it directly adds to the inaccuracy of the sensor. For example, assume a  $\pm 1\%$  variation in  $\eta$  from part to part (Xeon processors targeted for the LM93 do not have published thermal diode specifications at the time of this printing, therefore this is probably a very conservative estimate). Assume a temperature sensor has an accuracy specification of  $\pm 3^\circ\text{C}$  at room temperature of  $25^\circ\text{C}$  and the process used to manufacture the diode has a non-ideality variation of  $\pm 1\%$ . The resulting accuracy of the temperature sensor at room temperature is:

$$\text{TACC} = \pm 3^\circ\text{C} + (\pm 1\% \text{ of } 298^\circ\text{K}) = \pm 6^\circ\text{C} \quad (7)$$

The additional inaccuracy in the temperature measurement caused by  $\eta$ , can be eliminated if each temperature sensor is calibrated with the remote diode that it is paired with. The LM93 can be paired with an MMBT3904 when not being used to monitor the thermal diode within an Intel Processor.

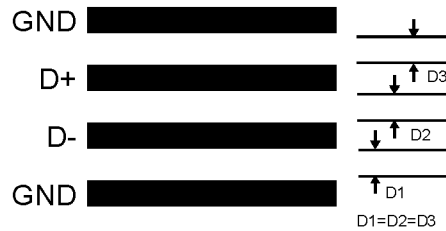
### 3.16.9.2 PCB Layout for Minimizing Noise

In the following guidelines, D+ and D- refer to the REMOTE1+, REMOTE1-, REMOTE2+, REMOTE2- pins.

In a noisy environment, such as a power supply, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the LM93 can cause temperature conversion errors.

The following guidelines should be followed:

1. Place a  $0.1 \mu\text{F}$  and  $100 \text{ pF}$  LM93 power bypass capacitors as close as possible to the  $V_{DD}$  pin, with the  $100 \text{ pF}$  capacitor being the closest. Place  $10 \mu\text{F}$  capacitor in the near vicinity of the LM93 power pin.
2. Place  $100 \text{ pF}$  capacitor as close as possible to the LM93 thermal diode Remote+ and Remote- pins. Make sure the traces to the  $100 \text{ pF}$  capacitor are matched and as short as possible. This capacitor is required to minimize high frequency noise error.
3. Ideally, the LM93 should be placed within  $10 \text{ cm}$  of the thermal diode pins with the traces being as straight, short and identical as possible. Trace resistance of  $1 \Omega$  can cause as much as  $1^\circ\text{C}$  of error.
4. Diode traces should be surrounded by a GND guard ring to either side, above and below, if possible. This GND guard should not be between the Remote+ and Remote- lines. In the event that noise does couple to the diode lines, it would be ideal if it is coupled to both identically, i.e. common mode. That is, equally to the Remote+ (D+) and Remote- (D-) lines. (See [Recommended Diode Trace Layout](#) figure below):



**Figure 3-4. Recommended Diode Trace Layout**

5. Avoid routing diode traces in close proximity to any power supply switching or filtering inductors.
6. Avoid running diode traces close to or parallel to high speed digital and bus lines. Diode traces should be kept at least 2 cm apart from the high speed digital traces.
7. If it is necessary to cross high speed digital traces, the diode traces and the high speed digital traces should cross at a 90 degree angle.
8. Leakage current between Remote+ and GND should be kept to a minimum. 1 nA of leakage can cause as much as 1°C of error in the diode temperature reading. Keeping the printed circuit board as clean as possible minimizes leakage current.

### 3.16.10 FAN CONTROL

#### 3.16.10.1 Automatic Fan Control Algorithm

The LM93 fan speed control method is optimized for fan power efficiency, fan reliability and minimum cost. The PWMx outputs can be filtered using an external switching regulator type output stage that provides 5V to 12V DC for fan power. A high PWM frequency is required to minimize the size and cost of the inductor and other components used in the output stage. The PWM outputs of the LM93 can operate up to 22.5 kHz with a step size of 6.25%.

The LM93 fan control method uses a look up table that contains 12 temperature offset settings and a base temperature. The actual duty cycle value for each step is pre-assigned. There are two possible assignments. They are dependent on the PWM output to Zone binding and the PWM output frequency. The temperature of each step is determined by the programmed offsets and zone base temperature. There are two sets of offset values, one set applies to Zone 1 and Zone 2 while the other set applies to Zone 3 and Zone 4. Each zone has an independent base temperature. A measured temperature can then be correlated to a PWM duty cycle level. Programmable temperature hysteresis is included that prevents fan speed oscillations between two steps. Each offset table has one hysteresis value assigned to it. Therefore, Zones 1 and 2 share a hysteresis value while Zones 3 and 4 share a different hysteresis value.

Shown in [Figure 3-5](#) is a plot of one example of the transfer function of the PWM output duty cycle (%) with respect to temperature (°C) for Zone 1 - 4. [Table 3-2](#) and [Table 3-3](#) show the actual register values used for the plot. For this example: Zones 1 and 2 are bound to PWM1 and PWM1 is programmed to have a low frequency PWM signal; Zones 3 and 4 are bound to PWM2 and PWM2 is programmed to have a high frequency PWM signal. As can be seen in [Table 3-2](#) and [Table 3-3](#) the duty cycle assignments differ. Low frequency PWM output assignments have a non-linear incremental increase in the duty cycle as shown in [Table 3-2](#) while high frequency PWM assignments have a linear incremental increase in the duty cycle as shown in [Table 3-3](#).

To minimize the size of the LM93's lookup table structure, temperature values in the registers are programmed as an offset value of 4 bits. This offset gets added in a cumulative manner to the 8-bit base temperature. The calculated temperature is then used in the comparison that determines the PWM output duty cycle. The minimum PWM (minPWM) value sets the duty cycle when the measured temperature is less than or equal to the base temperature. All offset values that map to a PWM value less than or equal to the minPWM setting must be set to zero as shown in [Table 3-2](#) and [Table 3-3](#). If the offset values are not set to zero, the LM93 fan control circuitry may function unpredictably.

Duty cycle levels may be skipped by setting their offset value to zero. As shown in Table 3-2, the 53.57% duty cycle step is skipped. When the temperature exceeds 74°C for CPU1 and 64°C for CPU2 the duty cycle changes from 50% to 57.14%.

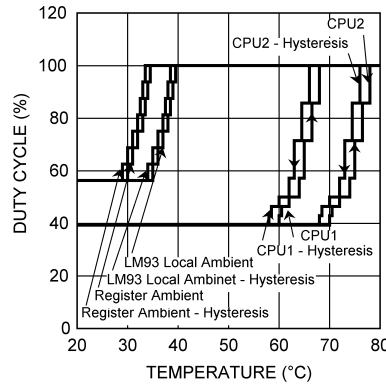


Figure 3-5. Example of the LM93 Fan Control Transfer Function.

Table 3-2. Zone 1/2 (CPU1 and CPU2) Table<sup>(1)</sup>

| Lookup Table<br>Duty Cycle | Zone 1/2<br>Toffset<br>table | Tbase<br>CPU1,<br>Zone1 | CPU1 Thermal Diode, Zone 1 (T <sub>D</sub> ) |                        | Tbase<br>CPU2,<br>Zone2 | CPU2 Thermal Diode, Zone 2 (T <sub>D</sub> ) |                        |
|----------------------------|------------------------------|-------------------------|----------------------------------------------|------------------------|-------------------------|----------------------------------------------|------------------------|
|                            |                              |                         | (°C)                                         | (°C)                   |                         | (°C)                                         | (°C)                   |
|                            |                              | 70                      |                                              | T <sub>D</sub> < 70    | 60                      |                                              | T <sub>D</sub> < 60    |
| 25                         | 0                            |                         |                                              |                        |                         |                                              |                        |
| 28.57                      | 0                            |                         |                                              |                        |                         |                                              |                        |
| 32.14                      | 0                            |                         |                                              |                        |                         |                                              |                        |
| 35.71                      | 0                            |                         |                                              |                        |                         |                                              |                        |
| 39.29                      | 0                            |                         |                                              |                        |                         |                                              |                        |
| 42.86                      | 0.5                          |                         | 70                                           | ≤T <sub>D</sub> < 70.5 |                         | 60                                           | ≤T <sub>D</sub> < 60.5 |
| 46.43                      | 1.5                          |                         | 70.5                                         | ≤T <sub>D</sub> < 72   |                         | 60.5                                         | ≤T <sub>D</sub> < 62   |
| 50                         | 2                            |                         | 72                                           | ≤T <sub>D</sub> < 74   |                         | 62                                           | ≤T <sub>D</sub> < 64   |
| 53.57                      | 0                            |                         |                                              |                        |                         |                                              |                        |
| 57.14                      | 1                            |                         | 74                                           | ≤T <sub>D</sub> < 75   |                         | 64                                           | ≤T <sub>D</sub> < 65   |
| 71.43                      | 1.5                          |                         | 75                                           | ≤T <sub>D</sub> < 76.5 |                         | 65                                           | ≤T <sub>D</sub> < 66.5 |
| 85.71                      | 1.5                          |                         | 76.5                                         | ≤T <sub>D</sub> < 78   |                         | 66.5                                         | ≤T <sub>D</sub> < 68   |
| 100                        |                              |                         | 78                                           | ≤T <sub>D</sub>        |                         | 68                                           | ≤T <sub>D</sub>        |

(1) In this example: Zones 1 and 2 are bound to the PWM1 output and the PWM1 frequency set to a value in the low range; Hysteresis is set to 2°C; Toffset and hysteresis resolution is set to 0.5°C; minPWM register set to 05h for Zones 1/2. Note, the duty cycle assignment depends on the zone to PWM output binding and the frequency setting of that PWM output.

**Table 3-3. Zone 3/4 (LM93 Ambient and External Ambient) Table<sup>(1)</sup>**

| Lookup Table<br>Duty Cycle | Zone 3/4<br>Toffset<br>table | Tbase<br>LM93<br>Ambient | LM93 Ambient, Zone 3 (T <sub>A</sub> ) |                  |                   | Tbase<br>External<br>Ambient | External Ambient, Zone 4 (T <sub>A</sub> ) |                  |      |                   |      |
|----------------------------|------------------------------|--------------------------|----------------------------------------|------------------|-------------------|------------------------------|--------------------------------------------|------------------|------|-------------------|------|
|                            |                              |                          | (°C)                                   |                  | (°C)              |                              | (°C)                                       |                  | (°C) |                   |      |
|                            |                              | 30                       |                                        | T <sub>A</sub> < | 30                | 35                           |                                            | T <sub>A</sub> < | 35   |                   |      |
| 25                         | 0                            |                          |                                        |                  |                   |                              |                                            |                  |      |                   |      |
| 31.25                      | 0                            |                          |                                        |                  |                   |                              |                                            |                  |      |                   |      |
| 37.5                       | 0                            |                          |                                        |                  |                   |                              |                                            |                  |      |                   |      |
| 43.75                      | 0                            |                          |                                        |                  |                   |                              |                                            |                  |      |                   |      |
| 50                         | 0                            |                          |                                        |                  |                   |                              |                                            |                  |      |                   |      |
| 56.25                      | 0                            |                          |                                        |                  |                   |                              |                                            |                  |      |                   |      |
| 62.5                       | 1                            |                          |                                        | 30               | ≤T <sub>A</sub> < |                              | 31                                         |                  | 35   | ≤T <sub>A</sub> < | 36   |
| 68.75                      | 1                            |                          |                                        | 31               | ≤T <sub>A</sub> < |                              | 32                                         |                  | 36   | ≤T <sub>A</sub> < | 37   |
| 75                         | 1                            |                          |                                        | 32               | ≤T <sub>A</sub> < |                              | 33                                         |                  | 37   | ≤T <sub>A</sub> < | 38   |
| 81.25                      | 0.5                          |                          |                                        | 33               | ≤T <sub>A</sub> < |                              | 33.5                                       |                  | 38   | ≤T <sub>A</sub> < | 38.5 |
| 87.5                       | 0.5                          |                          |                                        | 33.5             | ≤T <sub>A</sub> < |                              | 34                                         |                  | 38.5 | ≤T <sub>A</sub> < | 39   |
| 93.75                      | 0.5                          |                          |                                        | 34               | ≤T <sub>A</sub> < |                              | 34.5                                       |                  | 39   | ≤T <sub>A</sub> < | 39.5 |
| 100                        |                              |                          |                                        | 34.5             | ≤T <sub>A</sub>   |                              |                                            |                  | 39.5 | ≤T <sub>A</sub>   |      |

(1) In this example: Zone 3 and Zone 4 are bound to the PWM 2 output and the PWM2 output frequency set to 22.5kHz; Hysteresis is set to 1°C; Toffset and hysteresis resolution set to 0.5°C; minPWM for Zones 3/4 register is set to 06h. Note, the duty cycle assignment depends on the zone to PWM output binding and the frequency setting of that PWM output.

### 3.16.10.2 Fan Control Temperature Resolution

As shown in the example the auto fan control algorithm can operate in a mode that allows 0.5°C of temperature resolution instead of the normal 1°C. When this mode is enabled, the temperature offset registers that make up the lookup table are interpreted differently. One LSB represents 0.5°C, and the available range between each datapoint is 0°C to 7.5°C instead of 0°C to 15°C. In addition, the hysteresis registers for auto fan control are interpreted in the same way (one LSB equals 0.5°C).

Zones 1, 2 and 3 all have 9-bits of internal resolution, which makes this feature useful. Zone 4 is written in from the SMBus and only has 8-bits of resolution. The LM93 left justifies the value into a 9-bit field before using it, if the 0.5°C mode is enabled.

Note that since zones 1 and 2 share the same lookup table, both zones must be operating in the same resolution mode. The same applies to zones 3 and 4 since they share the same lookup table.

### 3.16.10.3 Zone 1-4 to PWM1-2 Binding

Each zone must be bound to the PWM outputs in order to have effect on the output's duty cycle. Any combination of the zones may be used to drive a PWM output, they are not limited to the binding described in the previous example. For instance zones 1, 2 and 4 may be bound to PWM1 while zones 3 and 4 are bound to PWM2. Note that the duty cycle levels in the lookup table are dependent on the PWM output frequency assignment. Therefore, if PWM1 is assigned to a high frequency and PWM2 is assigned to a low frequency, in the binding example just mentioned, zone 4 has a different duty cycle calculated through the lookup table for PWM1 than for PWM2, even though the same Toffset values are used. This is due to the fact that PWM levels assigned to a high frequency PWM output are different than the levels assigned to a low frequency PWM output.

### 3.16.10.4 Fan Control Duty Cycles

Several registers in the LM93 use 4-bit values to represent a duty cycle. All of them use a common mapping that associates the 4-bit value with a duty cycle. The 4-bit values correspond also with the 14 steps of the auto fan control algorithm. The mapping is shown below. This applies for PWM outputs running at the default 22.5 kHz (high) frequency.

| 4-Bit Value | Step | 22.5 kHz (High Frequency)<br>Duty Cycle |
|-------------|------|-----------------------------------------|
| 0h          |      | 0.00%                                   |
| 1h          | 1    | 25.00%                                  |
| 2h          | 2    | 31.25%                                  |
| 3h          | 3    | 37.50%                                  |
| 4h          | 4    | 43.75%                                  |
| 5h          | 5    | 50.00%                                  |
| 6h          | 6    | 56.25%                                  |
| 7h          | 7    | 62.50%                                  |
| 8h          | 8    | 68.75%                                  |
| 9h          | 9    | 75.00%                                  |
| Ah          | 10   | 81.25%                                  |
| Bh          | 11   | 87.50%                                  |
| Ch          | 12   | 93.75%                                  |
| Dh          | 13   | 100.00%                                 |
| Eh          | —    | Reserved                                |
| Fh          | —    | Reserved                                |

### 3.16.10.5 Alternate PWM Frequencies

The PWM output can operate at lower frequencies, instead of the default 22.5 kHz. The alternate lower frequencies can be enabled through the PWMx Control 4 registers. When operating in the lower frequency mode, the mapping between step numbers and duty cycles changes. This effects the auto fan control and all LM93 registers that describe a duty cycle using a 4-bit value.

The low frequency PWM output duty cycle mapping is listed in the following table:

| 4-Bit Value | Step | Low Frequencies<br>Duty Cycle |
|-------------|------|-------------------------------|
| 0h          |      | 0%                            |
| 1h          | 1    | 25.00%                        |
| 2h          | 2    | 28.57%                        |
| 3h          | 3    | 32.14%                        |
| 4h          | 4    | 35.71%                        |
| 5h          | 5    | 39.29%                        |
| 6h          | 6    | 42.86%                        |
| 7h          | 7    | 46.43%                        |
| 8h          | 8    | 50.00%                        |
| 9h          | 9    | 53.57%                        |
| Ah          | 10   | 57.14%                        |
| Bh          | 11   | 71.43%                        |
| Ch          | 12   | 85.71%                        |
| Dh          | 13   | 100.00%                       |
| Eh          | —    | Reserved                      |
| Fh          | —    | Reserved                      |

### 3.16.10.6 Fan Control Priorities

The automatic fan control is not the only function that influences PWM duty cycle. There are several other functions that influence the PWM duty cycle. All the functions can be classified into several categories:

| Category # | Category Name                                          |
|------------|--------------------------------------------------------|
| 1          | PWM to 100% conditions                                 |
| 2          | $\overline{\text{VRDx\_HOT}}$ ramp-up/ramp-down        |
| 3          | $\overline{\text{PROCHOT}}$ ramp-up/ramp-down function |
| 4          | Manual PWM Override                                    |
| 5          | Fan Spin-Up Control                                    |
| 6          | Automatic Fan Control Algorithm                        |

The ultimate PWM duty cycle that is chosen can be described by the following formula:

If (Manual PWM Override is active)

$$\text{PWM} = \max(1,2,3,4)$$

Else

$$\text{PWM} = \max(1,2,3,5,6)$$

So in general, categories 1, 2 and 3 are always active. In addition to that, either category 4 or categories 5 and 6 are active depending on whether manual override is enabled. In this sense the manual override, when enabled, replaces category 5 and 6.

### 3.16.10.7 PWM to 100% Conditions

There are several conditions that cause the duty cycles of all PWM outputs to immediately get set to 100%. They are:

1. Any of the four temperature zones has exceeded the programmed Fan Boost Limit setting but has not yet cooled down enough to drop below the hysteresis point.
2. The OVRID bit is set in the LM93 Status/Control.

### 3.16.10.8 $\overline{\text{VRDx\_HOT}}$ Ramp-Up/Ramp-Down

This function causes the duty cycle of the PWM outputs to gradually increase over time if  $\overline{\text{VRD1\_HOT}}$  or  $\overline{\text{VRD2\_HOT}}$  are asserted.

When  $\overline{\text{VRDx\_HOT}}$  is asserted, the ramp function is enabled. The enabling process involves two steps:

1. The current duty cycle being requested by other PWM functions is memorized.
2. The ramp function immediately adds one PWM duty cycle step to the memorized value and requests this duty cycle.

Once the function is enabled, it gradually adds additional duty cycle steps every X milliseconds whenever  $\overline{\text{VRDx\_HOT}}$  is asserted (X is programmable via the PWM Ramp Control register). If  $\overline{\text{VRDx\_HOT}}$  remains asserted for a long enough time, the duty cycle eventually reaches 100%.

Whenever  $\overline{\text{VRDx\_HOT}}$  is de-asserted, the ramp function begins to ramp down by subtracting one PWM duty cycle step every X milliseconds. If  $\overline{\text{VRDx\_HOT}}$  is currently de-asserted, and the ramp function is less than to the PWM duty cycle being requested by other functions, the ramp function is disabled.

As long as the function is enabled, it continues to ramp up or ramp down depending on the state of  $\overline{\text{VRDx\_HOT}}$ . The ramp enabling process described above can only re-occur after the ramp function has been disabled. Rapid assertion/de-assertion of  $\overline{\text{VRDx\_HOT}}$  does not trigger the enabling process unless  $\overline{\text{VRDx\_HOT}}$  was de-asserted long enough for the ramp function to disable itself.



This ramp function operates independently for  $\overline{\text{VRD1\_HOT}}$  and  $\overline{\text{VRD2\_HOT}}$ . In addition, the ramp function only applies to the PWM(s) that are bound to one or two  $\overline{\text{VRDx\_HOT}}$  inputs. Depending on the bindings, it is possible that up to four independent ramp functions are active at any given moment:

PWM1/VRD1

PWM1/VRD2

PWM2/VRD1

PWM2/VRD2

If a PWM is bound to both  $\overline{\text{VRD1\_HOT}}$  and  $\overline{\text{VRD2\_HOT}}$ , then two ramp functions are active for that PWM output. In this case the duty cycle that is used is the maximum of the two ramp functions.

### 3.16.10.9 $\overline{\text{PROCHOT}}$ Ramp-Up/Ramp-Down

This function is very similar to the  $\overline{\text{VRDx\_HOT}}$  ramp-up/ramp-down function. The PWM duty cycle ramps up in the same fashion whenever the  $\overline{\text{PROCHOT}}$  measurement exceeds the user programmed threshold. Once a new  $\overline{\text{PROCHOT}}$  measurement is made that no longer exceeds the user limit, the PWM will begin to ramp down.

Just as with the  $\overline{\text{VRDx\_HOT}}$  ramp function, the  $\overline{\text{PROCHOT}}$  ramp function uses independent bindings to determine which PWM outputs should be effected by each  $\overline{\text{PROCHOT}}$  input ( $\overline{\text{P1\_PROCHOT}}$  or  $\overline{\text{P2\_PROCHOT}}$ ).

If a PWM is bound to both  $\overline{\text{P1\_PROCHOT}}$  and  $\overline{\text{P2\_PROCHOT}}$ , two  $\overline{\text{PROCHOT}}$  ramp functions could be active at the same time. In this case the duty cycle that is used is the maximum of the two ramp functions.

### 3.16.10.10 Manual PWM Override

When a PWM channel is configured for manual PWM override, software can manually control the PWM duty cycle. There are some PWM control functions that could still cause the duty cycle to be higher than the manual setting. See the [Fan Control Priorities](#) for details.

### 3.16.10.11 Fan Spin-Up Control

All of the other PWM control functions are combined to produce a final duty cycle that is actually used for the PWM output. If this final value changes from zero to a non-zero value, the Fan Spin-Up Control function is triggered. Once triggered, the Fan Spin-Up Control requests the programmed duty cycle for a programmed period of time.

### 3.16.11 XOR TREE TEST

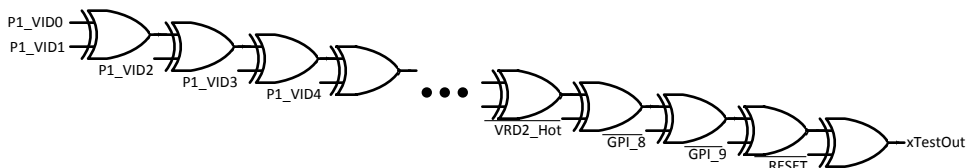
An XOR tree is provided in the LM93 for Automated Test Equipment (ATE) board level connectivity testing. This allows the functionality of all digital inputs to be tested in a simple manner and any pins that are non-functional or shorted together to be identified. When the test mode is enabled by setting the 'XEN' bit in the XOR Test register, the part enters XOR test mode.

The following signals are included in the XOR test tree:

|                              |                             |                          |                                 |                               |                                 |                           |
|------------------------------|-----------------------------|--------------------------|---------------------------------|-------------------------------|---------------------------------|---------------------------|
| $\overline{\text{Px\_VIDy}}$ | $\overline{\text{GPIO\_x}}$ | $\overline{\text{PWMx}}$ | $\overline{\text{Px\_PROCHOT}}$ | $\overline{\text{VRDx\_HOT}}$ | $\overline{\text{SCSI\_TERMx}}$ | $\overline{\text{RESET}}$ |
|------------------------------|-----------------------------|--------------------------|---------------------------------|-------------------------------|---------------------------------|---------------------------|



Since the test mode is XOR tree, the order of the signals in the tree is not important. SMBDAT and SMBCLK should not be included in the test tree.



**Figure 3-6. Example of XOR Test Tree (not showing all signals)**

To properly implement the XOR TREE test on the PCB, no pins listed in the tree should be connected directly to power or ground. If a pin needs to be configured as a permanent low, such as an address, it should be connected to ground through a low value resistor such as 10 k $\Omega$ , to allow the ATE (Automatic Test Equipment) to drive it high.

When generating test waveforms, a typical propagation delay of 500 ns through the XOR tree should be allowed for.

## 3.17 Registers

### 3.17.1 REGISTER WARNINGS

In most cases, reserved registers and register bits return zero when read. This should not be relied upon, since reserved registers can be used for future expansion of the LM93 functions.

Some registers have “N/D” for their default value. This means that the power-up default of the register is not defined. In the case of value registers, care should be taken to ensure that software does not read a value register until the associated measurement function has acquired a measurement. This applies to temperatures, voltages, fan RPM, and  $\overline{\text{PROCHOT}}$  monitoring. In the case of other registers, such as fan control settings, N/D means that software must initialize these registers to ensure they have a known value before setting the START bit in the LM93 Configuration register.

### 3.17.2 REGISTER SUMMARY TABLE

**Table 3-4. Register Key**

| Term | Description            |
|------|------------------------|
| N/D  | Not Defined            |
| N/A  | Not Applicable         |
| R    | Read Only              |
| R/W  | Read or Write          |
| RWC  | Read or Write to Clear |

| Lock                               | Register Name             | Address | Default | Description                                             |
|------------------------------------|---------------------------|---------|---------|---------------------------------------------------------|
| <b>FACTORY REGISTERS</b>           |                           |         |         |                                                         |
| x                                  | XOR Test                  | 00h     | 00h     | Used to set the XOR test tree mode                      |
|                                    | SMBus Test                | 01h     | N/D     | SMBus read/write test register                          |
|                                    | Reserved                  | 02h-3Dh | N/D     |                                                         |
|                                    | Manufacturer ID           | 3Eh     | 01h     | Contains manufacturer ID code                           |
|                                    | Version/Stepping          | 3Fh     | 73h     | Contains code for major and minor revisions             |
| <b>BMC ERROR STATUS REGISTERS</b>  |                           |         |         |                                                         |
|                                    | B_Error Status 1          | 40h     | 00h     | BMC error status register 1                             |
|                                    | B_Error Status 2          | 41h     | 00h     | BMC error register 2                                    |
|                                    | B_Error Status 3          | 42h     | 00h     | BMC error register 3                                    |
|                                    | B_Error Status 4          | 43h     | 00h     | BMC error register 4                                    |
|                                    | B_P1_PROCHOT Error Status | 44h     | 00h     | BMC error register for $\overline{\text{P1\_PROCHOT}}$  |
|                                    | B_P2_PROCHOT Error Status | 45h     | 00h     | BMC error register for $\overline{\text{P2\_PROCHOT}}$  |
|                                    | B_GPI Error Status        | 46h     | 00h     | BMC error register for GPIs                             |
|                                    | B_Fan Error Status        | 47h     | 00h     | BMC error register for Fans                             |
| <b>HOST ERROR STATUS REGISTERS</b> |                           |         |         |                                                         |
|                                    | H_Error Status 1          | 48h     | 00h     | HOST error status register 1                            |
|                                    | H_Error Status 2          | 49h     | 00h     | HOST error register 2                                   |
|                                    | H_Error Status 3          | 4Ah     | 00h     | HOST error register 3                                   |
|                                    | H_Error Status 4          | 4Bh     | 00h     | HOST error register 4                                   |
|                                    | H_P1_PROCHOT Error Status | 4Ch     | 00h     | HOST error register for $\overline{\text{P1\_PROCHOT}}$ |
|                                    | H_P2_PROCHOT Error Status | 4Dh     | 00h     | HOST error register for $\overline{\text{P2\_PROCHOT}}$ |
|                                    | H_GPI Error Status        | 4Eh     | 00h     | HOST error register for GPIs                            |
|                                    | H_Fan Error Status        | 4Fh     | 00h     | HOST error register for Fans                            |

| Lock                   | Register Name                    | Address | Default | Description                                                                  |
|------------------------|----------------------------------|---------|---------|------------------------------------------------------------------------------|
| <b>VALUE REGISTERS</b> |                                  |         |         |                                                                              |
|                        | Zone 1 (CPU1) Temp               | 50h     | N/D     | Measured value of remote thermal diode temperature channel 1                 |
|                        | Zone 2 (CPU2) Temp               | 51h     | N/D     | Measured value of remote thermal diode temperature channel 2                 |
|                        | Zone 3 (Internal) Temp           | 52h     | N/D     | Measured temperature from on-chip sensor                                     |
|                        | Zone 4 (External Digital) Temp   | 53h     | N/D     | Measured temperature from external temperature sensor                        |
|                        | Zone 1 (CPU1) Filtered Temp      | 54h     | 00h     | Filtered value of remote thermal diode temperature channel 1                 |
|                        | Zone 2 (CPU2) Filtered Temp      | 55h     | 00h     | Filtered value of remote thermal diode temperature channel 2                 |
|                        | AD_IN1 Voltage                   | 56h     | N/D     | Measured value of AD_IN1                                                     |
|                        | AD_IN2 Voltage                   | 57h     | N/D     | Measured value of AD_IN2                                                     |
|                        | AD_IN3 Voltage                   | 58h     | N/D     | Measured value of AD_IN3                                                     |
|                        | AD_IN4 Voltage                   | 59h     | N/D     | Measured value of AD_IN4                                                     |
|                        | AD_IN5 Voltage                   | 5Ah     | N/D     | Measured value of AD_IN5                                                     |
|                        | AD_IN6 Voltage                   | 5Bh     | N/D     | Measured value of AD_IN6                                                     |
|                        | AD_IN7 Voltage                   | 5Ch     | N/D     | Measured value of AD_IN7                                                     |
|                        | AD_IN8 Voltage                   | 5Dh     | N/D     | Measured value of AD_IN8                                                     |
|                        | AD_IN9 Voltage                   | 5Eh     | N/D     | Measured value of AD_IN9                                                     |
|                        | AD_IN10 Voltage                  | 5Fh     | N/D     | Measured value of AD_IN10                                                    |
|                        | AD_IN11 Voltage                  | 60h     | N/D     | Measured value of AD_IN11                                                    |
|                        | AD_IN12 Voltage                  | 61h     | N/D     | Measured value of AD_IN12                                                    |
|                        | AD_IN13 Voltage                  | 62h     | N/D     | Measured value of AD_IN13                                                    |
|                        | AD_IN14 Voltage                  | 63h     | N/D     | Measured value of AD_IN14                                                    |
|                        | AD_IN15 Voltage                  | 64h     | N/D     | Measured value of AD_IN15                                                    |
|                        | AD_IN16 Voltage                  | 65h     | N/D     | Measured value of AD_IN16 (V <sub>DD</sub> 3.3V S/B)                         |
|                        | Reserved                         | 66h     | N/D     |                                                                              |
|                        | Current $\overline{P1\_PROCHOT}$ | 67h     | 00h     | Measured $\overline{P1\_PROCHOT}$ throttle percentage                        |
|                        | Average $\overline{P1\_PROCHOT}$ | 68h     | N/D     | Average $\overline{P1\_PROCHOT}$ throttle percentage                         |
|                        | Current $\overline{P2\_PROCHOT}$ | 69h     | 00h     | Measured $\overline{P2\_PROCHOT}$ throttle percentage                        |
|                        | Average $\overline{P2\_PROCHOT}$ | 6Ah     | N/D     | Average $\overline{P2\_PROCHOT}$ throttle percentage                         |
|                        | GPI State                        | 6Bh     | N/D     | Current GPIO state                                                           |
|                        | P1_VID                           | 6Ch     | N/D     | Current 6-bit VID value of Processor 1                                       |
|                        | P2_VID                           | 6Dh     | N/D     | Current 6-bit VID value of Processor 2                                       |
|                        | FAN Tach 1 LSB                   | 6Eh     | N/D     | Measured FAN Tach 1 LSB                                                      |
|                        | FAN Tach 1 MSB                   | 6Fh     | N/D     | Measured FAN Tach 1 MSB                                                      |
|                        | FAN Tach 2 LSB                   | 70h     | N/D     | Measured FAN Tach 2 LSB                                                      |
|                        | FAN Tach 2 MSB                   | 71h     | N/D     | Measured FAN Tach 2 MSB                                                      |
|                        | FAN Tach 3 LSB                   | 72h     | N/D     | Measured FAN Tach 3 LSB                                                      |
|                        | FAN Tach 3 MSB                   | 73h     | N/D     | Measured FAN Tach 3 MSB                                                      |
|                        | FAN Tach 4 LSB                   | 74h     | N/D     | Measured FAN Tach 4 LSB                                                      |
|                        | FAN Tach 4 MSB                   | 75h     | N/D     | Measured FAN Tach 4 MSB                                                      |
|                        | Reserved                         | 76h-77h | N/D     |                                                                              |
| <b>LIMIT REGISTERS</b> |                                  |         |         |                                                                              |
|                        | Zone 1 (CPU1) Low Temp           | 78h     | 80h     | Low limit for external thermal diode temperature channel 1 (D1) measurement  |
|                        | Zone 1 (CPU1) High Temp          | 79h     | 80h     | High limit for external thermal diode temperature channel 1 (D1) measurement |
|                        | Zone 2 (CPU2) Low Temp           | 7Ah     | 80h     | Low limit for external thermal diode temperature channel 2 (D2) measurement  |
|                        | Zone 2 (CPU2) High Temp          | 7Bh     | 80h     | High limit for external thermal diode temperature channel 2 (D2) measurement |
|                        | Zone 3 (Internal) Low Temp       | 7Ch     | 80h     | Low limit for local temperature measurement                                  |

| Lock | Register Name                       | Address | Default | Description                                                    |
|------|-------------------------------------|---------|---------|----------------------------------------------------------------|
|      | Zone 3 (Internal) High Temp         | 7Dh     | 80h     | High limit for local temperature measurement                   |
|      | Zone 4 (External Digital) Low Temp  | 7Eh     | 80h     | Low limit for external digital temperature sensor              |
|      | Zone 4 (External Digital) High Temp | 7Fh     | 80h     | High limit for external digital temperature sensor             |
| x    | Fan Boost Temp Zone 1               | 80h     | 3Ch     | Zone 1 (CPU1) fan boost temperature                            |
| x    | Fan Boost Temp Zone 2               | 81h     | 3Ch     | Zone 2 (CPU2) fan boost temperature                            |
| x    | Fan Boost Temp Zone 3               | 82h     | 23h     | Zone 3 (Internal) fan boost temperature                        |
| x    | Fan Boost Temp Zone 4               | 83h     | 23h     | Zone 4 (External Digital) fan boost temperature                |
|      | Reserved                            | 84h-8Fh | N/D     |                                                                |
|      | AD_IN1 Low Limit                    | 90h     | 00h     | Low limit for analog input 1 measurement                       |
|      | AD_IN1 High Limit                   | 91h     | FFh     | High limit for analog input 1 measurement                      |
|      | AD_IN2 Low Limit                    | 92h     | 00h     | Low limit for analog input 2 measurement                       |
|      | AD_IN2 High Limit                   | 93h     | FFh     | High limit for analog input 2 measurement                      |
|      | AD_IN3 Low Limit                    | 94h     | 00h     | Low limit for analog input 3 measurement                       |
|      | AD_IN3 High Limit                   | 95h     | FFh     | High limit for analog input 3 measurement                      |
|      | AD_IN4 Low Limit                    | 96h     | 00h     | Low limit for analog input 4 measurement                       |
|      | AD_IN4 High Limit                   | 97h     | FFh     | High limit for analog input 4 measurement                      |
|      | AD_IN5 Low Limit                    | 98h     | 00h     | Low limit for analog input 5 measurement                       |
|      | AD_IN5 High Limit                   | 99h     | FFh     | High limit for analog input 5 measurement                      |
|      | AD_IN6 Low Limit                    | 9Ah     | 00h     | Low limit for analog input 6 measurement                       |
|      | AD_IN6 High Limit                   | 9Bh     | FFh     | High limit for analog input 6 measurement                      |
|      | AD_IN7 Low Limit                    | 9Ch     | 00h     | Low limit for analog input 7 measurement                       |
|      | AD_IN7 High Limit                   | 9Dh     | FFh     | High limit for analog input 7 measurement                      |
|      | AD_IN8 Low Limit                    | 9Eh     | 00h     | Low limit for analog input 8 measurement                       |
|      | AD_IN8 High Limit                   | 9Fh     | FFh     | High limit for analog input 8 measurement                      |
|      | AD_IN9 Low Limit                    | A0h     | 00h     | Low limit for analog input 9 measurement                       |
|      | AD_IN9 High Limit                   | A1h     | FFh     | High limit for analog input 9 measurement                      |
|      | AD_IN10 Low Limit                   | A2h     | 00h     | Low limit for analog input 10 measurement                      |
|      | AD_IN10 High Limit                  | A3h     | FFh     | High limit for analog input 10 measurement                     |
|      | AD_IN11 Low Limit                   | A4h     | 00h     | Low limit for analog input 11 measurement                      |
|      | AD_IN11 High Limit                  | A5h     | FFh     | High limit for analog input 11 measurement                     |
|      | AD_IN12 Low Limit                   | A6h     | 00h     | Low limit for analog input 12 measurement                      |
|      | AD_IN12 High Limit                  | A7h     | FFh     | High limit for analog input 12 measurement                     |
|      | AD_IN13 Low Limit                   | A8h     | 00h     | Low limit for analog input 13 measurement                      |
|      | AD_IN13 High Limit                  | A9h     | FFh     | High limit for analog input 13 measurement                     |
|      | AD_IN14 Low Limit                   | AAh     | 00h     | Low limit for analog input 14 measurement                      |
|      | AD_IN14 High Limit                  | ABh     | FFh     | High limit for analog input 14 measurement                     |
|      | AD_IN15 Low Limit                   | ACh     | 00h     | Low limit for analog input 15 measurement                      |
|      | AD_IN15 High Limit                  | ADh     | FFh     | High limit for analog input 15 measurement                     |
|      | AD_IN16 Low Limit                   | A Eh    | 00h     | Low limit for analog input 16 measurement                      |
|      | AD_IN16 High Limit                  | A Fh    | FFh     | High limit for analog input 16 measurement                     |
|      | $\overline{P1\_PROCHOT}$ User Limit | B0h     | FFh     | User settable limit for $\overline{P1\_PROCHOT}$               |
|      | $\overline{P2\_PROCHOT}$ User Limit | B1h     | FFh     | User settable limit for $\overline{P2\_PROCHOT}$               |
|      | Vccp1 Limit Offsets                 | B2h     | 17h     | VID offset values for window comparator for CPU1 Vccp (AD_IN7) |
|      | Vccp2 Limit Offsets                 | B3h     | 17h     | VID offset values for window comparator for CPU2 Vccp (AD_IN8) |
|      | FAN Tach 1 Limit LSB                | B4h     | FCh     | FAN Tach 1 Limit LSB                                           |
|      | FAN Tach 1 Limit MSB                | B5h     | FFh     | FAN Tach 1 Limit MSB                                           |
|      | FAN Tach 2 Limit LSB                | B6h     | FCh     | FAN Tach 2 Limit LSB                                           |
|      | FAN Tach 2 Limit MSB                | B7h     | FFh     | FAN Tach 2 Limit MSB                                           |
|      | FAN Tach 3 Limit LSB                | B8h     | FCh     | FAN Tach 3 Limit LSB                                           |

| Lock                   | Register Name                             | Address | Default | Description                                                                                                                                                                        |
|------------------------|-------------------------------------------|---------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                        | FAN Tach 3 Limit MSB                      | B9h     | FFh     | FAN Tach 3 Limit MSB                                                                                                                                                               |
|                        | FAN Tach 4 Limit LSB                      | BAh     | FCb     | FAN Tach 4 Limit LSB                                                                                                                                                               |
|                        | FAN Tach 4 Limit MSB                      | BBh     | FFh     | FAN Tach 4 Limit MSB                                                                                                                                                               |
| <b>SETUP REGISTERS</b> |                                           |         |         |                                                                                                                                                                                    |
| x                      | Special Function Control 1                | BCh     | 00h     | Controls the hysteresis for voltage limit comparisons. Also selects filtered or unfiltered temperature usage for temperature limit comparisons and fan control.                    |
| x                      | Special Function Control 2                | BDh     | 00h     | Enables smart tach detection. Also selects 0.5°C or 1.0°C resolution for fan control.                                                                                              |
| x                      | GPI / VID Level Control                   | BEh     | 00h     | Control the input threshold levels for the P1_VIDx, P2_VIDx and GPIO_x inputs.                                                                                                     |
| x                      | PWM Ramp Control                          | BFh     | 00h     | Controls the ramp rate of the PWM duty cycle when $\overline{\text{VRDx\_HOT}}$ is asserted, as well as the ramp rate when $\overline{\text{PROCHOT}}$ exceeds the user threshold. |
| x                      | Fan Boost Hysteresis (Zones 1/2)          | C0h     | 44h     | Fan Boost Hysteresis for zones 1 and 2                                                                                                                                             |
| x                      | Fan Boost Hysteresis (Zones 3/4)          | C1h     | 44h     | Fan Boost Hysteresis for zones 3 and 4                                                                                                                                             |
| x                      | Zones 1/2 Spike Smoothing Control         | C2h     | 00h     | Configures Spike Smoothing for zones 1 and 2                                                                                                                                       |
| x                      | Zones 1/2 MinPWM and Hysteresis           | C3h     | N/D     | Controls MinPWM and hysteresis setting for zones 1 and 2 auto-fan control                                                                                                          |
| x                      | Zones 3/4 MinPWM and Hysteresis           | C4h     | N/D     | Controls MinPWM and hysteresis setting for zones 3 and 4 auto-fan control                                                                                                          |
|                        | GPO                                       | C5h     | 00h     | Controls the output state of the GPIO pins                                                                                                                                         |
|                        | $\overline{\text{PROCHOT}}$ Override      | C6h     | 00h     | Allows manual assertion of $\overline{\text{P1\_PROCHOT}}$ or $\overline{\text{P2\_PROCHOT}}$                                                                                      |
|                        | $\overline{\text{PROCHOT}}$ Time Interval | C7h     | 11h     | Configures the time window over which the $\overline{\text{PROCHOT}}$ inputs are measured                                                                                          |
| x                      | PWM1 Control 1                            | C8h     | 0Fh     | Controls PWM control source bindings.                                                                                                                                              |
| x                      | PWM1 Control 2                            | C9h     | 00h     | Controls PWM override and output polarity                                                                                                                                          |
| x                      | PWM1 Control 3                            | CAh     | 00h     | Controls PWM spin-up duration and duty cycle                                                                                                                                       |
| x                      | PWM1 Control 4                            | CBh     | 00h     | Frequency control for PWM1.                                                                                                                                                        |
| x                      | PWM2 Control 1                            | CCh     | 0Fh     | Controls PWM control source bindings.                                                                                                                                              |
| x                      | PWM2 Control 2                            | CDh     | 00h     | Controls PWM override and output polarity                                                                                                                                          |
| x                      | PWM2 Control 3                            | CEh     | 00h     | Controls PWM spin-up duration and duty cycle                                                                                                                                       |
| x                      | Special Function PWM2 Control 4           | CFh     | 00h     | Frequency control for PWM2                                                                                                                                                         |
| x                      | Zone 1 Base Temperature                   | D0h     | N/D     | Base temperature to which look-up table offset is applied for Zone 1                                                                                                               |
| x                      | Zone 2 Base Temperature                   | D1h     | N/D     | Base temperature to which look-up table offset is applied for Zone 2                                                                                                               |
| x                      | Zone 3 Base Temperature                   | D2h     | N/D     | Base temperature to which look-up table offset is applied for Zone 3                                                                                                               |
| x                      | Zone 4 Base Temperature                   | D3h     | N/D     | Base temperature to which look-up table offset is applied for Zone 4                                                                                                               |
| x                      | Step 2 Temp Offset                        | D4h     | N/D     | Step 2 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                   |
| x                      | Step 3 Temp Offset                        | D5h     | N/D     | Step 3 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                   |
| x                      | Step 4 Temp Offset                        | D6h     | N/D     | Step 4 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                   |
| x                      | Step 5 Temp Offset                        | D7h     | N/D     | Step 5 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                   |
| x                      | Step 6 Temp Offset                        | D8h     | N/D     | Step 6 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                   |
| x                      | Step 7 Temp Offset                        | D9h     | N/D     | Step 7 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                   |
| x                      | Step 8 Temp Offset                        | DAh     | N/D     | Step 8 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                   |
| x                      | Step 9 Temp Offset                        | DBh     | N/D     | Step 9 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                   |
| x                      | Step 10 Temp Offset                       | DCh     | N/D     | Step 10 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                  |
| x                      | Step 11 Temp Offset                       | DDh     | N/D     | Step 11 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                  |
| x                      | Step 12 Temp Offset                       | DEh     | N/D     | Step 12 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                  |
| x                      | Step 13 Temp Offset                       | DFh     | N/D     | Step 13 Zone 1/2 and Zone 3/4 Offset Temperatures                                                                                                                                  |
| x                      | Special Function TACH to PWM Binding      | E0h     | 00h     | Controls the tachometer input to PWM output binding                                                                                                                                |
|                        | Reserved                                  | E1      | N/D     |                                                                                                                                                                                    |

| Lock                                                     | Register Name                             | Address | Default | Description                                                                                                                |
|----------------------------------------------------------|-------------------------------------------|---------|---------|----------------------------------------------------------------------------------------------------------------------------|
| x                                                        | LM93 Status/Control                       | E2h     | 00h     | Gives Master error status, ASF reset control and Max PWM control                                                           |
| x                                                        | LM93 Configuration                        | E3h     | 00h     | Configures various outputs and provides START bit                                                                          |
| <b>SLEEP STATE CONTROL AND MASK REGISTERS</b>            |                                           |         |         |                                                                                                                            |
|                                                          | Sleep State Control                       | E4h     | 03h     | Used to communicate the system sleep state to the LM93                                                                     |
|                                                          | S1 GPI Mask                               | E5h     | FFh     | Sleep state S1 GPI error mask register                                                                                     |
|                                                          | S1 Fan Mask                               | E6h     | 0Fh     | Sleep state S1 fan tach error mask register                                                                                |
|                                                          | S3 GPI Mask                               | E7h     | FFh     | Sleep state S3 GPI error mask register                                                                                     |
|                                                          | S3 Fan Mask                               | E8h     | 0Fh     | Sleep state S3 fan tach error mask register                                                                                |
|                                                          | S3 Temperature/Voltage Mask               | E9h     | 07h     | Sleep state S3 temperature or voltage error mask register                                                                  |
|                                                          | S4/5 GPI Mask                             | EAh     | FFh     | Sleep state S4/5 GPI error mask register                                                                                   |
|                                                          | S4/5 Temperature/Voltage Mask             | EBh     | 07h     | Sleep state S4/5 temperature or voltage error mask register                                                                |
| <b>OTHER MASK REGISTERS</b>                              |                                           |         |         |                                                                                                                            |
|                                                          | GPI Error Mask                            | ECh     | FFh     | Error mask register for GPI faults                                                                                         |
|                                                          | Miscellaneous Error Mask                  | EDh     | 3Fh     | Error mask register for $\overline{\text{VRDx\_HOT}}$ , $\overline{\text{SCSI\_TERMx}}$ , and dynamic Vccp limit checking. |
| <b>ZONE 1 AND 2 TEMPERATURE READING OFFSET REGISTERS</b> |                                           |         |         |                                                                                                                            |
| x                                                        | Special Function Zone 1 Adjustment Offset | EEh     | 00h     | Allows all Zone 1 temperature measurements to be adjusted by a programmable offset                                         |
| x                                                        | Special Function Zone 2 Adjustment Offset | EFh     | 00h     | Allows all Zone 2 temperature measurements to be adjusted by a programmable offset                                         |
| <b>BLOCK COMMANDS</b>                                    |                                           |         |         |                                                                                                                            |
|                                                          | Block Write Command                       | F0h     | N/A     | SMBus Block Write Command Code                                                                                             |
|                                                          | Block Read Command                        | F1h     | N/A     | SMBus Block Write/Read Process call                                                                                        |
|                                                          | Fixed Block 0                             | F2h     | N/A     | Fixed block code address 40h, size 8 bytes                                                                                 |
|                                                          | Fixed Block 1                             | F3h     | N/A     | Fixed block code address 48h, size 8 bytes                                                                                 |
|                                                          | Fixed Block 2                             | F4h     | N/A     | Fixed block code address 50h, size 6 bytes                                                                                 |
|                                                          | Fixed Block 3                             | F5h     | N/A     | Fixed block code address 56h, size 16 bytes                                                                                |
|                                                          | Fixed Block 4                             | F6h     | N/A     | Fixed block code address 67h, size 4 bytes                                                                                 |
|                                                          | Fixed Block 5                             | F7h     | N/A     | Fixed block code address 6Eh, size 8 bytes                                                                                 |
|                                                          | Fixed Block 6                             | F8h     | N/A     | Fixed block code address 78h, size 12 bytes                                                                                |
|                                                          | Fixed Block 7                             | F9h     | N/A     | Fixed block code address 90h, size 32 bytes                                                                                |
|                                                          | Fixed Block 8                             | FAh     | N/A     | Fixed block code address B4h, size 8 bytes                                                                                 |
|                                                          | Fixed Block 9                             | FBh     | N/A     | Fixed block code address C8h, size 8 bytes                                                                                 |
|                                                          | Fixed Block 10                            | FCh     | N/A     | Fixed block code address D0h, size 16 bytes                                                                                |
|                                                          | Fixed Block 11                            | FDh     | N/A     | Fixed block code address E5h, size 9 bytes                                                                                 |
|                                                          | Reserved                                  | FEh-FFh | N/A     | Reserved for future commands                                                                                               |

### 3.17.3 FACTORY REGISTERS 00h–3Fh

#### 3.17.3.1 Register 00h XOR Test

| Register Address | Read/Write | Register Name | Bit 7   | Bit 6                                                                                                                                                                                  | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|---------------|
| 00h              | R/W        | XOR Test      |         |                                                                                                                                                                                        |       |       |       |       |       | XEN   | 00h           |
|                  |            |               |         |                                                                                                                                                                                        |       |       |       |       |       |       |               |
| Bit              | Name       | R/W           | Default | Description                                                                                                                                                                            |       |       |       |       |       |       | Sleep Masking |
| 0                | XEN        | R/W           | 0       | The LM93 incorporates an XOR tree test mode. When the test mode is enabled by setting this bit, the part enters XOR test mode. Clearing this bit brings the part out of XOR test mode. |       |       |       |       |       |       | N/A           |
| 7:1              | RES        | R             | 0       | Reserved                                                                                                                                                                               |       |       |       |       |       |       | N/A           |

The reserved bits of this register should only be used by the manufacturer for testing of the ASIC.

### 3.17.3.2 Register 01h SMBus Test

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 01h              | R/W        | SMBus Test    | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |

This register can be used to verify that the SMBus can read and write to the device without effecting any programmed settings.

### 3.17.3.3 Register 3Eh Manufacturer ID

| Register Address | Read/Write | Register Name   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 3Eh              | R          | Manufacturer ID | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 01h           |

The Manufacturer ID register contains the manufacturer identification number. This number is assigned by Texas Instruments and is a method for uniquely identifying the part manufacturer.

### 3.17.3.4 Register 3Fh Version/Stepping

| Register Address | Read/Write | Register Name    | Bit 7    | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------|----------|-------|-------|-------|----------|-------|-------|-------|---------------|
| 3Fh              | R          | Version/Stepping | VER[3:0] |       |       |       | STP[3:0] |       |       |       | 73h           |
|                  |            |                  | 0        | 1     | 1     | 1     | 0        | 0     | 1     | 1     |               |

The four least significant bits of the Version/Stepping register [3:0] contain the current stepping of the LM93 silicon. The four most significant bits [7:4] reflect the LM93 version number. The LM93 has a fixed version number of 0111b. For the first stepping of LM93, this register reads 01110000b. For the second stepping of the LM93, this register reads 01110001b and so on. It is incrementally increased for future versions for the silicon. The final released silicon has a stepping of 3h therefore this register reads 73h.

The register is used by application software to identify which device in the family of hardware monitoring ASICs has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Application software may use the current stepping to implement work-a-rounds for bugs found in a specific silicon stepping.

## 3.17.4 BMC ERROR STATUS REGISTERS 40h–47h

The B\_Error Status Registers contain several bits that each represent a particular error event that the LM93 can monitor. The LM93 sets a given bit whenever the corresponding error event occurs. The BMC\_ERR bit in the LM93 Status/Control register is also set if any bit in the BMC Error Status registers is set. If enabled,  $\overline{\text{ALERT}}$  is also asserted anytime BMC\_ERR is set. The exception to this is the fixed threshold error status bits in the  $\overline{\text{PROCHOT}}$  Error Status registers. They have no influence on BMC\_ERR or  $\overline{\text{ALERT}}$ .

Once a bit is set in the BMC Error Status registers, it is not automatically cleared by the LM93 if the error event goes away. Each bit must be cleared by software. If software attempts to clear a bit while the error condition still exists, and the error is unmasked, the bit does not clear. If the error is masked, the bit can be cleared even if the error condition still exists.

If the LM93 is in ASF mode, the BMC Error Status registers are both read-to-clear and write-one-to-clear. When not in ASF mode, the registers are only write-one-to-clear.

Each register described in this section has a column labeled **Sleep Masking**. This column describes which error events are masked in various sleep states. The sleep state of the system is communicated to the LM93 by writing to the Sleep State Control register. If a sleep state in this column has a '\*' next to it, it denotes that the error event is optionally masked in that sleep mode, depending on the Sleep State Mask registers.



**3.17.4.1 Register 40h B\_Error Status 1**

| Register Address | Read/Write | Register Name    | Bit 7                                                                                         | Bit 6 | Bit 5    | Bit 4    | Bit 3   | Bit 2   | Bit 1   | Bit 0   | Default Value |
|------------------|------------|------------------|-----------------------------------------------------------------------------------------------|-------|----------|----------|---------|---------|---------|---------|---------------|
| 40h              | RWC        | B_Error Status 1 | RES                                                                                           |       | VRD2_ERR | VRD1_ERR | ZN4_ERR | ZN3_ERR | ZN2_ERR | ZN1_ERR | 00h           |
| Bit              | Name       | R/W              | Description                                                                                   |       |          |          |         |         |         |         | Sleep Masking |
| 0                | ZN1_ERR    | RWC              | This bit is set when the zone 1 temperature has fallen outside the zone 1 temperature limits. |       |          |          |         |         |         |         | S3*, S4/5*    |
| 1                | ZN2_ERR    | RWC              | This bit is set when the zone 2 temperature has fallen outside the zone 2 temperature limits. |       |          |          |         |         |         |         | S3*, S4/5*    |
| 2                | ZN3_ERR    | RWC              | This bit is set when the zone 3 temperature has fallen outside the zone 3 temperature limits. |       |          |          |         |         |         |         | none          |
| 3                | ZN4_ERR    | RWC              | This bit is set when the zone 4 temperature has fallen outside the zone 4 temperature limits. |       |          |          |         |         |         |         | none          |
| 4                | VRD1_ERR   | RWC              | This bit is set when the $\overline{\text{VRD1\_HOT}}$ input has been asserted.               |       |          |          |         |         |         |         | S3, S4/5      |
| 5                | VRD2_ERR   | RWC              | This bit is set when the $\overline{\text{VRD2\_HOT\#}}$ input has been asserted.             |       |          |          |         |         |         |         | S3, S4/5      |
| 7:6              | RES        | R                | Reserved                                                                                      |       |          |          |         |         |         |         | N/A           |

**3.17.4.2 Register 41h B\_Error Status 2**

| Register Address | Read/Write | Register Name    | Bit 7                                                                                                                                     | Bit 6     | Bit 5     | Bit 4     | Bit 3     | Bit 2     | Bit 1     | Bit 0     | Default Value |
|------------------|------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---------------|
| 41h              | RWC        | B_Error Status 2 | ADIN8_ERR                                                                                                                                 | ADIN7_ERR | ADIN6_ERR | ADIN5_ERR | ADIN4_ERR | ADIN3_ERR | ADIN2_ERR | ADIN1_ERR | 00h           |
| Bit              | Name       | R/W              | Description                                                                                                                               |           |           |           |           |           |           |           | Sleep Masking |
| 0                | AD1_ERR    | RWC              | This bit is set when the AD_IN1 voltage has fallen outside the range defined by the AD_IN1 Low Limit and the AD_IN1 High Limit registers. |           |           |           |           |           |           |           | S3, S4/5      |
| 1                | AD2_ERR    | RWC              | This bit is set when the AD_IN2 voltage has fallen outside the range defined by the AD_IN2 Low Limit and the AD_IN2 High Limit registers. |           |           |           |           |           |           |           | S3, S4/5      |
| 2                | AD3_ERR    | RWC              | This bit is set when the AD_IN3 voltage has fallen outside the range defined by the AD_IN3 Low Limit and the AD_IN3 High Limit registers. |           |           |           |           |           |           |           | S3, S4/5      |
| 3                | AD4_ERR    | RWC              | This bit is set when the AD_IN4 voltage has fallen outside the range defined by the AD_IN4 Low Limit and the AD_IN4 High Limit registers. |           |           |           |           |           |           |           | S3, S4/5      |
| 4                | AD5_ERR    | RWC              | This bit is set when the AD_IN5 voltage has fallen outside the range defined by the AD_IN5 Low Limit and the AD_IN5 High Limit registers. |           |           |           |           |           |           |           | S3, S4/5      |
| 5                | AD6_ERR    | RWC              | This bit is set when the AD_IN6 voltage has fallen outside the range defined by the AD_IN6 Low Limit and the AD_IN6 High Limit registers. |           |           |           |           |           |           |           | S3, S4/5      |
| 6                | AD7_ERR    | RWC              | This bit is set when the AD_IN7 voltage has fallen outside the range defined by the AD_IN7 Low Limit and the AD_IN7 High Limit registers. |           |           |           |           |           |           |           | S3, S4/5      |
| 7                | AD8_ERR    | RWC              | This bit is set when the AD_IN8 voltage has fallen outside the range defined by the AD_IN8 Low Limit and the AD_IN8 High Limit registers. |           |           |           |           |           |           |           | S3, S4/5      |

**3.17.4.3 Register 42h B\_Error Status 3**

| Register Address | Read/Write | Register Name    | Bit 7                                                                                                                                        | Bit 6      | Bit 5      | Bit 4      | Bit 3      | Bit 2      | Bit 1      | Bit 0     | Default Value |
|------------------|------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------------|------------|------------|------------|------------|------------|-----------|---------------|
| 42h              | RWC        | B_Error Status 3 | ADIN16_ERR                                                                                                                                   | ADIN15_ERR | ADIN14_ERR | ADIN13_ERR | ADIN12_ERR | ADIN11_ERR | ADIN10_ERR | ADIN9_ERR | 00h           |
| Bit              | Name       | R/W              | Description                                                                                                                                  |            |            |            |            |            |            |           | Sleep Masking |
| 0                | AD9_ERR    | RWC              | This bit is set when the AD_IN9 voltage has fallen outside the range defined by the AD_IN9 Low Limit and the AD_IN9 High Limit registers.    |            |            |            |            |            |            |           | S3, S4/5      |
| 1                | AD10_ERR   | RWC              | This bit is set when the AD_IN10 voltage has fallen outside the range defined by the AD_IN10 Low Limit and the AD_IN10 High Limit registers. |            |            |            |            |            |            |           | S3, S4/5      |
| 2                | AD11_ERR   | RWC              | This bit is set when the AD_IN11 voltage has fallen outside the range defined by the AD_IN11 Low Limit and the AD_IN11 High Limit registers. |            |            |            |            |            |            |           | S3, S4/5      |



| Bit | Name     | R/W | Description                                                                                                                                  | Sleep Masking |
|-----|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 3   | AD12_ERR | RWC | This bit is set when the AD_IN12 voltage has fallen outside the range defined by the AD_IN12 Low Limit and the AD_IN12 High Limit registers. | S3*, S4/5*    |
| 4   | AD13_ERR | RWC | This bit is set when the AD_IN13 voltage has fallen outside the range defined by the AD_IN13 Low Limit and the AD_IN13 High Limit registers. | S3*, S4/5*    |
| 5   | AD14_ERR | RWC | This bit is set when the AD_IN14 voltage has fallen outside the range defined by the AD_IN14 Low Limit and the AD_IN14 High Limit registers. | S3*, S4/5*    |
| 6   | AD15_ERR | RWC | This bit is set when the AD_IN15 voltage has fallen outside the range defined by the AD_IN15 Low Limit and the AD_IN15 High Limit registers. | S3, S4/5      |
| 7   | AD16_ERR | RWC | This bit is set when the AD_IN16 voltage has fallen outside the range defined by the AD_IN16 Low Limit and the AD_IN16 High Limit registers. | none          |

#### 3.17.4.4 Register 43h B\_Error Status 4

| Register Address | Read/Write | Register Name    | Bit 7  | Bit 6  | Bit 5                   | Bit 4                   | Bit 3     | Bit 2     | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------|--------|--------|-------------------------|-------------------------|-----------|-----------|-------|-------|---------------|
| 43h              | RWC        | B_Error Status 4 | D2_ERR | D1_ERR | DV <sub>DD</sub> P2_ERR | DV <sub>DD</sub> P1_ERR | SCSI2_ERR | SCSI1_ERR | RES   |       | 00h           |

| Bit | Name                    | R/W | Description                                                                                                                      | Sleep Masking |
|-----|-------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------|---------------|
| 1:0 | RES                     | R   | Reserved                                                                                                                         | N/A           |
| 2   | SCSI1_ERR               | RWC | SCSI Fuse Error<br>This bit is set if SCSI_TERM1 has been asserted.                                                              | S3, S4/5      |
| 3   | SCSI2_ERR               | RWC | SCSI Fuse Error<br>This bit is set if SCSI_TERM2 has been asserted.                                                              | S3, S4/5      |
| 4   | DV <sub>DD</sub> P1_ERR | RWC | Dynamic Vccp Limit Error.<br>This bit is set if AD_IN7 (P1_Vccp) did not match the requested voltage as reported by P1_VID[5:0]. | S3, S4/5      |
| 5   | DV <sub>DD</sub> P2_ERR | RWC | Dynamic Vccp Limit Error.<br>This bit is set if AD_IN8 (P2_Vccp) did not match the requested voltage as reported by P1_VID[5:0]. | S3, S4/5      |
| 6   | D1_ERR                  | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE1+ and REMOTE1- pins.                     | S3*, S4/5*    |
| 7   | D2_ERR                  | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE2+ and REMOTE2- pins.                     | S3*, S4/5*    |

#### 3.17.4.5 Register 44h B\_P1\_PROCHOT Error Status

| Register Address | Read/Write | Register Name             | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------|---------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 44h              | RWC        | B_P1_PROCHOT Error Status | PH1_ERR | TMAX  | T100  | T75   | T50   | T25   | T12   | T0    | 00h           |

| Bit | Name | R/W | Description                                                                                                            | Sleep Masking |
|-----|------|-----|------------------------------------------------------------------------------------------------------------------------|---------------|
| 0   | T0   | RWC | Set when $\overline{P1\_PROCHOT}$ has had a throttled event. This bit is set for any amount of PROCHOT throttling >0%. | S3, S4/5      |
| 1   | T12  | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 0.39% but less than 12.5%.                    | S3, S4/5      |
| 2   | T25  | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 12.5% but less than 25%.                      | S3, S4/5      |
| 3   | T50  | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 25% but less than 50%.                        | S3, S4/5      |
| 4   | T75  | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 50% but less than 75%.                        | S3, S4/5      |
| 5   | T100 | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled greater than or equal to 75% but less than 100%.                       | S3, S4/5      |

| Bit | Name    | R/W | Description                                                               | Sleep Masking |
|-----|---------|-----|---------------------------------------------------------------------------|---------------|
| 6   | TMAX    | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled 100%.                     | S3, S4/5      |
| 7   | PH1_ERR | RWC | Set when $\overline{P1\_PROCHOT}$ has throttled more than the user limit. | S3, S4/5      |

The PH1\_ERR bit is the only bit in this register that will set BMC\_ERR in the LM93 Status/Control register.

### 3.17.4.6 Register 45h B\_P2\_PROCHOT Error Status

| Register Address | Read/Write | Register Name             | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------|---------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 45h              | RWC        | B_P2_PROCHOT Error Status | PH2_ERR | TMAX  | T100  | T75   | T50   | T25   | T12   | T0    | 00h           |

| Bit | Name    | R/W | Description                                                                                                            | Sleep Masking |
|-----|---------|-----|------------------------------------------------------------------------------------------------------------------------|---------------|
| 0   | T0      | RWC | Set when $\overline{P2\_PROCHOT}$ has had a throttled event. This bit is set for any amount of PROCHOT throttling >0%. | S3, S4/5      |
| 1   | T12     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 0.0% but less than 12.5%.                     | S3, S4/5      |
| 2   | T25     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 12.5% but less than 25%.                      | S3, S4/5      |
| 3   | T50     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 25% but less than 50%.                        | S3, S4/5      |
| 4   | T75     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 50% but less than 75%.                        | S3, S4/5      |
| 5   | T100    | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 75% but less than 100%.                       | S3, S4/5      |
| 6   | TMAX    | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled 100%.                                                                  | S3, S4/5      |
| 7   | PH2_ERR | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled more than the user limit.                                              | S3, S4/5      |

The PH2\_ERR bit is the only bit in this register that will set BMC\_ERR in the LM93 Status/Control register.

### 3.17.4.7 Register 46h B\_GPI Error Status

| Register Address | Read/Write | Register Name      | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------|----------|----------|----------|----------|----------|----------|----------|----------|---------------|
| 46h              | RWC        | B_GPI Error Status | GPI7_ERR | GPI6_ERR | GPI5_ERR | GPI4_ERR | GPI3_ERR | GPI2_ERR | GPI1_ERR | GPI0_ERR | 00h           |

| Bit | Name     | R/W | Description                                                                                   | Sleep Masking   |
|-----|----------|-----|-----------------------------------------------------------------------------------------------|-----------------|
| 0   | GPI0_ERR | RWC | This bit is set whenever GPIO0 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 1   | GPI1_ERR | RWC | This bit is set whenever GPIO1 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 2   | GPI2_ERR | RWC | This bit is set whenever GPIO2 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 3   | GPI3_ERR | RWC | This bit is set whenever GPIO3 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 4   | GPI4_ERR | RWC | This bit is set whenever GPIO4 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 5   | GPI5_ERR | RWC | This bit is set whenever GPIO5 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 6   | GPI6_ERR | RWC | This bit is set whenever GPIO6 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |

| Bit | Name     | R/W | Description                                                                                   | Sleep Masking   |
|-----|----------|-----|-----------------------------------------------------------------------------------------------|-----------------|
| 7   | GPI7_ERR | RWC | This bit is set whenever GPIO7 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |

### 3.17.4.8 Register 47h B\_Fan Error Status

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|----------|----------|----------|----------|---------------|
| 47h              | RWC        | B_Fan Error Status | RES   |       |       |       | FAN4_ERR | FAN3_ERR | FAN2_ERR | FAN1_ERR | 00h           |

| Bit | Name     | R/W | Description                                                                                                 | Sleep Masking  |
|-----|----------|-----|-------------------------------------------------------------------------------------------------------------|----------------|
| 0   | FAN1_ERR | RWC | This bit is set when the Fan Tach 1 value register is above the value set in the Fan Tach 1 Limit register. | S1*, S3*, S4/5 |
| 1   | FAN2_ERR | RWC | This bit is set when the Fan Tach 2 value register is above the value set in the Fan Tach 2 Limit register. | S1*, S3*, S4/5 |
| 2   | FAN3_ERR | RWC | This bit is set when the Fan Tach 3 value register is above the value set in the Fan Tach 3 Limit register. | S1*, S3*, S4/5 |
| 3   | FAN4_ERR | RWC | This bit is set when the Fan Tach 4 value register is above the value set in the Fan Tach 4 Limit register. | S1*, S3*, S4/5 |
| 7:4 | RES      | R   | Reserved                                                                                                    | N/A            |

### 3.17.5 HOST ERROR STATUS REGISTERS

The Host Error Status Registers contain several bits that each represent a particular error event that the LM93 can monitor. The LM93 sets a given bit whenever the corresponding error event occurs. The HOST\_ERR bit in the LM93 Status/Control register also sets if any bit in the Host Error Status registers is set. The exception to this is the fixed threshold error status bits in the PROCHOT Error Status registers. They have no influence on HOST\_ERR.

Once a bit is set in the Host Error Status registers, it is not automatically cleared by the LM93 if the error event goes away. Each bit must be cleared by software. If software attempts to clear a bit while the error condition still exists, the bit does not clear.

Software must specifically write a 1 to any bits it wishes to clear in the Host Error Status registers (write-one-to-clear).

Each register described in this section has a column labeled **Sleep Masking**. This column describes which error events are masked in various sleep states. The sleep state of the system is communicated to the LM93 by writing to the Sleep State Control register. If a sleep state in this column has a '\*' next to it, it denotes that the error event is optionally masked in that sleep mode, depending on the Sleep State Mask registers.

#### 3.17.5.1 Register 48h H\_Error Status 1

| Register Address | Read/Write | Register Name    | Bit 7 | Bit 6 | Bit 5    | Bit 4    | Bit 3   | Bit 2   | Bit 1   | Bit 0   | Default Value |
|------------------|------------|------------------|-------|-------|----------|----------|---------|---------|---------|---------|---------------|
| 48h              | RWC        | H_Error Status 1 | RES   |       | VRD2_ERR | VRD1_ERR | ZN4_ERR | ZN3_ERR | ZN2_ERR | ZN1_ERR | 00h           |

| Bit | Name    | R/W | Description                                                                                   | Sleep Masking |
|-----|---------|-----|-----------------------------------------------------------------------------------------------|---------------|
| 0   | ZN1_ERR | RWC | This bit is set when the zone 1 temperature has fallen outside the zone 1 temperature limits. | S3*, S4/5*    |
| 1   | ZN2_ERR | RWC | This bit is set when the zone 2 temperature has fallen outside the zone 2 temperature limits. | S3*, S4/5*    |
| 2   | ZN3_ERR | RWC | This bit is set when the zone 3 temperature has fallen outside the zone 3 temperature limits. | none          |

| Bit | Name     | R/W | Description                                                                                   | Sleep Masking |
|-----|----------|-----|-----------------------------------------------------------------------------------------------|---------------|
| 3   | ZN4_ERR  | RWC | This bit is set when the zone 4 temperature has fallen outside the zone 4 temperature limits. | none          |
| 4   | VRD1_ERR | RWC | This bit is set when the $\overline{\text{VRD1\_HOT}}$ input has been asserted.               | S3, S4/5      |
| 5   | VRD2_ERR | RWC | This bit is set when the $\overline{\text{VRD2\_HOT}}$ input has been asserted.               | S3, S4/5      |
| 7:6 | RES      | R   | Reserved                                                                                      | N/A           |

### 3.17.5.2 Register 49h H\_Error Status 2

| Register Address | Read/Write | Register Name    | Bit 7     | Bit 6     | Bit 5     | Bit 4     | Bit 3     | Bit 2     | Bit 1     | Bit 0     | Default Value |
|------------------|------------|------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---------------|
| 49h              | RWC        | H_Error Status 2 | ADIN8_ERR | ADIN7_ERR | ADIN6_ERR | ADIN5_ERR | ADIN4_ERR | ADIN3_ERR | ADIN2_ERR | ADIN1_ERR | 00h           |

| Bit | Name    | R/W | Description                                                                                                                               | Sleep Masking |
|-----|---------|-----|-------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 0   | AD1_ERR | RWC | This bit is set when the AD_IN1 voltage has fallen outside the range defined by the AD_IN1 Low Limit and the AD_IN1 High Limit registers. | S3, S4/5      |
| 1   | AD2_ERR | RWC | This bit is set when the AD_IN2 voltage has fallen outside the range defined by the AD_IN2 Low Limit and the AD_IN2 High Limit registers. | S3, S4/5      |
| 2   | AD3_ERR | RWC | This bit is set when the AD_IN3 voltage has fallen outside the range defined by the AD_IN3 Low Limit and the AD_IN3 High Limit registers. | S3, S4/5      |
| 3   | AD4_ERR | RWC | This bit is set when the AD_IN4 voltage has fallen outside the range defined by the AD_IN4 Low Limit and the AD_IN4 High Limit registers. | S3, S4/5      |
| 4   | AD5_ERR | RWC | This bit is set when the AD_IN5 voltage has fallen outside the range defined by the AD_IN5 Low Limit and the AD_IN5 High Limit registers. | S3, S4/5      |
| 5   | AD6_ERR | RWC | This bit is set when the AD_IN6 voltage has fallen outside the range defined by the AD_IN6 Low Limit and the AD_IN6 High Limit registers. | S3, S4/5      |
| 6   | AD7_ERR | RWC | This bit is set when the AD_IN7 voltage has fallen outside the range defined by the AD_IN7 Low Limit and the AD_IN7 High Limit registers. | S3, S4/5      |
| 7   | AD8_ERR | RWC | This bit is set when the AD_IN8 voltage has fallen outside the range defined by the AD_IN8 Low Limit and the AD_IN8 High Limit registers. | S3, S4/5      |

### 3.17.5.3 Register 4Ah H\_Error Status 3

| Register Address | Read/Write | Register Name    | Bit 7      | Bit 6      | Bit 5      | Bit 4      | Bit 3      | Bit 2      | Bit 1      | Bit 0     | Default Value |
|------------------|------------|------------------|------------|------------|------------|------------|------------|------------|------------|-----------|---------------|
| 4Ah              | RWC        | H_Error Status 3 | ADIN16_ERR | ADIN15_ERR | ADIN14_ERR | ADIN13_ERR | ADIN12_ERR | ADIN11_ERR | ADIN10_ERR | ADIN9_ERR | 00h           |

| Bit | Name     | R/W | Description                                                                                                                                  | Sleep Masking |
|-----|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 0   | AD9_ERR  | RWC | This bit is set when the AD_IN9 voltage has fallen outside the range defined by the AD_IN9 Low Limit and the AD_IN9 High Limit registers.    | S3, S4/5      |
| 1   | AD10_ERR | RWC | This bit is set when the AD_IN10 voltage has fallen outside the range defined by the AD_IN10 Low Limit and the AD_IN10 High Limit registers. | S3, S4/5      |
| 2   | AD11_ERR | RWC | This bit is set when the AD_IN11 voltage has fallen outside the range defined by the AD_IN11 Low Limit and the AD_IN11 High Limit registers. | S3, S4/5      |
| 3   | AD12_ERR | RWC | This bit is set when the AD_IN12 voltage has fallen outside the range defined by the AD_IN12 Low Limit and the AD_IN12 High Limit registers. | S3*, S4/5*    |
| 4   | AD13_ERR | RWC | This bit is set when the AD_IN13 voltage has fallen outside the range defined by the AD_IN13 Low Limit and the AD_IN13 High Limit registers. | S3*, S4/5*    |
| 5   | AD14_ERR | RWC | This bit is set when the AD_IN14 voltage has fallen outside the range defined by the AD_IN14 Low Limit and the AD_IN14 High Limit registers. | S3*, S4/5*    |
| 6   | AD15_ERR | RWC | This bit is set when the AD_IN15 voltage has fallen outside the range defined by the AD_IN15 Low Limit and the AD_IN15 High Limit registers. | S3, S4/5      |
| 7   | AD16_ERR | RWC | This bit is set when the AD_IN16 voltage has fallen outside the range defined by the AD_IN16 Low Limit and the AD_IN16 High Limit registers. | none          |

**3.17.5.4 Register 4Bh H\_Error Status 4**

| Register Address | Read/Write | Register Name    | Bit 7  | Bit 6  | Bit 5                   | Bit 4                   | Bit 3     | Bit 2     | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------|--------|--------|-------------------------|-------------------------|-----------|-----------|-------|-------|---------------|
| 4Bh              | RWC        | H_Error Status 4 | D2_ERR | D1_ERR | DV <sub>DD</sub> P2_ERR | DV <sub>DD</sub> P1_ERR | SCSI2_ERR | SCSI1_ERR | RES   |       | 00h           |

| Bit | Name                    | R/W | Description                                                                                                                      | Sleep Masking |
|-----|-------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------|---------------|
| 1:0 | RES                     | R   | Reserved                                                                                                                         | N/A           |
| 2   | SCSI1_ERR               | RWC | SCSI Fuse Error<br>This bit is set if <u>SCSI_TERM1</u> has been asserted.                                                       | S3, S4/5      |
| 3   | SCSI2_ERR               | RWC | SCSI Fuse Error<br>This bit is set if <u>SCSI_TERM2</u> has been asserted.                                                       | S3, S4/5      |
| 4   | DV <sub>DD</sub> P1_ERR | RWC | Dynamic Vccp Limit Error.<br>This bit is set if AD_IN7 (P1_Vccp) did not match the requested voltage as reported by P1_VID[5:0]. | S3, S4/5      |
| 5   | DV <sub>DD</sub> P2_ERR | RWC | Dynamic Vccp Limit Error.<br>This bit is set if AD_IN8 (P2_Vccp) did not match the requested voltage as reported by P1_VID[5:0]. | S3, S4/5      |
| 6   | D1_ERR                  | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE1+ and REMOTE1- pins.                     | S3*, S4/5*    |
| 7   | D2_ERR                  | RWC | Diode Fault Error<br>This bit is set if there is an open or short circuit on the REMOTE2+ and REMOTE2- pins.                     | S3*, S4/5*    |

**3.17.5.5 Register 4Ch H\_P1\_PROCHOT Error Status**

| Register Address | Read/Write | Register Name             | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------|---------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 4Ch              | RWC        | H_P1_PROCHOT Error Status | PH1_ERR | TMAX  | T100  | T75   | T50   | T25   | T12   | T0    | 00h           |

| Bit | Name    | R/W | Description                                                                                                     | Sleep Masking |
|-----|---------|-----|-----------------------------------------------------------------------------------------------------------------|---------------|
| 0   | T0      | RWC | Set when <u>P1_PROCHOT</u> has had a throttled event. This bit is set for any amount of PROCHOT throttling >0%. | S3, S4/5      |
| 1   | T12     | RWC | Set when <u>P1_PROCHOT</u> has throttled greater than or equal to 0.00% but less than 12.5%.                    | S3, S4/5      |
| 2   | T25     | RWC | Set when <u>P1_PROCHOT</u> has throttled greater than or equal to 12.5% but less than 25%.                      | S3, S4/5      |
| 3   | T50     | RWC | Set when <u>P1_PROCHOT</u> has throttled greater than or equal to 25% but less than 50%.                        | S3, S4/5      |
| 4   | T75     | RWC | Set when <u>P1_PROCHOT</u> has throttled greater than or equal to 50% but less than 75%.                        | S3, S4/5      |
| 5   | T100    | RWC | Set when <u>P1_PROCHOT</u> has throttled greater than or equal to 75% but less than 100%.                       | S3, S4/5      |
| 6   | TMAX    | RWC | Set when <u>P1_PROCHOT</u> has throttled 100%.                                                                  | S3, S4/5      |
| 7   | PH1_ERR | RWC | Set when <u>P1_PROCHOT</u> has throttled more than the user limit.                                              | S3, S4/5      |

The PH1\_ERR bit is the only bit in this register that will set HOST\_ERR in the LM93 Status/Control register.

**3.17.5.6 Register 4Dh B\_P2\_PROCHOT Error Status**

| Register Address | Read/Write | Register Name             | Bit 7   | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------|---------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 4Dh              | RWC        | H_P2_PROCHOT Error Status | PH2_ERR | TMAX  | T100  | T75   | T50   | T25   | T12   | T0    | 00h           |

| Bit | Name    | R/W | Description                                                                                                                         | Sleep Masking |
|-----|---------|-----|-------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 0   | T0      | RWC | Set when $\overline{P2\_PROCHOT}$ has had a throttled event. This bit is set for any amount of $\overline{PROCHOT}$ throttling >0%. | S3, S4/5      |
| 1   | T12     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 0.00% but less than 12.5%.                                 | S3, S4/5      |
| 2   | T25     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 12.5% but less than 25%.                                   | S3, S4/5      |
| 3   | T50     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 25% but less than 50%.                                     | S3, S4/5      |
| 4   | T75     | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 50% but less than 75%.                                     | S3, S4/5      |
| 5   | T100    | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled greater than or equal to 75% but less than 100%.                                    | S3, S4/5      |
| 6   | TMAX    | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled 100%.                                                                               | S3, S4/5      |
| 7   | PH2_ERR | RWC | Set when $\overline{P2\_PROCHOT}$ has throttled more than the user limit.                                                           | S3, S4/5      |

The PH2\_ERR bit is the only bit in this register that will set HOST\_ERR in the LM93 Status/Control register.

### 3.17.5.7 Register 4Eh H\_GPI Error Status

| Register Address | Read/Write | Register Name      | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------|----------|----------|----------|----------|----------|----------|----------|----------|---------------|
| 4Eh              | RWC        | H_GPI Error Status | GPI7_ERR | GPI6_ERR | GPI5_ERR | GPI4_ERR | GPI3_ERR | GPI2_ERR | GPI1_ERR | GPI0_ERR | 00h           |

| Bit | Name     | R/W | Description                                                                                   | Sleep Masking   |
|-----|----------|-----|-----------------------------------------------------------------------------------------------|-----------------|
| 0   | GPI0_ERR | RWC | This bit is set whenever GPIO0 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 1   | GPI1_ERR | RWC | This bit is set whenever GPIO1 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 2   | GPI2_ERR | RWC | This bit is set whenever GPIO2 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 3   | GPI3_ERR | RWC | This bit is set whenever GPIO3 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 4   | GPI4_ERR | RWC | This bit is set whenever GPIO4 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 5   | GPI5_ERR | RWC | This bit is set whenever GPIO5 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 6   | GPI6_ERR | RWC | This bit is set whenever GPIO6 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |
| 7   | GPI7_ERR | RWC | This bit is set whenever GPIO7 is driven low (unless masked via the GPI Error Mask register). | S1*, S3*, S4/5* |

### 3.17.5.8 Register 4Fh H\_Fan Error Status

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|----------|----------|----------|----------|---------------|
| 4Fh              | RWC        | H_Fan Error Status | RES   |       |       |       | FAN4_ERR | FAN3_ERR | FAN2_ERR | FAN1_ERR | 00h           |

| Bit | Name     | R/W | Description                                                                                                 | Sleep Masking  |
|-----|----------|-----|-------------------------------------------------------------------------------------------------------------|----------------|
| 0   | FAN1_ERR | RWC | This bit is set when the Fan Tach 1 value register is above the value set in the Fan Tach 1 Limit register. | S1*, S3*, S4/5 |
| 1   | FAN2_ERR | RWC | This bit is set when the Fan Tach 2 value register is above the value set in the Fan Tach 2 Limit register. | S1*, S3*, S4/5 |

| Bit | Name     | R/W | Description                                                                                                 | Sleep Masking  |
|-----|----------|-----|-------------------------------------------------------------------------------------------------------------|----------------|
| 2   | FAN3_ERR | RWC | This bit is set when the Fan Tach 3 value register is above the value set in the Fan Tach 3 Limit register. | S1*, S3*, S4/5 |
| 3   | FAN4_ERR | R   | This bit is set when the Fan Tach 4 value register is above the value set in the Fan Tach 4 Limit register. | S1*, S3*, S4/5 |
| 7:4 | RES      | R   | Reserved                                                                                                    | N/A            |

### 3.17.6 VALUE REGISTERS

#### 3.17.6.1 Registers 50–53h Unfiltered Temperature Value Registers

| Register Address | Read/Write | Register Name                  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 50h              | R          | Zone 1 (CPU1) Temp             | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 51h              | R          | Zone 2 (CPU1) Temp             | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 52h              | R          | Zone 3 (Internal) Temp         | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 53h              | R/W        | Zone 4 (External Digital) Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |

Zones 1, 2 and 3 are all automatically updated by the LM93. The Zone 4 (External Digital) Temp register must be written by an external SMBus device.

The temperature registers for zones 1 and 2 must return a value of 80h if the remote diode pins are not implemented by the board designer or are not functioning properly.

#### 3.17.6.2 Registers 54–55h Filtered Temperature Value Registers

| Register Address | Read/Write | Register Name               | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 54h              | R          | Zone 1 (CPU1) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 55h              | R          | Zone 2 (CPU1) Filtered Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

These registers reflect the temperature of zones 1 and 2 after the spike smoothing filter has been applied.

The characteristics of the filtering can be adjusted by using the Zones 1/2 Spike Smoothing Control register.

#### 3.17.6.3 Register 56–65h A/D Channel Voltage Registers

| Register Address | Read/Write | Register Name  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 56h              | R          | AD_IN1 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 57h              | R          | AD_IN2 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 58h              | R          | AD_IN3 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 59h              | R          | AD_IN4 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |



| Register Address | Read/Write | Register Name   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 5Ah              | R          | AD_IN5 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Bh              | R          | AD_IN6 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Ch              | R          | AD_IN7 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Dh              | R          | AD_IN8 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Eh              | R          | AD_IN9 Voltage  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 5Fh              | R          | AD_IN10 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 60h              | R          | AD_IN11 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 61h              | R          | AD_IN12 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 62h              | R          | AD_IN13 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 63h              | R          | AD_IN14 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 64h              | R          | AD_IN15 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| 65h              | R          | AD_IN16 Voltage | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |

The voltage reading registers reflect the current voltage of the LM93 voltage monitoring inputs. Voltages are presented in the registers at  $\frac{3}{4}$  full scale for the nominal voltage. Therefore, at nominal voltage, each register reads C0h.

#### 3.17.6.4 Register 67h Current P1\_PROCHOT

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 67h              | R          | Current P1_PROCHOT | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

This is the value of the PROCHOT percentage active time for Processor 1 at the end of each PROCHOT monitoring interval as set by the PROCHOT Time Interval register. Writing to this register does not effect the register contents, but does restart the capture cycle for both PROCHOT channels (P1\_PROCHOT and P2\_PROCHOT). A register value of one represents anything greater than 0% but less than 0.39% of active time.

| Register Value (Decimal) | Percentage Active Time |
|--------------------------|------------------------|
| 0                        | 0%                     |
| 1                        | 0.39%                  |
| 2                        | 0.78%                  |
| •                        | •                      |
| •                        | •                      |
| •                        | •                      |
| n                        | $n/256 * 100$          |
| 255                      | 99.60%                 |



**3.17.6.5 Register 68h Average P1\_PROCHOT**

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 68h              | R          | Average P1_PROCHOT | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |

This is the average percentage active time of  $\overline{P1\_PROCHOT}$ . It is the result of adding the contents of this register to the contents of the Current  $\overline{P1\_PROCHOT}$  register and dividing the result by 2. The update occurs at the same time that the Current  $\overline{P1\_PROCHOT}$  register gets updated. A register value of one represents anything greater than 0% but less than 0.39% of active time.

**3.17.6.6 Register 69h Current P2\_PROCHOT**

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 69h              | R          | Current P2_PROCHOT | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |

This is the value of the  $\overline{PROCHOT}$  percentage active time for Processor 2 at the end of each  $\overline{PROCHOT}$  monitoring interval as set by the  $\overline{PROCHOT}$  Time Interval register. Writing to this register does not effect the register contents, but does restart the capture cycle for both  $\overline{PROCHOT}$  channels ( $\overline{P1\_PROCHOT}$  and  $\overline{P2\_PROCHOT}$ ). A register value of one represents anything greater than 0% but less than 0.39% of active time.

| Register Value (Decimal) | Percentage Active Time |
|--------------------------|------------------------|
| 0                        | 0%                     |
| 1                        | 0.39%                  |
| 2                        | 0.78%                  |
| •                        | •                      |
| •                        | •                      |
| •                        | •                      |
| n                        | $n/256 \times 100$     |
| 255                      | 99.60%                 |

**3.17.6.7 Register 6Ah Average P2\_PROCHOT**

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 6Ah              | R          | Average P2_PROCHOT | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |

This is the average percentage active time of  $\overline{P2\_PROCHOT}$ . It is the result of adding the contents of this register to the contents of the Current  $\overline{P2\_PROCHOT}$  register and dividing the result by 2. The update occurs at the same time that the Current  $\overline{P2\_PROCHOT}$  register gets updated. A register value of one represents anything greater than 0% but less than 0.39% of active time.

**3.17.6.8 Register 6Bh GPI State**

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 6Bh              | R          | GPI State     | GPI7  | GPI6  | GP15  | GPI4  | GPI3  | GPI2  | GPI1  | GPI0  | N/D           |

| Bit | Name | Read/Write | Description              |
|-----|------|------------|--------------------------|
| 0   | GPI0 | R          | 1 if GPIO_0 input is LOW |
| 1   | GPI1 | R          | 1 if GPIO_1 input is LOW |
| 2   | GPI2 | R          | 1 if GPIO_2 input is LOW |
| 3   | GPI3 | R          | 1 if GPIO_3 input is LOW |
| 4   | GPI4 | R          | 1 if GPIO_4 input is LOW |
| 5   | GPI5 | R          | 1 if GPIO_5 input is LOW |
| 6   | GPI6 | R          | 1 if GPIO_6 input is LOW |
| 7   | GPI7 | R          | 1 if GPIO_7 input is LOW |

### 3.17.6.9 Register 6Ch P1\_VID

| Register Address | Read/Write | Register Name | Bit 7                                                                                                                                                                                        | Bit 6 | Bit 5  | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |     |
|------------------|------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|-------|-------|-------|-------|-------|---------------|-----|
| 6Ch              | R          | P1_VID        | RES                                                                                                                                                                                          |       | P1_VID |       |       |       |       |       |               | N/D |
| Bit              | Name       | Read/Write    | Description                                                                                                                                                                                  |       |        |       |       |       |       |       |               |     |
| 5:0              | P1_VID     | R             | Processor 1 VID status.<br>Reports the current value of the P1_VID5 through P1_VID0 pins. This register should only be updated if P1_VID5 through P1_VID0 remain stable for at least 600 ns. |       |        |       |       |       |       |       |               |     |
| 7:6              | RES        | R             | Reserved                                                                                                                                                                                     |       |        |       |       |       |       |       |               |     |

### 3.17.6.10 Register 6Dh P2\_VID

| Register Address | Read/Write | Register Name | Bit 7                                                                                                                                                                                       | Bit 6 | Bit 5  | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |     |
|------------------|------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|-------|-------|-------|-------|-------|---------------|-----|
| 6Dh              | R          | P2_VID        | RES                                                                                                                                                                                         |       | P2_VID |       |       |       |       |       |               | N/D |
| Bit              | Name       | Read/Write    | Description                                                                                                                                                                                 |       |        |       |       |       |       |       |               |     |
| 5:0              | P2_VID     | R             | Processor 2VID status.<br>Reports the current value of the P2_VID5 through P2_VID0 pins. This register should only be updated if P2_VID5 through P2_VID0 remain stable for at least 600 ns. |       |        |       |       |       |       |       |               |     |
| 7:6              | RES        | R             | Reserved                                                                                                                                                                                    |       |        |       |       |       |       |       |               |     |

### 3.17.6.11 Register 6E–75h Fan Tachometer Readings

| Register Address | Read/Write | Register Name  | Bit 7       | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |     |
|------------------|------------|----------------|-------------|-------|-------|-------|-------|-------|-------|-------|---------------|-----|
| 6Eh              | R          | Fan Tach 1 LSB | TACH[5:0]   |       |       |       |       |       |       | RES   |               | N/D |
| 6Fh              | R          | Fan Tach 1 MSB | TACH[13:6]  |       |       |       |       |       |       |       |               | N/D |
| 70h              | R          | Fan Tach 2 LSB | TACH2[5:0]  |       |       |       |       |       |       | RES   |               | N/D |
| 71h              | R          | Fan Tach 2 MSB | TACH2[13:6] |       |       |       |       |       |       |       |               | N/D |
| 72h              | R          | Fan Tach 3 LSB | TACH3[5:0]  |       |       |       |       |       |       | RES   |               | N/D |
| 73h              | R          | Fan Tach 3 MSB | TACH3[13:6] |       |       |       |       |       |       |       |               | N/D |
| 74h              | R          | Fan Tach 4 LSB | TACH4[5:0]  |       |       |       |       |       |       | RES   |               | N/D |

| Register Address | Read/Write | Register Name        | Bit 7       | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------|-------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 75h              | R          | Fan Tach<br>4<br>MSB | TACH4[13:6] |       |       |       |       |       |       |       | N/D           |

The 14-bit fan tach readings indicate the number of 22.5 kHz clock periods that occurred during two full periods of the tachometer input signal. Most fans produce two tachometer pulses per full revolution. These registers must be updated at least once every second.

The fan tachometer reading registers must always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional. 3FFFh indicates that the fan is stalled, not spinning fast enough to measure, or the tachometer input is not connected to a valid signal.

If the pulses per revolution of the fan is known, the RPM can be calculated with the following equation:

$$\text{RPM} = 22500 \text{ cycles/sec} * 60 \text{ sec/min} * 2 \text{ pulses} / \text{COUNT cycles} / \text{PULSES\_PER\_REV}$$

where:

- PULSES\_PER\_REV = the number of pulses that the fan produces per revolution
- COUNT = The 14-bit value read from the tach register

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### 3.17.7 LIMIT REGISTERS

#### 3.17.7.1 Registers 78–7Fh Temperature Limit Registers

| Register Address | Read/Write | Register Name                               | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 78h              | R/W        | Processor 1<br>(Zone1)<br>Low Temp          | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 79h              | R/W        | Processor 1<br>(Zone1)<br>High Temp         | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Ah              | R/W        | Processor 2<br>(Zone2)<br>Low Temp          | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Bh              | R/W        | Processor 2<br>(Zone2)<br>High Temp         | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Ch              | R/W        | Internal<br>(Zone3)<br>Low Temp             | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Dh              | R/W        | Internal<br>(Zone3)<br>High Temp            | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Eh              | R/W        | External<br>Digital<br>(Zone4)<br>Low Temp  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |
| 7Fh              | R/W        | External<br>Digital<br>(Zone4)<br>High Temp | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 80h           |

If an external temperature input or the internal temperature sensor either exceeds the value set in the high limit register or falls below the value set in the low limit register, the corresponding bit in the B\_ and H\_Error Status 1 register is set automatically by the LM93. For example, if the temperature read from the Remote1- and Remote1+ inputs exceeds the Processor (Zone1) High Temp register limit setting, the ZN1\_ERR bit in both B\_Error Status 1 and H\_Error Status 1 registers is set. The temperature limits in these registers is represented as 8 bit, 2's complement, signed numbers in Celsius.

If any high temp limit register is set to 80h then the B\_ and H\_Error Status register bit for that temperature channel is masked.

### 3.17.7.2 Registers 80–83h Fan Boost Temperature Registers

| Register Address | Read/Write | Register Name         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 80h              | R/W        | Fan Boost Temp Zone 1 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 3Ch           |
| 81h              | R/W        | Fan Boost Temp Zone 2 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 3Ch           |
| 82h              | R/W        | Fan Boost Temp Zone 3 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 23h           |
| 83h              | R/W        | Fan Boost Temp Zone 4 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 23h           |

If any thermal zone exceeds the temperature set in the Fan Boost Limit register, both of the PWM outputs are set to 100%. The fan boost function takes precedence over manual override. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event. If set to 7Fh and the fan control temperature resolution is 1°C, the feature is disabled.

Default = 60°C = 3Ch for zones 1 and 2

Default = 35°C = 23h for zones 3 and 4

The temperature has to fall the number of degrees specified in the Fan Boost Hysteresis registers, below this temperature to cause the PWM outputs to return to normal operation.

### 3.17.7.3 Registers 90–AFh Voltage Limit Registers

| Register Address | Read/Write | Register Name     | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 90h              | R/W        | AD_IN1 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 91h              | R/W        | AD_IN1 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 92h              | R/W        | AD_IN2 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 93h              | R/W        | AD_IN2 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 94h              | R/W        | AD_IN3 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 95h              | R/W        | AD_IN3 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 96h              | R/W        | AD_IN4 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 97h              | R/W        | AD_IN4 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 98h              | R/W        | AD_IN5 Low Limit   | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 99h              | R/W        | AD_IN5 High Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 9Ah              | R/W        | AD_IN6 Low Limit   | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 9Bh              | R/W        | AD_IN6 High Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 9Ch              | R/W        | AD_IN7 Low Limit   | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 9Dh              | R/W        | AD_IN7 High Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| 9Eh              | R/W        | AD_IN8 Low Limit   | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| 9Fh              | R/W        | AD_IN8 High Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A0h              | R/W        | AD_IN9 Low Limit   | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A1h              | R/W        | AD_IN9 High Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A2h              | R/W        | AD_IN10 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A3h              | R/W        | AD_IN10 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A4h              | R/W        | AD_IN11 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A5h              | R/W        | AD_IN11 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A6h              | R/W        | AD_IN12 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A7h              | R/W        | AD_IN12 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A8h              | R/W        | AD_IN13 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A9h              | R/W        | AD_IN13 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| AAh              | R/W        | AD_IN14 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| ABh              | R/W        | AD_IN14 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| ACh              | R/W        | AD_IN15 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| ADh              | R/W        | AD_IN15 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| A Eh             | R/W        | AD_IN16 Low Limit  | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 00h           |
| A Fh             | R/W        | AD_IN16 High Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |

FFh as the high limit acts as a mask for that voltage sensor and so prevents this channel from being able to set the associated error status bit in the B\_ or H\_ Error Status registers, for both high and low limit errors.

If a voltage input either exceeds the value set in the voltage high limit register or falls below the value set in the voltage low limit register, the corresponding bit is set automatically by the LM93 in the B\_ and H\_ Error Status registers.

### 3.17.7.4 Register B0–B1h PROCHOT User Limit Registers

| Register Address | Read/Write | Register Name                   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| B0h              | R/W        | <u>P1_PROCHOT</u><br>User Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |
| B1h              | R/W        | <u>P2_PROCHOT</u><br>User Limit | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | FFh           |

These registers allow a user limit to be set for the PROCHOT monitoring function. If the corresponding Current Px\_PROCHOT register exceeds this value, the PH1\_ERR or PH2\_ERR bit is set in the corresponding Host and BMC error status registers. A value of FFh acts as a mask and prevents the error status bits from being set.

| Register Value (Decimal) | Threshold Percentage |
|--------------------------|----------------------|
| 0                        | 0%                   |
| 1                        | 0.39%                |
| 2                        | 0.78%                |
| •                        | •                    |
| •                        | •                    |
| •                        | •                    |
| n                        | $n/256 \times 100$   |
| 255                      | 99.60%               |

### 3.17.7.5 Register B2–B3h Dynamic Vccp Limit Offset Registers

| Register Address | Read/Write | Register Name             | Bit 7         | Bit 6 | Bit 5 | Bit 4 | Bit 3         | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------|---------------|-------|-------|-------|---------------|-------|-------|-------|---------------|
| B2h              | R/W        | Vccp1<br>Limit<br>Offsets | UPPER_OFFSET1 |       |       |       | LOWER_OFFSET1 |       |       |       | 17h           |
| B3h              | R/W        | Vccp2<br>Limit<br>Offsets | UPPER_OFFSET2 |       |       |       | LOWER_OFFSET2 |       |       |       | 17h           |

These offsets are used to determine the upper and lower limits of the dynamic Vccp window comparator. These offsets are added or subtracted from the value selected by the VID bits.

| LOWER_OFFSET1 or<br>LOWER_OFFSET2 | Lower Offset |
|-----------------------------------|--------------|
| 0h                                | 25 mV        |
| 1h                                | 50 mV        |
| 2h                                | 75 mV        |
| 3h                                | 100 mV       |
| ~ ~                               | ~ ~          |
| Ch                                | 325 mV       |
| Dh                                | 350 mV       |
| Eh                                | 375 mV       |
| Fh                                | 400 mV       |

| UPPER_OFFSET1 or<br>UPPER_OFFSET2 | Upper Offset |
|-----------------------------------|--------------|
| 0h                                | 12.5 mV      |
| 1h                                | 25 mV        |
| 2h                                | 37.5 mV      |
| 3h                                | 50 mV        |
| ~ ~                               | ~ ~          |
| Dh                                | 175 mV       |
| Eh                                | 187.5 mV     |
| Fh                                | 200 mV       |

### 3.17.7.6 Register B4–BBh Fan Tach Limit Registers

| Register Address | Read/Write | Register Name        | Bit 7         | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |     |
|------------------|------------|----------------------|---------------|-------|-------|-------|-------|-------|-------|-------|---------------|-----|
| B4h              | R/W        | Fan Tach 1 Limit LSB | TLIMIT1[5:0]  |       |       |       |       |       | RES   |       | FCh           |     |
| B5h              | R/W        | Fan Tach 1 Limit MSB | TLIMIT1[13:6] |       |       |       |       |       |       |       |               | FFh |
| B6h              | R/W        | Fan Tach 2 Limit LSB | TLIMIT2[5:0]  |       |       |       |       |       | RES   |       | FCh           |     |
| B7h              | R/W        | Fan Tach 2 Limit MSB | TLIMIT2[13:6] |       |       |       |       |       |       |       |               | FFh |
| B8h              | R/W        | Fan Tach 3 Limit LSB | TLIMIT3[5:0]  |       |       |       |       |       | RES   |       | FCh           |     |
| B9h              | R/W        | Fan Tach 3 Limit MSB | TLIMIT3[13:6] |       |       |       |       |       |       |       |               | FFh |
| BAh              | R/W        | Fan Tach 4 Limit LSB | TLIMIT4[5:0]  |       |       |       |       |       | RES   |       | FCh           |     |
| BBh              | R/W        | Fan Tach 4 Limit MSB | TLIMIT4[13:6] |       |       |       |       |       |       |       |               | FFh |

If a tachometer reading exceeds its limit (as defined by these registers) the corresponding bit is set in the Host and BMC Error Status registers. The fan tachometer readings can be associated with a particular PWM output, but the tach errors are not automatically masked when a PWM is at 0% or set to level that causes the fan RPM to be below the limit purposely. In order to prevent false errors, care needs to be taken to make sure that the Fan Tach Limits are properly set. Errors are never generated for a fan if its limit is set to 3FFFh.

### 3.17.8 SETUP REGISTERS

#### 3.17.8.1 Register BCh Special Function Control 1 (Voltage Hysteresis and Fan Control Filter Enable)

| Register Address | Read/Write | Register Name              | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| BCh              | R/W        | Special Function Control 1 | RES   | FCFE2 | FCFE1 | LCFE2 | LCFE1 | VH    |       |       | 00h           |

| Bit | Name  | R/W | Description                                                                                                                                                                                                                                                             |
|-----|-------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | VH    | R/W | Voltage hysteresis control. This determines the amount of hysteresis to be applied to all voltage limit comparisons. It applies to both high and low limits. One LSB equals one A/D count, so the actual voltage represented by one LSB depends on the voltage channel. |
| 3   | LCFE1 | R/W | Limit Comparison Filter Enable. Setting this bit causes limit comparisons for temperature zone 1 to use the filtered (spike smoothed) temperature instead of the unfiltered temperature.                                                                                |
| 4   | LCFE2 | R/W | Limit Comparison Filter Enable. Setting this bit causes limit comparisons for temperature zone 2 to use the filtered (spike smoothed) temperature instead of the unfiltered temperature.                                                                                |
| 5   | FCFE1 | R/W | Fan Control Filter Enable. Setting this bit causes fan control functions for zone 1 (including fan boost) to use the filtered (spike smoothed) temperature instead of the unfiltered temperature.                                                                       |
| 6   | FCFE2 | R/W | Fan Control Filter Enable. Setting this bit causes fan control functions for zone 2 (including fan boost) to use the filtered (spike smoothed) temperature instead of the unfiltered temperature.                                                                       |
| 7   | RES   | R   | Reserved                                                                                                                                                                                                                                                                |

In order for the LCFE1, LCFE2, FCFE1 and FCFE2 bits to work correctly, the ZN1E and ZN2E bits in the Zones 1/2 Spike Smoothing Control register should be cleared.

**Application Note:** If hysteresis for voltage limit comparisons is non-zero, special care needs to be taken when changing the voltage limit registers while a voltage error condition exists. If software relaxes the voltage limits in an attempt to prevent an error condition, it may be necessary to relax the limits by an amount greater than the hysteresis value and wait several milliseconds before attempting to clear the error status bit for the given voltage channel. Once the error status bit has been cleared, the desired limit(s) can be programmed.

#### 3.17.8.2 Register BDh Special Function Control 2 (Smart Tach Mode Enable and Fan Control Temperature Resolution Control)

| Register Address | Read/Write | Register Name              | Bit 7 | Bit 6 | Bit 5   | Bit 4   | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------|-------|-------|---------|---------|-------|-------|-------|-------|---------------|
| BDh              | R/W        | Special Function Control 2 | RES   | RES   | ZN34_RS | ZN12_RS | STE4  | STE3  | STE2  | STE1  | 00h           |

| Bit | Name    | R/W | Description                                                                               |
|-----|---------|-----|-------------------------------------------------------------------------------------------|
| 0   | STE1    | R/W | Enable Smart Tach for Tach 1                                                              |
| 1   | STE2    | R/W | Enable Smart Tach for Tach 2                                                              |
| 2   | STE3    | R/W | Enable Smart Tach for Tach 3                                                              |
| 3   | STE4    | R/W | Enable Smart Tach for Tach 4                                                              |
| 4   | ZN12_RS | R/W | When this bit is set, the auto fan control will use 0.5°C of resolution for zones 1 and 2 |
| 5   | ZN34_RS | R/W | When this bit is set, the auto fan control will use 0.5°C of resolution for zones 3 and 4 |
| 6   | RES     | R   | Reserved                                                                                  |
| 7   | RES     | R   | Reserved                                                                                  |



**Application Note:** Enabling Smart Tach mode is not supported while either PWM output is configured for 22.5 kHz. The behavior of the part is undefined if this configuration is programmed. Register E0h Special Function TACH to PWM Binding must be setup when Smart Tach modes are enabled.

### 3.17.8.3 Register BEh GPI/VID Level Control

| Register Address | Read/Write | Register Name         | Bit 7                                                                   | Bit 6    | Bit 5    | Bit 4    | Bit 3 | Bit 2 | Bit 1      | Bit 0      | Default Value |
|------------------|------------|-----------------------|-------------------------------------------------------------------------|----------|----------|----------|-------|-------|------------|------------|---------------|
| BEh              | R/W        | GPI/VID Level Control | GPI7_LVL                                                                | GPI6_LVL | GPI5_LVL | GPI4_LVL | RES   |       | P2_VID_LVL | P1_VID_LVL | 00h           |
| Bit              | Name       | R/W                   | Description                                                             |          |          |          |       |       |            |            |               |
| 0                | P1_VID_LVL | R/W                   | If set, P1_VIDx inputs use alternate lower $V_{IH}$ and $V_{IL}$ levels |          |          |          |       |       |            |            |               |
| 1                | P2_VID_LVL | R/W                   | If set, P2_VIDx inputs use alternate lower $V_{IH}$ and $V_{IL}$ levels |          |          |          |       |       |            |            |               |
| 3:2              | RES        | R                     | Reserved                                                                |          |          |          |       |       |            |            |               |
| 4                | GPI4_LVL   | R/W                   | If set, GPIO4 input use alternate lower $V_{IH}$ and $V_{IL}$ levels    |          |          |          |       |       |            |            |               |
| 5                | GPI5_LVL   | R/W                   | If set, GPIO5 input use alternate lower $V_{IH}$ and $V_{IL}$ levels    |          |          |          |       |       |            |            |               |
| 6                | GPI6_LVL   | R/W                   | If set, GPIO6 input use alternate lower $V_{IH}$ and $V_{IL}$ levels    |          |          |          |       |       |            |            |               |
| 7                | GPI7_LVL   | R/W                   | If set, GPIO7 input use alternate lower $V_{IH}$ and $V_{IL}$ levels    |          |          |          |       |       |            |            |               |

See the [DC Electrical Characteristics](#) for exact  $V_{IH}$  and  $V_{IL}$  levels.

### 3.17.8.4 Register BFh PWM Ramp Control

| Register Address | Read/Write | Register Name    | Bit 7                                                                                                   | Bit 6 | Bit 5 | Bit 4 | Bit 3    | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|------------------|---------------------------------------------------------------------------------------------------------|-------|-------|-------|----------|-------|-------|-------|---------------|
| BFh              | R/W        | PWM Ramp Control | PH_RAMP                                                                                                 |       |       |       | VRD_RAMP |       |       |       | 00h           |
| Bit              | Name       | R/W              | Description                                                                                             |       |       |       |          |       |       |       |               |
| 3:0              | VRD_RAMP   | R/W              | Sets the time delay between ramp steps for the $\overline{VRDx\_HOT}$ ramp up/ramp down PWM function.   |       |       |       |          |       |       |       |               |
| 7:4              | PH_RAMP    | R/W              | Sets the time delay between ramp steps for the $\overline{Px\_PROCHOT}$ ramp up/ramp down PWM function. |       |       |       |          |       |       |       |               |

If the time delay between steps is set to 0 ms, the PWM duty cycle goes immediately to 100% instead of ramping up gradually.

| VRD_RAMP or PH_RAMP | Time Delay between Ramp Steps |
|---------------------|-------------------------------|
| 0h                  | 0 ms                          |
| 1h                  | 50 ms                         |
| 2h                  | 100 ms                        |
| 3h                  | 150 ms                        |
| 4h                  | 200 ms                        |
| 5h                  | 250 ms                        |
| 6h                  | 300 ms                        |
| 7h                  | 350 ms                        |
| 8h                  | 400 ms                        |
| 9h                  | 450 ms                        |
| Ah                  | 500 ms                        |
| Bh                  | 550 ms                        |
| Ch                  | 600 ms                        |
| Dh                  | 650 ms                        |

| VRD_RAMP<br>or PH_RAMP | Time Delay between<br>Ramp Steps |
|------------------------|----------------------------------|
| Eh                     | 700 ms                           |
| Fh                     | 750 ms                           |

### 3.17.8.5 Register C0h Fan Boost Hysteresis (Zones 1/2)

| Register Address | Read/Write | Register Name                    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C0h              | R/W        | Fan Boost Hysteresis (Zones 1/2) |       | H2    |       |       |       |       | H1    |       | 44h           |

| Bit | Name | R/W | Description                              |
|-----|------|-----|------------------------------------------|
| 3:0 | H1   | R/W | Sets the fan boost hysteresis for zone 1 |
| 7:4 | H2   | R/W | Sets the fan boost hysteresis for zone 2 |

If the temperature zone is above fan boost temperature and then drops below the fan boost temperature, the following occurs: the PWM output remains at 100% until the temperature goes a certain amount below the fan boost temperature. These hysteresis registers control this amount and can be set anywhere from 0°C to 15°C (unsigned).

### 3.17.8.6 Register C1h Fan Boost Hysteresis (Zones 3/4)

| Register Address | Read/Write | Register Name                    | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C1h              | R/W        | Fan Boost Hysteresis (Zones 3/4) |       | H4    |       |       |       |       | H3    |       | 44h           |

| Bit | Name | R/W | Description                              |
|-----|------|-----|------------------------------------------|
| 3:0 | H3   | R/W | Sets the fan boost hysteresis for zone 3 |
| 7:4 | H4   | R/W | Sets the fan boost hysteresis for zone 4 |

If the temperature zone is above fan boost temperature and then drops below the fan boost temperature, the following occurs: the PWM output remains at 100% until the temperature goes a certain amount below the fan boost temperature. These hysteresis registers control this amount and can be set anywhere from 0°C to 15°C (unsigned).

### 3.17.8.7 Register C2h Zones 1/2 Spike Smoothing Control

| Register Address | Read/Write | Register Name                     | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C2h              | R/W        | Zones 1/2 Spike Smoothing Control | ZN2E  |       | ZN2   |       | ZN1E  |       | ZN1   |       | 00h           |

| Bit | Name | R/W | Description                                                                                                                                                                                                                                                       |
|-----|------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | ZN1  | R/W | Configures the spike smoothing characteristics for zone 1                                                                                                                                                                                                         |
| 3   | ZN1E | R/W | When set, the filtered temperature for zone 1 is used for both limit checking and auto-fan control instead of the unfiltered temperature. Even when this bit is cleared, the filtered temperature can be read by software from the filtered temperature register. |
| 6:4 | ZN2  | R/W | Configures the spike smoothing characteristics for zone 2                                                                                                                                                                                                         |

| Bit | Name | R/W | Description                                                                                                                                                                                                                                                       |
|-----|------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | ZN2E | R/W | When set, the filtered temperature for zone 2 is used for both limit checking and auto-fan control instead of the unfiltered temperature. Even when this bit is cleared, the filtered temperature can be read by software from the filtered temperature register. |

If the REMOTE1 or REMOTE2 pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the LM93. If these spikes are not ignored, the PWM outputs may cause the fans to turn on prematurely and produce unpleasant noise. Also, false error events may occur. For this reason, any zone that is connected to a chipset or processor may need spike smoothing enabled. The spike smoothing provides additional filtering above and beyond any  $\Sigma\Delta$  A/D inherent averaging.

When spike smoothing is enabled, the temperature reading registers still reflect the current value of the temperature—not the filtered value. Only the filtered temperature registers reflect the filtered value.

| ZN1 or ZN2 | Spike Smoothed Over |
|------------|---------------------|
| 0h         | 11.8 seconds        |
| 1h         | 7.0 seconds         |
| 2h         | 4.4 seconds         |
| 3h         | 3.0 seconds         |
| 4h         | 1.6 seconds         |
| 5h         | 0.8 seconds         |
| 6h         | 0.6 seconds         |
| 7h         | 0.4 seconds         |

### 3.17.8.8 Register C3h Zones 1/2 MinPWM and Hysteresis

| Register Address | Read/Write | Register Name                   | Bit 7                                                                                                                                                                                                                                                                                                                                | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C3h              | R/W        | Zones 1/2 MinPWM and Hysteresis | MinPWM                                                                                                                                                                                                                                                                                                                               |       |       |       | FC_TH |       |       |       | N/D           |
| Bit              | Name       | R/W                             | Description                                                                                                                                                                                                                                                                                                                          |       |       |       |       |       |       |       |               |
| 3:0              | FC_TH      | R/W                             | This field sets the amount of hysteresis (in degrees C) that is used by the auto-fan control for zones 1 and 2. This should be set greater than 0 to avoid unwanted oscillation between two steps in the look-up table.                                                                                                              |       |       |       |       |       |       |       |               |
| 7:4              | MinPWM     | R/W                             | This field determines the duty cycle that the auto-fan control requests for zones 1 and 2 if the temperature for the given zone falls below the programmed base temperature for that zone. This field accepts 16 possible values that are mapped to duty cycles according the table in the <a href="#">Auto-Fan Control</a> section. |       |       |       |       |       |       |       |               |

### 3.17.8.9 Register C4h Zones 3/4 MinPWM and Hysteresis

| Register Address | Read/Write | Register Name                   | Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------------|--------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C4h              | R/W        | Zones 3/4 MinPWM and Hysteresis | MinPWM |       |       |       | FC_TH |       |       |       | N/D           |

| Bit | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                          |
|-----|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | FC_TH  | R/W | This field sets the amount of hysteresis (in degrees C) that is used by the auto-fan control for zones 3 and 4. This should be set greater than 0 to avoid unwanted oscillation between two steps in the look-up table.                                                                                                              |
| 7:4 | MinPWM | R/W | This field determines the duty cycle that the auto-fan control requests for zones 3 and 4 if the temperature for the given zone falls below the programmed base temperature for that zone. This field accepts 16 possible values that are mapped to duty cycles according the table in the <a href="#">Auto-Fan Control</a> section. |

### 3.17.8.10 Register C5h GPO

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C5h              | R/W        | GPO           | GPO7  | GPO6  | GPO5  | GPO4  | GPO3  | GPO2  | GPO1  | GPO0  | 00h           |

| Bit | Name | R/W | Description                                                                                                                            |
|-----|------|-----|----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | GPO0 | R/W | If set, GPIO_0 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_0 is being used as an input. |
| 1   | GPO1 | R/W | If set, GPIO_1 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_1 is being used as an input. |
| 2   | GPO2 | R/W | If set, GPIO_2 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_2 is being used as an input. |
| 3   | GPO3 | R/W | If set, GPIO_3 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_3 is being used as an input. |
| 4   | GPO4 | R/W | If set, GPIO_4 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_4 is being used as an input. |
| 5   | GPO5 | R/W | If set, GPIO_5 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_5 is being used as an input. |
| 6   | GPO6 | R/W | If set, GPIO_6 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_6 is being used as an input. |
| 7   | GPO7 | R/W | If set, GPIO_7 will be pulled low. If cleared, the output is not pulled low. This bit should be 0 if GPIO_7 is being used as an input. |

### 3.17.8.11 Register C6h PROCHOT Override

| Register Address | Read/Write | Register Name                           | Bit 7    | Bit 6    | Bit 5 | Bit 4 | Bit 3 | Bit 2  | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------------------------|----------|----------|-------|-------|-------|--------|-------|-------|---------------|
| C6h              | R/W        | $\overline{\text{PROCHOT}}$<br>Override | FORCE_P1 | FORCE_P2 | RES   |       |       | PHT_DC |       |       | 00h           |

| Bit | Name     | R/W | Description                                                                                                                        |
|-----|----------|-----|------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | PHT_DC   | R/W | $\overline{\text{PROCHOT}}$ duty cycle select.                                                                                     |
| 5:4 | RES      | R   | Reserved                                                                                                                           |
| 6   | FORCE_P1 | R/W | When this is set by software, $\overline{\text{P1\_PROCHOT}}$ will be asserted by the LM93 with the duty cycle selected by PHT_DC. |
| 7   | FORCE_P2 | R/W | When this is set by software, $\overline{\text{P2\_PROCHOT}}$ will be asserted by the LM93 with the duty cycle selected by PHT_DC. |

Note that if the  $\overline{\text{P1P2\_PROCHOT}}$  bit is set to short the  $\overline{\text{Px\_PROCHOT}}$  pins together, both  $\overline{\text{Px\_PROCHOT}}$  outputs will be driven together, even if only one of the FORCE\_Px bits is set.

The period of the PWM signal driven on  $\overline{\text{Px\_PROCHOT}}$  is 3.56 ms (80 internal 22.5 kHz clocks). The asserted time can be increased in 5 clock increments. 5 clocks is about 220  $\mu\text{s}$  and would represent 6.25% percent throttled.

Possible settings for PHT\_DC:

| PHT_DC | Asserted Period |
|--------|-----------------|
| 0h     | 5 clocks        |
| 1h     | 10 clocks       |
| 2h     | 15 clocks       |
| 3h     | 20 clocks       |
| 4h     | 25 clocks       |
| 5h     | 30 clocks       |
| 6h     | 35 clocks       |
| 7h     | 40 clocks       |
| 8h     | 45 clocks       |
| 9h     | 50 clocks       |
| Ah     | 55 clocks       |
| Bh     | 60 clocks       |
| Ch     | 65 clocks       |
| Dh     | 70 clocks       |
| Eh     | 75 clocks       |
| Fh     | 80 clocks       |

**3.17.8.12 Register C7h PROCHOT Time Interval**

| Register Address | Read/Write | Register Name         | Bit 7                                       | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-----------------------|---------------------------------------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C7h              | R/W        | PROCHOT Time Interval | P2_TI                                       |       |       |       | P1_TI |       |       |       | 11h           |
| Bit              | Name       | R/W                   | Description                                 |       |       |       |       |       |       |       |               |
| 3:0              | P1_TI      | R/W                   | Sets the monitoring interval for P1_PROCHOT |       |       |       |       |       |       |       |               |
| 7:4              | P2_TI      | R/W                   | Sets the monitoring interval for P2_PROCHOT |       |       |       |       |       |       |       |               |

Possible settings for P1\_TI and P2\_TI:

| P1_TI or P2_TI | Monitoring Time Interval (seconds) |
|----------------|------------------------------------|
| 0h             | 0.73                               |
| 1h             | 1.46                               |
| 2h             | 2.9                                |
| 3h             | 5.8                                |
| 4h             | 11.7                               |
| 5h             | 23.3                               |
| 6h             | 46.6                               |
| 7h             | 93.2                               |
| 8h             | 186                                |
| 9h             | 372                                |
| Ah–Fh          | Reserved                           |

Note that changing this value while  $\overline{\text{PROCHOT}}$  measurements are running may cause the monitoring circuit to produce an erroneous value. To avoid alerts and invalid B\_Px\_PROCHOT or B\_Px\_PROCHOT Error Status values, only change this value while the chip is programmed for S3 or S4/5.

### 3.17.8.13 Register C8h PWM1 Control 1

| Register Address | Read/Write | Register Name  | Bit 7                                                           | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-----------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C8h              | R/W        | PWM1 Control 1 | VRD2                                                            | VRD1  | PH2   | PH1   | ZN4   | ZN3   | ZN2   | ZN1   | 0Fh           |
| Bit              | Name       | R/W            | Description                                                     |       |       |       |       |       |       |       |               |
| 0                | ZN1        | R/W            | If set, PWM1 will be bound to temperature zone 1.               |       |       |       |       |       |       |       |               |
| 1                | ZN2        | R/W            | If set, PWM1 will be bound to temperature zone 2.               |       |       |       |       |       |       |       |               |
| 2                | ZNE        | R/W            | If set, PWM1 will be bound to temperature zone 3.               |       |       |       |       |       |       |       |               |
| 3                | ZN4        | R/W            | If set, PWM1 will be bound to temperature zone 4.               |       |       |       |       |       |       |       |               |
| 4                | PH1        | R/W            | If set, PWM1 will be bound to $\overline{\text{P1\_PROCHOT}}$ . |       |       |       |       |       |       |       |               |
| 5                | PH2        | R/W            | If set, PWM1 will be bound to $\overline{\text{P2\_PROCHOT}}$ . |       |       |       |       |       |       |       |               |
| 6                | VRD1       | R/W            | If set, PWM1 will be bound to $\overline{\text{VRD1\_HOT1}}$ .  |       |       |       |       |       |       |       |               |
| 7                | VRD2       | R/W            | If set, PWM1 will be bound to $\overline{\text{VRD1\_HOT2}}$ .  |       |       |       |       |       |       |       |               |

This register can bind PWM1 to several different control sources. The temperature zones control the PWM duty cycle using the table lookup function. The  $\overline{\text{Px\_PROCHOT}}$  and  $\overline{\text{VRDx\_HOT}}$  inputs control the PWM using the ramp up/ramp down functions. If multiple control sources are bound to PWM1, the largest duty cycle being requested will be used.

### 3.17.8.14 Register C9h PWM1 Control 2

| Register Address | Read/Write | Register Name  | Bit 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|---------------|
| C9h              | R/W        | PWM1 Control 2 | OVR_DC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |       |       |       | PL    | EPPL  | INV   | OVR   | 00h           |
| Bit              | Name       | R/W            | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |       |       |       |       |       |       |       |               |
| 0                | OVR        | R/W            | When set, enables manual duty cycle override for PWM1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |       |       |       |       |       |       |       |               |
| 1                | INV        | R/W            | Invert PWM1 output. When 0, 100% duty cycle corresponds to the PWM output continuously HIGH. When 1, 100% duty cycle corresponds to the PWM output continuously LOW.                                                                                                                                                                                                                                                                                                                                                                                                                 |       |       |       |       |       |       |       |               |
| 2                | EPPL       | R/W            | Enable PROCHOT PWM1 lock. When set, this bit causes bound PROCHOT events on PWM1 to trigger PPL (bit [3]). When cleared, PPL never gets set.                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |       |       |       |       |       |       |               |
| 3                | PPL        | R/W            | PROCHOT PWM1 lock. When set, this bit indicates that PWM1 is currently being held at 100% because a bound PROCHOT event occurred while EPPL (bit [2]) was set. This bit is cleared by writing a zero. Clearing this bit allows the fans to return to normal operation. This bit is not locked by the LOCK bit in the LM93 Configuration register.                                                                                                                                                                                                                                    |       |       |       |       |       |       |       |               |
| 7:4              | OVR_DC     | R/W            | This field sets the duty cycle that will be used by PWM1 whenever manual override mode is active. This field accepts 16 possible values that are mapped to duty cycles according to the table in the <a href="#">FAN CONTROL</a> section. Whenever this register is read, it returns the duty cycle that is currently being used by PWM1 regardless of whether override mode is active or not. The value read may not match the last value written if another control source is requesting a greater duty cycle. This field always returns 0h when the PWM1 spin up cycle is active. |       |       |       |       |       |       |       |               |

### 3.17.8.15 Register CAh PWM1 Control 3

| Register Address | Read/Write | Register Name  | Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|--------|-------|-------|-------|-------|-------|-------|-------|---------------|
| CAh              | R/W        | PWM1 Control 3 | SU_DUR |       |       | RES   | SU_DC |       |       |       | 00h           |

| Bit | Name   | R/W | Description                                                                                                                                                                                                                                                                                      |
|-----|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | SU_DC  | R/W | This field sets the duty cycle that will be used whenever PWM1 experiences a Spin-Up cycle. This field accepts 16 possible values that are mapped to duty cycles according the table in the <a href="#">Auto-Fan Control</a> section. Setting this field to 0h will effectively disable Spin-Up. |
| 4   | RES    | R   | Reserved                                                                                                                                                                                                                                                                                         |
| 7:5 | SU_DUR | R/W | Sets the Spin-Up duration for PWM1.                                                                                                                                                                                                                                                              |

Bits 7:5 configure the spin-up duration. When the duty cycle of PWM1 changes from zero to a non-zero value, the spin-up sequence is activated for the specified amount of time. The available settings are defined according to this table:

| SU_DUR | Spin-Up Time     |
|--------|------------------|
| 0h     | Spin-up disabled |
| 1h     | 100 ms           |
| 2h     | 250 ms           |
| 3h     | 400 ms           |
| 4h     | 700 ms           |
| 5h     | 1000 ms          |
| 6h     | 2000 ms          |
| 7h     | 4000 ms          |

### 3.17.8.16 Register CBh Special Function PWM1 Control 4

| Register Address | Read/Write | Register Name                   | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| CBh              | R/W        | Special Function PWM1 Control 4 | RES   | RES   | RES   | RES   | RES   | FREQ1 |       |       | 00h           |

| Bit | Name  | R/W | Description                                                                                                        |
|-----|-------|-----|--------------------------------------------------------------------------------------------------------------------|
| 2:0 | FREQ1 | R/W | PWM1 frequency control. Setting this value controls the frequency of the PWM1 output according to the table below. |
| 7:3 | RES   | R   | Reserved                                                                                                           |

| FREQ1 or FREQ2 | Frequency of PWM1 or PWM2 (Hz) |
|----------------|--------------------------------|
| 0h             | 22500                          |
| 1h             | 96                             |
| 2h             | 84                             |
| 3h             | 72                             |
| 4h             | 60                             |
| 5h             | 48                             |
| 6h             | 36                             |
| 7h             | 12                             |

### 3.17.8.17 Register CCh PWM2 Control 1

| Register Address | Read/Write | Register Name  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| CCh              | R/W        | PWM2 Control 1 | VRD2  | VRD1  | PH2   | PH1   | ZN4   | ZN3   | ZN2   | ZN1   | 0Fh           |

| Bit | Name | R/W | Description                                              |
|-----|------|-----|----------------------------------------------------------|
| 0   | ZN1  | R/W | If set, PWM2 will be bound to temperature zone 1.        |
| 1   | ZN2  | R/W | If set, PWM2 will be bound to temperature zone 2.        |
| 2   | ZN3  | R/W | If set, PWM2 will be bound to temperature zone 3.        |
| 3   | ZN4  | R/W | If set, PWM2 will be bound to temperature zone 4.        |
| 4   | PH1  | R/W | If set, PWM2 will be bound to $\overline{P1\_PROCHOT}$ . |
| 5   | PH2  | R/W | If set, PWM2 will be bound to $\overline{P2\_PROCHOT}$ . |
| 6   | VRD1 | R/W | If set, PWM2 will be bound to $\overline{VRD1\_HOT}$ .   |
| 7   | VRD2 | R/W | If set, PWM2 will be bound to $\overline{VRD2\_HOT}$ .   |

This register can bind PWM2 to several different control sources. The temperature zones control the PWM duty cycle using the table lookup function. The  $\overline{Px\_PROCHOT}$  and  $\overline{VRDx\_HOT}$  inputs control the PWM using the ramp up/ramp down functions. If multiple control sources are bound to PWM2, the largest duty cycle being requested will be used.

### 3.17.8.18 Register CDh PWM2 Control 2

| Register Address | Read/Write | Register Name  | Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|--------|-------|-------|-------|-------|-------|-------|-------|---------------|
| CDh              | R/W        | PWM2 Control 2 | OVR_DC |       |       |       | PL    | EPPL  | INV   | OVR   | 00h           |

| Bit | Name   | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|--------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | OVR    | R/W | When set, enables manual duty cycle override for PWM2.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1   | INV    | R/W | Invert PWM1 output. When 0, 100% duty cycle corresponds to the PWM output continuously HIGH. When 1, 100% duty cycle corresponds to the PWM output continuously LOW.                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2   | EPPL   | R/W | Enable PROCHOT PWM2 lock. When set, this bit causes bound PROCHOT events on PWM2 to trigger PPL (bit [3]). When cleared, PPL never gets set.                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3   | PPL    | R/W | PROCHOT PWM2 lock. When set, this bit indicates that PWM2 is currently being held at 100% because a bound PROCHOT event occurred while EPPL (bit [2]) was set. This bit is cleared by writing a zero. Clearing this bit allows the fans to return to normal operation. This bit is not locked by the LOCK bit in the LM93 Configuration register.                                                                                                                                                                                                                                 |
| 7:4 | OVR_DC | R/W | This field sets the duty cycle that will be used by PWM2 whenever manual override mode is active. This field accepts 16 possible values that are mapped to duty cycles according the table in the <a href="#">FAN CONTROL</a> section. Whenever this register is read, it returns the duty cycle that is currently being used by PWM2 regardless of whether override mode is active or not. The value read may not match the last value written if another control source is requesting a greater duty cycle. This field always returns 0h when the PWM2 spin up cycle is active. |

### 3.17.8.19 Register CEh PWM2 Control 3

| Register Address | Read/Write | Register Name  | Bit 7  | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|----------------|--------|-------|-------|-------|-------|-------|-------|-------|---------------|
| CEh              | R/W        | PWM2 Control 3 | SU_DUR |       |       | RES   | SU_DC |       |       | 00h   |               |

| Bit | Name   | R/W | Description                                                                                                                                                                                                                                                                          |
|-----|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | SU_DC  | R/W | This field sets the duty cycle that used whenever PWM2 experiences a Spin-Up cycle. This field accepts 16 possible values that are mapped to duty cycles according the table in the <a href="#">Auto-Fan Control</a> section. Setting this field to 0h effectively disables Spin-Up. |
| 4   | RES    | R   | Reserved                                                                                                                                                                                                                                                                             |
| 7:5 | SU_DUR | R/W | Sets the Spin-Up duration for PWM2.                                                                                                                                                                                                                                                  |

Bits 7:5 configure the spin-up duration. When the duty cycle of PWM2 changes from zero to a non-zero value, the spin-up sequence is activated for the specified amount of time. The available settings are defined according to this table:



| SU_DUR | Spin-Up Time     |
|--------|------------------|
| 0h     | Spin-up disabled |
| 1h     | 100 ms           |
| 2h     | 250 ms           |
| 3h     | 400 ms           |
| 4h     | 700 ms           |
| 5h     | 1000 ms          |
| 6h     | 2000 ms          |
| 7h     | 4000 ms          |

### 3.17.8.20 Register CFh Special Function PWM2 Control 4

| Register Address | Read/Write | Register Name                   | Bit 7 | Bit 6 | Bit 5                                                                                                                          | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------------------|-------|-------|--------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------|-------|---------------|
| CFh              | R/W        | Special Function PWM2 Control 4 | RES   | RES   | RES                                                                                                                            | RES   | RES   | FREQ2 |       |       | 00h           |
| Bit              | Name       |                                 | R/W   |       | Description                                                                                                                    |       |       |       |       |       |               |
| 2:0              | FREQ2      |                                 | R/W   |       | PWM2 frequency control. Controls the frequency of the PWM2 output in the same fashion as FREQ1 in the PWM1 Control 4 register. |       |       |       |       |       |               |
| 7:3              | RES        |                                 | R     |       | Reserved                                                                                                                       |       |       |       |       |       |               |

### 3.17.8.21 Register D0h–D3h Zone 1 to 4 Base Temperatures

| Register Address | Read/Write | Register Name           | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| D0h              | R/W        | Zone 1 Base Temperature | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| D1h              | R/W        | Zone 2 Base Temperature | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| D2h              | R/W        | Zone 3 Base Temperature | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |
| D3h              | R/W        | Zone 4 Base Temperature | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | N/D           |

The value in this register is used as the base in the temperature calculation for the auto fan control look-up table. These registers use the standard temperature format (8-bit signed data). The look-up table contains the temperature offsets. The offsets are added to the base temperature to determine the true temperature to be used for each table entry for auto fan control.

### 3.17.8.22 Register D4h–DFh Lookup Table Steps—Zone 1/2 and Zone 3/4 Offset Temperature

| Register Address | Read/Write | Register Name      | Bit 7      | Bit 6 | Bit 5 | Bit 4 | Bit 3      | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|------------|-------|-------|-------|------------|-------|-------|-------|---------------|
| D4h              | R/W        | Step 2 Temp Offset | Z3/4_STEP2 |       |       |       | Z1/2_STEP2 |       |       |       | N/D           |
| D5h              | R/W        | Step 3 Temp Offset | Z3/4_STEP3 |       |       |       | Z1/2_STEP3 |       |       |       | N/D           |

| Register Address | Read/Write | Register Name       | Bit 7       | Bit 6 | Bit 5 | Bit 4 | Bit 3       | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|-------------|-------|-------|-------|-------------|-------|-------|-------|---------------|
| D6h              | R/W        | Step 4 Temp Offset  | Z3/4_STEP4  |       |       |       | Z1/2_STEP4  |       |       |       | N/D           |
| D7h              | R/W        | Step 5 Temp Offset  | Z3/4_STEP5  |       |       |       | Z1/2_STEP5  |       |       |       | N/D           |
| D8h              | R/W        | Step 6 Temp Offset  | Z3/4_STEP6  |       |       |       | Z1/2_STEP6  |       |       |       | N/D           |
| D9h              | R/W        | Step 7 Temp Offset  | Z3/4_STEP7  |       |       |       | Z1/2_STEP7  |       |       |       | N/D           |
| DAh              | R/W        | Step 8 Temp Offset  | Z3/4_STEP8  |       |       |       | Z1/2_STEP8  |       |       |       | N/D           |
| DBh              | R/W        | Step 9 Temp Offset  | Z3/4_STEP9  |       |       |       | Z1/2_STEP9  |       |       |       | N/D           |
| DCh              | R/W        | Step 10 Temp Offset | Z3/4_STEP10 |       |       |       | Z1/2_STEP10 |       |       |       | N/D           |
| DDh              | R/W        | Step 11 Temp Offset | Z3/4_STEP11 |       |       |       | Z1/2_STEP11 |       |       |       | N/D           |
| DEh              | R/W        | Step 12 Temp Offset | Z3/4_STEP12 |       |       |       | Z1/2_STEP12 |       |       |       | N/D           |
| DFh              | R/W        | Step 13 Temp Offset | Z3/4_STEP13 |       |       |       | Z1/2_STEP13 |       |       |       | N/D           |

There are two look up tables of 13 steps (12 offsets), one for Zones 1 and 2 the other for Zones 3 and 4. Each 8-bit offset register contains the offset temperature for Zones 1 and 2 as well as the offset temperature for Zones 3 and 4. The format for the offsets is a 4-bit unsigned value, and one LSB = 1°C.

See the [FAN CONTROL](#) for information on how the base temperature/lookup table should be used for controlling the PWM output(s).

### 3.17.8.23 Register E0h Special Function TACH to PWM Binding

| Register Address | Read/Write | Register Name                        | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| E0h              | R/W        | Special Function TACH to PWM Binding | T4P2  | T4P1  | T3P2  | T3P1  | T2P2  | T2P1  | T1P2  | T1P1  | 00h           |

| Bit | Name | R/W | Description                     |
|-----|------|-----|---------------------------------|
| 0   | T1P1 | R/W | If set, TACH1 is bound to PWM1. |
| 1   | T1P2 | R/W | If set, TACH1 is bound to PWM2. |
| 2   | T2P1 | R/W | If set, TACH2 is bound to PWM1. |
| 3   | T2P2 | R/W | If set, TACH2 is bound to PWM2. |
| 4   | T3P1 | R/W | If set, TACH3 is bound to PWM1. |
| 5   | T3P2 | R/W | If set, TACH3 is bound to PWM2. |
| 6   | T4P1 | R/W | If set, TACH4 is bound to PWM1. |
| 7   | T4P2 | R/W | If set, TACH4 is bound to PWM2. |

If a TACH channel is bound to a PWM channel, TACH errors on that channel are automatically masked when the bound PWM is at 0% duty cycle or performing spin-up. Behavior is undefined if a TACH channel is bound to both PWM outputs. This register must be setup when Smart Tach Mode is enabled in register BDh, Special Function Control 2.

### 3.17.8.24 Register E2h LM93 Status Control

| Register Address | Read/Write | Register Name       | Bit 7   | Bit 6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Bit 5     | Bit 4 | Bit 3   | Bit 2   | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|---------|---------|-------|-------|---------------|
| E2h              | R/W        | LM93 Status/Control | BMC_ERR | HOST_ERR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | TACH_EDGE |       | GPI5_AM | GPI4_AM | ASF   | OVRID | 00h           |
| Lock             | Bit        | Name                | R/W     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |           |       |         |         |       |       |               |
|                  | 0          | OVRID               | R/W     | If this bit is set, all PWM outputs go to 100% duty cycle.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |           |       |         |         |       |       |               |
| X                | 1          | ASF                 | R/W     | If this bit is set, BMC error registers support ASF, i.e. reset on read. When not in ASF mode, a write "1" is required to clear the bits in the BMC error status registers.                                                                                                                                                                                                                                                                                                                                                                   |           |       |         |         |       |       |               |
|                  | 2          | GPI4_AM             | R/W     | GPI4 Auto Mask Enable<br>If this bit is set, an error event on GPI4 causes all other error events to be masked.<br>The BMC Error Status registers do not reflect any new error events until the GPI4_ERR bit is cleared in the B_GPI Error Status register. The HOST Error Status registers do not reflect any new error events until the GPI4_ERR bit is cleared in the H_GPI Error Status register.<br>If a CPU_THERMTRIP signal is connected to GPIO4, this ensures that unwanted error events do not fire once CPU_THERMTRIP is asserted. |           |       |         |         |       |       |               |
|                  | 3          | GP15_AM             | R/W     | GPI5 Auto Mask Enable<br>This bit works exactly the same as GPI4_AM, but applies to GPI5.                                                                                                                                                                                                                                                                                                                                                                                                                                                     |           |       |         |         |       |       |               |
|                  | 5:4        | TACH_EDGE           | R/W     | This field determines what type of edges are used for measuring fan tach pulses. This effects all four tachometer inputs.                                                                                                                                                                                                                                                                                                                                                                                                                     |           |       |         |         |       |       |               |
|                  | 6          | HOST_ERR            | R       | This bit gets set if any error bit is set in any of the Host Error Status registers (H_).                                                                                                                                                                                                                                                                                                                                                                                                                                                     |           |       |         |         |       |       |               |
|                  | 7          | BMC_ERR             | R       | This bit gets set if any error bit is set in any of the BMC Error Status registers (B_). When this bit is set, ALERT are asserted if enabled.                                                                                                                                                                                                                                                                                                                                                                                                 |           |       |         |         |       |       |               |

| TACH_EDGE | Edge Type Used for Tachometer Measurements  |
|-----------|---------------------------------------------|
| 0h        | Either rising or falling edges may be used. |
| 1h        | Rising edges only                           |
| 2h        | Falling edges only                          |
| 3h        | Reserved                                    |

### 3.17.8.25 Register E3h LM93 Configuration

| Register Address | Read/Write | Register Name      | Bit 7 | Bit 6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Bit 5 | Bit 4        | Bit 3    | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|--------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------|----------|-------|-------|-------|---------------|
| E3h              | R/W        | LM93 Configuration | READY | RES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |       | P1P2_PROCHOT | ALERT_EN | GMSK  | LOCK  | START | 00h           |
| Lock             | Bit        | Name               | R/W   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |       |              |          |       |       |       |               |
| x                | 0          | START              | R/W   | When this bit is 0, the LM93 operates in basic mode. All error events are masked. The auto fan control algorithm is disabled. Both PWMs are set to 0%, but the Fan Boost function operates based on default limits. All monitoring functions are active and the value registers are updated. Once this bit is set, error events are no longer globally masked, and the auto-fan control algorithm is enabled. Fan boost uses the programmed values instead of the defaults. It is expected that all limit and setup registers are set by BIOS or application software prior to setting this bit. |       |              |          |       |       |       |               |

| Lock | Bit | Name         | R/W | Description                                                                                                                                                                                                                                                                                                                                             |
|------|-----|--------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| X    | 1   | LOCK         | R/W | Setting this bit locks all registers and register bits that are indicated as lockable. Lockable registers have an "x" in the <b>Lock</b> column of their description. This register is locked once it is set. This bit can only be cleared by an external device asserting RESET.                                                                       |
|      | 2   | GMSK         | R/W | Global Mask<br>When this bit is set by software, <b>all</b> error events are masked. Setting this bit does not effect any other mask registers or value registers.                                                                                                                                                                                      |
|      | 3   | ALERT_EN     | R/W | When this bit is set, the $\overline{\text{ALERT}}$ output is enabled. If this bit is cleared, the $\overline{\text{ALERT}}$ output is disabled.                                                                                                                                                                                                        |
|      | 4   | P1P2_PROCHOT | R/W | In some configurations it may be required to have both processors throttling at the same rate. When this bit is set, the LM93 connects P1_PROCHOT to P2_PROCHOT. If P1_PROCHOT and P2_PROCHOT are already shorted by some other means, this bit should NOT be set. Doing so would cause both PROCHOT signals to be stuck low until this bit is cleared. |
|      | 6:5 | RES          | R/W | Reserved                                                                                                                                                                                                                                                                                                                                                |
|      | 7   | READY        | R   | The LM93 sets this bit automatically after valid data has been collected for all temperatures and voltages. Software should not use any temperature or voltage values until this bit has been set.                                                                                                                                                      |

### 3.17.9 SLEEP STATE CONTROL AND MASK REGISTERS

#### 3.17.9.1 Register E4h Sleep State Control

| Register Address | Read/Write | Register Name       | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|---------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| E4h              | R          | Sleep State Control | RES   |       |       |       |       |       | SB    |       | 07h           |

| Bit | Name | R/W | Description                                                                                                                                                      |
|-----|------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | SB   | R/W | Sleep State Control. Setting this field tells the LM93 which sleep state the system is in. Several error events are masked depending on the state of this field. |
| 7:2 | RES  | R   | Reserved                                                                                                                                                         |

| SB | Description                                                                                                                                                                  |
|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00 | Sleep state = S0<br>Do not mask errors.                                                                                                                                      |
| 01 | Sleep state = S1<br>Mask errors according to S1 mask registers and standard S1 masking.                                                                                      |
| 10 | Sleep state = S3<br>Mask errors according to S3 mask registers and standard S3 masking.                                                                                      |
| 11 | Sleep state = S4/5<br>Mask errors according to S4/5 mask registers and standard S4/5 masking.<br>This <u>mode</u> is activated automatically if the RESET input is asserted. |

#### 3.17.9.2 Register E5h S1 GPI Mask

| Register Address | Read/Write | Register Name | Bit 7       | Bit 6       | Bit 5       | Bit 4       | Bit 3       | Bit 2       | Bit 1       | Bit 0       | Default Value |
|------------------|------------|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------|
| E5h              | R/W        | S1 GPI Mask   | GPI7_S1_MSK | GPI6_S1_MSK | GPI5_S1_MSK | GPI4_S1_MSK | GPI3_S1_MSK | GPI2_S1_MSK | GPI1_S1_MSK | GPI0_S1_MSK | FFh           |

| Bit | Name        | R/W | Description                                       |
|-----|-------------|-----|---------------------------------------------------|
| 0   | GPI0_S1_MSK | R/W | If set, GPI0 errors are masked in S1 sleep state. |
| 1   | GPI1_S1_MSK | R/W | If set, GPI1 errors are masked in S1 sleep state. |
| 2   | GPI2_S1_MSK | R/W | If set, GPI2 errors are masked in S1 sleep state. |
| 3   | GPI3_S1_MSK | R/W | If set, GPI3 errors are masked in S1 sleep state. |
| 4   | GPI4_S1_MSK | R/W | If set, GPI4 errors are masked in S1 sleep state. |
| 5   | GPI5_S1_MSK | R/W | If set, GPI5 errors are masked in S1 sleep state. |
| 6   | GPI6_S1_MSK | R/W | If set, GPI6 errors are masked in S1 sleep state. |
| 7   | GPI7_S1_MSK | R/W | If set, GPI7 errors are masked in S1 sleep state. |

### 3.17.9.3 Register E6h S1 Tach Mask

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3        | Bit 2        | Bit 1        | Bit 0        | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|--------------|--------------|--------------|--------------|---------------|
| E6h              | R/W        | S1 Tach Mask  | RES   |       |       |       | TACH4_S1_MSK | TACH3_S1_MSK | TACH2_S1_MSK | TACH1_S1_MSK | 0Fh           |

| Bit | Name         | R/W | Description                                        |
|-----|--------------|-----|----------------------------------------------------|
| 0   | TACH1_S1_MSK | R/W | If set, Tach1 errors are masked in S1 sleep state. |
| 1   | TACH2_S1_MSK | R/W | If set, Tach2 errors are masked in S1 sleep state. |
| 2   | TACH3_S1_MSK | R/W | If set, Tach3 errors are masked in S1 sleep state. |
| 3   | TACH4_S1_MSK | R/W | If set, Tach4 errors are masked in S1 sleep state. |
| 7:4 | RES          | R   | Reserved                                           |

### 3.17.9.4 Register E7h S3 GPI Mask

| Register Address | Read/Write | Register Name | Bit 7       | Bit 6       | Bit 5       | Bit 4       | Bit 3       | Bit 2       | Bit 1       | Bit 0       | Default Value |
|------------------|------------|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------|
| E7h              | R/W        | S3 GPI Mask   | GPI7_S3_MSK | GPI6_S3_MSK | GPI5_S3_MSK | GPI4_S3_MSK | GPI3_S3_MSK | GPI2_S3_MSK | GPI1_S3_MSK | GPI0_S3_MSK | FFh           |

| Bit | Name        | R/W | Description                                       |
|-----|-------------|-----|---------------------------------------------------|
| 0   | GPI0_S3_MSK | R/W | If set, GPI0 errors are masked in S3 sleep state. |
| 1   | GPI1_S3_MSK | R/W | If set, GPI1 errors are masked in S3 sleep state. |
| 2   | GPI2_S3_MSK | R/W | If set, GPI2 errors are masked in S3 sleep state. |
| 3   | GPI3_S3_MSK | R/W | If set, GPI3 errors are masked in S3 sleep state. |
| 4   | GPI4_S3_MSK | R/W | If set, GPI4 errors are masked in S3 sleep state. |
| 5   | GPI5_S3_MSK | R/W | If set, GPI5 errors are masked in S3 sleep state. |
| 6   | GPI6_S3_MSK | R/W | If set, GPI6 errors are masked in S3 sleep state. |
| 7   | GPI7_S3_MSK | R/W | If set, GPI7 errors are masked in S3 sleep state. |

### 3.17.9.5 Register E8h S3 Tach Mask

| Register Address | Read/Write | Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3        | Bit 2        | Bit 1        | Bit 0        | Default Value |
|------------------|------------|---------------|-------|-------|-------|-------|--------------|--------------|--------------|--------------|---------------|
| E8h              | R/W        | S3 Tach Mask  | RES   |       |       |       | TACH4_S3_MSK | TACH3_S3_MSK | TACH2_S3_MSK | TACH1_S3_MSK | 0Fh           |

| Bit | Name         | R/W | Description                                        |
|-----|--------------|-----|----------------------------------------------------|
| 0   | TACH1_S3_MSK | R/W | If set, Tach1 errors are masked in S3 sleep state. |
| 1   | TACH2_S3_MSK | R/W | If set, Tach2 errors are masked in S3 sleep state. |
| 2   | TACH3_S3_MSK | R/W | If set, Tach3 errors are masked in S3 sleep state. |
| 3   | TACH4_S3_MSK | R/W | If set, Tach4 errors are masked in S3 sleep state. |
| 7:4 | RES          | R   | Reserved                                           |

**3.17.9.6 Register E9h S3 Temperature/Voltage Mask**

| Register Address | Read/Write   | Register Name   | Bit 7                                                                                             | Bit 6 | Bit 5 | Bit 4 | Bit 3       | Bit 2        | Bit 1        | Bit 0        | Default Value |
|------------------|--------------|-----------------|---------------------------------------------------------------------------------------------------|-------|-------|-------|-------------|--------------|--------------|--------------|---------------|
| E9h              | R/W          | S3 Voltage Mask | RES                                                                                               |       |       |       | TEMP_S3_MSK | AIN14_S3_MSK | AIN13_S3_MSK | AIN12_S3_MSK | 07h           |
| Bit              | Name         | R/W             | Description                                                                                       |       |       |       |             |              |              |              |               |
| 0                | AIN12_S3_MSK | R/W             | If set, AIN12 errors as masked in S3 sleep state.                                                 |       |       |       |             |              |              |              |               |
| 1                | AIN13_S3_MSK | R/W             | If set, AIN13 errors as masked in S3 sleep state.                                                 |       |       |       |             |              |              |              |               |
| 2                | AIN14_S3_MSK | R/W             | If set, AIN14 errors as masked in S3 sleep state.                                                 |       |       |       |             |              |              |              |               |
| 3                | TEMP_S3_MSK  | R/W             | If set, temperature errors and diode fault errors for zones 1 and 2 are masked in S3 sleep state. |       |       |       |             |              |              |              |               |
| 7:3              | RES          | R               | Reserved                                                                                          |       |       |       |             |              |              |              |               |

**3.17.9.7 Register EAh S4/5 GPI Mask**

| Register Address | Read/Write    | Register Name | Bit 7                                               | Bit 6         | Bit 5         | Bit 4         | Bit 3         | Bit 2         | Bit 1         | Bit 0         | Default Value |
|------------------|---------------|---------------|-----------------------------------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| EAh              | R/W           | S4/5 GPI Mask | GPI7_S4/5_MSK                                       | GPI6_S4/5_MSK | GPI5_S4/5_MSK | GPI4_S4/5_MSK | GPI3_S4/5_MSK | GPI2_S4/5_MSK | GPI1_S4/5_MSK | GPI0_S4/5_MSK | FFh           |
| Bit              | Name          | R/W           | Description                                         |               |               |               |               |               |               |               |               |
| 0                | GPI0_S4/5_MSK | R/W           | If set, GPI0 errors are masked in S4/5 sleep state. |               |               |               |               |               |               |               |               |
| 1                | GPI1_S4/5_MSK | R/W           | If set, GPI1 errors are masked in S4/5 sleep state. |               |               |               |               |               |               |               |               |
| 2                | GPI2_S4/5_MSK | R/W           | If set, GPI2 errors are masked in S4/5 sleep state. |               |               |               |               |               |               |               |               |
| 3                | GPI3_S4/5_MSK | R/W           | If set, GPI3 errors are masked in S4/5 sleep state. |               |               |               |               |               |               |               |               |
| 4                | GPI4_S4/5_MSK | R/W           | If set, GPI4 errors are masked in S4/5 sleep state. |               |               |               |               |               |               |               |               |
| 5                | GPI5_S4/5_MSK | R/W           | If set, GPI5 errors are masked in S4/5 sleep state. |               |               |               |               |               |               |               |               |
| 6                | GPI6_S4/5_MSK | R/W           | If set, GPI6 errors are masked in S4/5 sleep state. |               |               |               |               |               |               |               |               |
| 7                | GPI7_S4/5_MSK | R/W           | If set, GPI7 errors are masked in S4/5 sleep state. |               |               |               |               |               |               |               |               |

**3.17.9.8 Register EBh S4/5 Temperature/Voltage Mask**

| Register Address | Read/Write     | Register Name     | Bit 7                                                                                               | Bit 6 | Bit 5 | Bit 4 | Bit 3         | Bit 2          | Bit 1          | Bit 0          | Default Value |
|------------------|----------------|-------------------|-----------------------------------------------------------------------------------------------------|-------|-------|-------|---------------|----------------|----------------|----------------|---------------|
| EBh              | R/W            | S4/5 Voltage Mask | RES                                                                                                 |       |       |       | TEMP_S4/5_MSK | AIN14_S4/5_MSK | AIN13_S4/5_MSK | AIN12_S4/5_MSK | 07h           |
| Bit              | Name           | R/W               | Description                                                                                         |       |       |       |               |                |                |                |               |
| 0                | AIN12_S4/5_MSK | R/W               | If set, AIN12 errors as masked in S4/5 sleep state.                                                 |       |       |       |               |                |                |                |               |
| 1                | AIN13_S4/5_MSK | R/W               | If set, AIN13 errors as masked in S4/5 sleep state.                                                 |       |       |       |               |                |                |                |               |
| 2                | AIN14_S4/5_MSK | R/W               | If set, AIN14 errors as masked in S4/5 sleep state.                                                 |       |       |       |               |                |                |                |               |
| 3                | TEMP_S4/5_MSK  | R/W               | If set, temperature errors and diode fault errors for zones 1 and 2 are masked in S4/5 sleep state. |       |       |       |               |                |                |                |               |
| 7:3              | RES            | R                 | Reserved                                                                                            |       |       |       |               |                |                |                |               |

**3.17.10 OTHER MASK REGISTERS****3.17.10.1 Register ECh GPI Error Mask**

| Register Address | Read/Write | Register Name  | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    | Default Value |
|------------------|------------|----------------|----------|----------|----------|----------|----------|----------|----------|----------|---------------|
| ECh              | R/W        | GPI Error Mask | GPI7_MSK | GPI6_MSK | GPI5_MSK | GPI4_MSK | GPI3_MSK | GPI2_MSK | GPI1_MSK | GPI0_MSK | FFh           |

| Bit | Name     | R/W | Description                                         |
|-----|----------|-----|-----------------------------------------------------|
| 0   | GPI0_MSK | R/W | When this bit is set, GPI0 error events are masked. |
| 1   | GPI1_MSK | R/W | When this bit is set, GPI1 error events are masked. |
| 2   | GPI2_MSK | R/W | When this bit is set, GPI2 error events are masked. |
| 3   | GPI3_MSK | R/W | When this bit is set, GPI3 error events are masked. |
| 4   | GPI4_MSK | R/W | When this bit is set, GPI4 error events are masked. |
| 5   | GPI5_MSK | R/W | When this bit is set, GPI5 error events are masked. |
| 6   | GPI6_MSK | R/W | When this bit is set, GPI6 error events are masked. |
| 7   | GPI7_MSK | R/W | When this bit is set, GPI7 error events are masked. |

These bits mask the corresponding bits in the B\_ and H\_GPI Error Status Registers. They do not effect the GPI State register.

### 3.17.10.2 Register EDh Miscellaneous Error Mask

| Register Address | Read/Write | Register Name            | Bit 7 | Bit 6 | Bit 5      | Bit 4      | Bit 3     | Bit 2     | Bit 1    | Bit 0    | Default Value |
|------------------|------------|--------------------------|-------|-------|------------|------------|-----------|-----------|----------|----------|---------------|
| EDh              | R/W        | Miscellaneous Error Mask | RES   |       | DVccp2_MSK | DVccp1_MSK | SCSI2_MSK | SCSI1_MSK | VRD2_MSK | VRD1_MSK | 3Fh           |

| Bit | Name       | R/W | Description                                                                         |
|-----|------------|-----|-------------------------------------------------------------------------------------|
| 0   | VRD1_MSK   | R/W | When this bit is set, $\overline{\text{VRD1\_HOT}}$ error events are masked.        |
| 1   | VRD2_MSK   | R/W | When this bit is set, $\overline{\text{VRD2\_HOT}}$ error events are masked.        |
| 2   | SCSI1_MSK  | R/W | When this bit is set, $\overline{\text{SCSI\_TERM1}}$ error events are masked.      |
| 3   | SCSI2_MSK  | R/W | When this bit is set, $\overline{\text{SCSI\_TERM2}}$ error events are masked.      |
| 4   | DVccp1_MSK | R/W | When this bit is set, dynamic Vccp limit error events for AD_IN7 (CPU1) are masked. |
| 5   | DVccp2_MSK | R/W | When this bit is set, dynamic Vccp limit error events for AD_IN8 (CPU2) are masked. |
| 7:6 | RES        | R   | Reserved                                                                            |

### 3.17.10.3 Register EEh Special Function Zone 1 Adjustment Offset

| Register Address | Read/Write | Register Name                             | Bit 7 | Bit 6 | Bit 5     | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------------------------|-------|-------|-----------|-------|-------|-------|-------|-------|---------------|
| EEh              | R/W        | Special Function Zone 1 Adjustment Offset | RES   | RES   | Z1_ADJUST |       |       |       |       |       | 00h           |

| Bit | Name      | R/W | Description                                                                                                                                                                                                                                                                                                      |
|-----|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:0 | Z1_ADJUST | R/W | 6-bit signed 2's complement offset adjustment. This value is added to all zone 1 temperature measurements as they are made. All LM93 registers and functions behave as if the resulting temperature was the true measured temperature. This register allows offset adjustments from +31°C to -32°C in 1°C steps. |
| 7:6 | RES       | R   | Reserved                                                                                                                                                                                                                                                                                                         |

### 3.17.10.4 Register EFh Special Function Zone 2 Adjustment Offset

| Register Address | Read/Write | Register Name                             | Bit 7 | Bit 6                                                                                                                                                                                                                                                                                                            | Bit 5     | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
|------------------|------------|-------------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------|-------|-------|-------|-------|---------------|
| EFh              | R/W        | Special Function Zone 2 Adjustment Offset | RES   | RES                                                                                                                                                                                                                                                                                                              | Z2_ADJUST |       |       |       |       |       | 00h           |
| Bit              | Name       |                                           | R/W   | Description                                                                                                                                                                                                                                                                                                      |           |       |       |       |       |       |               |
| 5:0              | Z2_ADJUST  |                                           | R/W   | 6-bit signed 2's complement offset adjustment. This value is added to all zone 2 temperature measurements as they are made. All LM93 registers and functions behave as if the resulting temperature was the true measured temperature. This register allows offset adjustments from +31°C to -32°C in 1°C steps. |           |       |       |       |       |       |               |
| 7:6              | RES        |                                           | R     | Reserved                                                                                                                                                                                                                                                                                                         |           |       |       |       |       |       |               |

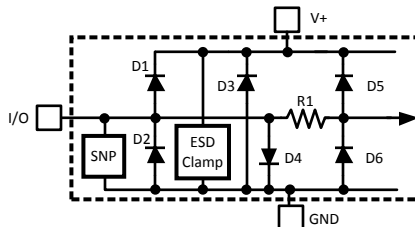


## 4 Electrical Specifications

### 4.1 Absolute Maximum Ratings <sup>(1)(2)(3)</sup>

|                                                                                                                                                                              |                                         |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|
| Positive Supply Voltage ( $V_{DD}$ )                                                                                                                                         | 6.0V                                    |
| Voltage on Any Digital Input or Output Pin                                                                                                                                   | -0.3V to 6.0V<br>(Except Analog Inputs) |
| Voltage on +5V Input                                                                                                                                                         | -0.3V to +6.667V                        |
| Voltage at Positive Thermal Diode Inputs, $\pm 12V$ Inputs                                                                                                                   | -0.3V to ( $V_{DD} + 0.05V$ )           |
| Voltage at Other Analog Voltage Inputs                                                                                                                                       | -0.3V to +6.0V                          |
| Input Current at Thermal Diode Negative Inputs                                                                                                                               | $\pm 1$ mA                              |
| Input Current at any pin <sup>(4)</sup>                                                                                                                                      | $\pm 10$ mA                             |
| Package Input Current <sup>(4)</sup>                                                                                                                                         | $\pm 100$ mA                            |
| Maximum Junction Temperature ( $T_{JMAX}$ ) <sup>(5)</sup>                                                                                                                   | 150 °C                                  |
| ESD Susceptibility <sup>(6)</sup>                                                                                                                                            |                                         |
| Human Body Model                                                                                                                                                             | 3 kV                                    |
| Machine Model                                                                                                                                                                | 300V                                    |
| Storage Temperature                                                                                                                                                          | -65°C to +150°C                         |
| <b>Soldering process must comply with reflow temperature profile specifications. Refer to <a href="http://www.ti.com/packaging">www.ti.com/packaging</a>. <sup>(7)</sup></b> |                                         |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the DC Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) All voltages are measured with respect to GND, unless otherwise noted.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (4) When the input voltage ( $V_{IN}$ ) at any pin exceeds the power supplies ( $V_{IN} < (GND \text{ or } AGND)$  or  $V_{IN} > V_{DD}$ , except for analog voltage inputs), the current at that pin should be limited to 10 mA. The 100 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to ten. Parasitic components and/or ESD protection circuitry are shown below for the LM93's pins. Care should be taken not to forward bias the parasitic diode, D1, present on pins D+ and D-. Doing so by more than 50 mV may corrupt temperature measurements. An "✓" in [Table 4-1](#) below indicates that the device is connected to the pin listed. D3 and the ESD Clamp are connected between  $V+$  ( $V_{DD}$ , AD\_IN16) and GND. SNP stands for snap-back device.



- (5) Typical parameters are at  $T_J = T_A = 25$  °C and represent most likely parametric norm.
- (6) Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor. Machine model, 200 pF discharged directly into each pin.
- (7) Reflow temperature profiles are different for lead-free and non lead-free packages.

## 4.2 Operating Ratings <sup>(1)(2)</sup>

|                                           |                                                       |
|-------------------------------------------|-------------------------------------------------------|
| Operating Temperature Range               | $0^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ |
| Nominal Supply Voltage                    | 3.3V                                                  |
| Supply Voltage Range ( $V_{DD}$ )         | +3.0V to +3.6V                                        |
| VID0-VID5                                 | -0.05V to +5.5V                                       |
| Digital Input Voltage Range               | -0.05V to ( $V_{DD} + 0.05V$ )                        |
| Package Thermal Resistance <sup>(3)</sup> | 79°C/W                                                |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the DC Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) All voltages are measured with respect to GND, unless otherwise noted.
- (3) The maximum power dissipation must be de-rated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$  and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any temperature is  $PD = (T_{JMAX} - T_A) / \theta_{JA}$ . The  $\theta_{JA}$  for the LM93 when mounted to 1 oz. copper foil PCB with different air flow is listed in the following table.

| Air Flow            | Junction to Ambient Thermal Resistance, $\theta_{JA}$ |
|---------------------|-------------------------------------------------------|
| 0 m/s               | 79 °C/W                                               |
| 1.14 m/s (225 LFPM) | 62 °C/W                                               |
| 2.54 m/s (500 LFPM) | 52 °C/W                                               |

## 4.3 DC Electrical Characteristics

The following limits apply for +3.0  $V_{DC}$  to +3.6  $V_{DC}$ , unless otherwise noted. **Bold face limits apply for  $T_A = T_J$  over  $T_{MIN}$  to  $T_{MAX}$  of the operating range**; all other limits  $T_A = T_J = 25^{\circ}\text{C}$  unless otherwise noted.  $T_A$  is the ambient temperature of the LM93;  $T_J$  is the junction temperature of the LM93;  $T_D$  is the junction temperature of the thermal diode.

| Symbol                                                  | Parameter                                                                                                           | Conditions                                                                                                      | Typical (1) | Limits (2)                  | Units (Limits)           |
|---------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------|-------------|-----------------------------|--------------------------|
| <b>POWER SUPPLY CHARACTERISTICS</b>                     |                                                                                                                     |                                                                                                                 |             |                             |                          |
|                                                         | Power Supply Current                                                                                                | Converting, Interface and Fans Inactive, Peak Current                                                           | 2           | <b>3</b>                    | mA (max)                 |
|                                                         |                                                                                                                     | Converting, Interface and Fans Inactive, Average Current                                                        | 0.9         |                             | mA                       |
|                                                         | Power-On Reset Threshold Voltage                                                                                    |                                                                                                                 | 2           | <b>1.6</b>                  | V (min)                  |
|                                                         |                                                                                                                     |                                                                                                                 |             | <b>2.7</b>                  | V (max)                  |
| <b>TEMPERATURE-TO-DIGITAL CONVERTER CHARACTERISTICS</b> |                                                                                                                     |                                                                                                                 |             |                             |                          |
|                                                         | Local Temperature Accuracy Over Full Range                                                                          | $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$                                                            | $\pm 2$     | <b><math>\pm 3</math></b>   | $^{\circ}\text{C}$ (max) |
|                                                         |                                                                                                                     | $T_A = +55^{\circ}\text{C}$                                                                                     | $\pm 1$     | <b><math>\pm 2.8</math></b> | $^{\circ}\text{C}$ (max) |
|                                                         | Local Temperature Resolution                                                                                        |                                                                                                                 | 1           |                             | $^{\circ}\text{C}$       |
|                                                         | Remote Thermal Diode Temperature Accuracy Over Full Range; targeted for a typical Prescott processor <sup>(3)</sup> | $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $25^{\circ}\text{C} \leq T_D \leq 100^{\circ}\text{C}$ |             | <b><math>\pm 3</math></b>   | $^{\circ}\text{C}$ (max) |
|                                                         | Remote Thermal Diode Temperature Accuracy; targeted for a typical Prescott processor <sup>(3)</sup>                 | $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $25^{\circ}\text{C} \leq T_D \leq 70^{\circ}\text{C}$  | $\pm 1$     |                             | $^{\circ}\text{C}$       |
|                                                         | Remote Temperature Resolution                                                                                       |                                                                                                                 | 1           |                             | $^{\circ}\text{C}$       |
|                                                         | Thermal Diode Source Current                                                                                        | High Level                                                                                                      | 188         | 280                         | $\mu\text{A}$ (max)      |
|                                                         |                                                                                                                     | Low Level                                                                                                       | 11.75       |                             | $\mu\text{A}$            |
|                                                         | Thermal Diode Current Ration                                                                                        |                                                                                                                 | 16          |                             |                          |
| $T_C$                                                   | Total Monitoring Cycle Time                                                                                         |                                                                                                                 |             | <b>100</b>                  | ms (max)                 |

- (1) Typical parameters are at  $T_J = T_A = 25^{\circ}\text{C}$  and represent most likely parametric norm.
- (2) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
- (3) When measuring an MMBT3904 transistor, 4  $^{\circ}\text{C}$  should be subtracted from all temperature readings.

**DC Electrical Characteristics (continued)**

The following limits apply for +3.0 V<sub>DC</sub> to +3.6 V<sub>DC</sub>, unless otherwise noted. **Bold face limits apply for T<sub>A</sub> = T<sub>J</sub> over T<sub>MIN</sub> to T<sub>MAX</sub> of the operating range;** all other limits T<sub>A</sub> = T<sub>J</sub> = 25°C unless otherwise noted. T<sub>A</sub> is the ambient temperature of the LM93; T<sub>J</sub> is the junction temperature of the LM93; T<sub>D</sub> is the junction temperature of the thermal diode.

| Symbol                                                                                                                                  | Parameter                                                                                                            | Conditions                                              | Typical<br>(1) | Limits<br>(2)                                          | Units<br>(Limits)  |
|-----------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|----------------|--------------------------------------------------------|--------------------|
| <b>ANALOG-TO-DIGITAL VOLTAGE MEASUREMENT CONVERTER CHARACTERISTICS</b>                                                                  |                                                                                                                      |                                                         |                |                                                        |                    |
| TUE <sup>(1)</sup>                                                                                                                      | Total Unadjusted Error <sup>(2)</sup>                                                                                |                                                         |                | <b>±2</b>                                              | % of FS (max)      |
| DNL                                                                                                                                     | Differential Non-Linearity                                                                                           |                                                         | ±1             |                                                        | LSB                |
| PSS                                                                                                                                     | Power Supply (V <sub>DD</sub> ) Sensitivity                                                                          |                                                         | ±1             |                                                        | %/V (of FS)        |
| T <sub>C</sub>                                                                                                                          | Total Monitoring Cycle Time                                                                                          |                                                         |                | <b>100</b>                                             | ms (max)           |
|                                                                                                                                         | Input Resistance for Inputs with Dividers                                                                            |                                                         | 200            | <b>140</b>                                             | kΩ (min)           |
|                                                                                                                                         | AD_IN1- AD_IN3 and AD_IN15 Analog Input Leakage Current <sup>(3)</sup>                                               |                                                         |                | 60                                                     | nA (max)           |
| <b>REFERENCE OUTPUT (V<sub>REF</sub>) CHARACTERISTICS</b>                                                                               |                                                                                                                      |                                                         |                |                                                        |                    |
|                                                                                                                                         | Tolerance                                                                                                            |                                                         |                | <b>±1</b>                                              | % (max)            |
| V <sub>REF</sub>                                                                                                                        | Output Voltage <sup>(4)</sup>                                                                                        |                                                         | 2.500          | <b>2.525</b><br><b>2.475</b>                           | V (max)<br>V (min) |
|                                                                                                                                         | Load Regulation                                                                                                      | I <sub>SOURCE</sub> = -2 mA<br>I <sub>SINK</sub> = 2 mA | 0.1            |                                                        | %                  |
| <b>DIGITAL OUTPUTS: PWM1, PWM2</b>                                                                                                      |                                                                                                                      |                                                         |                |                                                        |                    |
| I <sub>OL</sub>                                                                                                                         | Current Sink                                                                                                         |                                                         |                | <b>8</b>                                               | mA (min)           |
| V <sub>OL</sub>                                                                                                                         | Output Low Voltage                                                                                                   | I <sub>OUT</sub> = 8.0 mA                               |                | <b>0.4</b>                                             | V (max)            |
| <b>DIGITAL OUTPUTS: ALL</b>                                                                                                             |                                                                                                                      |                                                         |                |                                                        |                    |
| V <sub>OL</sub>                                                                                                                         | Output Low Voltage (Note excessive current flow causes self-heating and degrades the internal temperature accuracy.) | I <sub>OUT</sub> = 4.0 mA                               |                | <b>0.4</b>                                             | V (min)            |
|                                                                                                                                         |                                                                                                                      | I <sub>OUT</sub> = 6 mA                                 |                | <b>0.55</b>                                            | V (min)            |
| I <sub>OH</sub>                                                                                                                         | High Level Output Leakage Current                                                                                    | V <sub>OUT</sub> = V <sub>DD</sub>                      | 0.1            | <b>10</b>                                              | μA (max)           |
| I <sub>OTMAX</sub>                                                                                                                      | Maximum Total Sink Current for all Digital Outputs Combined                                                          |                                                         |                | <b>32</b>                                              | mA (max)           |
| C <sub>O</sub>                                                                                                                          | Digital Output Capacitance                                                                                           |                                                         | 20             |                                                        | pF                 |
| <b>DIGITAL INPUTS: ALL</b>                                                                                                              |                                                                                                                      |                                                         |                |                                                        |                    |
| V <sub>IH</sub>                                                                                                                         | Input High Voltage Except Address Select                                                                             |                                                         |                | <b>2.1</b>                                             | V (min)            |
| V <sub>IL</sub>                                                                                                                         | Input Low Voltage Except Address Select                                                                              |                                                         |                | <b>0.8</b>                                             | V (max)            |
| V <sub>IH</sub>                                                                                                                         | Input High Voltage for Address Select                                                                                |                                                         |                | <b>90% V<sub>DD</sub></b>                              | V (min)            |
| V <sub>IM</sub>                                                                                                                         | Input Mid Voltage for Address Select                                                                                 |                                                         |                | <b>43% V<sub>DD</sub></b><br><b>57% V<sub>DD</sub></b> | V (min)<br>V (max) |
| V <sub>IL</sub>                                                                                                                         | Input Low Voltage for Address Select                                                                                 |                                                         |                | <b>10% V<sub>DD</sub></b>                              | V (max)            |
| V <sub>HYST</sub>                                                                                                                       | DC Hysteresis                                                                                                        |                                                         | 0.3            |                                                        | V                  |
| I <sub>IH</sub>                                                                                                                         | Input High Current                                                                                                   | V <sub>IN</sub> = V <sub>DD</sub>                       |                | <b>-10</b>                                             | μA (min)           |
| I <sub>IL</sub>                                                                                                                         | Input Low Current                                                                                                    | V <sub>IN</sub> = 0V                                    |                | <b>10</b>                                              | μA (max)           |
| C <sub>IN</sub>                                                                                                                         | Digital Input Capacitance                                                                                            |                                                         | 20             |                                                        | pF                 |
| <b>DIGITAL INPUTS: P1_VIDx, P2_VIDx, GPIO_7, GPIO_6, GPIO_5, GPIO_4 (When respective bit set in Register BEh GPI/VID Level Control)</b> |                                                                                                                      |                                                         |                |                                                        |                    |
| V <sub>IH</sub>                                                                                                                         | Alternate Input High Voltage (AGTL+ Compatible)                                                                      |                                                         |                | <b>0.8</b>                                             | V (min)            |
| V <sub>IL</sub>                                                                                                                         | Alternate Input Low Voltage (AGTL+ Compatible)                                                                       |                                                         |                | <b>0.4</b>                                             | V (max)            |

(1) TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

(2) Total Monitoring Cycle Time includes all temperature and voltage conversions.

(3) Leakage current approximately doubles every 20 °C.

(4) A total digital I/O current of 40mA can cause 6mV of offset in Vref.

#### 4.4 AC Electrical Characteristics

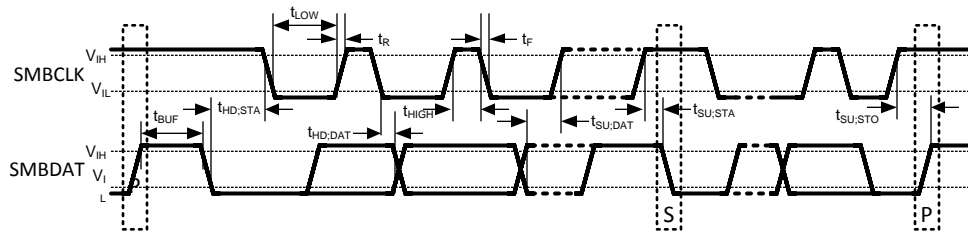
The following limits apply for +3.0 V<sub>DC</sub> to +3.6 V<sub>DC</sub>, unless otherwise noted. **Bold face limits apply for T<sub>A</sub> = T<sub>J</sub> = T<sub>MIN</sub> to T<sub>MAX</sub> of the operating range;** all other limits T<sub>A</sub> = T<sub>J</sub> = 25°C unless otherwise noted.

| Symbol                                            | Parameter                                                                                      | Conditions                | Typical<br>(1) | Limits<br>(2)            | Units<br>(Limits)          |
|---------------------------------------------------|------------------------------------------------------------------------------------------------|---------------------------|----------------|--------------------------|----------------------------|
| <b>FAN RPM-TO-DIGITAL CHARACTERISTICS</b>         |                                                                                                |                           |                |                          |                            |
|                                                   | Counter Resolution                                                                             |                           | 14             |                          | bits                       |
|                                                   | Number of fan tach pulses count is based on                                                    |                           | 2              |                          | pulses                     |
|                                                   | Counter Frequency                                                                              |                           | 22.5           |                          | kHz                        |
|                                                   | Accuracy                                                                                       |                           |                | ±6                       | % (max)                    |
| <b>PWM OUTPUT CHARACTERISTICS</b>                 |                                                                                                |                           |                |                          |                            |
|                                                   | Frequency Tolerances                                                                           |                           |                | ±6                       | % (max)                    |
|                                                   | Duty-Cycle Tolerance                                                                           |                           | ±2             | ±6                       | % (max)                    |
| <b>RESET INPUT/OUTPUT CHARACTERISTICS</b>         |                                                                                                |                           |                |                          |                            |
|                                                   | Output Pulse Width Upon Power Up                                                               |                           |                | <b>250</b><br><b>330</b> | ms (min)<br>ms (max)       |
|                                                   | Minimum Input Pulse Width                                                                      |                           |                | <b>10</b>                | µs (min)                   |
|                                                   | Reset Output Fall Time                                                                         | 1.6V to 0.4V Logic Levels |                | <b>1</b>                 | µs (max)                   |
| <b>SMBUS TIMING CHARACTERISTICS<sup>(3)</sup></b> |                                                                                                |                           |                |                          |                            |
| f <sub>SMBCLK</sub>                               | SMBCLK (Clock) Clock Frequency                                                                 |                           |                | <b>10</b><br><b>100</b>  | kHz (min)<br>kHz (max)     |
| t <sub>BUF</sub>                                  | SMBus Free Time between Stop and Start Conditions                                              |                           |                | <b>4.7</b>               | µs (min)                   |
| t <sub>HD;STA</sub>                               | Hold time after (Repeated) Start Condition. After this period, the first clock is generated.   |                           |                | <b>4.0</b>               | µs (min)                   |
| t <sub>SU;STA</sub>                               | Repeated Start Condition Setup Time                                                            |                           |                | <b>4.7</b>               | µs (min)                   |
| t <sub>SU;STO</sub>                               | Stop Condition Setup Time                                                                      |                           |                | <b>4.0</b>               | µs (min)                   |
| t <sub>SU;DAT</sub>                               | Data Input Setup Time to SMBCLK High                                                           |                           |                | <b>250</b>               | ns (min)                   |
| t <sub>HD;DAT</sub>                               | Data Output Hold Time after SMBCLK Low                                                         |                           |                | <b>300</b><br><b>930</b> | ns (min)<br>ns (max)       |
| t <sub>LOW</sub>                                  | SMBCLK Low Period                                                                              |                           |                | <b>4.7</b><br><b>50</b>  | µs (min)<br>µs (max)       |
| t <sub>HIGH</sub>                                 | SMBCLK High Period                                                                             |                           |                | <b>4.0</b><br><b>50</b>  | µs (min)<br>µs (max)       |
| t <sub>R</sub>                                    | Rise Time                                                                                      |                           |                | <b>1</b>                 | µs (max)                   |
| t <sub>F</sub>                                    | Fall Time                                                                                      |                           |                | <b>300</b>               | ns (max)                   |
| t <sub>TIMEOUT</sub>                              | Timeout SMBDAT or SMBCLK low time required to reset the Serial Bus Interface to the Idle State |                           | 31             | <b>25</b><br><b>35</b>   | ms<br>ms (min)<br>ms (max) |
| t <sub>POR</sub>                                  | Time in which a device must be operational after power-on reset                                | V <sub>DD</sub> > +2.8V   |                | <b>500</b>               | ms (max)                   |
| C <sub>L</sub>                                    | Capacitance Load on SMBCLK and SMBDAT                                                          |                           |                | <b>400</b>               | pF (max)                   |

(1) Typical parameters are at T<sub>J</sub> = T<sub>A</sub> = 25 °C and represent most likely parametric norm.

(2) Limits are specified to TI's AOQL (Average Outgoing Quality Level).

(3) Timing specifications are tested at the TTL logic levels, V<sub>IL</sub> = 0.4V for a falling edge and V<sub>IH</sub> = 2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.



**Table 4-1.**

| Symbol                | Pin # | D1                             | D2 | D4 | D5 | D6 | SNP | R1   |  |
|-----------------------|-------|--------------------------------|----|----|----|----|-----|------|--|
| GPIO_0/TACH1          | 1     |                                | ✓  |    |    | ✓  | ✓   | 50 Ω |  |
| GPIO_1/TACH2          | 2     |                                | ✓  |    |    | ✓  | ✓   | 50 Ω |  |
| GPIO_2/TACH3          | 3     |                                | ✓  |    |    | ✓  | ✓   | 50 Ω |  |
| GPIO_3/TACH4          | 4     |                                | ✓  |    |    | ✓  | ✓   | 50 Ω |  |
| GPIO_4 / P1_THERMTRIP | 5     |                                | ✓  |    |    | ✓  | ✓   | 50 Ω |  |
| GPIO_5 / P2_THERMTRIP | 6     |                                | ✓  |    |    | ✓  | ✓   | 50 Ω |  |
| GPIO_6                | 7     |                                | ✓  |    |    | ✓  | ✓   | 50 Ω |  |
| GPIO_7                | 8     |                                | ✓  |    |    | ✓  | ✓   | 50 Ω |  |
| VRD1_HOT              | 9     |                                | ✓  |    |    |    | ✓   |      |  |
| VRD2_HOT              | 10    |                                | ✓  |    |    |    | ✓   |      |  |
| SCSI_TERM1            | 11    |                                | ✓  |    |    |    | ✓   |      |  |
| SCSI_TERM2            | 12    |                                | ✓  |    |    |    | ✓   |      |  |
| SMBDAT                | 13    |                                | ✓  |    |    |    | ✓   |      |  |
| SMBCLK                | 14    |                                | ✓  |    |    |    | ✓   |      |  |
| ALERT/XtestOut        | 15    |                                | ✓  |    |    |    | ✓   |      |  |
| RESET                 | 16    |                                | ✓  |    |    |    | ✓   |      |  |
| AGND                  | 17    | Internally shorted to GND pin. |    |    |    |    |     |      |  |
| V <sub>REF</sub>      | 18    | ✓                              | ✓  |    |    |    |     |      |  |
| REMOTE1-              | 19    | ✓                              | ✓  | ✓  | ✓  | ✓  |     | 50 Ω |  |
| REMOTE1+              | 20    | ✓                              | ✓  |    | ✓  | ✓  |     | 50 Ω |  |
| REMOTE2-              | 21    | ✓                              | ✓  | ✓  | ✓  | ✓  |     | 50 Ω |  |
| REMOTE+               | 22    | ✓                              | ✓  |    | ✓  | ✓  |     | 50 Ω |  |
| AD_IN1                | 23    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN2                | 24    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN3                | 25    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN4                | 26    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN5                | 27    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN6                | 28    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN7                | 29    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN8                | 30    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN9                | 31    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN10               | 32    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN11               | 33    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN12               | 34    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN13               | 35    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN14               | 36    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |
| AD_IN15               | 37    |                                | ✓  |    | ✓  | ✓  | ✓   | ✓    |  |

Table 4-1. (continued)

| Symbol                       | Pin # | D1                          | D2 | D4 | D5 | D6 | SNP | R1   |
|------------------------------|-------|-----------------------------|----|----|----|----|-----|------|
| ADDR_SEL                     | 38    |                             | ✓  |    |    |    | ✓   |      |
| AD_IN16/V <sub>DD</sub> (V+) | 39    |                             | ✓  |    | ✓  | ✓  |     | ✓    |
| GND                          | 40    | Internally shorted to AGND. |    |    |    |    |     |      |
| PWM1                         | 41    |                             | ✓  |    |    | ✓  | ✓   | 50 Ω |
| PWM2                         | 42    |                             | ✓  |    |    | ✓  | ✓   | 50 Ω |
| P1_VID0                      | 43    |                             | ✓  |    |    |    | ✓   |      |
| P1_VID1                      | 44    |                             | ✓  |    |    |    | ✓   |      |
| P1_VID2                      | 45    |                             | ✓  |    |    |    | ✓   |      |
| P1_VID3                      | 46    |                             | ✓  |    |    |    | ✓   |      |
| P1_VID4                      | 47    |                             | ✓  |    |    |    | ✓   |      |
| P1_VID5                      | 48    |                             | ✓  |    |    |    | ✓   |      |
| P1_PROCHOT                   | 49    |                             | ✓  |    |    | ✓  | ✓   | 50 Ω |
| P2_PROCHOT                   | 50    |                             | ✓  |    |    | ✓  | ✓   | 50 Ω |
| P2_VID0                      | 51    |                             | ✓  |    |    |    | ✓   |      |
| P2_VID1                      | 52    |                             | ✓  |    |    |    | ✓   |      |
| P2_VID2                      | 53    |                             | ✓  |    |    |    | ✓   |      |
| P2_VID3                      | 54    |                             | ✓  |    |    |    | ✓   |      |
| P2_VID4                      | 55    |                             | ✓  |    |    |    | ✓   |      |
| P2_VID5                      | 56    |                             | ✓  |    |    |    | ✓   |      |

### Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Revision | Date              | Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F        | March 27, 2013    | Changed layout of National Data Sheet to TI Format                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2.0      | April 12, 2004    | <ol style="list-style-type: none"> <li>Updated <a href="#">Registers 80–83h Fan Boost Temperature Registers</a>, changed "If set to 80h, the feature is disabled." to "If set to 7Fh and the fan control temperature resolution is 1°C, the feature is disabled."</li> <li>Updated <a href="#">DC Electrical Characteristics</a>, Thermal Diode Source Current typical specifications, changed: "170" to 188" and "10.625" to "11.75".</li> <li>Updated <a href="#">DC Electrical Characteristics</a>, added Thermal Diode Current Ratio typical specification.</li> <li>Updated <a href="#">Absolute Maximum Ratings</a>, replaced Soldering Information with note.</li> </ol> |
| 1.2      | February 22, 2004 | <ol style="list-style-type: none"> <li>Typographical changes</li> </ol>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1.1      | December 22, 2004 | <ol style="list-style-type: none"> <li>Typographical changes</li> </ol>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1.0      | November 11, 2003 | <ol style="list-style-type: none"> <li>Final data sheet initial release</li> </ol>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| LM93C1MT/NOPB    | OBSOLETE      | TSSOP        | DGG             | 56   |             | TBD             | Call TI                              | Call TI              | 0 to 85      | LM93C1MT                |         |
| LM93C1MTX/NOPB   | ACTIVE        | TSSOP        | DGG             | 56   | 1000        | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | 0 to 85      | LM93C1MT                | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM93CIMTX/NOPB | TSSOP        | DGG             | 56   | 1000 | 330.0              | 24.4               | 8.6     | 14.5    | 1.8     | 12.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM93CIMTX/NOPB | TSSOP        | DGG             | 56   | 1000 | 356.0       | 356.0      | 45.0        |



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NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

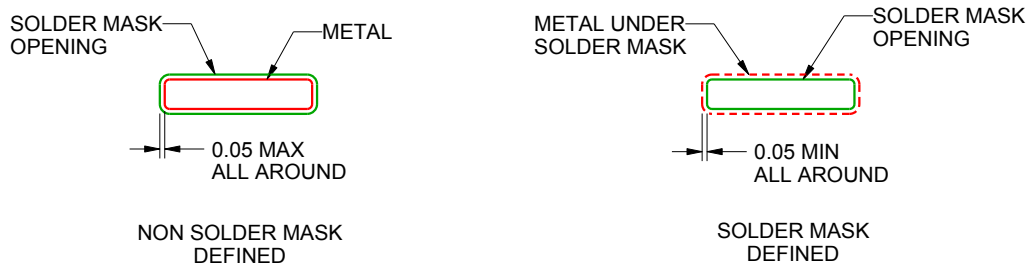
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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