# LMT70, LMT70A ±0.05°C Precision Analog Temperature Sensor, RTD and Precision NTC Thermistor IC

## 1 Features

- Accuracy:
  - ±0.05°C (typ) or ±0.13°C (max) from 20°C to 42°C
  - ±0.2°C (max) from -20°C to 90°C
  - ±0.23°C (max) from 90°C to 110°C
  - ±0.36°C (max) from -55°C to 150°C
- Wide Temperature Range: −55°C to 150°C
- Matching of Two Adjacent LMT70A on Tape and Reel: 0.1°C (max) at 30°C
- Very Linear Analog Temperature Sensor with Output Enable Pin
- NTC Output Slope: -5.19 mV/°C
- Output On/Off Switch with $R_{DS\ on}$ < 80 Ω
- Wide Power Supply Range: 2.0 V to 5.5 V
- Low Power Supply Current: 9.2 µA (typ)12 µA (max)
- Ultra Small 0.88 mm by 0.88 mm 4-bump WLCSP (DSBGA) Package

## 2 Applications

- Internet of Things (IoT) Sensor Nodes
- Industrial RTD (Class AA) or Precision NTC/PTC Thermistor Replacement
- Medical/Fitness Equipment
- Medical Thermometer
- Human Body temperature monitor
- Metering Temperature Compensation

## 3 Description

The LMT70 is an ultra-small, high-precision, low-power CMOS analog temperature sensor with an output enable pin. Applications for the LMT70 include virtually any type of temperature sensing where cost-effective, high precision and low-power are required, such as Internet of Things (IoT) sensor nodes, medical thermometers, high-precision instrumentation and battery powered devices. The LMT70 is also a great replacement for RTD and precision NTC/PTC thermistors.

Its output enable pin allows multiple LMT70s to share one ADC channel, thus simplifying ADC calibration and reducing the overall system cost for precision temperature sensing. The LMT70 also has a linear and low impedance output allowing seamless interface to an off-the-shelf MCU/ADC. Dissipating less than 36µW, the LMT70 has ultra-low self-heating supporting its high-precision over a wide temperature range.

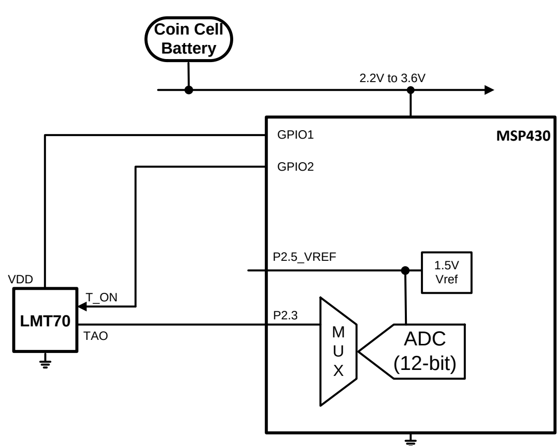
The LMT70A provides unparalleled temperature matching performance of 0.1°C (max) for two adjacent LMT70A's picked from the same tape and reel. Therefore, the LMT70A is an ideal solution for energy metering applications requiring heat transfer calculations.

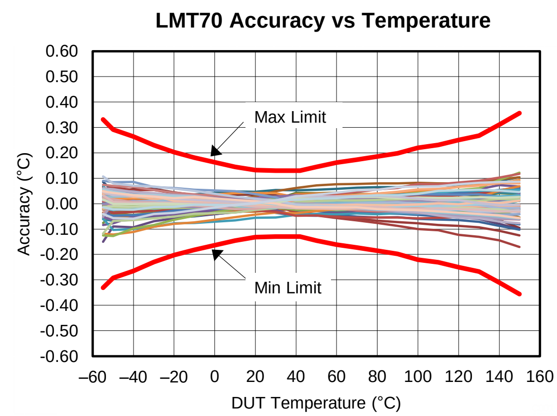
**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LMT70 | DSBGA - WLCSP (4) YFQ | 0.88 mm x 0.88 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Wide-Range Precision Active RTD or NTC Replacement (−55°C to 150°C)



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## 5 Revision History

**Changes from Original (March 2015) to Revision A** | **Page**

- Added typical accuracy specification. ........ 1
- Expanded range for ±0.2°C accuracy from "20°C to 90°C" to "-20°C to 90°C". ........ 1
- Added 9.2µA (typ). ........ 1
- Updated schematic ........ 3
- Added -20°C accuracy specification ........ 5
- Changed from 20°C to 20°C to 42°C for accuracy specification condition ........ 5
- Added 50°C accuracy specification ........ 5
- Added typical supply current specification. ........ 6
- Changed from 942.547 to 942.552 ........ 6
- Changed from 943.907 to 943.902 ........ 6
- Changed from 890.423 to 890.500 ........ 6
- Changed from 891.934 to 891.857 ........ 6
- Added -20°C histogram curve ........ 8
- Removed erroneous 10°C histogram ........ 8
- Changed y axis units from (V) to (mV) ........ 9
- Added Output Noise vs Frequency curve ........ 10

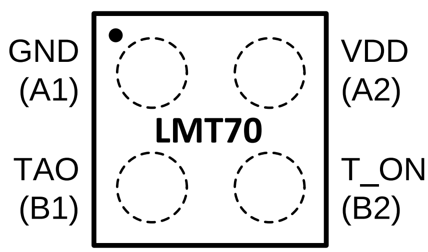
# 6 Device Comparison Table

| Order Number | Matching Specification Provided (1) |
|---|---|
| LMT70YFQR, LMT70YFQT | No |
| LMT70AYFQR, LMT70AYFQT | Yes, 0.1°C at approximately 30°C (1) |

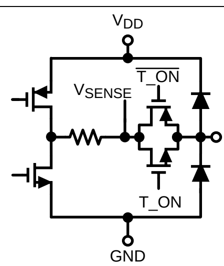
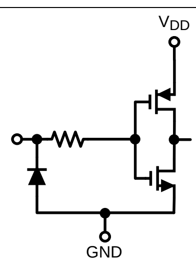
(1) In order to meet the matching specification of the LMT70A, two units must be picked from adjacent positions from one tape and reel. If PCB rework is required, involving the LMT70A, then the pair of the LMT70A matched units must be replaced. Matching features (which include, without limitation, electrical matching characteristics of adjacent Components as they are delivered in original packaging from TI) are warranted solely to the extent that the purchaser can demonstrate to TI's satisfaction that the particular Component(s) at issue were adjacent in original packaging as delivered by TI. Customers should be advised that the small size of these Components means they are not individually traceable at the unit level and it may be difficult to establish the original position of the Components once they have been removed from that original packaging as delivered by TI.

# 7 Pin Configuration and Functions

**DSBGA or WLCSP**
**4 Pins YFQ**
**(Top View)**




**Pin Functions**

| PIN | | TYPE | EQUIVALENT CIRCUIT | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| GND | A1 | Ground | | Ground reference for the device |
| VDD | A2 | Power | | Supply voltage |
| TAO | B1 | Analog Output |  | Temperature analog output pin |
| T_ON | B2 | Digital Input |  | T_ON pin. Active High input.<br>If T_ON = 0, then the TAO output is open.<br>If T_ON = 1, then TAO pin is connected to the temperature output voltage.<br>Tie this pin to VDD if not used. |

# 8 Specifications

## 8.1 Absolute Maximum Ratings(1)(2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage | −0.3 | 6 | V |
| Voltage at T_ON and TAO | −0.3 | 6 | V |
| Current at any pin | | 5 | mA |
| Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Soldering process must comply with Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Specified temperature ($T_{MIN} \le T_A \le T_{MAX}$) | −55 | | 150 | °C |
| Supply voltage | 2.0 | | 5.5 | V |

## 8.4 Thermal Information

| THERMAL METRIC[1] | | LMT70 DSBGA or WLCSP YFQ 4 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 187 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 2.3 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 105 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 104 | |
| | Thermal response time to 63% of final value in stirred oil (dominated by PCB see layout) | 1.5 | sec |
| | Thermal response time to 63% of final value in still air (dominated by PCB see layout) | 73 | sec |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 8.5 Electrical Characteristics

Limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$ and VDD of 2.00V to 5.5V and VDD ≥ $V_{TAO}$ + 1V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **TEMPERATURE ACCURACY** | | | | | | | |
| | TAO accuracy (These stated accuracy limits are with reference to the values in *Electrical Characteristics Temperature Lookup Table (LUT)*, LMT70 temperature-to-voltage.)[1] | $T_A$ = –55°C | VDD = 2.7 V | -0.33 | | 0.33 | |
| | | $T_A$ = –40°C | VDD = 2.7 V | –0.27 | | 0.27 | |
| | | $T_A$ = –20°C | VDD = 2.7 V | –0.2 | | 0.2 | |
| | | $T_A$ = –10°C | VDD = 2.7 V | –0.18 | | 0.18 | |
| | | $T_A$ = 20°C to 42°C | VDD = 2.7 V | –0.13 | ±0.05 | 0.13 | °C |
| | | $T_A$ = 50°C | VDD = 2.7 V | -0.15 | | 0.15 | |
| | | $T_A$ = 90°C | VDD = 2.7 V | –0.20 | | 0.20 | |
| | | $T_A$ = 110°C | VDD = 2.7 V | –0.23 | | 0.23 | |
| | | $T_A$ = 150°C | VDD = 2.7 V | –0.36 | | 0.36 | |
| ATC | Accuracy temperature coefficient (note, uses end point calculations)[2] | VDD = 2.7V | | -2.6 | | +2.6 | m°C/°C |
| APSS | Accuracy power supply sensitivity (note uses end point calculations) | –55°C ≤ $T_A$ ≤ 10°C | VDD = $V_{TAO}$ + 1.1 V to 4.0 V | –9 | –2 | 8 | m°C /V |
| | | 10°C ≤ $T_A$ ≤ 120°C | VDD = 2.0 V to 4.0 V | | | | |
| | | 120°C ≤ $T_A$ ≤ 150°C | VDD = 2.0 V to 4.0 V | –15 | | 8 | |
| | | | VDD = 4 V to 5.5 V | –30 | –12 | 0 | |
| $V_{TAO}$ | Output Voltage | $T_A$ = 30°C | VDD = 2.7 V | | 943.227 | | mV |
| | Sensor gain | | | | –5.194 | | mV/°C |
| | Matching of two adjacent parts in tape and reel for LMT70AYFQR, LMT70AYFQT only (see curve Figure 19 for specification at other temperatures)[3][2] | $T_A$ approximately 30°C | $V_{DD}$ = 2.0 V to 3.6 V | | | 0.1 | °C |
| | | $T_A$ = 30°C to 150°C | | | | 2.5 | m°C /°C |
| | | $T_A$ = 20°C to 30°C | $V_{DD}$ = 2.0 V to 3.6 V | -2.5 | | | |
| | | $T_A$ = -55°C to 30°C | $V_{DD}$ = 2.7 V to 3.6 V | –2.5 | | | |
| | Time stability[4] | 10k hours at 90°C | | –0.1 | ±0.01 | 0.1 | °C |
| **ANALOG OUTPUT** | | | | | | | |
| | Operating output voltage change with load current | 0 µA≤$I_L$≤5 µA | | 0 | | 0.4 | mV |
| | | -5 µA≤$I_L$≤0 µA | | -0.4 | | 0 | mV |
| ROUT | Output Resistance | | | | 28 | 80 | Ω |
| | TAO Off Leakage Current | $V_{TAO}$ ≤ VDD – 0.6v, $V_{T\_ON}$=GND | | | 0.005 | 0.5 | µA |
| | | $V_{TAO}$ ≥ 0.2V, $V_{T\_ON}$ = GND | | -0.5 | -0.005 | | |
| | Output Load Capacitance | | | | | 1100 | pF |

(1) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Conversion Table at the specified conditions of supply voltage and temperature (expressed in °C). These stated accuracy limits are with reference to the values in *Electrical Characteristics Temperature Lookup Table (LUT)*, see Accuracy Curve for other temperatures. Accuracy limits do not include load regulation or aging; they assume no DC load.
(2) The accuracy temperature coefficient specification is given to indicate part to part performance and does not correlate to the limits given in the curve Figure 3.
(3) In order to meet the matching specification of the LMT70A, two units must be picked from adjacent positions from one tape and reel. If PCB rework is required, involving the LMT70A, then the pair of the LMT70A matched units must be replaced. Matching features (which include, without limitation, electrical matching characteristics of adjacent Components as they are delivered in original packaging from TI) are warranted solely to the extent that the purchaser can demonstrate to TI's satisfaction that the particular Component(s) at issue were adjacent in original packaging as delivered by TI. Customers should be advised that the small size of these Components means they are not individually traceable at the unit level and it may be difficult to establish the original position of the Components once they have been removed from that original packaging as delivered by TI.
(4) Determined using accelerated operational life testing at 150°C junction temperature; not tested during production.

## Electrical Characteristics (continued)

Limits apply for $T_A$ = $T_J$ = $T_{MIN}$ to $T_{MAX}$ and VDD of 2.00V to 5.5V and VDD ≥ $V_{TAO}$ + 1V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| VDO | Dropout Voltage (VDD-$V_{TAO}$)(5) | –20°C ≤ $T_A$ ≤ 20°C | 1.0 | | | V |
| | | –55°C ≤ $T_A$ ≤ –20°C | 1.1 | | | |
| | Power Supply Current | | | 9.2 | 12 | µA |
| | Shutdown Current | VDD ≤ 0.4V (-55°C to +110°C) | | | 50 | nA |
| | | VDD ≤ 0.4V (+110°C to +150°C) | | | 350 | nA |
| **LOGIC INPUT** | | | | | | |
| | T_ON Logic Low Input Threshold | -55°C to +150°C | 0.5 | 0.33*VDD | | V |
| | T_ON Logic High Input Threshold | -55°C to +150°C | | 0.66*VDD | VDD-0.5 | V |
| | T_ON Input Current | $V_{T\_ON}$ = VDD | | 0.15 | 1 | µA |
| | | $V_{T\_ON}$ = GND | -1 | -0.02 | | |

(5) Dropout voltage (VDO) is defined as the smallest possible differential voltage measured between $V_{TAO}$ and VDD that causes the temperature error to degrade by 0.02°C.

## 8.6 Electrical Characteristics Temperature Lookup Table (LUT)

applies for VDD of 2.7V

| TEMPERATURE (°C) | $V_{TAO}$ (mV) MIN | TYP | MAX | LOCAL SLOPE (mV/°C) |
|---|---|---|---|---|
| -55 | 1373.576 | 1375.219 | 1376.862 | -4.958 |
| -50 | 1348.990 | 1350.441 | 1351.892 | -4.976 |
| -40 | 1299.270 | 1300.593 | 1301.917 | -5.002 |
| -30 | 1249.242 | 1250.398 | 1251.555 | -5.036 |
| -20 | 1198.858 | 1199.884 | 1200.910 | -5.066 |
| -10 | 1148.145 | 1149.070 | 1149.995 | -5.108 |
| 0 | 1097.151 | 1097.987 | 1098.823 | -5.121 |
| 10 | 1045.900 | 1046.647 | 1047.394 | -5.134 |
| 20 | 994.367 | 995.050 | 995.734 | -5.171 |
| 30 | 942.547 | 943.227 | 943.902 | -5.194 |
| 40 | 890.500 | 891.178 | 891.857 | -5.217 |
| 50 | 838.097 | 838.882 | 839.668 | -5.241 |
| 60 | 785.509 | 786.360 | 787.210 | -5.264 |
| 70 | 732.696 | 733.608 | 734.520 | -5.285 |
| 80 | 679.672 | 680.654 | 681.636 | -5.306 |
| 90 | 626.435 | 627.490 | 628.545 | -5.327 |
| 100 | 572.940 | 574.117 | 575.293 | -5.347 |
| 110 | 519.312 | 520.551 | 521.789 | -5.368 |
| 120 | 465.410 | 466.760 | 468.110 | -5.391 |
| 130 | 411.288 | 412.739 | 414.189 | -5.430 |
| 140 | 356.458 | 358.164 | 359.871 | -5.498 |
| 150 | 300.815 | 302.785 | 304.756 | -5.538 |

## 8.7 Switching Characteristics

Limits apply for $T_A = T_J = T_{MIN}$ to $T_{MAX}$ and VDD of 2.00V to 5.5V and VDD ≥ $V_{TAO}$ + 1V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{POWER}$ | Power-on Time to 99% of final voltage value | CL=0 pF to 1100 pF; VDD connected T_ON | | 0.6 | 1 | ms |
| $t_{T\_ON}$ | T_ON Time to 99% of final voltage value (note dependent on RON and C load) | CL=150pF | | 30 | 500 | µs |
| $C_{T\_ON}$ | T_ON Digital Input Capacitance | | | 2.2 | | pF |

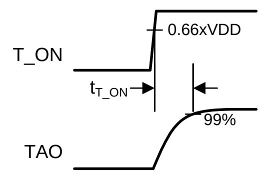



**Figure 1. Definition of $t_{T\_ON}$**

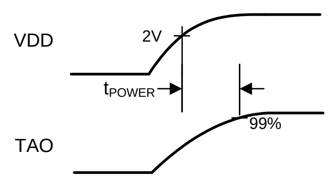
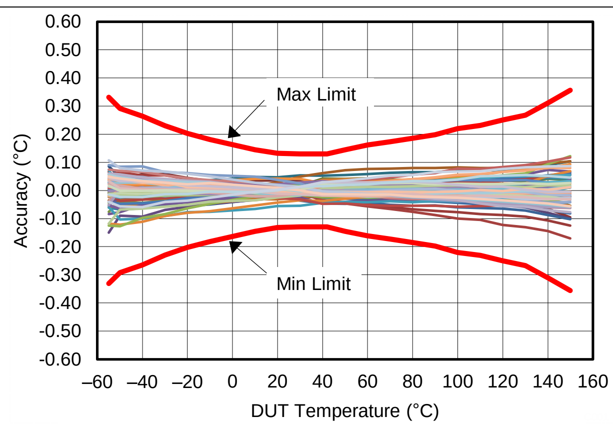


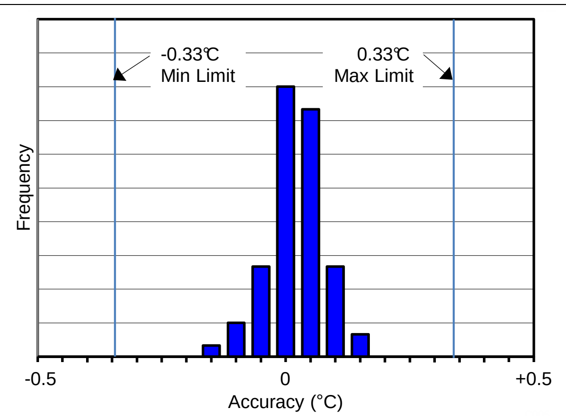

**Figure 2. Definition of $t_{POWER}$**

## 8.8 Typical Performance Characteristics




VDD=2.7V
using LUT (Look-Up Table) and linear interporlation for conversion of voltage to temperature

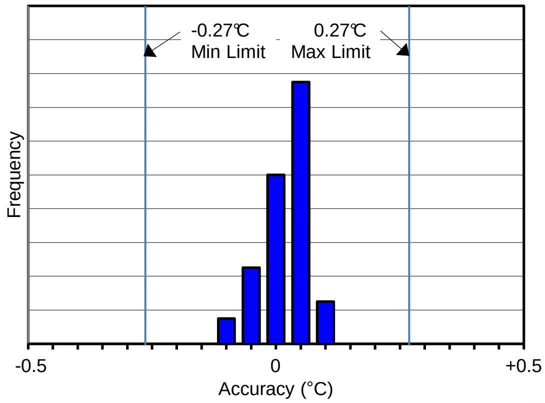
**Figure 3. Temperature Accuracy**




VDD=2.7V
using LUT table for conversion of voltage to temperature

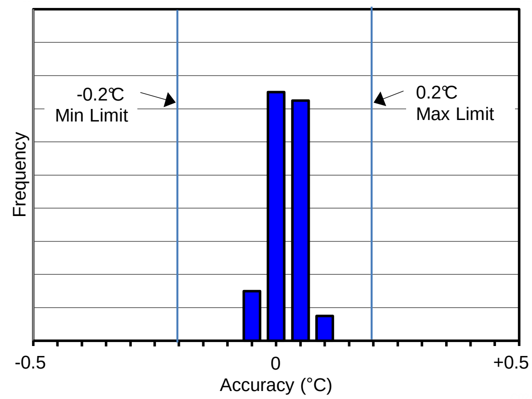
**Figure 4. Accuracy Histogram at -55°C**

## Typical Performance Characteristics (continued)



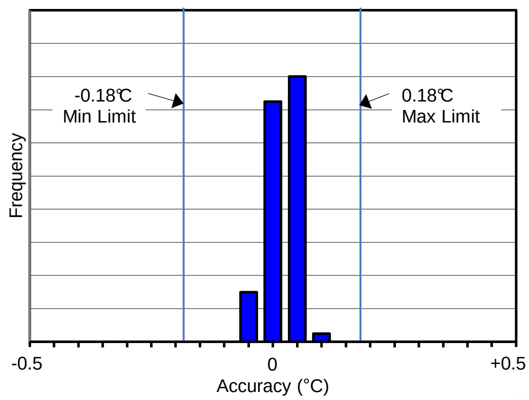

VDD=2.7V
using LUT table for conversion of voltage to temperature

**Figure 5. Accuracy Histogram at -40°C**



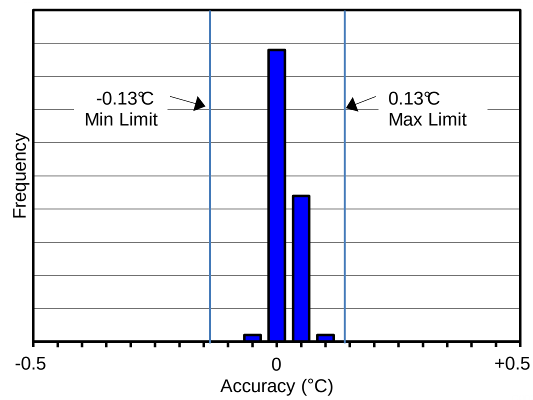

VDD=2.7V
using LUT table for conversion of voltage to temperature

**Figure 6. Accuracy Histogram at –20°C**



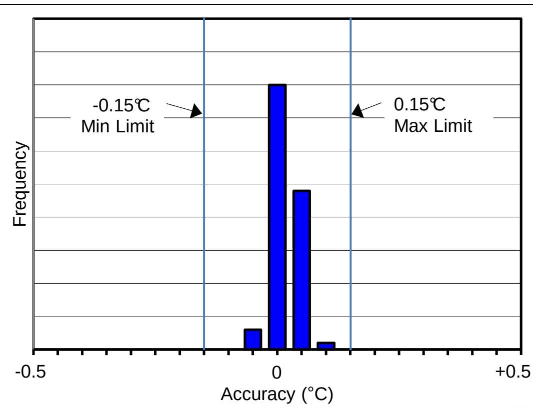

VDD=2.7V
using LUT table for conversion of voltage to temperature

**Figure 7. Accuracy Histogram at -10°C**



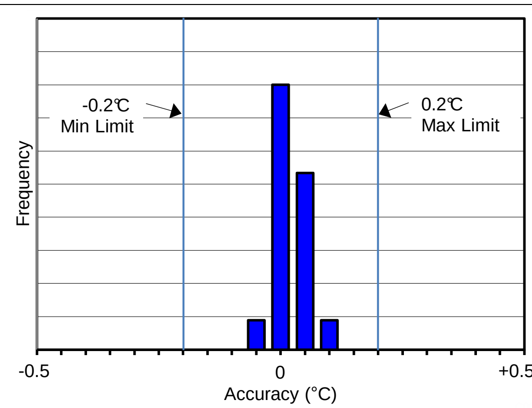

VDD=2.7V
using LUT table for conversion of voltage to temperature

**Figure 8. Accuracy Histogram at 30°C**




VDD=2.7V
using LUT table for conversion of voltage to temperature

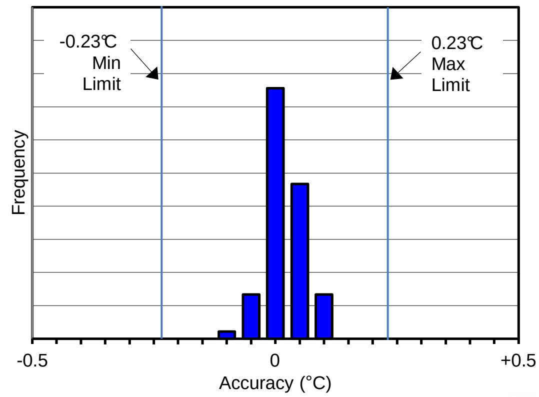
**Figure 9. Accuracy Histogram at 50°C**




VDD=2.7V
using LUT table for conversion of voltage to temperature

**Figure 10. Accuracy Histogram at 90°C**

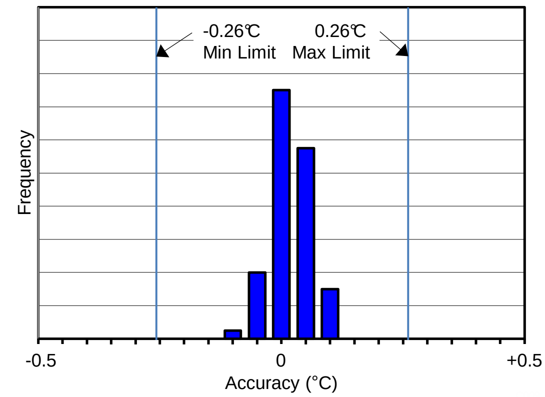
## Typical Performance Characteristics (continued)




VDD=2.7V

using LUT table for conversion of voltage to temperature

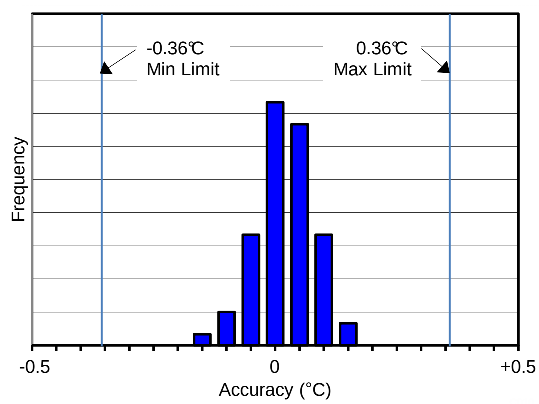
**Figure 11. Accuracy Histogram at 110°C**




VDD=2.7V

using LUT table for conversion of voltage to temperature

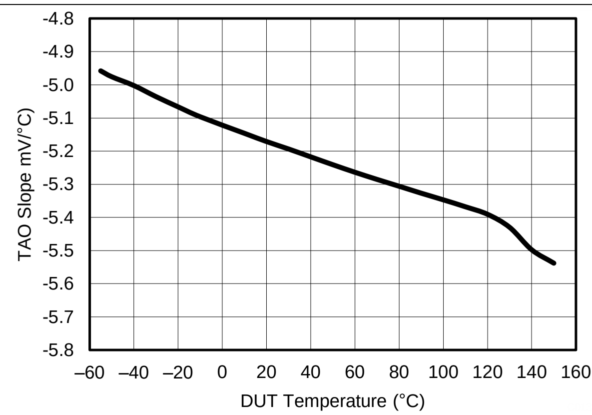
**Figure 12. Accuracy Histogram at 120°C**




VDD=2.7V

using LUT table for conversion of voltage to temperature

**Figure 13. Accuracy Histogram at 150°C**




VDD=2.7V

**Figure 14. TAO first order transfer function slope vs temperature**

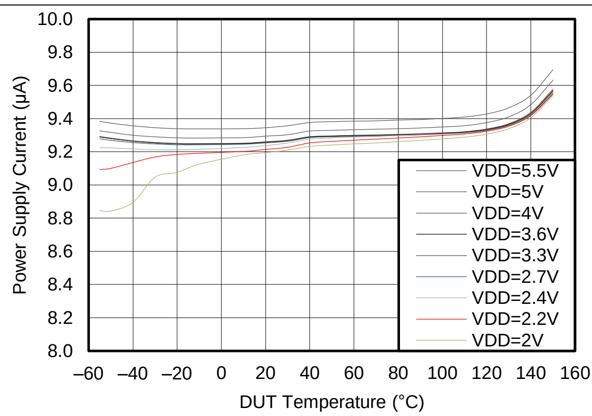
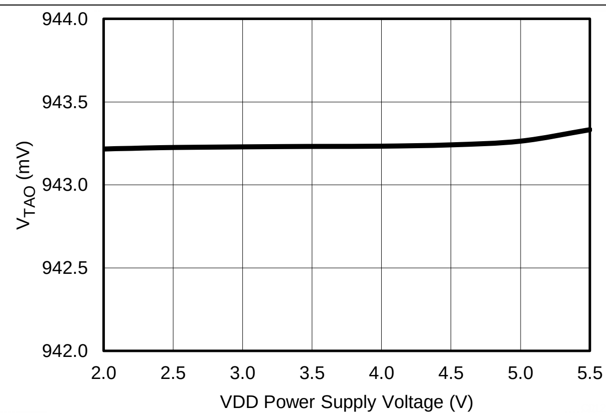


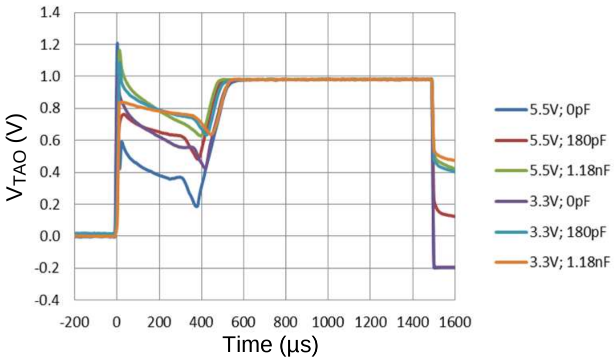

**Figure 15. IDD vs Temperature at Various VDD**




At 30°C

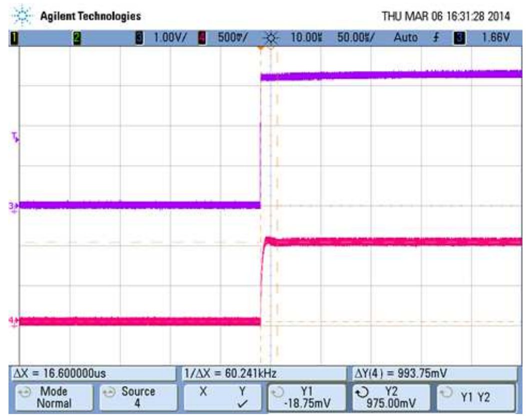
**Figure 16. TAO Line Regulation**

## Typical Performance Characteristics (continued)



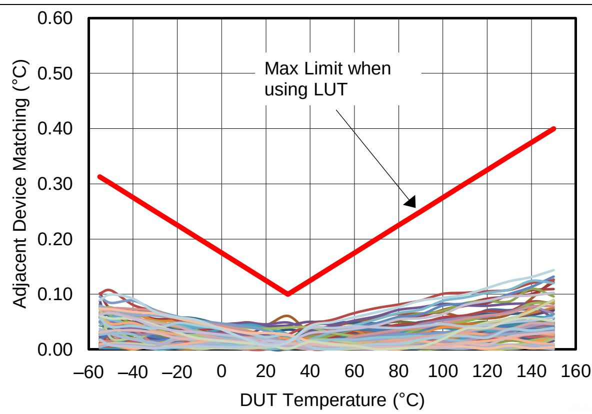

Conditions: Various VDD and $C_{LOAD}$

**Figure 17. Start-up Response**



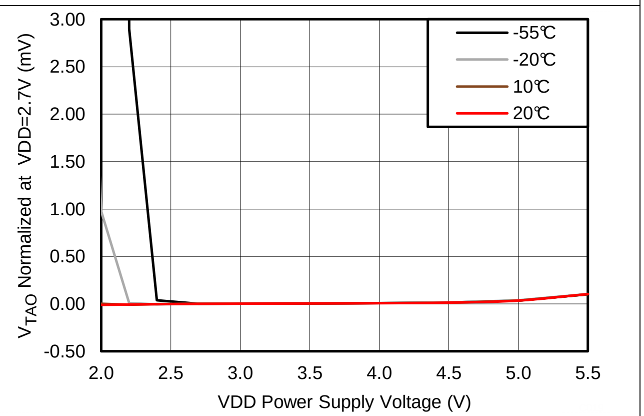

VDD=3.3V
Top trace is T_ON
Bottom trace is TAO

**Figure 18. TAO Response to T_ON**




VDD=2.7V
using LUT table for conversion of voltage to temperature

**Figure 19. LMT70A Matching of Adjacent Units on Tape and Reel**




at various temperatures

**Figure 20. Line Regulation Temperature Variation: $V_{TAO}$ vs Supply Voltage**

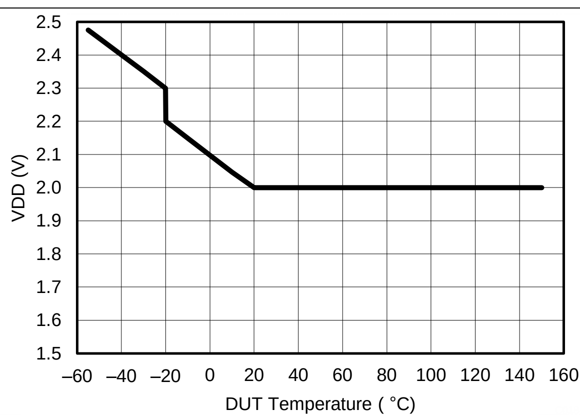



**Figure 21. Minimum Recommended Supply Voltage Temperature Sensitivity**

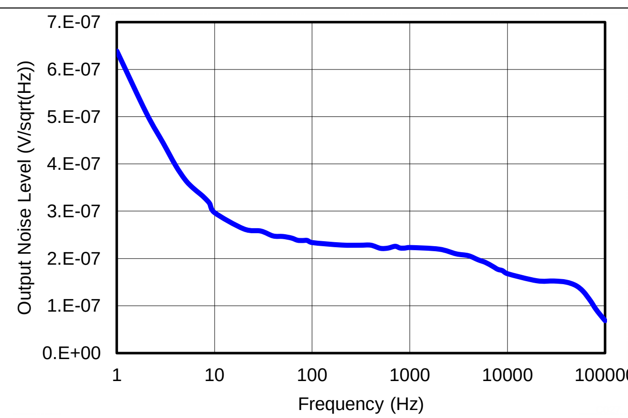



**Figure 22. Output Noise vs Frequency**

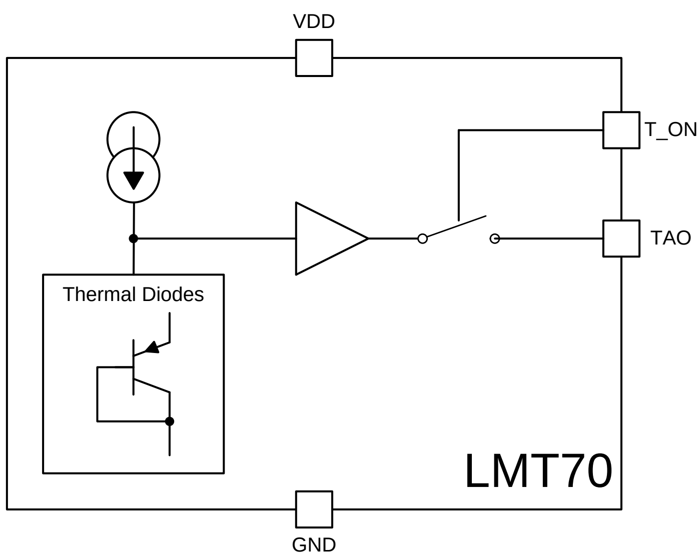
# 9 Detailed Description

## 9.1 Overview

The LMT70 is a precision analog output temperature sensor. It includes an output switch that is controlled by the T_ON digital input. The output switch enables the multiplexing of several devices onto a single ADC input thus expanding on the ADC input multiplexer capability.

The temperature sensing element is comprised of simply stacked BJT base emitter junctions that are biased by a current source. The temperature sensing element is then buffered by a precision amplifier before being connected to the output switch. The output amplifier has a simple class AB push-pull output stage that enables the device to easily source and sink current.

## 9.2 Functional Block Diagram




## 9.3 Feature Description

### 9.3.1 Temperature Analog Output (TAO)

The TAO push-pull output provides the ability to sink and source current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. See the *Typical Application* section for more discussion of this topic. The LMT70 is ideal for this and other applications which require strong source or sink current.

#### *9.3.1.1 LMT70 Output Transfer Function*

The LMT70 output voltage transfer function appears to be linear, but upon close inspection it can be seen that it is truly not linear and can be better described by a second or third order transfer function equation.

## Feature Description (continued)

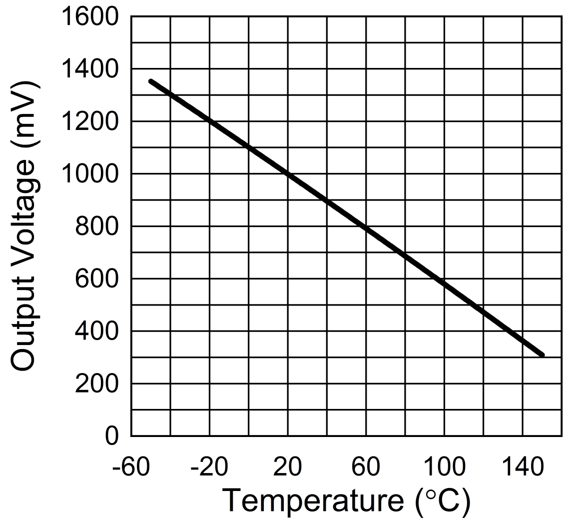



**Figure 23. LMT70 Output Transfer Function**

#### 9.3.1.1.1 First Order Transfer Function

A first order transfer function can be used to calculate the temperature LMT70 is sensing but over a wide temperature range it is the least accurate method. An equation can be easily generated using the LUT (Look-Up Table) information found in *Electrical Characteristics Temperature Lookup Table (LUT)* .

Over a narrow 10°C temperature range a linear equation will yield very accurate results. It is actually recommended that over a 10°C temperature range linear interpolation be used to calculate the temperature the device is sensing. When this method is used the accuracy minimum and maximum specifications would meet the values given in Figure 3.

For example the first order equation between 20°C and 30°C can be generated using the typical output voltage levels as given in *Electrical Characteristics Temperature Lookup Table (LUT)* and partially repeated here for reference from 20°C to 50°C:

## Feature Description (continued)

**Table 1. Output Voltage LUT**

| Temperature (°C) | $V_{TAO}$ (mV) | | | Local Slope (mV/°C) |
|---|---|---|---|---|
| | MIN | TYP | MAX | |
| 20 | 994.367 | 995.050 | 995.734 | -5.171 |
| 30 | 942.547 | 943.227 | 943.907 | -5.194 |
| 40 | 890.423 | 891.178 | 891.934 | -5.217 |
| 50 | 838.097 | 838.882 | 839.668 | -5.241 |

First calculate the slope:

$m = (T1 – T2) \div [(V_{TAO} (T1) – V_{TAO} (T2)]$

$m = (20°C - 30°C) \div (995.050 \text{ mV} – 943.227 \text{ mV})$

$m = –0.193$ °C/mV

Then calculate the y intercept b:

$b = (T1) – (m \times V_{TAO}(T1))$

$b = 20°C – (–0.193 \text{ °C/mV} \times 995.050 \text{ mV})$

$b = 212.009°C$

Thus the final equation used to calculate the measured temperature ($T_M$) in the range between 20°C and 30°C is:

$T_M = m \times V_{TAO} + b$

$T_M = –0.193 \text{ °C/mV} \times V_{TAO} + 212.009°C$

where $V_{TAO}$ is in mV and $T_M$ is in °C.

#### 9.3.1.1.2 Second Order Transfer Function

A second order transfer function can give good results over a wider limited temperature range. Over the full temperature range of -55°C to +150°C a single second order transfer function will have increased error at the temperature extremes. Using least squares sum method a best fit second order transfer function was generated using the values in *Electrical Characteristics Temperature Lookup Table (LUT)*:

$T_M = a (V_{TAO})^2 + b (V_{TAO}) + c$

where:

| | Best fit for -55°C to 150°C | Best fit for -10°C to 110°C |
|---|---|---|
| a | -8.451576E-06 | -7.857923E-06 |
| b | -1.769281E-01 | -1.777501E-01 |
| c | 2.043937E+02 | 2.046398E+02 |

and $V_{TAO}$ is in mV and $T_M$ is in °C.

#### 9.3.1.1.3 Third Order Transfer Function

Over a wide temperature range the most accurate single equation is a third order transfer function. Using least squares sum method a best fit third order transfer function was generated using the values in Figure 3:

$T_M = a\,(V_{TAO})^3 + b\,(V_{TAO})^2 + c(V_{TAO}) + d$

where:

| | Best fit for -55°C to 150°C | Best fit for -10°C to 110°C |
|---|---|---|
| a | -1.064200E-09 | -1.809628E-09 |
| b | -5.759725E-06 | -3.325395E-06 |
| c | -1.789883E-01 | -1.814103E-01 |
| d | 2.048570E+02 | 2.055894E+02 |

and $V_{TAO}$ is in mV and $T_M$ is in °C.

### *9.3.1.2 LMT70A TAO Matching*

In order to meet the matching specification of the LMT70A, two units must be picked from adjacent positions from one tape and reel. If PCB rework is required, involving the LMT70A, then the pair of the LMT70A matched units must be replaced. Matching features (which include, without limitation, electrical matching characteristics of adjacent Components as they are delivered in original packaging from TI) are warranted solely to the extent that the purchaser can demonstrate to TI's satisfaction that the particular Component(s) at issue were adjacent in original packaging as delivered by TI. Customers should be advised that the small size of these components means they are not individually traceable at the unit level and it may be difficult to establish the original position of the Components once they have been removed from that original packaging as delivered by TI.

### *9.3.1.3 TAO Noise Considerations*

A load capacitor on TAO pin can help to filter noise.

For noisy environments, TI recommends at minimum 100 nF supply decoupling capacitor placed close across VDD and GND pins of LMT70.

### *9.3.1.4 TAO Capacitive Loads*

TAO handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the $V_{TAO}$ can drive a capacitive load less than or equal to 1 nF as shown in Figure 24. For capacitive loads greater than 1 nF, a series resistor is required on the output, as shown in Figure 25, to maintain stable conditions.

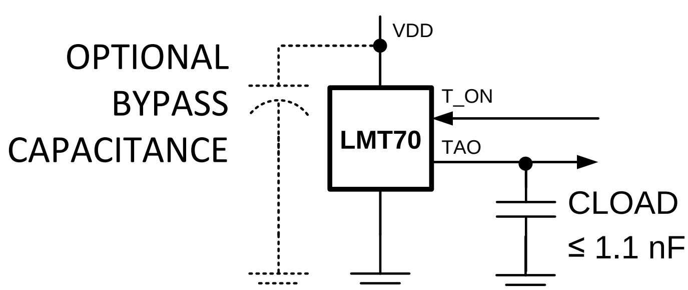



**Figure 24. LMT70 No Isolation Resistor Required**

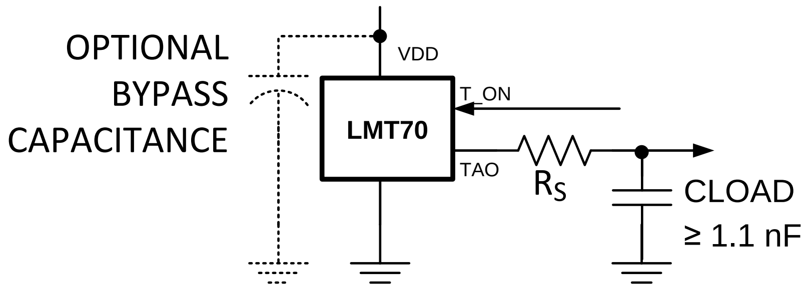



**Figure 25. LMT70 With Series Resistor for Capacitive Loading Greater than 1 nF**

**Table 2. $C_{LOAD}$ and $R_S$ Values of Figure 25**

| $C_{LOAD}$ | Minimum $R_S$ |
|---|---|
| 1.1 to 90 nF | 3 kΩ |
| 90 to 900 nF | 1.5 kΩ |
| 0.9 µF | 750 Ω |

### 9.3.2 $T_{ON}$ Digital Input

The T_ON digital input enables and disables the analog output voltage presented at the TAO pin by controlling the state of the internal switch that is in series with the internal temperature sensor circuitry output. When T_ON is driven to a logic "HIGH" the temperature sensor output voltage is present on the TAO pin. When T_ON is set to a logic "LOW" the TAO pin is set to a high impedance state.

### 9.3.3 Light Sensitivity

Although the LMT70 package has a protective backside coating that reduces the amount of light exposure on the die, unless it is fully shielded, ambient light will still reach the active region of the device from the side of the package. Depending on the amount of light exposure in a given application, an increase in temperature error should be expected. In circuit board tests under ambient light conditions, a typical increase in error may not be observed and is dependent on the angle that the light approaches the package. The LMT70 is most sensitive to IR radiation. Best practice should include end-product packaging that provides shielding from possible light sources during operation.

## 9.4 Device Functional Modes

The LMT70 is a simple precise analog output temperature sensor with a switch in series with its output. It has only two functional modes: output on or output off.

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The LMT70 analog output temperature sensor is an ideal device to connect to an integrated 12-Bit ADC such as that found in the MSP430 microcontroller family.

Applications for the LMT70 included but are not limited to: IoT based temperature sensor nodes, medical fitness equipment (e.g. thermometers, fitness/smart bands or watches, activity monitors, human body temperature monitor), Class AA or lower RTD replacement, precision NTC or PTC thermistor replacement, instrumentation temperature compensation, metering temperature compensation (e. g. heat cost allocator, heat meter).

## 10.2 Typical Application

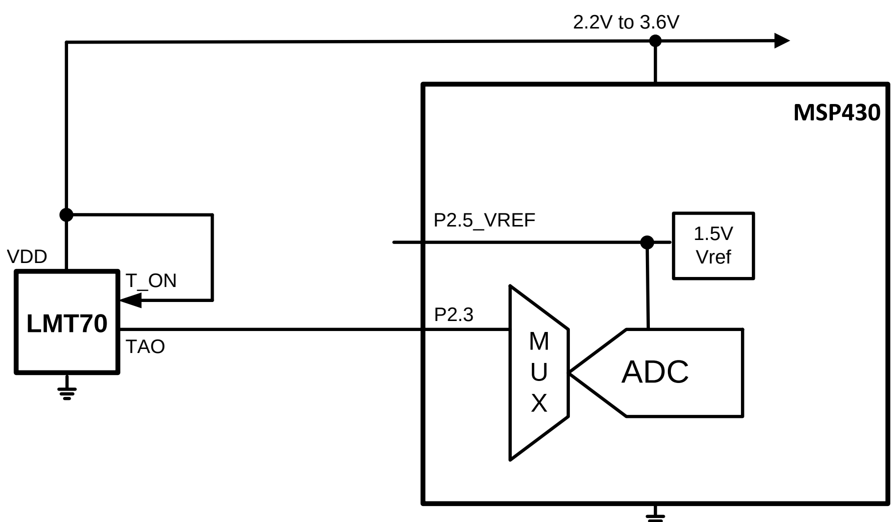



**Figure 26. Typical Application Schematic**

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LMT70 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor ($C_{FILTER}$) or the extension of the ADC acquisition time thus slowing the ADC sampling rate. The size of $C_{FILTER}$ depends on the size of the sampling capacitor and the sampling frequency. Since not all ADCs have identical input stages, the charge requirements will vary. The general ADC application shown in Figure 27 is an example only. The application in Figure 26 was actually tried and the extension of the MSP430 12-Bit ADC acquisition time was all that was necessary in order to accommodate the LMT70's output stage drive capability.

## Typical Application (continued)

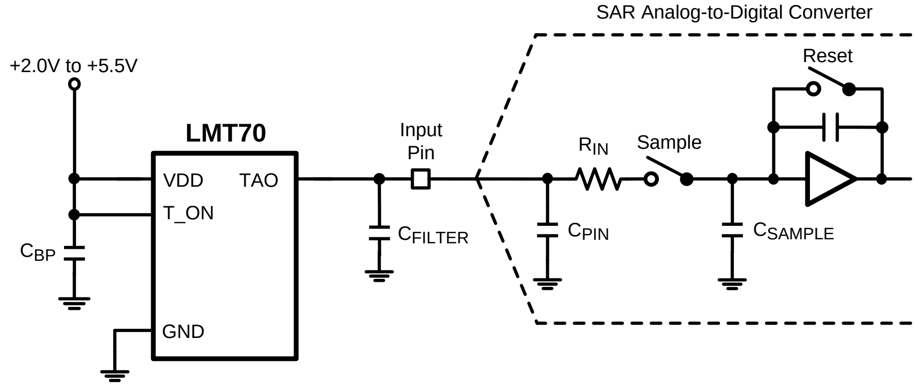



**Figure 27. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage**

### 10.2.1 Design Requirements

The circuit show in Figure 26 will support the design requirements as shown in Table 3.

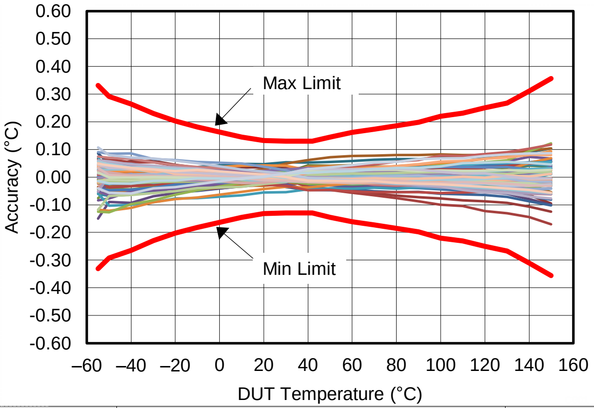
**Table 3. Design Requirements**

| PARAMETER | TARGET SPECIFICATION |
|---|---|
| Temperature Range | -40°C to +150°C LMT70, -40°C to +85°C for MSP430 |
| Accuracy | ±0.2°C typical over full temperature range |
| VDD | 2.2V to 3.6V with typical of 3.0V |
| IDD | 12µA |

### 10.2.2 Detailed Design Procedure

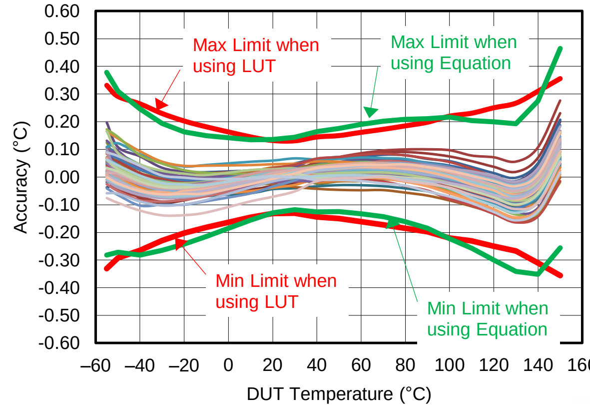
#### *10.2.2.1 Temperature Algorithm Selection*

Of the three algorithms presented in this datasheet, linear interpolation, second order transfer function or third order transfer function, the one selected will be determined by the users microcontroller resources and the temperature range that will be sensed. Therefore, a comparison of the expected accuracy from the LMT70 is given here. The following curves show effect on the accuracy of the LMT70 when using each of the different algorithms/equations given in *LMT70 Output Transfer Function*. The first curve (Figure 28) shows the performance when using linear interpolation of the LUT values shown in *Electrical Characteristics Temperature Lookup Table (LUT)* of every 10°C and provides the best performance. Linear interpolation of the LUT values shown in *Electrical Characteristics Temperature Lookup Table (LUT)* is used to determine the LMT70 min/max accuracy limits as shown in the *Electrical Characteristics* and the red lines of Figure 28. The other lines in the middle of Figure 28 show independent device performance. The green limit lines, shown in the subsequent figures, apply for the specific equation used to convert the output voltage of the LMT70 to temperature. The equations are shown under each figure for reference purposes. The green lines show the min/max limits when set in a similar manner to the red limit lines of *Figure 28*. The limits shown in red for Figure 28 are repeated in all the figures of this section for comparison purposes.



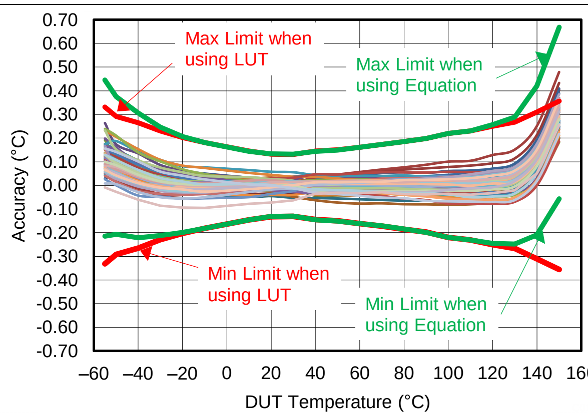

| Temp (°C) | $V_{TAO}$ (mV) MIN | TYP | MAX | Local Slope (mV/°C) |
|---|---|---|---|---|
| 20 | 994.367 | 995.050 | 995.734 | -5.171 |
| 30 | 942.547 | 943.227 | 943.907 | -5.194 |
| 40 | 890.423 | 891.178 | 891.934 | -5.217 |
| 50 | 838.097 | 838.882 | 839.668 | -5.241 |

**Figure 28. LMT70 Performance Using LUT and Linear Interpolation**



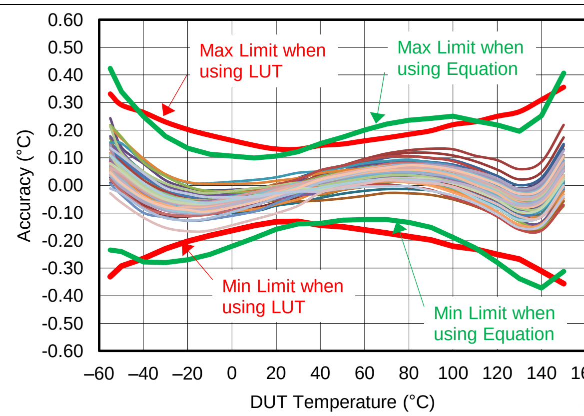

$T_M$ = -1.064200E-09 $(V_{TAO})^3$ – 5.759725E-06 $(V_{TAO})^2$ – 1.789883E-01$(V_{TAO})$ + 2.048570E+02

**Figure 29. Using Third Order Transfer Function Best Fit - 55°C to +150°C**



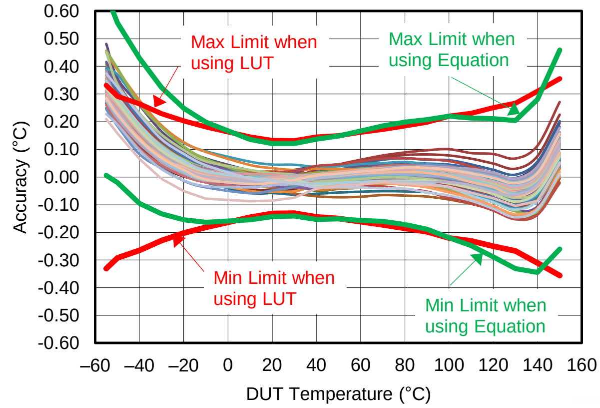

$T_M$ = -1.809628E-09 $(V_{TAO})^3$ – 3.325395E-06 $(V_{TAO})^2$ – 1.814103E-01$(V_{TAO})$ + 2.055894E+02

**Figure 30. Using Third Order Transfer Function Best Fit - 10°C to +110°C**




$T_M$ = -8.451576E-06 $(V_{TAO})^2$– 1.769281E-01 $(V_{TAO})$ + 2.043937E+02

**Figure 31. Using Second Order Transfer Function Best Fit -55°C to 150°C**




$T_M$ = -7.857923E-06 $(V_{TAO})^2$ – 1.777501E-01 $(V_{TAO})$ + 2.046398E+02

**Figure 32. Using Second Order Transfer Function Best Fit -10°C to 110°C**

### *10.2.2.2 ADC Requirements*

The ADC resolution and its specifications as well as reference voltage and its specifications will determine the overall system accuracy that you can obtain. For this example the 12-bit SAR ADC found in the MSP430 was used as well as it's integrated reference. At first glance the specifications may not seem to be precise enough to actually be used with the LMT70 but the MSP430 ADC and integrated reference errors are actually measured during production testing of the MSP430. Values are then provided to user for software calibration. These calibration values are located in the MSP430A device descriptor tag-length-value (TLV) structure and found in the device-specific datasheet. The MSP430 Users Guide includes information on how to use these calibration values to calibrate the ADC reading. The specific values used to calibrate the ADC readings are: CAL_ADC_15VREF_FACTOR, CAL_ADC_GAIN_FACTOR and CAL_ADC_OFFSET.

### 10.2.3 Finer Resolution LUT

The following table is given for reference only and not meant to be used for calculation purposes.

| Temp (°C) | $V_{TAO}$ (mV) | Temp (°C) | $V_{TAO}$ (mV) | Temp (°C) | $V_{TAO}$ (mV) | Temp (°C) | $V_{TAO}$ (mV) | Temp (°C) | $V_{TAO}$ (mV) | Temp (°C) | $V_{TAO}$ (mV) | Temp (°C) | $V_{TAO}$ (mV) | Temp (°C) | $V_{TAO}$ (mV) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TYP | | TYP | | TYP | | TYP | | TYP | | TYP | | TYP | | TYP |
| | | -30 | 1250.398 | 0 | 1097.987 | 30 | 943.227 | 60 | 786.360 | 90 | 627.490 | 120 | 466.760 | 150 | 302.785 |
| | | -29 | 1244.953 | 1 | 1092.532 | 31 | 937.729 | 61 | 780.807 | 91 | 621.896 | 121 | 460.936 | | |
| | | -28 | 1239.970 | 2 | 1087.453 | 32 | 932.576 | 62 | 775.580 | 92 | 616.603 | 122 | 455.612 | | |
| | | -27 | 1234.981 | 3 | 1082.370 | 33 | 927.418 | 63 | 770.348 | 93 | 611.306 | 123 | 450.280 | | |
| | | -26 | 1229.986 | 4 | 1077.282 | 34 | 922.255 | 64 | 765.113 | 94 | 606.006 | 124 | 444.941 | | |
| -55 | 1375.219 | -25 | 1224.984 | 5 | 1072.189 | 35 | 917.087 | 65 | 759.873 | 95 | 600.701 | 125 | 439.593 | | |
| -54 | 1370.215 | -24 | 1219.977 | 6 | 1067.090 | 36 | 911.915 | 66 | 754.628 | 96 | 595.392 | 126 | 434.238 | | |
| -53 | 1365.283 | -23 | 1214.963 | 7 | 1061.987 | 37 | 906.738 | 67 | 749.380 | 97 | 590.079 | 127 | 428.875 | | |
| -52 | 1360.342 | -22 | 1209.943 | 8 | 1056.879 | 38 | 901.556 | 68 | 744.127 | 98 | 584.762 | 128 | 423.504 | | |
| -51 | 1355.395 | -21 | 1204.916 | 9 | 1051.765 | 39 | 896.370 | 69 | 738.870 | 99 | 579.442 | 129 | 418.125 | | |
| -50 | 1350.441 | -20 | 1199.884 | 10 | 1046.647 | 40 | 891.178 | 70 | 733.608 | 100 | 574.117 | 130 | 412.739 | | |
| -49 | 1345.159 | -19 | 1194.425 | 11 | 1041.166 | 41 | 885.645 | 71 | 728.055 | 101 | 568.504 | 131 | 406.483 | | |
| -48 | 1340.229 | -18 | 1189.410 | 12 | 1036.062 | 42 | 880.468 | 72 | 722.804 | 102 | 563.192 | 132 | 401.169 | | |
| -47 | 1335.293 | -17 | 1184.388 | 13 | 1030.952 | 43 | 875.287 | 73 | 717.550 | 103 | 557.877 | 133 | 395.841 | | |
| -46 | 1330.352 | -16 | 1179.361 | 14 | 1025.838 | 44 | 870.100 | 74 | 712.292 | 104 | 552.557 | 134 | 390.499 | | |
| -45 | 1325.405 | -15 | 1174.327 | 15 | 1020.720 | 45 | 864.909 | 75 | 707.029 | 105 | 547.233 | 135 | 385.144 | | |
| -44 | 1320.453 | -14 | 1169.288 | 16 | 1015.596 | 46 | 859.713 | 76 | 701.762 | 106 | 541.905 | 136 | 379.775 | | |
| -43 | 1315.496 | -13 | 1164.242 | 17 | 1010.467 | 47 | 854.513 | 77 | 696.491 | 107 | 536.573 | 137 | 374.393 | | |
| -42 | 1310.534 | -12 | 1159.191 | 18 | 1005.333 | 48 | 849.307 | 78 | 691.217 | 108 | 531.236 | 138 | 368.997 | | |
| -41 | 1305.566 | -11 | 1154.134 | 19 | 1000.194 | 49 | 844.097 | 79 | 685.937 | 109 | 525.895 | 139 | 363.587 | | |
| -40 | 1300.593 | -10 | 1149.070 | 20 | 995.050 | 50 | 838.882 | 80 | 680.654 | 110 | 520.551 | 140 | 358.164 | | |
| -39 | 1295.147 | -9 | 1143.654 | 21 | 989.583 | 51 | 833.343 | 81 | 675.073 | 111 | 514.886 | 141 | 351.937 | | |
| -38 | 1290.202 | -8 | 1138.599 | 22 | 984.450 | 52 | 828.141 | 82 | 669.803 | 112 | 509.557 | 142 | 346.508 | | |
| -37 | 1285.250 | -7 | 1133.540 | 23 | 979.313 | 53 | 822.934 | 83 | 664.528 | 113 | 504.223 | 143 | 341.071 | | |
| -36 | 1280.291 | -6 | 1128.476 | 24 | 974.171 | 54 | 817.723 | 84 | 659.250 | 114 | 498.885 | 144 | 335.625 | | |
| -35 | 1275.326 | -5 | 1123.407 | 25 | 969.025 | 55 | 812.507 | 85 | 653.967 | 115 | 493.542 | 145 | 330.172 | | |
| -34 | 1270.353 | -4 | 1118.333 | 26 | 963.875 | 56 | 807.287 | 86 | 648.680 | 116 | 488.195 | 146 | 324.711 | | |
| -33 | 1265.375 | -3 | 1113.254 | 27 | 958.720 | 57 | 802.062 | 87 | 643.389 | 117 | 482.843 | 147 | 319.241 | | |
| -32 | 1260.389 | -2 | 1108.170 | 28 | 953.560 | 58 | 796.832 | 88 | 638.094 | 118 | 477.486 | 148 | 313.764 | | |
| -31 | 1255.397 | -1 | 1103.081 | 29 | 948.396 | 59 | 791.598 | 89 | 632.794 | 119 | 472.125 | 149 | 308.279 | | |

### 10.2.4 Application Curves

The LMT70 performance using the MSP430 with integrated 12-bit ADC is shown in Figure 33. This curve includes the error of the MSP430 integrated 12-bit ADC and reference as shown in the schematic Figure 26. The MSP430 was kept at room temperature and the LMT70 was submerged in a precision temperature calibration oil bath. A calibrated temperature probe was used to monitor the temperature of the oil. As can be seen in Figure 33 the combined performance on the MSP430 and the LMT70 is better than 0.12°C for the entire -40°C to +150°C temperature range. The only calibration performed was with software using the MSP430A device descriptor tag-length-value (TLV) calibration values for ADC and VREF error.

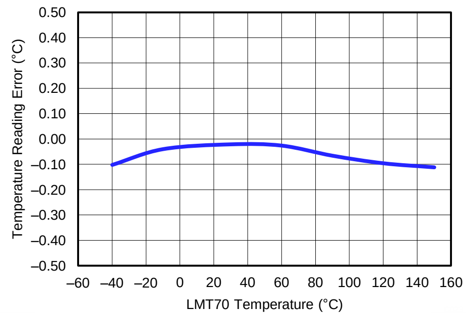



**Figure 33. LMT70 with MSP430 typical performance**

## 10.3 System Examples

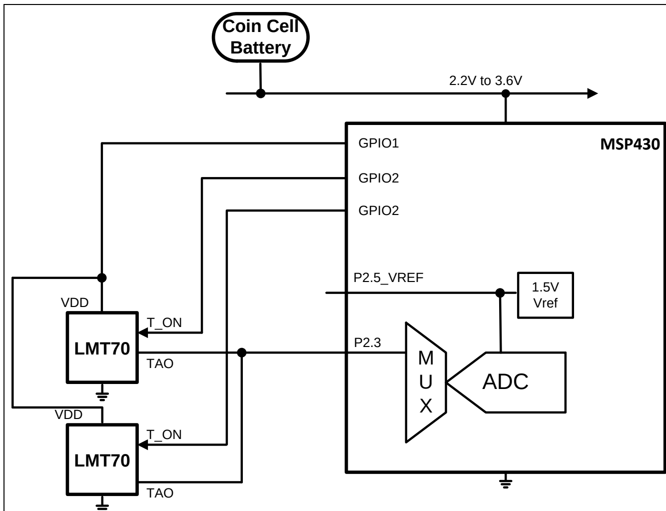



**Figure 34. Multiple LMT70s connected to one 12-bit ADC channel on an MSP430**

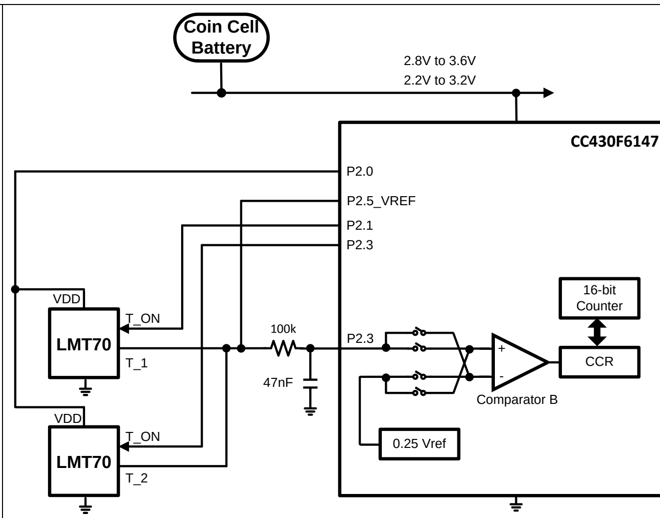



**Figure 35. Multiple LMT70s connected to a slope ADC for high resolution**

# 11 Power Supply Recommendations

Power supply bypass capacitors are optional and may be required if the supply line is noisy. It is recommended that a local supply decoupling capacitor be used to reduce noise. For noisy environments, TI recommends a 100 nF supply decoupling capacitor placed closed across VDD and GND pins of LMT70.

# 12 Layout

## 12.1 Layout Guidelines

The LMT70 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface. The temperatures of the lands and traces to the other leads of the LMT70 will also affect the temperature reading.

### 12.1.1 Mounting and Temperature Conductivity

Alternatively, the LMT70 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LMT70 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the TAO output to ground or VDD, the TAO output from the LMT70 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The LMT70's junction temperature is the actual temperature being measured. The thermal resistance junction-to-ambient ($R_{\theta JA}$) is the parameter (from *Thermal Information*) used to calculate the rise of a device junction temperature due to its power dissipation. Equation 1 is used to calculate the rise in the LMT70's die temperature.

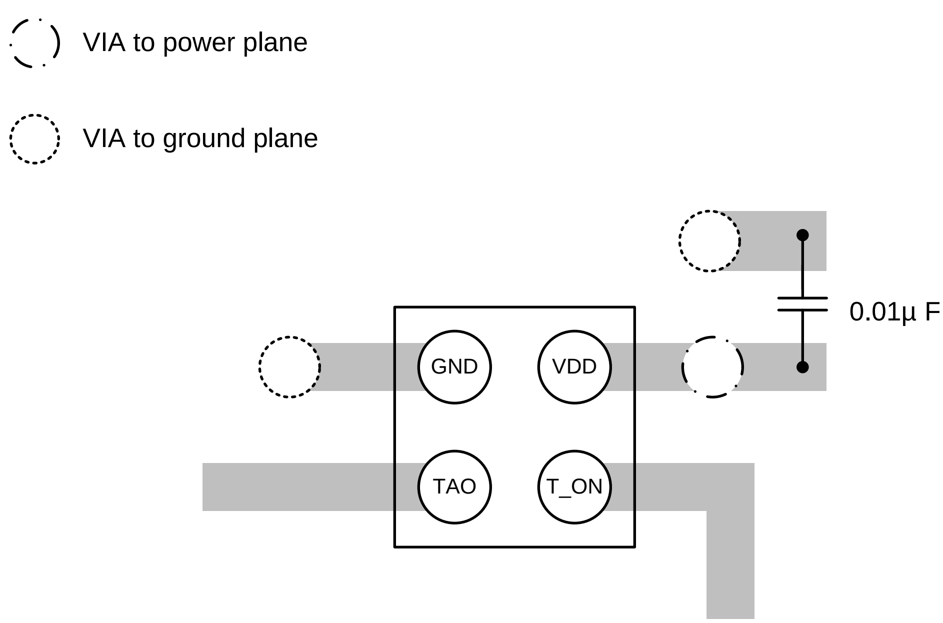
$$T_J = T_A + R_{\theta JA}\left[(V_{DD} I_Q) + (V_{DD} - V_{TEMP})\ I_L\right]$$

where

- $T_A$ is the ambient temperature.
- $I_Q$ is the quiescent current.
- $I_L$ is the load current on $V_{TEMP}$. (1)

For example, in an application where $T_A$ = 30°C, VDD = 3 V, IDD = 12µA, $V_{TAO}$ = 943.227 mV, and $I_L$ = 0 µA, the total temperature rise would be [187°C/W × 3 V × 12 µA] = 0.007°C. To minimize self-heating, the load current on TAO pin should be minimized.

## 12.2 Layout Example



# 13 Device and Documentation Support

## 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| LMT70 | Click here | Click here | Click here | Click here | Click here |
| LMT70A | Click here | Click here | Click here | Click here | Click here |

## 13.2 Documentation Support

### 13.2.1 Related Documentation

*Reflow Temperature Profile* specifications. Refer to www.ti.com/packaging.

*IC Package Thermal Metrics* application report, SPRA953

## 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMT70AYFQR | ACTIVE | DSBGA | YFQ | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -55 to 150 | | Samples |
| LMT70AYFQT | OBSOLETE | DSBGA | YFQ | 4 | | TBD | Call TI | Call TI | -55 to 150 | | |
| LMT70YFQR | ACTIVE | DSBGA | YFQ | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -55 to 150 | | Samples |
| LMT70YFQT | OBSOLETE | DSBGA | YFQ | 4 | | TBD | Call TI | Call TI | -55 to 150 | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

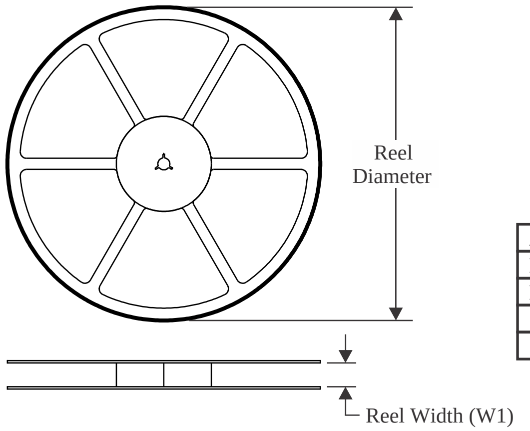
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

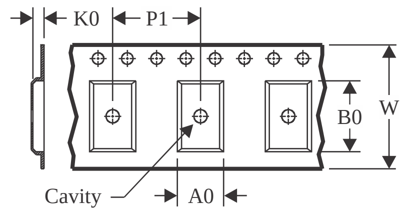
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

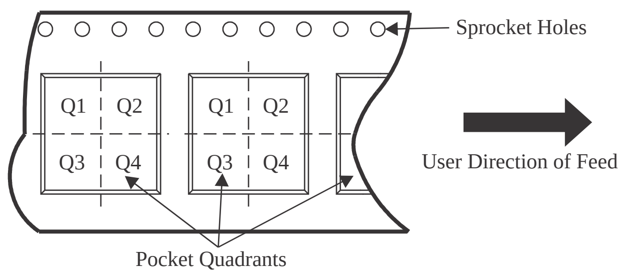



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

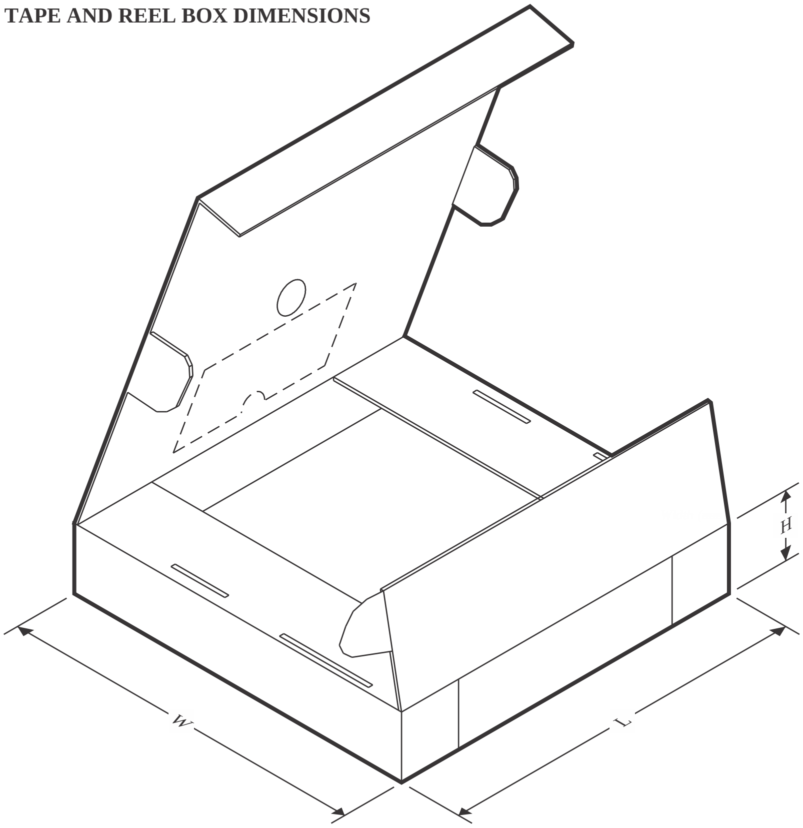
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMT70AYFQR | DSBGA | YFQ | 4 | 3000 | 178.0 | 8.4 | 0.94 | 0.94 | 0.71 | 4.0 | 8.0 | Q1 |
| LMT70YFQR | DSBGA | YFQ | 4 | 3000 | 178.0 | 8.4 | 0.94 | 0.94 | 0.71 | 4.0 | 8.0 | Q1 |

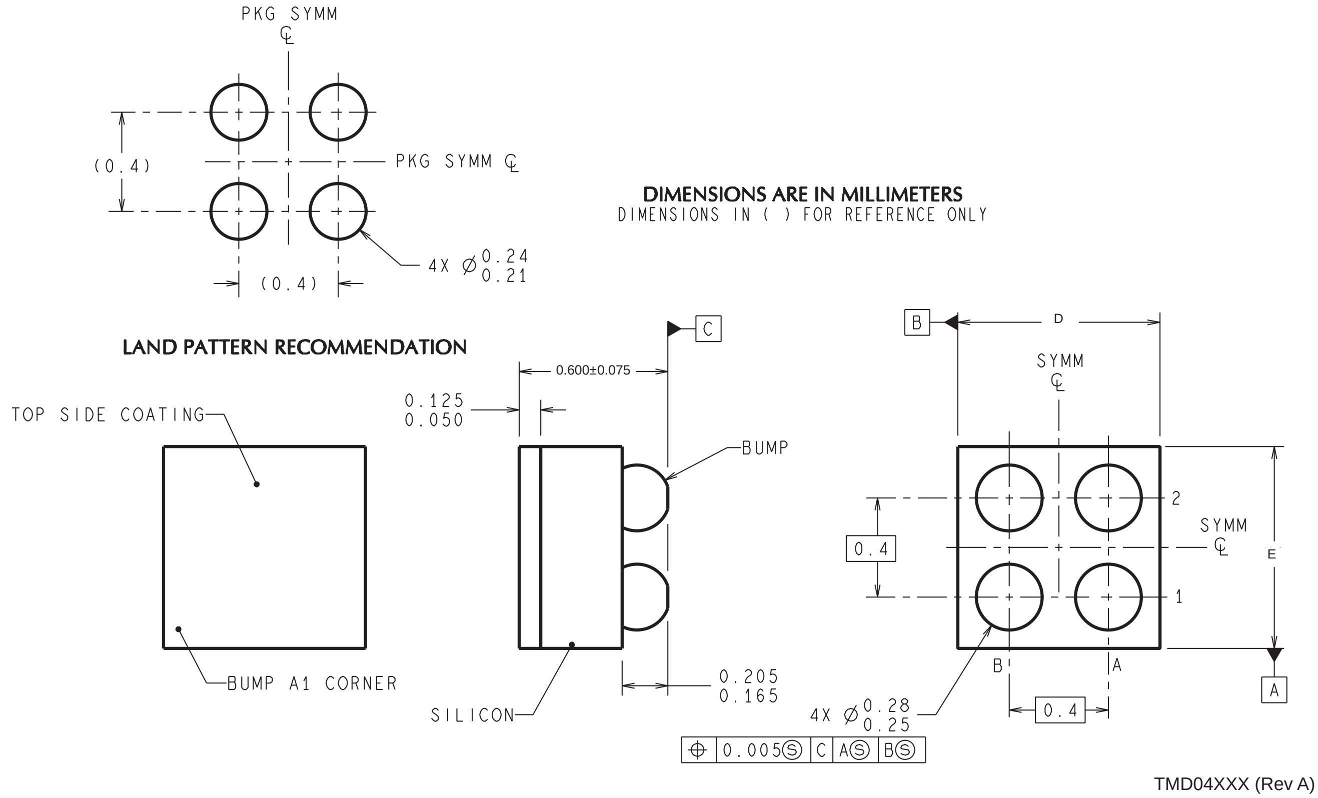
## TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMT70AYFQR | DSBGA | YFQ | 4 | 3000 | 208.0 | 191.0 | 35.0 |
| LMT70YFQR | DSBGA | YFQ | 4 | 3000 | 208.0 | 191.0 | 35.0 |

# YFQ0004




D: Max = 0.914 mm, Min =0.854 mm

E: Max = 0.914 mm, Min =0.854 mm

4215073/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265