LSF0002 Ultra-Small Auto-Bidirectional Translator for Open Drain or Push Pull Applications

1 Features

- Provides bidirectional voltage translation with no direction pin
- Supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pF capacitive load and up To 40MHz up or down translation at 50pF capacitive load
- Allows bidirectional voltage-level translation between
  - 0.95V ↔ 1.8/2.5/3.3/5V
  - 1.2V ↔ 1.8/2.5/3.3/5V
  - 1.8V ↔ 2.5/3.3/5V
  - 2.5V ↔ 3.3/5V
  - 3.3V ↔ 5V
- Low standby current
- 5V tolerance I/O port to support TTL
- Low R_{ON} provides less signal distortion
- High-impedance I/O pins for EN = Low
- Flow-through pinout for easy PCB trace routing
- Latch-up performance >100mA per JESD 17
- –40°C to 125°C operating temperature range

2 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I²C, and other interfaces in telecom infrastructure
- Enterprise systems
- Communications equipment
- Personal electronics
- Industrial applications

3 Description

The LSF0002 supports bidirectional voltage translation without the need for DIR pin, which minimizes system effort (for PMBus, I²C, SMBus, and so forth). The LSF family of devices supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pF capacitive load and up to 40MHz up or down translation at 50pF capacitive load, which allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO).

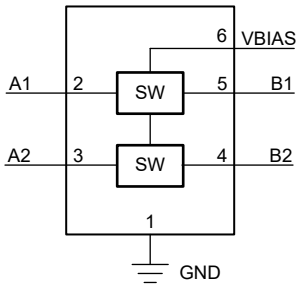
LSF family supports 5V tolerance on I/O port, which makes it compatible with TTL levels in industrial and telecom applications. The LSF family can set up different voltage translation levels, which makes it very flexible.

Unlike the LSF0x0x family, the LSF0002 does not require VREF_A and VREF_B power supplies and the 200kΩ bias resistor. The LSF0002 utilizes the V_{BIAS} pin that enables translation by being biased to the same voltage as the lower power supply at the I/Os that is being translated to and from.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LSF0002	DTQ (X2SON, 6)	1mm × 0.8mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

Table of Contents

4 Pin Configuration and Functions

Pinout drawings are not to scale

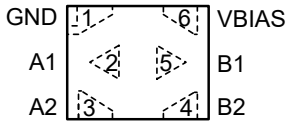


Figure 4-1. LSF0002 DTQ Package, 6-Pin X2SON (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A1	2	I/O	Auto-Bidirectional Data port
A2	3	I/O	
B1	5	I/O	
B2	4	I/O	
VBIAS	6	I	Enable input/ Supply Voltage
GND	1	—	Ground

(1) I= input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage(2)		–0.5	7	V
$V_{I/O}$	Input/output voltage(2)		–0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and input/output voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(3)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-001	±1000	V
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
V_{BIAS}	Reference Voltage		0	5.5	V
$V_{I/O}$	Input/Output voltage	A1, A2, B1, B2	0	5.5	V
I_{PASS}	Pass switch current			64	mA
T_A	Operating free-air temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		LSF0002 DTQ (X2SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	294.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	188.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	216.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	216.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	I_I = -18mA	EN = 0V				-1.2	V
I_{IH}	V_I = 5V	EN = 0V				5.0	µA
I_{CCBA}	$V_{ref\_B} = V_{EN}$ = 5.5V, V_{ref_A} = 4.5V, I_O = 0, $V_I = V_{CC}$ or GND				1		µA
$C_{I(ref\_A/B/EN)}$	V_I = 3V or 0				11		pF
$C_{io(off)}$	V_O = 3V or 0,	V_{EN} = 0V			4.0	6.0	pF
$C_{io(on)}$	V_O = 3V or 0,	V_{EN} = 3V			10.5	12.5	pF
r_{ON} (2)	V_I = 0,	I_O = 64mA	V_{ref_A} = 3.3V; $V_{ref\_B} = V_{EN}$ = 5V		8.0		Ω
			V_{ref_A} = 1.8V; $V_{ref\_B} = V_{EN}$ = 5V		9.0		
			V_{ref_A} = 1.0V; $V_{ref\_B} = V_{EN}$ = 5V		10		
	V_I = 0,	I_O = 32mA	V_{ref_A} = 1.8V; $V_{ref\_B} = V_{EN}$ = 5V		10		Ω
			V_{ref_A} = 2.5V; $V_{ref\_B} = V_{EN}$ = 5V		15		
	V_I = 1.8V,	I_O = 15mA	V_{ref_A} = 3.3V; $V_{ref\_B} = V_{EN}$ = 5V		9.0		Ω
	V_I = 1.0V,	I_O = 10mA	V_{ref_A} = 1.8V; $V_{ref\_B} = V_{EN}$ = 3.3V		18		Ω
	V_I = 0V,	I_O = 10mA	V_{ref_A} = 1.0V; $V_{ref\_B} = V_{EN}$ = 3.3V		20		Ω
	V_I = 0V,	I_O = 10mA	V_{ref_A} = 1.0V; $V_{ref\_B} = V_{EN}$ = 1.8V		30		Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two (A or B) pins.

5.6 Switching Characteristics (Translating Down): B_N = 3.3V

over recommended operating free-air temperature range, B_N = 3.3V, B_N = VIH = A_N + 1, VIL = 0, and VM = 0.5A_N (unless otherwise noted) (see *Parameter Measurement Information*)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	From (input) A or B to (output) B or A	C_L = 15pF		0.3		ns
			C_L = 30pF		0.7		
			C_L = 50pF		1.1		
T_{PHL}	High to low propagation delay		C_L = 15pF		0.4		ns
			C_L = 30pF		0.8		
			C_L = 50pF		1.2		

5.7 Switching Characteristics (Translating Down): B_N = 2.5V

over recommended operating free-air temperature range, B_N = 2.5V, B_N = VIH = A_N + 1, VIL = 0, and VM = 0.5A_N (unless otherwise noted) (see *Parameter Measurement Information*)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	From (input) A or B to (output) B or A	C_L = 15pF		0.35		ns
			C_L = 30pF		0.8		
			C_L = 50pF		1.2		
T_{PHL}	High to low propagation delay		C_L = 15pF		0.5		ns
			C_L = 30pF		1		
			C_L = 50pF		1.3		

5.8 Switching Characteristics (Translating Up): B_N = 3.3V

over recommended operating free-air temperature range, B_N = 3.3V, B_N = VT = A_N + 1, Vref_A = VIH, VIL = 0, VM = 0.5A_N and RL = 300 (unless otherwise noted) (see *Parameter Measurement Information*)

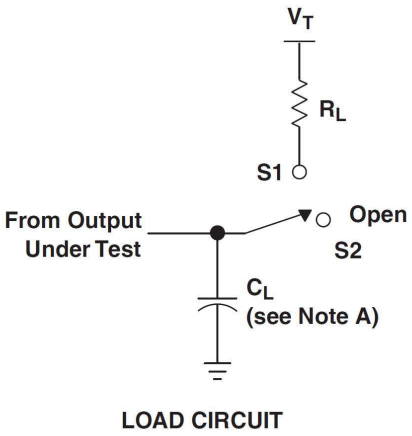
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	From (input) A or B to (output) B or A	C_L = 15pF		0.4		ns
			C_L = 30pF		0.8		
			C_L = 50pF		1		
T_{PHL}	High to low propagation delay		C_L = 15pF		0.4		ns
			C_L = 30pF		0.9		
			C_L = 50pF		1		

5.9 Switching Characteristics (Translating Up):B_N = 2.5V

over recommended operating free-air temperature range, B_N = 2.5V, B_N = VT = A_N + 1, A_N = VIH, VIL = 0, VM = 0.5A_N and RL = 300 (unless otherwise noted) (see *Parameter Measurement Information*)

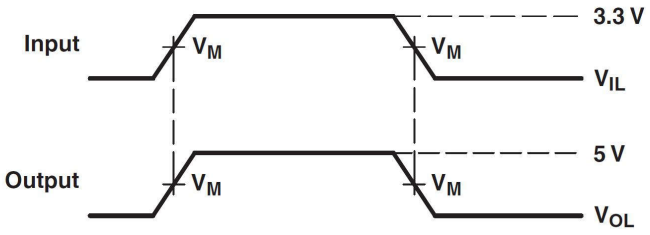
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	From (input) A or B to (output) B or A	C_L = 15pF		0.45		ns
			C_L = 30pF		0.9		
			C_L = 50pF		1.1		
T_{PHL}	High to low propagation delay		C_L = 15pF		0.6		ns
			C_L = 30pF		1.1		
			C_L = 50pF		1.3		

6 Parameter Measurement Information

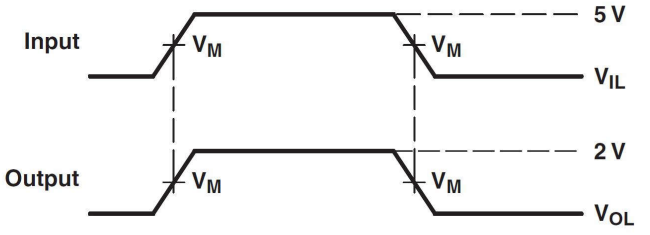


LOAD CIRCUIT

USAGE	SWITCH
Translating up	S1
Translating down	S2



TRANSLATING UP



TRANSLATING DOWN

A. C_L includes probe and jig capacitance.
B. Generators that have the following characteristics generate all input pulses: PRR ≤ 10MHs, Z_O = 50Ω, t_r ≤ 2ns, t_f ≤ 2ns.
C. The outputs are measured one at a time, with one transition per measurement.

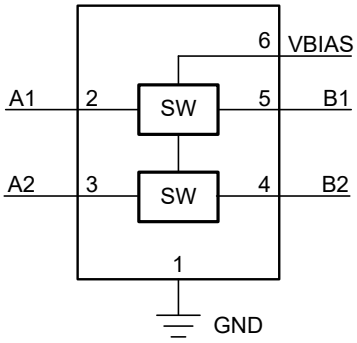
Figure 6-1. Load Circuit for Outputs

7 Detailed Description

7.1 Overview

The LSF0002 can be used in level-translation applications for interfacing devices or systems operating with one another that operate at different interface voltages. The LSF family is an excellent choice for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pull-up resistors and layout, LSF can achieve 100MHz. The LSF family can also be used in applications where a push-pull driver is connected to the data I/Os. For an overview of device setup and operation, see *The Logic Minute* training series on *Understanding the LSF Family of Bidirectional, Multi-Voltage Level Translators*.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Auto Bidirectional Voltage Translation

The LSF family is an auto bidirectional voltage level translator that is operational from 0.95 to 5.5V. This allows for bidirectional voltage translation between 0.95V and 5.5V without the need for a direction pin in open-drain or push-pull applications. The LSF family supports level translation applications with transmission speeds greater than 100Mbps for open-drain systems using a 30pF capacitance and 250Ω pullup resistor. Both the output driver of the controller and the peripheral device output can be push-pull or open-drain (pull-up resistors may be required). In both up and down translation, the B-side is often referred to as the high side and refers to devices connected to the B ports. The A-side can be referred to as the low side.

7.3.2 V_{BIAS}/ Enable

To enable the I/O pins, the V_{BIAS} input should be referenced towards the lower power supply (in the following example, $V_{EXT,A}$) during voltage translation. To be in the high impedance state during power-up, power-down, or during operation, the V_{BIAS} pin must be pulled low and at GND or disabled by an open-drain driver without a pullup resistor. Use the V_{BIAS} pin to properly bias the I/O channels. A filter capacitor on V_{BIAS} is also recommended for a stable supply at the device.

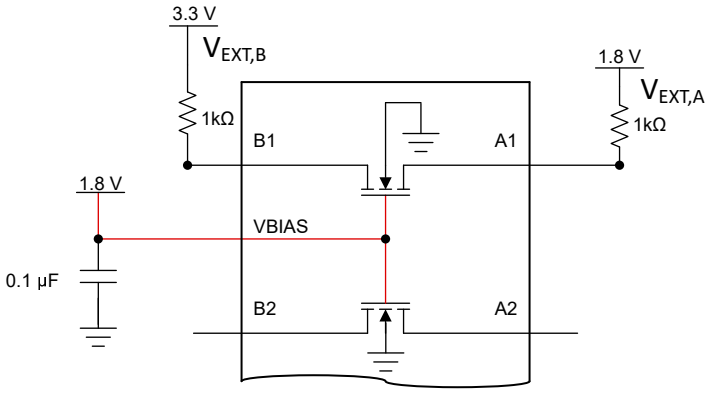


Figure 7-1. V_{BIAS} Tied to Lower Power Supply

The supply voltage of open drain I/O devices can be completely different from the supplies used for the LSF and has no impact on the operation. For additional details on how to use the enable pin, see the *Using the Enable Pin with the LSF Family video.*

Table 7-1. Enable Pin Function Table

INPUT V_{BIAS}PIN	Data Port State
Tied directly to V_{BIAS}	An = Bn
L	Hi-Z

7.4 Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low R_{ON} of the switch allows connections to be made with minimal propagation delay and signal distortion.

Table 7-1 provides a summary of device operation. For additional details on the functional operation of the LSF family of devices, see the *Down Translation with the LSF Family* and *Up Translation with the LSF Family* videos.

Table 7-2. Device Functionality

Signal Direction(1)	Input State	Switch State	Functionality
B to A (Down Translation)	B = LOW	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage
	B = HIGH	OFF (High Impedance)	A-side voltage is clamped at $V_{EXT,A}$ (2)
A to B (Up Translation)	A = LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A = HIGH	OFF (High Impedance)	B-side voltage is clamped at $V_{EXT,A}$ and then pulled up to the $V_{EXT,B}$ supply voltage

(1) The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.
(2) The A-side can have a pullup to $V_{EXT,A}$ for additional current drive capability or may also be pulled above $V_{EXT,A}$ with a pullup resistor. Specifications in the *Recommended Operating Conditions* section should always be followed.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LSF devices can perform voltage translation for open-drain or push-pull interfaces. Table 8-1 provides common interfaces and the corresponding device recommendation from the LSF family, which supports the corresponding bit count.

Table 8-1. Voltage Translator for Common Interfaces

Part Name	Channel Number	Interface
LSF0002	2	GPIO, MDIO, SMBus, PMBus, and I^2C

Some important reminders regarding the LSF0002 are as follows:

- LSF devices are switch-based, not buffer-based (for more information, see the TXB family for buffer-based devices).
- Specific data rates cannot be calculated by using 1/Tpd.
- $V_{EXT,A}$/$V_{EXT,B}$ are referenced to the external power supplies at the I/Os.
- V_{BIAS} should be tied towards the lowest voltage being translated to at the I/Os.

8.2 Typical Applications

8.2.1 Open-Drain Interface (I^2C, PMBus, SMBus, and GPIO)

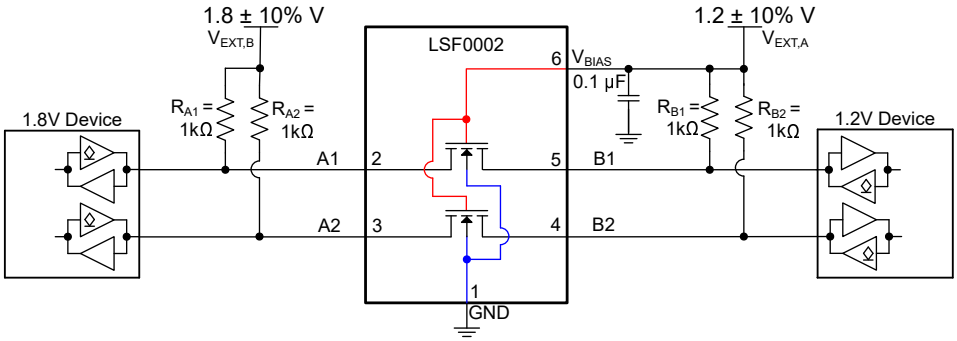


Figure 8-1. Typical Application Circuit for Open-Drain Translation (MDIO Shown as an Example)

8.2.1.1 Design Requirements

8.2.1.1.1 Enable and Disable Guidelines

In the previous figure, V_{BIAS} is referenced to the lower power supply ($V_{EXT,A}$) of 1.8V power supply and $V_{EXT,B}$ is set to 3.3V. The A1 and A2 channels have a maximum output voltage equal to $V_{EXT,A}$ and the B1 and B2 channels have a maximum output voltage equal to $V_{EXT,B}$.

The LSF0002 has an V_{BIAS} input that is used to disable the device by driving this node LOW to GND, placing all I/Os in the high-impedance state. Since the LSF family of devices are switch-type voltage translators, the power consumption is very low. TI recommends always enabling the LSF family for bidirectional applications (I^2C, SMBus, PMBus, or MDIO).

Table 8-2. Application Operating Condition

PARAMETER		MIN	TYP	MAX	UNIT
$V_{EXT,A}$ (1)	reference voltage (A)	0.9		5.5	V
$V_{EXT,B}$	reference voltage (B)	$V_{EXT,A}$ + 0.8		5.5	V
V_{BIAS}	input voltage on V_{BIAS} pin	$V_{EXT,A}$		$V_{EXT,A}$ + 0.8	V
V_{PU}	pull-up supply voltage	0		$V_{EXT,B}$	V

(1) $V_{EXT,A}$ is required to be the lowest voltage level across all inputs and outputs.

Note

The 200kΩ, bias resistor is not required for the LSF0002.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Bidirectional Translation

For the bidirectional translation configuration (higher voltage to lower voltage or lower voltage to higher voltage), the V_{BIAS} input must be connected to $V_{EXT,A}$. This allows V_{BIAS} to regulate the bias of the I/O channels for proper translation. A filter capacitor on V_{BIAS} is recommended for a stable supply at the device. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to V_{PU}).

Note

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW bus contention in either direction. If both outputs are open-drain, no direction control is needed.

8.2.1.2.2 Pull-Up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15mA. Doing this causes a voltage drop of 260mV to 350mV to have a valid LOW signal on the downstream channel. If the current through the pass transistor is higher than 15mA, then the voltage drop is also higher in the ON state. To set the current through each pass transistor at 15mA, calculate the pull-up resistor value using the following equation:

$$Rpu = \frac{(\mathrm{Vpu} - 0.35\ \mathrm{V})}{0.015\ A} \quad (1)$$

Table 8-3 provides resistor values, reference voltages, and currents at 8mA, 5mA, and 3mA. The resistor value shown in the +10% column (or a larger value) should be used so that the voltage drop across the transistor is 350mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175V, although the 15mA applies only to current flowing through the LSF family device. The device driving the low state at 0.175V must sink current from one or more of the pull-up resistors and maintain V_{OL}. A decrease in resistance will increase current, and thus result in increased V_{OL}.

Table 8-3. Pull-Up Resistor Values

V_{PU} (1) (2)	8mA		5mA		3mA	
	NOMINAL (Ω)	+10%(3) (Ω)	NOMINAL (Ω)	+10%(3) (Ω)	NOMINAL (Ω)	+10%(3) (Ω)
5V	581	639	930	1023	1550	1705
3.3V	369	406	590	649	983	1082
2.5V	269	296	430	473	717	788
1.8V	181	199	290	319	483	532
1.5V	144	158	230	253	383	422
1.2V	106	117	170	187	283	312

(1) Calculated for V_{OL} = 0.35V
(2) Assumes output driver V_{OL} = 0.175V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

8.2.1.3 Application Curve

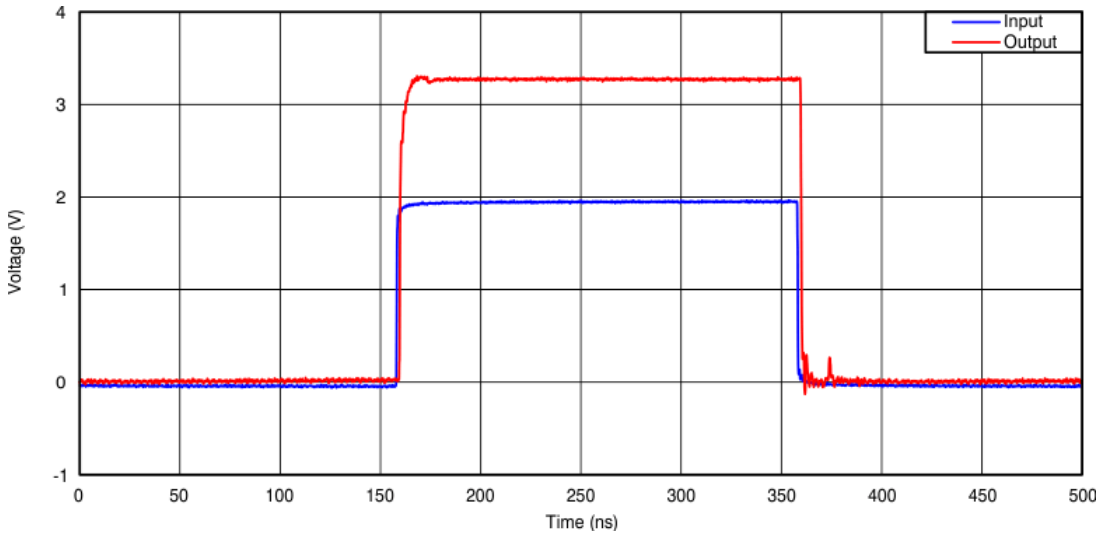


Figure 8-2. Open Drain Translation (1.8V to 3.3V at 2.5MHz)

8.2.2 Mixed-Mode Voltage Translation

The supply voltage ($V_{EXT\ A,B}$) for each channel can be individually set with a pull-up resistor. Figure 8-3 shows an example of this mixed-mode multi-voltage translation. For additional details on multi-voltage translation, see the *Multi-voltage Translation with the LSF Family* video.

With $V_{EXT,B}$ pulled up to 5V and $V_{EXT,A}$ connected to 1.2V, all channels will be clamped to 1.2V at which point a pullup can be used to define the high level voltage for a given channel.

- **Push-Pull Down Translation (5V to 1.2V):** Channel 1 is an example of this setup. When A2 is 5V, B1 is clamped to 1.2V, and when A1 is LOW, B1 is driven LOW through the switch.
- **Push-Pull Up Translation (1.2V to 3.3V)**: Channel 2 is an example of this setup. When B2 is 1.2V, the switch is high impedance and the A2 channel is pulled up to 3.3V. When B2 is LOW, A2 is driven LOW through the switch.
- **Push-Pull Down Translation (3.3V to 1.2V):** Channels 2 is an example of this setup. When A2 is driven to 3.3V, B2 is clamped to 1.2V, and when A2 is LOW, B2 is driven LOW through the switch.

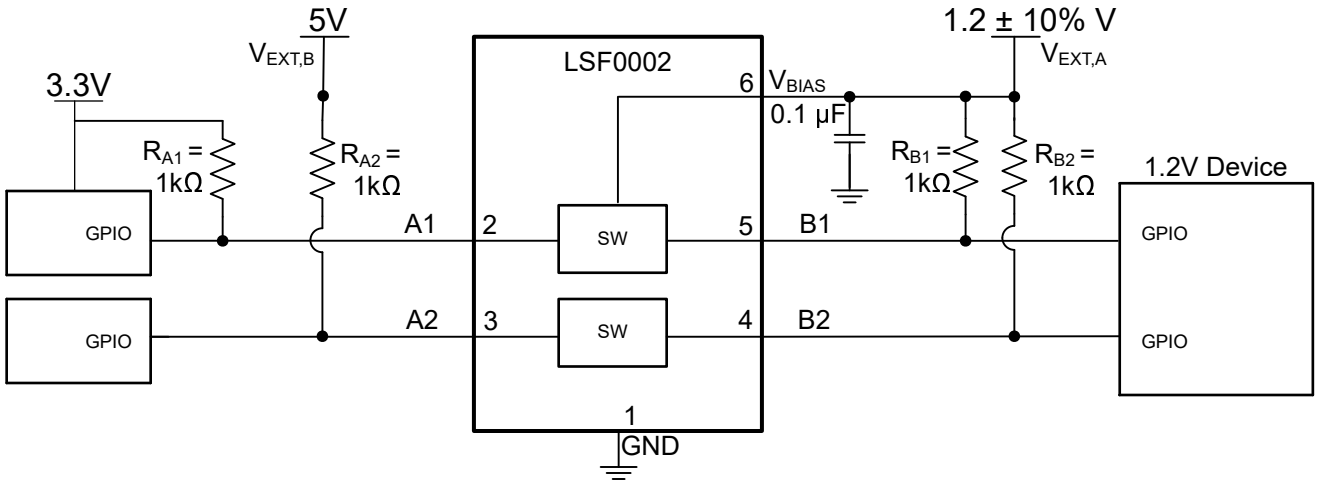


Figure 8-3. Multi-Voltage Translation Example with the LSF Translators

8.2.3 Voltage Translation for $V_{ref\_B} < V_{ref\_A} + 0.8V$

As described in the *Enable and Disable Guidelines* section, it is generally recommended that $V_{EXT,B} > V_{EXT,A} + 0.8V$; however, the device can still operate in the condition where $V_{EXT,B} < V_{EXT,A} + 0.8V$ as long as additional considerations are made for the design.

Typical Operation ($V_{EXT,B} > V_{EXT,A} + 0.8V$): in this scenario, pullup resistors are not required on the A-side for proper down-translation. When down translating from B to A, the A-side I/O ports will clamp at $V_{EXT,A}$ to provide proper voltage translation. For further explanation of device operation, see the *Down Translation with the LSF Family* video.

Requirements for $V_{EXT,B} < V_{EXT,A} + 0.8V$ Operation: in this scenario, there is not a large enough voltage difference between $V_{EXT,A}$ and $V_{EXT,B}$ so that the A side I/O ports will be clamped at $V_{EXT,A}$, but rather at a voltage approximately equal to $V_{EXT,B} – 0.8V$. For example, if $V_{EXT,B} = 1.8V$ and $V_{EXT,A} = 1.2V$, the A-side I/Os will clamp to a voltage around 1.0V. Therefore, to operate in such a condition, the following additional design considerations must be met:

- $V_{EXT,B}$ must be greater than $V_{EXT,A}$ during operation ($V_{EXT,B} > V_{EXT,A}$)
- Pullup resistors should be populated on A-side I/O ports for the line to be fully pulled up to the desired voltage.

Figure 8-4 shows an example of this setup, where 1.2V ↔ 1.8V translation is achieved with the LSF0002. This type of setup also applies for other voltage nodes such as 1.8V ↔ 2.5V, 1.05V ↔ 1.5V, and others as long as the *Recommended Operating Conditions* table is followed.

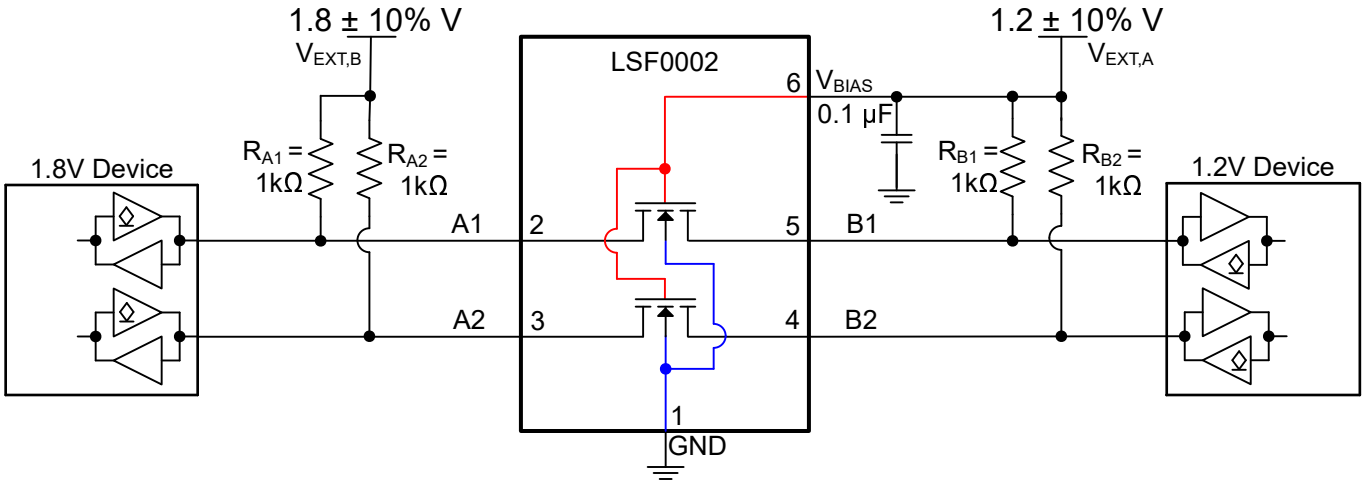


Figure 8-4. 1.2V to 1.8V Level Translation with LSF0002

8.3 Power Supply Recommendations

There are no power sequence requirements for the LSF family. Table 8-4 provides recommended operating voltages for all supply and input pins.

Table 8-4. Recommended Operating Voltages

PARAMETER		MIN	TYP	MAX	UNIT
$V_{EXT,A}$ (1)	reference voltage (A)	0.9		5.5	V
$V_{EXT,B}$	reference voltage (B)	$V_{EXT,A}$ + 0.8		5.5	V
V_{BIAS}	input voltage on EN pin	$V_{EXT,A}$		$V_{EXT,A}$ + 0.8	V
V_{PU}	pull-up supply voltage	0		$V_{EXT,B}$	V

(1) $V_{EXT,A}$ is required to be the lowest voltage level across all inputs and outputs.

8.4 Layout

8.4.1 Layout Guidelines

Because the LSF family is a switch-type level translator, the signal integrity is highly related with a pull-up resistor and PCB capacitance condition. Therefore, do as follows:

- Short the signal trace as short as possible to reduce capacitance and minimize stub from the pull-up resistor.
- Place the LSF device as close to the high voltage side as possible.
- Select the appropriate pull-up resistor that applies to translation levels and the driving capability of the transmitter.

8.4.2 Layout Example

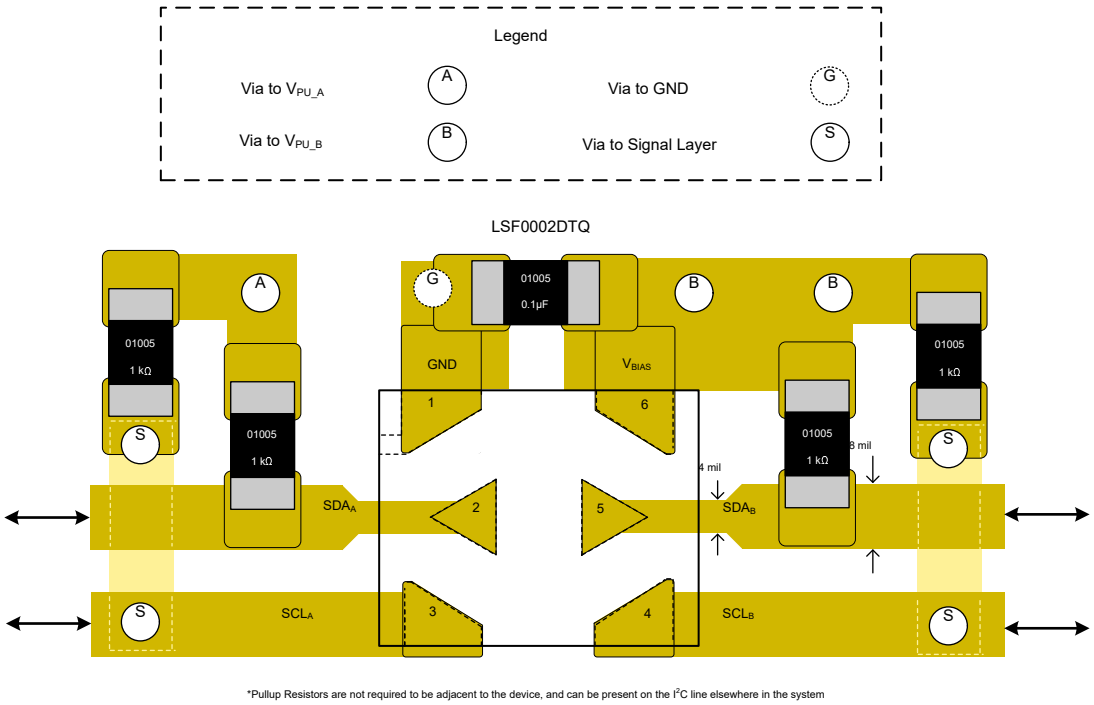


Figure 8-5. Short Trace Layout

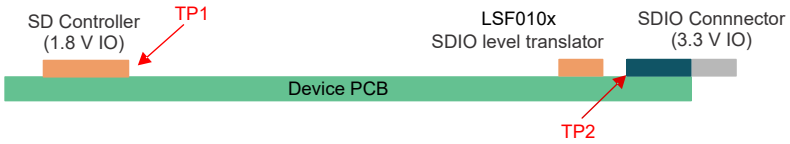


Figure 8-6. Device Placement

9 Device and Documentation Support

9.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LSF Translator Family Evaluation Module* user's guide
- Texas Instruments, *Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators* application note
- Texas Instruments, *Voltage Level Translation with the LSF Family* application note
- The Logic Minute Video Training Series on Understanding the LSF Family of Devices:
  - Texas Instruments, *Introduction - Voltage Level Translation with the LSF Family*
  - Texas Instruments, *Understanding the Bias Circuit for the LSF Family*
  - Texas Instruments, *Using the Enable Pin with the LSF Family*
  - Texas Instruments, *Translation Basics with the LSF Family*
  - Texas Instruments, *Down Translation with the LSF Family*
  - Texas Instruments, *Up Translation with the LSF Family*
  - Texas Instruments, *Multi-Voltage Translation with the LSF Family*
  - Texas Instruments, *Single Supply Translation with the LSF Family*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
April 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0002DTQR	ACTIVE	X2SON	DTQ	6	12000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

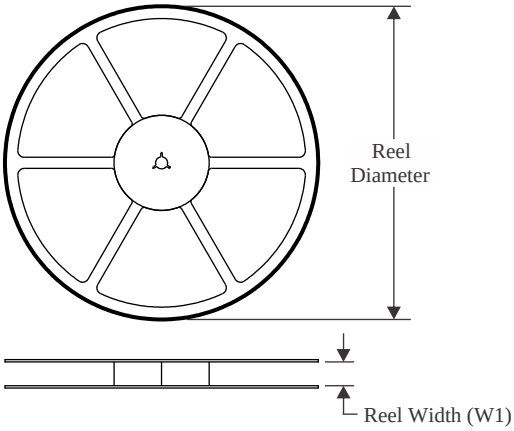
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

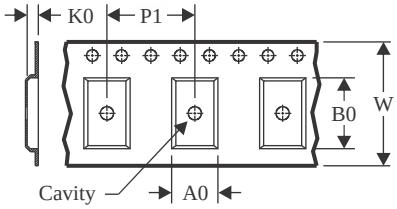
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

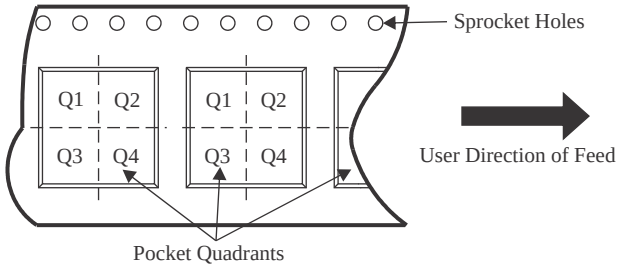


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

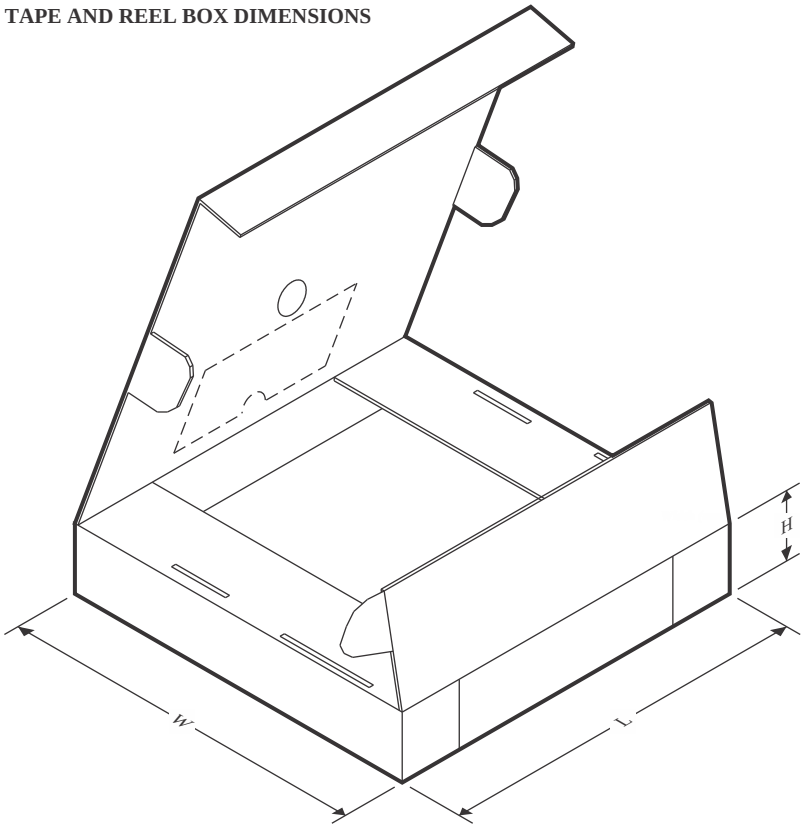
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0002DTQR	X2SON	DTQ	6	12000	180.0	8.4	0.92	1.12	0.47	4.0	8.1	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

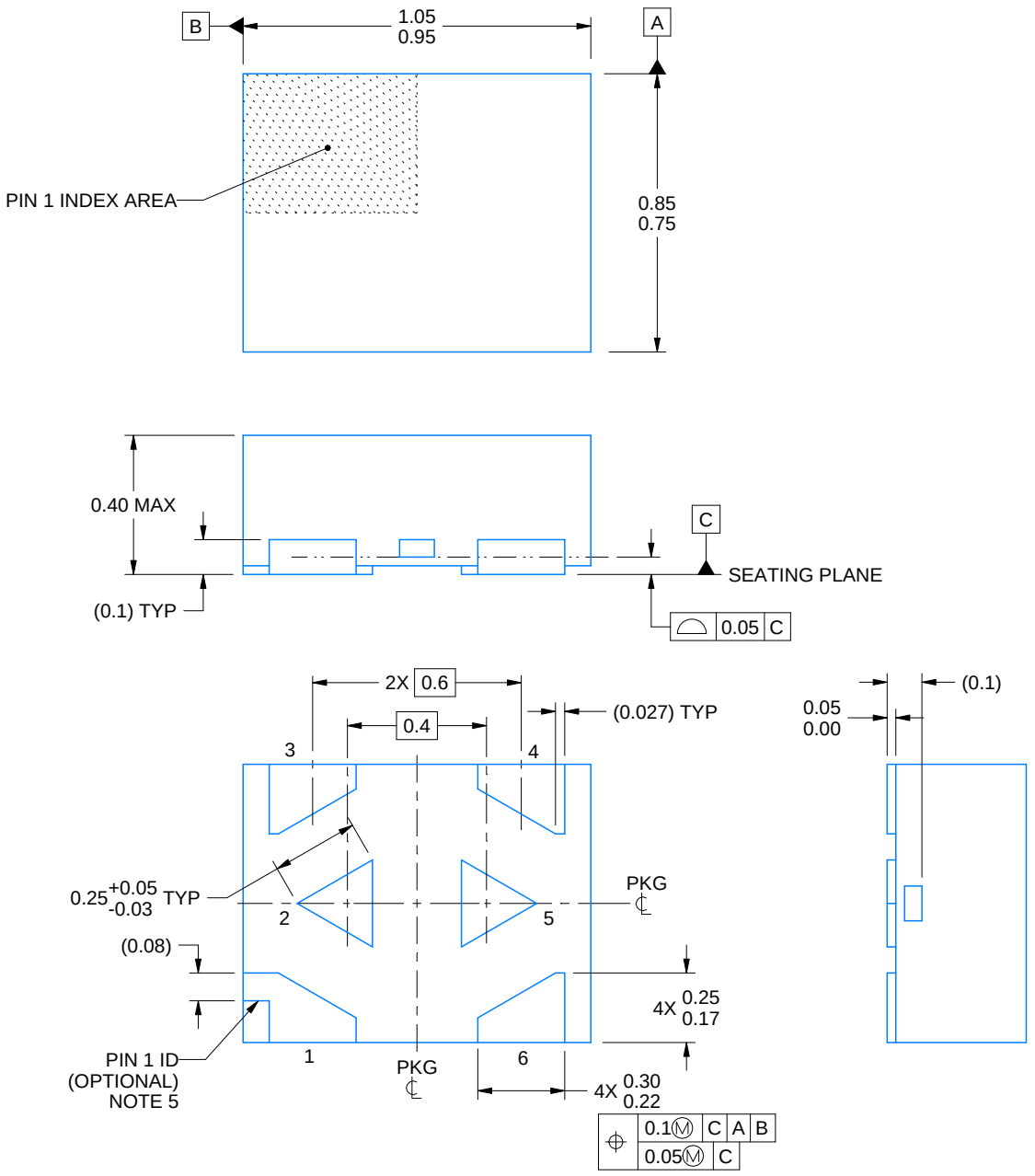
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0002DTQR	X2SON	DTQ	6	12000	182.0	182.0	20.0

DTQ0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

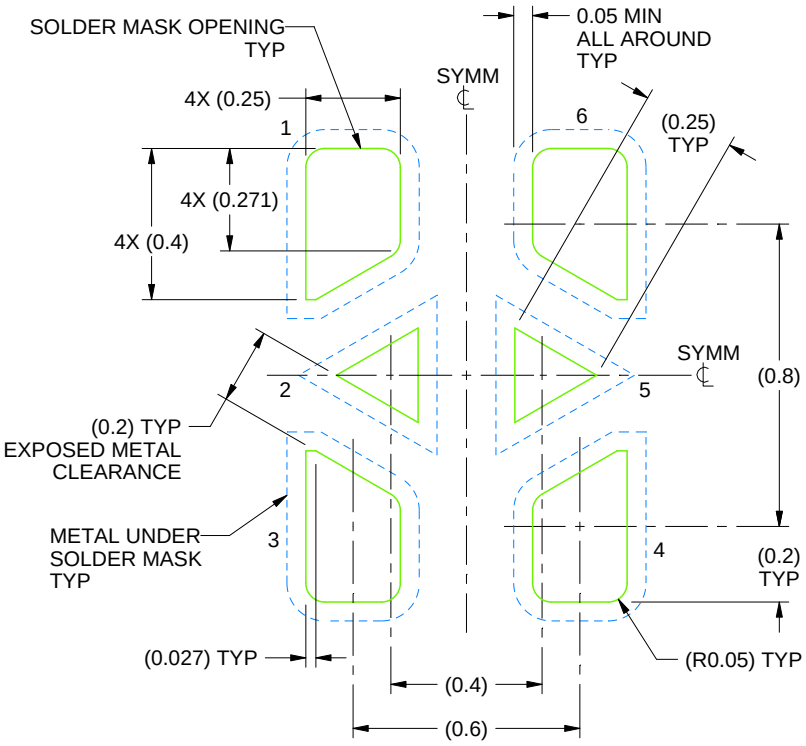
PLASTIC SMALL OUTLINE - NO LEAD



4224056/B 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

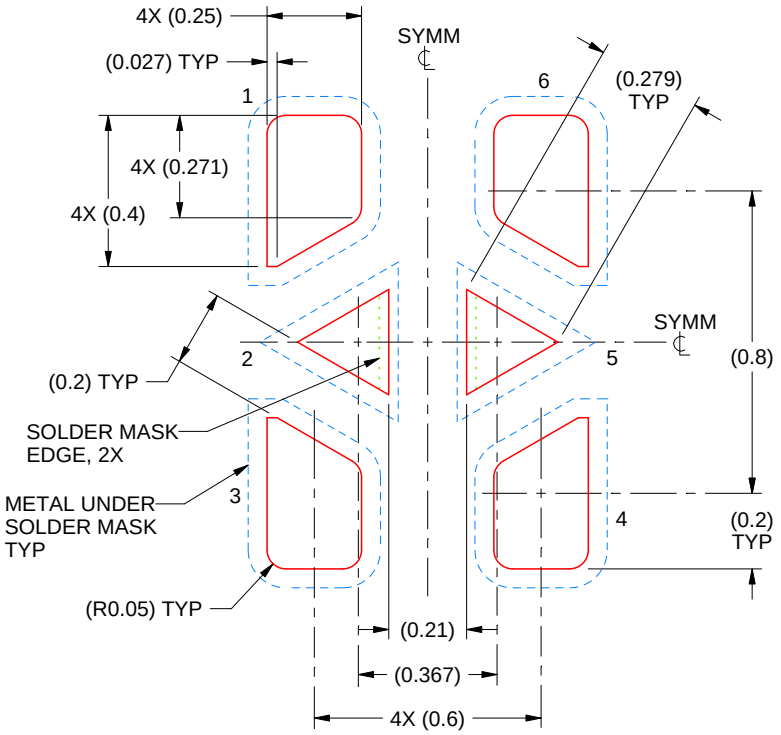


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4224056/B 07/2024

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4224056/B 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265