



3V Video Amplifier with 6dB Gain and Filter in SC70

FEATURES

- EXCELLENT VIDEO PERFORMANCE
- INTERNAL GAIN: 6dB
- 2-POLE RECONSTRUCTION FILTER
- SAG CORRECTION
 - Reduces Coupling Capacitor Size
- INPUT RANGE INCLUDES GROUND
 - DC-Coupled Input
- INTEGRATED LEVEL SHIFTER
 - DC-Coupled Output⁽¹⁾
 - No Output Capacitors Needed
- RAIL-TO-RAIL OUTPUT
- LOW QUIESCENT CURRENT: 6mA
- SHUTDOWN CURRENT: 5 μ A (max)
- SINGLE-SUPPLY: 2.7V to 3.3V
- SC70-6 PACKAGE: 2.0mm x 2.1mm

⁽¹⁾ Internal circuitry prevents the output from saturating, even with 0V sync tip level at the input video signal.

APPLICATIONS

- DIGITAL CAMERAS
- CAMERA PHONES
- SET-TOP-BOX VIDEO FILTERS

RELATED LOW VOLTAGE VIDEO AMPS

| FEATURES | PRODUCT |
|--------------------------------------------------------------------------------|---------|
| 2.7V to 5.5V, 200MHz GBW, 300V/ μ s, 6 μ A Sleep, SOT23 | OPA355 |
| 2.7V to 5.5V, RRIO, 150V/ μ s, 5mA I _Q , 6 μ A Sleep, SOT23 | OPA357 |
| 2.7V to 3.3V, SC70, 80MHz, 7.5mA I _Q , 5 μ A Sleep | OPA358 |
| 2.5V to 3.3V, SC70, Filter, G = 5.2V/V, 3 μ A Sleep | OPA361 |

DESCRIPTION

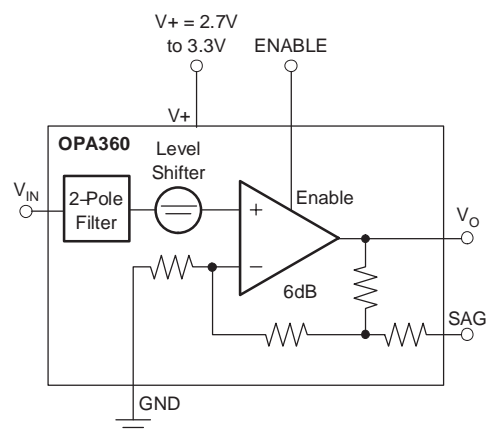
The OPA360 high-speed amplifier is optimized for 3V portable video applications. It has been specifically designed to be compatible with digital-to-analog converters (DACs) embedded in video processors, such as Texas Instruments' family of Digital Media Processors and others. The input common-mode range includes GND, which allows the Video-DAC to be DC-coupled to the OPA360.

The output swings within 25mV of GND and 300mV to V₊ with a standard back-terminated video load (150 Ω). An internal level shift circuit prevents the output from saturating with 0V input, thus preventing sync-pulse clipping in common video circuits. Therefore, the OPA360 is ideally suited for DC-coupling to the video load. If AC-coupling is preferred, the OPA360 offers a sag-correction feature that significantly reduces the size of the output coupling capacitor.

The OPA360 has been optimized for space-sensitive applications by integrating sag-correction, internal gain setting resistors (G = 2), and a 2-pole video-DAC reconstruction filter.

In shutdown mode, the quiescent current is reduced to < 5 μ A, dramatically reducing power consumption and prolonging battery life.

The OPA360 is available in the tiny 2mm x 2.1mm SC70-6 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ORDERING INFORMATION(1)

| PRODUCT | PACKAGE | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---------|---------|--------------------|-----------------|
| OPA360 | SC70-6 | DCK | AUW |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

| | |
|--------------------------------------------|---------------------------|
| Supply Voltage, V+ to V- | +3.6V |
| Signal Input Terminals, Voltage(2) | (V-) -0.5V to (V+) + 0.5V |
| Current(2) | ±10mA |
| Output Short-Circuit through 75Ω to GND(3) | Continuous |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |
| Junction Temperature | +160°C |

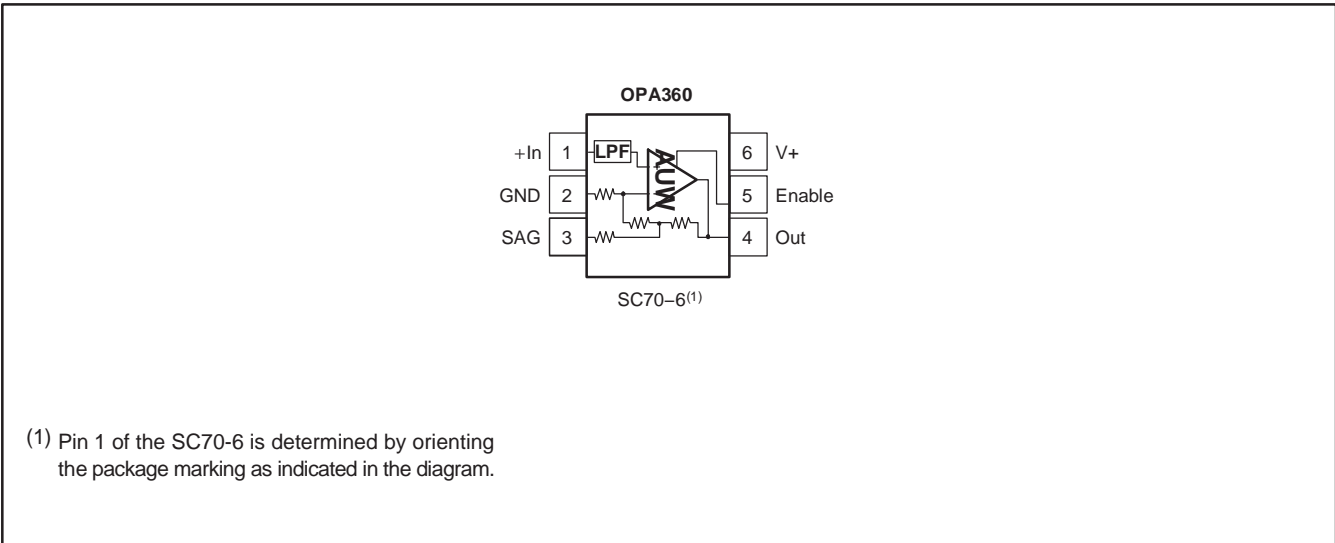
- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
- (3) Short-circuit to ground.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS: $V_S = +2.7V$ to $+3.3V$ Single-Supply
Boldface limits apply over the temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\mathbf{C}$.

 All specifications at $T_A = +25^\circ\text{C}$, $R_L = 150\Omega$ connected to GND, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA360 | | | UNITS |
|-------------------------------------------|--------------------------------------------------------------------|--------|------------|--------------|--------------------|
| | | MIN | TYP | MAX | |
| OFFSET LEVEL-SHIFT VOLTAGE | | | | | |
| Output Level-Shift Voltage ⁽¹⁾ | $V_S = +3.3V$, $V_{IN} = \text{GND}$, $G = +2$ | 30 | 60 | 80 | mV |
| Over Temperature | Specified Temperature Range | | 60 | | mV |
| vs. Power Supply | $V_S = +2.7V$ to $+3.3V$ | | ± 80 | | $\mu\text{V/V}$ |
| INPUT BIAS CURRENT | | | | | |
| Input Bias Current | | | ± 3 | | pA |
| INPUT VOLTAGE RANGE | | | | | |
| Common-Mode Voltage Range ⁽²⁾ | $V_S = 3.3V$, $G = +2$ | GND | | $(V+) - 1.5$ | V |
| VOLTAGE GAIN | | | | | |
| | $V_S = +3.3V$, $0 < V_{IN} < 1.5V$ | 5.8 | 6 | 6.2 | dB |
| FREQUENCY RESPONSE | | | | | |
| Filter Response | | | | | |
| Normalized Gain: $f_{IN} = 4.5\text{MHz}$ | $V_O = 2V_{PP}$ | -0.6 | -0.1 | +0.4 | dB |
| $f_{IN} = 27\text{MHz}$ | $V_O = 2V_{PP}$ | -18 | -21 | | dB |
| Differential Gain Error | $R_L = 150\Omega$ | | 0.5 | | % |
| Differential Phase Error | $R_L = 150\Omega$ | | 1 | | $^\circ$ |
| Group Delay Variation | 100kHz, 5MHz | | 13 | | ns |
| Signal-to-Noise Ratio | 100% White Signal | | 70 | | dB |
| OUTPUT | | | | | |
| Positive Voltage Output Swing from Rail | $V_S = +3.3V$, $G = 2$, $V_{IN} = 2V$, $R_L = 150\Omega$ to GND | | 160 | 300 | mV |
| Negative Voltage Output Swing from Rail | $V_S = +3.3V$, $G = 2$, $V_{IN} = 0V$, $R_L = 150\Omega$ to GND | | 3 | 25 | mV |
| Positive Voltage Output Swing from Rail | $V_S = +3.3V$, $G = 2$, $V_{IN} = 2V$, $R_L = 75\Omega$ to GND | | 300 | | mV |
| Negative Voltage Output Swing from Rail | $V_S = +3.3V$, $G = 2$, $V_{IN} = 0V$, $R_L = 75\Omega$ to GND | | 10 | | mV |
| Output Current ⁽³⁾ | $V_S = +3.3V$ | | ± 80 | | mA |
| POWER SUPPLY | | | | | |
| Specified Voltage Range | | 2.7 | | 3.3 | V |
| Minimum Operating Voltage Range | | | 2.5 to 3.6 | | V |
| Quiescent Current | $V_S = +3.3V$, Enabled, $I_O = 0$ | | 6 | 7.5 | mA |
| | Specified Temperature Range | | | 9 | mA |
| ENABLE/SHUTDOWN FUNCTION | | | | | |
| Disabled (logic-LOW Threshold) | | 1.6 | | 0.8 | V |
| Enabled (logic-HIGH Threshold) | | | | | V |
| Enable Time | | | 1.5 | | μs |
| Disable Time | | | 50 | | ns |
| Shutdown Current | $V_S = +3.3V$, Disabled | | 2.5 | 5 | μA |
| TEMPERATURE RANGE | | | | | |
| Specified Range | | -40 | | +85 | $^\circ\text{C}$ |
| Operating Range | | -40 | | +85 | $^\circ\text{C}$ |
| Storage Range | | -65 | | +150 | $^\circ\text{C}$ |
| Thermal Resistance | θ_{JA} | | | | $^\circ\text{C/W}$ |
| SC70 | | | 250 | | |

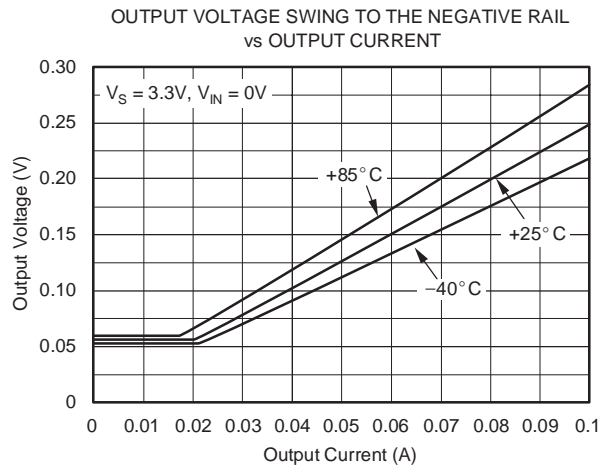
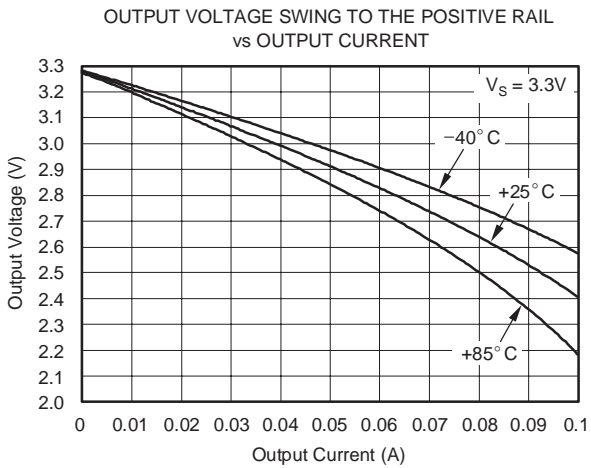
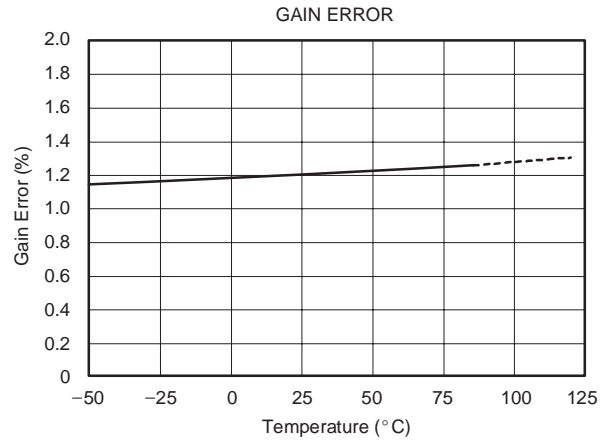
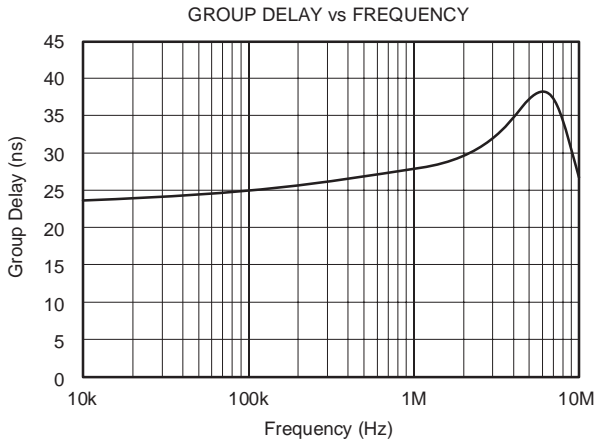
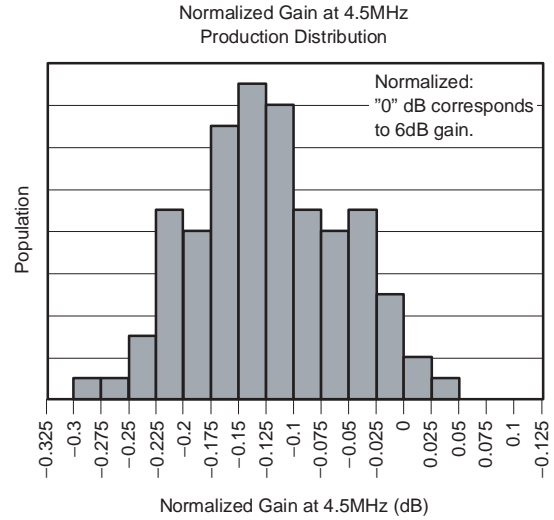
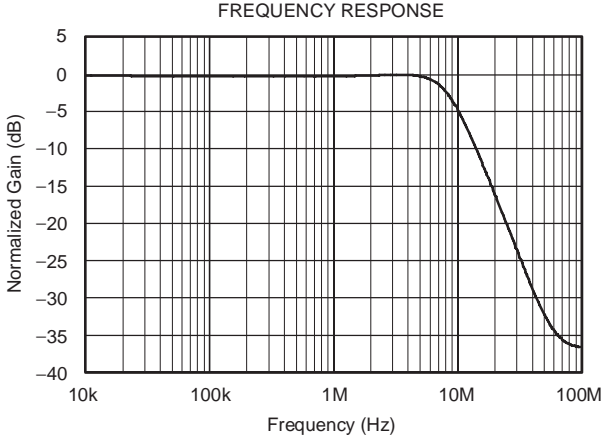
(1) Output referred. Tested with SAG pin connected to OUT pin.

 (2) Limited by output swing and internal $G = 2$. Tested with the SAG pin connected to OUT pin.

 (3) See typical characteristics *Output Voltage Swing vs Output Current*.

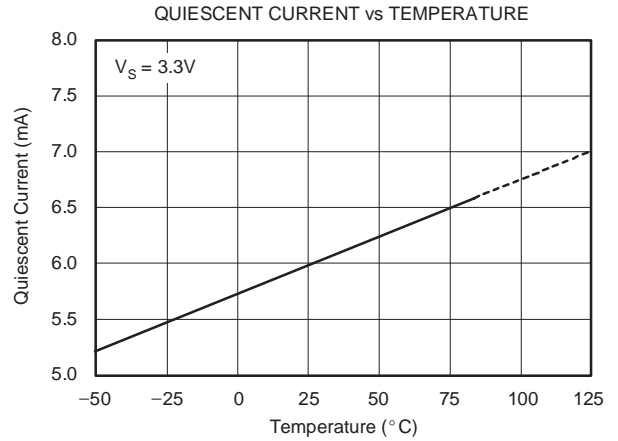
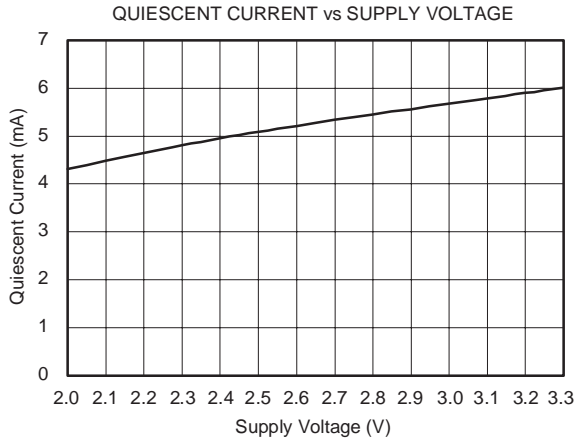
TYPICAL CHARACTERISTICS: $V_S = 3.3V$

At $T_A = +25^\circ C$ and $R_L = 150\Omega$, unless otherwise noted.



TYPICAL CHARACTERISTICS: $V_S = 3.3V$ (continued)

At $T_A = +25^\circ C$ and $R_L = 150\Omega$, unless otherwise noted.

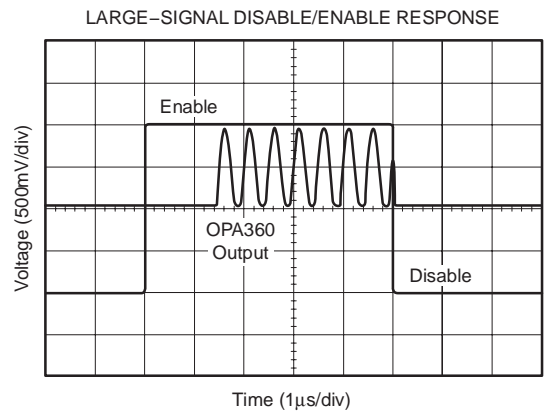
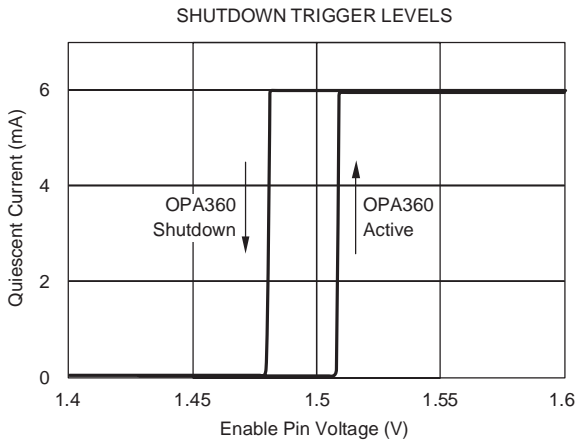
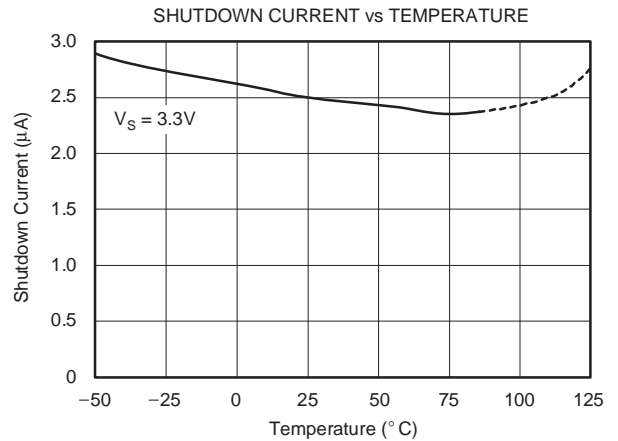


DIFFERENTIAL GAIN

| INP=A-C | SYNG=INT | MTIME=10 μ | LINE=330 |
|---------|----------|----------------|----------|
| DG1 | -0.23 % | 0 | +5 |
| DG2 | -0.37 % | █ | |
| DG3 | -0.45 % | █ | |
| DG4 | -0.49 % | █ | |
| DG5 | -0.46 % | █ | |
| STEPS | 4 | 5 | |
| ZOOM | 0 | 1 | 2 |
| MODE | | | 4 |

DIFFERENTIAL PHASE

| INP=A-C | SYNG=INT | MTIME=10 μ | LINE=330 |
|---------|----------|----------------|----------|
| DP1 | 0.56 deg | █ | |
| DP2 | 0.87 deg | █ | |
| DP3 | 1.00 deg | █ | |
| DP4 | 1.02 deg | █ | |
| DP5 | 0.90 deg | █ | |
| STEPS | 4 | 5 | |
| ZOOM | 0 | 1 | 2 |
| MODE | | | 1 |



APPLICATIONS INFORMATION

The OPA360 video amplifier has been optimized for portable video applications:

- Internal gain setting resistors ($G = 2$) reduce the number of external components needed in the video circuit.
- A 2-pole filter is incorporated for DAC signal reconstruction.
- The sag correction function reduces the size of the output coupling capacitors without compromising performance.
- OPA360 employs an internal level shift circuit that avoids sync pulse clipping and allows DC-coupled output.
- A shutdown feature reduces quiescent current to less than $5\mu\text{A}$ —crucial for portable applications such as digital still cameras (DSCs) and camera phones.

The OPA360 interfaces to digital media processors (DM320/270, DSC25). It has been optimized for the requirements of digital still cameras and cell phone/camera designs.

OPERATING VOLTAGE

The OPA360 is fully specified from 2.7V to 3.3V over a temperature range of -40°C to $+85^{\circ}\text{C}$. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

Power-supply pins should be bypassed with 100nF ceramic capacitors.

INPUT VOLTAGE

The input common-mode range of the OPA360 series extends from GND to $(V+) - 1.5\text{V}$. Because of the internal gain, the input voltage range necessary for an output in the valid range will be limited.

INPUT OVERVOLTAGE PROTECTION

All OPA360 pins are static-protected with internal ESD protection diodes connected to the supplies. These diodes will provide input overdrive protection if the current is externally limited to 10mA

ENABLE/SHUTDOWN

The OPA360 has a shutdown feature that disables the output and reduces the quiescent current to less than $5\mu\text{A}$. This feature is especially useful for portable video applications such as digital still cameras and camera phones, where the equipment is infrequently connected to a TV or other video device.

The Enable logic input voltage is referenced to the OPA360 GND pin. A logic level HIGH applied to the enable pin enables the op amp. A valid logic HIGH is defined as $\geq 1.6\text{V}$ above GND. A valid logic LOW is defined as $\leq 0.8\text{V}$ above GND. If the Enable pin is not connected, internal pull-up circuitry will enable the amplifier. Enable pin voltage levels are tested for a valid logic HIGH threshold of 1.6V minimum and a valid logic LOW threshold of 0.8V maximum.

INTERNAL 2-POLE FILTER

The OPA360 filter is a Sallen-Key topology with a 9MHz cutoff frequency. This allows the video signals to pass without any visible distortion, as shown in Figure 3 through Figure 5. The video DACs embedded in TI's Digital Media Processors over-sample at 27MHz. At this frequency, the attenuation is typically 21dB, which effectively attenuates the sampling aliases.

The filter characteristics vary somewhat with signal source impedance. A source impedance greater than 500Ω can degrade filter performance. With current-output video DACs, a resistor to GND is often used to create a voltage output which is then applied to the OPA360 input (see Figure 1). TI's Digital Media Processors, such as the DM270 or DM320, typically use a 200Ω resistor to GND to convert the current output signal. This 200Ω source impedance does not degrade video performance.

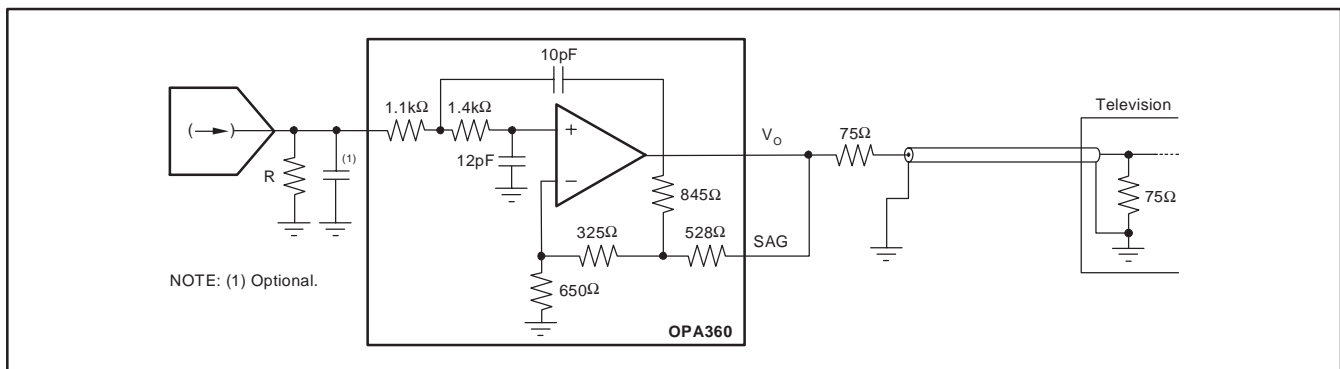


Figure 1. Filter Structure of OPA360

A capacitor placed in parallel with the resistor (Figure 1) creates an additional filter pole that provides additional stop-band attenuation. With a 200Ω source impedance, a 67pF ceramic capacitor provides approximately 28dB attenuation at 27MHz without affecting the pass band.

VIDEO PERFORMANCE

Industry standard video test patterns include:

- Multiburst—packets of different test frequencies to check for basic frequency response.
- Multipulse—pulses modulated at different frequencies to test for comprehensive measurement

of amplitude and group delay errors across the video baseband.

- Chrominance-to-luminance (CCIR17) — tests amplitude, phase and some distortion
- 50Hz, 1/2 black–1/2 white screen test signal—tests the worst case signal swing required by the amplifier. Performance on these test signals are shown.

Figure 2 shows the test circuits for Figure 3 through Figure 13 and Figure 16. (NOTE: 1 and 2 indicate measurement points corresponding to the waveforms labeled 1 and 2 in the figures.)

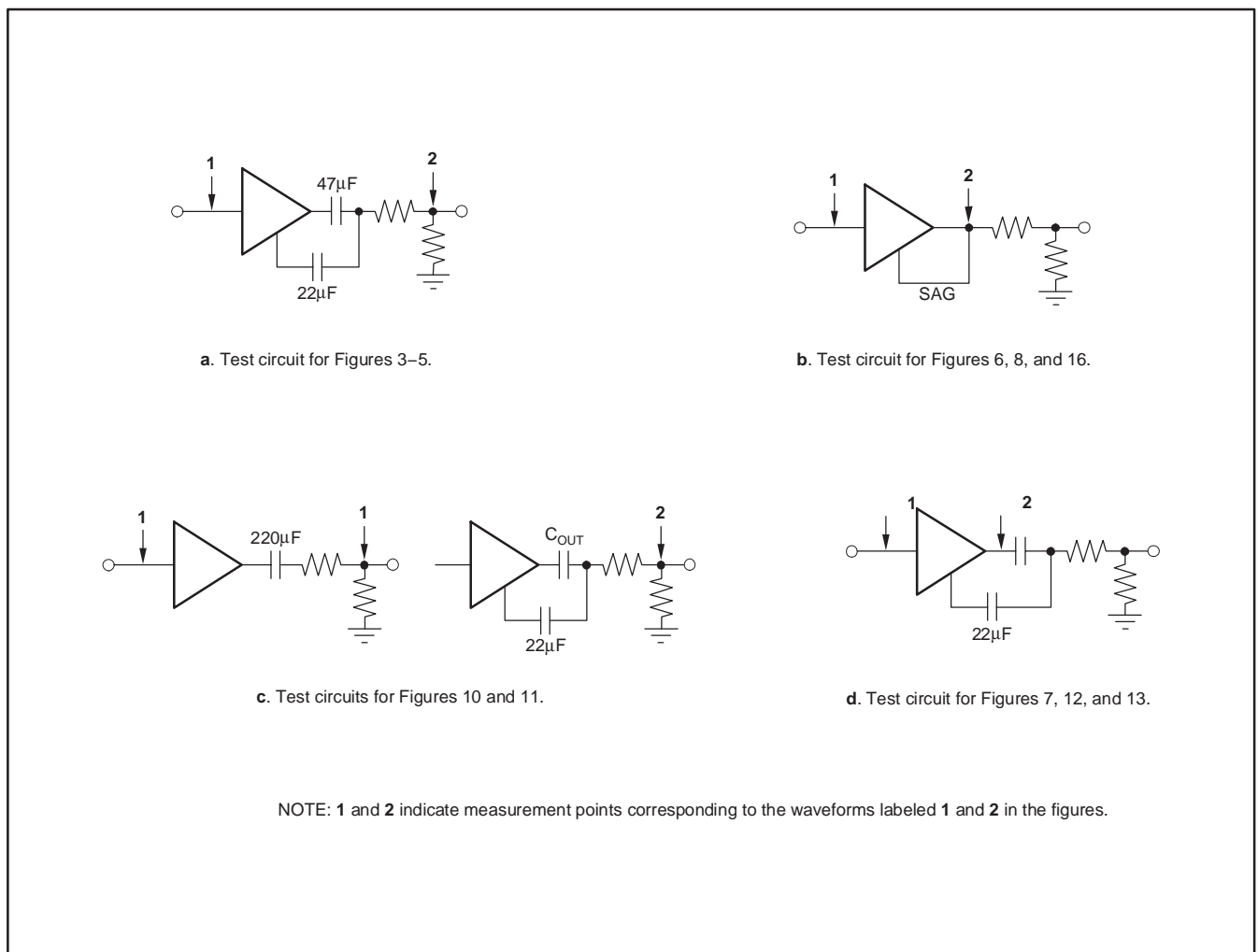


Figure 2. Test Circuits Used for Figures 3–13

FREQUENCY RESPONSE OF THE OPA360

Frequency response measurements evaluate the ability of a video system to uniformly transfer signal components of different frequencies without affecting their respective amplitudes. Figure 3 shows the multiburst test pattern; Figure 4 shows the multipulse. The top waveforms in these figures show the full test pattern. The middle and bottom waveform are a more detailed view of the critical portion of the full waveform. The middle waveform represents the input signal from the video generator; the bottom waveform is the OPA360 output to the line.

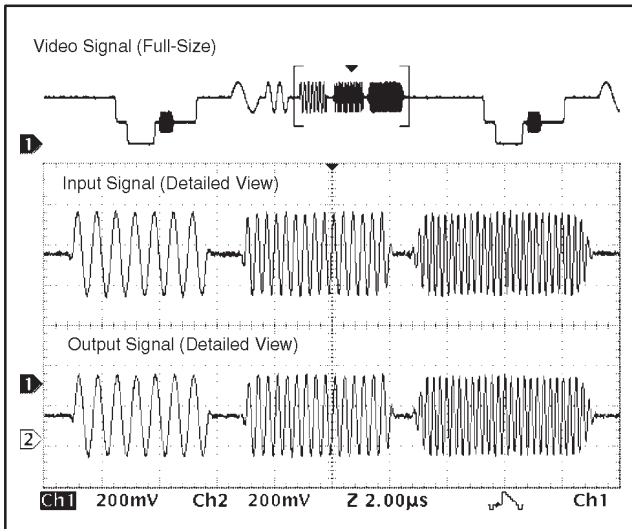


Figure 3. Multiburst (CCIR 18) Test Pattern (PAL)

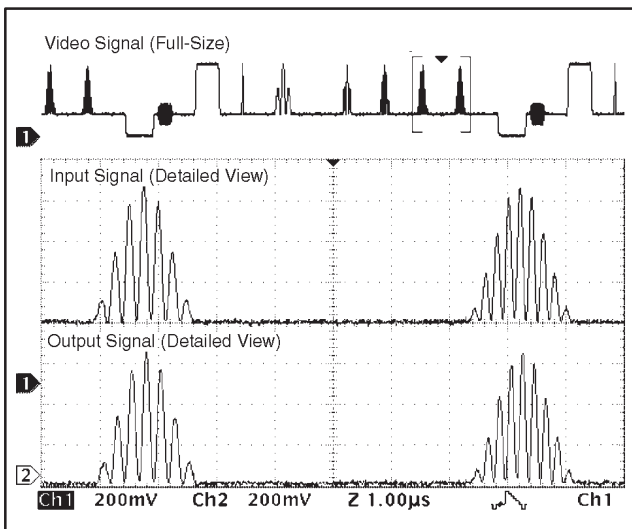


Figure 4. Multipulse Test Pattern (PAL)

Chrominance-to-luminance gain inequality (or relative chrominance level) is a change in the gain ratio of the chrominance and luminance components of a video signal, which are at different frequencies. A common test pattern is the pulse in test pattern CCIR 17, shown in Figure 5. As in Figure 3 and Figure 4, the top waveform shows the full test pattern; the middle and bottom waveform are a more detailed view of the critical portion of the full waveform, with the middle waveform representing the input signal from the video generator and the bottom waveform being the OPA360 output to the line.

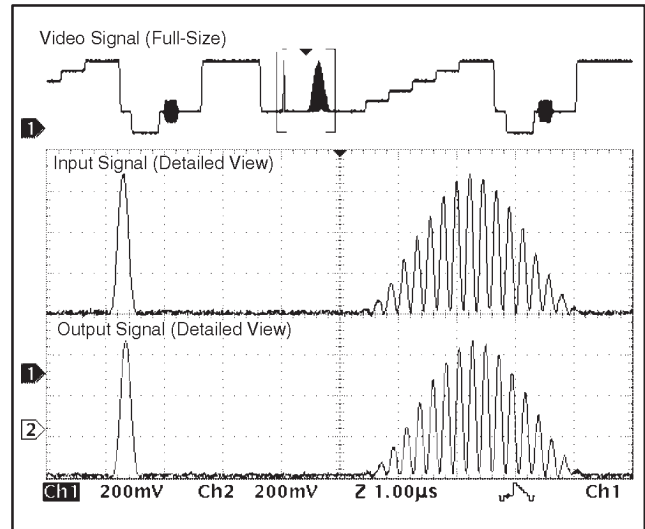


Figure 5. CCIR 17 Test Pattern (PAL)

Gain errors most commonly appear as attenuation or peaking of the chrominance information. This shows up in the picture as incorrect color saturation. Delay distortion will cause color smearing or bleeding, particularly at the edges of objects in the picture. It may also cause poor reproduction of sharp luminance transitions.

All waveforms in Figure 3 through Figure 5 were taken using the sag correction feature of OPA360. Figure 3 through Figure 5 show that the OPA360 causes no visible distortion or change in gain throughout the entire video frequency range.

INTERNAL LEVEL SHIFT

Many common video DACs embedded in digital media processors like TI's TMS320DM270 and the new OMAP2420 processors operate on a single supply (no negative supply). Typically, the lowest point of the sync pulse output by these Video DACs corresponds to 0V. With a 0V input, the output of common single-supply op amps saturates at a voltage > 0V. This effect would clip the tip of the sync pulse and therefore degrade the video signal integrity. The OPA360 employs an internal level shift circuit to avoid clipping. The input signal is typically shifted by

approximately 60mV. This is well within the linear output voltage range of the OPA360 with a standard 150Ω video load. Figure 6 shows the function of the level shifter.

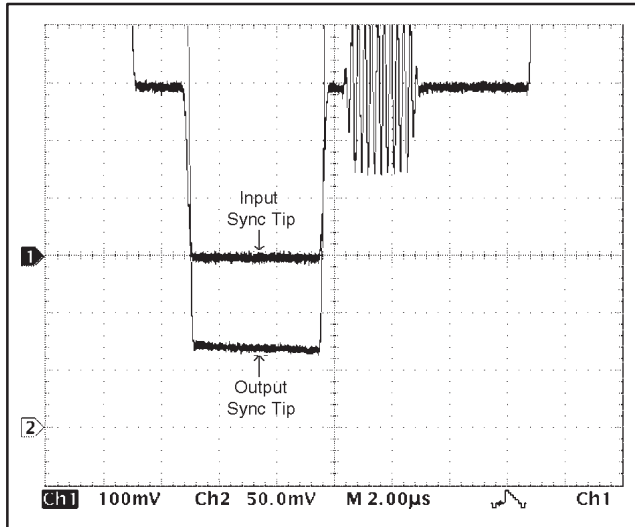


Figure 6. Internal Level Shifter, Shifts Input Signal by Approximately 60mV to Prevent Sync Tip Clipping

The level shift function is particularly useful when the output of the OPA360 is DC-coupled to the video load. However, it is also helpful when sag correction is employed. The offset helps to shift the video signal closer to the positive rail, so that with even a small 33µF coupling capacitor, the output is well outside the saturation limits of the OPA360. Figure 7 shows the output swing of the OPA360, operated on 3.0V supplies, with a 22µF sag correction capacitor and a 33µF output coupling capacitor. The test signal is a 50Hz signal constructed to generate a 1/2 black, 1/2 white screen. This video pattern is one of the most difficult patterns to display because it is the worst case signal regarding signal swing. A worst case signal such as this is highly unlikely in normal operation. Any other signal has a lower swing range. Note in Figure 7 that neither the white nor the black portion of the video signal is clipped.

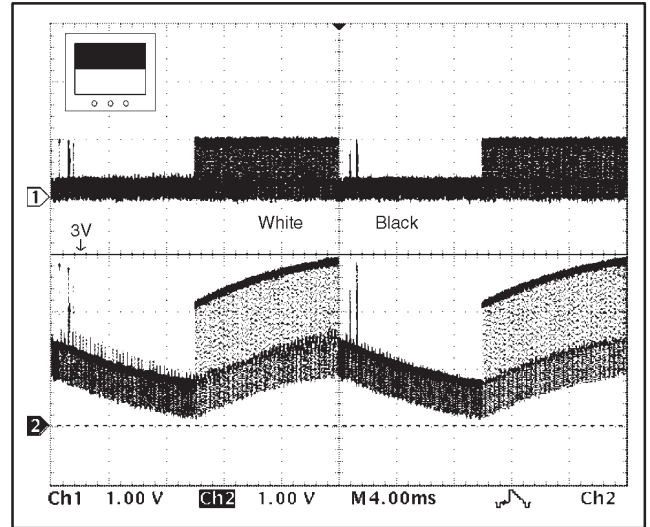


Figure 7. Output Swing with 33µF on 3V Supply

OUTPUT SWING TO GND (SYNC PULSE)

Figure 8 shows the true output swing capability of the OPA360 by taking the tip of the input sync pulse to a slightly negative voltage. Even when the output sync tip is at 8mV, the output shows no clipping of the sync pulse.

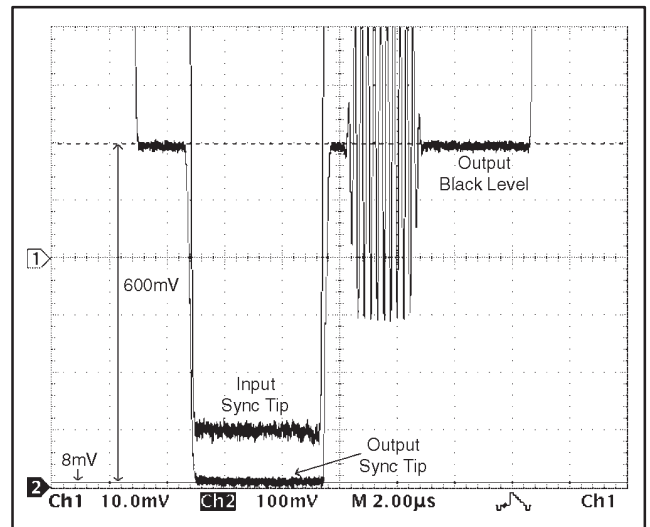


Figure 8. Input Sync Tip at -30mV (Output Shows No Sign of Clipping)

SAG CORRECTION

Sag correction provides excellent video performance with two small output coupling capacitors. It eliminates the traditional, large 220µF output capacitor. The traditional 220µF circuit (Figure 9a) creates a single low frequency pole (–3dB frequency) at 5Hz. If this capacitor is made much smaller, excessive phase shift in the critical 50 to 100Hz range produces *field tilt* which can interfere with proper recovery of synchronization signals in the television receiver.

The OPA360 sag correction circuit (Figure 9b, see also Figure 14) creates an amplitude response peak in the 20Hz region. This small amount of peaking (a few tenths of a dB) provides compensation of the phase response in the critical 50Hz to 100Hz range, greatly reducing field tilt. Note that two significantly smaller and lower cost capacitors are required.

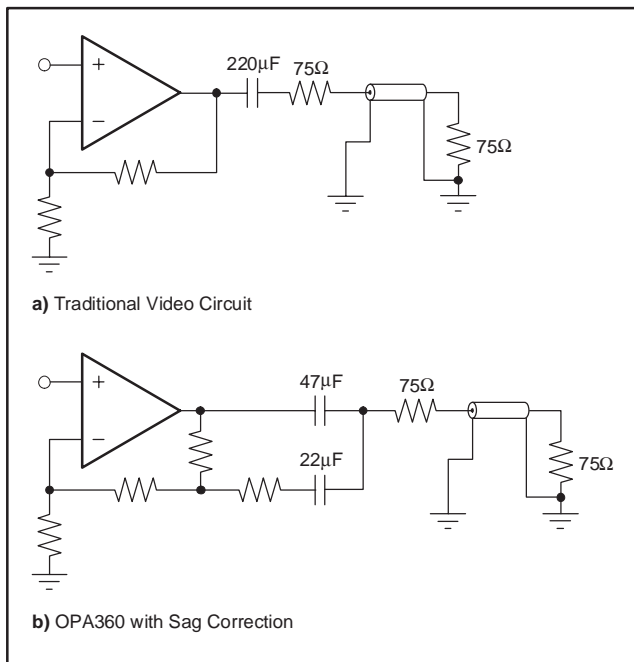


Figure 9. Traditional Video Circuit vs OPA360 with Sag Correction

To achieve good performance, a 22µF sag correction and 47µF coupling capacitor can be used. Figure 10 and Figure 11 show comparisons for a standard video circuit with a 220µF coupling capacitor and the OPA360 with sag correction.

Figure 10 shows that the 22µF/47µF combination leads to only a slightly greater tilt in the 50Hz, 1/2 black – 1/2 white video signal. No degradation in video quality is observed.

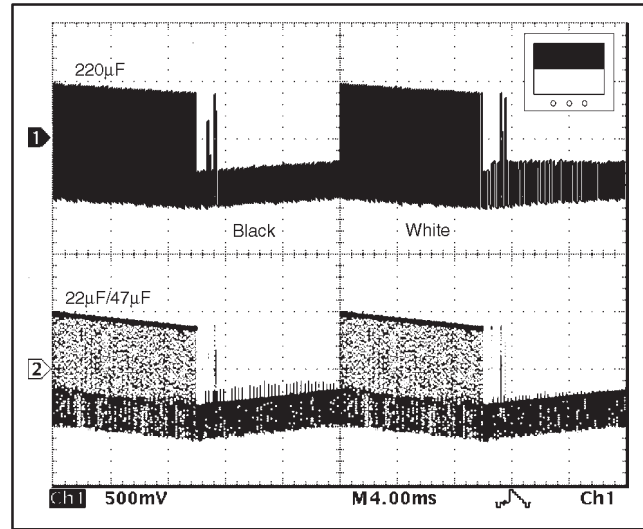


Figure 10. Standard Video Circuit with 220µF Capacitor (top trace) vs OPA360 with 22µF and 47µF Capacitors

A field tilt equivalent to that achieved using the standard 220µF coupling capacitor can be achieved with a 22µF/67µF combination – see Figure 11. These capacitor values are optimized—sag correction capacitors larger than 22µF do not provide significant improvement. Smaller sag correction capacitors will lead to higher tilt.

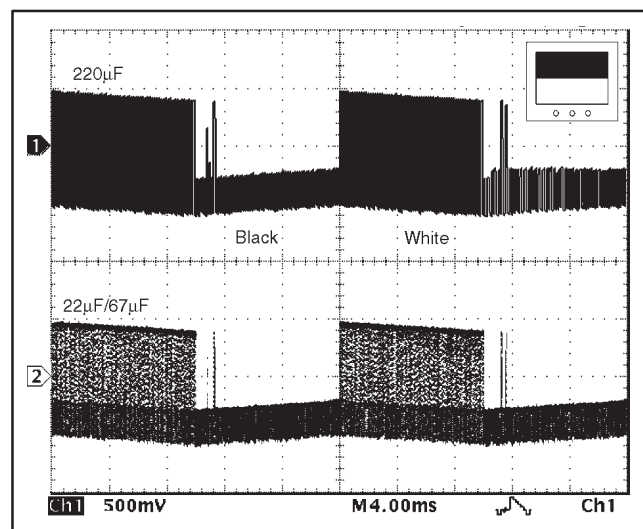


Figure 11. 220µF Standard Video Circuit (top trace) vs OPA360 with 22µF and 67µF Capacitors

SUPPLY VOLTAGE vs COUPLING CAPACITOR

The output voltage swing is a function of the coupling capacitor value. The value of the sag correction capacitor has only a minor influence. The smaller the coupling capacitor, the greater the output swing. Therefore, to accommodate the large signal swing with very small coupling capacitors (22 μ F and 33 μ F), a higher supply voltage might be needed.

As seen in Figure 7, the output swing with a 33 μ F coupling capacitor is already very close to the saturation limit on a 3V supply. Over time and temperature, a capacitor might change its value slightly, which in turn could force the output into saturation. Using the 50Hz, 1/2 black—1/2 white screen test signal as a worst-case analysis, Figure 12 and Figure 13 demonstrate that a 3V supply could be used with a coupling capacitor as low as 47 μ F.

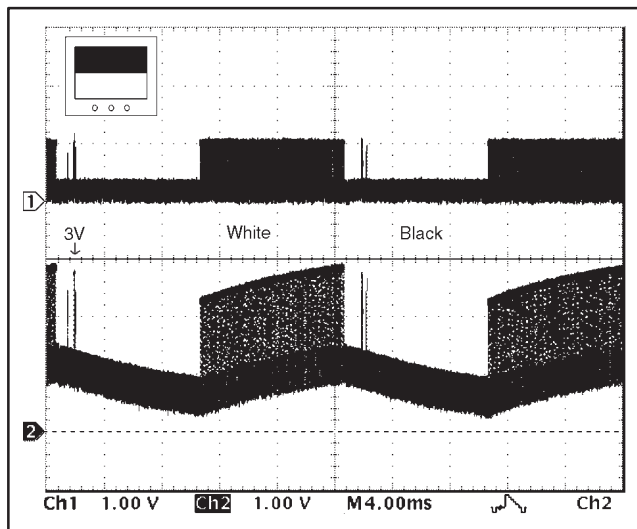


Figure 12. Output Swing with 47 μ F on 3V Supply

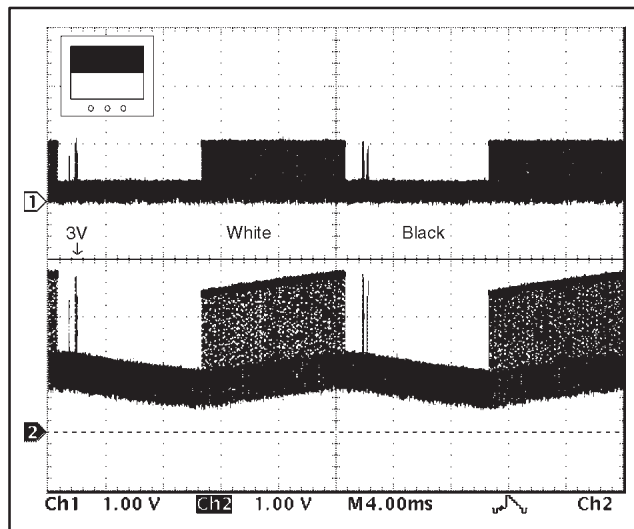


Figure 13. Output Swing with 67 μ F on 3V Supply

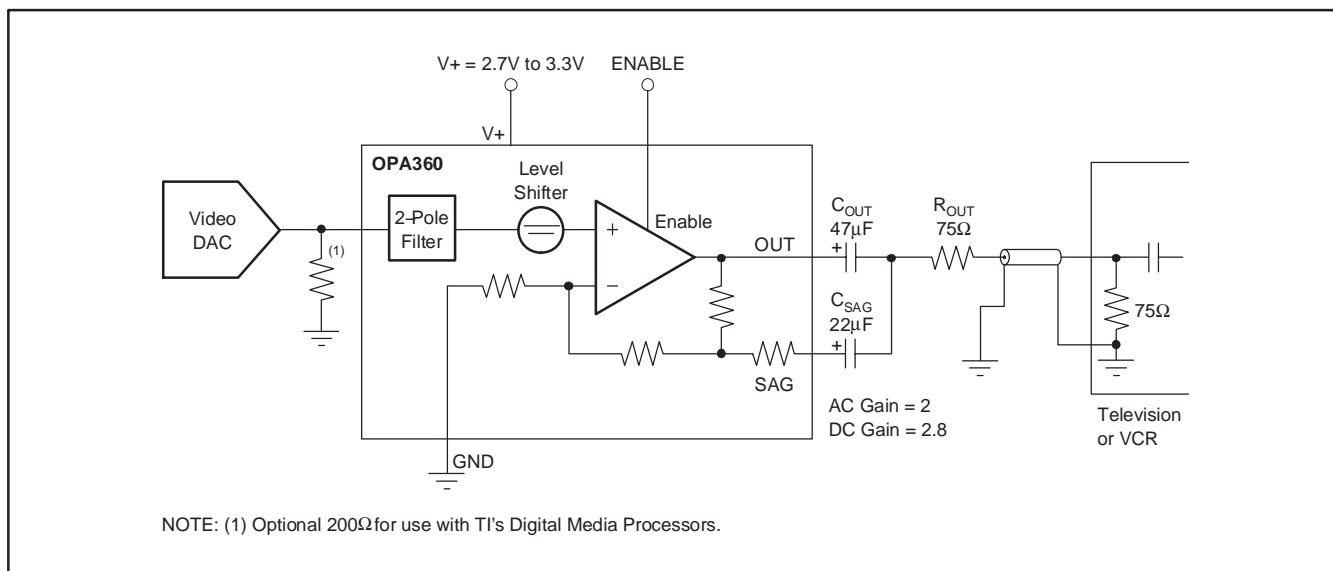


Figure 14. DC-Coupled Input/AC-Coupled Output

DC-COUPLED OUTPUT

Due to the internal level shift, the OPA360 can also be DC-coupled to a video load. As shown in Figure 15, this eliminates the need for AC-coupling capacitors at the output. This is especially important in portable video applications where board space is restricted.

The DC-coupled output configuration also shows the best video performance. As seen in Figure 16, there is no line or field tilt—allowing use of the lowest power supply. In this mode, the OPA360 will safely operate down to 2.5V with no clipping of the signal.

The disadvantage with DC-coupled output is that it uses somewhat higher supply current.

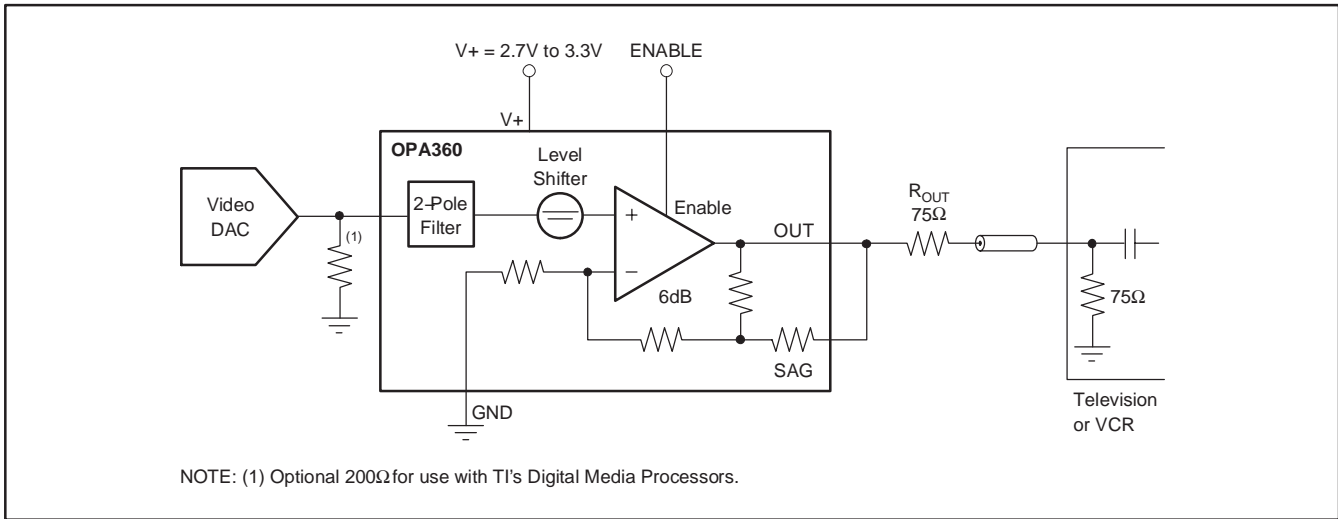


Figure 15. DC-Coupled Input/DC-Coupled Output

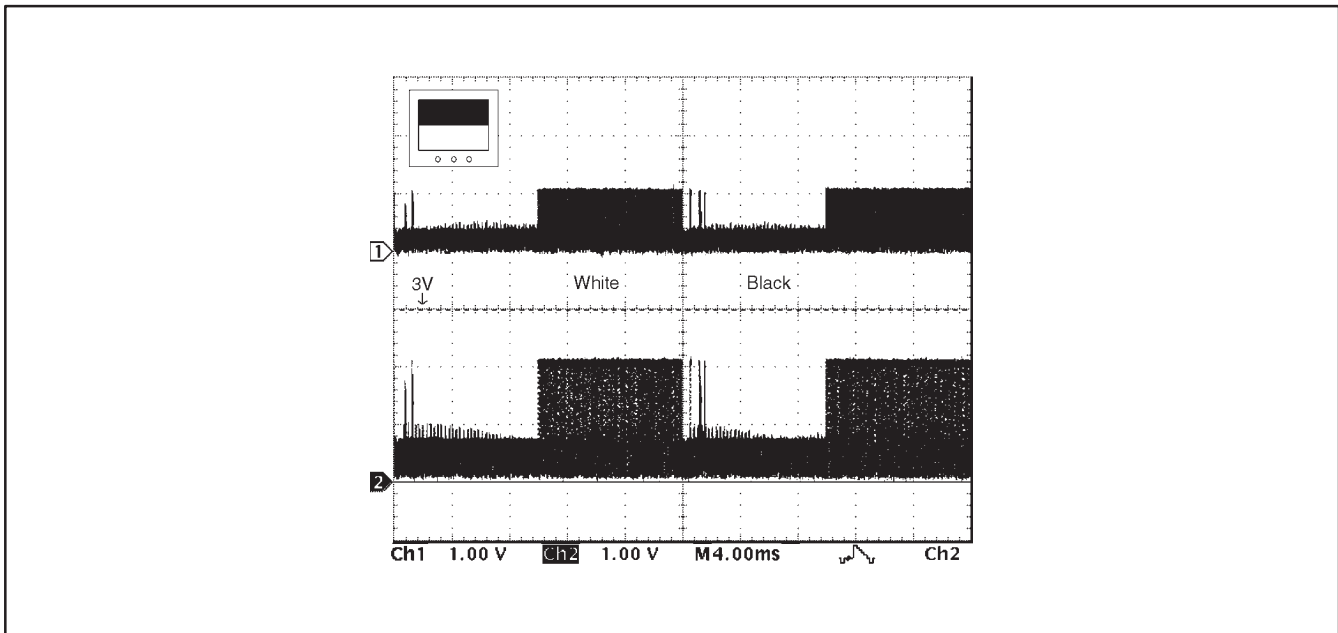


Figure 16. DC-Coupled Output

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| OPA360AIDCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA360AIDCKRE4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA360AIDCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA360AIDCKTG4 | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA360AIDCKR | SC70 | DCK | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| OPA360AIDCKT | SC70 | DCK | 6 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS

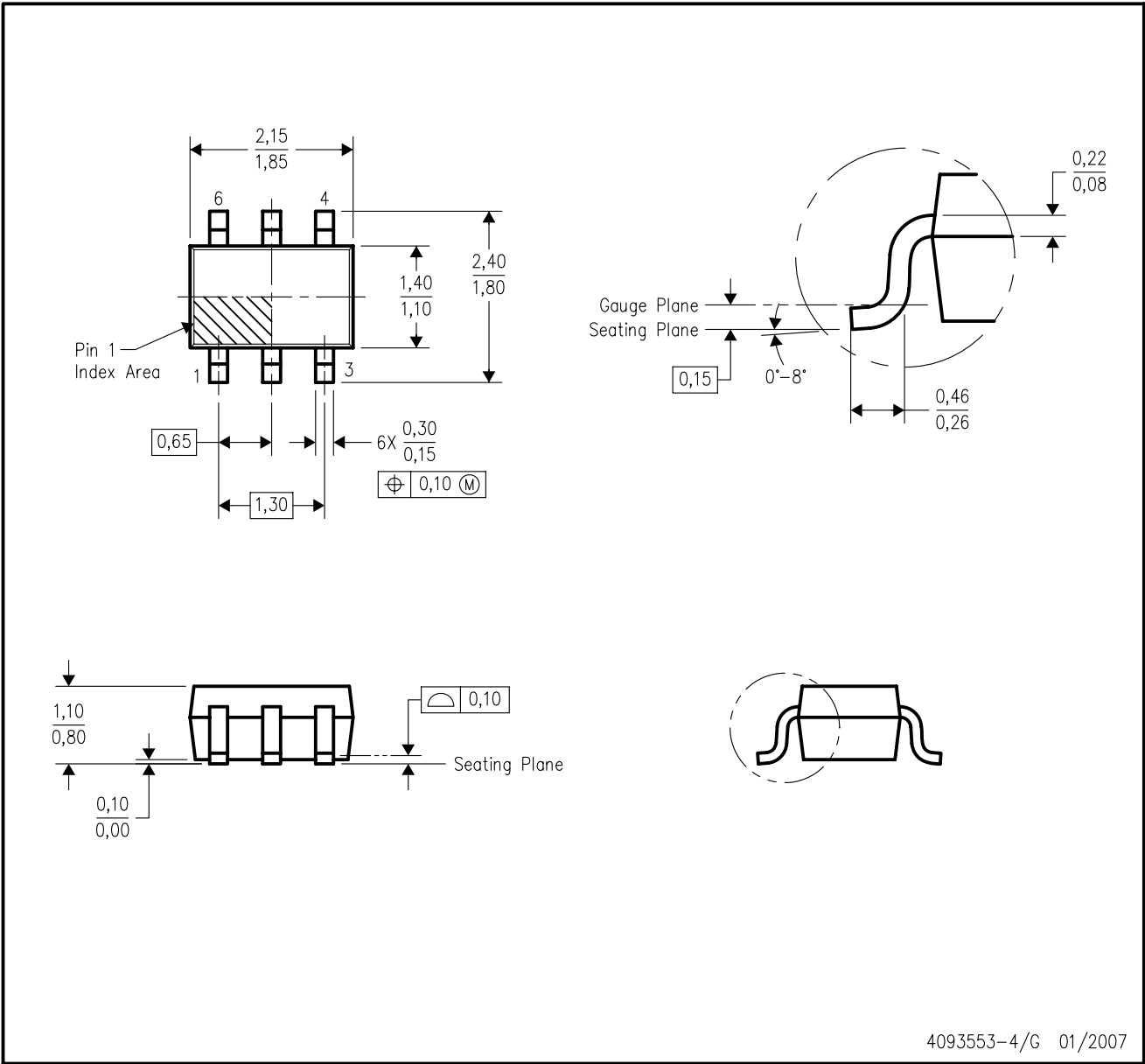


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA360AIDCKR | SC70 | DCK | 6 | 3000 | 195.0 | 200.0 | 45.0 |
| OPA360AIDCKT | SC70 | DCK | 6 | 250 | 195.0 | 200.0 | 45.0 |

DCK (R-PDSO-G6)

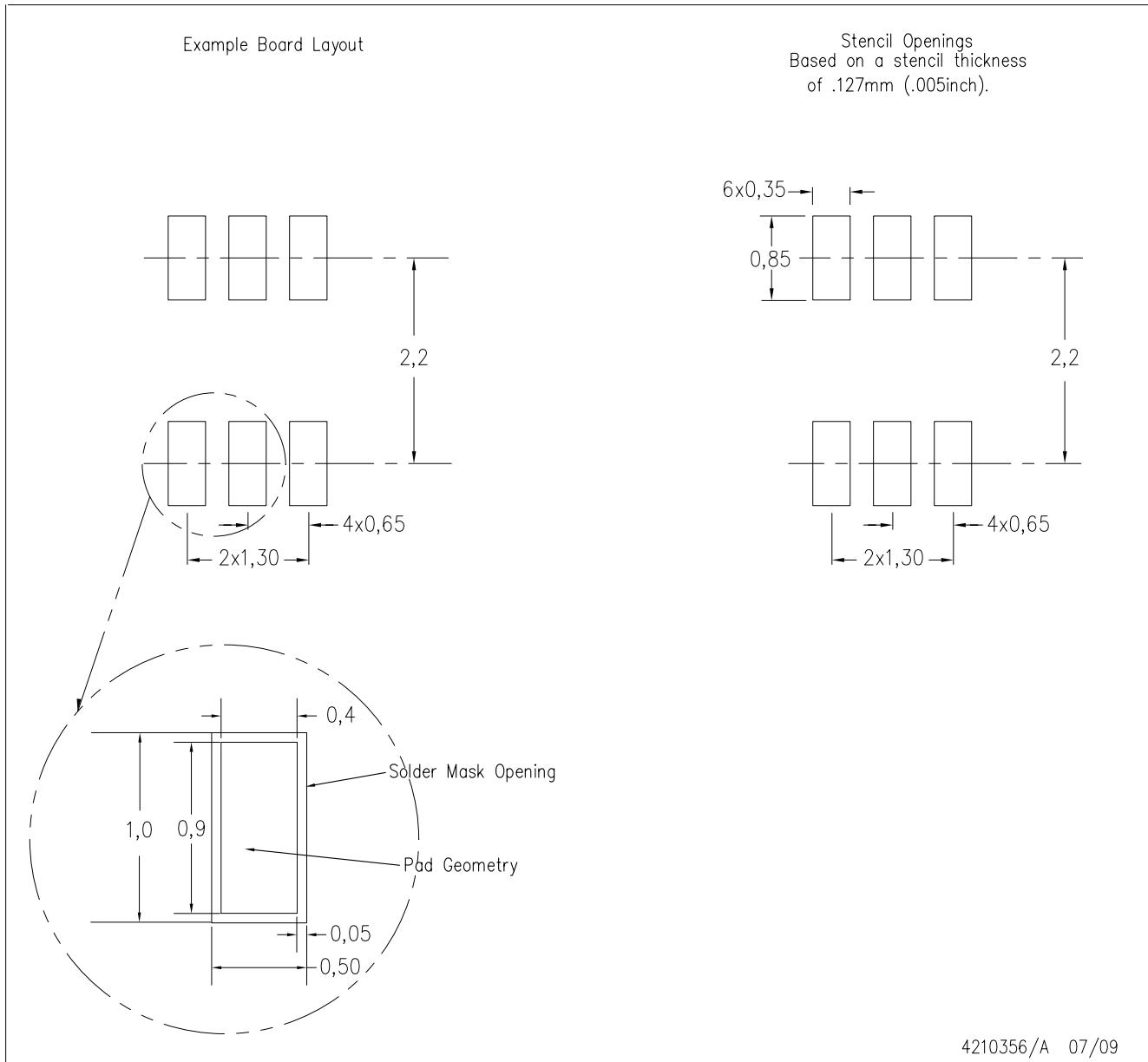
PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| OPA360AIDCKR | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | AUW | Samples |
| OPA360AIDCKT | ACTIVE | SC70 | DCK | 6 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | AUW | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA360AIDCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| OPA360AIDCKR | SC70 | DCK | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| OPA360AIDCKT | SC70 | DCK | 6 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| OPA360AIDCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA360AIDCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| OPA360AIDCKR | SC70 | DCK | 6 | 3000 | 213.0 | 191.0 | 35.0 |
| OPA360AIDCKT | SC70 | DCK | 6 | 250 | 213.0 | 191.0 | 35.0 |
| OPA360AIDCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |

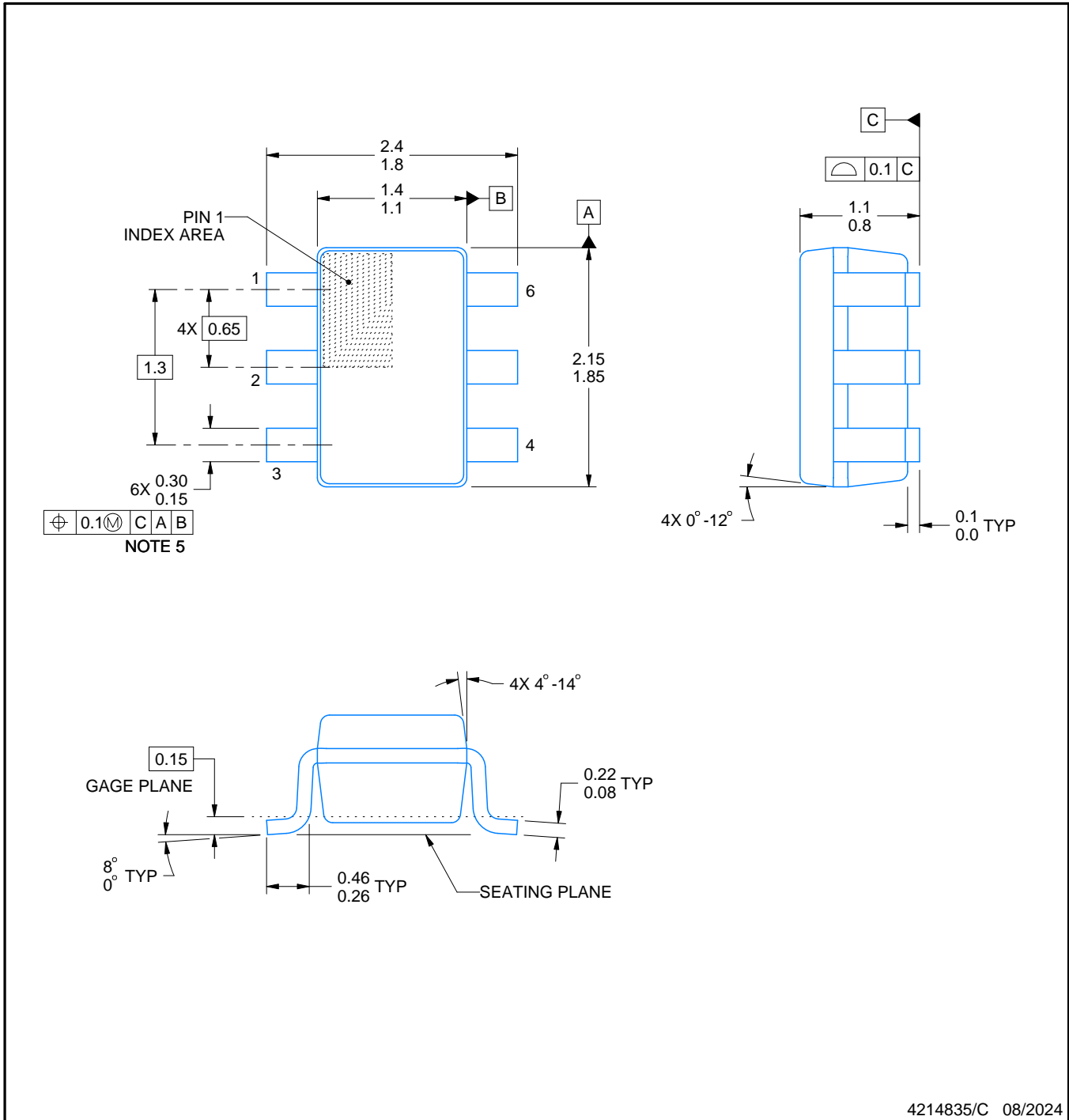
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

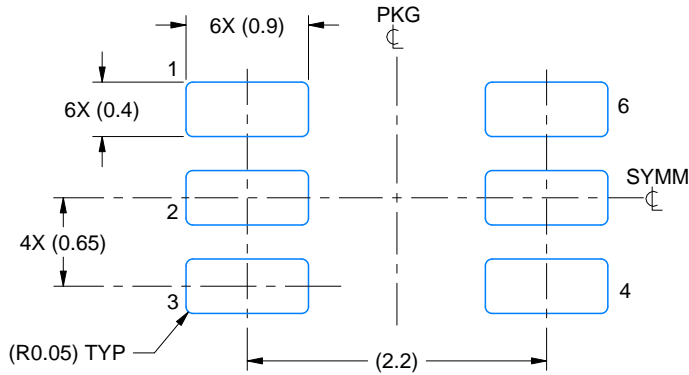
SMALL OUTLINE TRANSISTOR



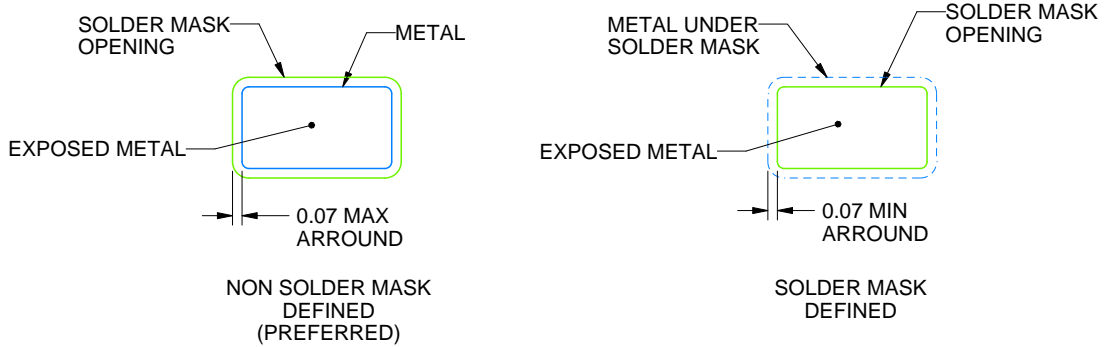
4214835/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

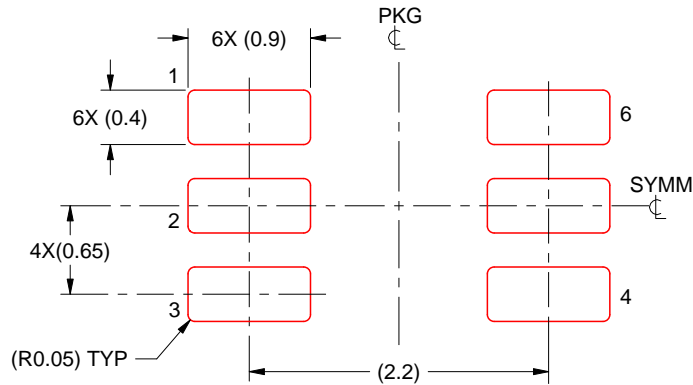


SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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