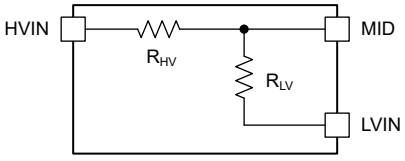
RES60A-Q1 Automotive, 1400V_{DC}, Precision Resistive Divider

1 Features

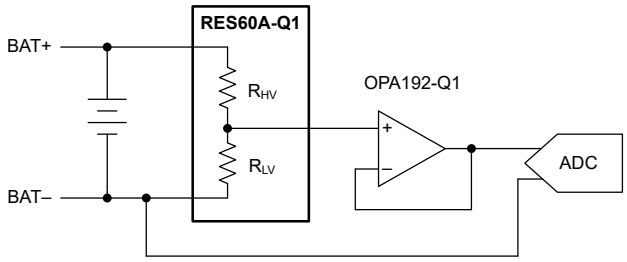
- AEC-Q200 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C
- High voltage rating:
  - Survives 3+ HiPOT tests at 4000V_{DC} (60s)
  - 1700V_{DC} creepage and clearance support between HVIN and LVIN (IEC-61010 PD 2)
- High dc precision with low shift and drift:
  - Initial ratio matching precision: ±0.1% (max)
  - Low drift: ±1ppm/°C (typ)
  - Accurate ±0.2% across aging and temperature
- Low thermal noise (1kHz) thin-film resistors:
  - 30nV/√Hz (210:1 ratio)
  - 25nV/√Hz (310:1 ratio)
  - 22nV/√Hz (410:1 ratio)
  - 20nV/√Hz (500:1 ratio)
  - 18nV/√Hz (610:1 ratio)
  - 14nV/√Hz (1000:1 ratio)

2 Applications

- High-voltage bus and battery voltage monitoring
  - HEV/EV battery management system (BMS)
  - HEV/EV DC/DC converter
  - HEV/EV onboard charger (OBC)
  - HEV/EV inverter and motor control
- Nonisolated, same-ground, always-on dividers
- High common-mode range amplifiers



Functional Block Diagram



Typical Schematic

3 Description

The RES60A-Q1 is a matched resistive divider, implemented in thin-film SiCr with Texas Instruments' modern, high-performance, analog wafer process. A high quality SiO_2 insulative layer encapsulates the resistors and enables usage at extremely high voltages, up to 1400V_{DC} for sustained operation or 4000V_{DC} for HiPOT testing (60s). The device has a nominal input resistance of R_{HV} = 12.5MΩ, and is available in several nominal ratios to meet a wide array of system needs.

The RES60A-Q1 series features high ratio matching precision, with the measured ratio of each divider within ±0.1% (max) of the nominal. This precision is maintained over the specified temperature range and aging, with a cumulative drift of only ±0.2% (max). Therefore, the lifetime tolerance of an uncalibrated RES60A-Q1 remains within a ±0.3% (max) envelope.

The RES60A-Q1 is automotive qualified under AEC-Q200 temperature grade 1, with a specified temperature range from –40°C to +125°C. The device is offered in an 8-pin SOIC package, with nominal body size 7.5mm × 5.85mm, and features creepage and clearance distances of at least 8.5mm between the high-voltage and low-voltage pins.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
RES60A-Q1	DWV (SOIC, 8)	5.85mm × 11.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	NOMINAL RATIO (R_{HV}:R_{LV})
RES60A210-Q1 (1)	210:1
RES60A310-Q1	310:1
RES60A410-Q1	410:1
RES60A500-Q1	500:1
RES60A610-Q1 (1)	610:1
RES60A100-Q1	1000:1

(1) Preview information (not Advanced Information).

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Pin Configuration and Functions

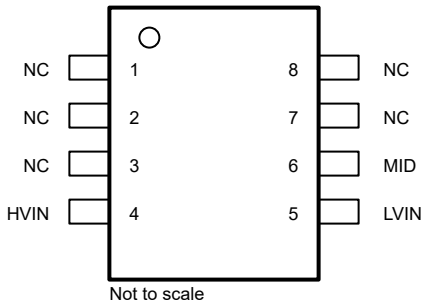


Figure 4-1. DWV Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
HVIN	4	Input	High-voltage input of divider
LVIN	5	Input	Low-voltage input of divider
MID	6	Output	Center tap of divider
NC	1, 2, 3	—	Noninternally-connected pins on high-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.
NC	7, 8	—	Noninternally-connected pins on low-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Maximum short-term overload voltage per divider, $\Delta V = V_{HVIN} - V_{LVIN}$ (100ms, T_A = 25°C)(2) (3)	RES60A210		2700	V
		RES60A310		2700	
		RES60A410		2700	
		RES60A500		2700	
		RES60A610		2700	
		RES60A100		2700	
	Transient high-potential voltage, ac (50Hz, T_A = 25°C)(4) (5) (6)	RES60A210		3000	V_{RMS}
		RES60A310		2500	
		RES60A410		2500	
		RES60A500		3000	
		RES60A610		3000	
		RES60A100		3000	
	Transient high-potential voltage, dc (T_A = 25°C)(4) (5) (6)	RES60A210		4000	V_{DC}
		RES60A310		3500	
		RES60A410		3500	
		RES60A500		4000	
		RES60A610		4000	
		RES60A100		4000	
T_A	Ambient temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	175	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Maximum short-term voltage permitted under transient conditions without performance degradation. Avoid sustained operation at or beyond these voltage levels, especially if the resulting self-heating causes T_J to exceed 150°C.
(3) Tested in production.
(4) Differential voltage from high-voltage domain (pins 1-4) to low-voltage domain (pins 5-8) of the package.
(5) Total stress duration of 180s, accumulated over lifetime in increments of no longer than 60s periods, duty cycle < 10%. Repeated transient high-potential voltage testing can lead to performance degradation or device damage.
(6) Rating for Advanced-Information and preview devices only. Final value for Production-Data devices is pending.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1), all pins except 5 and 6		±4000	V
		Human body model (HBM), per AEC Q100-002(1), pins 5 and 6	RES60A210, RES60A500, RES60A610, RES60A100	±2000	
			RES60A310, RES60A410	±1500	
		Charged device model (CDM), per AEC Q100-011		±1500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ADVANCE INFORMATION

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Maximum sustained dc voltage per divider (HVIN pin to LVIN pin, 10 years at T_A = 25°C)(1)	RES60A210			1400	V_{DC}
		RES60A310			1400	
		RES60A410			1400	
		RES60A500			1400	
		RES60A610			1400	
		RES60A100			1400	
	Maximum sustained 50Hz ac voltage per divider (HVIN pin to LVIN pin, 10 years at T_A = 25°C)(1)	RES60A210			760	V_{RMS}
		RES60A310			760	
		RES60A410			760	
		RES60A500			760	
		RES60A610			760	
		RES60A100			760	
T_A	Ambient temperature		–40		125	°C

(1) Assumes $R_{\theta JA}$ = 111.2°C/W.

5.4 Thermal Information

THERMAL METRIC(1)		RES60A-Q1 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at ΔV = 1000V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RESISTANCE							
R_{HV}	Input resistance				12.5		MΩ
R_{LV}	Ratio-dependent resistance	RES60A210			59.5		kΩ
		RES60A310			40.3		
		RES60A410			30.5		
		RES60A500			25		
		RES60A610			20.5		
		RES60A100			12.5		
G_{nom}	Nominal ratio	R_{HV} / R_{LV}	RES60A210		210		
			RES60A310		310		
			RES60A410		410		
			RES60A500[1]		499.1		
			RES60A610		610		
			RES60A100[2]		997.6		
t_D	Initial ratio tolerance[3]	(R_{HV} / R_{LV}) / G_{nom} – 1[4]	RES60A210			±0.1	%
			RES60A310		±0.03	±0.1	
			RES60A410		±0.02	±0.1	
			RES60A500		±0.02	±0.1	
			RES60A610			±0.1	
			RES60A100		±0.02	±0.1	
	Ratio tolerance drift across operating lifetime[5]	10 years, T_A = –40°C to +85°C, ΔV = 1000V, ($G_{INITIAL}$ – G_{FINAL}) / $G_{INITIAL}$ [4]				±0.2	%
t_{abs}	Absolute tolerance (per resistor)[6]					±15	%
TCR_{ratio}	Temperature coefficient of resistance ratio[3] [5]	T_A = –40°C to +85°C			±1	±5	ppm/°C
		T_A = –40°C to +125°C			±1		
TCR_{abs}	Absolute temperature coefficient of resistance (per resistor)[6] [5]	T_A = –40°C to +125°C			±20		ppm/°C
VCR_{ratio}	Voltage coefficient of resistance ratio				±2		ppm/V

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

at ΔV = 1000V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IMPEDANCE							
C_{IN}	Pin capacitance(7)	HVIN to LVIN			TBD		pF
		MID to LVIN			TBD		
	–3dB bandwidth	$C_{MID\ to\ LVIN}$ = 10pF	RES60A210		268		kHz
			RES60A310		395		
			RES60A410		521		
			RES60A500		637		
			RES60A610		776		
			RES60A100		1270		
t_s	Settling time(5)	To 0.1%, 10V step	RES60A210		TBD		µs
			RES60A310		TBD		
			RES60A410		TBD		
			RES60A500		TBD		
			RES60A610		TBD		
			RES60A100		TBD		
		To 0.01%, 10V step	RES60A210		TBD		µs
			RES60A310		TBD		
			RES60A410		TBD		
			RES60A500		TBD		
			RES60A610		TBD		
			RES60A100		TBD		
e_N	Thermal noise density(7)	f = 1kHz	RES60A210		30		nV/√Hz
			RES60A310		25		
			RES60A410		22		
			RES60A500		20		
			RES60A610		18		
			RES60A100		14		

(1) For Advanced-Information devices, the typical value is 499.1. For Production-Data devices, this value will be 500.
(2) For Advanced-Information devices, the typical value is 997.6. For Production-Data devices, this value will be 1000.
(3) R_{HV} / R_{LV} vs nominal ratio.
(4) The specification is the result of this expression, given as a percentage (multiplied by 100%)
(5) Specified by characterization.
(6) R_{HV} and R_{LV} vs nominal values.
(7) Specified by design.

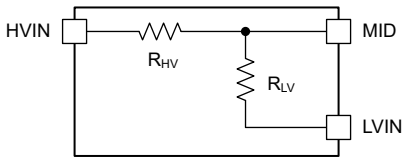
ADVANCE INFORMATION

6 Detailed Description

6.1 Overview

The RES60A-Q1 consists of two, precision, thin-film SiCr resistors, arranged to form a matched divider and encapsulated by an insulative SiO_2 layer. The device contains an *input* resistor, R_{HV}, that is nominally 12.5MΩ. The device also incorporates a *gain* resistor, R_{LV}, with a value that depends on the nominal ratio (R_{HV} / R_{LV}) of the RES60A-Q1.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Ratiometric Matching

The resistors of the RES60A-Q1 are described by the following two equations:

$$R_{HV} = R_{HVnom} \times (1 \pm t_{abs}) = R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr}) \quad (1)$$

$$R_{LV} = R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr}) \quad (2)$$

where

- R_{HVnom} and R_{LVnom} are the nominal values of each resistor.
- t_{abs} is an error term that describes the absolute tolerance of the resistors of the RES60A-Q1, such that $|t_{abs}| \leq 15\%$.
- t_{SiCr} is the variation in the SiCr resistivity for a wafer, and dominates the absolute tolerance for a given resistor. The two resistors of a given RES60A-Q1 are interdigitated and come from the same area of the wafer; therefore, t_{SiCr} is effectively the same for both of the two resistors, although t_{SiCr} varies on a part-to-part basis. When the divider is considered in ratiometric terms, these error terms drop out; see the following equations.
- t_{RHV} and t_{RLV} are localized per-resistor variation or offset error terms. These terms describe the remaining effective tolerances of the respective resistors for a given RES60A-Q1 device, after accounting for the universal t_{SiCr}.

$$\frac{R_{HV}}{R_{LV}} = \frac{R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}{R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr})} = \frac{R_{HVnom} \times (1 \pm t_{RHV})}{R_{LVnom} \times (1 \pm t_{RLV})} = G_{nom} \times \frac{(1 \pm t_{RHV})}{(1 \pm t_{RLV})} = G \quad (3)$$

$$\frac{R_{HV}}{R_{LV} + R_{HV}} = \frac{R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}{R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr}) + R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})} = \frac{R_{HVnom} \times (1 \pm t_{RHV})}{R_{LVnom} \times (1 \pm t_{RLV}) + R_{HVnom} \times (1 \pm t_{RHV})} \quad (4)$$

The RES60A-Q1 is specified with a maximum initial divider ratio tolerance of 0.1%, meaning that the relationship between the actual divider ratio, G, and the nominal ratio, G_{nom}, of a given divider is described by the following:

$$G = G_{nom} \times (1 \pm t_D) \quad (5)$$

such that $t_D \leq 0.1\%$. Because any devices that do not meet these criteria are screened out at final test, these equations can be used with the previous equations to prove the effective bounds of t_{RHV} and t_{RLV}. Therefore, despite the device absolute end-to-end tolerance bounds of ±15%, the effective error tolerances of each resistor (for ratiometric applications) are within approximately ±0.05%, for the worst-case t_{RHV} and t_{RlV}.

ADVANCE INFORMATION

6.3.2 Ultra-Low Noise

Noise in resistors can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or 1/f noise, is extremely important for systems that require signal gain at frequencies less that 100Hz. The flicker noise for thin-film resistors, including the RES60A-Q1, is lower than that of thick-film resistor processes. Thermal noise typically dominates in the region greater than 1kHz, and increases as resistor magnitude increases. Noise is modeled as a voltage source in series with the resistor.

For a resistive divider such as the RES60A-Q1, the thermal noise as measured at the center tap of two resistors R_{HV} and R_{LV} is equivalent to the thermal noise of a resistor with value $R_{HV} \parallel R_{LV}$:

$$e_N = \sqrt{(4k_B TR)} \tag{6}$$

where:

- e_N is the thermal noise density in nV/√Hz
- T is the absolute temperature in kelvins (K)
- k_B is the Boltzmann constant, 1.381 × 10-23 J/K
- $R = R_{HV} \parallel R_{LV}$

$R_{HV} >> R_{LV}$; therefore, $R \approx R_{LV}$. As an example, for the RES60A610-Q1:

$$e_N = \sqrt{(4k_B TR)} = \sqrt{4 \times 1.38E^{-23} \frac{J}{K} \times 278K \times (12.5M\Omega \parallel 20.49k\Omega)} = 18nV/\sqrt{Hz} \tag{7}$$

6.4 Device Functional Modes

The RES60A-Q1 features a single pad for the HVIN pin and two pads for the MID and LVIN pins, with all other pads and pins electrically floating. Connect both the MID and LVIN pins to the *low-voltage domain* of the system, such as a microcontroller ADC input and chassis ground, respectively. Bias the HVIN pin to the high potential of the measured system, such as the high side of the battery stack.

HVIN and LVIN can be used to measure directly between the high side and low side of the battery. However, to avoid an overvoltage condition, verify that the downstream circuitry driven by MID is properly referenced to the low side (LVIN).

ADVANCE INFORMATION

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Battery Stack Measurement

The RES60A-Q1 can be used in conjunction with an automotive precision amplifier, such as the OPA192-Q1, for single-ended measurement of the high side (BAT+) of an EV battery relative to a fixed potential. For those systems where BAT– and GND are equivalent, as in Figure 7-1 (a), the configuration shown in Figure 7-2 applies. An alternative approach is to measure directly across the battery from BAT+ to BAT–, as shown in Figure 7-3. This approach is useful for systems referenced to the low side of the battery, BAT–, as in Figure 7-1 (b).

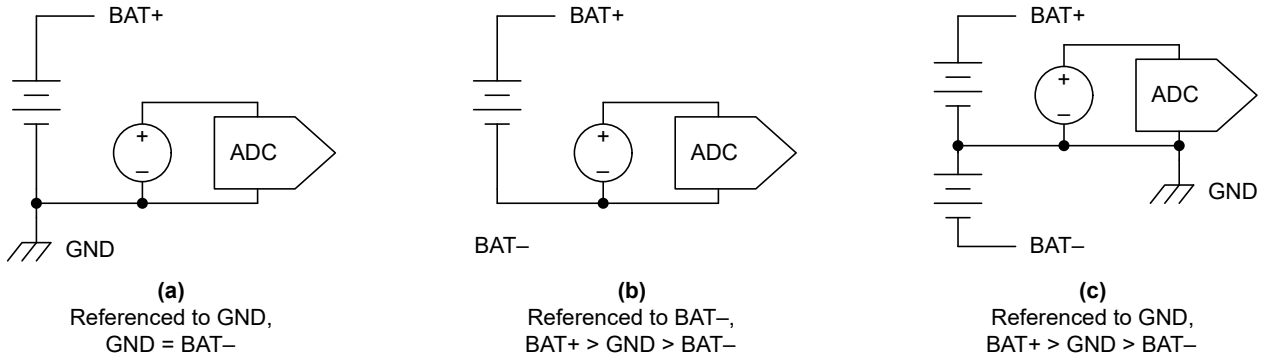


Figure 7-1. Common Battery and System Configurations

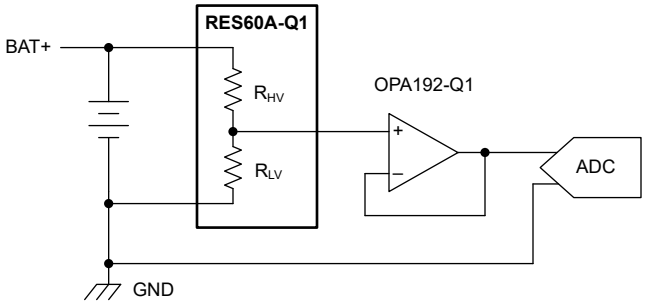


Figure 7-2. Single-Ended Measurement, BAT+ to GND

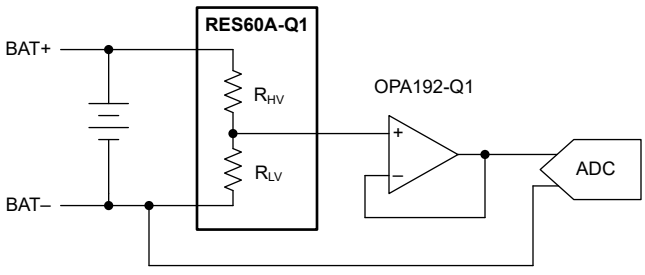


Figure 7-3. Single-Ended Measurement, BAT+ to BAT–

ADVANCE INFORMATION

For some system architectures, BAT– floats relative to the chassis GND; see also Figure 7-1 (c). If for example a microcontroller referenced to chassis ground needs to measure the voltage across the entire battery stack, a difference amplifier can be constructed using two RES60A-Q1 devices and an OPA192-Q1. Figure 7-4 shows this approach. If two ADC channels are available, two single-ended measurements can be done using two RES60A-Q1 devices and an OPA2192-Q1.

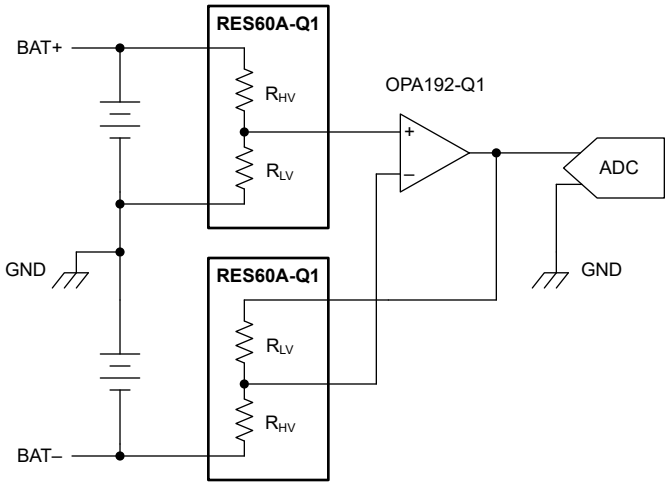


Figure 7-4. Differential Measurement, BAT+ to BAT–

Leakage in the system and quiescent current from the amplifier input reduce the precision of the measurement. In some cases, a guard buffer can be used to reduce leakage currents. Follow best practices to reduce board contamination and leakage.

For an 800V single-ended battery measurement (see also Figure 7-2), the static current through the divider is:

$$I_{STATIC} = \frac{V_{BATT}}{(R_{HV} + R_{LV})} = \frac{800V}{(12.5M\Omega + 20.49k\Omega)} = 63.9\mu A \quad (8)$$

Therefore, the buffer amplifier used must have a low bias current, such that $I_B << I_{STATIC}$. The low bias current of the OPA192-Q1 (5pA typical at 25°C, 5nA maximum from –40°C to +125°C) makes the device an excellent choice for this role.

ADVANCE INFORMATION

7.2 Typical Application

The RES60A-Q1 can be configured with an isolated amplifier such as the AMC1311B-Q1 for measurements requiring reinforced isolation. Figure 7-5 shows an example circuit configuration for such an application, where the RES60A-Q1 attenuates the input voltage and the AMC1311B-Q1 crosses the isolation barrier. A discrete difference amplifier with RES11A-Q1 and OPA388-Q1 is used to adapt the differential output voltage of the AMC1311B-Q1 for use with a single-ended 5V ADC.

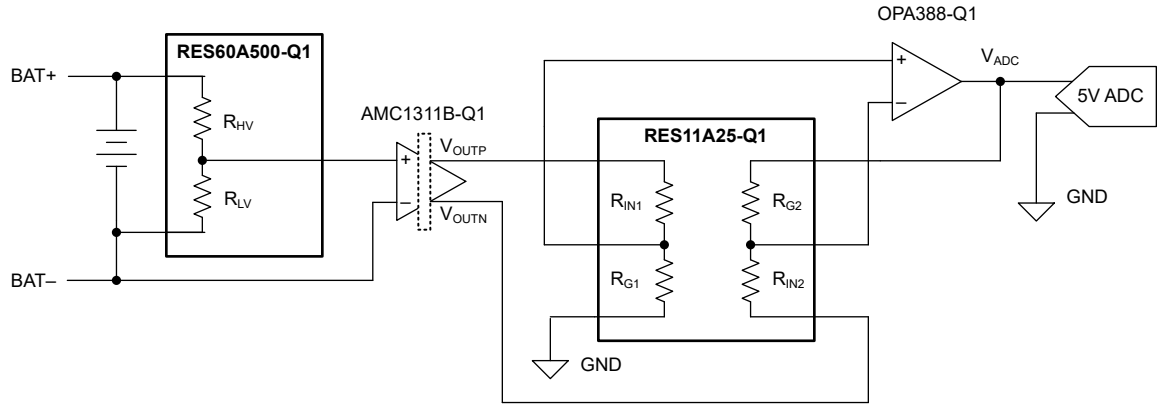


Figure 7-5. DC Bus Measurement With the RES60A-Q1 and AMC1311B-Q1

7.2.1 Design Requirements

PARAMETER	DESIGN GOAL
DC bus voltage range	0V to 1000V
Output (V_{ADC}) full-scale range	0V to 5V
Attenuation (nominal ratio)	500:1
Uncalibrated initial measurement error	±0.5% FSR

7.2.2 Detailed Design Procedure

This design attenuates the high common-mode voltage of the bus to a level that falls within the linear input range of the AMC1311B-Q1. Some key possible circuit error sources can be considered as follows:

- The AMC1311B-Q1 has a typical input bias current of 3.5nA. With R_{LV} = 25kΩ, this input bias current manifests appears as an 88µV offset error at MID. When this offset is calculated in a root-sum-of-squares with the 400µV typical input offset voltage of the AMC1311B-Q1, a 410µV offset results. This offset represents 0.0205% of the 2V full-scale range, and is typically not the dominating error factor.
- The gain error and integrated nonlinearity error of the AMC1311B-Q1 can be approximated using the Isolated Amplifier Voltage Sensing Excel Calculator. For this example, the typical FSR error is calculated as 0.06%.
- The typical initial ratiometric gain tolerance of the RES60A500-Q1 is 0.02%, which sums with the previously mentioned errors of the AMC1311B-Q1 in a root-sum-of-squares manner to give a total typical FSR error of 0.066%.
- The level-shifting circuit introduces additional errors, and applies a gain factor to the previously discussed errors. However, due to the low offset of the OPA388-Q1 and high precision of the RES11A-Q1, these errors (0.012% FSR) are low enough to not significantly impact the final typical error.

The final calculated result of 0.068% typical FSR error represents a 1σ value, so a ±6σ estimate gives ±0.41% FSR error. The results suggest the circuit meets the ±0.5% FSR application requirement, with margin.

ADVANCE INFORMATION

7.2.3 Application Curves

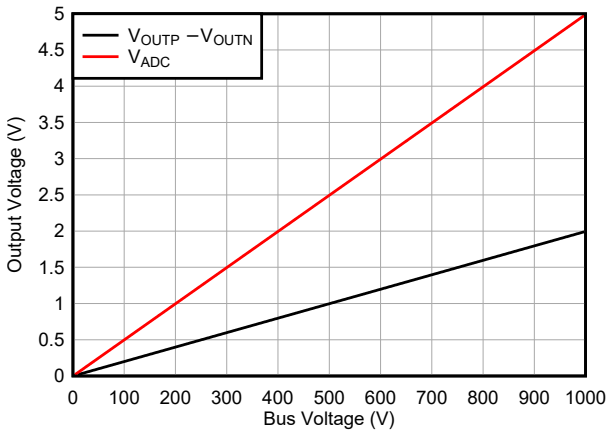


Figure 7-6. Transfer Function

7.3 Power Supply Recommendations

The RES60A-Q1 is a high-voltage resistor divider, with no active circuitry or protective diodes. There are no specific power-supply connection requirements other than respecting the limits expressed in *Absolute Maximum Ratings* and *Recommended Operating Conditions*. To provide additional protection against high-edge-rate transient events, use a high-voltage capacitor at the device input. Be aware that additional input capacitance extends step-response settling times. A TVS diode at the MID pin provides additional protection against fast transients for downstream low-voltage circuitry, if necessary.

ADVANCE INFORMATION

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running sensitive traces, such as the MID connection, as far away from supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Make sure supply voltages are adequately filtered.
- Power dissipated in the RES60A-Q1 causes the junction temperature to rise. For reliable operation, junction temperature must be limited to 150°C, maximum. Maintaining a lower junction temperature results in higher reliability.
  - Package thermal resistance, $R_{\theta JA}$, is affected by mounting techniques and environments. Poor air circulation can significantly increase thermal resistance to the ambient environment. Best thermal performance is achieved by soldering the RES60A-Q1 onto a circuit board with wide printed circuit traces, especially for the LVIN connection, to allow greater conduction through the device leads.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process.
  - A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
- Use conformal coating or potting, the deposition of an insulating polymer or other material layer over an assembled PCB, to reduce the pollution degree around the RES60A-Q1. This process reduces the requirements for creepage and clearance distances by eliminating or reducing the influence of pollutants.
- Use groove cutting to attain a lower PCB creepage distance. For grooves wider than 1mm, the effective creepage distance is the existing creepage distance plus the width of the groove and twice the depth of the groove. This sum must equal or exceed the required creepage distance. The groove must not weaken the substrate to the point of failure to meet mechanical test requirements. All layers under the groove must be free from traces, vias, and pads to maintain the maximum creepage distance.

7.4.2 Layout Example

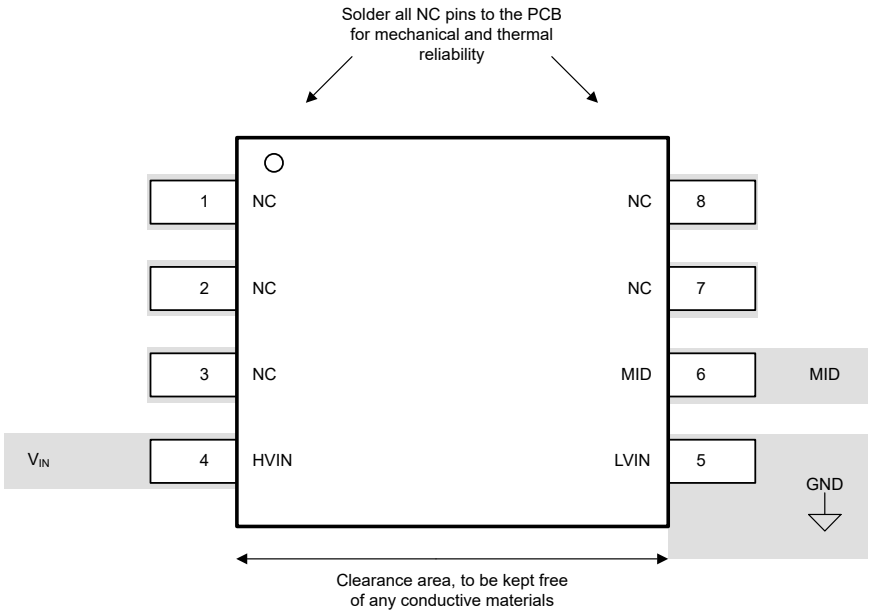


Figure 7-7. Layout Example

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.1.1.3 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

8.1.1.4 Analog Filter Designer

Available as a web-based tool from the Design and simulation tool web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *What Are Creepage And Clearance?* TI Precision Labs video
- Texas Instruments, *RES11A-Q1 Automotive, Low-Noise, Precision, Matched, Thin-Film Resistor Pairs* data sheet
- Texas Instruments, *RES60EVM* evaluation module

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial Draft

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XRES60A100QDWVRQ1	ACTIVE	SOIC	DWV	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XRES60A310QDWVRQ1	ACTIVE	SOIC	DWV	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XRES60A410QDWVRQ1	ACTIVE	SOIC	DWV	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XRES60A500QDWVRQ1	ACTIVE	SOIC	DWV	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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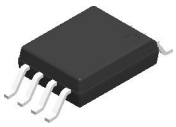
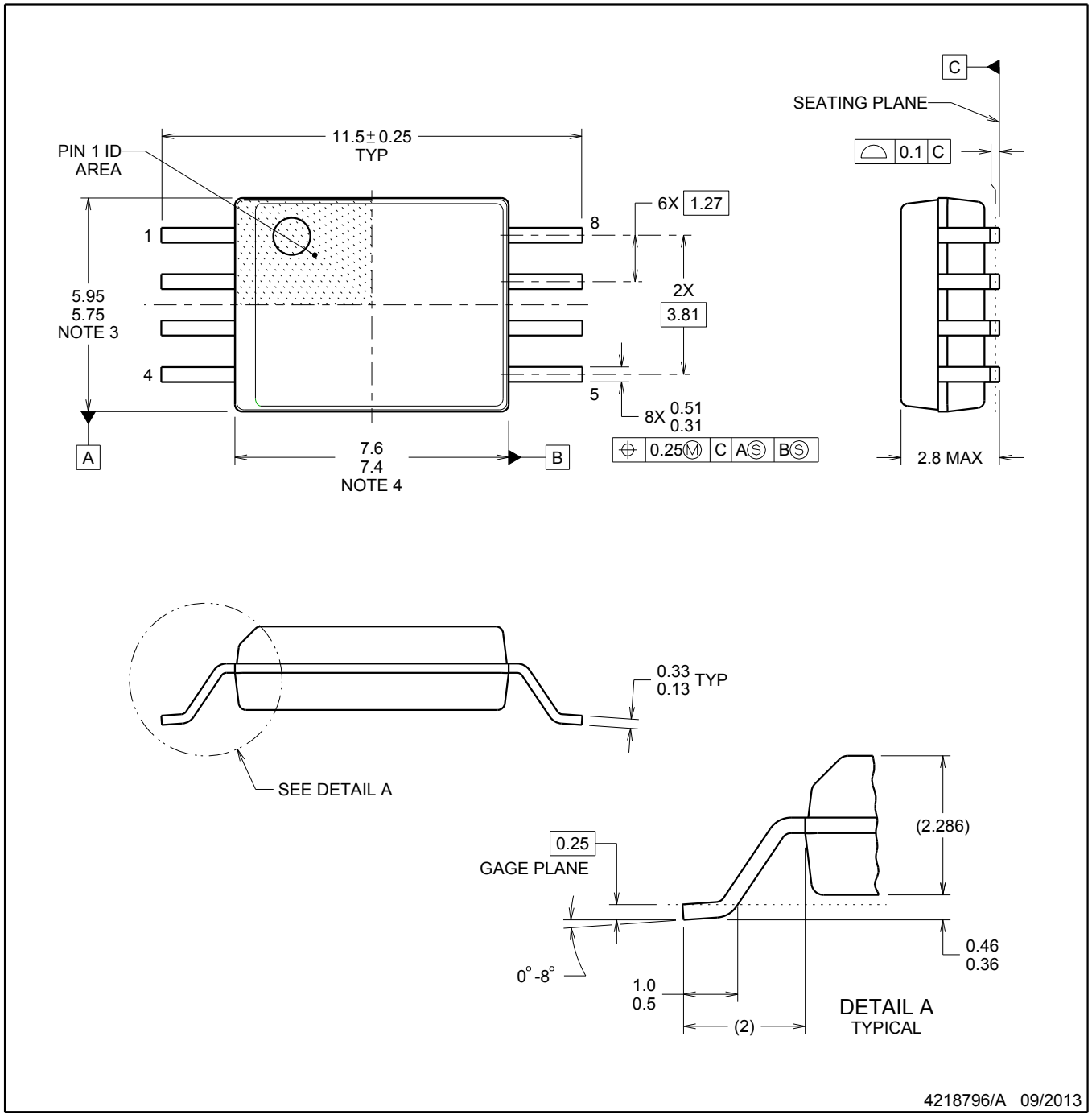


DWV0008A

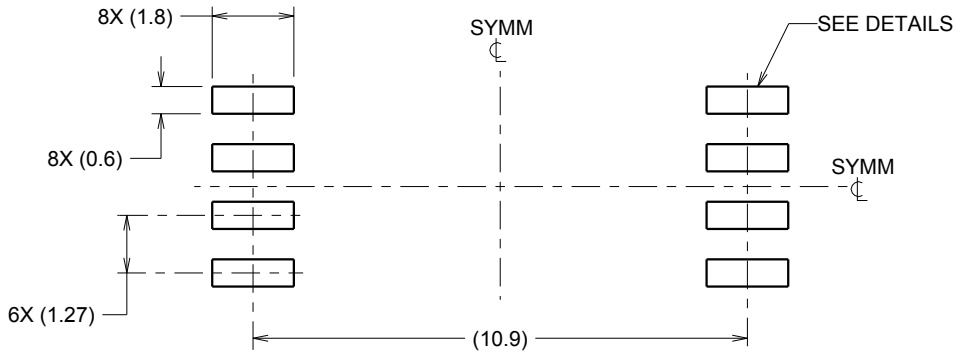
SOIC - 2.8 mm max height

SOIC

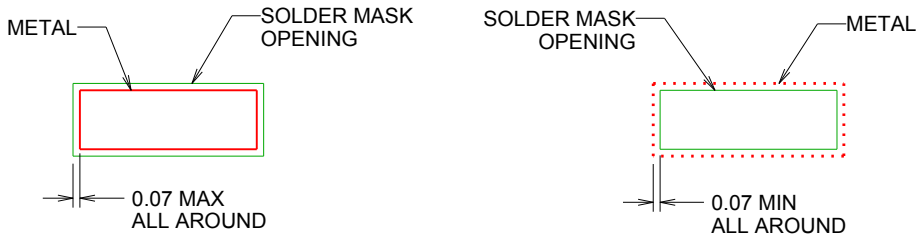


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

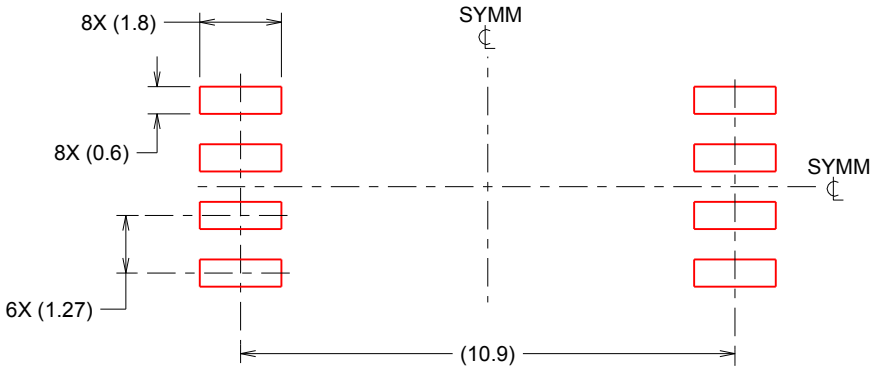
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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