SN74ACT08-Q1 Automotive Quadruple 2-Input AND Gates With TTL-Compatible Inputs

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Operating voltage range of 4.5V to 5.5V
- TTL-compatible inputs
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Fast operation with delay of 10ns max (V_{CC} = 5V, C_L = 50pF)

2 Applications

- Combine power good signals
- Combine enable signals

3 Description

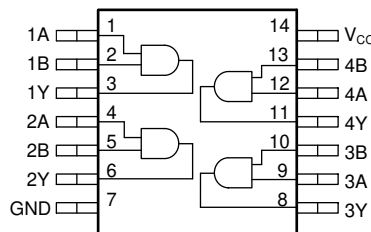The SN74ACT08-Q1 contains four independent 2-input AND gates.

Package Information

PART NUMBER	PACKAGE [1]	PACKAGE SIZE[2]	BODY SIZE [3]
SN74ACT08-Q1	PW (TSSOP, 14)	6.4mm × 4.4mm	5mm × 4.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
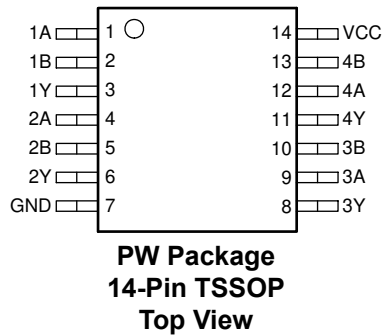(3) The body size (length × width) is a nominal value and does not include pins.

Logic Diagram (Positive Logic)

Table of Contents

4 Pin Configuration and Functions

```
           ┌───────○───────┐
    1A  ▭──┤ 1          14 ├──▭  VCC
    1B  ▭──┤ 2          13 ├──▭  4B
    1Y  ▭──┤ 3          12 ├──▭  4A
    2A  ▭──┤ 4          11 ├──▭  4Y
    2B  ▭──┤ 5          10 ├──▭  3B
    2Y  ▭──┤ 6           9 ├──▭  3A
   GND  ▭──┤ 7           8 ├──▭  3Y
           └───────────────┘
```

PW Package
14-Pin TSSOP
Top View

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
1Y	3	O	Channel 1, Output Y
2A	4	I	Channel 2, Input A
2B	5	I	Channel 2, Input B
2Y	6	O	Channel 2, Output Y
GND	7	G	Ground
3Y	8	O	Channel 3, Output Y
3A	9	I	Channel 3, Input A
3B	10	I	Channel 3, Input B
4Y	11	O	Channel 4, Output Y
4A	12	I	Channel 4, Input A
4B	13	I	Channel 4, Input B
V_{CC}	14	P	Positive Supply

(1)   Signal types: I = input, O = output, I/O = input or output, P = power, G = ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range[2]		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range[2]		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous output current through V_{CC} or GND			±200	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	4.5V ≤ V_{CC} ≤ 5.5V	2		V
V_{IL}	Low-Level input voltage	4.5V ≤ V_{CC} ≤ 5.5V		0.8	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current	4.5V ≤ V_{CC} ≤ 5.5V		-24	mA
I_{OL}	Low-level output current	4.5V ≤ V_{CC} ≤ 5.5V		24	mA
Δt/Δv	Input transition rise or fall rate	4.5V ≤ V_{CC} ≤ 5.5V		20	ns/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

	THERMAL METRIC[1]		PW (TSSOP)	UNIT
			14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance		145.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		76.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		102.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		18.8	°C/W

THERMAL METRIC[1]		PW (TSSOP)	UNIT
		14 PINS	
Ψ_{JB}	Junction-to-board characterization parameter	100.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\mu A$	4.5V	4.4	4.49		4.4			V
		5.5V	5.4	5.49		5.4			
	$I_{OH} = -24mA$	4.5V	3.94			3.7			
	$I_{OH} = -24mA$	5.5V	4.86			4.7			
	$I_{OH} = -50mA$	5.5V				3.85			
	$I_{OH} = -75mA$	5.5V				3.85			
V_{OL}	$I_{OH} = 50\mu A$	4.5V		0.001	0.1			0.1	V
		5.5V		0.001	0.1			0.1	
	$I_{OH} = 24mA$	4.5V			0.36			0.5	
	$I_{OH} = 24mA$	5.5V			0.36			0.5	
	$I_{OH} = 50mA$	5.5V						1.65	
	$I_{OH} = 75mA$	5.5V						1.65	
I_I	$V_I = 5.5V$ or GND	0V to 5.5V			±0.1			±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5V			2			80	μA
ΔI_{CC}	$V_I = V_{CC} - 2.1V$; Any Input	4.5V to 5.5V		0.6	1.2			1.5	mA
C_I	$V_I = V_{CC}$ or GND	5V		8					pF
C_{PD} [1] [2]	$C_L = 50pF$, F = 1MHz	5V		14					pF

(1) C_{PD} is used to determine the dynamic power consumption, per channel
(2) $P_D = V_{CC}^2 x F_I x (C_{PD} + C_L)$ where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage

5.6 Switching Characteristics

$C_L = 50pF$; over operating free-air temperature range; typical values measured at $T_A = 25°C$ (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A or B	Y	5V	1	6.5	9	1		10	ns
t_{PHL}			5V	1	6.5	9	1		10	ns
t_r		Y	5V		2.4	3.9	3		4.6	ns
t_f			5V		2.3	3.4	2.6		4.1	ns

5.7 Typical Characteristics

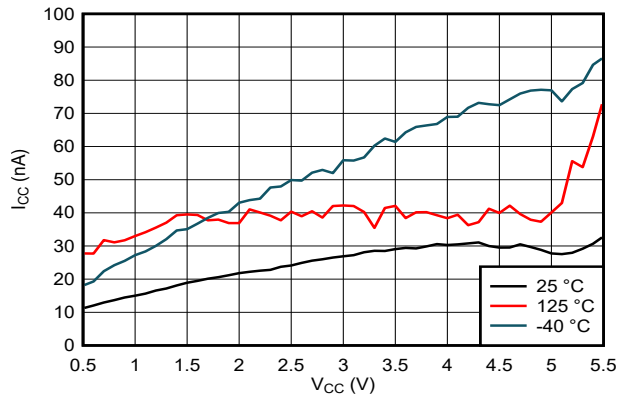$T_A = 25°C$ (unless otherwise noted)

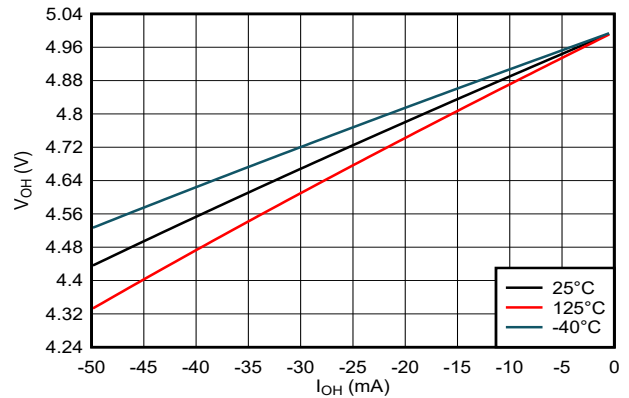**Figure 5-1. Supply Current Across Supply Voltage**

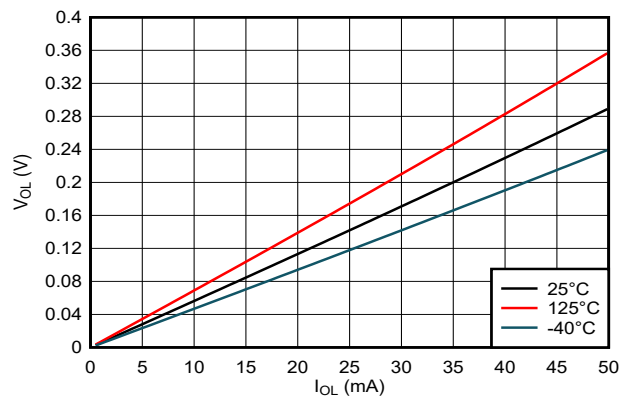**Figure 5-2. Output Voltage vs Current in HIGH State; 5V Supply**

Figure 5-3. Output Voltage vs Current in LOW State; 5V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O = 50\Omega$, $t_t < 2.5$ns, $V_t = 1.5$V. For push-pull outputs, $R_L = 500\Omega$.

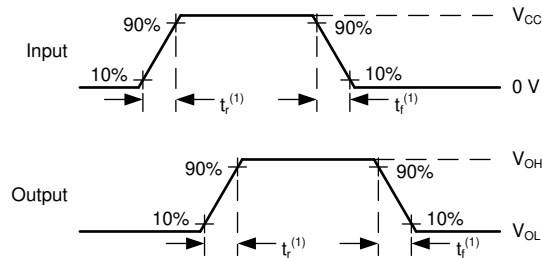The outputs are measured individually with one input transition per measurement.
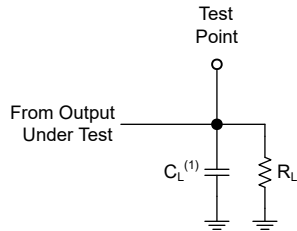
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs
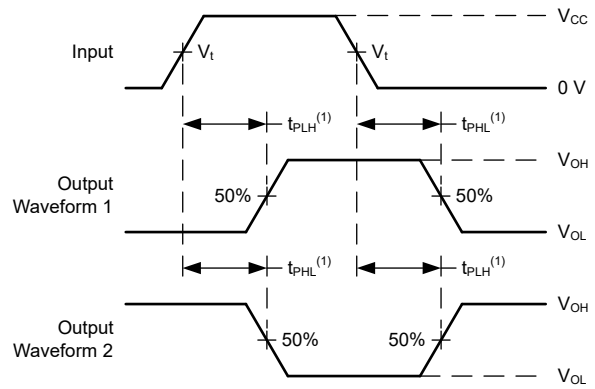
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays

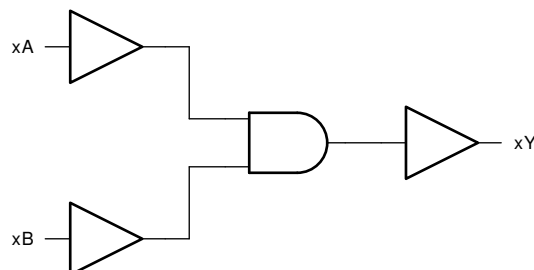(1) The greater between t_r and t_f is the same as t_t.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

This device contains four independent 2-input AND Gates. Each gate performs the Boolean function Y = A ● B in positive logic.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

7.3.3 Clamp Diode Structure

As shown in Figure 7-1, the inputs and outputs to this device have both positive and negative clamping diodes.

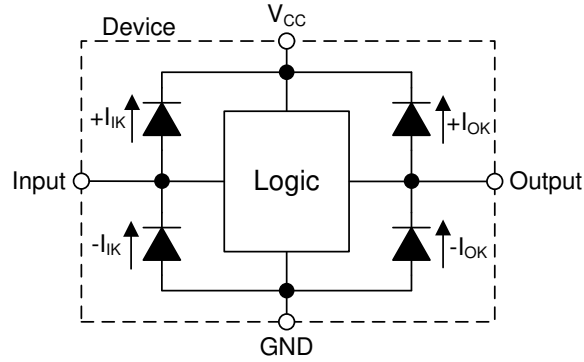| **CAUTION** |
|---|
| Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed. |

Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74ACT08-Q1.

Table 7-1. Function Table

INPUTS[1]		OUTPUT Y
A	**B**	
H	H	H
L	X	L
X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in *Figure 8-1*. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

This device is used to directly control the RESET pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.
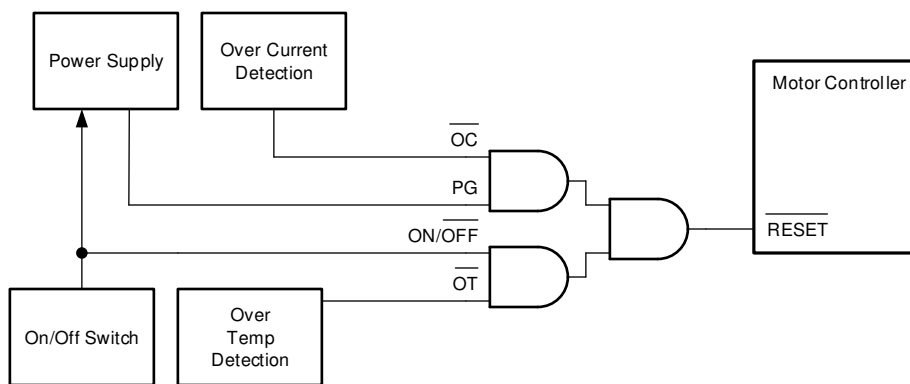
8.2 Typical Application

Figure 8-1. Typical application schematic

Product Folder Links: *SN74ACT08-Q1*

8.3 Design Requirements

8.3.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74ACT08-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74ACT08-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74ACT08-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74ACT08-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

> **CAUTION**
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.3.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74ACT08-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74ACT08-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.3.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74ACT08-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.
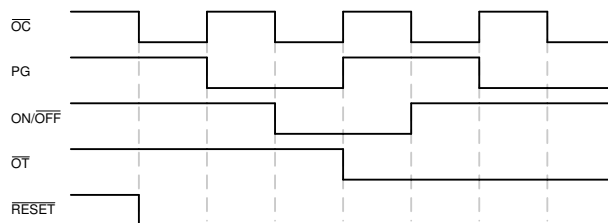
8.5 Application Curves

Figure 8-2. Typical application timing diagram

8.6 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.7 Layout

8.7.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.
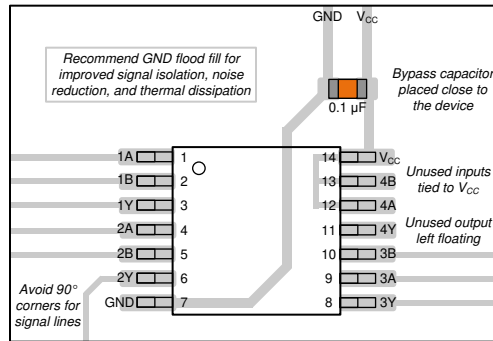
8.7.2 Layout Example

Figure 8-3. Example Layout for the SN74ACT08-Q1

Product Folder Links: *SN74ACT08-Q1*

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

![ESD warning symbol]

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.
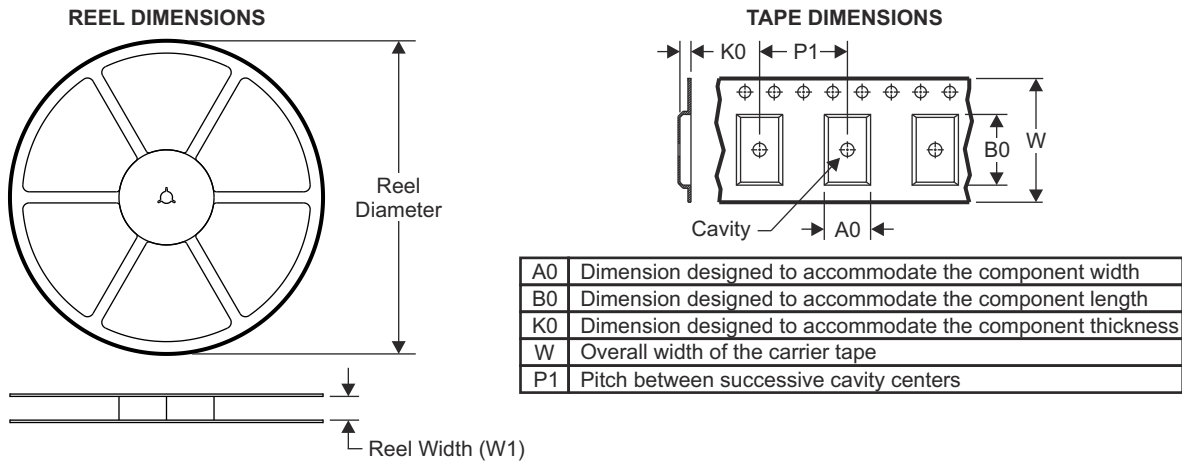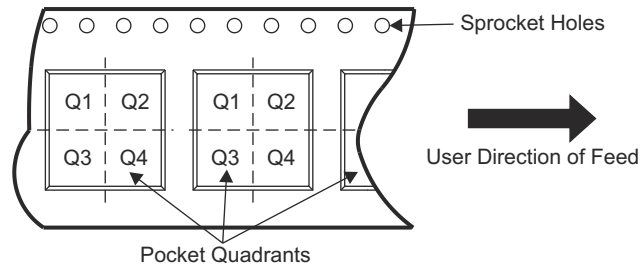
10 Revision History

Changes from Revision * (March 2024) to Revision A (December 2024)   **Page**
• Changed from Advance Information to Production Data..1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PSN74ACT08PWRQ1	TSSOP	PW	14	3000	330	12.4	6.90	5.60	1.60	8	12	Q1

TAPE AND REEL BOX DIMENSIONS

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PSN74ACT08PWRQ1	TSSOP	PW	14	3000	356	356	35

11.2 Mechanical Data

PWP0014G

PACKAGE OUTLINE

PowerPAD ™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE
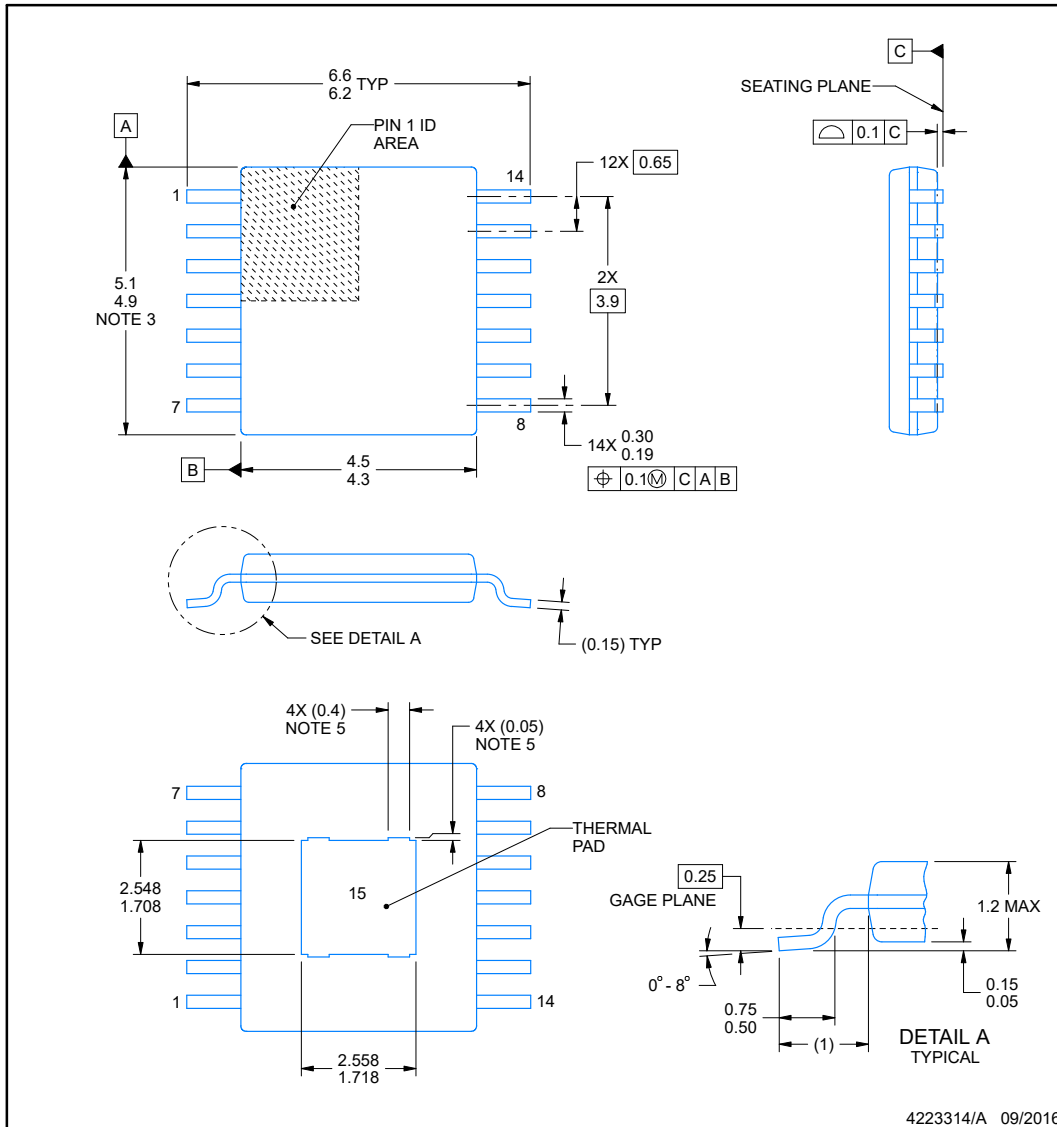
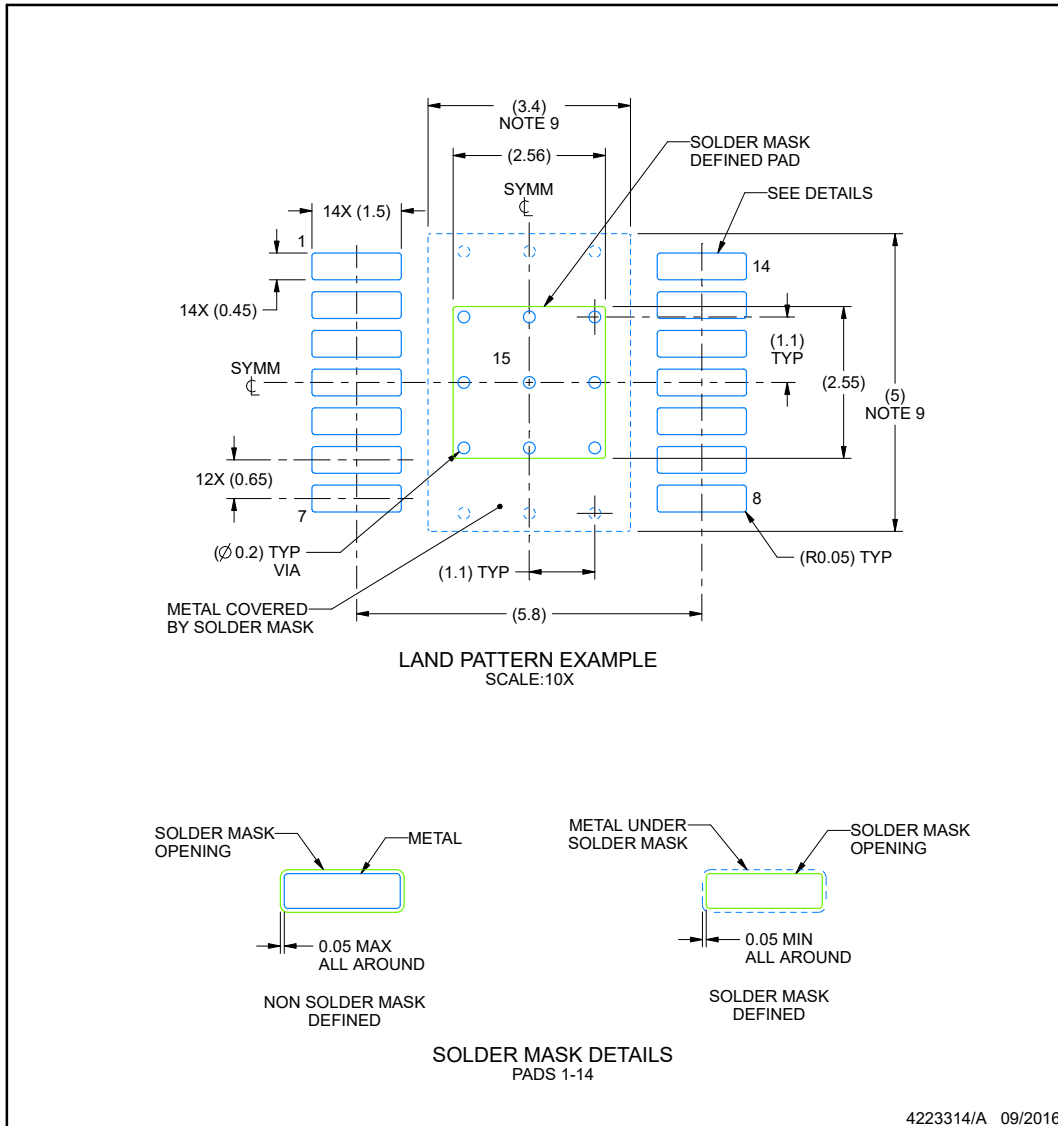4223314/A   09/2016

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

Product Folder Links: *SN74ACT08-Q1*

EXAMPLE BOARD LAYOUT

PWP0014G

PowerPAD ™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

LAND PATTERN EXAMPLE
SCALE:10X

(3.4) NOTE 9
(2.56)
SYMM
SOLDER MASK DEFINED PAD
SEE DETAILS
14X (1.5)
1
14X (0.45)
14
SYMM
15
(1.1) TYP
(2.55)
(5) NOTE 9
12X (0.65)
7
8
(Ø 0.2) TYP VIA
(1.1) TYP
(R0.05) TYP
METAL COVERED BY SOLDER MASK
(5.8)

SOLDER MASK DETAILS
PADS 1-14

SOLDER MASK OPENING
METAL
0.05 MAX ALL AROUND
NON SOLDER MASK DEFINED

METAL UNDER SOLDER MASK
SOLDER MASK OPENING
0.05 MIN ALL AROUND
SOLDER MASK DEFINED

4223314/A   09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

TEXAS INSTRUMENTS
www.ti.com

Product Folder Links: SN74ACT08-Q1

EXAMPLE STENCIL DESIGN

PWP0014G

PowerPAD ™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.86 X 2.85
0.125	2.56 X 2.55 (SHOWN)
0.15	2.34 X 2.33
0.175	2.16 X 2.16

4223314/A   09/2016
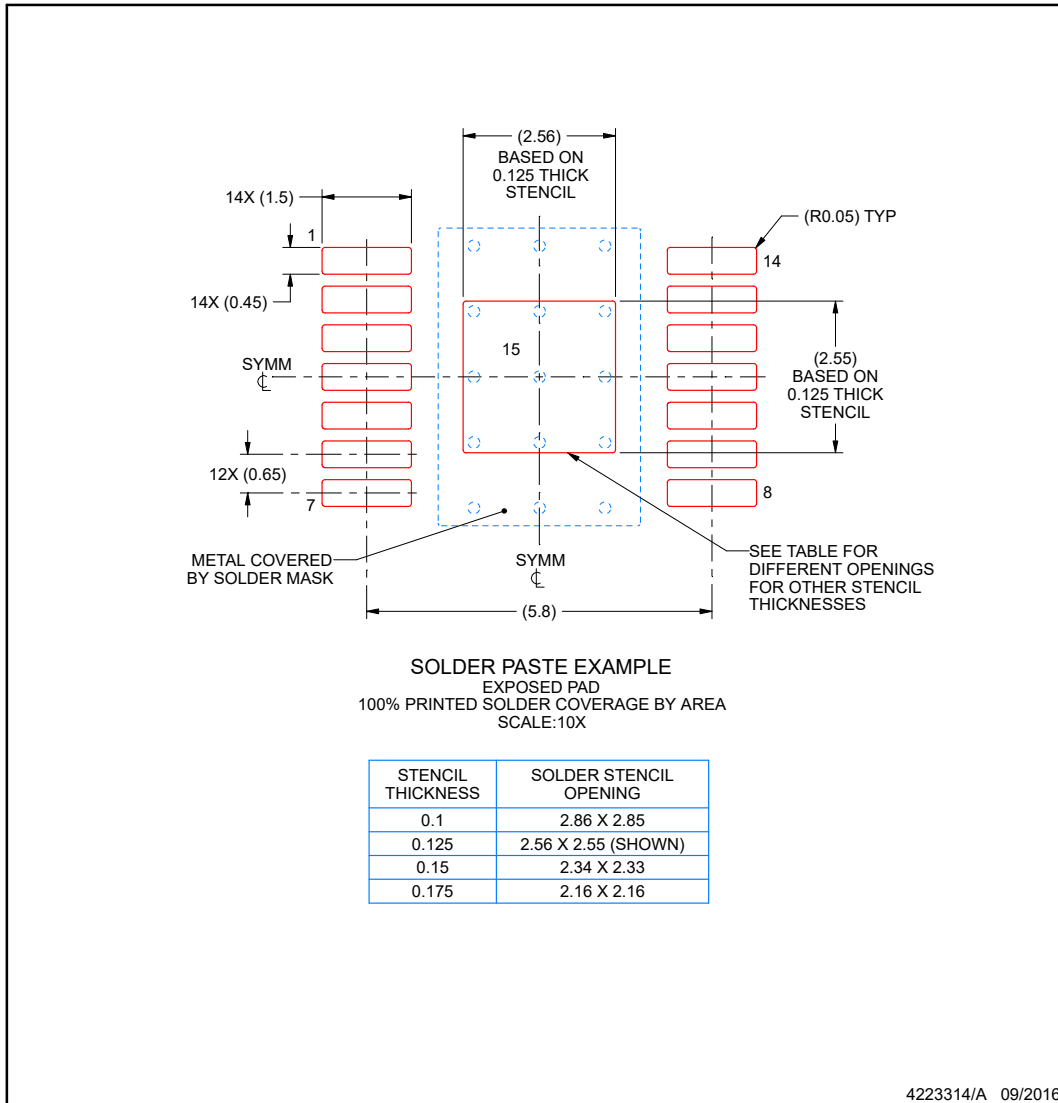
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

TEXAS INSTRUMENTS
www.ti.com

Submit Document Feedback

Product Folder Links: *SN74ACT08-Q1*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PSN74ACT08PWRQ1	ACTIVE	TSSOP	PW	14	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ACT08-Q1 :

- Catalog : SN74ACT08

- Enhanced Product : SN74ACT08-EP

- Military : SN54ACT08

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

IMPORTANT NOTICE AND DISCLAIMER