TCAN1044-Q1 Automotive Fault-Protected CAN FD Transceiver With 1.8V I/O Support

1 Features

- AEC-Q100: Qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C T_A
- Meets the requirements of ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Support of classical CAN and optimized CAN FD performance at 2, 5, and 8Mbps
  - Short and symmetrical propagation delays for enhanced timing margin
  - Higher data rates in loaded CAN networks
- I/O voltage range supports 1.7V to 5.5V
  - Support for 1.8V, 2.5V, 3.3V, and 5V applications
- Protection features:
  - Bus fault protection: ±58V
  - Undervoltage protection
  - TXD dominant timeout (DTO)
    - Data rates down to 9.2kbps
  - Thermal-shutdown protection (TSD)
- Operating modes:
  - Normal mode
  - Low power standby mode supporting remote wake-up request
- Optimized behavior when unpowered
  - Bus and logic pins are high impedance (no load to operating bus or application)
  - Hot-plug capable: power up/down glitch free operation on bus and RXD output
- Junction temperatures from: –40°C to 150°C
- Receiver common mode input voltage: ±12V
- Available in SOIC (8), SOT23 (8) packages and leadless VSON (8) packages with improved automated optical inspection (AOI) capability

2 Applications

- Automotive and Transportation
  - Body control modules
  - Automotive gateway
  - Advanced driver assistance system (ADAS)
  - Infotainment

3 Description

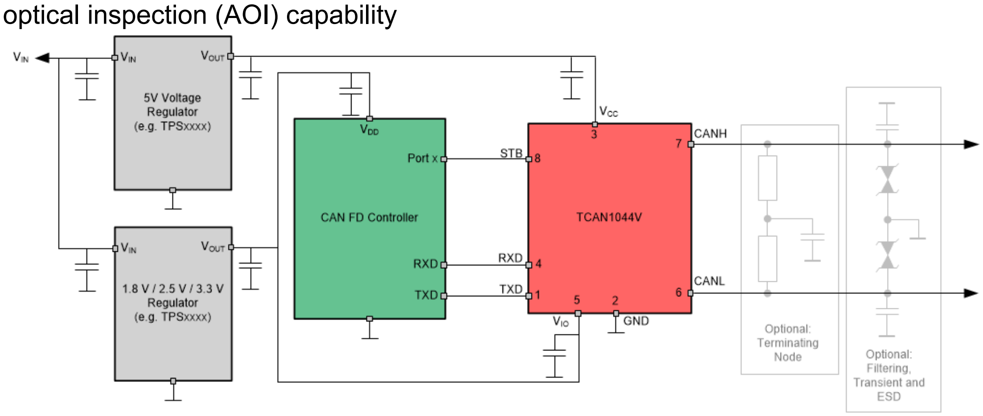
The TCAN1044-Q1 is a high speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification.

The TCAN1044-Q1 transceiver supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps). The TCAN1044-Q1 includes internal logic level translation via the V_{IO} terminal to allow for interfacing the transceiver I/Os directly to 1.8V, 2.5V, 3.3V, or 5V logic I/Os. The transceiver supports a low-power standby mode and wake over CAN compliant to the ISO 11898-2:2016 defined wake-up pattern (WUP). The TCAN1044-Q1 transceiver also includes protection and diagnostic features supporting thermal-shutdown (TSD), TXD-dominant time-out (DTO), supply undervoltage detection, and bus fault protection up to ±58V.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN1044-Q1	SOT (DDF, 8)	2.9mm x 2.8mm
	VSON (DRB, 8)	3mm x 3mm
	SOIC (D, 8)	4.9mm x 6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

1 Features.....1
2 Applications.....1
3 Description.....1
4 Pin Configuration and Functions.....3
5 Specifications.....4
5.1 Absolute Maximum Ratings.....4
5.2 ESD Ratings.....4
5.3 ESD Ratings.....4
5.4 Recommended Operating Conditions.....4
5.5 Thermal Characteristics.....5
5.6 Supply Characteristics.....5
5.7 Dissipation Ratings.....6
5.8 Electrical Characteristics.....7
5.9 Switching Characteristics.....8
5.10 Typical Characteristics.....10
6 Parameter Measurement Information.....11
7 Detailed Description.....14
7.1 Overview.....14
7.2 Functional Block Diagram.....15
7.3 Feature Description.....16
7.4 Device Functional Modes.....20
8 Application and Implementation.....23
8.1 Application Information.....23
8.2 Typical Application.....23
8.3 System Examples.....26
8.4 Power Supply Recommendations.....26
8.5 Layout.....26
9 Device and Documentation Support.....28
9.1 Receiving Notification of Documentation Updates.....28
9.2 Support Resources.....28
9.3 Trademarks.....28
9.4 Electrostatic Discharge Caution.....28
9.5 Glossary.....28
10 Revision History.....28
11 Mechanical, Packaging, and Orderable Information.....29

4 Pin Configuration and Functions

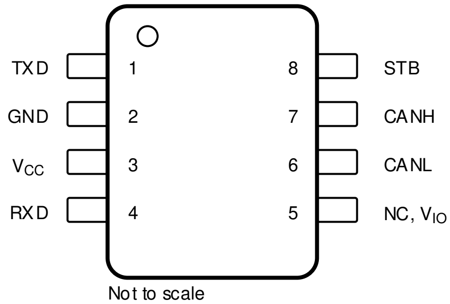


Figure 4-1. DDF Package, 8-Pin SOT (Top View)

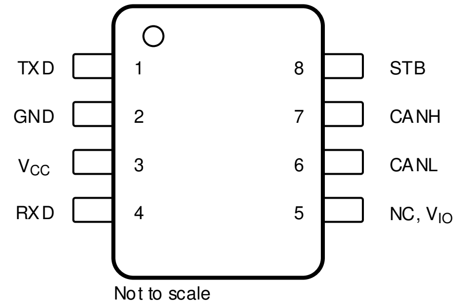


Figure 4-2. D Package, 8-Pin SOIC (Top View)

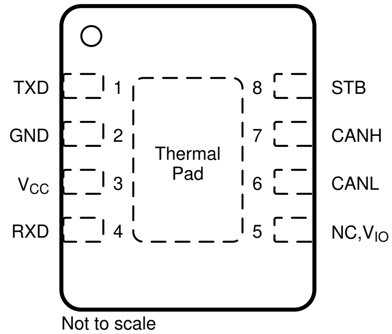


Figure 4-3. DRB Package, 8-Pin VSON (Top View)

Table 4-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD	1	Digital Input	CAN transmit data input
GND	2	GND	Ground connection
V_{CC}	3	Supply	5V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-state when powered off
NC	5	—	No Connect (not internally connected); Devices without V_{IO}
V_{IO}		Supply	I/O supply voltage
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby input for mode control, integrated pull up
Thermal Pad (VSON only)		—	Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus IO voltage CANH and CANL	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL	–45	45	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Operating virtual junction temperature range	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential IO bus voltages, are with respect to ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	HBM classification level 3A for all pins	±3000	V
			HBM classification level 3B for global pins CANH & CANL	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings

				VALUE	UNIT
V_{ESD}	System Level Electro-Static Discharge (ESD)[(3)]	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10650 Powered Contact Discharge	±8000	V
			SAE J2962-2 per ISO 10650 Powered Air Discharge	±15000	V
V_{Tran}	ISO 7637 ISO Pulse Transients[(1)]	CAN bus terminals (CANH, CANL)	Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	ISO 7637 Slow transients pulse[(2)]	CAN bus terminals (CANH, CANL) to GND	DCC slow transient pulse	±85	V

(1) Tested according to IEC 62228-3:2019 CAN Transceivers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(2) Tested according to ISO 7637-3 (2017); Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
(3) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for I/O level shifter	1.7		5.5	V
$I_{OH(RXD)}$	RXD terminal high level output current	–2			mA
$I_{OL(RXD)}$	RXD terminal low level output current			2	mA
T_A	Operating ambient temperature	–40		125	°C

5.5 Thermal Characteristics

THERMAL METRIC[1]		TCAN1044x-Q1			UNIT
		D (SOIC)	DDF (SOT)	DRB (VSON)	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	128.1	119.9	49.9	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	61.8	58.2	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	71.6	39.7	23.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	2.1	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.8	39.5	23.8	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	–	6.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Supply Characteristics

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current Normal mode	Dominant	TXD = 0 V, STB = 0 V, R_L = 60 Ω, C_L = open See Figure 6-1		45	70	mA
			TXD = 0 V, STB = 0 V, R_L = 50 Ω, C_L = open See Figure 6-1		49	80	mA
		Recessive	TXD = V_{CC}, STB = 0 V, R_L = 50 Ω, C_L = open See Figure 6-1		4.5	7.5	mA
		Dominant with bus fault	TXD = 0 V, STB = 0 V, CANH = CANL = ±25 V, R_L = open, C_L = open See Figure 6-1			130	mA
I_{CC}	Supply current Standby mode Devices with V_{IO}		TXD = STB = V_{IO}, R_L = 50 Ω, C_L = open See Figure 6-1		0.2	1	µA
I_{CC}	Supply current Standby mode Devices without V_{IO}		TXD = STB = V_{CC}, R_L = 50 Ω, C_L = open See Figure 6-1			14.5	µA
I_{IO}	I/O supply current Normal mode	Dominant	TXD = 0 V, STB= 0 V RXD floating		125	300	µA
I_{IO}	I/O supply current Normal mode	Recessive	TXD = 0 V, STB = 0 V RXD floating		25	48	µA
I_{IO}	I/O supply current Standby mode		TXD = 0 V, STB = V_{IO} RXD floating		8.5	13.5	µA
UV_{VCC}	Rising under voltage detection on V_{CC} for protected mode				4.2	4.4	V
UV_{VCC}	Falling under voltage detection on V_{CC} for protected mode			3.5	4	4.25	V
UV_{VIO}	Rising under voltage detection on V_{IO} (Devices with V_{IO})				1.56	1.65	V
UV_{VIO}	Falling under voltage detection on V_{IO} (Devices with V_{IO})			1.4	1.51	1.59	V

5.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 1.8 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		110		mW
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		110		mW
		V_{CC} = 5 V, V_{IO} = 5 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		110		mW
		V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_A= 125°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_A= 125°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 5 V, T_A= 125°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

5.8 Electrical Characteristics

Over recommended operating conditions with T_A = -40°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage Normal mode	CANH	TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open See Figure 6-2 and Figure 7-3 ,	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage Normal mode	CANH and CANL	TXD = V_{IO} , STB = 0 V, R_L = open (no load), R_{CM} = open See Figure 6-2 and Figure 7-3	2	0.5 V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		STB = 0 V, R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = open, R_{CM} = open, TXD = 250 kHz, 1 MHz, 2.5 MHz See Figure 6-2 and Figure 8-2	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		STB = 0 V, R_L = 60 Ω, C_L = open See Figure 6-2 and Figure 7-3	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Normal mode Dominant	CANH - CANL	TXD = 0 V, STB = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open See Figure 6-2 and Figure 7-3	1.5		3	V
			TXD = 0 V, STB = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open See Figure 6-2 and Figure 7-3	1.4		3.3	V
			TXD = 0 V, STB = 0 V, R_L = 2240 Ω, C_L = open See Figure 6-2 and Figure 7-3	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Normal mode Recessive	CANH - CANL	TXD = V_{IO} , STB = 0 V, R_L = 60 Ω, C_L = open See Figure 6-2 and Figure 7-3	–120		12	mV
			TXD = V_{IO} , STB = 0 V, R_L = open, C_L = open See Figure 6-2 and Figure 7-3	–50		50	mV
$V_{O(STB)}$	Bus output voltage Standby mode	CANH	STB = V_{IO} , R_L = open (no load) See Figure 6-2 and Figure 7-3	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant Normal mode		STB = 0 V, $V_{(CANH)}$ = -15 V to 40 V, CANL = open, TXD = 0 V See Figure 6-7 and Figure 7-3	–115			mA
			STB = 0 V, $V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open, TXD = 0 V See Figure 6-7 and Figure 7-3			115	mA
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive Normal mode		STB = 0 V, –27 V ≤ V_{BUS} ≤ 32 V, where V_{BUS} = CANH = CANL, TXD = V_{IO} See Figure 6-7 and Figure 7-3	–5		5	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage Normal mode		STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3, Table 6-1, and Table 7-6	500		900	mV
$V_{IT(STB)}$	Input threshold Standby mode		STB = V_{IO} , -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3, Table 6-1, and Table 7-6	400		1150	mV
V_{DOM}	Dominant state differential input voltage range Normal mode		STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3, Table 6-1, and Table 7-6	0.9		9	V
V_{REC}	Recessive state differential input voltage range Normal mode		STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3, Table 6-1, and Table 7-6	-4		0.5	V
$V_{DOM(STB)}$	Dominant state differential input voltage range Standby mode		STB = V_{IO} , -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3, Table 6-1, and Table 7-6	1.15		9	V
$V_{REC(STB)}$	Recessive state differential input voltage range Standby mode		STB = V_{IO} , -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3, Table 6-1, and Table 7-6	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold Normal mode		STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V See Figure 6-3, Table 6-1, and Table 7-6		100		mV
V_{CM}	Common mode range Normal and standby modes		See Figure 6-3 and Table 7-6 Table 7-6	–12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current		CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	µA

5.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance to ground (CANH or CANL)	$TXD = V_{IO}$ (1)			20	pF
C_{ID}	Differential input capacitance				10	pF
R_{ID}	Differential input resistance	$TXD = V_{IO}$ (1), STB = 0 V, -12 V ≤ V_{CM} ≤ 12 V	40		90	kΩ
R_{IN}	Single ended input resistance (CANH or CANL)		20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)} = V_{(CAN\_L)}$ = 5 V	–1%		1%	
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	$TXD = V_{CC} = V_{IO}$ = 5.5 V	–2.5	0	1	μA
I_{IL}	Low-level input leakage current	TXD = 0 V, $V_{CC} = V_{IO}$ = 5.5 V	–200	-100	–20	μA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, $V_{CC} = V_{IO}$ = 0 V	–1	0	1	μA
C_I	Input Capacitance	$V_{IN} = 0.4×\sin(2×\pi×2×10^6×t)+2.5$ V		5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	I_O = –2 mA, Devices without V_{IO} See Figure 6-3	0.8 V_{CC}			V
V_{OH}	High-level output voltage	I_O = –2 mA, Devices with V_{IO} See Figure 6-3	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	I_O = 2 mA, Devices without V_{IO} See Figure 6-3			0.2 V_{CC}	V
V_{OL}	Low-level output voltage	I_O = –2 mA, Devices with V_{IO} See Figure 6-3			0.2 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V, $V_{CC} = V_{IO}$ = 0 V	–1	0	1	μA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V, $V_{CC} = V_{IO}$ = 0 V	–1	0	1	μA

(1) $V_{IO} = V_{CC}$ in non-V variants of device

5.9 Switching Characteristics

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

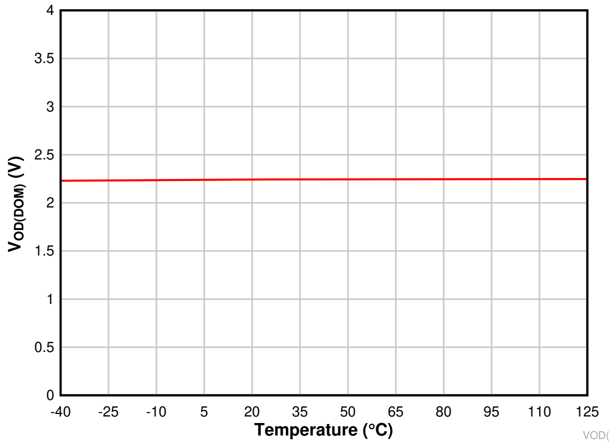
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF V_{IO} = 2.8 V to 5.5 V See Figure 6-4		125	210	ns
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF V_{IO} = 1.7 V See Figure 6-4		165	255	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF V_{IO} = 2.8 V to 5.5 V See Figure 6-4		150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	Normal mode, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF V_{IO} = 1.7 V See Figure 6-4		180	255	ns

5.9 Switching Characteristics (continued)

Over recommended operating conditions with T_A = -40℃ to 125℃ (unless otherwise noted)

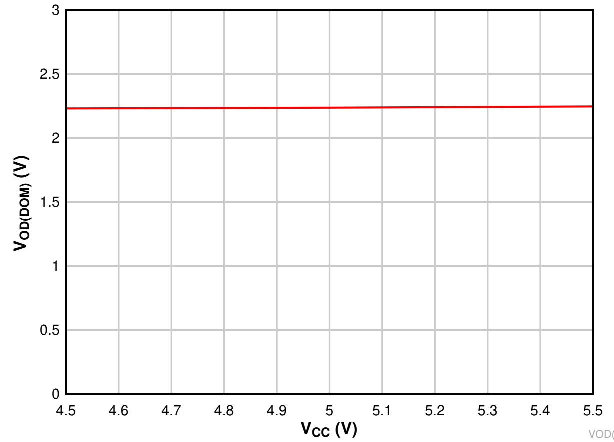
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See Figure 6-5			20	μs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See Figure 7-5	0.5		1.8	μs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout	See Figure 7-5	0.8		6	ms
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	STB = 0 V, R_L = 60 Ω, C_L = 100 pF See Figure 6-2 and Figure 6-6		80		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			20		ns
t_R	Differential output signal rise time			30		ns
t_F	Differential output signal fall time			50		ns
t_{TXD_DTO}	Dominant timeout		1.2		4.0	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	STB = 0 V, $C_{L(RXD)}$ = 15 pF See Figure 6-3		90		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			65		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 500 ns	STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See Figure 6-4	450		530	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 200 ns		155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins $t_{BIT(TXD)}$ = 500 ns		400		550	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins $t_{BIT(TXD)}$ = 200 ns		120		220	ns
t_{REC}	Receiver timing symmetry $t_{BIT(TXD)}$ = 500 ns		-50		20	ns
t_{REC}	Receiver timing symmetry $t_{BIT(TXD)}$ = 200 ns		-45		15	ns

5.10 Typical Characteristics



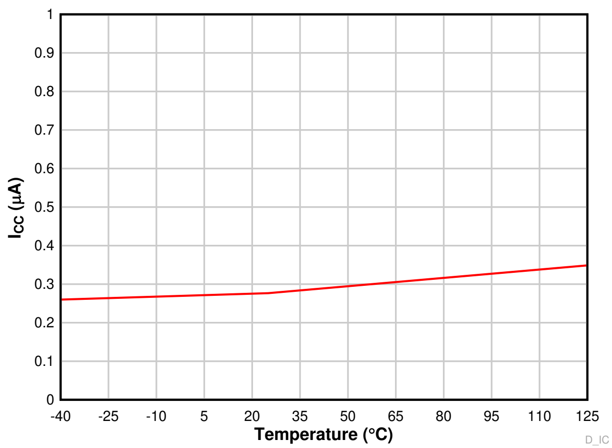
V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 5-1. $V_{OD(DOM)}$ vs Temperature



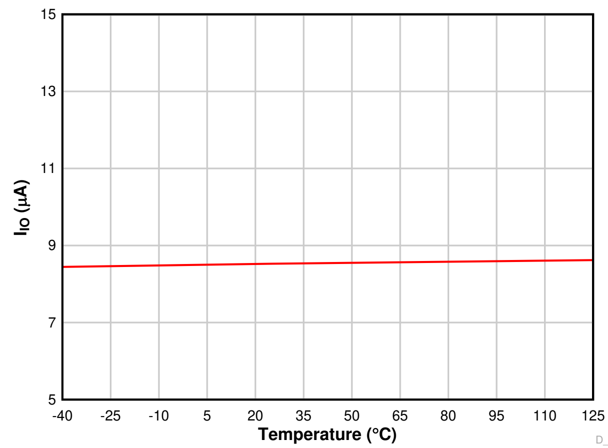
Temp = 25°C R_L = 60Ω

Figure 5-2. $V_{OD(DOM)}$ vs V_{CC}



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 5-3. I_{CC} Standby vs Temperature



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 5-4. I_{IO} Standby vs Temperature

6 Parameter Measurement Information

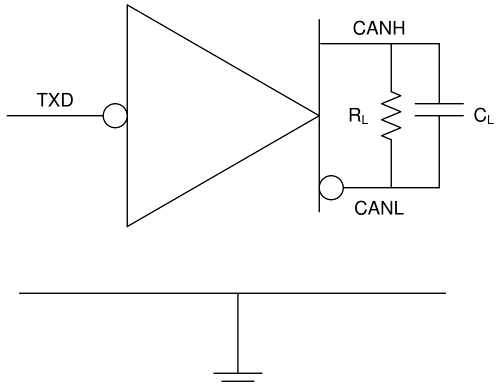


Figure 6-1. I_{CC} Test Circuit

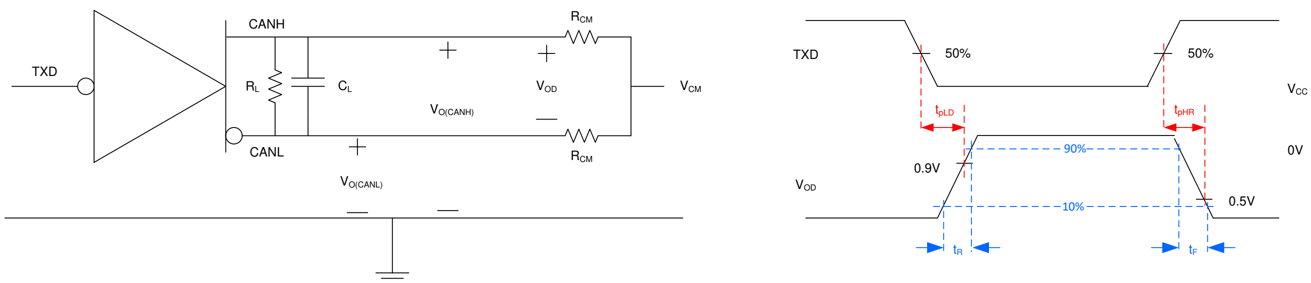


Figure 6-2. Driver Test Circuit and Measurement

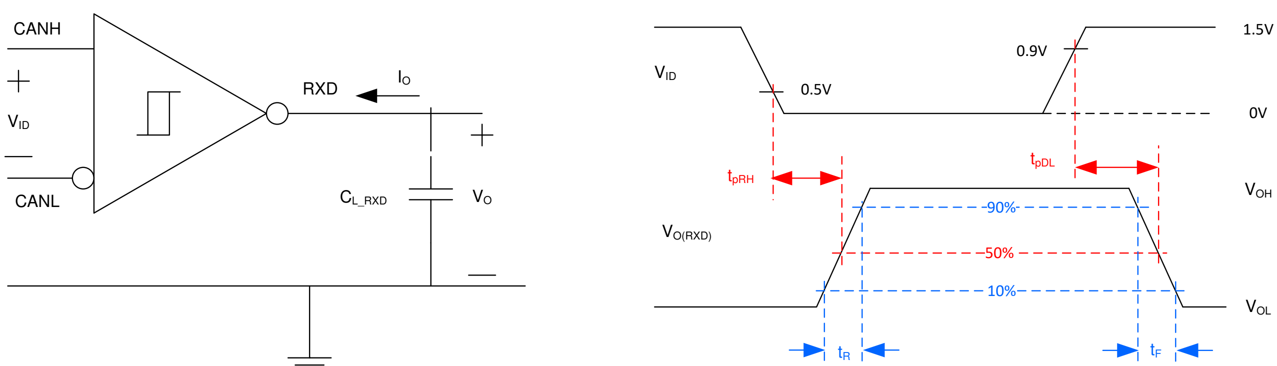


Figure 6-3. Receiver Test Circuit and Measurement

Table 6-1. Receiver Differential Input Voltage Threshold Test

Input (See Figure 6-3)			Output	
V_{CANH}	V_{CANL}	$\lvert V_{ID} \rvert$	RXD	
-11.5V	-12.5V	1000mV	Low	V_{OL}
12.5V	11.5V	1000mV		
-8.55V	-9.45V	900mV		
9.45 V	8.55V	900mV		
-8.75V	-9.25V	500mV	High	V_{OH}
9.25V	8.75V	500mV		
-11.8 V	-12.2V	400mV		
12.2V	11.8V	400mV		
Open	Open	X		

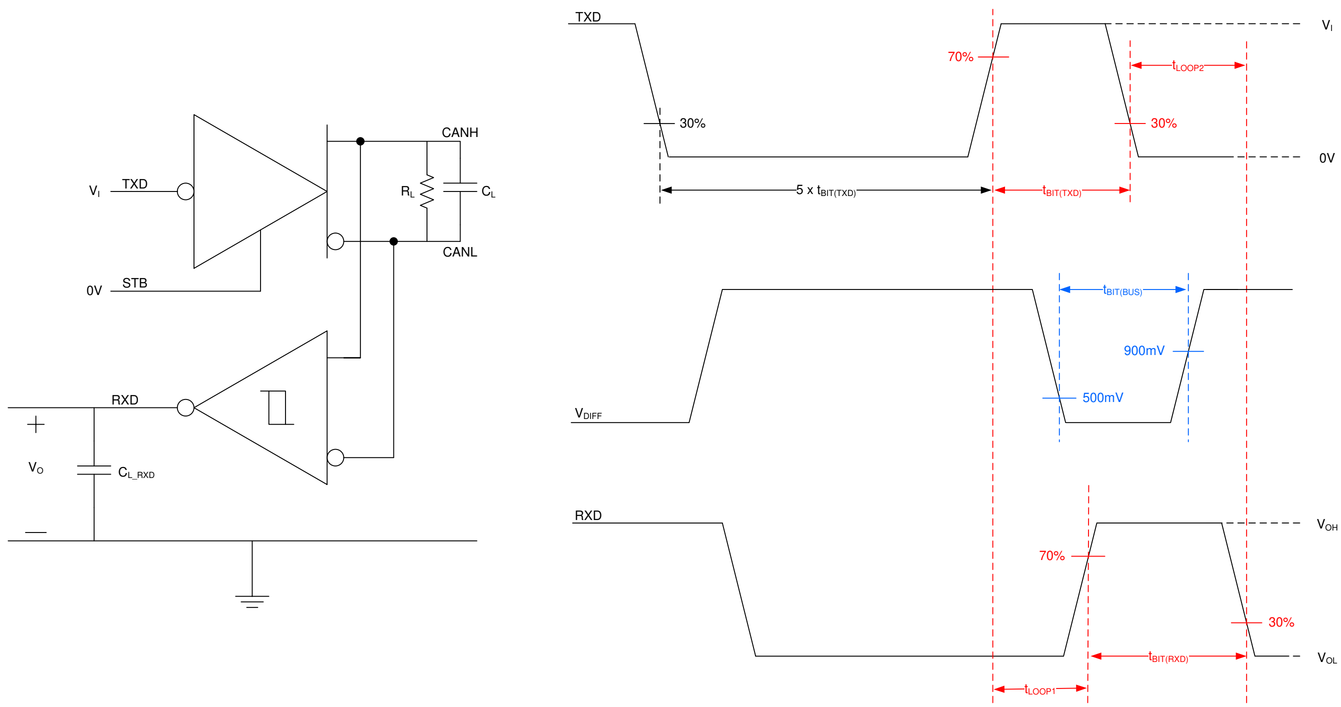


Figure 6-4. Transmitter and Receiver Timing Test Circuit and Measurement

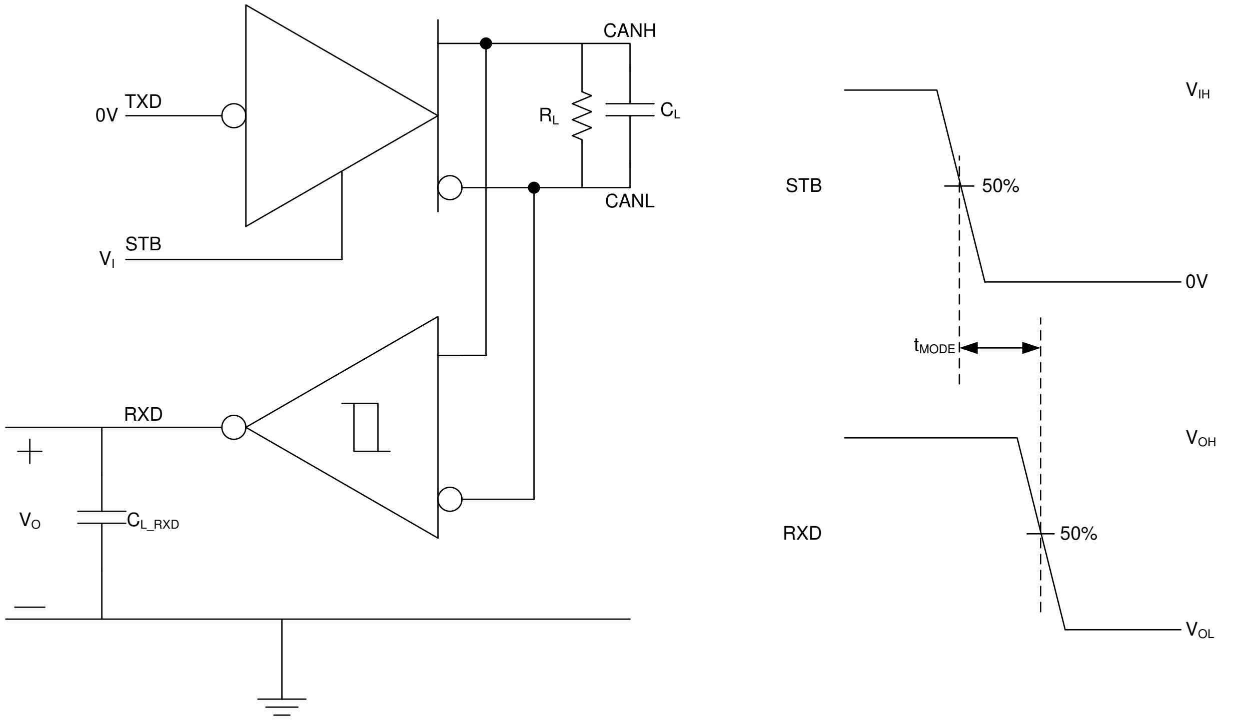


Figure 6-5. t_{MODE} Test Circuit and Measurement

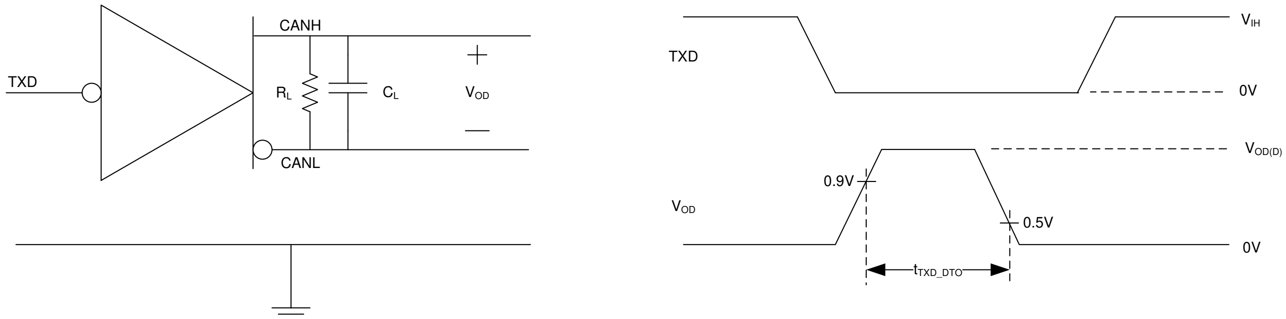


Figure 6-6. TXD Dominant Timeout Test Circuit and Measurement

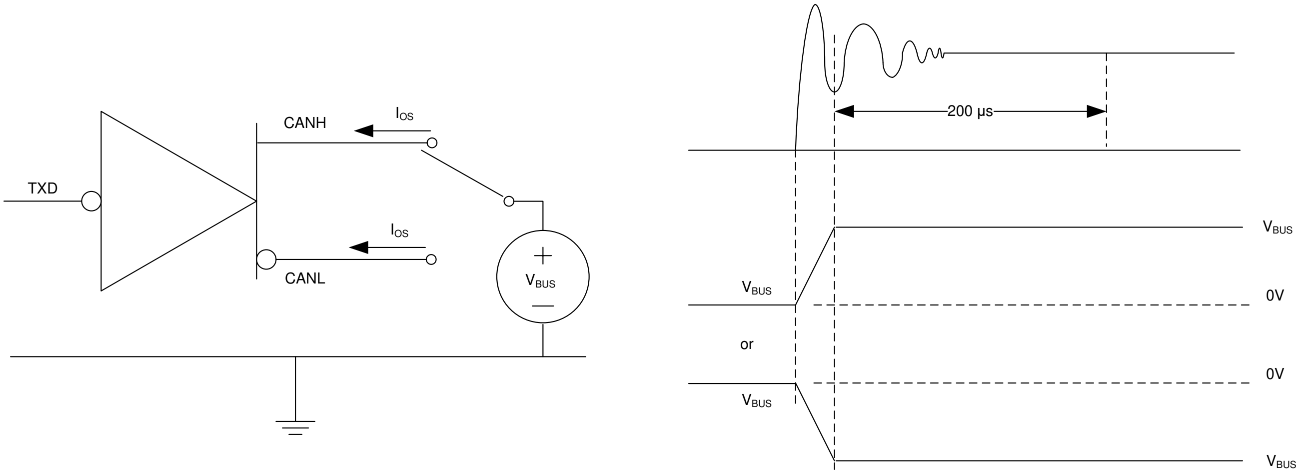


Figure 6-7. Driver Short-Circuit Current Test and Measurement

7 Detailed Description

7.1 Overview

The TCAN1044-Q1 meets or exceeds the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 and ISO 11898-5:2007 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8Mbps.

The TCAN1044-Q1 conforms to the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2016 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps
  - ARINC 825-4 General Standardization of CAN (Controller Area Network) Bus Protocol For Airborne Use
- EMC requirements:
  - VeLIO (Vehicle LAN Interoperability and Optimization) CAN and CAN-FD Transceiver Requirements
  - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

7.2 Functional Block Diagram

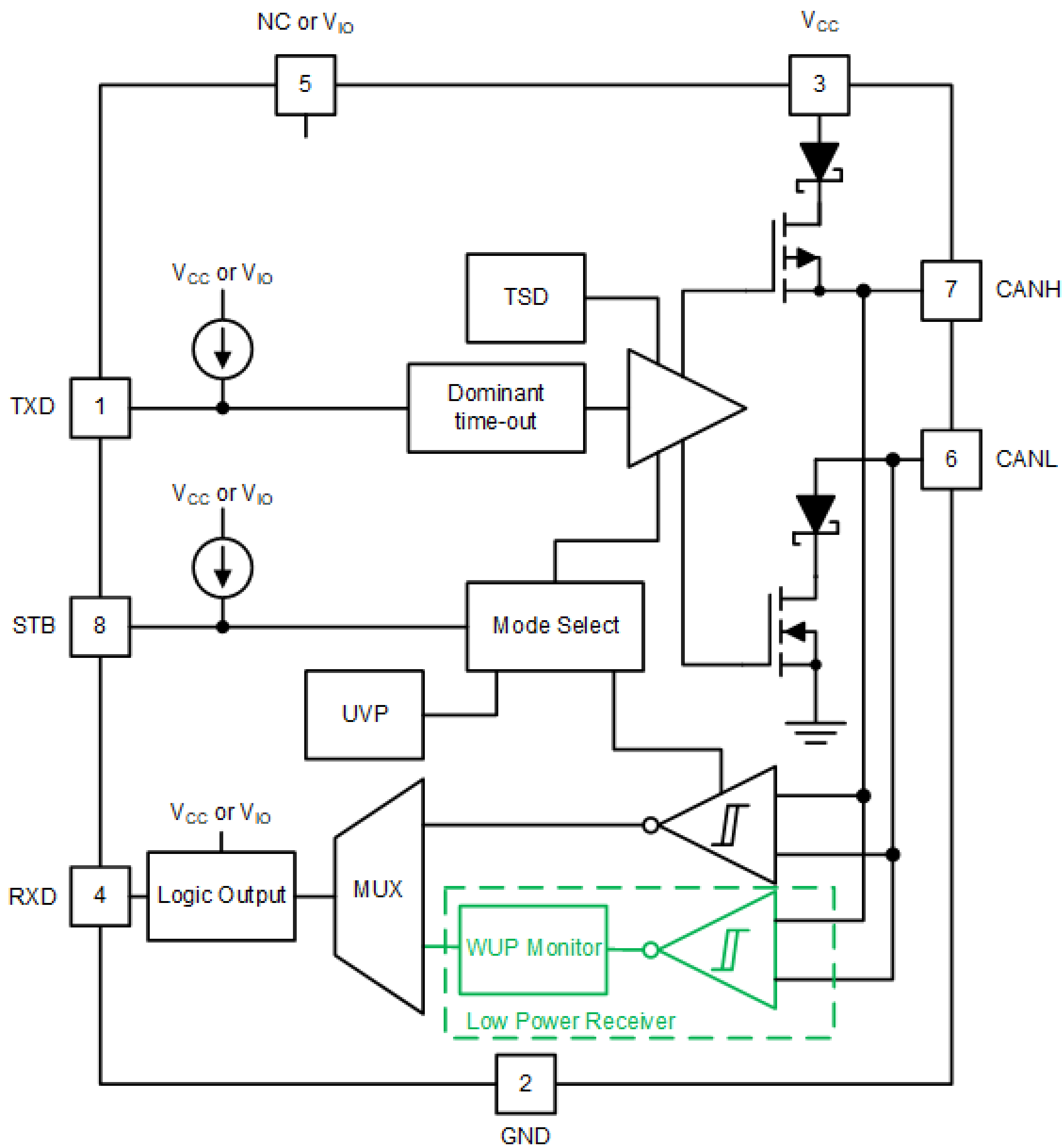


Figure 7-1. Block Diagram

7.3 Feature Description

7.3.1 Pin Description

7.3.1.1 TXD

The TXD input is a logic-level signal, referenced to either V_{CC} or V_{IO} from a CAN controller to the TCAN1044-Q1 transceivers.

7.3.1.2 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

7.3.1.3 V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

7.3.1.4 RXD

The RXD output is a logic-level signal, referenced to either V_{CC} or V_{IO} , from the TCAN1044-Q1 transceivers to the CAN controller. RXD is only driven once V_{IO} is present.

When a wake event takes place RXD is driven low.

7.3.1.5 V_{IO}

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. It supports voltages from 1.7V to 5.5V providing the widest range of controller support.

7.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

7.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, then the STB pin can be tied directly to GND.

7.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 7-2 and Figure 7-3 .

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1044-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 7-2 and Figure 7-3.

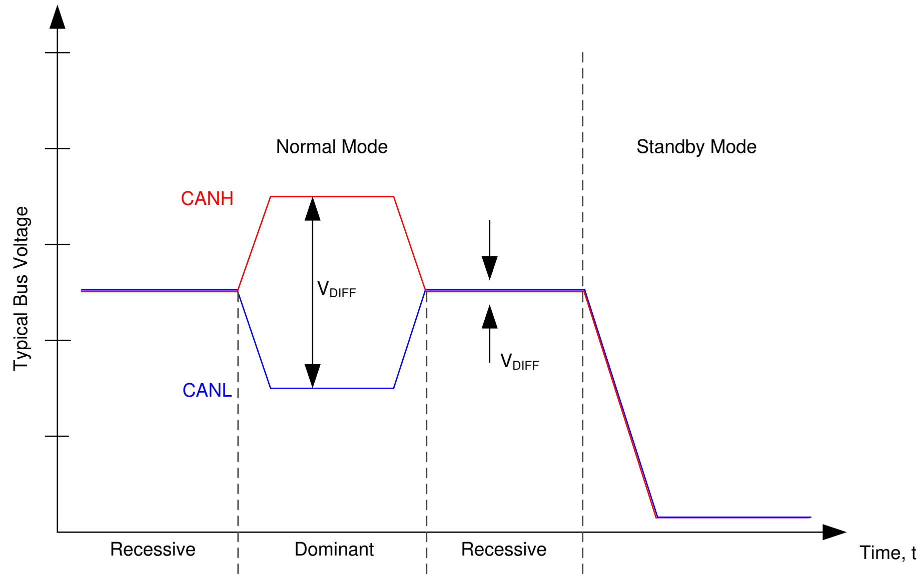
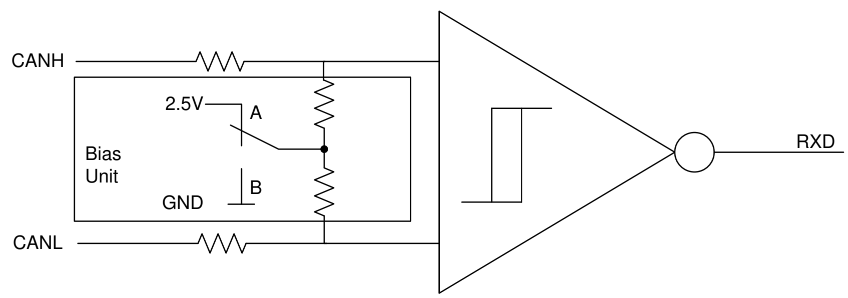


Figure 7-2. Bus States



A. Normal Mode
B. Standby Mode

Figure 7-3. Simplified Recessive Common Mode Bias Unit and Receiver

7.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant timeout. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

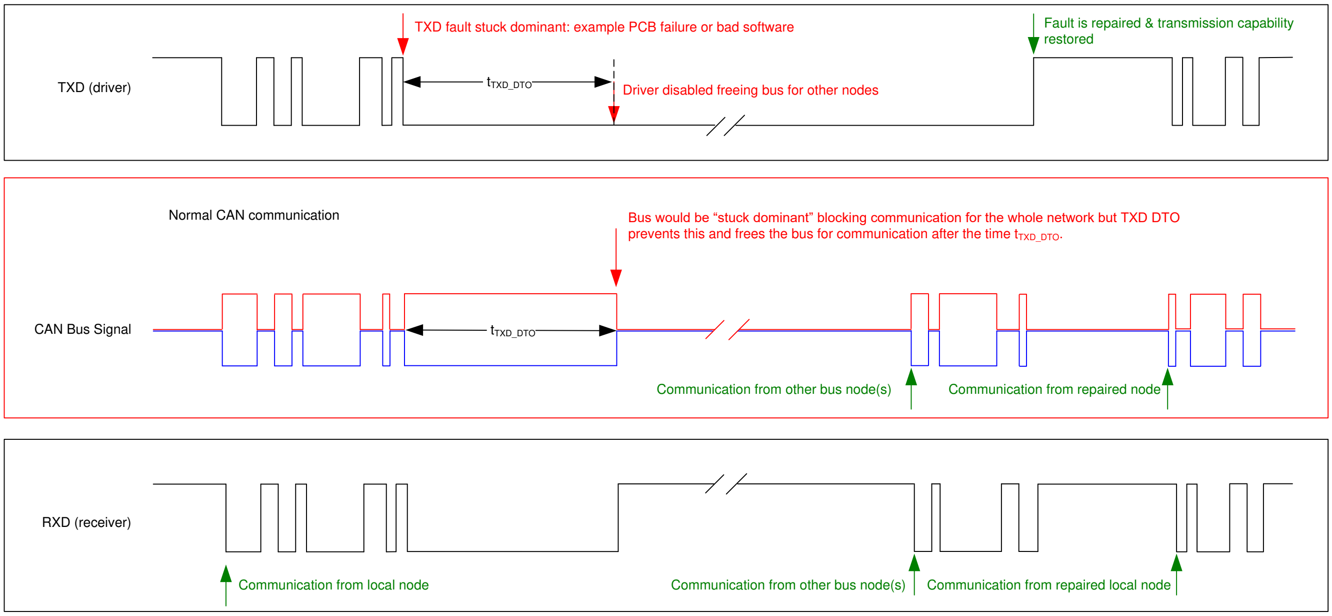


Figure 7-4. Example Timing Diagram for TXD Dominant Timeout

7.3.4 CAN Bus Short Circuit Current Limiting

The TCAN1044-Q1 has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\ Transmit\ x\ [(\%\ REC\_Bits\ x\ I_{OS(SS)\_REC}) + (\%\ DOM\_Bits\ x\ I_{OS(SS)\_DOM})] + [\%\ Receive\ x\ I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

This short circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

7.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1044-Q1 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The TCAN1044-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

7.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 7-1. Undervoltage Lockout - TCAN1044-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance Weak pull-down to ground(1)	High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$

Table 7-2. Undervoltage Lockout - TCAN1044V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: standby mode	High impedance Weak pull-down to ground(1)	V_{IO}: Remote wake request(2)
		STB = GND: Protected		Recessive
> UV_{VCC}	< UV_{VIO}	Protected		High impedance
< UV_{VCC}	< UV_{VIO}	Protected		High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$
(2) See Section 7.4.3.1

Once the undervoltage condition is cleared and t_{MODE} has expired the TCAN1044-Q1 transitions to normal mode and the host controller can send and receive CAN traffic again.

7.3.7 Unpowered Device

The TCAN1044-Q1 is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

7.3.8 Floating pins

The TCAN1044-Q1 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This makes sure the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 7-3 for details on pin bias conditions.

Table 7-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

7.4 Device Functional Modes

7.4.1 Operating Modes

The TCAN1044-Q1 has two main operating modes: normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin on the TCAN1044-Q1.

Table 7-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See Section 7.4.3.1
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

7.4.2 Normal Mode

This is the normal operating mode of the TCAN1044-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

7.4.3 Standby Mode

This is the low-power mode of the TCAN1044-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in Figure 7-5. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode; see Figure 7-2 and Figure 7-3.

In standby mode, only the V_{IO} supply is required therefore the V_{CC} may be switched off for additional system level current savings.

7.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1044-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN1044-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 7-5 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500kbps, or two back-to-back bit times at 1Mbps triggers the filter in either bus state. Any CAN frame at 500kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 7-5 for the timing diagram of the wake-up pattern with wake timeout feature.

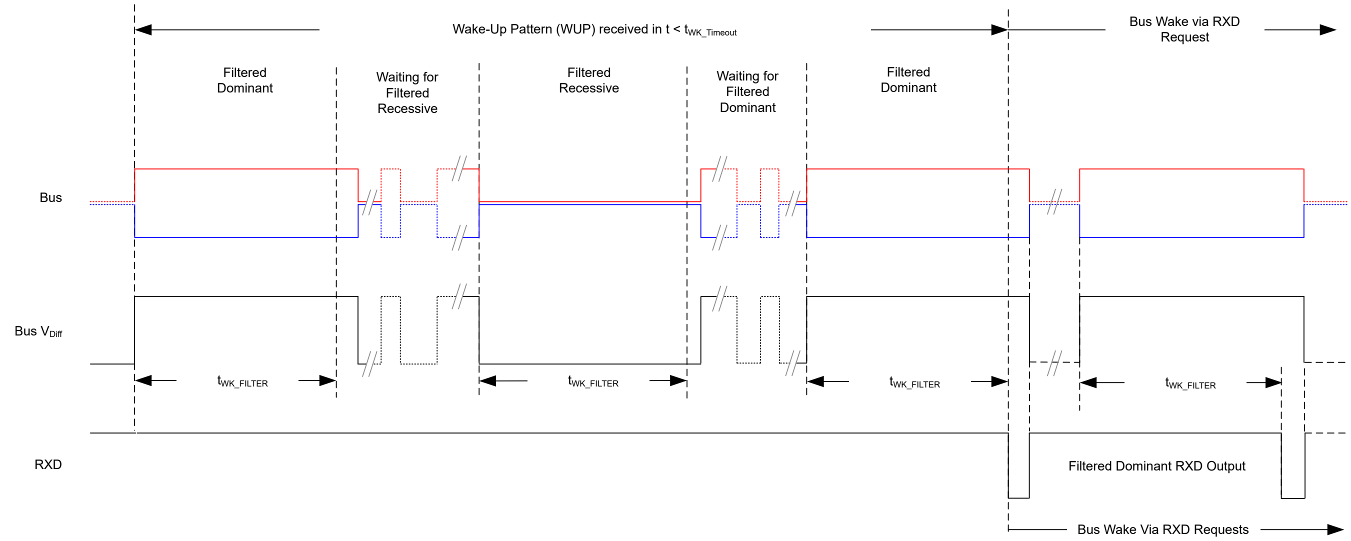


Figure 7-5. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

7.4.4 Driver and Receiver Function

The digital logic input and output levels for the TCAN1044-Q1 are CMOS levels with respect to either V_{CC} for 5V systems or V_{IO} for compatible with MCUs having 1.8V, 2.5V, 3.3V, or 5V systems.

Table 7-5. Driver Function Table

Device Mode	TXD Input[1]	Bus Outputs		Driven Bus State[2]
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see Figure 7-2 and Figure 7-3

Table 7-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	High
Standby	$V_{ID} \geq 1.15V$	Dominant	High Low if a remote wake event occurred See Figure 7-5
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Any	Open ($V_{ID} \approx 0V$)	Open	High

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

The TCAN1044-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. Figure 8-1 shows a typical configuration for 5V controller applications. The bus termination is shown for illustrative purposes.

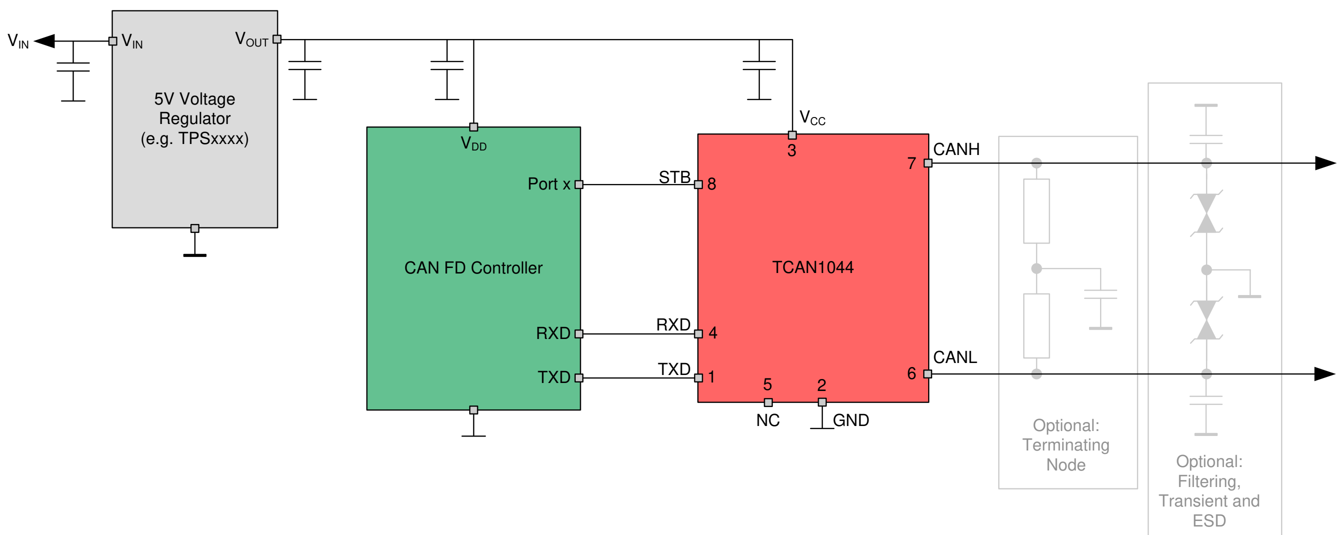


Figure 8-1. Transceiver Application Using 5V I/O Connections

8.2.1 Design Requirements

8.2.1.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see Figure 8-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

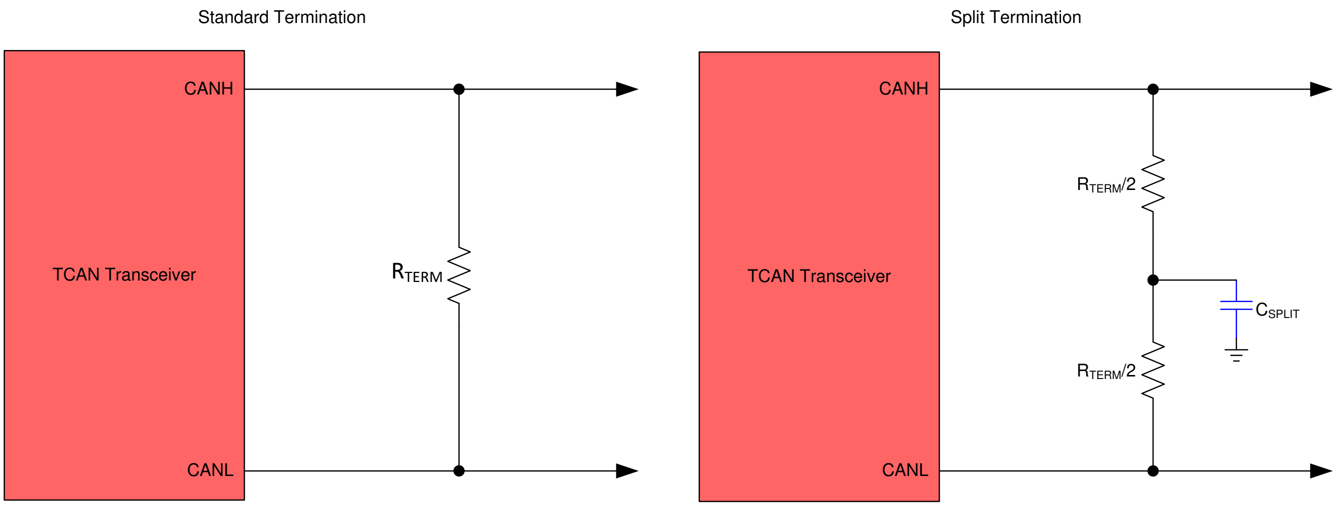


Figure 8-2. CAN Bus Termination Concepts

8.2.2 Detailed Design Procedures

8.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1044-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN1044-Q1 family is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of the TCAN1044-Q1 is a minimum of 40kΩ. If 100 TCAN1044-Q1 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN1044-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity; thus, a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design for a robust network operation.

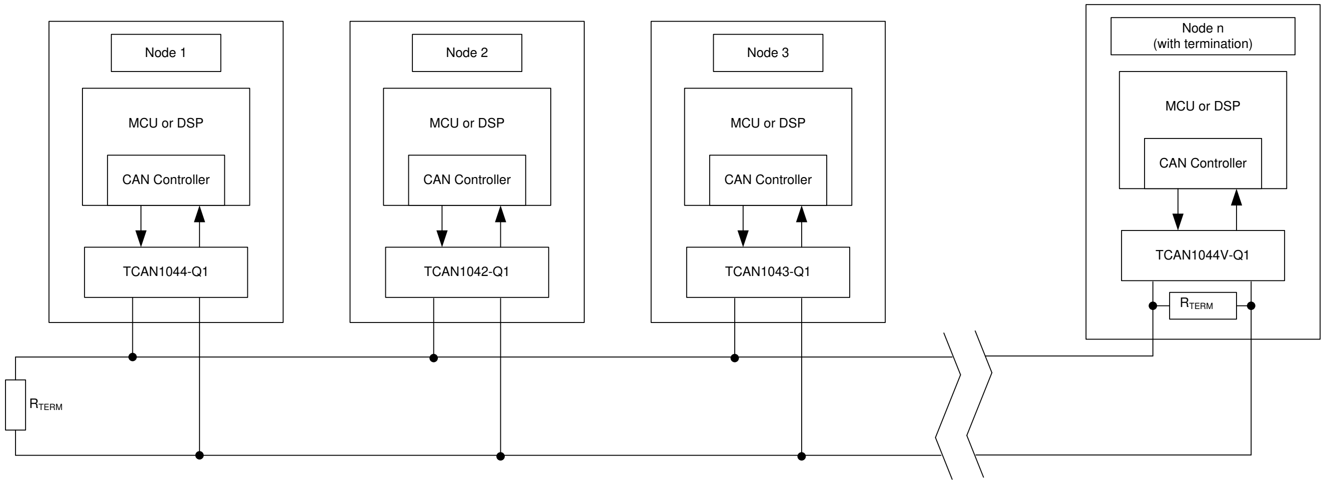
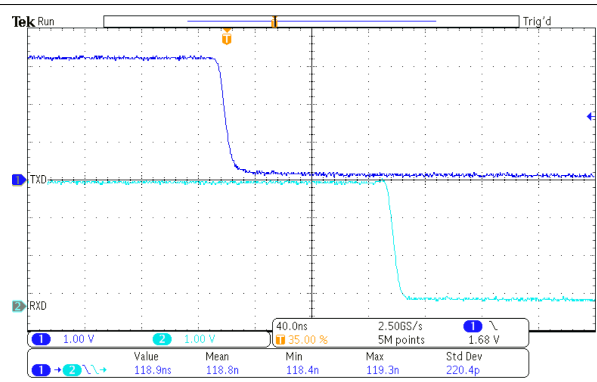


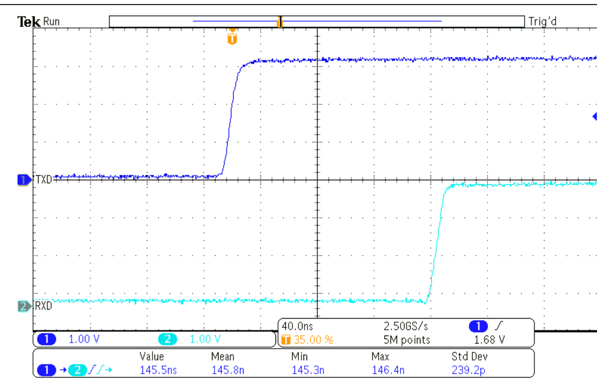
Figure 8-3. Typical CAN Bus

8.2.3 Application Curves



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 8-4. $t_{PROP(LOOP1)}$



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 8-5. $t_{PROP(LOOP2)}$

8.3 System Examples

The TCAN1044-Q1 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8V, 2.5V, or 3.3V application is shown in Figure 8-6. The bus termination is shown for illustrative purposes.

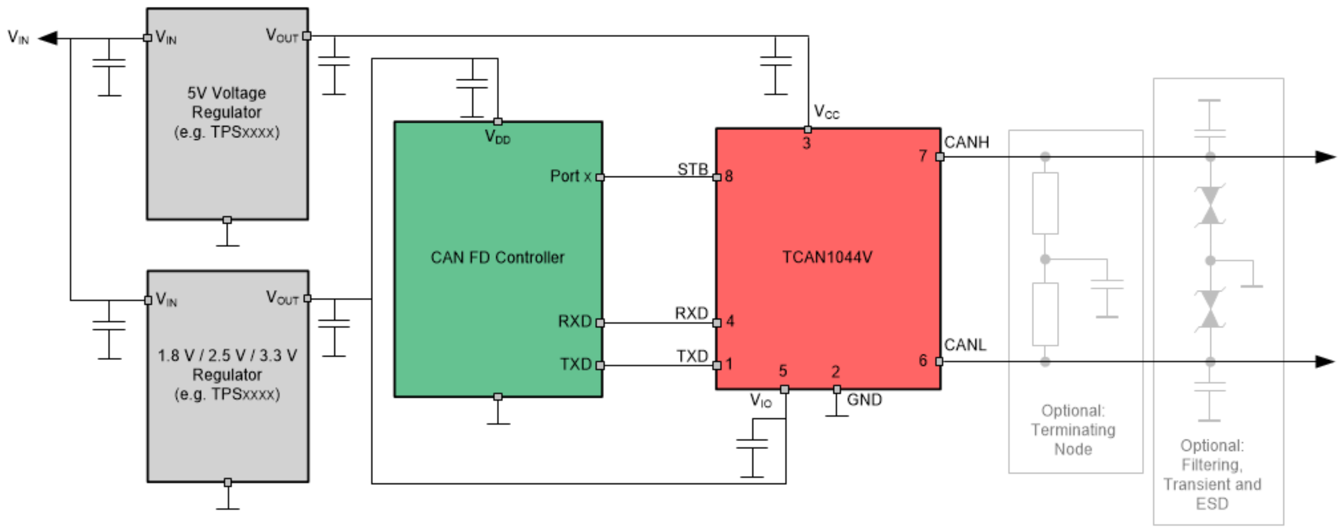


Figure 8-6. Typical Transceiver Application Using 1.8V, 2.5V, 3.3V IO Connections

8.4 Power Supply Recommendations

The TCAN1044-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.5V and 5.5V. The TCAN1044V-Q1 implements an IO level shifting supply input, V_{IO}, designed for a range between 1.8V and 5.5V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100nF, should be placed near the CAN transceiver main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100nF, should be placed near the CAN transceiver V_{IO} supply pin in addition to bypass capacitors.

8.5 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

8.5.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See Section 8.2.1.1, Section

7.3.4, and Equation 2 for information on termination concepts and power ratings needed for the termination resistor(s).

- To limit current, digital lines series resistors can be used. Examples are R2, R3 and R4.
- Pin 1 is shown for the TXD input of the device with R1 as an optional pull-up resistor. If an open drain host controller is used, making sure the bit timing into the device is met is mandatory.
- Pin 8 is shown with R4 assuming the mode pin STB, is used. If the device is used in normal mode only, R4 is not needed and the pads of C4 could be used for the pull down resistor R5 to GND.

8.5.2 Layout Example

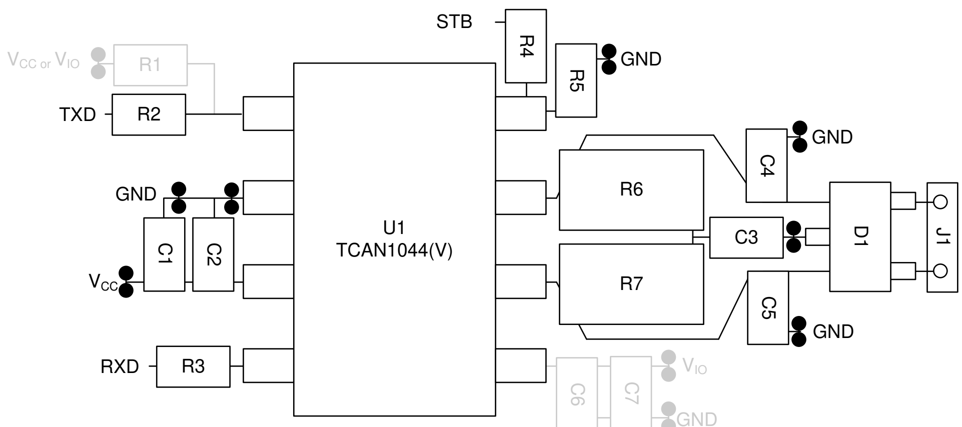


Figure 8-7. Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2021) to Revision C (October 2024) **Page**

- Changed *Feature*: "Available in SOIC..." 1
- Deleted part number TCAN1044V-Q1 from the data sheet title and header information 1
- Changed the *Device Information* table to the *Package Information* table 1

Changes from Revision A (December 2019) to Revision B (October 2021) **Page**

- Added *Feature* "Functional Safety-Capable" 1
- Changed the *Simplified Schematic* image 1
- Changed Figure 8-2 24

Changes from Revision * (August 2019) to Revision A (December 2019) **Page**

- First public release of the data sheet 1
- Added SAE j2962-2 ESD 4
- Changed footnote to Tested according to IEC 62228-3:2019 CAN Transceivers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011) 4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1044DRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1044	Samples
TCAN1044DRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1044	Samples
TCAN1044VDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26SF	Samples
TCAN1044VDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1044V	Samples
TCAN1044VDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1044V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

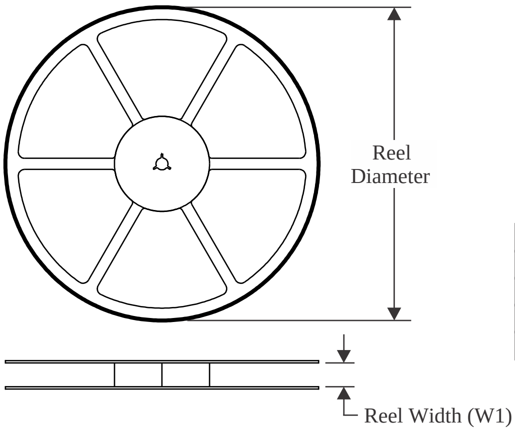
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

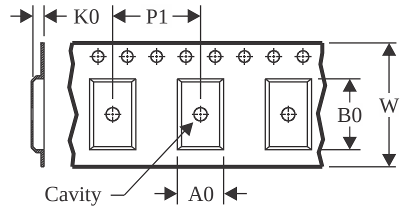
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

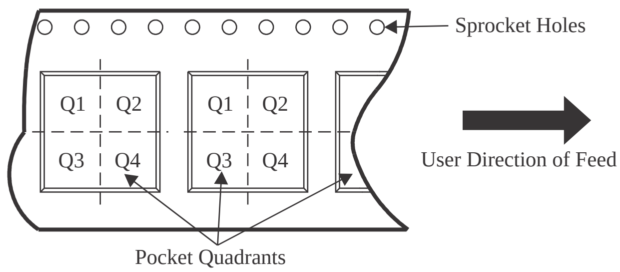


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

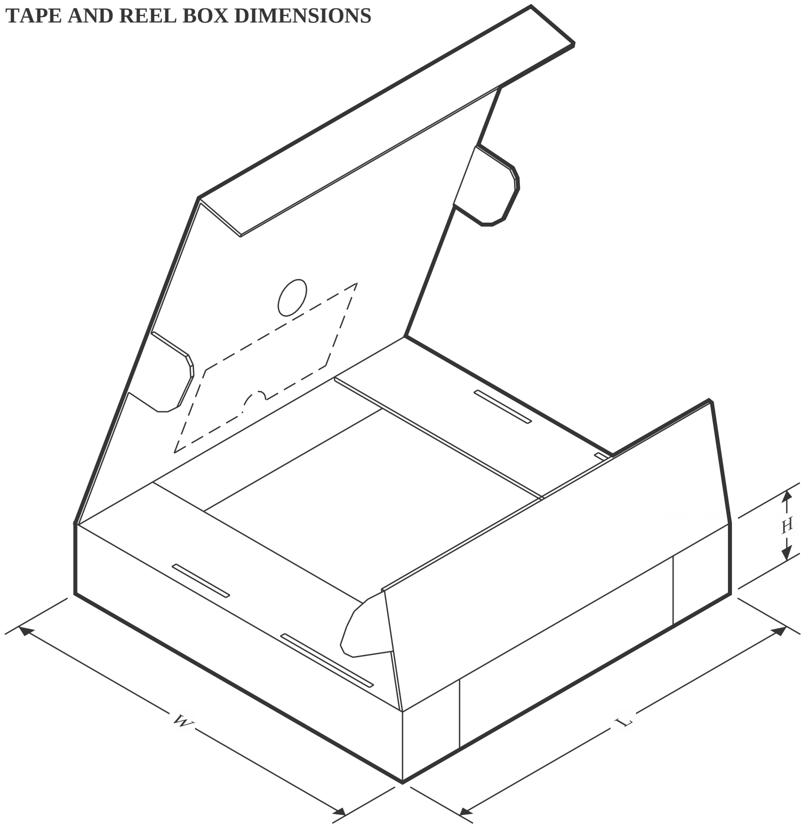
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

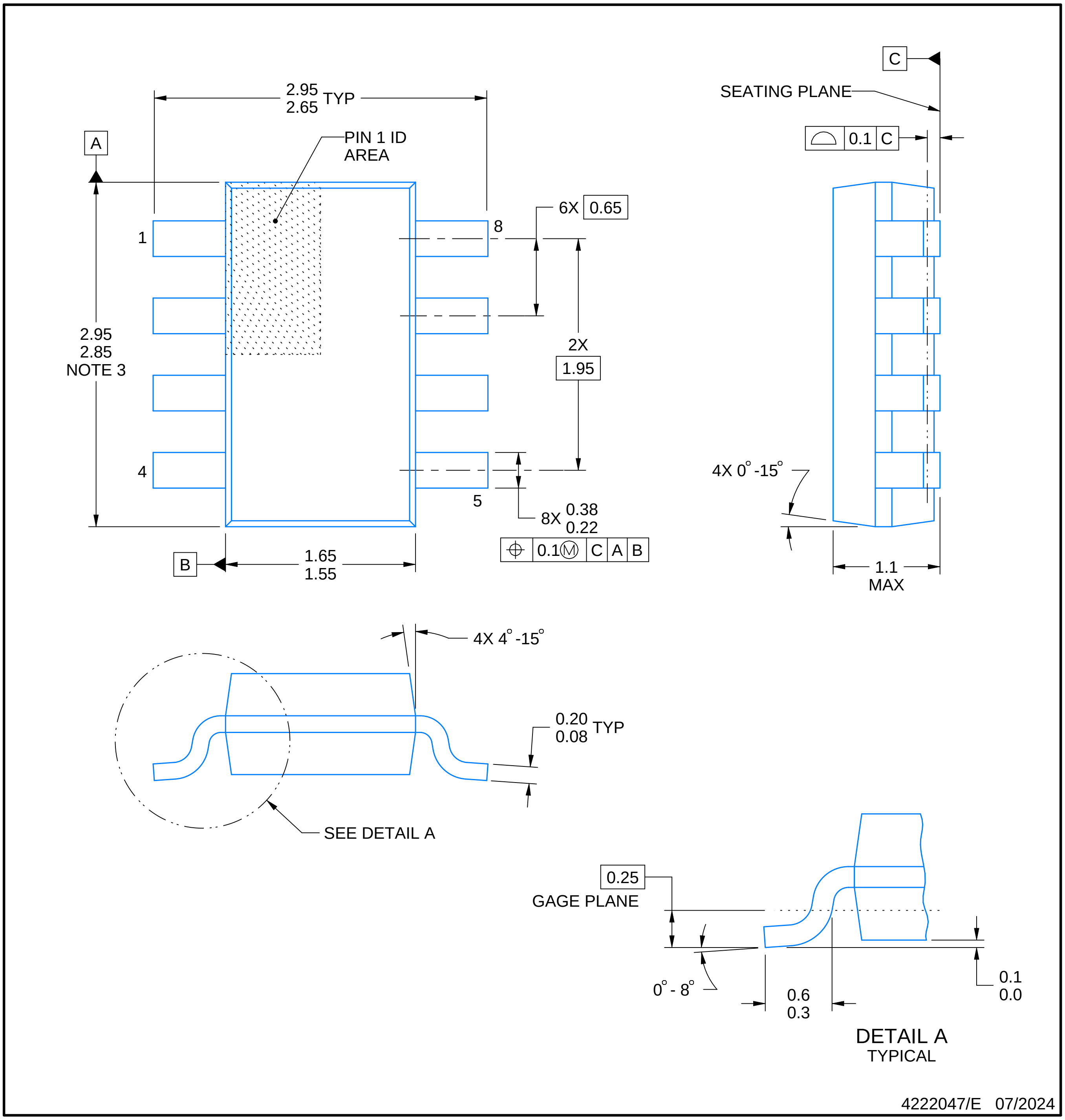
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1044DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1044VDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TCAN1044VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1044VDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



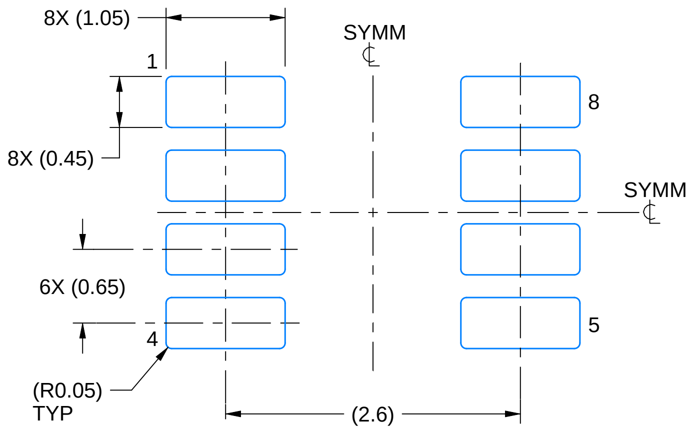
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1044DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1044VDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TCAN1044VDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1044VDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

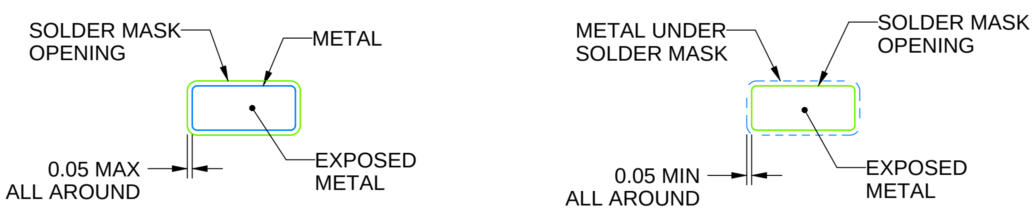


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED

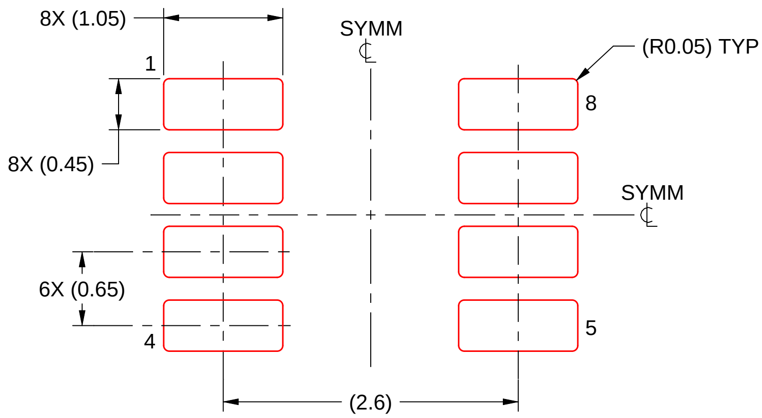
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

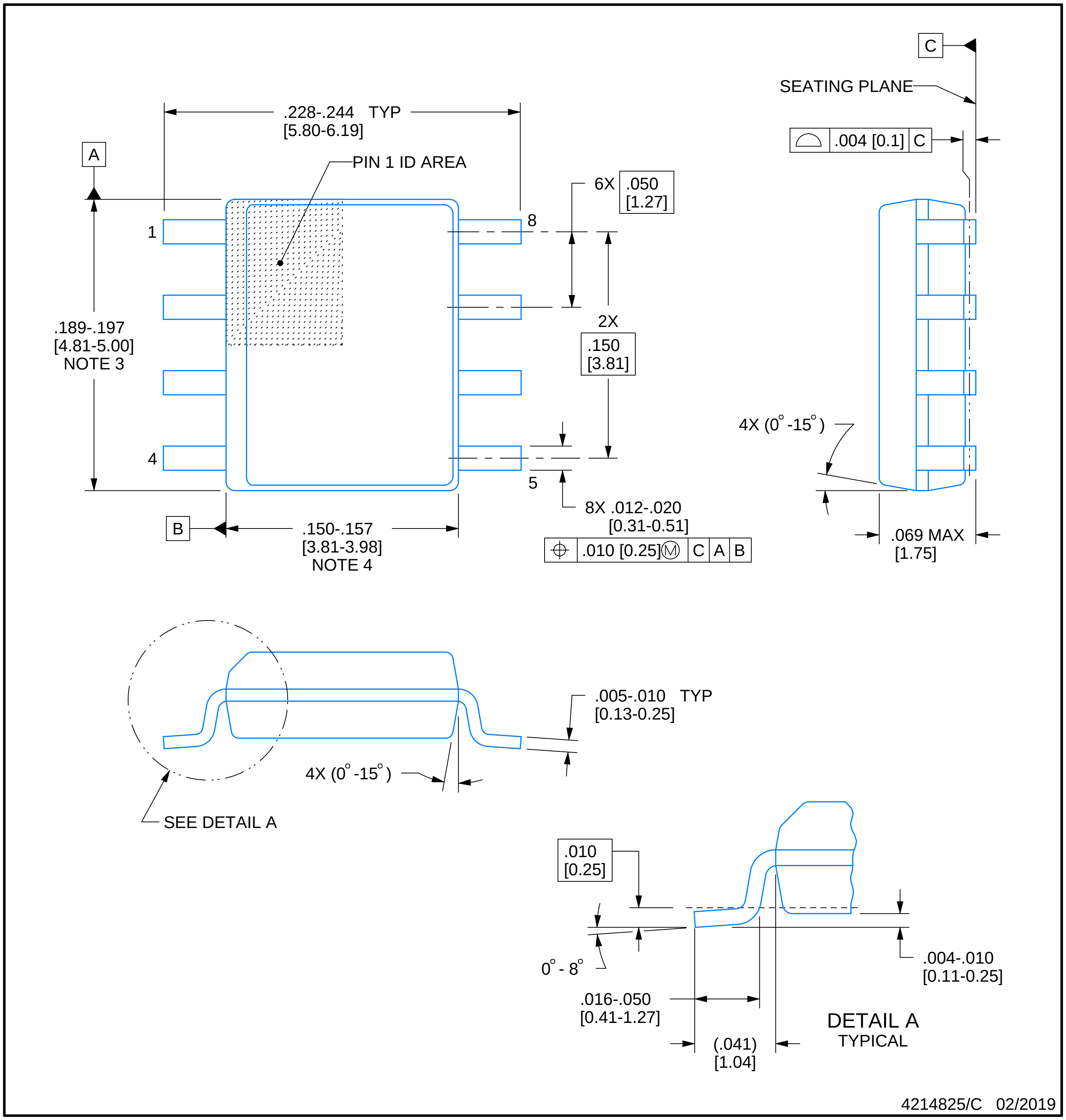


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

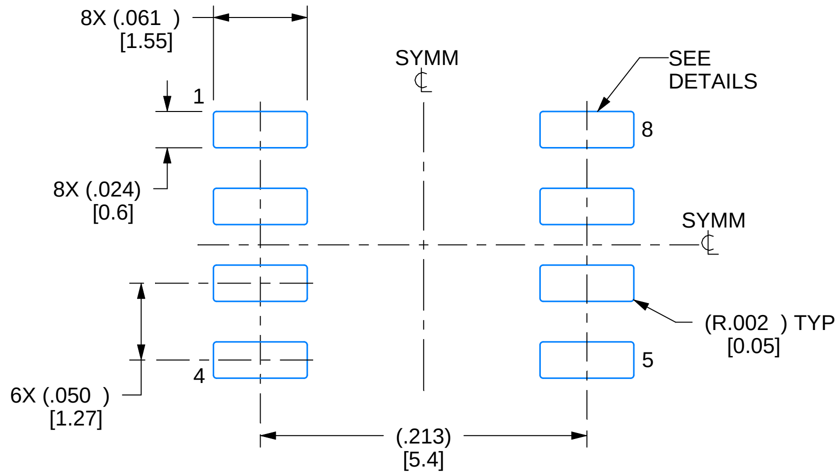
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



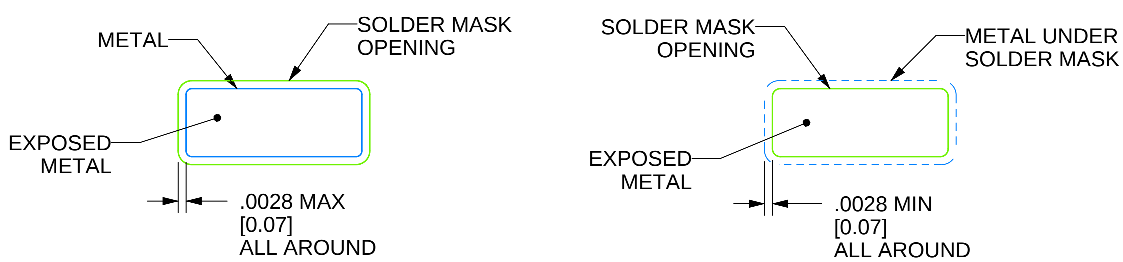
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

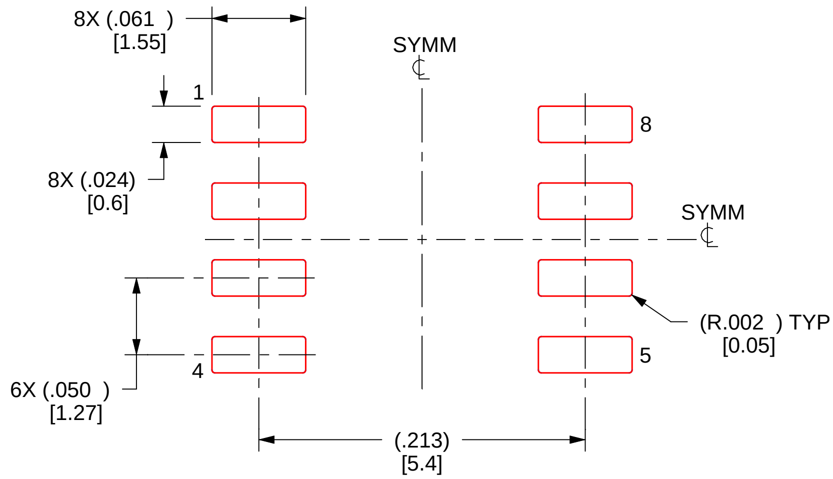
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



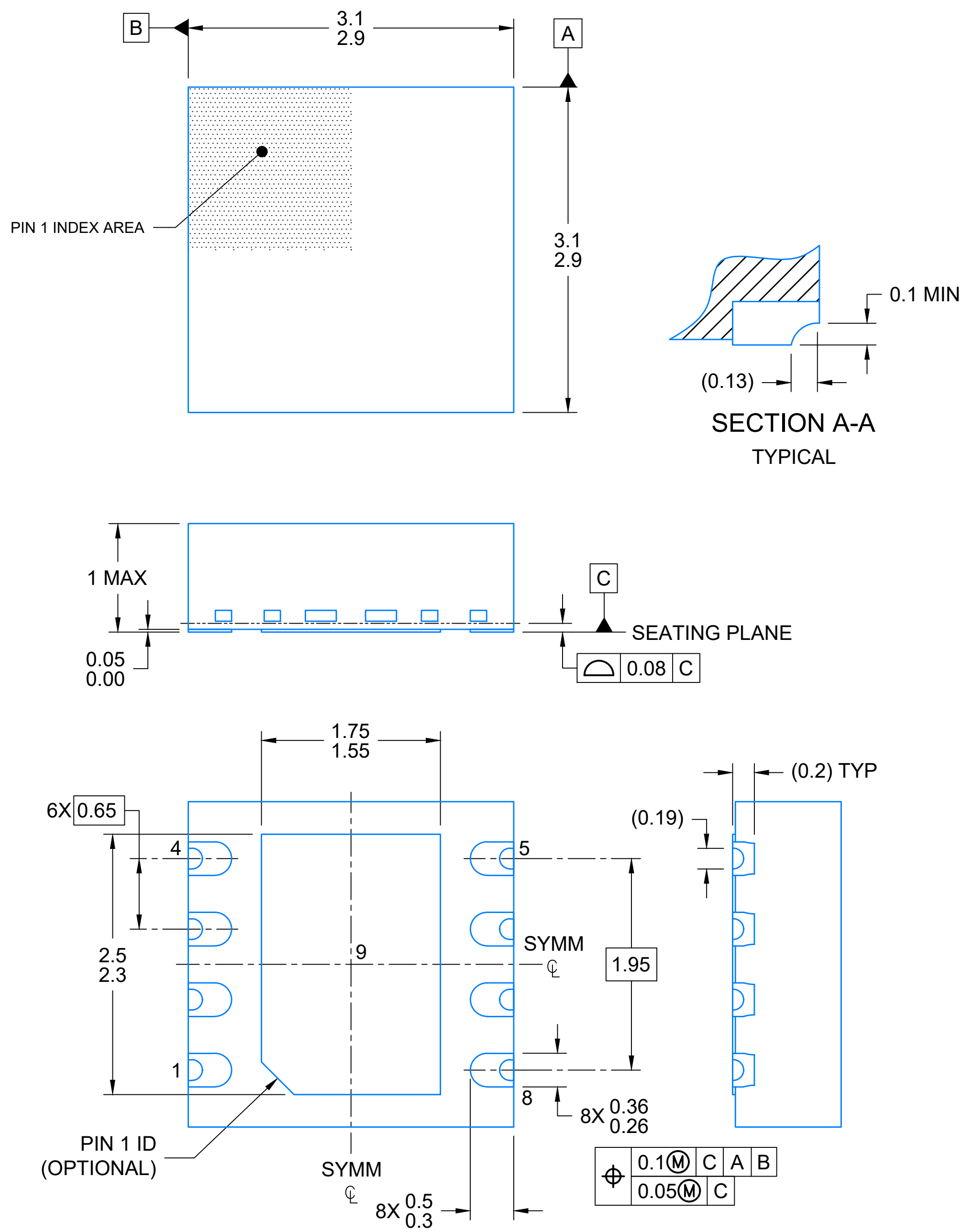
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

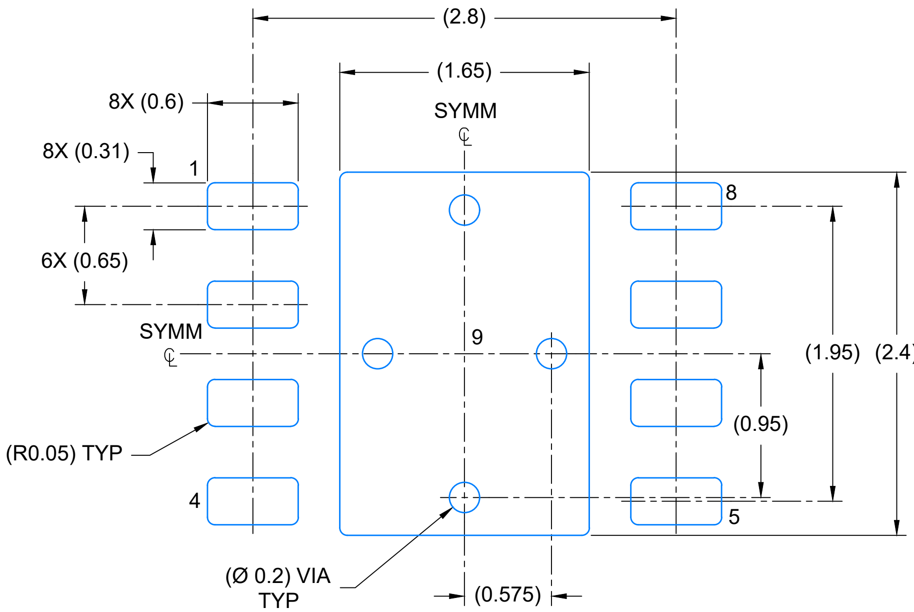
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



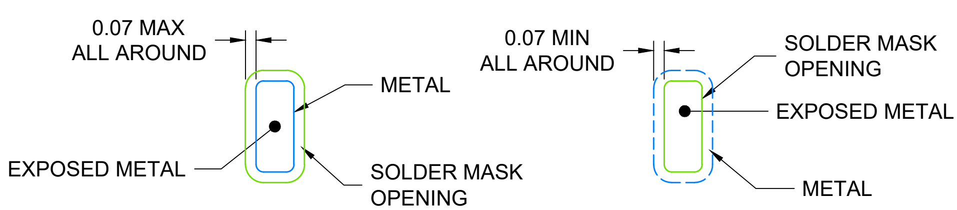
4225036/A 06/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

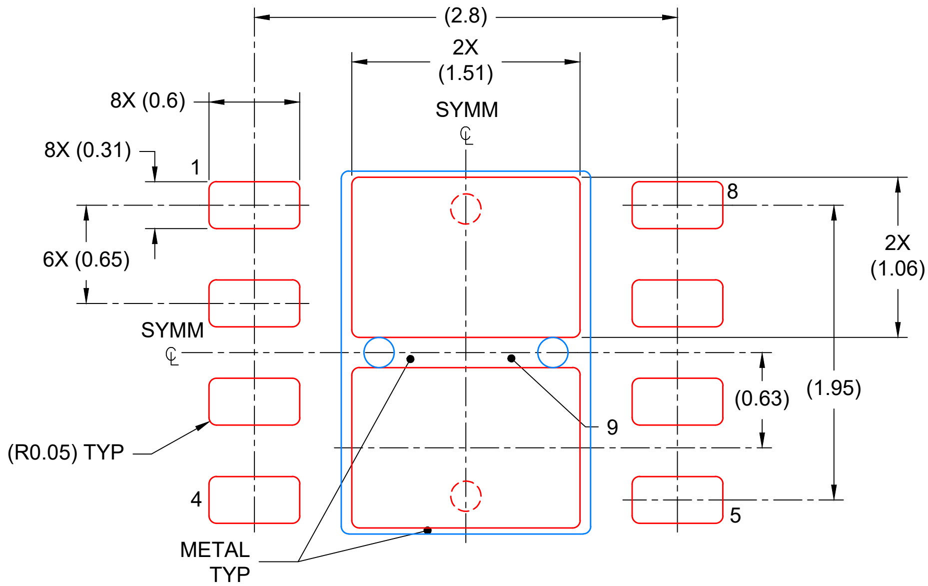
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.