TDA2Px ADAS Applications Processor 23mm Package (ABZ Package) Silicon Revision 1.0

1 Device Overview

1.1 Features

- Architecture Designed for ADAS Applications
- Video, Image, and Graphics Processing Support
  - Full-HD Video (1920 × 1080p, 60 fps)
  - Multiple Video Input and Video Output
- Dual Arm® Cortex®-A15 Microprocessor Subsystem
- Up to Two C66x Floating-Point VLIW DSP
  - Fully Object-Code Compatible with C67x and C64x+
  - Up to Thirty-Two 16 × 16-Bit Fixed-Point Multiplies per Cycle
- Up to 2.5MB of On-Chip L3 RAM
- Level 3 (L3) and Level 4 (L4) Interconnects
- Two DDR2/DDR3/DDR3L Memory Interface (EMIF) Modules
  - Supports up to DDR2-800 and DDR3-1333
  - Up to 2GB Supported per EMIF
- Dual Arm® Cortex®-M4 Image Processing Units (IPU)
- Vision AccelerationPac
  - Up to Two Embedded Vision Engines (EVEs)
- Imaging Subsystem (ISS)
  - Image Signal Processor (ISP)
  - Wide Dynamic Range and Lens Distortion Correction (WDR and Mesh LDC)
  - One Camera Adaptation Layer (CAL_B)
- IVA-HD Subsystem
- Display Subsystem
  - Display Controller with DMA Engine and up to Three Pipelines
  - HDMI™ Encoder: HDMI 1.4a and DVI 1.0 Compliant
- 2D-Graphics Accelerator (BB2D) Subsystem
  - Vivante® GC320 Core
- Video Processing Engine (VPE)
- Dual-Core PowerVR® SGX544 3D GPU
- Two Video Input Port (VIP) Modules
  - Support for up to Eight Multiplexed Input Ports
- General-Purpose Memory Controller (GPMC)
- Enhanced Direct Memory Access (EDMA) Controller
- 2-Port Gigabit Ethernet (GMAC)
- Up to Two Controller Area Network (DCAN) Modules
  - CAN 2.0B Protocol
- Modular Controller Area Network (MCAN) Module
  - CAN 2.0B Protocol with Available FD (Flexible Data Rate) Functionality
- PCI Express® 3.0 Port with Integrated PHY
  - One 2-Lane Gen2-Compliant Port
  - or Two 1-Lane Gen2-Compliant Ports
- Sixteen 32-Bit General-Purpose Timers
- 32-Bit MPU Watchdog Timer
- Ten Configurable UART/IrDA/CIR Modules
- Four Multichannel Serial Peripheral Interfaces (McSPI)
- Quad SPI Interface
- Five Inter-Integrated Circuit (I^2C) Ports
- SATA Interface
- Eight Multichannel Audio Serial Port (McASP) Modules
- SuperSpeed USB 3.0 Dual-Role Device
- Three High-Speed USB 2.0 Dual-Role Devices
- Four MultiMedia Card/Secure Digital/Secure Digital Input Output Interfaces (MMC™/ SD®/SDIO)
- Up to 247 General-Purpose I/O (GPIO) Pins
- Real-Time Clock Subsystem (RTCSS)
- Device Security Features
  - Hardware Crypto Accelerators and DMA
  - Firewalls
  - JTAG® Lock
  - Secure Keys
  - Secure ROM and Boot
  - Customer Programmable Keys and OTP Data
- Power, Reset, and Clock Management
- On-Chip Debug With CTools Technology
- Automotive AEC-Q100 Qualified
- 28-nm CMOS Technology
- 23 mm × 23 mm, 0.8-mm Pitch, 760-Pin BGA (ABZ)

1.2 Applications

- Mono, Stereo or Tri-Optic Front Camera
  - Object Detection
  - Pedestrian Detection
  - Traffic Sign Recognition
  - Lane Detection and Departure Warning
  - Automatic Emergency Braking
  - Adaptive Cruise Control
  - Forward Collision Warning
  - High Beam Assist
- LVDS or Ethernet Surround View
  - 2D surround view
  - 3D surround view
  - Rear object detection
  - Parking assist
  - Pedestrian Detection
  - Lane tracking
  - Drive Recording
- Sensor Fusion – Vision, Radar, Ultrasonic, Lidar sensors
  - Object data fusion
  - Raw data fusion

1.3 Description

TI's new TDA2Px System-on-Chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS). The TDA2Px family enables broad ADAS applications in automobiles by integrating an optimal mix of performance, low power and ADAS vision analytics processing that aims to facilitate a more autonomous and collision-free driving experience.

The TDA2Px SoC enables sophisticated embedded vision technology in automobiles by broadest range of ADAS applications including front camera, park assist, surround view and sensor fusion on a single architecture.

The TDA2Px SoC incorporates a heterogeneous, scalable architecture that includes a mix of TI's fixed and floating-point TMS320C66x digital signal processor (DSP) generation cores, Vision AccelerationPac, Arm Cortex-A15 MPCore™ and dual-Cortex-M4 processors. The integration of a video accelerator for decoding multiple video streams over an Ethernet AVB network, along with graphics accelerators for rendering virtual views, enable a 3D viewing experience. And the TDA2Px SoC also integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and GigB Ethernet AVB.

The Vision AccelerationPac for this family of products includes multiple embedded vision engines (EVEs) offloading the vision analytics functionality from the application processor while also reducing the power footprint. The Vision AccelerationPac is optimized for vision processing with a 32-bit RISC core for efficient program execution and a vector coprocessor for specialized vision processing.

Additionally, TI provides a complete set of development tools for the Arm, DSP, and EVE coprocessor, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

Cryptographic acceleration is available in all devices. All other supported security features, including support for secure boot, debug security and support for trusted execution environment are available on High-Security (HS) devices. For more information about HS devices, contact your TI representative.

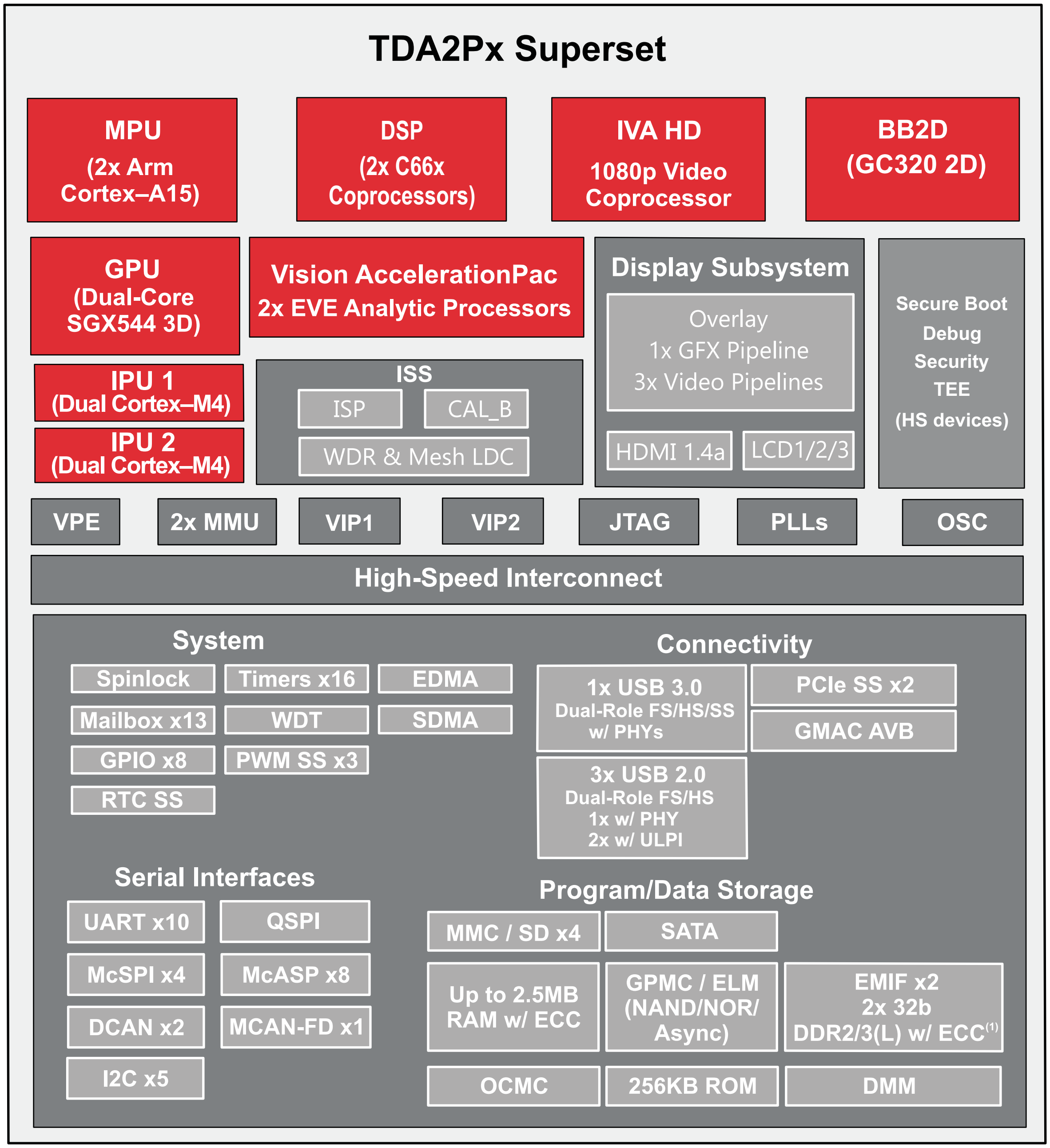
The TDA2Px ADAS processor is qualified according to the AEC-Q100 standard.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
TDA2Px	FCBGA (760)	23.0 mm × 23.0 mm

1.4 Functional Block Diagram

Figure 1-1 is functional block diagram of the superset.



intro-001

Figure 1-1. TDA2Px Block Diagram

(1) ECC is only available on EMIF1.

Table of Contents

2 Revision History

Changes from March 17, 2018 to December 15, 2018 (from E Revision (March 2018) to F Revision) **Page**

3 Device Comparison

3.1 Device Comparison Table

Table 3-1 shows a comparison between devices, highlighting the differences.

Table 3-1. Device Comparison[6]

Features			Device				
			TDA2PSxx	TDA2PHxx			
			TDA2PSXx	TDA2PHGx	TDA2PHFx	TDA2PHVx	TDA2PHAx
Features							
CTRL_WKUP_STD_FUSE_DIE_ID_2[31:24] Base PN register bitfield value[5][6]			51 (0x33)	42 (0x2A)	41 (0x29)	38 (0x26)	37 (0x25)
Processors/ Accelerators							
Speed Grades			T	R, D	U	R, D	R, D
Arm Dual Cortex-A15 Microprocessor Subsystem		MPU core 0	Yes	Yes	Yes	Yes	Yes
		MPU core 1	Yes	No	Yes	No	No
C66x VLIW DSP		DSP1 (with L1D ECC)	Yes	Yes	Yes	Yes	Yes
		DSP2 (with L1D ECC)	Yes	Yes	Yes	Yes	Yes
BitBLT 2D Hardware Acceleration Engine		BB2D	Yes	Yes	No	No	No
Display Subsystem		VOUT1	Yes[1]	Yes[1]	Yes[1]	Yes[1]	Yes[1]
		VOUT2	Yes[1]	Yes[1]	Yes[1]	Yes[1]	Yes[1]
		VOUT3	Yes[1]	Yes[1]	Yes[1]	Yes[1]	Yes[1]
		HDMI	Yes	Yes	Yes	Yes	Yes
Embedded Vision Engine		EVE1	Yes	Yes	Yes	Yes	Yes
		EVE2	Yes	Yes	Yes	Yes	Yes
Arm Dual Cortex-M4 Image Processing Unit		IPU1	Yes	Yes	Yes	Yes	Yes
		IPU2	Yes	Yes	Yes	Yes	Yes
Image Video Accelarator		IVA	Yes	Yes	Yes	Yes	No
SGX544 Dual-Core 3D Graphics Processing Unit		GPU	Yes	Yes	No	No	No
Imaging Subsystem with WDR & LDC (ISS)		ISP	Yes	Yes	Yes	Yes	No
		WDR & Mesh LDC[4]	Yes	Yes	Yes	Yes	No
		CAL_B	Yes	Yes	Yes	Yes	No
Video Input Port	VIP1	vin1a	Yes	Yes	Yes	Yes	Yes
		vin1b	Yes	Yes	Yes	Yes	Yes
		vin2a	Yes	Yes	Yes	Yes	Yes
		vin2b	Yes	Yes	Yes	Yes	Yes
	VIP2	vin3a	Yes	Yes	Yes	Yes	Yes
		vin3b	Yes	Yes	Yes	Yes	Yes
		vin4a	Yes	Yes	Yes	Yes	Yes
		vin4b	Yes	Yes	Yes	Yes	Yes
	VIP3	vin5a	No	No	No	No	No
		vin6a	No	No	No	No	No
Video Processing Engine		VPE	Yes	Yes	Yes	Yes	Yes
Camera Adaptation Layer (CAL) Camera Serial Interface 2 (CSI2)		CSI2_0 (CLK + 4 Data)	No	No	No	No	No
		CSI2_1 (CLK + 2 Data)	No	No	No	No	No

Table 3-1. Device Comparison(6) (continued)

Features		Device				
		TDA2PSxx	TDA2PHxx			
		TDA2PSXx	TDA2PHGx	TDA2PHFx	TDA2PHVx	TDA2PHAx
Program/Data Storage						
On-Chip Shared Memory (RAM)	OCMC_RAM1	512 KB	512 KB	512 KB	512 KB	512 KB
	OCMC_RAM2	1 MB	1 MB	1 MB	1 MB	1 MB
	OCMC_RAM3	1 MB	1 MB	1 MB	1 MB	1 MB
General-Purpose Memory Controller	GPMC	Yes	Yes	Yes	Yes	Yes
DDR2/DDR3/DDR3L Memory Controller(2)	EMIF1 (with R-mod-W ECC)	up to 2 GB	up to 2 GB	up to 2 GB	up to 2 GB	up to 2 GB
	EMIF2	up to 2 GB	up to 2 GB	up to 2 GB	up to 2 GB	up to 2 GB
Dynamic Memory Manager	DMM	Yes	Yes	Yes	Yes	Yes
Radio Support						
Audio Tracking Logic	ATL	No	No	No	No	No
Viterbi Coprocessor	VCP1	No	No	No	No	No
	VCP2	No	No	No	No	No
Peripherals						
Controller Area Network Interface (CAN)	DCAN1(3)	Yes	Yes	Yes	Yes	Yes
	DCAN2(3)	Yes	Yes	Yes	Yes	Yes
	MCAN with FD(3)	Yes	Yes	Yes	Yes	Yes
Enhanced DMA	EDMA	Yes	Yes	Yes	Yes	Yes
System DMA	SDMA	Yes	Yes	Yes	Yes	Yes
Ethernet Subsystem (Ethernet SS)	GMAC_SW[0]	Yes	Yes	Yes	Yes	Yes
	GMAC_SW[1]	Yes	Yes	Yes	Yes	Yes
General-Purpose IO	GPIO	up to 247	up to 247	up to 247	up to 247	up to 247
Inter-Integrated Circuit Interface	I2C	5	5	5	5	5
System Mailbox Module	MAILBOX	13	13	13	13	13
Media Local Bus	MLB	No	No	No	No	No
Multi-Channel Audio Serial Port	McASP1	16 serializers	16 serializers	16 serializers	16 serializers	16 serializers
	McASP2	16 serializers	16 serializers	16 serializers	16 serializers	16 serializers
	McASP3	4 serializers	4 serializers	4 serializers	4 serializers	4 serializers
	McASP4	4 serializers	4 serializers	4 serializers	4 serializers	4 serializers
	McASP5	4 serializers	4 serializers	4 serializers	4 serializers	4 serializers
	McASP6	4 serializers	4 serializers	4 serializers	4 serializers	4 serializers
	McASP7	4 serializers	4 serializers	4 serializers	4 serializers	4 serializers
	McASP8	4 serializers	4 serializers	4 serializers	4 serializers	4 serializers
MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO)	MMC1	Yes	Yes	Yes	Yes	Yes
	MMC2	Yes	Yes	Yes	Yes	Yes
	MMC3	Yes	Yes	Yes	Yes	Yes
	MMC4	Yes	Yes	Yes	Yes	Yes
PCI Express 3.0 Port with Integrated PHY	PCIe_SS1	Yes	Yes	Yes	Yes	Yes
	PCIe_SS2	Yes	Yes	Yes	Yes	Yes
SATA Gen2 Interface	SATA	Yes	Yes	Yes	Yes	Yes
Real-Time Clock Subsystem	RTCSS	Yes	Yes	Yes	Yes	Yes
Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem	PRU-ICSS	No	No	No	No	No
Multichannel Serial Peripheral Interface	McSPI	4	4	4	4	4

Table 3-1. Device Comparison(6) (continued)

Features		Device				
		TDA2PSxx	TDA2PHxx			
		TDA2PSXx	TDA2PHGx	TDA2PHFx	TDA2PHVx	TDA2PHAx
HDQ1W	HDQ1W	No	No	No	No	No
Quad SPI	QSPI	Yes	Yes	Yes	Yes	Yes
Spinlock Module	SPINLOCK	Yes	Yes	Yes	Yes	Yes
Keyboard Controller	KBD	No	No	No	No	No
Timers, General-Purpose	TIMER	16	16	16	16	16
Timer, Watchdog	WATCHDOG TIMER	Yes	Yes	Yes	Yes	Yes
Pulse-Width Modulation Subsystem	PWMSS1	Yes	Yes	Yes	Yes	Yes
	PWMSS2	Yes	Yes	Yes	Yes	Yes
	PWMSS3	Yes	Yes	Yes	Yes	Yes
Universal Asynchronous Receiver/Transmitter	UART	10	10	10	10	10
Universal Serial Bus (USB3.0)	USB1 (SuperSpeed, Dual-Role-Device [DRD])	Yes	Yes	Yes	Yes	Yes
Universal Serial Bus (USB2.0)	USB2 (HighSpeed, Dual-Role-Device [DRD], with embedded HS PHY)	Yes	Yes	Yes	Yes	Yes
	USB3 (HighSpeed, OTG2.0, with ULPI)	Yes	Yes	Yes	Yes	Yes
	USB4 (HighSpeed, OTG2.0, with ULPI)	Yes	Yes	Yes	Yes	Yes

(1) DSS clock jitter can be improved by providing an external clock source (via inputs vin1a_clk, vin1b_clk, wakeup0, wakeup1) or from internal SATA or PCIe PLLs.

(2) In the Unified L3 memory map, there is maximum of 2 GB of SDRAM space which is available to all L3 initiators including MPU (MPU, GPU, DSP, IVA, DMA, etc). Typically this space is interleaved across both EMIFs to optimize memory performance. If a system populates > 2 GB of physical memory, that additional addressable space can be accessed only by the MPU via the Arm V7 Large Physical Address Extensions (LPAE).

(3) DCAN1 has one pin mux option that can optionally be used for MCAN functionality. DCAN2 has two pin mux options, one of which can be optionally used for MCAN functionality.

(4) Wide Dynamic Range and Lens Distortion Correction.

(5) For more details about the CTRL_WKUP_STD_FUSE_DIE_ID_2 register and Base PN bitfield, see the *TDA2Px Technical Reference Manual*.

(6) X577Px is the base part number for the superset device. Software should constrain the features used to match the intended production device. The Base PN register bitfield value is 0x69.

3.2 Related Products

Automotive Processors

TDAx ADAS SoCs TI's TDAx Driver Assistance System-on-Chip (SoC) family offers scalable and open solutions and a common hardware and software architecture for Advanced Driver Assistance Systems (ADAS) applications including camera-based front (mono and stereo), rear, surround view and night vision systems, and mid- and long-range radar and sensor fusion systems.

Companion Products for TDA2 Review products that are frequently purchased or used in conjunction with this product.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the ball locations for the 760 plastic ball grid array (PBGA) package and are used in conjunction with Table 4-1 through Table 4-27 to locate signal names and ball grid numbers.

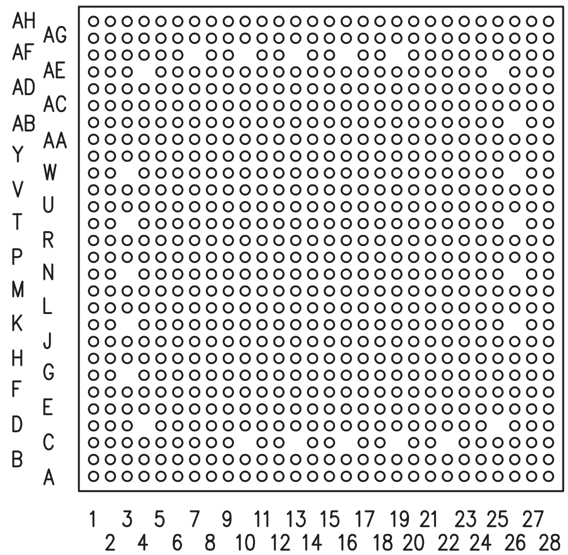


Figure 4-1. ABZ S-PBGA-N760 Package (Bottom View)

NOTE

The following bottom balls are not connected: AF7 / AF10 / AF13 / AF16 / AF19 / AE4 / AE25 / AB26 / W3 / W26 / T3 / T26 / N3 / N26 / K3 / K26 / G3 / D4 / D25 / C10 / C13 / C16 / C19 / C22.

These balls do not exist on the package.

4.2 Pin Attributes

Table 4-1 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL NUMBER:** Ball number(s) on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

NOTE

Table 4-1 does not take into account the subsystem multiplexing signals. The subsystem multiplexing signals are described in Section 4.3, *Signal Descriptions*.

NOTE

In the Driver off mode, the buffer is configured in high-impedance.

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4. **PHxx:** This column shows if the functionality is applicable for **TDA2PHxx** devices.
   Note that the Pin Attributes table presents the functionality of **TDA2PSxx** device.
   PHxx - TDA2PHGx; TDA2PHFx; TDA2PHVx; TDA2PHAx;

5. **MUXMODE:** Multiplexing mode number:
   a. MUXMODE 0 is the primary mode; this means that when MUXMODE = 0, the function mapped on the pin corresponds to the name of the pin. The primary muxmode is not necessarily the default muxmode.

   NOTE

   The default muxmode is the mode at the release of the reset; also see the RESET REL. MUXMODE column.

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   b. MUXMODE 1 through 15 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
   c. An empty box means Not Applicable
6. **TYPE:** Signal type and direction:
   – I = Input
   – O = Output
   – IO = Input or Output
   – D = Open drain
   – DS = Differential Signaling
   – A = Analog
   – PWR = Power
   – GND = Ground
   – CAP = LDO Capacitor
7. **BALL RESET STATE:** The state of the terminal at power-on reset:
   – drive 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated)
   – drive 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated)
   – OFF: High-impedance
   – PD: High-impedance with an active pulldown resistor
   – PU: High-impedance with an active pullup resistor
   – An empty box means Not Applicable
8. **BALL RESET REL. STATE:** The state of the terminal at the deactivation of the rstoutn signal (also mapped to the PRCM SYS_WARM_OUT_RST signal)
   – drive 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated)
   – drive clk (OFF): The buffer drives a toggling clock (pulldown or pullup resistor not activated)
   – drive 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated)
   – OFF: High-impedance
   – PD: High-impedance with an active pulldown resistor
   – PU: High-impedance with an active pullup resistor
   – An empty box means Not Applicable

   NOTE

   For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see the Power Reset and Clock Management / PRCM Reset Management Functional Description section of the Device TRM.

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9. **RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal (also mapped to the PRCM SYS_WARM_OUT_RST signal).

   An empty box means Not Applicable.
10. **IO VOLTAGE VALUE**: This column describes the IO voltage value (the corresponding power supply).

    An empty box means Not Applicable.
11. **POWER:** The voltage supply that powers the terminal IO buffers.

An empty box means Not Applicable.

12. **HYS:** Indicates if the input buffer is with hysteresis:
   – Yes: With hysteresis
   – No: Without hysteresis
   – An empty box: Not Applicable

NOTE

For more information, see the hysteresis values in Section 5.7, *Electrical Characteristics*.

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13. **BUFFER TYPE:** Drive strength of the associated output buffer.

   An empty box means Not Applicable.

NOTE

For programmable buffer strength:
– The default value is given in Table 4-1.
– A note describes all possible values according to the selected muxmode.

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14. **PULLUP / PULLDOWN TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
   – PU: Internal pullup
   – PD: Internal pulldown
   – PU/PD: Internal pullup and pulldown
   – PUx/PDy: Programmable internal pullup and pulldown
   – PDy: Programmable internal pulldown
   – An empty box means No pull
15. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0" or logic "1") when the peripheral pin function is not selected by any of the PINCNTLx registers.
   – 0: Logic 0 driven on the peripheral's input signal port.
   – 1: Logic 1 driven on the peripheral's input signal port.
   – blank: Pin state driven on the peripheral's input signal port.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad’s behavior is undefined. This should be avoided.

CAUTION

Peripherals exposed in Ball Characteristics Table and Pin Multiplexing Table represent functionality of a superset device. Not all exposed peripherals are supported on ADAS devices. For peripherals supported on ADAS family of products please refer to Table 3-1, *Device Comparison*.

NOTE

Some of the DDR1 and DDR2 signals have an additional state change at the release of porz. The state that the signals change to at the release of porz is as follows:

drive 0 (OFF) for: ddr1_csn0, ddr1_ck, ddr1_nck, ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_ba[2:0], ddr1_a[15:0], ddr2_csn0, ddr2_ck, ddr2_nck, ddr2_casn, ddr2_rasn, ddr2_wen, ddr2_ba[2:0], ddr2_a[15:0].

OFF for: ddr1_ecc_d[7:0], ddr1_dqm[3:0], ddr1_dqm_ecc, ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_dqs_ecc, ddr1_dqsn_ecc, ddr1_d[31:0], ddr2_dqm[3:0], ddr2_dqs[3:0], ddr2_dqsn[3:0], ddr2_d[31:0].

Table 4-1. Pin Attributes(1)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
K9	cap_vbbldo_dspeve	cap_vbbldo_dspeve			CAP									
Y14	cap_vbbldo_gpu	cap_vbbldo_gpu			CAP									
R20	cap_vbbldo_iva	cap_vbbldo_iva			CAP									
J16	cap_vbbldo_mpu	cap_vbbldo_mpu			CAP									
L9	cap_vddram_core1	cap_vddram_core1			CAP									
J19	cap_vddram_core2	cap_vddram_core2			CAP									
Y15	cap_vddram_core3	cap_vddram_core3			CAP									
P19	cap_vddram_core4	cap_vddram_core4			CAP									
Y16	cap_vddram_core5	cap_vddram_core5			CAP									
J10	cap_vddram_dspeve1	cap_vddram_dspeve1			CAP									
J9	cap_vddram_dspeve2	cap_vddram_dspeve2			CAP									
Y13	cap_vddram_gpu	cap_vddram_gpu			CAP									
T20	cap_vddram_iva	cap_vddram_iva			CAP									
K16	cap_vddram_mpu1	cap_vddram_mpu1			CAP									
K19	cap_vddram_mpu2	cap_vddram_mpu2			CAP									
G19	dcan1_rx	dcan1_rx mcan_rx		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		uart8_txd		2	O									
		mmc2_sdwp		3	I									0
		sata1_led		4	O									
		hdmi1_cec		6	IO									
		gpio1_15		14	IO									
		Driver off		15	I									
G20	dcan1_tx	dcan1_tx mcan_tx		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		uart8_rxd		2	I									1
		mmc2_sdcd		3	I									1
		hdmi1_hpd		6	I									
		gpio1_14		14	IO									
		Driver off		15	I									
AD20	ddr1_a0	ddr1_a0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC19	ddr1_a1	ddr1_a1		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC20	ddr1_a2	ddr1_a2		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AB19	ddr1_a3	ddr1_a3		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AF21	ddr1_a4	ddr1_a4		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AH22	ddr1_a5	ddr1_a5		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AG23	ddr1_a6	ddr1_a6		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AE21	ddr1_a7	ddr1_a7		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF22	ddr1_a8	ddr1_a8		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AE22	ddr1_a9	ddr1_a9		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AD21	ddr1_a10	ddr1_a10		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AD22	ddr1_a11	ddr1_a11		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC21	ddr1_a12	ddr1_a12		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF18	ddr1_a13	ddr1_a13		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AE17	ddr1_a14	ddr1_a14		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AD18	ddr1_a15	ddr1_a15		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF17	ddr1_ba0	ddr1_ba0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AE18	ddr1_ba1	ddr1_ba1		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AB18	ddr1_ba2	ddr1_ba2		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC18	ddr1_casn	ddr1_casn		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AG24	ddr1_ck	ddr1_ck		0	O	PD	drive clk (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AG22	ddr1_cke	ddr1_cke		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AH23	ddr1_csn0	ddr1_csn0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF25	ddr1_d0	ddr1_d0		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF26	ddr1_d1	ddr1_d1		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AG26	ddr1_d2	ddr1_d2		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AH26	ddr1_d3	ddr1_d3		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AF24	ddr1_d4	ddr1_d4		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AE24	ddr1_d5	ddr1_d5		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF23	ddr1_d6	ddr1_d6		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AE23	ddr1_d7	ddr1_d7		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC23	ddr1_d8	ddr1_d8		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF27	ddr1_d9	ddr1_d9		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AG27	ddr1_d10	ddr1_d10		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF28	ddr1_d11	ddr1_d11		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AE26	ddr1_d12	ddr1_d12		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC25	ddr1_d13	ddr1_d13		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC24	ddr1_d14	ddr1_d14		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AD25	ddr1_d15	ddr1_d15		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
V20	ddr1_d16	ddr1_d16		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
W20	ddr1_d17	ddr1_d17		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AB28	ddr1_d18	ddr1_d18		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC28	ddr1_d19	ddr1_d19		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC27	ddr1_d20	ddr1_d20		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
Y19	ddr1_d21	ddr1_d21		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AB27	ddr1_d22	ddr1_d22		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
Y20	ddr1_d23	ddr1_d23		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AA23	ddr1_d24	ddr1_d24		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
Y22	ddr1_d25	ddr1_d25		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
Y23	ddr1_d26	ddr1_d26		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AA24	ddr1_d27	ddr1_d27		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
Y24	ddr1_d28	ddr1_d28		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AA26	ddr1_d29	ddr1_d29		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AA25	ddr1_d30	ddr1_d30		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AA28	ddr1_d31	ddr1_d31		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AD23	ddr1_dqm0	ddr1_dqm0		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AB23	ddr1_dqm1	ddr1_dqm1		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AC26	ddr1_dqm2	ddr1_dqm2		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AA27	ddr1_dqm3	ddr1_dqm3		0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
V26	ddr1_dqm_ecc	ddr1_dqm_ecc	No	0	O	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AH25	ddr1_dqs0	ddr1_dqs0		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
AE27	ddr1_dqs1	ddr1_dqs1		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
AD27	ddr1_dqs2	ddr1_dqs2		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
Y28	ddr1_dqs3	ddr1_dqs3		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
AG25	ddr1_dqsn0	ddr1_dqsn0		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
AE28	ddr1_dqsn1	ddr1_dqsn1		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
AD28	ddr1_dqsn2	ddr1_dqsn2		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
Y27	ddr1_dqsn3	ddr1_dqsn3		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
V28	ddr1_dqsn_ecc	ddr1_dqsn_ecc	No	0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
V27	ddr1_dqs_ecc	ddr1_dqs_ecc	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1		LVCMOS DDR	Pux/PDy	
W22	ddr1_ecc_d0	ddr1_ecc_d0	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
V23	ddr1_ecc_d1	ddr1_ecc_d1	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
W19	ddr1_ecc_d2	ddr1_ecc_d2	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
W23	ddr1_ecc_d3	ddr1_ecc_d3	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
Y25	ddr1_ecc_d4	ddr1_ecc_d4	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
V24	ddr1_ecc_d5	ddr1_ecc_d5	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
V25	ddr1_ecc_d6	ddr1_ecc_d6	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
Y26	ddr1_ecc_d7	ddr1_ecc_d7	No	0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AH24	ddr1_nck	ddr1_nck		0	O	PD	drive clk (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AE20	ddr1_odt0	ddr1_odt0		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AF20	ddr1_rasn	ddr1_rasn		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
AG21	ddr1_rst	ddr1_rst		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
Y18	ddr1_vref0	ddr1_vref0		0	PWR	OFF	OFF		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR		
AH21	ddr1_wen	ddr1_wen		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr1	No	LVCMOS DDR	Pux/PDy	
R25	ddr2_a0	ddr2_a0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
R26	ddr2_a1	ddr2_a1		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
R28	ddr2_a2	ddr2_a2		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
R27	ddr2_a3	ddr2_a3		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
P23	ddr2_a4	ddr2_a4		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
P22	ddr2_a5	ddr2_a5		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
P25	ddr2_a6	ddr2_a6		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
N20	ddr2_a7	ddr2_a7		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
P27	ddr2_a8	ddr2_a8		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
N27	ddr2_a9	ddr2_a9		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
N23	ddr2_a10	ddr2_a10		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
P26	ddr2_a11	ddr2_a11		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
N28	ddr2_a12	ddr2_a12		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
T22	ddr2_a13	ddr2_a13		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
R22	ddr2_a14	ddr2_a14		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
U22	ddr2_a15	ddr2_a15		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
U23	ddr2_ba0	ddr2_ba0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
U27	ddr2_ba1	ddr2_ba1		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
U26	ddr2_ba2	ddr2_ba2		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
U28	ddr2_casn	ddr2_casn		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
T28	ddr2_ck	ddr2_ck		0	O	PD	drive clk (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
U24	ddr2_cke	ddr2_cke		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
P24	ddr2_csn0	ddr2_csn0		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
E26	ddr2_d0	ddr2_d0		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
G25	ddr2_d1	ddr2_d1		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
F25	ddr2_d2	ddr2_d2		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
F24	ddr2_d3	ddr2_d3		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
F26	ddr2_d4	ddr2_d4		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
F27	ddr2_d5	ddr2_d5		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
E27	ddr2_d6	ddr2_d6		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
E28	ddr2_d7	ddr2_d7		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
H23	ddr2_d8	ddr2_d8		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
H25	ddr2_d9	ddr2_d9		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
H24	ddr2_d10	ddr2_d10		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
H26	ddr2_d11	ddr2_d11		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
G26	ddr2_d12	ddr2_d12		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
J25	ddr2_d13	ddr2_d13		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
J26	ddr2_d14	ddr2_d14		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
J24	ddr2_d15	ddr2_d15		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
L22	ddr2_d16	ddr2_d16		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
K20	ddr2_d17	ddr2_d17		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
K21	ddr2_d18	ddr2_d18		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
L23	ddr2_d19	ddr2_d19		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
L24	ddr2_d20	ddr2_d20		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
J23	ddr2_d21	ddr2_d21		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
K22	ddr2_d22	ddr2_d22		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
J20	ddr2_d23	ddr2_d23		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
L27	ddr2_d24	ddr2_d24		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
L26	ddr2_d25	ddr2_d25		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
L25	ddr2_d26	ddr2_d26		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
L28	ddr2_d27	ddr2_d27		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
M23	ddr2_d28	ddr2_d28		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
M24	ddr2_d29	ddr2_d29		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
M25	ddr2_d30	ddr2_d30		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
M26	ddr2_d31	ddr2_d31		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
F28	ddr2_dqm0	ddr2_dqm0		0	O	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
G24	ddr2_dqm1	ddr2_dqm1		0	O	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
K23	ddr2_dqm2	ddr2_dqm2		0	O	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
M22	ddr2_dqm3	ddr2_dqm3		0	O	PU	PU		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
G28	ddr2_dqs0	ddr2_dqs0		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr2		LVCMOS DDR	Pux/PDy	
H27	ddr2_dqs1	ddr2_dqs1		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr2		LVCMOS DDR	Pux/PDy	
K27	ddr2_dqs2	ddr2_dqs2		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr2		LVCMOS DDR	Pux/PDy	
M28	ddr2_dqs3	ddr2_dqs3		0	IO	PD	PD		1.35/1.5/1.8	vdds_ddr2		LVCMOS DDR	Pux/PDy	
G27	ddr2_dqsn0	ddr2_dqsn0		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2		LVCMOS DDR	Pux/PDy	
H28	ddr2_dqsn1	ddr2_dqsn1		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2		LVCMOS DDR	Pux/PDy	
K28	ddr2_dqsn2	ddr2_dqsn2		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2		LVCMOS DDR	Pux/PDy	
M27	ddr2_dqsn3	ddr2_dqsn3		0	IO	PU	PU		1.35/1.5/1.8	vdds_ddr2		LVCMOS DDR	Pux/PDy	
T27	ddr2_nck	ddr2_nck		0	O	PD	drive clk (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
R23	ddr2_odt0	ddr2_odt0		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
T23	ddr2_rasn	ddr2_rasn		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
R24	ddr2_rst	ddr2_rst		0	O	PD	drive 0 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
N22	ddr2_vref0	ddr2_vref0		0	PWR	OFF	OFF		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR		
U25	ddr2_wen	ddr2_wen		0	O	PD	drive 1 (OFF)		1.35/1.5/1.8	vdds_ddr2	No	LVCMOS DDR	Pux/PDy	
G21	emu0	emu0		0	IO	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_30		14	IO									
D24	emu1	emu1		0	IO	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_31		14	IO									
AC5	gpio6_10	gpio6_10		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	
		mdio_mclk		1	O									1
		i2c3_sda		2	IO									1
		usb3_ulpi_d7		3	IO									0
		vin2b_hsync1		4	I									
		ehrpwm2A		10	O									
		gpio6_10		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AB4	gpio6_11	gpio6_11		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	
		mdio_d		1	IO									1
		i2c3_scl		2	IO									1
		usb3_ulpi_d6		3	IO									0
		vin2b_vsync1		4	I									
		ehrpwm2B		10	O									
		gpio6_11		14	IO									
		Driver off		15	I									
E21	gpio6_14	gpio6_14		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp1_axr8		1	IO									0
		dcan2_tx mcan_tx		2	IO									
		uart10_rxd		3	I									1
		vout2_hsync		6	O									
		vin4a_hsync0		8	I									0
		i2c3_sda		9	IO									1
		timer1		10	IO									
		gpio6_14		14	IO									
		Driver off		15	I									
F20	gpio6_15	gpio6_15		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp1_axr9		1	IO									0
		dcan2_rx mcan_rx		2	IO									
		uart10_txd		3	O									
		vout2_vsync		6	O									
		vin4a_vsync0		8	I									0
		i2c3_scl		9	IO									1
		timer2		10	IO									
		gpio6_15		14	IO									
		Driver off		15	I									
F21	gpio6_16	gpio6_16		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp1_axr10		1	IO									0
		vout2_fld		6	O									
		vin4a_fld0		8	I									0
		clkout1		9	O									
		timer3		10	IO									
		gpio6_16		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
R6	gpmc_a0	gpmc_a0		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d16		2	I									0
		vout3_d16		3	O									
		vin4a_d0		4	I									0
		vin4b_d0		6	I									0
		i2c4_scl		7	IO									1
		uart5_rxd		8	I									1
		gpio7_3 gpmc_a26 gpmc_a16		14	IO									
		Driver off		15	I									
T9	gpmc_a1	gpmc_a1		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d17		2	I									0
		vout3_d17		3	O									
		vin4a_d1		4	I									0
		vin4b_d1		6	I									0
		i2c4_sda		7	IO									1
		uart5_txd		8	O									
		gpio7_4		14	IO									
		Driver off		15	I									
T6	gpmc_a2	gpmc_a2		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d18		2	I									0
		vout3_d18		3	O									
		vin4a_d2		4	I									0
		vin4b_d2		6	I									0
		uart7_rxd		7	I									1
		uart5_ctsn		8	I									1
		gpio7_5		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
T7	gpmc_a3	gpmc_a3		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs2		1	O									1
		vin3a_d19		2	I									0
		vout3_d19		3	O									
		vin4a_d3		4	I									0
		vin4b_d3		6	I									0
		uart7_txd		7	O									
		uart5_rtsn		8	O									
		gpio7_6		14	IO									
		Driver off		15	I									
P6	gpmc_a4	gpmc_a4		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs3		1	O									1
		vin3a_d20		2	I									0
		vout3_d20		3	O									
		vin4a_d4		4	I									0
		vin4b_d4		6	I									0
		i2c5_scl		7	IO									1
		uart6_rxd		8	I									1
		gpio1_26		14	IO									
		Driver off		15	I									
R9	gpmc_a5	gpmc_a5		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d21		2	I									0
		vout3_d21		3	O									
		vin4a_d5		4	I									0
		vin4b_d5		6	I									0
		i2c5_sda		7	IO									1
		uart6_txd		8	O									
		gpio1_27		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
R5	gpmc_a6	gpmc_a6		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d22		2	I									0
		vout3_d22		3	O									
		vin4a_d6		4	I									0
		vin4b_d6		6	I									0
		uart8_rxd		7	I									1
		uart6_ctsn		8	I									1
		gpio1_28		14	IO									
		Driver off		15	I									
P5	gpmc_a7	gpmc_a7		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_d23		2	I									0
		vout3_d23		3	O									
		vin4a_d7		4	I									0
		vin4b_d7		6	I									0
		uart8_txd		7	O									
		uart6_rtsn		8	O									
		gpio1_29		14	IO									
		Driver off		15	I									
N7	gpmc_a8	gpmc_a8		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_hsync0		2	I									0
		vout3_hsync		3	O									
		vin4b_hsync1		6	I									0
		timer12		7	IO									
		spi4_sclk		8	IO									0
		gpio1_30		14	IO									
		Driver off		15	I									
R4	gpmc_a9	gpmc_a9		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_vsync0		2	I									0
		vout3_vsync		3	O									
		vin4b_vsync1		6	I									0
		timer11		7	IO									
		spi4_d1		8	IO									0
		gpio1_31		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
N9	gpmc_a10	gpmc_a10		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_de0		2	I									0
		vout3_de		3	O									
		vin4b_clk1		6	I									0
		timer10		7	IO									
		spi4_d0		8	IO									0
		gpio2_0		14	IO									
		Driver off		15	I									
P9	gpmc_a11	gpmc_a11		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin3a_fld0		2	I									0
		vout3_fld		3	O									
		vin4a_fld0		4	I									0
		vin4b_de1		6	I									0
		timer9		7	IO									
		spi4_cs0		8	IO									1
		gpio2_1		14	IO									
		Driver off		15	I									
P4	gpmc_a12	gpmc_a12		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		vin4a_clk0		4	I									0
		gpmc_a0		5	O									
		vin4b_fld1		6	I									0
		timer8		7	IO									
		spi4_cs1		8	IO									1
		dma_evt1		9	I									0
		gpio2_2		14	IO									
		Driver off		15	I									
R3	gpmc_a13	gpmc_a13		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_rtclk		1	I									0
		vin4a_hsync0		4	I									0
		timer7		7	IO									
		spi4_cs2		8	IO									1
		dma_evt2		9	I									0
		gpio2_3		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
T2	gpmc_a14	gpmc_a14		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_d3		1	I									0
		vin4a_vsync0		4	I									0
		timer6		7	IO									
		spi4_cs3		8	IO									1
		gpio2_4		14	IO									
		Driver off		15	I									
U2	gpmc_a15	gpmc_a15		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_d2		1	I									0
		vin4a_d8		4	I									0
		timer5		7	IO									
		gpio2_5		14	IO									
		Driver off		15	I									
U1	gpmc_a16	gpmc_a16		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_d0		1	IO									0
		vin4a_d9		4	I									0
		gpio2_6		14	IO									
		Driver off		15	I									
P3	gpmc_a17	gpmc_a17		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_d1		1	I									0
		vin4a_d10		4	I									0
		gpio2_7		14	IO									
		Driver off		15	I									
R2	gpmc_a18	gpmc_a18		0	O	PD	PD	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_sclk		1	O									
		vin4a_d11		4	I									0
		gpio2_8		14	IO									
		Driver off		15	I									
K7	gpmc_a19	gpmc_a19		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat4		1	IO									1
		gpmc_a13		2	O									
		vin4a_d12		4	I									0
		vin3b_d0		6	I									0
		gpio2_9		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
M7	gpmc_a20	gpmc_a20		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat5		1	IO									1
		gpmc_a14		2	O									
		vin4a_d13		4	I									0
		vin3b_d1		6	I									0
		gpio2_10		14	IO									
		Driver off		15	I									
J5	gpmc_a21	gpmc_a21		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat6		1	IO									1
		gpmc_a15		2	O									
		vin4a_d14		4	I									0
		vin3b_d2		6	I									0
		gpio2_11		14	IO									
		Driver off		15	I									
K6	gpmc_a22	gpmc_a22		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat7		1	IO									1
		gpmc_a16		2	O									
		vin4a_d15		4	I									0
		vin3b_d3		6	I									0
		gpio2_12		14	IO									
		Driver off		15	I									
J7	gpmc_a23	gpmc_a23		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_clk		1	IO									1
		gpmc_a17		2	O									
		vin4a_fld0		4	I									0
		vin3b_d4		6	I									0
		gpio2_13		14	IO									
		Driver off		15	I									
J4	gpmc_a24	gpmc_a24		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat0		1	IO									1
		gpmc_a18		2	O									
		vin3b_d5		6	I									0
		gpio2_14		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
J6	gpmc_a25	gpmc_a25		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat1		1	IO									1
		gpmc_a19		2	O									
		vin3b_d6		6	I									0
		gpio2_15		14	IO									
		Driver off		15	I									
H4	gpmc_a26	gpmc_a26		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat2		1	IO									1
		gpmc_a20		2	O									
		vin3b_d7		6	I									0
		gpio2_16		14	IO									
		Driver off		15	I									
H5	gpmc_a27	gpmc_a27		0	O	PD	PD	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_dat3		1	IO									1
		gpmc_a21		2	O									
		vin3b_hsync1		6	I									0
		gpio2_17		14	IO									
		Driver off		15	I									
M6	gpmc_ad0	gpmc_ad0		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d0		2	I									0
		vout3_d0		3	O									
		gpio1_6		14	IO									
		sysboot0		15	I									
M2	gpmc_ad1	gpmc_ad1		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d1		2	I									0
		vout3_d1		3	O									
		gpio1_7		14	IO									
		sysboot1		15	I									
L5	gpmc_ad2	gpmc_ad2		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d2		2	I									0
		vout3_d2		3	O									
		gpio1_8		14	IO									
		sysboot2		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
M1	gpmc_ad3	gpmc_ad3		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d3		2	I									0
		vout3_d3		3	O									
		gpio1_9		14	IO									
		sysboot3		15	I									
L6	gpmc_ad4	gpmc_ad4		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d4		2	I									0
		vout3_d4		3	O									
		gpio1_10		14	IO									
		sysboot4		15	I									
L4	gpmc_ad5	gpmc_ad5		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d5		2	I									0
		vout3_d5		3	O									
		gpio1_11		14	IO									
		sysboot5		15	I									
L3	gpmc_ad6	gpmc_ad6		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d6		2	I									0
		vout3_d6		3	O									
		gpio1_12		14	IO									
		sysboot6		15	I									
L2	gpmc_ad7	gpmc_ad7		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d7		2	I									0
		vout3_d7		3	O									
		gpio1_13		14	IO									
		sysboot7		15	I									
L1	gpmc_ad8	gpmc_ad8		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d8		2	I									0
		vout3_d8		3	O									
		gpio7_18		14	IO									
		sysboot8		15	I									
K2	gpmc_ad9	gpmc_ad9		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d9		2	I									0
		vout3_d9		3	O									
		gpio7_19		14	IO									
		sysboot9		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
J1	gpmc_ad10	gpmc_ad10		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d10		2	I									0
		vout3_d10		3	O									
		gpio7_28		14	IO									
		sysboot10		15	I									
J2	gpmc_ad11	gpmc_ad11		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d11		2	I									0
		vout3_d11		3	O									
		gpio7_29		14	IO									
		sysboot11		15	I									
H1	gpmc_ad12	gpmc_ad12		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d12		2	I									0
		vout3_d12		3	O									
		gpio1_18		14	IO									
		sysboot12		15	I									
J3	gpmc_ad13	gpmc_ad13		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d13		2	I									0
		vout3_d13		3	O									
		gpio1_19		14	IO									
		sysboot13		15	I									
H2	gpmc_ad14	gpmc_ad14		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d14		2	I									0
		vout3_d14		3	O									
		gpio1_20		14	IO									
		sysboot14		15	I									
H3	gpmc_ad15	gpmc_ad15		0	IO	OFF	OFF	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_d15		2	I									0
		vout3_d15		3	O									
		gpio1_21		14	IO									
		sysboot15		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
N1	gpmc_advn_ale	gpmc_advn_ale		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs6		1	O									
		clkout2		2	O									
		gpmc_wait1		3	I									1
		vin4a_vsync0		4	I									0
		gpmc_a2		5	O									
		gpmc_a23		6	O									
		timer3		7	IO									
		i2c3_sda		8	IO									1
		dma_evt2		9	I									0
		gpio2_23 gpmc_a19		14	IO									
		Driver off		15	I									
N6	gpmc_ben0	gpmc_ben0		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs4		1	O									
		vin1b_hsync1	No	3	I									0
		vin3b_de1		6	I									0
		timer2		7	IO									
		dma_evt3		9	I									0
		gpio2_26 gpmc_a21		14	IO									
		Driver off		15	I									
M4	gpmc_ben1	gpmc_ben1		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpmc_cs5		1	O									
		vin1b_de1	No	3	I									0
		vin3b_clk1		4	I									0
		gpmc_a3		5	O									
		vin3b_fld1		6	I									0
		timer1		7	IO									
		dma_evt4		9	I									0
		gpio2_27 gpmc_a22		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
P7	gpmc_clk	gpmc_clk		0	IO	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpmc_cs7		1	O									
		clkout1		2	O									
		gpmc_wait1		3	I									1
		vin4a_hsync0		4	I									0
		vin4a_de0		5	I									0
		vin3b_clk1		6	I									0
		timer4		7	IO									
		i2c3_scl		8	IO									1
		dma_evt1		9	I									0
		gpio2_22 gpmc_a20		14	IO									
		Driver off		15	I									
T1	gpmc_cs0	gpmc_cs0		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_19		14	IO									
		Driver off		15	I									
H6	gpmc_cs1	gpmc_cs1		0	O	PU	PU	15	1.8/3.3	vddshv11	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc2_cmd		1	IO									1
		gpmc_a22		2	O									
		vin4a_de0		4	I									0
		vin3b_vsync1		6	I									0
		gpio2_18		14	IO									
		Driver off		15	I									
P2	gpmc_cs2	gpmc_cs2		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs0		1	O									1
		gpio2_20 gpmc_a23 gpmc_a13		14	IO									
		Driver off		15	I									
P1	gpmc_cs3	gpmc_cs3		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		qspi1_cs1		1	O									1
		vin3a_clk0		2	I									0
		vout3_clk		3	O									
		gpmc_a1		5	O									
		gpio2_21 gpmc_a24 gpmc_a14		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
M5	gpmc_oen_ren	gpmc_oen_ren		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_24		14	IO									
		Driver off		15	I									
N2	gpmc_wait0	gpmc_wait0		0	I	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	1
		gpio2_28 gpmc_a25 gpmc_a15		14	IO									
		Driver off		15	I									
M3	gpmc_wen	gpmc_wen		0	O	PU	PU	15	1.8/3.3	vddshv10	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio2_25		14	IO									
		Driver off		15	I									
AG16	hdmi1_clockx	hdmi1_clockx		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AH16	hdmi1_clocky	hdmi1_clocky		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AG17	hdmi1_data0x	hdmi1_data0x		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AH17	hdmi1_data0y	hdmi1_data0y		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AG18	hdmi1_data1x	hdmi1_data1x		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AH18	hdmi1_data1y	hdmi1_data1y		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AG19	hdmi1_data2x	hdmi1_data2x		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
AH19	hdmi1_data2y	hdmi1_data2y		0	O				1.8	vdda_hdmi		HDMIPHY	PDy	
C20	i2c1_scl	i2c1_scl		0	IO	OFF	OFF		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	
C21	i2c1_sda	i2c1_sda		0	IO	OFF	OFF		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	
F17	i2c2_scl	i2c2_scl		0	IO	OFF	OFF	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	1
		hdmi1_ddc_sda		1	IO									
		Driver off		15	I									
C25	i2c2_sda	i2c2_sda		0	IO	OFF	OFF	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS I2C	PU/PD	1
		hdmi1_ddc_scl		1	IO									
		Driver off		15	I									
AH15	ljcb_clkn	ljcb_clkn		0	IO				1.8	vdda_pcie		LJCB		
AG15	ljcb_clkp	ljcb_clkp		0	IO				1.8	vdda_pcie		LJCB		

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B14	mcasp1_aclkr	mcasp1_aclkr		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_axr2		1	IO									0
		vout2_d0		6	O									
		vin4a_d0		8	I									0
		i2c4_sda		10	IO									1
		gpio5_0		14	IO									
		Driver off		15	I									
C14	mcasp1_aclkx	mcasp1_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		i2c3_sda		10	IO									1
		gpio7_31		14	IO									
		Driver off		15	I									
G12	mcasp1_axr0	mcasp1_axr0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart6_rxd		3	I									1
		i2c5_sda		10	IO									1
		gpio5_2		14	IO									
		Driver off		15	I									
F12	mcasp1_axr1	mcasp1_axr1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart6_txd		3	O									
		i2c5_scl		10	IO									1
		gpio5_3		14	IO									
		Driver off		15	I									
G13	mcasp1_axr2	mcasp1_axr2		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_axr2		1	IO									0
		uart6_ctsn		3	I									1
		vout2_d2		6	O									
		vin4a_d2		8	I									0
		gpio5_4		14	IO									
		Driver off		15	I									
J11	mcasp1_axr3	mcasp1_axr3		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_axr3		1	IO									0
		uart6_rtsn		3	O									
		vout2_d3		6	O									
		vin4a_d3		8	I									0
		gpio5_5		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E12	mcasp1_axr4	mcasp1_axr4		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp4_axr2		1	IO									0
		vout2_d4		6	O									
		vin4a_d4		8	I									0
		gpio5_6		14	IO									
		Driver off		15	I									
F13	mcasp1_axr5	mcasp1_axr5		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp4_axr3		1	IO									0
		vout2_d5		6	O									
		vin4a_d5		8	I									0
		gpio5_7		14	IO									
		Driver off		15	I									
C12	mcasp1_axr6	mcasp1_axr6		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp5_axr2		1	IO									0
		vout2_d6		6	O									
		vin4a_d6		8	I									0
		gpio5_8		14	IO									
		Driver off		15	I									
D12	mcasp1_axr7	mcasp1_axr7		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp5_axr3		1	IO									0
		vout2_d7		6	O									
		vin4a_d7		8	I									0
		timer4		10	IO									
		gpio5_9		14	IO									
		Driver off		15	I									
B12	mcasp1_axr8	mcasp1_axr8		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_axr0		1	IO									0
		spi3_sclk		3	IO									0
		timer5		10	IO									
		gpio5_10		14	IO									
		Driver off		15	I									
A11	mcasp1_axr9	mcasp1_axr9		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_axr1		1	IO									0
		spi3_d1		3	IO									0
		timer6		10	IO									
		gpio5_11		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B13	mcasp1_axr10	mcasp1_axr10		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_aclkx		1	IO									0
		mcasp6_aclkr		2	IO									
		spi3_d0		3	IO									0
		timer7		10	IO									
		gpio5_12		14	IO									
		Driver off		15	I									
A12	mcasp1_axr11	mcasp1_axr11		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp6_fsx		1	IO									0
		mcasp6_fsr		2	IO									
		spi3_cs0		3	IO									1
		timer8		10	IO									
		gpio4_17		14	IO									
		Driver off		15	I									
E14	mcasp1_axr12	mcasp1_axr12		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_axr0		1	IO									0
		spi3_cs1		3	IO									1
		timer9		10	IO									
		gpio4_18		14	IO									
		Driver off		15	I									
A13	mcasp1_axr13	mcasp1_axr13		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_axr1		1	IO									0
		timer10		10	IO									
		gpio6_4		14	IO									
		Driver off		15	I									
G14	mcasp1_axr14	mcasp1_axr14		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_aclkx		1	IO									0
		mcasp7_aclkr		2	IO									
		timer11		10	IO									
		gpio6_5		14	IO									
		Driver off		15	I									
F14	mcasp1_axr15	mcasp1_axr15		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_fsx		1	IO									0
		mcasp7_fsr		2	IO									
		timer12		10	IO									
		gpio6_6		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
J14	mcasp1_fsr	mcasp1_fsr		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp7_axr3		1	IO									0
		vout2_d1		6	O									
		vin4a_d1		8	I									0
		i2c4_scl		10	IO									1
		gpio5_1		14	IO									
		Driver off		15	I									
D14	mcasp1_fsx	mcasp1_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		i2c3_scl		10	IO									1
		gpio7_30		14	IO									
		Driver off		15	I									
E15	mcasp2_aclkr	mcasp2_aclkr		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_axr2		1	IO									0
		vout2_d8		6	O									
		vin4a_d8		8	I									0
		Driver off		15	I									
A19	mcasp2_aclkx	mcasp2_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		Driver off		15	I									
B15	mcasp2_axr0	mcasp2_axr0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d10		6	O									
		vin4a_d10		8	I									0
		Driver off		15	I									
A15	mcasp2_axr1	mcasp2_axr1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d11		6	O									
		vin4a_d11		8	I									0
		Driver off		15	I									
C15	mcasp2_axr2	mcasp2_axr2		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp3_axr2		1	IO									0
		gpio6_8		14	IO									
		Driver off		15	I									
A16	mcasp2_axr3	mcasp2_axr3		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp3_axr3		1	IO									0
		gpio6_9		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
D15	mcasp2_axr4	mcasp2_axr4		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_axr0		1	IO									0
		vout2_d12		6	O									
		vin4a_d12		8	I									0
		gpio1_4		14	IO									
		Driver off		15	I									
B16	mcasp2_axr5	mcasp2_axr5		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_axr1		1	IO									0
		vout2_d13		6	O									
		vin4a_d13		8	I									0
		gpio6_7		14	IO									
		Driver off		15	I									
B17	mcasp2_axr6	mcasp2_axr6		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_aclkx		1	IO									0
		mcasp8_aclkr		2	IO									
		vout2_d14		6	O									
		vin4a_d14		8	I									0
		gpio2_29		14	IO									
		Driver off		15	I									
A17	mcasp2_axr7	mcasp2_axr7		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_fsx		1	IO									0
		mcasp8_fsr		2	IO									
		vout2_d15		6	O									
		vin4a_d15		8	I									0
		gpio1_5		14	IO									
		Driver off		15	I									
A20	mcasp2_fsr	mcasp2_fsr		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp8_axr3		1	IO									0
		vout2_d9		6	O									
		vin4a_d9		8	I									0
		Driver off		15	I									
A18	mcasp2_fsx	mcasp2_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B18	mcasp3_aclkx	mcasp3_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp3_aclkr		1	IO									
		mcasp2_axr12		2	IO									0
		uart7_rxd		3	I									1
		gpio5_13		14	IO									
		Driver off		15	I									
B19	mcasp3_axr0	mcasp3_axr0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp2_axr14		2	IO									0
		uart7_ctsn		3	I									1
		uart5_rxd		4	I									1
		Driver off		15	I									
C17	mcasp3_axr1	mcasp3_axr1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp2_axr15		2	IO									0
		uart7_rtsn		3	O									
		uart5_txd		4	O									
		Driver off		15	I									
F15	mcasp3_fsx	mcasp3_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp3_fsr		1	IO									
		mcasp2_axr13		2	IO									0
		uart7_txd		3	O									
		gpio5_14		14	IO									
		Driver off		15	I									
C18	mcasp4_aclkx	mcasp4_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp4_aclkr		1	IO									
		spi3_sclk		2	IO									0
		uart8_rxd		3	I									1
		i2c4_sda		4	IO									1
		vout2_d16		6	O									
		vin4a_d16		8	I									0
		Driver off		15	I									
G16	mcasp4_axr0	mcasp4_axr0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi3_d0		2	IO									0
		uart8_ctsn		3	I									1
		uart4_rxd		4	I									1
		vout2_d18		6	O									
		vin4a_d18		8	I									0
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
D17	mcasp4_axr1	mcasp4_axr1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi3_cs0		2	IO									1
		uart8_rtsn		3	O									
		uart4_txd		4	O									
		vout2_d19		6	O									
		vin4a_d19		8	I									0
		Driver off		15	I									
A21	mcasp4_fsx	mcasp4_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp4_fsr		1	IO									
		spi3_d1		2	IO									0
		uart8_txd		3	O									
		i2c4_scl		4	IO									1
		vout2_d17		6	O									
		vin4a_d17		8	I									0
		Driver off		15	I									
AA3	mcasp5_aclkx	mcasp5_aclkx		0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp5_aclkr		1	IO									
		spi4_sclk		2	IO									0
		uart9_rxd		3	I									1
		i2c5_sda		4	IO									1
		vout2_d20		6	O									
		vin4a_d20		8	I									0
		Driver off		15	I									
AB3	mcasp5_axr0	mcasp5_axr0		0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi4_d0		2	IO									0
		uart9_ctsn		3	I									1
		uart3_rxd		4	I									1
		vout2_d22		6	O									
		vin4a_d22		8	I									0
		Driver off		15	I									
AA4	mcasp5_axr1	mcasp5_axr1		0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		spi4_cs0		2	IO									1
		uart9_rtsn		3	O									
		uart3_txd		4	O									
		vout2_d23		6	O									
		vin4a_d23		8	I									0
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AB9	mcasp5_fsx	mcasp5_fsx		0	IO	PD	PD	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	0
		mcasp5_fsr		1	IO									
		spi4_d1		2	IO									0
		uart9_txd		3	O									
		i2c5_scl		4	IO									1
		vout2_d21		6	O									
		vin4a_d21		8	I									0
		Driver off		15	I									
U4	mdio_d	mdio_d		0	IO	PU	PU	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_ctsn		1	I									1
		mii0_txer		3	O									0
		vin2a_d0		4	I									0
		vin4b_d0		5	I									0
		gpio5_16		14	IO									
		Driver off		15	I									
V1	mdio_mclk	mdio_mclk		0	O	PU	PU	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rtsn		1	O									
		mii0_col		3	I									0
		vin2a_clk0		4	I									
		vin4b_clk1		5	I									0
		gpio5_15		14	IO									
		Driver off		15	I									
W6	mmc1_clk	mmc1_clk		0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO1833	PU/PD	1
		gpio6_21		14	IO									
		Driver off		15	I									
Y6	mmc1_cmd	mmc1_cmd		0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO1833	PU/PD	1
		gpio6_22		14	IO									
		Driver off		15	I									
AA6	mmc1_dat0	mmc1_dat0		0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO1833	PU/PD	1
		gpio6_23		14	IO									
		Driver off		15	I									
Y4	mmc1_dat1	mmc1_dat1		0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO1833	PU/PD	1
		gpio6_24		14	IO									
		Driver off		15	I									
AA5	mmc1_dat2	mmc1_dat2		0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO1833	PU/PD	1
		gpio6_25		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
Y3	mmc1_dat3	mmc1_dat3		0	IO	PU	PU	15	1.8/3.3	vddshv8	Yes	SDIO1833	PU/PD	1
		gpio6_26		14	IO									
		Driver off		15	I									
W7	mmc1_sdcd	mmc1_sdcd		0	I	PU	PU	15	1.8/3.3	vddshv8	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart6_rxd		3	I									1
		i2c4_sda		4	IO									1
		gpio6_27		14	IO									
		Driver off		15	I									
Y9	mmc1_sdwp	mmc1_sdwp		0	I	PD	PD	15	1.8/3.3	vddshv8	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart6_txd		3	O									
		i2c4_scl		4	IO									1
		gpio6_28		14	IO									
		Driver off		15	I									
AD4	mmc3_clk	mmc3_clk		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		usb3_ulpi_d5		3	IO									0
		vin2b_d7		4	I									0
		ehrpwm2_tripzone_input		10	IO									0
		gpio6_29		14	IO									
		Driver off		15	I									
AC4	mmc3_cmd	mmc3_cmd		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_sclk		1	IO									0
		usb3_ulpi_d4		3	IO									0
		vin2b_d6		4	I									0
		eCAP2_in_PWM2_out		10	IO									0
		gpio6_30		14	IO									
		Driver off		15	I									
AC7	mmc3_dat0	mmc3_dat0		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_d1		1	IO									0
		uart5_rxd		2	I									1
		usb3_ulpi_d3		3	IO									0
		vin2b_d5		4	I									0
		eQEP3A_in		10	I									0
		gpio6_31		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AC6	mmc3_dat1	mmc3_dat1		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_d0		1	IO									0
		uart5_txd		2	O									
		usb3_ulpi_d2		3	IO									0
		vin2b_d4		4	I									0
		eQEP3B_in		10	I									0
		gpio7_0		14	IO									
		Driver off		15	I									
AC9	mmc3_dat2	mmc3_dat2		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_cs0		1	IO									1
		uart5_ctsn		2	I									1
		usb3_ulpi_d1		3	IO									0
		vin2b_d3		4	I									0
		eQEP3_index		10	IO									0
		gpio7_1		14	IO									
		Driver off		15	I									
AC3	mmc3_dat3	mmc3_dat3		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi3_cs1		1	IO									1
		uart5_rtsn		2	O									
		usb3_ulpi_d0		3	IO									0
		vin2b_d2		4	I									0
		eQEP3_strobe		10	IO									0
		gpio7_2		14	IO									
		Driver off		15	I									
AC8	mmc3_dat4	mmc3_dat4		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_sclk		1	IO									0
		uart10_rxd		2	I									1
		usb3_ulpi_nxt		3	I									0
		vin2b_d1		4	I									0
		ehrpwm3A		10	O									
		gpio1_22		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AD6	mmc3_dat5	mmc3_dat5		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_d1		1	IO									0
		uart10_txd		2	O									
		usb3_ulpi_dir		3	I									0
		vin2b_d0		4	I									0
		ehrpwm3B		10	O									
		gpio1_23		14	IO									
		Driver off		15	I									
AB8	mmc3_dat6	mmc3_dat6		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_d0		1	IO									0
		uart10_ctsn		2	I									1
		usb3_ulpi_stp		3	O									
		vin2b_de1		4	I									
		ehrpwm3_tripzone_input		10	IO									0
		gpio1_24		14	IO									
		Driver off		15	I									
AB5	mmc3_dat7	mmc3_dat7		0	IO	PU	PU	15	1.8/3.3	vddshv7	Yes	Dual Voltage LVCMOS	PU/PD	1
		spi4_cs0		1	IO									1
		uart10_rtsn		2	O									
		usb3_ulpi_clk		3	I									0
		vin2b_clk1		4	I									
		eCAP3_in_PWM3_out		10	IO									0
		gpio1_25		14	IO									
		Driver off		15	I									
D21	nmin_dsp	nmin_dsp		0	I	PD	PD		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
Y11	on_off	on_off		0	O	PU	drive 1 (OFF)		1.8/3.3	vddshv5	Yes	BC1833IHHV	PU/PD	
AG13	pcie_rxn0	pcie_rxn0		0	I	OFF	OFF		1.8	vdda_pcie0		SERDES		
AG11	pcie_rxn1	pcie_rxn1	No	0	I	OFF	OFF		1.8	vdda_pcie1		SERDES		
AH13	pcie_rxp0	pcie_rxp0		0	I	OFF	OFF		1.8	vdda_pcie0		SERDES		
AH11	pcie_rxp1	pcie_rxp1	No	0	I	OFF	OFF		1.8	vdda_pcie1		SERDES		
AG14	pcie_txn0	pcie_txn0		0	O				1.8	vdda_pcie0		SERDES		
AG12	pcie_txn1	pcie_txn1	No	0	O				1.8	vdda_pcie1		SERDES		
AH14	pcie_txp0	pcie_txp0		0	O				1.8	vdda_pcie0		SERDES		
AH12	pcie_txp1	pcie_txp1	No	0	O				1.8	vdda_pcie1		SERDES		
F22	porz	porz		0	I				1.8/3.3	vddshv3	Yes	IHHV1833	PU/PD	

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E23	resetn	resetn		0	I	PU	PU		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
U5	rgmii0_rxc	rgmii0_rxc		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii1_txen		2	O									
		mii0_txclk		3	I									0
		vin2a_d5		4	I									0
		vin4b_d5		5	I									0
		usb4_ulpi_d2		6	IO									0
		gpio5_26		14	IO									
		Driver off		15	I									
V5	rgmii0_rxctl	rgmii0_rxctl		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii1_txd1		2	O									
		mii0_txd3		3	O									
		vin2a_d6		4	I									0
		vin4b_d6		5	I									0
		usb4_ulpi_d3		6	IO									0
		gpio5_27		14	IO									
		Driver off		15	I									
W2	rgmii0_rxd0	rgmii0_rxd0		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii0_txd0		1	O									
		mii0_txd0		3	O									
		vin2a_fld0		4	I									
		vin4b_fld1		5	I									0
		usb4_ulpi_d7		6	IO									0
		gpio5_31		14	IO									
		Driver off		15	I									
Y2	rgmii0_rxd1	rgmii0_rxd1		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii0_txd1		1	O									
		mii0_txd1		3	O									
		vin2a_d9		4	I									0
		usb4_ulpi_d6		6	IO									0
		gpio5_30		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
V3	rgmii0_rxd2	rgmii0_rxd2		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii0_txen		1	O									
		mii0_txen		3	O									
		vin2a_d8		4	I									0
		usb4_ulpi_d5		6	IO									0
		gpio5_29		14	IO									
		Driver off		15	I									
V4	rgmii0_rxd3	rgmii0_rxd3		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		rmii1_txd0		2	O									
		mii0_txd2		3	O									
		vin2a_d7		4	I									0
		vin4b_d7		5	I									0
		usb4_ulpi_d4		6	IO									0
		gpio5_28		14	IO									
		Driver off		15	I									
W9	rgmii0_txc	rgmii0_txc		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_ctsn		1	I									1
		rmii1_rxd1		2	I									0
		mii0_rxd3		3	I									0
		vin2a_d3		4	I									0
		vin4b_d3		5	I									0
		usb4_ulpi_clk		6	I									0
		spi3_d0		7	IO									0
		spi4_cs2		8	IO									1
		gpio5_20		14	IO									
		Driver off		15	I									
V9	rgmii0_txctl	rgmii0_txctl		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_rtsn		1	O									
		rmii1_rxd0		2	I									0
		mii0_rxd2		3	I									0
		vin2a_d4		4	I									0
		vin4b_d4		5	I									0
		usb4_ulpi_stp		6	O									
		spi3_cs0		7	IO									1
		spi4_cs3		8	IO									1
		gpio5_21		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
U6	rgmii0_txd0	rgmii0_txd0		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxd0		1	I									0
		mii0_rxd0		3	I									0
		vin2a_d10		4	I									0
		usb4_ulpi_d1		6	IO									0
		spi4_cs0		7	IO									1
		uart4_rtsn		8	O									
		gpio5_25		14	IO									
		Driver off		15	I									
V6	rgmii0_txd1	rgmii0_txd1		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxd1		1	I									0
		mii0_rxd1		3	I									0
		vin2a_vsync0		4	I									
		vin4b_vsync1		5	I									0
		usb4_ulpi_d0		6	IO									0
		spi4_d0		7	IO									0
		uart4_ctsn		8	IO									1
		gpio5_24		14	IO									
		Driver off		15	I									
U7	rgmii0_txd2	rgmii0_txd2		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_rxer		1	I									0
		mii0_rxer		3	I									0
		vin2a_hsync0		4	I									
		vin4b_hsync1		5	I									0
		usb4_ulpi_nxt		6	I									0
		spi4_d1		7	IO									0
		uart4_txd		8	O									
		gpio5_23		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
V7	rgmii0_txd3	rgmii0_txd3		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii0_crs		1	I									0
		mii0_crs		3	I									0
		vin2a_de0		4	I									
		vin4b_de1		5	I									0
		usb4_ulpi_dir		6	I									0
		spi4_sclk		7	IO									0
		uart4_rxd		8	I									1
		gpio5_22		14	IO									
		Driver off		15	I									
U3	RMII_MHZ_50_CLK	RMII_MHZ_50_CLK		0	IO	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2a_d11		4	I									0
		gpio5_17		14	IO									
		Driver off		15	I									
F23	rstoutn	rstoutn		0	O	PD	drive 1 (OFF)		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
E18	rtck	rtck		0	O	PU	drive clk (OFF)	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_29		14	IO									
AF14	rtc_iso	rtc_iso		0	I				1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
AE14	rtc_osc_xi_clkin32	rtc_osc_xi_clkin32		0	I				1.8	vdda_rtc	No	LVCMOS OSC		
AD14	rtc_osc_xo	rtc_osc_xo		0	O				1.8	vdda_rtc	No	LVCMOS OSC		
AB17	rtc_porz	rtc_porz		0	I				1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
AH9	sata1_rxn0	sata1_rxn0		0	I	OFF	OFF		1.8	vdda_sata		SATAPHY		
AG9	sata1_rxp0	sata1_rxp0		0	I	OFF	OFF		1.8	vdda_sata		SATAPHY		
AG10	sata1_txn0	sata1_txn0		0	O				1.8	vdda_sata		SATAPHY		
AH10	sata1_txp0	sata1_txp0		0	O				1.8	vdda_sata		SATAPHY		
A24	spi1_cs0	spi1_cs0		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		gpio7_10		14	IO									
		Driver off		15	I									
A22	spi1_cs1	spi1_cs1		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		sata1_led		2	O									
		spi2_cs1		3	IO									1
		gpio7_11		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B21	spi1_cs2	spi1_cs2		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart4_rxd		1	I									1
		mmc3_sdcd		2	I									1
		spi2_cs2		3	IO									1
		dcan2_tx		4	IO									1
		mdio_mclk		5	O									1
		hdmi1_hpd		6	I									
		gpio7_12		14	IO									
		Driver off		15	I									
B20	spi1_cs3	spi1_cs3		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart4_txd		1	O									
		mmc3_sdwp		2	I									0
		spi2_cs3		3	IO									1
		dcan2_rx		4	IO									1
		mdio_d		5	IO									1
		hdmi1_cec		6	IO									
		gpio7_13		14	IO									
		Driver off		15	I									
B25	spi1_d0	spi1_d0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_9		14	IO									
		Driver off		15	I									
F16	spi1_d1	spi1_d1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_8		14	IO									
		Driver off		15	I									
A25	spi1_sclk	spi1_sclk		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		gpio7_7		14	IO									
		Driver off		15	I									
B24	spi2_cs0	spi2_cs0		0	IO	PU	PU	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rtsn		1	O									
		uart5_txd		2	O									
		gpio7_17		14	IO									
		Driver off		15	I									
G17	spi2_d0	spi2_d0		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart3_ctsn		1	I									1
		uart5_rxd		2	I									1
		gpio7_16		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B22	spi2_d1	spi2_d1		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart3_txd		1	O									
		gpio7_15		14	IO									
		Driver off		15	I									
A26	spi2_sclk	spi2_sclk		0	IO	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	0
		uart3_rxd		1	I									1
		gpio7_14		14	IO									
		Driver off		15	I									
E20	tclk	tclk		0	I	PU	PU	0	1.8/3.3	vddshv3	Yes	IQ1833	PU/PD	
D23	tdi	tdi		0	I	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_27		14	I									
F19	tdo	tdo		0	O	PU	PU	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		gpio8_28		14	IO									
F18	tms	tms		0	IO	OFF	OFF	0	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
D20	trstn	trstn		0	I	PD	PD		1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
E25	uart1_ctsn	uart1_ctsn		0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart9_rxd		2	I									1
		mmc4_clk		3	IO									1
		gpio7_24		14	IO									
		Driver off		15	I									
C27	uart1_rtsn	uart1_rtsn		0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		uart9_txd		2	O									
		mmc4_cmd		3	IO									1
		gpio7_25		14	IO									
		Driver off		15	I									
B27	uart1_rxd	uart1_rxd		0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		mmc4_sdcd		3	I									1
		gpio7_22		14	IO									
		Driver off		15	I									
C26	uart1_txd	uart1_txd		0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		mmc4_sdwp		3	I									0
		gpio7_23		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
D27	uart2_ctsn	uart2_ctsn		0	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rxd		2	I									1
		mmc4_dat2		3	IO									1
		uart10_rxd		4	I									1
		uart1_dtrn		5	O									
		gpio1_16		14	IO									
		Driver off		15	I									
C28	uart2_rtsn	uart2_rtsn		0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_txd		1	O									
		uart3_irtx		2	O									
		mmc4_dat3		3	IO									1
		uart10_txd		4	O									
		uart1_rin		5	I									1
		gpio1_17		14	IO									
		Driver off		15	I									
D28	uart2_rxd	uart3_ctsn		1	I	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	1
		uart3_rctx		2	O									
		mmc4_dat0		3	IO									1
		uart2_rxd		4	I									1
		uart1_dcdn		5	I									1
		gpio7_26		14	IO									
		Driver off		15	I									
D26	uart2_txd	uart2_txd		0	O	PU	PU	15	1.8/3.3	vddshv4	Yes	Dual Voltage LVCMOS	PU/PD	
		uart3_rtsn		1	O									
		uart3_sd		2	O									
		mmc4_dat1		3	IO									1
		uart2_txd		4	O									
		uart1_dsrn		5	I									0
		gpio7_27		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
V2	uart3_rxd	uart3_rxd		0	I	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	1
		rmii1_crs		2	I									0
		mii0_rxdv		3	I									0
		vin2a_d1		4	I									0
		vin4b_d1		5	I									0
		spi3_sclk		7	IO									0
		gpio5_18		14	IO									
		Driver off		15	I									
Y1	uart3_txd	uart3_txd		0	O	PD	PD	15	1.8/3.3	vddshv9	Yes	Dual Voltage LVCMOS	PU/PD	
		rmii1_rxer		2	I									0
		mii0_rxclk		3	I									0
		vin2a_d2		4	I									0
		vin4b_d2		5	I									0
		spi3_d1		7	IO									0
		spi4_cs1		8	IO									1
		gpio5_19		14	IO									
		Driver off		15	I									
AC12	usb1_dm	usb1_dm		0	IO	OFF	OFF		3.3	vdda33v_usb1		USBPHY		
AD12	usb1_dp	usb1_dp		0	IO	OFF	OFF		3.3	vdda33v_usb1		USBPHY		
AB10	usb1_drvvbus	usb1_drvvbus		0	O	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	
		timer16		7	IO									
		gpio6_12		14	IO									
		Driver off		15	I									
AF11	usb2_dm	usb2_dm		0	IO				3.3	vdda33v_usb2	No	USBPHY		
AE11	usb2_dp	usb2_dp		0	IO				3.3	vdda33v_usb2	No	USBPHY		
AC10	usb2_drvvbus	usb2_drvvbus		0	O	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	
		timer15		7	IO									
		gpio6_13		14	IO									
		Driver off		15	I									
AF12	usb_rxn0	usb_rxn0		0	I	OFF	OFF		1.8	vdda_usb1		SERDES		
AE12	usb_rxp0	usb_rxp0		0	I	OFF	OFF		1.8	vdda_usb1		SERDES		
AC11	usb_txn0	usb_txn0		0	O				1.8	vdda_usb1		SERDES		
AD11	usb_txp0	usb_txp0		0	O				1.8	vdda_usb1		SERDES		

Table 4-1. Pin Attributes[1] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
H13, H14, J17, J18, L7, L8, N10, N13, P11, P12, P13, R11, R16, R19, T13, T16, T19, U13, U16, U8, U9, V16, V8	vdd	vdd			PWR									
K14	vpp	vpp[8]			PWR									
AA12	vdda33v_usb1	vdda33v_usb1			PWR									
Y12	vdda33v_usb2	vdda33v_usb2			PWR									
M14	vdda_abe_per	vdda_abe_per			PWR									
P16	vdda_ddr	vdda_ddr			PWR									
N11	vdda_debug	vdda_debug			PWR									
N12	vdda_dsp_eve	vdda_dsp_eve			PWR									
P15	vdda_gmac_core	vdda_gmac_core			PWR									
R14	vdda_gpu	vdda_gpu			PWR									
Y17	vdda_hdmi	vdda_hdmi			PWR									
R17	vdda_iva	vdda_iva			PWR									
N16	vdda_mpu	vdda_mpu			PWR									
AD16, AE16	vdda_osc	vdda_osc			PWR									
W14	vdda_pcie	vdda_pcie			PWR									
AA17	vdda_pcie0	vdda_pcie0			PWR									
AA16	vdda_pcie1	vdda_pcie1			PWR									
AB13	vdda_rtc	vdda_rtc			PWR									
V13	vdda_sata	vdda_sata			PWR									
AA13	vdda_usb1	vdda_usb1			PWR									
AB12	vdda_usb2	vdda_usb2			PWR									
W12	vdda_usb3	vdda_usb3			PWR									
P14	vdda_video	vdda_video			PWR									
G18, H17, M8, M9, N8, P8, R8, T8, V21, V22, W17, W18	vdds18v	vdds18v			PWR									
AA18, AA19, W21, Y21	vdds18v_ddr1	vdds18v_ddr1			PWR									
J21, J22, N21, P20, P21	vdds18v_ddr2	vdds18v_ddr2			PWR									
E3, E5, G4, G5, H8, H9	vddshv1	vddshv1			PWR									
B6, D10, E10, H10, H11	vddshv2	vddshv2			PWR									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B23, D16, D22, E16, E22, G15, H15, H16, H18, H19	vddshv3	vddshv3			PWR									
C24	vddshv4	vddshv4			PWR									
V12	vddshv5	vddshv5			PWR									
AD5, AD7, AE7, AF5	vddshv6	vddshv6			PWR									
AB6, AB7	vddshv7	vddshv7			PWR									
W8, Y8	vddshv8	vddshv8			PWR									
U10, W4, W5	vddshv9	vddshv9			PWR									
N4, N5, P10, R10, R7, T4, T5	vddshv10	vddshv10			PWR									
J8, K8	vddshv11	vddshv11			PWR									
AA21, AA22, AB21, AB22, AB24, AB25, AC22, AD26, AG20, AG28, AH27, W16, W27	vdds_ddr1	vdds_ddr1			PWR									
E24, G22, G23, H20, H21, H22, J27, L20, L21, M20, M21, T24, T25	vdds_ddr2	vdds_ddr2			PWR									
AA7, Y7	vdds_mlbp	vdds_mlbp			PWR									
J13, K10, K11, K12, K13, L10, L11, L12, M10, M11, M12, M13	vdd_dspeve	vdd_dspeve			PWR									
U11, U12, V10, V11, V14, W10, W11, W13	vdd_gpu	vdd_gpu			PWR									
U18, U19, V18, V19	vdd_iva	vdd_iva			PWR									
K17, K18, L15, L16, L17, L18, L19, M15, M16, M17, M18, N17, N18, P17, P18, R18	vdd_mpu	vdd_mpu			PWR									
AB15	vdd_rtc	vdd_rtc			PWR									
AG8	vin1a_clk0	vin1a_clk0	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d16		3	O									
		vout3_fld		4	O									
		gpio2_30		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AE8	vin1a_d0	vin1a_d0	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d7		3	O									
		vout3_d23		4	O									
		uart8_rxd		5	I									1
		ehrpwm1A		10	O									
		gpio3_4		14	IO									
		Driver off		15	I									
AD8	vin1a_d1	vin1a_d1	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d6		3	O									
		vout3_d22		4	O									
		uart8_txd		5	O									
		ehrpwm1B		10	O									
		gpio3_5		14	IO									
		Driver off		15	I									
AG7	vin1a_d2	vin1a_d2	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d5		3	O									
		vout3_d21		4	O									
		uart8_ctsn		5	I									1
		ehrpwm1_tripzone_input		10	IO									0
		gpio3_6		14	IO									
		Driver off		15	I									
AH6	vin1a_d3	vin1a_d3	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d4		3	O									
		vout3_d20		4	O									
		uart8_rtsn		5	O									
		eCAP1_in_PWM1_out		10	IO									0
		gpio3_7		14	IO									
		Driver off		15	I									
AH3	vin1a_d4	vin1a_d4	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d3		3	O									
		vout3_d19		4	O									
		ehrpwm1_synci		10	I									0
		gpio3_8		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AH5	vin1a_d5	vin1a_d5	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d2		3	O									
		vout3_d18		4	O									
		ehrpwm1_synco		10	O									
		gpio3_9		14	IO									
		Driver off		15	I									
AG6	vin1a_d6	vin1a_d6	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d1		3	O									
		vout3_d17		4	O									
		eQEP2A_in		10	I									0
		gpio3_10		14	IO									
		Driver off		15	I									
AH4	vin1a_d7	vin1a_d7	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout3_d0		3	O									
		vout3_d16		4	O									
		eQEP2B_in		10	I									0
		gpio3_11		14	IO									
		Driver off		15	I									
AG4	vin1a_d8	vin1a_d8	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d7	No	1	I									0
		vout3_d15		4	O									
		eQEP2_index		10	IO									0
		gpio3_12		14	IO									
		Driver off		15	I									
AG2	vin1a_d9	vin1a_d9	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d6	No	1	I									0
		vout3_d14		4	O									
		eQEP2_strobe		10	IO									0
		gpio3_13		14	IO									
		Driver off		15	I									
AG3	vin1a_d10	vin1a_d10	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d5	No	1	I									0
		vout3_d13		4	O									
		gpio3_14		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AG5	vin1a_d11	vin1a_d11	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d4	No	1	I									0
		vout3_d12		4	O									
		gpmc_a23		5	O									
		gpio3_15		14	IO									
		Driver off		15	I									
AF2	vin1a_d12	vin1a_d12	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d3	No	1	I									0
		usb3_ulpi_d7		2	IO									0
		vout3_d11		4	O									
		gpmc_a24		5	O									
		gpio3_16		14	IO									
		Driver off		15	I									
AF6	vin1a_d13	vin1a_d13	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d2	No	1	I									0
		usb3_ulpi_d6		2	IO									0
		vout3_d10		4	O									
		gpmc_a25		5	O									
		gpio3_17		14	IO									
		Driver off		15	I									
AF3	vin1a_d14	vin1a_d14	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d1	No	1	I									0
		usb3_ulpi_d5		2	IO									0
		vout3_d9		4	O									
		gpmc_a26		5	O									
		gpio3_18		14	IO									
		Driver off		15	I									
AF4	vin1a_d15	vin1a_d15	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d0	No	1	I									0
		usb3_ulpi_d4		2	IO									0
		vout3_d8		4	O									
		gpmc_a27		5	O									
		gpio3_19		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AF1	vin1a_d16	vin1a_d16	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d7	No	1	I									0
		usb3_ulpi_d3		2	IO									0
		vout3_d7		4	O									
		vin3a_d0		6	I									0
		gpio3_20		14	IO									
		Driver off		15	I									
AE3	vin1a_d17	vin1a_d17	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d6	No	1	I									0
		usb3_ulpi_d2		2	IO									0
		vout3_d6		4	O									
		vin3a_d1		6	I									0
		gpio3_21		14	IO									
		Driver off		15	I									
AE5	vin1a_d18	vin1a_d18	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d5	No	1	I									0
		usb3_ulpi_d1		2	IO									0
		vout3_d5		4	O									
		vin3a_d2		6	I									0
		gpio3_22		14	IO									
		Driver off		15	I									
AE1	vin1a_d19	vin1a_d19	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d4	No	1	I									0
		usb3_ulpi_d0		2	IO									0
		vout3_d4		4	O									
		vin3a_d3		6	I									0
		gpio3_23		14	IO									
		Driver off		15	I									
AE2	vin1a_d20	vin1a_d20	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d3	No	1	I									0
		usb3_ulpi_nxt		2	I									0
		vout3_d3		4	O									
		vin3a_d4		6	I									0
		gpio3_24		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AE6	vin1a_d21	vin1a_d21	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d2	No	1	I									0
		usb3_ulpi_dir		2	I									0
		vout3_d2		4	O									
		vin3a_d5		6	I									0
		gpio3_25		14	IO									
		Driver off		15	I									
AD2	vin1a_d22	vin1a_d22	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d1	No	1	I									0
		usb3_ulpi_stp		2	O									
		vout3_d1		4	O									
		vin3a_d6		6	I									0
		gpio3_26		14	IO									
		Driver off		15	I									
AD3	vin1a_d23	vin1a_d23	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_d0	No	1	I									0
		usb3_ulpi_clk		2	I									0
		vout3_d0		4	O									
		vin3a_d7		6	I									0
		gpio3_27		14	IO									
		Driver off		15	I									
AD9	vin1a_de0	vin1a_de0	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_hsync1	No	1	I									0
		vout3_d17		3	O									
		vout3_de		4	O									
		uart7_rxd		5	I									1
		timer16		7	IO									
		spi3_sclk		8	IO									0
		eQEP1A_in		10	I									0
		gpio3_0		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AF9	vin1a_fld0	vin1a_fld0	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_vsync1	No	1	I									0
		vout3_clk		4	O									
		uart7_txd		5	O									
		timer15		7	IO									
		spi3_d1		8	IO									0
		eQEP1B_in		10	I									0
		gpio3_1		14	IO									
		Driver off		15	I									
AE9	vin1a_hsync0	vin1a_hsync0	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_fld1	No	1	I									0
		vout3_hsync		4	O									
		uart7_ctsn		5	I									1
		timer14		7	IO									
		spi3_d0		8	IO									0
		eQEP1_index		10	IO									0
		gpio3_2		14	IO									
		Driver off		15	I									
AF8	vin1a_vsync0	vin1a_vsync0	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin1b_de1	No	1	I									0
		vout3_vsync		4	O									
		uart7_rtsn		5	O									
		timer13		7	IO									
		spi3_cs0		8	IO									1
		eQEP1_strobe		10	IO									0
		gpio3_3		14	IO									
		Driver off		15	I									
AH7	vin1b_clk1	vin1b_clk1	No	0	I	PD	PD	15	1.8/3.3	vddshv6	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin3a_clk0		6	I									0
		gpio2_31		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E1	vin2a_clk0	vin2a_clk0		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vout2_fld		4	O									
		emu5		5	O									
		eQEP1A_in		10	I									0
		gpio3_28 gpmc_a27 gpmc_a17		14	IO									
		Driver off		15	I									
F2	vin2a_d0	vin2a_d0		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d23		4	O									
		emu10		5	O									
		uart9_ctsn		7	I									1
		spi4_d0		8	IO									0
		ehrpwm1B		10	O									
		gpio4_1		14	IO									
		Driver off		15	I									
F3	vin2a_d1	vin2a_d1		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d22		4	O									
		emu11		5	O									
		uart9_rtsn		7	O									
		spi4_cs0		8	IO									1
		ehrpwm1_tripzone_input		10	IO									0
		gpio4_2		14	IO									
		Driver off		15	I									
D1	vin2a_d2	vin2a_d2		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d21		4	O									
		emu12		5	O									
		uart10_rxd		8	I									1
		eCAP1_in_PWM1_out		10	IO									0
		gpio4_3		14	IO									
		Driver off		15	I									
E2	vin2a_d3	vin2a_d3		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d20		4	O									
		emu13		5	O									
		uart10_txd		8	O									
		ehrpwm1_synci		10	I									0
		gpio4_4		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
D2	vin2a_d4	vin2a_d4		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d19		4	O									
		emu14		5	O									
		uart10_ctsn		8	I									1
		ehrpwm1_synco		10	O									
		gpio4_5		14	IO									
		Driver off		15	I									
F4	vin2a_d5	vin2a_d5		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d18		4	O									
		emu15		5	O									
		uart10_rtsn		8	O									
		eQEP2A_in		10	I									0
		gpio4_6		14	IO									
		Driver off		15	I									
C1	vin2a_d6	vin2a_d6		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d17		4	O									
		emu16		5	O									
		mii1_rxd1		8	I									0
		eQEP2B_in		10	I									0
		gpio4_7		14	IO									
		Driver off		15	I									
E4	vin2a_d7	vin2a_d7		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d16		4	O									
		emu17		5	O									
		mii1_rxd2		8	I									0
		eQEP2_index		10	IO									0
		gpio4_8		14	IO									
		Driver off		15	I									
F5	vin2a_d8	vin2a_d8		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d15		4	O									
		emu18		5	O									
		mii1_rxd3		8	I									0
		eQEP2_strobe		10	IO									0
		gpio4_9 gpmc_a26		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
E6	vin2a_d9	vin2a_d9		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vout2_d14		4	O									
		emu19		5	O									
		mii1_rxd0		8	I									0
		ehrpwm2A		10	O									
		gpio4_10 gpmc_a25		14	IO									
		Driver off		15	I									
D3	vin2a_d10	vin2a_d10		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		mdio_mclk		3	O									1
		vout2_d13		4	O									
		ehrpwm2B		10	O									
		gpio4_11 gpmc_a24		14	IO									
		Driver off		15	I									
F6	vin2a_d11	vin2a_d11		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		mdio_d		3	IO									1
		vout2_d12		4	O									
		ehrpwm2_tripzone_input		10	IO									0
		gpio4_12 gpmc_a23		14	IO									
		Driver off		15	I									
D5	vin2a_d12	vin2a_d12		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txc		3	O									
		vout2_d11		4	O									
		mii1_rxclk		8	I									0
		eCAP2_in_PWM2_out		10	IO									0
		gpio4_13		14	IO									
		Driver off		15	I									
C2	vin2a_d13	vin2a_d13		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txctl		3	O									
		vout2_d10		4	O									
		mii1_rxdv		8	I									0
		eQEP3A_in		10	I									0
		gpio4_14		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
C3	vin2a_d14	vin2a_d14		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txd3		3	O									
		vout2_d9		4	O									
		mii1_txclk		8	I									0
		eQEP3B_in		10	I									0
		gpio4_15		14	IO									
		Driver off		15	I									
C4	vin2a_d15	vin2a_d15		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		rgmii1_txd2		3	O									
		vout2_d8		4	O									
		mii1_txd0		8	O									
		eQEP3_index		10	IO									0
		gpio4_16		14	IO									
		Driver off		15	I									
B2	vin2a_d16	vin2a_d16		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d7		2	I									0
		rgmii1_txd1		3	O									
		vout2_d7		4	O									
		vin3a_d8		6	I									0
		mii1_txd1		8	O									
		eQEP3_strobe		10	IO									0
		gpio4_24		14	IO									
		Driver off		15	I									
D6	vin2a_d17	vin2a_d17		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d6		2	I									0
		rgmii1_txd0		3	O									
		vout2_d6		4	O									
		vin3a_d9		6	I									0
		mii1_txd2		8	O									
		ehrpwm3A		10	O									
		gpio4_25		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
C5	vin2a_d18	vin2a_d18		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d5		2	I									0
		rgmii1_rxc		3	I									0
		vout2_d5		4	O									
		vin3a_d10		6	I									0
		mii1_txd3		8	O									
		ehrpwm3B		10	O									
		gpio4_26		14	IO									
		Driver off		15	I									
A3	vin2a_d19	vin2a_d19		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d4		2	I									0
		rgmii1_rxctl		3	I									0
		vout2_d4		4	O									
		vin3a_d11		6	I									0
		mii1_txer		8	O									0
		ehrpwm3_tripzone_input		10	IO									0
		gpio4_27		14	IO									
		Driver off		15	I									
B3	vin2a_d20	vin2a_d20		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d3		2	I									0
		rgmii1_rxd3		3	I									0
		vout2_d3		4	O									
		vin3a_de0		5	I									0
		vin3a_d12		6	I									0
		mii1_rxer		8	I									0
		eCAP3_in_PWM3_out		10	IO									0
		gpio4_28		14	IO									
		Driver off		15	I									
B4	vin2a_d21	vin2a_d21		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d2		2	I									0
		rgmii1_rxd2		3	I									0
		vout2_d2		4	O									
		vin3a_fld0		5	I									0
		vin3a_d13		6	I									0
		mii1_col		8	I									0
		gpio4_29		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
B5	vin2a_d22	vin2a_d22		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d1		2	I									0
		rgmii1_rxd1		3	I									0
		vout2_d1		4	O									
		vin3a_hsync0		5	I									0
		vin3a_d14		6	I									0
		mii1_crs		8	I									0
		gpio4_30		14	IO									
		Driver off		15	I									
A4	vin2a_d23	vin2a_d23		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	0
		vin2b_d0		2	I									0
		rgmii1_rxd0		3	I									0
		vout2_d0		4	O									
		vin3a_vsync0		5	I									0
		vin3a_d15		6	I									0
		mii1_txen		8	O									
		gpio4_31		14	IO									
		Driver off		15	I									
G2	vin2a_de0	vin2a_de0		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2a_fld0		1	I									
		vin2b_fld1		2	I									
		vin2b_de1		3	I									
		vout2_de		4	O									
		emu6		5	O									
		eQEP1B_in		10	I									0
		gpio3_29		14	IO									
		Driver off		15	I									
H7	vin2a_fld0	vin2a_fld0		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_clk1		2	I									
		vout2_clk		4	O									
		emu7		5	O									
		eQEP1_index		10	IO									0
		gpio3_30 gpmc_a27 gpmc_a18		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
G1	vin2a_hsync0	vin2a_hsync0		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_hsync1		3	I									
		vout2_hsync		4	O									
		emu8		5	O									
		uart9_rxd		7	I									1
		spi4_sclk		8	IO									0
		eQEP1_strobe		10	IO									0
		gpio3_31 gpmc_a27		14	IO									
		Driver off		15	I									
G6	vin2a_vsync0	vin2a_vsync0		0	I	PD	PD	15	1.8/3.3	vddshv1	Yes	Dual Voltage LVCMOS	PU/PD	
		vin2b_vsync1		3	I									
		vout2_vsync		4	O									
		emu9		5	O									
		uart9_txd		7	O									
		spi4_d1		8	IO									0
		ehrpwm1A		10	O									
		gpio4_0		14	IO									
		Driver off		15	I									
D11	vout1_clk	vout1_clk		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin4a_fld0		3	I									0
		vin3a_fld0		4	I									0
		spi3_cs0		8	IO									1
		gpio4_19		14	IO									
		Driver off		15	I									
F11	vout1_d0	vout1_d0		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart5_rxd		2	I									1
		vin4a_d16		3	I									0
		vin3a_d16		4	I									0
		spi3_cs2		8	IO									1
		gpio8_0		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
G10	vout1_d1	vout1_d1		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart5_txd		2	O									
		vin4a_d17		3	I									0
		vin3a_d17		4	I									0
		gpio8_1		14	IO									
		Driver off		15	I									
F10	vout1_d2	vout1_d2		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu2		2	O									
		vin4a_d18		3	I									0
		vin3a_d18		4	I									0
		obs0		5	O									
		obs16		6	O									
		obs_irq1		7	O									
		gpio8_2		14	IO									
		Driver off		15	I									
G11	vout1_d3	vout1_d3		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu5		2	O									
		vin4a_d19		3	I									0
		vin3a_d19		4	I									0
		obs1		5	O									
		obs17		6	O									
		obs_dmarq1		7	O									
		gpio8_3		14	IO									
		Driver off		15	I									
E9	vout1_d4	vout1_d4		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu6		2	O									
		vin4a_d20		3	I									0
		vin3a_d20		4	I									0
		obs2		5	O									
		obs18		6	O									
		gpio8_4		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
F9	vout1_d5	vout1_d5		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu7		2	O									
		vin4a_d21		3	I									0
		vin3a_d21		4	I									0
		obs3		5	O									
		obs19		6	O									
		gpio8_5		14	IO									
		Driver off		15	I									
F8	vout1_d6	vout1_d6		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu8		2	O									
		vin4a_d22		3	I									0
		vin3a_d22		4	I									0
		obs4		5	O									
		obs20		6	O									
		gpio8_6		14	IO									
		Driver off		15	I									
E7	vout1_d7	vout1_d7		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu9		2	O									
		vin4a_d23		3	I									0
		vin3a_d23		4	I									0
		gpio8_7		14	IO									
		Driver off		15	I									
E8	vout1_d8	vout1_d8		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart6_rxd		2	I									1
		vin4a_d8		3	I									0
		vin3a_d8		4	I									0
		gpio8_8		14	IO									
		Driver off		15	I									
D9	vout1_d9	vout1_d9		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart6_txd		2	O									
		vin4a_d9		3	I									0
		vin3a_d9		4	I									0
		gpio8_9		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
D7	vout1_d10	vout1_d10		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu3		2	O									
		vin4a_d10		3	I									0
		vin3a_d10		4	I									0
		obs5		5	O									
		obs21		6	O									
		obs_irq2		7	O									
		gpio8_10		14	IO									
		Driver off		15	I									
D8	vout1_d11	vout1_d11		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu10		2	O									
		vin4a_d11		3	I									0
		vin3a_d11		4	I									0
		obs6		5	O									
		obs22		6	O									
		obs_dmarq2		7	O									
		gpio8_11		14	IO									
		Driver off		15	I									
A5	vout1_d12	vout1_d12		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu11		2	O									
		vin4a_d12		3	I									0
		vin3a_d12		4	I									0
		obs7		5	O									
		obs23		6	O									
		gpio8_12		14	IO									
		Driver off		15	I									
C6	vout1_d13	vout1_d13		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu12		2	O									
		vin4a_d13		3	I									0
		vin3a_d13		4	I									0
		obs8		5	O									
		obs24		6	O									
		gpio8_13		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
C8	vout1_d14	vout1_d14		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu13		2	O									
		vin4a_d14		3	I									0
		vin3a_d14		4	I									0
		obs9		5	O									
		obs25		6	O									
		gpio8_14		14	IO									
		Driver off		15	I									
C7	vout1_d15	vout1_d15		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu14		2	O									
		vin4a_d15		3	I									0
		vin3a_d15		4	I									0
		obs10		5	O									
		obs26		6	O									
		gpio8_15		14	IO									
		Driver off		15	I									
B7	vout1_d16	vout1_d16		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart7_rxd		2	I									1
		vin4a_d0		3	I									0
		vin3a_d0		4	I									0
		gpio8_16		14	IO									
		Driver off		15	I									
B8	vout1_d17	vout1_d17		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		uart7_txd		2	O									
		vin4a_d1		3	I									0
		vin3a_d1		4	I									0
		gpio8_17		14	IO									
		Driver off		15	I									
A7	vout1_d18	vout1_d18		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu4		2	O									
		vin4a_d2		3	I									0
		vin3a_d2		4	I									0
		obs11		5	O									
		obs27		6	O									
		gpio8_18		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
A8	vout1_d19	vout1_d19		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu15		2	O									
		vin4a_d3		3	I									0
		vin3a_d3		4	I									0
		obs12		5	O									
		obs28		6	O									
		gpio8_19		14	IO									
		Driver off		15	I									
C9	vout1_d20	vout1_d20		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu16		2	O									
		vin4a_d4		3	I									0
		vin3a_d4		4	I									0
		obs13		5	O									
		obs29		6	O									
		gpio8_20		14	IO									
		Driver off		15	I									
A9	vout1_d21	vout1_d21		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu17		2	O									
		vin4a_d5		3	I									0
		vin3a_d5		4	I									0
		obs14		5	O									
		obs30		6	O									
		gpio8_21		14	IO									
		Driver off		15	I									
B9	vout1_d22	vout1_d22		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu18		2	O									
		vin4a_d6		3	I									0
		vin3a_d6		4	I									0
		obs15		5	O									
		obs31		6	O									
		gpio8_22		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
A10	vout1_d23	vout1_d23		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		emu19		2	O									
		vin4a_d7		3	I									0
		vin3a_d7		4	I									0
		spi3_cs3		8	IO									1
		gpio8_23		14	IO									
		Driver off		15	I									
B10	vout1_de	vout1_de		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin4a_de0		3	I									0
		vin3a_de0		4	I									0
		spi3_d1		8	IO									0
		gpio4_20		14	IO									
		Driver off		15	I									
B11	vout1_fld	vout1_fld		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin4a_clk0		3	I									0
		vin3a_clk0		4	I									0
		spi3_cs1		8	IO									1
		gpio4_21		14	IO									
		Driver off		15	I									
C11	vout1_hsync	vout1_hsync		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin4a_hsync0		3	I									0
		vin3a_hsync0		4	I									0
		spi3_d0		8	IO									0
		gpio4_22		14	IO									
		Driver off		15	I									
E11	vout1_vsync	vout1_vsync		0	O	PD	PD	15	1.8/3.3	vddshv2	Yes	Dual Voltage LVCMOS	PU/PD	
		vin4a_vsync0		3	I									0
		vin3a_vsync0		4	I									0
		spi3_sclk		8	IO									0
		gpio4_23		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes[(1)] (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
A1, A14, A2, A23, A28, A6, AA10, AA14, AA15, AA20, AA8, AA9, AB14, AB20, AD1, AD24, AG1, AH1, AH2, AH20, AH28, AH8, B1, D13, D19, E13, E19, F1, F7, G7, G8, G9, H12, J12, J15, J28, K1, K15, K24, K25, K4, K5, L13, L14, M19, N14, N15, N19, N24, N25, P28, R1, R12, R13, R15, R21, T10, T11, T12, T14, T15, T17, T18, T21, U15, U17, U20, U21, V15, V17, W1, W15, W24, W25, W28, AD19, AE19, AD13, AE13, AE10, AA11, AB11, AD10, U14	vss	vss			GND									
AF15	vssa_osc0	vssa_osc0			GND									
AC14	vssa_osc1	vssa_osc1			GND									
AD17	Wakeup0	Wakeup0		0	I	OFF	OFF	15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		dcan1_rx		1	I									1
		gpio1_0		14	I									
		Driver off		15	I									
AC17	Wakeup1	Wakeup1		0	I	OFF	OFF	15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		dcan2_rx		1	I									1
		gpio1_1		14	I									
		Driver off		15	I									
AB16	Wakeup2	Wakeup2		0	I	OFF	OFF	15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		sys_nirq2		1	I									
		gpio1_2		14	I									
		Driver off		15	I									
AC16	Wakeup3	Wakeup3		0	I	OFF	OFF	15	1.8/3.3	vddshv5	Yes	IHHV1833	PU/PD	
		sys_nirq1		1	I									
		gpio1_3		14	I									
		Driver off		15	I									
AE15	xi_osc0	xi_osc0		0	I				1.8	vdda_osc	No	LVCMOS Analog		

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
AC15	xi_osc1	xi_osc1		0	I				1.8	vdda_osc	No	LVCMOS Analog		
AD15	xo_osc0	xo_osc0		0	O				1.8	vdda_osc	No	LVCMOS Analog		
AC13	xo_osc1	xo_osc1		0	A				1.8	vdda_osc	No	LVCMOS Analog		
D18	xref_clk0	xref_clk0		0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp2_axr8		1	IO									0
		mcasp1_axr4		2	IO									0
		mcasp1_ahclkx		3	O									
		mcasp5_ahclkx		4	O									
		clkout2		9	O									
		timer13		10	IO									
		gpio6_17		14	IO									
		Driver off		15	I									
E17	xref_clk1	xref_clk1		0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp2_axr9		1	IO									0
		mcasp1_axr5		2	IO									0
		mcasp2_ahclkx		3	O									
		mcasp6_ahclkx		4	O									
		timer14		10	IO									
		gpio6_18		14	IO									
		Driver off		15	I									
B26	xref_clk2	xref_clk2		0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp2_axr10		1	IO									0
		mcasp1_axr6		2	IO									0
		mcasp3_ahclkx		3	O									
		mcasp7_ahclkx		4	O									
		vout2_clk		6	O									
		vin4a_clk0		8	I									0
		timer15		10	IO									
		gpio6_19		14	IO									
		Driver off		15	I									

Table 4-1. Pin Attributes(1) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PHxx [4]	MUXMODE [5]	TYPE [6]	BALL RESET STATE [7]	BALL RESET REL. STATE [8]	BALL RESET REL. MUXMODE [9]	I/O VOLTAGE VALUE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]	DSIS [15]
C23	xref_clk3	xref_clk3		0	I	PD	PD	15	1.8/3.3	vddshv3	Yes	Dual Voltage LVCMOS	PU/PD	
		mcasp2_axr11		1	IO									0
		mcasp1_axr7		2	IO									0
		mcasp4_ahclkx		3	O									
		mcasp8_ahclkx		4	O									
		vout2_de		6	O									
		vin4a_de0		8	I									0
		clkout3		9	O									
		timer16		10	IO									
		gpio6_20		14	IO									
		Driver off		15	I									

(1) NA in this table stands for Not Applicable.

(2) For more information on recommended operating conditions, see Section 5.4, *Recommended Operating Conditions*.

(3) The pullup or pulldown block strength is equal to: minimum = 50 μA, typical = 100 μA, maximum = 250 μA.

(4) The output impedance settings of this IO cell are programmable; by default, the value is DS[1:0] = 10, this means 40 Ω. For more information on DS[1:0] register configuration, see the Device TRM.

(5) IO drive strength for usb1_dp, usb1_dm, usb2_dp and usb2_dm: minimum 18.3 mA, maximum 89 mA (for a power supply vdda33v_usb1 and vdda33v_usb2 = 3.46 V).

(6) Minimum PU = 900 Ω, maximum PU = 3.090 kΩ and minimum PD = 14.25 kΩ, maximum PD = 24.8 kΩ.
For more information, see chapter 7 of the USB2.0 specification, in particular section Signaling / Device Speed Identification.

(7) In PUx / PDy, x and y = 60 μA to 200 μA.
The output impedance settings (or drive strengths) of this IO are programmable (34 Ω, 40 Ω, 48 Ω, 60 Ω, 80 Ω) depending on the values of the I[2:0] registers.

(8) This signal is valid only for High-Security devices. For more details, see Section 5.8, *VPP Specification for One-Time Programmable (OTP) eFUSEs*. For General Purpose devices do not connect any signal, test point, or board trace to this signal.

4.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The name of the signal passing through the pin.

NOTE

The subsystem multiplexing signals are not described in Table 4-1 and Table 4-29.

2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input or output
   - D = Open Drain
   - DS = Differential Signaling
   - A = Analog
   - PWR = Power
   - GND = Ground
4. **BALL:** Associated ball(s) number

NOTE

For more information, see the Control Module / Control Module Register Manual section of the Device TRM.

4.3.1 VIP

NOTE

For more information, see the Video Input Port (VIP) section of the Device TRM.

CAUTION

The I/O timings provided in Section 5.10, *Timing Requirements and Switching Characteristics* are applicable for all combinations of signals for vin1. However, the timings are valid only for vin2, vin3, and vin4 if signals within a single IOSET are used. The IOSETs are defined in the Table 5-34, Table 5-35 and Table 5-36.

Table 4-2. VIP Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Video Input 1			
vin1a_clk0	Video Input 1 Port A Clock input.Input clock for 8-bit 16-bit or 24-bit Port A video capture. Input data is sampled on the CLK0 edge.	I	AG8
vin1a_de0	Video Input 1 Port A Data Enable input	I	AD9
vin1a_fld0	Video Input 1 Port A Field ID input	I	AF9
vin1a_hsync0	Video Input 1 Port A Horizontal Sync input	I	AE9
vin1a_vsync0	Video Input 1 Port A Vertical Sync input	I	AF8
vin1a_d0	Video Input 1 Port A Data input	I	AE8
vin1a_d1	Video Input 1 Port A Data input	I	AD8

Table 4-2. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin1a_d2	Video Input 1 Port A Data input	I	AG7
vin1a_d3	Video Input 1 Port A Data input	I	AH6
vin1a_d4	Video Input 1 Port A Data input	I	AH3
vin1a_d5	Video Input 1 Port A Data input	I	AH5
vin1a_d6	Video Input 1 Port A Data input	I	AG6
vin1a_d7	Video Input 1 Port A Data input	I	AH4
vin1a_d8	Video Input 1 Port A Data input	I	AG4
vin1a_d9	Video Input 1 Port A Data input	I	AG2
vin1a_d10	Video Input 1 Port A Data input	I	AG3
vin1a_d11	Video Input 1 Port A Data input	I	AG5
vin1a_d12	Video Input 1 Port A Data input	I	AF2
vin1a_d13	Video Input 1 Port A Data input	I	AF6
vin1a_d14	Video Input 1 Port A Data input	I	AF3
vin1a_d15	Video Input 1 Port A Data input	I	AF4
vin1a_d16	Video Input 1 Port A Data input	I	AF1
vin1a_d17	Video Input 1 Port A Data input	I	AE3
vin1a_d18	Video Input 1 Port A Data input	I	AE5
vin1a_d19	Video Input 1 Port A Data input	I	AE1
vin1a_d20	Video Input 1 Port A Data input	I	AE2
vin1a_d21	Video Input 1 Port A Data input	I	AE6
vin1a_d22	Video Input 1 Port A Data input	I	AD2
vin1a_d23	Video Input 1 Port A Data input	I	AD3
vin1b_hsync1	Video Input 1 Port B Horizontal Sync input	I	N6/ AD9
vin1b_vsync1	Video Input 1 Port B Vertical Sync input	I	AF9
vin1b_fld1	Video Input 1 Port B Field ID input	I	AE9
vin1b_de1	Video Input 1 Port B Data Enable input	I	AF8/ M4
vin1b_clk1	Video Input 1 Port B Clock input	I	AH7
vin1b_d0	Video Input 1 Port B Data input	I	AF4/ AD3
vin1b_d1	Video Input 1 Port B Data input	I	AF3/ AD2
vin1b_d2	Video Input 1 Port B Data input	I	AF6/ AE6
vin1b_d3	Video Input 1 Port B Data input	I	AF2/ AE2
vin1b_d4	Video Input 1 Port B Data input	I	AG5/ AE1
vin1b_d5	Video Input 1 Port B Data input	I	AG3/ AE5
vin1b_d6	Video Input 1 Port B Data input	I	AG2/ AE3
vin1b_d7	Video Input 1 Port B Data input	I	AG4/ AF1
Video Input 2			
vin2a_clk0	Video Input 2 Port A Clock input	I	E1 / V1
vin2a_de0	Video Input 2 Port A Data Enable input	I	G2 / V7
vin2a_fld0	Video Input 2 Port A Field ID input	I	G2 / H7 / W2
vin2a_hsync0	Video Input 2 Port A Horizontal Sync input	I	G1 / U7
vin2a_vsync0	Video Input 2 Port A Vertical Sync input	I	G6 / V6
vin2a_d0	Video Input 2 Port A Data input	I	F2 / U4
vin2a_d1	Video Input 2 Port A Data input	I	F3 / V2
vin2a_d2	Video Input 2 Port A Data input	I	D1 / Y1
vin2a_d3	Video Input 2 Port A Data input	I	E2 / W9
vin2a_d4	Video Input 2 Port A Data input	I	D2 / V9
vin2a_d5	Video Input 2 Port A Data input	I	F4 / U5

Table 4-2. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin2a_d6	Video Input 2 Port A Data input	I	C1 / V5
vin2a_d7	Video Input 2 Port A Data input	I	E4 / V4
vin2a_d8	Video Input 2 Port A Data input	I	F5 / V3
vin2a_d9	Video Input 2 Port A Data input	I	E6 / Y2
vin2a_d10	Video Input 2 Port A Data input	I	D3 / U6
vin2a_d11	Video Input 2 Port A Data input	I	F6 / U3
vin2a_d12	Video Input 2 Port A Data input	I	D5
vin2a_d13	Video Input 2 Port A Data input	I	C2
vin2a_d14	Video Input 2 Port A Data input	I	C3
vin2a_d15	Video Input 2 Port A Data input	I	C4
vin2a_d16	Video Input 2 Port A Data input	I	B2
vin2a_d17	Video Input 2 Port A Data input	I	D6
vin2a_d18	Video Input 2 Port A Data input	I	C5
vin2a_d19	Video Input 2 Port A Data input	I	A3
vin2a_d20	Video Input 2 Port A Data input	I	B3
vin2a_d21	Video Input 2 Port A Data input	I	B4
vin2a_d22	Video Input 2 Port A Data input	I	B5
vin2a_d23	Video Input 2 Port A Data input	I	A4
vin2b_clk1	Video Input 2 Port B Clock input	I	AB5/ H7
vin2b_de1	Video Input 2 Port B Data Enable input	I	AB8/ G2
vin2b_fld1	Video Input 2 Port B Field ID input	I	G2
vin2b_hsync1	Video Input 2 Port B Horizontal Sync input	I	AC5/ G1
vin2b_vsync1	Video Input 2 Port B Vertical Sync input	I	AB4/ G6
vin2b_d0	Video Input 2 Port B Data input	I	AD6/ A4
vin2b_d1	Video Input 2 Port B Data input	I	AC8/ B5
vin2b_d2	Video Input 2 Port B Data input	I	AC3/ B4
vin2b_d3	Video Input 2 Port B Data input	I	AC9/ B3
vin2b_d4	Video Input 2 Port B Data input	I	AC6/ A3
vin2b_d5	Video Input 2 Port B Data input	I	AC7/ C5
vin2b_d6	Video Input 2 Port B Data input	I	AC4/ D6
vin2b_d7	Video Input 2 Port B Data input	I	AD4/ B2
Video Input 3			
vin3a_clk0	Video Input 3 Port A Clock input	I	B11/ AH7/ P1
vin3a_de0	Video Input 3 Port A Data Enable input	I	N9/ B3/ B10
vin3a_fld0	Video Input 3 Port A Field ID input	I	P9/ B4/ D11
vin3a_hsync0	Video Input 3 Port A Horizontal Sync input	I	N7/ B5/ C11
vin3a_vsync0	Video Input 3 Port A Vertical Sync input	I	R4/ A4/ E11
vin3a_d0	Video Input 3 Port A Data input	I	M6/ AF1/ B7
vin3a_d1	Video Input 3 Port A Data input	I	M2/ AE3/ B8
vin3a_d2	Video Input 3 Port A Data input	I	L5/ AE5/ A7
vin3a_d3	Video Input 3 Port A Data input	I	M1/ AE1/ A8
vin3a_d4	Video Input 3 Port A Data input	I	L6/ AE2/ C9
vin3a_d5	Video Input 3 Port A Data input	I	L4/ AE6/ A9
vin3a_d6	Video Input 3 Port A Data input	I	L3/ AD2/ B9
vin3a_d7	Video Input 3 Port A Data input	I	L2/ AD3/ A10
vin3a_d8	Video Input 3 Port A Data input	I	L1/ B2/ E8
vin3a_d9	Video Input 3 Port A Data input	I	K2/ D6/ D9

Table 4-2. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin3a_d10	Video Input 3 Port A Data input	I	J1/ C5/ D7
vin3a_d11	Video Input 3 Port A Data input	I	J2/ A3/ D8
vin3a_d12	Video Input 3 Port A Data input	I	H1/ B3/ A5
vin3a_d13	Video Input 3 Port A Data input	I	J3/ B4/ C6
vin3a_d14	Video Input 3 Port A Data input	I	H2/ B5/ C8
vin3a_d15	Video Input 3 Port A Data input	I	H3/ A4/ C7
vin3a_d16	Video Input 3 Port A Data input	I	R6/ F11
vin3a_d17	Video Input 3 Port A Data input	I	T9/ G10
vin3a_d18	Video Input 3 Port A Data input	I	T6/ F10
vin3a_d19	Video Input 3 Port A Data input	I	T7/ G11
vin3a_d20	Video Input 3 Port A Data input	I	P6/ E9
vin3a_d21	Video Input 3 Port A Data input	I	R9/ F9
vin3a_d22	Video Input 3 Port A Data input	I	R5/ F8
vin3a_d23	Video Input 3 Port A Data input	I	P5/ E7
vin3b_clk1	Video Input 3 Port B Clock input	I	P7/ M4
vin3b_de1	Video Input 3 Port B Data Enable input	I	N6
vin3b_fld1	Video Input 3 Port A Field ID input	I	M4
vin3b_hsync1	Video Input 3 Port A Horizontal Sync input	I	H5
vin3b_vsync1	Video Input 3 Port A Vertical Sync input	I	H6
vin3b_d0	Video Input 3 Port B Data input	I	K7
vin3b_d1	Video Input 3 Port B Data input	I	M7
vin3b_d2	Video Input 3 Port B Data input	I	J5
vin3b_d3	Video Input 3 Port B Data input	I	K6
vin3b_d4	Video Input 3 Port B Data input	I	J7
vin3b_d5	Video Input 3 Port B Data input	I	J4
vin3b_d6	Video Input 3 Port B Data input	I	J6
vin3b_d7	Video Input 3 Port B Data input	I	H4
Video Input 4			
vin4a_clk0	Video Input 4 Port A Clock input	I	P4/ B26/ B11
vin4a_de0	Video Input 4 Port A Data Enable input	I	H6/ C23/ B10/ P7
vin4a_fld0	Video Input 4 Port A Field ID input	I	J7/ F21/ P9/ D11
vin4a_hsync0	Video Input 4 Port A Horizontal Sync input	I	R3/ E21/ C11/ P7
vin4a_vsync0	Video Input 4 Port A Vertical Sync input	I	T2/ F20/ E11/ N1
vin4a_d0	Video Input 4 Port A Data input	I	R6/ B7/ B14
vin4a_d1	Video Input 4 Port A Data input	I	T9/ B8/ J14
vin4a_d2	Video Input 4 Port A Data input	I	T6/ A7/ G13
vin4a_d3	Video Input 4 Port A Data input	I	T7/ A8/ J11
vin4a_d4	Video Input 4 Port A Data input	I	P6/ C9/ E12
vin4a_d5	Video Input 4 Port A Data input	I	R9/ A9/ F13
vin4a_d6	Video Input 4 Port A Data input	I	R5/ B9/ C12
vin4a_d7	Video Input 4 Port A Data input	I	P5/ A10/ D12
vin4a_d8	Video Input 4 Port A Data input	I	E8/ U2/ E15
vin4a_d9	Video Input 4 Port A Data input	I	D9/ U1/ A20
vin4a_d10	Video Input 4 Port A Data input	I	D7/ P3/ B15
vin4a_d11	Video Input 4 Port A Data input	I	D8/ R2/ A15
vin4a_d12	Video Input 4 Port A Data input	I	A5/ K7/ D15
vin4a_d13	Video Input 4 Port A Data input	I	C6/ M7/ B16

Table 4-2. VIP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vin4a_d14	Video Input 4 Port A Data input	I	C8/ J5/ B17
vin4a_d15	Video Input 4 Port A Data input	I	C7/ K6/ A17
vin4a_d16	Video Input 4 Port A Data input	I	C18/ F11
vin4a_d17	Video Input 4 Port A Data input	I	A21/ G10
vin4a_d18	Video Input 4 Port A Data input	I	G16/ F10
vin4a_d19	Video Input 4 Port A Data input	I	D17/ G11
vin4a_d20	Video Input 4 Port A Data input	I	AA3/ E9
vin4a_d21	Video Input 4 Port A Data input	I	AB9/ F9
vin4a_d22	Video Input 4 Port A Data input	I	AB3/ F8
vin4a_d23	Video Input 4 Port A Data input	I	AA4/ E7
vin4b_clk1	Video Input 4 Port B Clock input	I	N9/ V1
vin4b_de1	Video Input 4 Port B Data Enable input	I	P9/ V7
vin4b_fld1	Video Input 4 Port B Field ID input	I	P4/ W2
vin4b_hsync1	Video Input 4 Port B Horizontal Sync input	I	N7/ U7
vin4b_vsync1	Video Input 4 Port B Vertical Sync input	I	R4/ V6
vin4b_d0	Video Input 4 Port B Data input	I	R6/ U4
vin4b_d1	Video Input 4 Port B Data input	I	T9/ V2
vin4b_d2	Video Input 4 Port B Data input	I	T6/ Y1
vin4b_d3	Video Input 4 Port B Data input	I	T7/ W9
vin4b_d4	Video Input 4 Port B Data input	I	P6/ V9
vin4b_d5	Video Input 4 Port B Data input	I	R9/ U5
vin4b_d6	Video Input 4 Port B Data input	I	R5/ V5
vin4b_d7	Video Input 4 Port B Data input	I	P5/ V4

4.3.2 DSS

CAUTION

The I/O timings provided in Section 5.10, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 5-48 and Table 5-49.

Table 4-3. DSS Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
DPI Video Output 1			
vout1_clk	Video Output 1 Clock output	O	D11
vout1_de	Video Output 1 Data Enable output	O	B10
vout1_fld	Video Output 1 Field ID output. This signal is not used for embedded sync modes.	O	B11
vout1_hsync	Video Output 1 Horizontal Sync output. This signal is not used for embedded sync modes.	O	C11
vout1_vsync	Video Output 1 Vertical Sync output. This signal is not used for embedded sync modes.	O	E11
vout1_d0	Video Output 1 Data output	O	F11
vout1_d1	Video Output 1 Data output	O	G10
vout1_d2	Video Output 1 Data output	O	F10
vout1_d3	Video Output 1 Data output	O	G11
vout1_d4	Video Output 1 Data output	O	E9
vout1_d5	Video Output 1 Data output	O	F9

Table 4-3. DSS Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vout1_d6	Video Output 1 Data output	O	F8
vout1_d7	Video Output 1 Data output	O	E7
vout1_d8	Video Output 1 Data output	O	E8
vout1_d9	Video Output 1 Data output	O	D9
vout1_d10	Video Output 1 Data output	O	D7
vout1_d11	Video Output 1 Data output	O	D8
vout1_d12	Video Output 1 Data output	O	A5
vout1_d13	Video Output 1 Data output	O	C6
vout1_d14	Video Output 1 Data output	O	C8
vout1_d15	Video Output 1 Data output	O	C7
vout1_d16	Video Output 1 Data output	O	B7
vout1_d17	Video Output 1 Data output	O	B8
vout1_d18	Video Output 1 Data output	O	A7
vout1_d19	Video Output 1 Data output	O	A8
vout1_d20	Video Output 1 Data output	O	C9
vout1_d21	Video Output 1 Data output	O	A9
vout1_d22	Video Output 1 Data output	O	B9
vout1_d23	Video Output 1 Data output	O	A10
DPI Video Output 2			
vout2_clk	Video Output 2 Clock output	O	H7/ B26
vout2_de	Video Output 2 Data Enable output	O	G2/ C23
vout2_fld	Video Output 2 Field ID output. This signal is not used for embedded sync modes.	O	E1/ F21
vout2_hsync	Video Output 2 Horizontal Sync output. This signal is not used for embedded sync modes.	O	G1/ E21
vout2_vsync	Video Output 2 Vertical Sync output. This signal is not used for embedded sync modes.	O	G6/ F20
vout2_d0	Video Output 2 Data output	O	A4/ B14
vout2_d1	Video Output 2 Data output	O	B5/ J14
vout2_d2	Video Output 2 Data output	O	B4/ G13
vout2_d3	Video Output 2 Data output	O	B3/ J11
vout2_d4	Video Output 2 Data output	O	A3/ E12
vout2_d5	Video Output 2 Data output	O	C5/ F13
vout2_d6	Video Output 2 Data output	O	D6/ C12
vout2_d7	Video Output 2 Data output	O	B2/ D12
vout2_d8	Video Output 2 Data output	O	C4/ E15
vout2_d9	Video Output 2 Data output	O	C3/ A20
vout2_d10	Video Output 2 Data output	O	C2/ B15
vout2_d11	Video Output 2 Data output	O	D5/ A15
vout2_d12	Video Output 2 Data output	O	F6/ D15
vout2_d13	Video Output 2 Data output	O	D3/ B16
vout2_d14	Video Output 2 Data output	O	E6/ B17
vout2_d15	Video Output 2 Data output	O	F5/ A17
vout2_d16	Video Output 2 Data output	O	E4/ C18
vout2_d17	Video Output 2 Data output	O	C1/ A21
vout2_d18	Video Output 2 Data output	O	F4/ G16
vout2_d19	Video Output 2 Data output	O	D2/ D17
vout2_d20	Video Output 2 Data output	O	E2/ AA3
vout2_d21	Video Output 2 Data output	O	D1/ AB9
vout2_d22	Video Output 2 Data output	O	F3/ AB3

Table 4-3. DSS Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vout2_d23	Video Output 2 Data output	O	F2/ AA4
DPI Video Output 3			
vout3_clk	Video Output 3 Clock output	O	P1/ AF9
vout3_de	Video Output 3 Data Enable output	O	N9/ AD9
vout3_fld	Video Output 3 Field ID output. This signal is not used for embedded sync modes.	O	P9/ AG8
vout3_hsync	Video Output 3 Horizontal Sync output. This signal is not used for embedded sync modes.	O	N7/ AE9
vout3_vsync	Video Output 3 Vertical Sync output. This signal is not used for embedded sync modes.	O	R4/ AF8
vout3_d0	Video Output 3 Data output	O	M6/ AH4 / AD3
vout3_d1	Video Output 3 Data output	O	M2/ AG6 / AD2
vout3_d2	Video Output 3 Data output	O	L5/ AH5 / AE6
vout3_d3	Video Output 3 Data output	O	M1/ AH3 / AE2
vout3_d4	Video Output 3 Data output	O	L6/ AH6 / AE1
vout3_d5	Video Output 3 Data output	O	L4/ AG7 / AE5
vout3_d6	Video Output 3 Data output	O	L3/ AD8 / AE3
vout3_d7	Video Output 3 Data output	O	L2/ AE8 / AF1
vout3_d8	Video Output 3 Data output	O	L1/ AF4
vout3_d9	Video Output 3 Data output	O	K2/ AF3
vout3_d10	Video Output 3 Data output	O	J1/ AF6
vout3_d11	Video Output 3 Data output	O	J2/ AF2
vout3_d12	Video Output 3 Data output	O	H1/ AG5
vout3_d13	Video Output 3 Data output	O	J3/ AG3
vout3_d14	Video Output 3 Data output	O	H2/ AG2
vout3_d15	Video Output 3 Data output	O	H3/ AG4
vout3_d16	Video Output 3 Data output	O	R6/ AG8 / AH4
vout3_d17	Video Output 3 Data output	O	T9/ AD9 / AG6
vout3_d18	Video Output 3 Data output	O	T6/ AH5
vout3_d19	Video Output 3 Data output	O	T7/ AH3
vout3_d20	Video Output 3 Data output	O	P6/ AH6
vout3_d21	Video Output 3 Data output	O	R9/ AG7
vout3_d22	Video Output 3 Data output	O	R5/ AD8
vout3_d23	Video Output 3 Data output	O	P5/ AE8

4.3.3 HDMI

NOTE

For more information, see the Display Subsystem section of the Device TRM.

Table 4-4. HDMI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
hdmi1_cec	HDMI consumer electronic control	IOD	B20/ G19
hdmi1_hpd	HDMI display hot plug detect	IO	B21/ G20
hdmi1_ddc_scl	HDMI display data channel clock	IOD	C25
hdmi1_ddc_sda	HDMI display data channel data	IOD	F17
hdmi1_clockx	HDMI clock differential positive or negative	ODS	AG16
hdmi1_clocky	HDMI clock differential positive or negative	ODS	AH16
hdmi1_data2x	HDMI data 2 differential positive or negative	ODS	AG19

Table 4-4. HDMI Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
hdmi1_data2y	HDMI data 2 differential positive or negative	ODS	AH19
hdmi1_data1x	HDMI data 1 differential positive or negative	ODS	AG18
hdmi1_data1y	HDMI data 1 differential positive or negative	ODS	AH18
hdmi1_data0x	HDMI data 0 differential positive or negative	ODS	AG17
hdmi1_data0y	HDMI data 0 differential positive or negative	ODS	AH17

4.3.4 EMIF

NOTE

For more information, see the Memory Subsystem / EMIF Controller section of the Device TRM.

Table 4-5. EMIF Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
EMIF Channel 1			
ddr1_csn0	EMIF1 Chip Select 0	O	AH23
ddr1_cke	EMIF1 Clock Enable	O	AG22
ddr1_ck	EMIF1 Clock	O	AG24
ddr1_nck	EMIF1 Negative Clock	O	AH24
ddr1_odt0	EMIF1 On-Die Termination for Chip Select 0	O	AE20
ddr1_casn	EMIF1 Column Address Strobe	O	AC18
ddr1_rasn	EMIF1 Row Address Strobe	O	AF20
ddr1_wen	EMIF1 Write Enable	O	AH21
ddr1_rst	EMIF1 Reset output (DDR3-SDRAM only)	O	AG21
ddr1_ba0	EMIF1 Bank Address	O	AF17
ddr1_ba1	EMIF1 Bank Address	O	AE18
ddr1_ba2	EMIF1 Bank Address	O	AB18
ddr1_a0	EMIF1 Address Bus	O	AD20
ddr1_a1	EMIF1 Address Bus	O	AC19
ddr1_a2	EMIF1 Address Bus	O	AC20
ddr1_a3	EMIF1 Address Bus	O	AB19
ddr1_a4	EMIF1 Address Bus	O	AF21
ddr1_a5	EMIF1 Address Bus	O	AH22
ddr1_a6	EMIF1 Address Bus	O	AG23
ddr1_a7	EMIF1 Address Bus	O	AE21
ddr1_a8	EMIF1 Address Bus	O	AF22
ddr1_a9	EMIF1 Address Bus	O	AE22
ddr1_a10	EMIF1 Address Bus	O	AD21
ddr1_a11	EMIF1 Address Bus	O	AD22
ddr1_a12	EMIF1 Address Bus	O	AC21
ddr1_a13	EMIF1 Address Bus	O	AF18
ddr1_a14	EMIF1 Address Bus	O	AE17
ddr1_a15	EMIF1 Address Bus	O	AD18
ddr1_d0	EMIF1 Data Bus	IO	AF25
ddr1_d1	EMIF1 Data Bus	IO	AF26
ddr1_d2	EMIF1 Data Bus	IO	AG26
ddr1_d3	EMIF1 Data Bus	IO	AH26

Table 4-5. EMIF Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
ddr1_d4	EMIF1 Data Bus	IO	AF24
ddr1_d5	EMIF1 Data Bus	IO	AE24
ddr1_d6	EMIF1 Data Bus	IO	AF23
ddr1_d7	EMIF1 Data Bus	IO	AE23
ddr1_d8	EMIF1 Data Bus	IO	AC23
ddr1_d9	EMIF1 Data Bus	IO	AF27
ddr1_d10	EMIF1 Data Bus	IO	AG27
ddr1_d11	EMIF1 Data Bus	IO	AF28
ddr1_d12	EMIF1 Data Bus	IO	AE26
ddr1_d13	EMIF1 Data Bus	IO	AC25
ddr1_d14	EMIF1 Data Bus	IO	AC24
ddr1_d15	EMIF1 Data Bus	IO	AD25
ddr1_d16	EMIF1 Data Bus	IO	V20
ddr1_d17	EMIF1 Data Bus	IO	W20
ddr1_d18	EMIF1 Data Bus	IO	AB28
ddr1_d19	EMIF1 Data Bus	IO	AC28
ddr1_d20	EMIF1 Data Bus	IO	AC27
ddr1_d21	EMIF1 Data Bus	IO	Y19
ddr1_d22	EMIF1 Data Bus	IO	AB27
ddr1_d23	EMIF1 Data Bus	IO	Y20
ddr1_d24	EMIF1 Data Bus	IO	AA23
ddr1_d25	EMIF1 Data Bus	IO	Y22
ddr1_d26	EMIF1 Data Bus	IO	Y23
ddr1_d27	EMIF1 Data Bus	IO	AA24
ddr1_d28	EMIF1 Data Bus	IO	Y24
ddr1_d29	EMIF1 Data Bus	IO	AA26
ddr1_d30	EMIF1 Data Bus	IO	AA25
ddr1_d31	EMIF1 Data Bus	IO	AA28
ddr1_ecc_d0	EMIF1 ECC Data Bus	IO	W22
ddr1_ecc_d1	EMIF1 ECC Data Bus	IO	V23
ddr1_ecc_d2	EMIF1 ECC Data Bus	IO	W19
ddr1_ecc_d3	EMIF1 ECC Data Bus	IO	W23
ddr1_ecc_d4	EMIF1 ECC Data Bus	IO	Y25
ddr1_ecc_d5	EMIF1 ECC Data Bus	IO	V24
ddr1_ecc_d6	EMIF1 ECC Data Bus	IO	V25
ddr1_ecc_d7	EMIF1 ECC Data Bus	IO	Y26
ddr1_dqm0	EMIF1 Data Mask	O	AD23
ddr1_dqm1	EMIF1 Data Mask	O	AB23
ddr1_dqm2	EMIF1 Data Mask	O	AC26
ddr1_dqm3	EMIF1 Data Mask	O	AA27
ddr1_dqm_ecc	EMIF1 ECC Data Mask	O	V26
ddr1_dqs0	Data strobe 0 input/output for byte 0 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	AH25
ddr1_dqsn0	Data strobe 0 invert	IO	AG25
ddr1_dqs1	Data strobe 1 input/output for byte 1 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	AE27
ddr1_dqsn1	Data strobe 1 invert	IO	AE28

Table 4-5. EMIF Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
ddr1_dqs2	Data strobe 2 input/output for byte 2 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	AD27
ddr1_dqsn2	Data strobe 2 invert	IO	AD28
ddr1_dqs3	Data strobe 3 input/output for byte 3 of the 32-bit data bus. This signal is output to the EMIF1 memory when writing and input when reading.	IO	Y28
ddr1_dqsn3	Data strobe 3 invert	IO	Y27
ddr1_dqs_ecc	EMIF1 ECC Data strobe input/output. This signal is output to the EMIF1 memory when writing and input when reading.	IO	V27
ddr1_dqsn_ecc	EMIF1 ECC Complementary Data strobe	IO	V28
ddr1_vref0	Reference Power Supply EMIF1	A	Y18
EMIF Channel 2			
ddr2_csn0	EMIF2 Chip Select 0	O	P24
ddr2_cke	EMIF2 Clock Enable	O	U24
ddr2_ck	EMIF2 Clock	O	T28
ddr2_nck	EMIF2 Negative Clock	O	T27
ddr2_odt0	EMIF2 On-Die Termination for Chip Select 0	O	R23
ddr2_casn	EMIF2 Column Address Strobe	O	U28
ddr2_rasn	EMIF2 Row Address Strobe	O	T23
ddr2_wen	EMIF2 Write Enable	O	U25
ddr2_rst	EMIF2 Reset output (DDR3-SDRAM only)	O	R24
ddr2_ba0	EMIF2 Bank Address	O	U23
ddr2_ba1	EMIF2 Bank Address	O	U27
ddr2_ba2	EMIF2 Bank Address	O	U26
ddr2_a0	EMIF2 Address Bus	O	R25
ddr2_a1	EMIF2 Address Bus	O	R26
ddr2_a2	EMIF2 Address Bus	O	R28
ddr2_a3	EMIF2 Address Bus	O	R27
ddr2_a4	EMIF2 Address Bus	O	P23
ddr2_a5	EMIF2 Address Bus	O	P22
ddr2_a6	EMIF2 Address Bus	O	P25
ddr2_a7	EMIF2 Address Bus	O	N20
ddr2_a8	EMIF2 Address Bus	O	P27
ddr2_a9	EMIF2 Address Bus	O	N27
ddr2_a10	EMIF2 Address Bus	O	N23
ddr2_a11	EMIF2 Address Bus	O	P26
ddr2_a12	EMIF2 Address Bus	O	N28
ddr2_a13	EMIF2 Address Bus	O	T22
ddr2_a14	EMIF2 Address Bus	O	R22
ddr2_a15	EMIF2 Address Bus	O	U22
ddr2_d0	EMIF2 Data Bus	IO	E26
ddr2_d1	EMIF2 Data Bus	IO	G25
ddr2_d2	EMIF2 Data Bus	IO	F25
ddr2_d3	EMIF2 Data Bus	IO	F24
ddr2_d4	EMIF2 Data Bus	IO	F26
ddr2_d5	EMIF2 Data Bus	IO	F27
ddr2_d6	EMIF2 Data Bus	IO	E27
ddr2_d7	EMIF2 Data Bus	IO	E28
ddr2_d8	EMIF2 Data Bus	IO	H23

Table 4-5. EMIF Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
ddr2_d9	EMIF2 Data Bus	IO	H25
ddr2_d10	EMIF2 Data Bus	IO	H24
ddr2_d11	EMIF2 Data Bus	IO	H26
ddr2_d12	EMIF2 Data Bus	IO	G26
ddr2_d13	EMIF2 Data Bus	IO	J25
ddr2_d14	EMIF2 Data Bus	IO	J26
ddr2_d15	EMIF2 Data Bus	IO	J24
ddr2_d16	EMIF2 Data Bus	IO	L22
ddr2_d17	EMIF2 Data Bus	IO	K20
ddr2_d18	EMIF2 Data Bus	IO	K21
ddr2_d19	EMIF2 Data Bus	IO	L23
ddr2_d20	EMIF2 Data Bus	IO	L24
ddr2_d21	EMIF2 Data Bus	IO	J23
ddr2_d22	EMIF2 Data Bus	IO	K22
ddr2_d23	EMIF2 Data Bus	IO	J20
ddr2_d24	EMIF2 Data Bus	IO	L27
ddr2_d25	EMIF2 Data Bus	IO	L26
ddr2_d26	EMIF2 Data Bus	IO	L25
ddr2_d27	EMIF2 Data Bus	IO	L28
ddr2_d28	EMIF2 Data Bus	IO	M23
ddr2_d29	EMIF2 Data Bus	IO	M24
ddr2_d30	EMIF2 Data Bus	IO	M25
ddr2_d31	EMIF2 Data Bus	IO	M26
ddr2_dqm0	EMIF2 Data Mask	O	F28
ddr2_dqm1	EMIF2 Data Mask	O	G24
ddr2_dqm2	EMIF2 Data Mask	O	K23
ddr2_dqm3	EMIF2 Data Mask	O	M22
ddr2_dqs0	Data strobe 0 input/output for byte 0 of the 32-bit data bus. This signal is output to the EMIF2 memory when writing and input when reading.	IO	G28
ddr2_dqsn0	Data strobe 0 invert	IO	G27
ddr2_dqs1	Data strobe 1 input/output for byte 1 of the 32-bit data bus. This signal is output to the EMIF2 memory when writing and input when reading.	IO	H27
ddr2_dqsn1	Data strobe 1 invert	IO	H28
ddr2_dqs2	Data strobe 2 input/output for byte 2 of the 32-bit data bus. This signal is output to the EMIF2 memory when writing and input when reading.	IO	K27
ddr2_dqsn2	Data strobe 2 invert	IO	K28
ddr2_dqs3	Data strobe 3 input/output for byte 3 of the 32-bit data bus. This signal is output to the EMIF2 memory when writing and input when reading.	IO	M28
ddr2_dqsn3	Data strobe 3 invert	IO	M27
ddr2_vref0	Reference Power Supply EMIF2	A	N22

NOTE

DDR SDRAM Channel 2 is not supported by Vision High Surround, Vision High and Vision Mid devices.

For more details on the device differentiation, refer to Table 3-1, *Device Comparison*.

NOTE

The index numbers 1 and 2 which is part of the EMIF1 and EMIF2 signal prefixes (ddr1_* and ddr2_*) listed in Table 4-5, DDR2/DDR3/DDR3L SDRAM Signal Descriptions, column "SIGNAL NAME" not to be confused with DDR1 and DDR2 types of SDRAM memories.

4.3.5 GPMC

NOTE

For more information, see the Memory Subsystem / General-Purpose Memory Controller section of the Device TRM.

Table 4-6. GPMC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_ad0	GPMC Data 0 in A/D nonmultiplexed mode and additionally Address 1 in A/D multiplexed mode	IO	M6
gpmc_ad1	GPMC Data 1 in A/D nonmultiplexed mode and additionally Address 2 in A/D multiplexed mode	IO	M2
gpmc_ad2	GPMC Data 2 in A/D nonmultiplexed mode and additionally Address 3 in A/D multiplexed mode	IO	L5
gpmc_ad3	GPMC Data 3 in A/D nonmultiplexed mode and additionally Address 4 in A/D multiplexed mode	IO	M1
gpmc_ad4	GPMC Data 4 in A/D nonmultiplexed mode and additionally Address 5 in A/D multiplexed mode	IO	L6
gpmc_ad5	GPMC Data 5 in A/D nonmultiplexed mode and additionally Address 6 in A/D multiplexed mode	IO	L4
gpmc_ad6	GPMC Data 6 in A/D nonmultiplexed mode and additionally Address 7 in A/D multiplexed mode	IO	L3
gpmc_ad7	GPMC Data 7 in A/D nonmultiplexed mode and additionally Address 8 in A/D multiplexed mode	IO	L2
gpmc_ad8	GPMC Data 8 in A/D nonmultiplexed mode and additionally Address 9 in A/D multiplexed mode	IO	L1
gpmc_ad9	GPMC Data 9 in A/D nonmultiplexed mode and additionally Address 10 in A/D multiplexed mode	IO	K2
gpmc_ad10	GPMC Data 10 in A/D nonmultiplexed mode and additionally Address 11 in A/D multiplexed mode	IO	J1
gpmc_ad11	GPMC Data 11 in A/D nonmultiplexed mode and additionally Address 12 in A/D multiplexed mode	IO	J2
gpmc_ad12	GPMC Data 12 in A/D nonmultiplexed mode and additionally Address 13 in A/D multiplexed mode	IO	H1
gpmc_ad13	GPMC Data 13 in A/D nonmultiplexed mode and additionally Address 14 in A/D multiplexed mode	IO	J3
gpmc_ad14	GPMC Data 14 in A/D nonmultiplexed mode and additionally Address 15 in A/D multiplexed mode	IO	H2
gpmc_ad15	GPMC Data 15 in A/D nonmultiplexed mode and additionally Address 16 in A/D multiplexed mode	IO	H3
gpmc_a0	GPMC Address 0. Only used to effectively address 8-bit data nonmultiplexed memories	O	R6 / P4
gpmc_a1	GPMC address 1 in A/D nonmultiplexed mode and Address 17 in A/D multiplexed mode	O	T9 / P1
gpmc_a2	GPMC address 2 in A/D nonmultiplexed mode and Address 18 in A/D multiplexed mode	O	T6 / N1
gpmc_a3	GPMC address 3 in A/D nonmultiplexed mode and Address 19 in A/D multiplexed mode	O	T7 / M4
gpmc_a4	GPMC address 4 in A/D nonmultiplexed mode and Address 20 in A/D multiplexed mode	O	P6

Table 4-6. GPMC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_a5	GPMC address 5 in A/D nonmultiplexed mode and Address 21 in A/D multiplexed mode	O	R9
gpmc_a6	GPMC address 6 in A/D nonmultiplexed mode and Address 22 in A/D multiplexed mode	O	R5
gpmc_a7	GPMC address 7 in A/D nonmultiplexed mode and Address 23 in A/D multiplexed mode	O	P5
gpmc_a8	GPMC address 8 in A/D nonmultiplexed mode and Address 24 in A/D multiplexed mode	O	N7
gpmc_a9	GPMC address 9 in A/D nonmultiplexed mode and Address 25 in A/D multiplexed mode	O	R4
gpmc_a10	GPMC address 10 in A/D nonmultiplexed mode and Address 26 in A/D multiplexed mode	O	N9
gpmc_a11	GPMC address 11 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	P9
gpmc_a12	GPMC address 12 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	P4
gpmc_a13	GPMC address 13 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	R3 / K7 / P2
gpmc_a14	GPMC address 14 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	T2 / M7 / P1
gpmc_a15	GPMC address 15 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	U2 / J5 / N2
gpmc_a16	GPMC address 16 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	U1 / K6 / R6
gpmc_a17	GPMC address 17 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	P3 / J7 / E1
gpmc_a18	GPMC address 18 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	R2 / J4 / H7
gpmc_a19	GPMC address 19 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	K7(3) / J6 / N1
gpmc_a20	GPMC address 20 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	M7(3) / H4 / P7
gpmc_a21	GPMC address 21 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	J5(3) / H5 / N6
gpmc_a22	GPMC address 22 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	K6(3) / H6 / M4
gpmc_a23	GPMC address 23 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	J7/ AG5/ N1 / P2 / F6
gpmc_a24	GPMC address 24 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	J4(3) / AF2 / P1 / D3
gpmc_a25	GPMC address 25 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	J6(3) / AF6 / N2 / E6
gpmc_a26	GPMC address 26 in A/D nonmultiplexed mode and unused in A/D multiplexed mode	O	H4(3) / AF3 / R6 / F5
gpmc_a27	GPMC address 27 in A/D nonmultiplexed mode and Address 27 in A/D multiplexed mode	O	H5(3) / AF4 / E1 / H7 / G1
gpmc_cs0	GPMC Chip Select 0 (active low)	O	T1
gpmc_cs1	GPMC Chip Select 1 (active low)	O	H6
gpmc_cs2	GPMC Chip Select 2 (active low)	O	P2
gpmc_cs3	GPMC Chip Select 3 (active low)	O	P1
gpmc_cs4	GPMC Chip Select 4 (active low)	O	N6
gpmc_cs5	GPMC Chip Select 5 (active low)	O	M4
gpmc_cs6	GPMC Chip Select 6 (active low)	O	N1
gpmc_cs7	GPMC Chip Select 7 (active low)	O	P7
gpmc_clk(1)(2)	GPMC Clock output	IO	P7

Table 4-6. GPMC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpmc_advn_ale	GPMC address valid active low or address latch enable	O	N1
gpmc_oen_ren	GPMC output enable active low or read enable	O	M5
gpmc_wen	GPMC write enable active low	O	M3
gpmc_ben0	GPMC lower-byte enable active low	O	N6
gpmc_ben1	GPMC upper-byte enable active low	O	M4
gpmc_wait0	GPMC external indication of wait 0	I	N2
gpmc_wait1	GPMC external indication of wait 1	I	P7 / N1

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any non-monotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

(2) The gpio6_16.clkout1 signal can be used as an “always-on” alternative to gpmc_clk provided that the external device can support the associated timing. See Table 5-55, *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default* and Table 5-57, *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate* for timing information.

(3) The internal pull resistors for balls K7, M7, J5, K6, J4, J6, H4, H5 are permanently disabled when sysboot15 is set to 1 as described in the section Sysboot Configuration of the Device TRM. If internal pull-up/down resistors are desired on these balls then sysboot15 should be set to 0. If gpmc boot mode is used with SYSBOOT15 = 1 (not recommended) then external pull-downs should be implemented to keep the address bus at logic-0 value during boot since the gpmc ms-address bits are Hi-Z during boot.

4.3.6 Timers

NOTE

For more information, see the Timers section of the Device TRM.

Table 4-7. Timers Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
timer1	PWM output/event trigger input	IO	M4/ E21
timer2	PWM output/event trigger input	IO	N6/ F20
timer3	PWM output/event trigger input	IO	N1/ F21
timer4	PWM output/event trigger input	IO	P7/ D12
timer5	PWM output/event trigger input	IO	U2/ B12
timer6	PWM output/event trigger input	IO	T2/ A11
timer7	PWM output/event trigger input	IO	R3/ B13
timer8	PWM output/event trigger input	IO	P4/ A12
timer9	PWM output/event trigger input	IO	P9/ E14
timer10	PWM output/event trigger input	IO	N9/ A13
timer11	PWM output/event trigger input	IO	R4/ G14
timer12	PWM output/event trigger input	IO	N7/ F14
timer13	PWM output/event trigger input	IO	D18/ AF8
timer14	PWM output/event trigger input	IO	E17/ AE9
timer15	PWM output/event trigger input	IO	B26/ AF9/ AC10
timer16	PWM output/event trigger input	IO	C23/ AD9/ AB10

4.3.7 I2C

NOTE

For more information, see the Serial Communication Interface / I2C section of the Device TRM.

NOTE

I2C1 and I2C2 do not support HS mode.

Table 4-8. I2C Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Inter-Integrated Circuit Interface (I2C1)			
i2c1_scl	I2C1 Clock	IOD	C20
i2c1_sda	I2C1 Data	IOD	C21
Inter-Integrated Circuit Interface (I2C2)			
i2c2_scl	I2C2 Clock	IOD	F17
i2c2_sda	I2C2 Data	IOD	C25
Inter-Integrated Circuit Interface (I2C3)			
i2c3_scl	I2C3 Clock	IOD	P7/ D14/ AB4/ F20
i2c3_sda	I2C3 Data	IOD	N1/ C14/ AC5/ E21
Inter-Integrated Circuit Interface (I2C4)			
i2c4_scl	I2C4 Clock	IOD	R6/ J14/ A21/ Y9
i2c4_sda	I2C4 Data	IOD	T9/ B14/ C18/ W7
Inter-Integrated Circuit Interface (I2C5)			
i2c5_scl	I2C5 Clock	IOD	AB9/ P6/ F12
i2c5_sda	I2C5 Data	IOD	AA3/ R9/ G12

4.3.8 UART

NOTE

For more information, see the Serial Communication Interface /UART/IrDA/CIR section of the Device TRM.

Table 4-9. UART Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Universal Asynchronous Receiver/Transmitter (UART1)			
uart1_dcdn	UART1 Data Carrier Detect active low	I	D28
uart1_dsrn	UART1 Data Set Ready active Low	I	D26
uart1_dtrn	UART1 Data Terminal Ready active Low	O	D27
uart1_rin	UART1 Ring Indicator	I	C28
uart1_rxd	UART1 Receive Data	I	B27
uart1_txd	UART1 Transmit Data	O	C26
uart1_ctsn	UART1 Clear to Send active low	I	E25
uart1_rtsn	UART1 Request to Send active low	O	C27
Universal Asynchronous Receiver/Transmitter (UART2)			
uart2_rxd	UART2 Receive Data	I	D28
uart2_txd	UART2 Transmit Data	O	D26
uart2_ctsn	UART2 Clear to Send active low	I	D27
uart2_rtsn	UART2 Request to Send active low	O	C28
Universal Asynchronous Receiver/Transmitter (UART3)/IrDA			
uart3_rxd	UART3 Receive Data for both normal UART mode and IrDA mode	I	V2 / AB3 / A26/ D27
uart3_txd	UART3 Transmit Data	O	Y1/ B22/ C28/ AA4
uart3_ctsn	UART3 Clear to Send active low	I	U4/ W9/ G17/ D28
uart3_rtsn	UART3 Request to Send active low	O	V1/ V9/ D26/ B24

Table 4-9. UART Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
uart3_rctx	Remote control data	O	D28
uart3_sd	Infrared transceiver configure/shutdown	O	D26
uart3_irtx	Infrared data output	O	C28
Universal Asynchronous Receiver/Transmitter (UART4)			
uart4_rxd	UART4 Receive Data	I	V7/ G16/ B21
uart4_txd	UART4 Transmit Data	O	U7/ D17/ B20
uart4_ctsn	UART4 Clear to Send active low	I	V6
uart4_rtsn	UART4 Request to Send active low	O	U6
Universal Asynchronous Receiver/Transmitter (UART5)			
uart5_rxd	UART5 Receive Data	I	R6/ F11/ B19/ AC7/ G17
uart5_txd	UART5 Transmit Data	O	T9/ G10/ C17/ AC6/ B24
uart5_ctsn	UART5 Clear to Send active low	I	T6/ AC9
uart5_rtsn	UART5 Request to Send active low	O	T7/ AC3
Universal Asynchronous Receiver/Transmitter (UART6)			
uart6_rxd	UART6 Receive Data	I	P6/ E8/ G12/ W7
uart6_txd	UART6 Transmit Data	O	R9/ D9/ F12/ Y9
uart6_ctsn	UART6 Clear to Send active low	I	R5/ G13
uart6_rtsn	UART6 Request to Send active low	O	P5/ J11
Universal Asynchronous Receiver/Transmitter (UART7)			
uart7_rxd	UART7 Receive Data	I	T6/ AD9/ B7/ B18
uart7_txd	UART7 Transmit Data	O	T7/ AF9/ B8/ F15
uart7_ctsn	UART7 Clear to Send active low	I	AE9/ B19
uart7_rtsn	UART7 Request to Send active low	O	AF8/ C17
Universal Asynchronous Receiver/Transmitter (UART8)			
uart8_rxd	UART8 Receive Data	I	AE8/ R5/ C18/ G20
uart8_txd	UART8 Transmit Data	O	AD8/ P5/ A21/ G19
uart8_ctsn	UART8 Clear to Send active low	I	AG7/ G16
uart8_rtsn	UART8 Request to Send active low	O	AH6/ D17
Universal Asynchronous Receiver/Transmitter (UART9)			
uart9_rxd	UART9 Receive Data	I	G1/ AA3/ E25
uart9_txd	UART9 Transmit Data	O	G6/ AB9/ C27
uart9_ctsn	UART9 Clear to Send active low	I	F2/ AB3
uart9_rtsn	UART9 Request to Send active low	O	F3/ AA4
Universal Asynchronous Receiver/Transmitter (UART10)			
uart10_rxd	UART10 Receive Data	I	D1/ E21/ AC8/ D27
uart10_txd	UART10 Transmit Data	O	E2/ F20/ AD6/ C28
uart10_ctsn	UART10 Clear to Send active low	I	D2/ AB8
uart10_rtsn	UART10 Request to Send active low	O	F4/ AB5

4.3.9 McSPI

CAUTION

The I/O timings provided in Section 5.10, *Timing Requirements and Switching Characteristics* are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are valid only for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETS are defined in the Table 5-70.

NOTE

For more information, see the Serial Communication Interface / McSPI section of the Device TRM.

Table 4-10. SPI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Serial Peripheral Interface 1			
spi1_sclk(1)	SPI1 Clock	IO	A25
spi1_d1	SPI1 Data. Can be configured as either MISO or MOSI.	IO	F16
spi1_d0	SPI1 Data. Can be configured as either MISO or MOSI.	IO	B25
spi1_cs0	SPI1 Chip Select	IO	A24
spi1_cs1	SPI1 Chip Select	IO	A22
spi1_cs2	SPI1 Chip Select	IO	B21
spi1_cs3	SPI1 Chip Select	IO	B20
Serial Peripheral Interface 2			
spi2_sclk(1)	SPI2 Clock	IO	A26
spi2_d1	SPI2 Data. Can be configured as either MISO or MOSI.	IO	B22
spi2_d0	SPI2 Data. Can be configured as either MISO or MOSI.	IO	G17
spi2_cs0	SPI2 Chip Select	IO	B24
spi2_cs1	SPI2 Chip Select	IO	A22
spi2_cs2	SPI2 Chip Select	IO	B21
spi2_cs3	SPI2 Chip Select	IO	B20
Serial Peripheral Interface 3			
spi3_sclk(1)	SPI3 Clock	IO	AD9/ V2/ B12/ E11/ AC4/ C18
spi3_d1	SPI3 Data. Can be configured as either MISO or MOSI.	IO	AF9/ Y1/ B10/ A11/ A21/ AC7
spi3_d0	SPI3 Data. Can be configured as either MISO or MOSI.	IO	AE9/ W9/ C11/ B13/ AC6/ G16
spi3_cs0	SPI3 Chip Select	IO	AF8/ V9/ D11/ A12/ AC9/ D17
spi3_cs1	SPI3 Chip Select	IO	B11/ AC3/ E14
spi3_cs2	SPI3 Chip Select	IO	F11
spi3_cs3	SPI3 Chip Select	IO	A10
Serial Peripheral Interface 4			
spi4_sclk(1)	SPI4 Clock	IO	N7/ G1/ AA3/ V7/ AC8
spi4_d1	SPI4 Data. Can be configured as either MISO or MOSI.	IO	R4/ G6/ AB9/ U7/ AD6
spi4_d0	SPI4 Data. Can be configured as either MISO or MOSI.	IO	N9/ F2/ AB3/ V6/ AB8

Table 4-10. SPI Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
spi4_cs0	SPI4 Chip Select	IO	P9/ F3/ AA4/ U6/ AB5
spi4_cs1	SPI4 Chip Select	IO	P4/ Y1
spi4_cs2	SPI4 Chip Select	IO	R3/ W9
spi4_cs3	SPI4 Chip Select	IO	T2/ V9

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

4.3.10 QSPI

NOTE

For more information, see the Serial Communication Interface / Quad Serial Peripheral Interface section of the Device TRM.

Table 4-11. QSPI Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
qspi1_sclk	QSPI1 Serial Clock	IO	R2
qspi1_rtclk	QSPI1 Return Clock Input.Must be connected from QSPI1_SCLK on PCB. Refer to PCB Guidelines for QSPI1	I	R3
qspi1_d0	QSPI1 Data[0]. This pin is output data for all commands/writes and for dual read and quad read modes it becomes input data pin during read phase.	IO	U1
qspi1_d1	QSPI1 Data[1]. Input read data in all modes.	I	P3
qspi1_d2	QSPI1 Data[2]. This pin is used only in quad read mode as input data pin during read phase	I	U2
qspi1_d3	QSPI1 Data[3]. This pin is used only in quad read mode as input data pin during read phase	I	T2
qspi1_cs0	QSPI1 Chip Select[0]. This pin is Used for QSPI1 boot modes.	O	P2
qspi1_cs1	QSPI1 Chip Select[1]	O	P1
qspi1_cs2	QSPI1 Chip Select[2]	O	T7
qspi1_cs3	QSPI1 Chip Select[3]	O	P6

4.3.11 McASP

NOTE

For more information, see the Serial Communication Interface / Multichannel Audio Serial Port (McASP) section of the Device TRM.

Table 4-12. McASP Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Multichannel Audio Serial Port 1			
mcasp1_axr0	McASP1 Transmit/Receive Data	IO	G12
mcasp1_axr1	McASP1 Transmit/Receive Data	IO	F12
mcasp1_axr2	McASP1 Transmit/Receive Data	IO	G13
mcasp1_axr3	McASP1 Transmit/Receive Data	IO	J11
mcasp1_axr4	McASP1 Transmit/Receive Data	IO	D18/ E12
mcasp1_axr5	McASP1 Transmit/Receive Data	IO	E17 / F13
mcasp1_axr6	McASP1 Transmit/Receive Data	IO	B26 / C12
mcasp1_axr7	McASP1 Transmit/Receive Data	IO	C23 / D12

Table 4-12. McASP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mcasp1_axr8	McASP1 Transmit/Receive Data	IO	E21 / B12
mcasp1_axr9	McASP1 Transmit/Receive Data	IO	F20/ A11
mcasp1_axr10	McASP1 Transmit/Receive Data	IO	F21 / B13
mcasp1_axr11	McASP1 Transmit/Receive Data	IO	A12
mcasp1_axr12	McASP1 Transmit/Receive Data	IO	E14
mcasp1_axr13	McASP1 Transmit/Receive Data	IO	A13
mcasp1_axr14	McASP1 Transmit/Receive Data	IO	G14
mcasp1_axr15	McASP1 Transmit/Receive Data	IO	F14
mcasp1_fsx	McASP1 Transmit Frame Sync	IO	D14
mcasp1_aclkr	McASP1 Receive Bit Clock	IO	B14
mcasp1_fsr	McASP1 Receive Frame Sync	IO	J14
mcasp1_ahclkx	McASP1 Transmit High-Frequency Master Clock	O	D18
mcasp1_aclkx	McASP1 Transmit Bit Clock	IO	C14
Multichannel Audio Serial Port 2			
mcasp2_axr0	McASP2 Transmit/Receive Data	IO	B15
mcasp2_axr1	McASP2 Transmit/Receive Data	IO	A15
mcasp2_axr2	McASP2 Transmit/Receive Data	IO	C15
mcasp2_axr3	McASP2 Transmit/Receive Data	IO	A16
mcasp2_axr4	McASP2 Transmit/Receive Data	IO	D15
mcasp2_axr5	McASP2 Transmit/Receive Data	IO	B16
mcasp2_axr6	McASP2 Transmit/Receive Data	IO	B17
mcasp2_axr7	McASP2 Transmit/Receive Data	IO	A17
mcasp2_axr8	McASP2 Transmit/Receive Data	IO	D18
mcasp2_axr9	McASP2 Transmit/Receive Data	IO	E17
mcasp2_axr10	McASP2 Transmit/Receive Data	IO	B26
mcasp2_axr11	McASP2 Transmit/Receive Data	IO	C23
mcasp2_axr12	McASP2 Transmit/Receive Data	IO	B18
mcasp2_axr13	McASP2 Transmit/Receive Data	IO	F15
mcasp2_axr14	McASP2 Transmit/Receive Data	IO	B19
mcasp2_axr15	McASP2 Transmit/Receive Data	IO	C17
mcasp2_fsx	McASP2 Transmit Frame Sync	IO	A18
mcasp2_aclkr(1)	McASP2 Receive Bit Clock	IO	E15
mcasp2_fsr	McASP2 Receive Frame Sync	IO	A20
mcasp2_ahclkx	McASP2 Transmit High-Frequency Master Clock	O	E17
mcasp2_aclkx(1)	McASP2 Transmit Bit Clock	IO	A19
Multichannel Audio Serial Port 3			
mcasp3_axr0	McASP3 Transmit/Receive Data	IO	B19
mcasp3_axr1	McASP3 Transmit/Receive Data	IO	C17
mcasp3_axr2	McASP3 Transmit/Receive Data	IO	C15
mcasp3_axr3	McASP3 Transmit/Receive Data	IO	A16
mcasp3_fsx	McASP3 Transmit Frame Sync	IO	F15
mcasp3_ahclkx	McASP3 Transmit High-Frequency Master Clock	O	B26
mcasp3_aclkx(1)	McASP3 Transmit Bit Clock	IO	B18
mcasp3_aclkr(1)	McASP3 Receive Bit Clock	IO	B18
mcasp3_fsr	McASP3 Receive Frame Sync	IO	F15
Multichannel Audio Serial Port 4			
mcasp4_axr0	McASP4 Transmit/Receive Data	IO	G16

Table 4-12. McASP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mcasp4_axr1	McASP4 Transmit/Receive Data	IO	D17
mcasp4_axr2	McASP4 Transmit/Receive Data	IO	E12
mcasp4_axr3	McASP4 Transmit/Receive Data	IO	F13
mcasp4_fsx	McASP4 Transmit Frame Sync	IO	A21
mcasp4_ahclkx	McASP4 Transmit High-Frequency Master Clock	O	C23
mcasp4_aclkx(1)	McASP4 Transmit Bit Clock	IO	C18
mcasp4_aclkr(1)	McASP4 Receive Bit Clock	IO	C18
mcasp4_fsr	McASP4 Receive Frame Sync	IO	A21
Multichannel Audio Serial Port 5			
mcasp5_axr0	McASP5 Transmit/Receive Data	IO	AB3
mcasp5_axr1	McASP5 Transmit/Receive Data	IO	AA4
mcasp5_axr2	McASP5 Transmit/Receive Data	IO	C12
mcasp5_axr3	McASP5 Transmit/Receive Data	IO	D12
mcasp5_fsx	McASP5 Transmit Frame Sync	IO	AB9
mcasp5_ahclkx	McASP5 Transmit High-Frequency Master Clock	O	D18
mcasp5_aclkx(1)	McASP5 Transmit Bit Clock	IO	AA3
mcasp5_aclkr(1)	McASP5 Receive Bit Clock	IO	AA3
mcasp5_fsr	McASP5 Receive Frame Sync	IO	AB9
Multichannel Audio Serial Port 6			
mcasp6_axr0	McASP6 Transmit/Receive Data	IO	B12
mcasp6_axr1	McASP6 Transmit/Receive Data	IO	A11
mcasp6_axr2	McASP6 Transmit/Receive Data	IO	G13
mcasp6_axr3	McASP6 Transmit/Receive Data	IO	J11
mcasp6_ahclkx	McASP6 Transmit High-Frequency Master Clock	O	E17
mcasp6_aclkx(1)	McASP6 Transmit Bit Clock	IO	B13
mcasp6_fsx	McASP6 Transmit Frame Sync	IO	A12
mcasp6_aclkr(1)	McASP6 Receive Bit Clock	IO	B13
mcasp6_fsr	McASP6 Receive Frame Sync	IO	A12
Multichannel Audio Serial Port 7			
mcasp7_axr0	McASP7 Transmit/Receive Data	IO	E14
mcasp7_axr1	McASP7 Transmit/Receive Data	IO	A13
mcasp7_axr2	McASP7 Transmit/Receive Data	IO	B14
mcasp7_axr3	McASP7 Transmit/Receive Data	IO	J14
mcasp7_ahclkx	McASP7 Transmit High-Frequency Master Clock	O	B26
mcasp7_aclkx(1)	McASP7 Transmit Bit Clock	IO	G14
mcasp7_fsx	McASP7 Transmit Frame Sync	IO	F14
mcasp7_aclkr(1)	McASP7 Receive Bit Clock	IO	G14
mcasp7_fsr	McASP7 Receive Frame Sync	IO	F14
Multichannel Audio Serial Port 8			
mcasp8_axr0	McASP8 Transmit/Receive Data	IO	D15
mcasp8_axr1	McASP8 Transmit/Receive Data	IO	B16
mcasp8_axr2	McASP8 Transmit/Receive Data	IO	E15
mcasp8_axr3	McASP8 Transmit/Receive Data	IO	A20
mcasp8_ahclkx	McASP8 Transmit High-Frequency Master Clock	O	C23
mcasp8_aclkx(1)	McASP8 Transmit Bit Clock	IO	B17
mcasp8_fsx	McASP8 Transmit Frame Sync	IO	A17
mcasp8_aclkr(1)	McASP8 Receive Bit Clock	IO	B17

Table 4-12. McASP Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mcasp8_fsr	McASP8 Receive Frame Sync	IO	A17

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

4.3.12 USB

NOTE

For more information, see Serial Communication Interface / SuperSpeed USB DRD Subsystem section of the Device TRM.

Table 4-13. Universal Serial Bus Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Universal Serial Bus 1			
usb1_dp	USB1 USB2.0 differential signal pair (positive)	IODS	AD12
usb1_dm	USB1 USB2.0 differential signal pair (negative)	IODS	AC12
usb1_drvvbus	USB1 Drive VBUS signal	O	AB10
usb_rxn0	USB1 USB3.0 receiver negative lane	IDS	AF12
usb_rxp0	USB1 USB3.0 receiver positive lane	IDS	AE12
usb_txn0	USB1 USB3.0 transmitter negative lane	ODS	AC11
usb_txp0	USB1 USB3.0 transmitter positive lane	ODS	AD11
Universal Serial Bus 2			
usb2_dp	USB2 USB2.0 differential signal pair (positive)	IODS	AE11
usb2_dm	USB2 USB2.0 differential signal pair (negative)	IODS	AF11
usb2_drvvbus	USB2 Drive VBUS signal	O	AC10
Universal Serial Bus 3			
usb3_ulpi_d0	USB3 - ULPI 8-bit data bus	IO	AC3 / AE1
usb3_ulpi_d1	USB3 - ULPI 8-bit data bus	IO	AC9 / AE5
usb3_ulpi_d2	USB3 - ULPI 8-bit data bus	IO	AC6 / AE3
usb3_ulpi_d3	USB3 - ULPI 8-bit data bus	IO	AC7 / AF1
usb3_ulpi_d4	USB3 - ULPI 8-bit data bus	IO	AC4 / AF4
usb3_ulpi_d5	USB3 - ULPI 8-bit data bus	IO	AD4 / AF3
usb3_ulpi_d6	USB3 - ULPI 8-bit data bus	IO	AB4 / AF6
usb3_ulpi_d7	USB3 - ULPI 8-bit data bus	IO	AC5 / AF2
usb3_ulpi_nxt	USB3 - ULPI next	I	AC8 / AE2
usb3_ulpi_dir	USB3 - ULPI bus direction	I	AD6 / AE6
usb3_ulpi_stp	USB3 - ULPI stop	O	AB8 / AD2
usb3_ulpi_clk	USB3 - ULPI functional clock	I	AB5 / AD3
Universal Serial Bus 4			
usb4_ulpi_d0	USB4 - ULPI 8-bit data bus	IO	V6
usb4_ulpi_d1	USB4 - ULPI 8-bit data bus	IO	U6
usb4_ulpi_d2	USB4 - ULPI 8-bit data bus	IO	U5
usb4_ulpi_d3	USB4 - ULPI 8-bit data bus	IO	V5
usb4_ulpi_d4	USB4 - ULPI 8-bit data bus	IO	V4
usb4_ulpi_d5	USB4 - ULPI 8-bit data bus	IO	V3
usb4_ulpi_d6	USB4 - ULPI 8-bit data bus	IO	Y2
usb4_ulpi_d7	USB4 - ULPI 8-bit data bus	IO	W2
usb4_ulpi_nxt	USB4 - ULPI next	I	U7

Table 4-13. Universal Serial Bus Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
usb4_ulpi_dir	USB4 - ULPI bus direction	I	V7
usb4_ulpi_stp	USB4 - ULPI stop	O	V9
usb4_ulpi_clk	USB4 - ULPI functional clock	I	W9

4.3.13 SATA

NOTE

For more information, see the Serial Communication Interfaces / SATA section of the Device TRM.

Table 4-14. SATA Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
sata1_rxn0	SATA differential negative receiver lane 0	IDS	AH9
sata1_rxp0	SATA differential positive receiver lane 0	IDS	AG9
sata1_txn0	SATA differential negative transmitter lane 0	ODS	AG10
sata1_txp0	SATA differential positive transmitter lane 0	ODS	AH10
sata1_led	SATA channel activity indicator	O	A22 / G19

4.3.14 PCIe

NOTE

For more information, see the Serial Communication Interfaces / PCIe section of the Device TRM.

Table 4-15. PCIe Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
pcie_rxn0	PCIe1_PHY_RX Receive Data Lane 0 (negative) - mapped to PCIe_SS1 only.	IDS	AG13
pcie_rxp0	PCIe1_PHY_RX Receive Data Lane 0 (positive) - mapped to PCIe_SS1 only.	IDS	AH13
pcie_txn0	PCIe1_PHY_TX Transmit Data Lane 0 (negative) - mapped to PCIe_SS1 only.	ODS	AG14
pcie_txp0	PCIe1_PHY_TX Transmit Data Lane 0 (positive) - mapped to PCIe_SS1 only.	ODS	AH14
pcie_rxn1	PCIe2_PHY_RX Receive Data Lane 1 (negative) - mapped to either PCIe_SS1 (dual-lane mode) or PCIe_SS2 (single-lane mode)	IDS	AG11
pcie_rxp1	PCIe2_PHY_RX Receive Data Lane 1 (positive) - mapped to either PCIe_SS1 (dual-lane mode) or PCIe_SS2 (single-lane mode)	IDS	AH11
pcie_txn1	PCIe2_PHY_TX Transmit Data Lane 1 (negative) - mapped to either PCIe_SS1 (dual-lane mode) or PCIe_SS2 (single-lane mode)	ODS	AG12
pcie_txp1	PCIe2_PHY_TX Transmit Data Lane 1 (positive) - mapped to either PCIe_SS1 (dual-lane mode) or PCIe_SS2 (single-lane mode)	ODS	AH12
ljcb_clkp	PCIe1_PHY shared Reference Clock Input / Output Differential Pair (positive)	IODS	AG15
ljcb_clkn	PCIe1_PHY shared Reference Clock Input / Output Differential Pair (negative)	IODS	AH15

4.3.15 DCAN and MCAN

NOTE

For more information, see the Serial Communication Interface / DCAN and MCAN section of the Device TRM.

Table 4-16. DCAN Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
DCAN 1			
dcan1_tx	DCAN1 transmit data pin	IO	G20
dcan1_rx	DCAN1 receive data pin	IO	G19/ AD17
DCAN 2			
dcan2_tx	DCAN2 transmit data pin	IO	E21/ B21
dcan2_rx	DCAN2 receive data pin	IO	F20/ AC17/ B20
MCAN			
mcan_tx	MCAN transmit data pin	IO	E21 / G20
mcan_rx	MCAN receive data pin	IO	F20 / G19

4.3.16 GMAC_SW

CAUTION

The I/O timings provided in Section 5.10, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the Table 5-100, Table 5-103, Table 5-108, and Table 5-115.

NOTE

For more information, see the Serial Communication Interfaces / Ethernet Controller section of the Device TRM.

Table 4-17. GMAC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
RGMII0			
rgmii0_txc	RGMII0 Transmit Clock	O	W9
rgmii0_txctl	RGMII0 Transmit Enable	O	V9
rgmii0_txd3	RGMII0 Transmit Data	O	V7
rgmii0_txd2	RGMII0 Transmit Data	O	U7
rgmii0_txd1	RGMII0 Transmit Data	O	V6
rgmii0_txd0	RGMII0 Transmit Data	O	U6
rgmii0_rxc	RGMII0 Receive Clock	I	U5
rgmii0_rxctl	RGMII0 Receive Control	I	V5
rgmii0_rxd3	RGMII0 Receive Data	I	V4
rgmii0_rxd2	RGMII0 Receive Data	I	V3
rgmii0_rxd1	RGMII0 Receive Data	I	Y2
rgmii0_rxd0	RGMII0 Receive Data	I	W2
RGMII1			
rgmii1_rxc	RGMII1 Receive Clock	I	C5

Table 4-17. GMAC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
rgmii1_rxctl	RGMII1 Receive Control	I	A3
rgmii1_rxd0	RGMII1 Receive Data	I	A4
rgmii1_rxd1	RGMII1 Receive Data	I	B5
rgmii1_rxd2	RGMII1 Receive Data	I	B4
rgmii1_rxd3	RGMII1 Receive Data	I	B3
rgmii1_txc	RGMII1 Transmit Clock	O	D5
rgmii1_txctl	RGMII1 Transmit Enable	O	C2
rgmii1_txd0	RGMII1 Transmit Data	O	D6
rgmii1_txd1	RGMII1 Transmit Data	O	B2
rgmii1_txd2	RGMII1 Transmit Data	O	C4
rgmii1_txd3	RGMII1 Transmit Data	O	C3
MII0			
mii0_rxd1	MII0 Receive Data	I	V6
mii0_rxd2	MII0 Receive Data	I	V9
mii0_rxd3	MII0 Receive Data	I	W9
mii0_rxd0	MII0 Receive Data	I	U6
mii0_rxclk	MII0 Receive Clock	I	Y1
mii0_rxdv	MII0 Receive Data Valid	I	V2
mii0_txclk	MII0 Transmit Clock	I	U5
mii0_txd0	MII0 Transmit Data	O	W2
mii0_txd1	MII0 Transmit Data	O	Y2
mii0_txd2	MII0 Transmit Data	O	V4
mii0_txd3	MII0 Transmit Data	O	V5
mii0_txer	MII0 Transmit Error	I	U4
mii0_rxer	MII0 Receive Data Error	I	U7
mii0_col	MII0 Collision Detect (Sense)	I	V1
mii0_crs	MII0 Carrier Sense	I	V7
mii0_txen	MII0 Transmit Data Enable	O	V3
MII1			
mii1_col	MII1 Collision Detect (Sense)	I	B4
mii1_crs	MII1 Carrier Sense	I	B5
mii1_rxclk	MII1 Receive Clock	I	D5
mii1_rxd0	MII1 Receive Data	I	E6
mii1_rxd1	MII1 Receive Data	I	C1
mii1_rxd2	MII1 Receive Data	I	E4
mii1_rxd3	MII1 Receive Data	I	F5
mii1_rxdv	MII1 Receive Data Valid	I	C2
mii1_rxer	MII1 Receive Data Error	I	B3
mii1_txclk	MII1 Transmit Clock	I	C3
mii1_txd0	MII1 Transmit Data	O	C4
mii1_txd1	MII1 Transmit Data	O	B2
mii1_txd2	MII1 Transmit Data	O	D6
mii1_txd3	MII1 Transmit Data	O	C5
mii1_txen	MII1 Transmit Data Enable	O	A4
mii1_txer	MII1 Transmit Error	I	A3
RMII0			
rmii0_crs	RMII0 Carrier Sense	I	V7

Table 4-17. GMAC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
rmii0_rxd0	RMII0 Receive Data	I	U6
rmii0_rxd1	RMII0 Receive Data	I	V6
rmii0_rxer	RMII0 Receive Data Error	I	U7
rmii0_txd0	RMII0 Transmit Data	O	W2
rmii0_txd1	RMII0 Transmit Data	O	Y2
rmii0_txen	RMII0 Transmit Data Enable	O	V3
RMII1			
rmii1_crs	RMII1 Carrier Sense	I	V2
rmii1_rxd0	RMII1 Receive Data	I	V9
rmii1_rxd1	RMII1 Receive Data	I	W9
rmii1_rxer	RMII1 Receive Data Error	I	Y1
rmii1_txd0	RMII1 Transmit Data	O	V4
rmii1_txd1	RMII1 Transmit Data	O	V5
rmii1_txen	RMII1 Transmit Data Enable	O	U5
MDIO			
mdio_d	Management Data	IO	AB4/ B20/ F6/ U4
mdio_mclk	Management Data Serial Clock	O	AC5/ B21/ D3/ V1

4.3.17 eMMC/SD/SDIO

NOTE

For more information, see the HS MMC/SDIO section of the Device TRM.

Table 4-18. eMMC/SD/SDIO Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Multi Media Card 1			
mmc1_clk(1)	MMC1 clock	IO	W6
mmc1_cmd	MMC1 command	IO	Y6
mmc1_sdcd	MMC1 Card Detect	I	W7
mmc1_sdwp	MMC1 Write Protect	I	Y9
mmc1_dat0	MMC1 data bit 0	IO	AA6
mmc1_dat1	MMC1 data bit 1	IO	Y4
mmc1_dat2	MMC1 data bit 2	IO	AA5
mmc1_dat3	MMC1 data bit 3	IO	Y3
Multi Media Card 2			
mmc2_clk(1)	MMC2 clock	IO	J7
mmc2_cmd	MMC2 command	IO	H6
mmc2_sdcd	MMC2 Card Detect	I	G20
mmc2_sdwp	MMC2 Write Protect	I	G19
mmc2_dat0	MMC2 data bit 0	IO	J4
mmc2_dat1	MMC2 data bit 1	IO	J6
mmc2_dat2	MMC2 data bit 2	IO	H4
mmc2_dat3	MMC2 data bit 3	IO	H5
mmc2_dat4	MMC2 data bit 4	IO	K7
mmc2_dat5	MMC2 data bit 5	IO	M7
mmc2_dat6	MMC2 data bit 6	IO	J5

Table 4-18. eMMC/SD/SDIO Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
mmc2_dat7	MMC2 data bit 7	IO	K6
Multi Media Card 3			
mmc3_clk(1)	MMC3 clock	IO	AD4
mmc3_cmd	MMC3 command	IO	AC4
mmc3_sdcd	MMC3 Card Detect	I	B21
mmc3_sdwp	MMC3 Write Protect	I	B20
mmc3_dat0	MMC3 data bit 0	IO	AC7
mmc3_dat1	MMC3 data bit 1	IO	AC6
mmc3_dat2	MMC3 data bit 2	IO	AC9
mmc3_dat3	MMC3 data bit 3	IO	AC3
mmc3_dat4	MMC3 data bit 4	IO	AC8
mmc3_dat5	MMC3 data bit 5	IO	AD6
mmc3_dat6	MMC3 data bit 6	IO	AB8
mmc3_dat7	MMC3 data bit 7	IO	AB5
Multi Media Card 4			
mmc4_sdcd	MMC4 Card Detect	I	B27
mmc4_sdwp	MMC4 Write Protect	I	C26
mmc4_clk(1)	MMC4 clock	IO	E25
mmc4_cmd	MMC4 command	IO	C27
mmc4_dat0	MMC4 data bit 0	IO	D28
mmc4_dat1	MMC4 data bit 1	IO	D26
mmc4_dat2	MMC4 data bit 2	IO	D27
mmc4_dat3	MMC4 data bit 3	IO	C28

(1) By default, this clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. mmc1_clk and mmc2_clk have an optional software programmable setting to use an 'internal loopback clock' instead of the default 'pad loopback clock'. If the 'pad loopback clock' is used, series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

4.3.18 GPIO

NOTE

For more information, see the General-Purpose Interface section of the Device TRM.

Table 4-19. GPIOs Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
GPIO 1			
gpio1_0	General-Purpose Input	I	AD17
gpio1_1	General-Purpose Input	I	AC17
gpio1_2	General-Purpose Input	I	AB16
gpio1_3	General-Purpose Input	I	AC16
gpio1_4	General-Purpose Input/Output	IO	D15
gpio1_5	General-Purpose Input/Output	IO	A17
gpio1_6	General-Purpose Input/Output	IO	M6
gpio1_7	General-Purpose Input/Output	IO	M2
gpio1_8	General-Purpose Input/Output	IO	L5
gpio1_9	General-Purpose Input/Output	IO	M1
gpio1_10	General-Purpose Input/Output	IO	L6

Table 4-19. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio1_11	General-Purpose Input/Output	IO	L4
gpio1_12	General-Purpose Input/Output	IO	L3
gpio1_13	General-Purpose Input/Output	IO	L2
gpio1_14	General-Purpose Input/Output	IO	G20
gpio1_15	General-Purpose Input/Output	IO	G19
gpio1_16	General-Purpose Input/Output	IO	D27
gpio1_17	General-Purpose Input/Output	IO	C28
gpio1_18	General-Purpose Input/Output	IO	H1
gpio1_19	General-Purpose Input/Output	IO	J3
gpio1_20	General-Purpose Input/Output	IO	H2
gpio1_21	General-Purpose Input/Output	IO	H3
gpio1_22	General-Purpose Input/Output	IO	AC8
gpio1_23	General-Purpose Input/Output	IO	AD6
gpio1_24	General-Purpose Input/Output	IO	AB8
gpio1_25	General-Purpose Input/Output	IO	AB5
gpio1_26	General-Purpose Input/Output	IO	P6
gpio1_27	General-Purpose Input/Output	IO	R9
gpio1_28	General-Purpose Input/Output	IO	R5
gpio1_29	General-Purpose Input/Output	IO	P5
gpio1_30	General-Purpose Input/Output	IO	N7
gpio1_31	General-Purpose Input/Output	IO	R4
GPIO 2			
gpio2_0	General-Purpose Input/Output	IO	N9
gpio2_1	General-Purpose Input/Output	IO	P9
gpio2_2	General-Purpose Input/Output	IO	P4
gpio2_3	General-Purpose Input/Output	IO	R3
gpio2_4	General-Purpose Input/Output	IO	T2
gpio2_5	General-Purpose Input/Output	IO	U2
gpio2_6	General-Purpose Input/Output	IO	U1
gpio2_7	General-Purpose Input/Output	IO	P3
gpio2_8	General-Purpose Input/Output	IO	R2
gpio2_9	General-Purpose Input/Output	IO	K7
gpio2_10	General-Purpose Input/Output	IO	M7
gpio2_11	General-Purpose Input/Output	IO	J5
gpio2_12	General-Purpose Input/Output	IO	K6
gpio2_13	General-Purpose Input/Output	IO	J7
gpio2_14	General-Purpose Input/Output	IO	J4
gpio2_15	General-Purpose Input/Output	IO	J6
gpio2_16	General-Purpose Input/Output	IO	H4
gpio2_17	General-Purpose Input/Output	IO	H5
gpio2_18	General-Purpose Input/Output	IO	H6
gpio2_19	General-Purpose Input/Output	IO	T1
gpio2_20	General-Purpose Input/Output	IO	P2
gpio2_21	General-Purpose Input/Output	IO	P1
gpio2_22	General-Purpose Input/Output	IO	P7
gpio2_23	General-Purpose Input/Output	IO	N1
gpio2_24	General-Purpose Input/Output	IO	M5

Table 4-19. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio2_25	General-Purpose Input/Output	IO	M3
gpio2_26	General-Purpose Input/Output	IO	N6
gpio2_27	General-Purpose Input/Output	IO	M4
gpio2_28	General-Purpose Input/Output	IO	N2
gpio2_29	General-Purpose Input/Output	IO	B17
gpio2_30	General-Purpose Input/Output	IO	AG8
gpio2_31	General-Purpose Input/Output	IO	AH7
GPIO 3			
gpio3_0	General-Purpose Input/Output	IO	AD9
gpio3_1	General-Purpose Input/Output	IO	AF9
gpio3_2	General-Purpose Input/Output	IO	AE9
gpio3_3	General-Purpose Input/Output	IO	AF8
gpio3_4	General-Purpose Input/Output	IO	AE8
gpio3_5	General-Purpose Input/Output	IO	AD8
gpio3_6	General-Purpose Input/Output	IO	AG7
gpio3_7	General-Purpose Input/Output	IO	AH6
gpio3_8	General-Purpose Input/Output	IO	AH3
gpio3_9	General-Purpose Input/Output	IO	AH5
gpio3_10	General-Purpose Input/Output	IO	AG6
gpio3_11	General-Purpose Input/Output	IO	AH4
gpio3_12	General-Purpose Input/Output	IO	AG4
gpio3_13	General-Purpose Input/Output	IO	AG2
gpio3_14	General-Purpose Input/Output	IO	AG3
gpio3_15	General-Purpose Input/Output	IO	AG5
gpio3_16	General-Purpose Input/Output	IO	AF2
gpio3_17	General-Purpose Input/Output	IO	AF6
gpio3_18	General-Purpose Input/Output	IO	AF3
gpio3_19	General-Purpose Input/Output	IO	AF4
gpio3_20	General-Purpose Input/Output	IO	AF1
gpio3_21	General-Purpose Input/Output	IO	AE3
gpio3_22	General-Purpose Input/Output	IO	AE5
gpio3_23	General-Purpose Input/Output	IO	AE1
gpio3_24	General-Purpose Input/Output	IO	AE2
gpio3_25	General-Purpose Input/Output	IO	AE6
gpio3_26	General-Purpose Input/Output	IO	AD2
gpio3_27	General-Purpose Input/Output	IO	AD3
gpio3_28	General-Purpose Input/Output	IO	E1
gpio3_29	General-Purpose Input/Output	IO	G2
gpio3_30	General-Purpose Input/Output	IO	H7
gpio3_31	General-Purpose Input/Output	IO	G1
GPIO 4			
gpio4_0	General-Purpose Input/Output	IO	G6
gpio4_1	General-Purpose Input/Output	IO	F2
gpio4_2	General-Purpose Input/Output	IO	F3
gpio4_3	General-Purpose Input/Output	IO	D1
gpio4_4	General-Purpose Input/Output	IO	E2
gpio4_5	General-Purpose Input/Output	IO	D2

Table 4-19. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio4_6	General-Purpose Input/Output	IO	F4
gpio4_7	General-Purpose Input/Output	IO	C1
gpio4_8	General-Purpose Input/Output	IO	E4
gpio4_9	General-Purpose Input/Output	IO	F5
gpio4_10	General-Purpose Input/Output	IO	E6
gpio4_11	General-Purpose Input/Output	IO	D3
gpio4_12	General-Purpose Input/Output	IO	F6
gpio4_13	General-Purpose Input/Output	IO	D5
gpio4_14	General-Purpose Input/Output	IO	C2
gpio4_15	General-Purpose Input/Output	IO	C3
gpio4_16	General-Purpose Input/Output	IO	C4
gpio4_17	General-Purpose Input/Output	IO	A12
gpio4_18	General-Purpose Input/Output	IO	E14
gpio4_19	General-Purpose Input/Output	IO	D11
gpio4_20	General-Purpose Input/Output	IO	B10
gpio4_21	General-Purpose Input/Output	IO	B11
gpio4_22	General-Purpose Input/Output	IO	C11
gpio4_23	General-Purpose Input/Output	IO	E11
gpio4_24	General-Purpose Input/Output	IO	B2
gpio4_25	General-Purpose Input/Output	IO	D6
gpio4_26	General-Purpose Input/Output	IO	C5
gpio4_27	General-Purpose Input/Output	IO	A3
gpio4_28	General-Purpose Input/Output	IO	B3
gpio4_29	General-Purpose Input/Output	IO	B4
gpio4_30	General-Purpose Input/Output	IO	B5
gpio4_31	General-Purpose Input/Output	IO	A4
GPIO 5			
gpio5_0	General-Purpose Input/Output	IO	B14
gpio5_1	General-Purpose Input/Output	IO	J14
gpio5_2	General-Purpose Input/Output	IO	G12
gpio5_3	General-Purpose Input/Output	IO	F12
gpio5_4	General-Purpose Input/Output	IO	G13
gpio5_5	General-Purpose Input/Output	IO	J11
gpio5_6	General-Purpose Input/Output	IO	E12
gpio5_7	General-Purpose Input/Output	IO	F13
gpio5_8	General-Purpose Input/Output	IO	C12
gpio5_9	General-Purpose Input/Output	IO	D12
gpio5_10	General-Purpose Input/Output	IO	B12
gpio5_11	General-Purpose Input/Output	IO	A11
gpio5_12	General-Purpose Input/Output	IO	B13
gpio5_13	General-Purpose Input/Output	IO	B18
gpio5_14	General-Purpose Input/Output	IO	F15
gpio5_15	General-Purpose Input/Output	IO	V1
gpio5_16	General-Purpose Input/Output	IO	U4
gpio5_17	General-Purpose Input/Output	IO	U3
gpio5_18	General-Purpose Input/Output	IO	V2
gpio5_19	General-Purpose Input/Output	IO	Y1

Table 4-19. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio5_20	General-Purpose Input/Output	IO	W9
gpio5_21	General-Purpose Input/Output	IO	V9
gpio5_22	General-Purpose Input/Output	IO	V7
gpio5_23	General-Purpose Input/Output	IO	U7
gpio5_24	General-Purpose Input/Output	IO	V6
gpio5_25	General-Purpose Input/Output	IO	U6
gpio5_26	General-Purpose Input/Output	IO	U5
gpio5_27	General-Purpose Input/Output	IO	V5
gpio5_28	General-Purpose Input/Output	IO	V4
gpio5_29	General-Purpose Input/Output	IO	V3
gpio5_30	General-Purpose Input/Output	IO	Y2
gpio5_31	General-Purpose Input/Output	IO	W2
GPIO 6			
gpio6_4	General-Purpose Input/Output	IO	A13
gpio6_5	General-Purpose Input/Output	IO	G14
gpio6_6	General-Purpose Input/Output	IO	F14
gpio6_7	General-Purpose Input/Output	IO	B16
gpio6_8	General-Purpose Input/Output	IO	C15
gpio6_9	General-Purpose Input/Output	IO	A16
gpio6_10	General-Purpose Input/Output	IO	AC5
gpio6_11	General-Purpose Input/Output	IO	AB4
gpio6_12	General-Purpose Input/Output	IO	AB10
gpio6_13	General-Purpose Input/Output	IO	AC10
gpio6_14	General-Purpose Input/Output	IO	E21
gpio6_15	General-Purpose Input/Output	IO	F20
gpio6_16	General-Purpose Input/Output	IO	F21
gpio6_17	General-Purpose Input/Output	IO	D18
gpio6_18	General-Purpose Input/Output	IO	E17
gpio6_19	General-Purpose Input/Output	IO	B26
gpio6_20	General-Purpose Input/Output	IO	C23
gpio6_21	General-Purpose Input/Output	IO	W6
gpio6_22	General-Purpose Input/Output	IO	Y6
gpio6_23	General-Purpose Input/Output	IO	AA6
gpio6_24	General-Purpose Input/Output	IO	Y4
gpio6_25	General-Purpose Input/Output	IO	AA5
gpio6_26	General-Purpose Input/Output	IO	Y3
gpio6_27	General-Purpose Input/Output	IO	W7
gpio6_28	General-Purpose Input/Output	IO	Y9
gpio6_29	General-Purpose Input/Output	IO	AD4
gpio6_30	General-Purpose Input/Output	IO	AC4
gpio6_31	General-Purpose Input/Output	IO	AC7
GPIO 7			
gpio7_0	General-Purpose Input/Output	IO	AC6
gpio7_1	General-Purpose Input/Output	IO	AC9
gpio7_2	General-Purpose Input/Output	IO	AC3
gpio7_3	General-Purpose Input/Output	IO	R6
gpio7_4	General-Purpose Input/Output	IO	T9

Table 4-19. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio7_5	General-Purpose Input/Output	IO	T6
gpio7_6	General-Purpose Input/Output	IO	T7
gpio7_7	General-Purpose Input/Output	IO	A25
gpio7_8	General-Purpose Input/Output	IO	F16
gpio7_9	General-Purpose Input/Output	IO	B25
gpio7_10	General-Purpose Input/Output	IO	A24
gpio7_11	General-Purpose Input/Output	IO	A22
gpio7_12	General-Purpose Input/Output	IO	B21
gpio7_13	General-Purpose Input/Output	IO	B20
gpio7_14	General-Purpose Input/Output	IO	A26
gpio7_15	General-Purpose Input/Output	IO	B22
gpio7_16	General-Purpose Input/Output	IO	G17
gpio7_17	General-Purpose Input/Output	IO	B24
gpio7_18	General-Purpose Input/Output	IO	L1
gpio7_19	General-Purpose Input/Output	IO	K2
gpio7_22	General-Purpose Input/Output	IO	B27
gpio7_23	General-Purpose Input/Output	IO	C26
gpio7_24	General-Purpose Input/Output	IO	E25
gpio7_25	General-Purpose Input/Output	IO	C27
gpio7_26	General-Purpose Input/Output	IO	D28
gpio7_27	General-Purpose Input/Output	IO	D26
gpio7_28	General-Purpose Input/Output	IO	J1
gpio7_29	General-Purpose Input/Output	IO	J2
gpio7_30	General-Purpose Input/Output	IO	D14
gpio7_31	General-Purpose Input/Output	IO	C14
GPIO 8			
gpio8_0	General-Purpose Input/Output	IO	F11
gpio8_1	General-Purpose Input/Output	IO	G10
gpio8_2	General-Purpose Input/Output	IO	F10
gpio8_3	General-Purpose Input/Output	IO	G11
gpio8_4	General-Purpose Input/Output	IO	E9
gpio8_5	General-Purpose Input/Output	IO	F9
gpio8_6	General-Purpose Input/Output	IO	F8
gpio8_7	General-Purpose Input/Output	IO	E7
gpio8_8	General-Purpose Input/Output	IO	E8
gpio8_9	General-Purpose Input/Output	IO	D9
gpio8_10	General-Purpose Input/Output	IO	D7
gpio8_11	General-Purpose Input/Output	IO	D8
gpio8_12	General-Purpose Input/Output	IO	A5
gpio8_13	General-Purpose Input/Output	IO	C6
gpio8_14	General-Purpose Input/Output	IO	C8
gpio8_15	General-Purpose Input/Output	IO	C7
gpio8_16	General-Purpose Input/Output	IO	B7
gpio8_17	General-Purpose Input/Output	IO	B8
gpio8_18	General-Purpose Input/Output	IO	A7
gpio8_19	General-Purpose Input/Output	IO	A8
gpio8_20	General-Purpose Input/Output	IO	C9

Table 4-19. GPIOs Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
gpio8_21	General-Purpose Input/Output	IO	A9
gpio8_22	General-Purpose Input/Output	IO	B9
gpio8_23	General-Purpose Input/Output	IO	A10
gpio8_27	General-Purpose Input	I	D23
gpio8_28	General-Purpose Input/Output	IO	F19
gpio8_29	General-Purpose Input/Output	IO	E18
gpio8_30	General-Purpose Input/Output	IO	G21
gpio8_31	General-Purpose Input/Output	IO	D24

4.3.19 PWM

NOTE

For more information, see the Pulse-Width Modulation (PWM) SS section of the Device TRM.

Table 4-20. PWM Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
PWMSS1			
eQEP1A_in	EQEP1 Quadrature Input A	I	E1 / AD9
eQEP1B_in	EQEP1 Quadrature Input B	I	G2 / AF9
eQEP1_index	EQEP1 Index Input	IO	AE9 / H7
eQEP1_strobe	EQEP1 Strobe Input	IO	G1 / AF8
ehrpwm1A	EHRPWM1 Output A	O	AE8 / G6
ehrpwm1B	EHRPWM1 Output B	O	AD8 / F2
ehrpwm1_tripzone_input	EHRPWM1 Trip Zone Input	IO	AG7 / F3
eCAP1_in_PWM1_out	ECAP1 Capture Input / PWM Output	IO	AH6 / D1
ehrpwm1_synci	EHRPWM1 Sync Input	I	AH3 / E2
ehrpwm1_synco	EHRPWM1 Sync Output	O	AH5 / D2
PWMSS2			
eQEP2A_in	EQEP2 Quadrature Input A	I	AG6 / F4
eQEP2B_in	EQEP2 Quadrature Input B	I	AH4 / C1
eQEP2_index	EQEP2 Index Input	IO	AG4 / E4
eQEP2_strobe	EQEP2 Strobe Input	IO	AG2 / F5
ehrpwm2A	EHRPWM2 Output A	O	AC5 / E6
ehrpwm2B	EHRPWM2 Output B	O	AB4 / D3
ehrpwm2_tripzone_input	EHRPWM2 Trip Zone Input	IO	AD4 / F6
eCAP2_in_PWM2_out	ECAP2 Capture Input / PWM Output	IO	AC4 / D5
PWMSS3			
eQEP3A_in	EQEP3 Quadrature Input A	I	AC7 / C2
eQEP3B_in	EQEP3 Quadrature Input B	I	AC6 / C3
eQEP3_index	EQEP3 Index Input	IO	AC9 / C4
eQEP3_strobe	EQEP3 Strobe Input	IO	AC3 / B2
ehrpwm3A	EHRPWM3 Output A	O	AC8 / D6
ehrpwm3B	EHRPWM3 Output B	O	AD6 / C5
ehrpwm3_tripzone_input	EHRPWM3 Trip Zone Input	IO	AB8 / A3

Table 4-20. PWM Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
eCAP3_in_PWM3_out	ECAP3 Capture Input / PWM Output	IO	AB5 / B3

4.3.20 System and Miscellaneous

4.3.20.1 Sysboot Interface

NOTE
For more information, see the Initialization (ROM Code) section of the Device TRM.

Table 4-21. Sysboot Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
sysboot0	Boot Mode Configuration 0. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	M6
sysboot1	Boot Mode Configuration 1. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	M2
sysboot2	Boot Mode Configuration 2. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L5
sysboot3	Boot Mode Configuration 3. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	M1
sysboot4	Boot Mode Configuration 4. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L6
sysboot5	Boot Mode Configuration 5. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L4
sysboot6	Boot Mode Configuration 6. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L3
sysboot7	Boot Mode Configuration 7. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L2
sysboot8	Boot Mode Configuration 8. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	L1
sysboot9	Boot Mode Configuration 9. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	K2
sysboot10	Boot Mode Configuration 10. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	J1
sysboot11	Boot Mode Configuration 11. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	J2
sysboot12	Boot Mode Configuration 12. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H1
sysboot13	Boot Mode Configuration 13. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	J3
sysboot14	Boot Mode Configuration 14. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H2
sysboot15	Boot Mode Configuration 15. The value latched on this pin upon porz reset release will determine the boot mode configuration of the device.	I	H3

4.3.20.2 PRCM

NOTE
For more information, see PRCM chapter of the Device TRM.

Table 4-22. PRCM Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
clkout1	Device Clock output 1. Can be used externally for devices with non-critical timing requirements, or for debug, or as a reference clock on GPMC as described in Table 5-55, *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default* and Table 5-57, *GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate*.	O	F21/ P7

Table 4-22. PRCM Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
clkout2	Device Clock output 2. Can be used externally for devices with non-critical timing requirements, or for debug.	O	D18/ N1
clkout3	Device Clock output 3. Can be used externally for devices with non-critical timing requirements, or for debug.	O	C23
rstoutn	Reset out (Active low) output is asserted low whenever any global reset condition exists. After a brief delay, it will be set high upon removal of the internal global reset condition (i.e. porz, warm reset). It is only functional after its output buffer's reference voltage (vddshv3) is valid. If it is used as a reset for device peripheral components, then it should be AND gated with porz to avoid the possibility of reset signal glitches during a power up sequence.(2)	O	F23
resetn	Reset (active low) input's falling edge can trigger a device warm reset state from an external component. This signal should be high prior to or simultaneous with, porz rising. If the signal is not used in the system, resetn should be pulled high with an external pull-up resistor to vddshv3.	I	E23
porz	Power-on Reset (active low) input must be asserted low during a device power up sequence or cold reset state when all supplies are disabled. Typically, an external PMIC is the source and sets porz high after all supplies reach valid operating levels. Asserting porz low puts the entire device in a safe reset state.	I	F22
xref_clk0	External Reference Clock 0. For Audio and other Peripherals.	I	D18
xref_clk1	External Reference Clock 1. For Audio and other Peripherals.	I	E17
xref_clk2	External Reference Clock 2. For Audio and other Peripherals.	I	B26
xref_clk3	External Reference Clock 3. For Audio and other Peripherals.	I	C23
xi_osc0	System Oscillator OSC0 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC0 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used.	I	AE15
xo_osc0	System Oscillator OSC0 Crystal output	O	AD15
xi_osc1	Auxiliary Oscillator OSC1 Crystal input / LVCMOS clock input. Functions as the input connection to a crystal when the internal oscillator OSC1 is used. Functions as an LVCMOS-compatible input clock when an external oscillator is used.	I	AC15
xo_osc1	Auxiliary Oscillator OSC1 Crystal output	O	AC13
RMII_MHZ_50_CLK(1)	RMII Reference Clock (50 MHz). This pin is an input when external reference is used or output when internal reference is used.	IO	U3

(1) This clock signal is implemented as 'pad loopback' inside the device - the output signal is looped back through the input buffer to serve as the internal reference signal. Series termination is recommended (as close to device pin as possible) to improve signal integrity of the clock input. Any nonmonotonicity in voltage that occurs at the pad loopback clock pin between V_{IH} and V_{IL} must be less than V_{HYS}.

(2) Note that rstoutn is only valid after vddshv3 is valid. If the rstoutn signal will be used as a reset into other devices attached to the SoC, it must be AND'ed with porz. This will prevent glitches occurring during supply ramping being propagated.

4.3.20.3 RTC

NOTE

For more information, see the Real Time Clock (RTC) SS section of the Device TRM.

Table 4-23. RTC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
Wakeup0	RTC External Wakeup Input 0	I	AD17
Wakeup1	RTC External Wakeup Input 1	I	AC17
Wakeup2	RTC External Wakeup Input 2	I	AB16
Wakeup3	RTC External Wakeup Input 3	I	AC16
rtc_porz	RTC Power Domain Power-On Reset Input	I	AB17

Table 4-23. RTC Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
rtc_osc_xi_clkin32	RTC Oscillator Input. Crystal connection to internal RTC oscillator. Functions as an RTC clock input when an external oscillator is used.	I	AE14
rtc_osc_xo	RTC Oscillator Output	O	AD14
rtc_iso(1)	RTC domain isolation signal	I	AF14
on_off	RTC Power Enable output pin	O	Y11

(1) This signal must be kept "0" if device power supplies are not valid during RTC mode and "1" during normal operation. This can typically be achieved by connecting rtc_iso to the same signal driving porz (not rtc_porz) with appropriate voltage level translation if necessary.

4.3.20.4 SDMA

NOTE

For more information, see the DMA Controllers / System DMA section of the Device TRM.

Table 4-24. System DMA Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
dma_evt1	System DMA Event Input 1	I	P7/ P4
dma_evt2	System DMA Event Input 2	I	N1/ R3
dma_evt3	System DMA Event Input 3	I	N6
dma_evt4	System DMA Event Input 4	I	M4

4.3.20.5 INTC

NOTE

For more information, see the Interrupt Controllers section of the Device TRM.

Table 4-25. INTC Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
nmin_dsp	Non-maskable interrupt input, active-low. This pin can be optionally routed to the DSP NMI input or as generic input to the Arm cores. Note that by default this pin has an internal pulldown resistor enabled. This internal pulldown should be disabled or countered by a stronger external pullup resistor before routing to the DSP or Arm processors.	I	D21
sys_nirq2	External interrupt event to any device INTC	I	AB16
sys_nirq1	External interrupt event to any device INTC	I	AC16

4.3.20.6 Observability

NOTE

For more information, see the Control Module chapter of the Device TRM.

Table 4-26. Observability Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
obs0	Observation Output 0	O	F10
obs1	Observation Output 1	O	G11
obs2	Observation Output 2	O	E9
obs3	Observation Output 3	O	F9
obs4	Observation Output 4	O	F8

Table 4-26. Observability Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
obs5	Observation Output 5	O	D7
obs6	Observation Output 6	O	D8
obs7	Observation Output 7	O	A5
obs8	Observation Output 8	O	C6
obs9	Observation Output 9	O	C8
obs10	Observation Output 10	O	C7
obs11	Observation Output 11	O	A7
obs12	Observation Output 12	O	A8
obs13	Observation Output 13	O	C9
obs14	Observation Output 14	O	A9
obs15	Observation Output 15	O	B9
obs16	Observation Output 16	O	F10
obs17	Observation Output 17	O	G11
obs18	Observation Output 18	O	E9
obs19	Observation Output 19	O	F9
obs20	Observation Output 20	O	F8
obs21	Observation Output 21	O	D7
obs22	Observation Output 22	O	D8
obs23	Observation Output 23	O	A5
obs24	Observation Output 24	O	C6
obs25	Observation Output 25	O	C8
obs26	Observation Output 26	O	C7
obs27	Observation Output 27	O	A7
obs28	Observation Output 28	O	A8
obs29	Observation Output 29	O	C9
obs30	Observation Output 30	O	A9
obs31	Observation Output 31	O	B9
obs_dmarq1	DMA Request External Observation Output 1	O	G11
obs_dmarq2	DMA Request External Observation Output 2	O	D8
obs_irq1	IRQ External Observation Output 1	O	F10
obs_irq2	IRQ External Observation Output 2	O	D7

4.3.20.7 Power Supplies

NOTE

For more information, see Power, Reset, and Clock Management / PRCM Subsystem Environment / External Voltage Inputs section of the Device TRM.

Table 4-27. Power Supply Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vdd	Core voltage domain supply	PWR	H13/ H14/ J17/ J18/ L7/ L8/ N10/ N13/ P11/ P12/ P13/ R11/ R16/ R19/ T13/ T16/ T19/ U8/ U9/ U13/ U16/ V8/ V16
vpp[(2)]	eFuse power supply	PWR	K14

Table 4-27. Power Supply Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vss	Ground	GND	A1/ A2/ A6/ A14/ A23/ A28/ B1/ D13/ D19/ E13/ E19/ F1/ F7/ G7/ G8/ G9/ H12/ J12/ J15/ J28/ K1/ K4/ K5/ K15/ K24/ K25/ L13/ L14/ M19/ N14/ N15/ N19/ N24/ N25/ P28/ R1/ R12/ R13/ R15/ R21/ T10/ T11/ T12/ T14/ T15/ T17/ T18/ T21/ U15/ U17/ U20/ U21/ V15/ V17/ W1/ W15/ W24/ W25/ W28/ AA8/ AA9/ AA10/ AA14/ AA15/ AA20/ AB14/ AB20/ AD1/ AD24/ AG1/ AH1/ AH2/ AH8/ AH20/ AH28 / AB11/ AA11 / AE19 / AD19 / AE13 / AD13 / AE10 / AD10 / U14
vdd_dspeve	DSP-EVE voltage domain supply	PWR	J13/ K10/ K11/ K12/ K13/ L10/ L11/ L12/ M10/ M11/ M12/ M13
vdd_iva	IVA voltage domain supply	PWR	U18/ U19/ V18/ V19
vdd_gpu	GPU voltage domain supply	PWR	U11/ U12/ V10/ V11/ V14/ W10/ W11/ W13
vdd_mpu	MPU voltage domain supply	PWR	K17/ K18/ L15/ L16/ L17/ L18/ L19/ M15/ M16/ M17/ M18/ N17/ N18/ P17/ P18/ R18
vdd_rtc	RTC voltage domain supply	PWR	AB15
vdda_usb1	DPLL_USB and HS USB1 1.8 V analog power supply	PWR	AA13
vdda_usb2	HS USB2 1.8 V analog power supply	PWR	AB12
vdda33v_usb1	HS USB1 3.3 V analog power supply. If USB1 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb1_dm/usb1_dp pins are left unconnected - The USB1 PHY is kept powered down	PWR	AA12
vdda33v_usb2	HS USB2 3.3 V analog power supply. If USB2 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb2_dm/usb2_dp pins are left unconnected - The USB2 PHY is kept powered down	PWR	Y12
vdda_abe_per	DPLL_ABE, DPLL_PER, and PER HSDIVIDER analog power supply	PWR	M14
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply	PWR	P16
vdda_debug	DPLL_DEBUG analog power supply	PWR	N11
vdda_dsp_eve	DPLL_DSP and DPLL_EVE analog power supply	PWR	N12
vdda_gmac_core	DPLL_CORE and CORE HSDIVIDER analog power supply	PWR	P15
vdda_gpu	DPLL_GPU analog power supply	PWR	R14
vdda_hdmi	PLL_HDMI and HDMI analog power supply	PWR	Y17
vdda_iva	DPLL_IVA analog power supply	PWR	R17
vdda_pcie	DPLL_PCIe_REF and PCIe analog power supply	PWR	W14
vdda_pcie0	PCIe ch0 RX/TX analog power supply	PWR	AA17
vdda_pcie1	PCIe ch1 RX/TX analog power supply	PWR	AA16
vdda_sata	DPLL_SATA and SATA RX/TX analog power supply	PWR	V13
vdda_usb3	DPLL_USB_OTG_SS and USB3.0 RX/TX analog power supply	PWR	W12
vdda_video	DPLL_VIDEO1 and DPLL_VIDEO2 analog power supply	PWR	P14

Table 4-27. Power Supply Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
vdds_mlbp	MLBP IO power supply	PWR	AA7/ Y7
vdda_mpu	DPLL_MPU analog power supply	PWR	N16
vdda_osc	HFOSC analog power supply	PWR	AE16/ AD16
vssa_osc0	OSC0 analog ground	GND	AF15
vssa_osc1	OSC1 analog ground	GND	AC14
vdda_rtc	RTC bias and RTC LFOSC analog power supply	PWR	AB13
vdds18v	1.8 V power supply	PWR	W17/ W18/ V21/ V22/ T8/ R8/ P8/ N8/ M8/ M9/ H17/ G18
vdds18v_ddr1	DDR1 bias power supply	PWR	AA18/ AA19/ Y21/ W21
vdds18v_ddr2	DDR2 bias power supply	PWR	P20/ P21/ N21/ J21/ J22
vdds_ddr2	DDR2 power supply (1.8 V for DDR2 mode/ 1.5 V for DDR3 mode / 1.35 V for DDR3L mode)	PWR	T24/ T25/ M20/ M21/ L20/ L21/ J27/ H20/ H21/ H22/ G22/ G23/ E24
vdds_ddr1	DDR1 power supply (1.8 V for DDR2 mode/ 1.5 V for DDR3 mode / 1.35 V for DDR3L mode)	PWR	AH27/ AG20/ AG28/ AD26/ AC22/ AB21/ AB22/ AB24/ AB25/ AA21/ AA22/ W16/ W27
vddshv5	Dual Voltage (1.8 V or 3.3 V) power supply for the RTC Power Group pins	PWR	V12
vddshv1	Dual Voltage (1.8 V or 3.3 V) power supply for the VIN2 Power Group pins	PWR	H8/ H9/ G4/ G5/ E3/ E5
vddshv10	Dual Voltage (1.8 V or 3.3 V) power supply for the GPMC Power Group pins	PWR	T4/ T5/ R7/ R10/ P10/ N4/ N5
vddshv11	Dual Voltage (1.8 V or 3.3 V) power supply for the MMC2 Power Group pins	PWR	K8/ J8
vddshv2	Dual Voltage (1.8 V or 3.3 V) power supply for the VOUT Power Group pins	PWR	H10/ H11/ E10/ D10/ B6
vddshv3	Dual Voltage (1.8 V or 3.3 V) power supply for the GENERAL Power Group pins	PWR	H15/ H16/ H18/ H19/ G15/ E16/ E22/ D16/ D22/ B23
vddshv4	Dual Voltage (1.8 V or 3.3 V) power supply for the MMC4 Power Group pins	PWR	C24
vddshv6	Dual Voltage (1.8 V or 3.3 V) power supply for the VIN1 Power Group pins	PWR	AF5/ AE7/ AD5/ AD7
vddshv7	Dual Voltage (1.8 V or 3.3 V) power supply for the WIFI Power Group pins	PWR	AB6/ AB7
vddshv8	Dual Voltage (1.8 V or 3.3 V) power supply for the MMC1 Power Group pins	PWR	Y8/ W8
vddshv9	Dual Voltage (1.8 V or 3.3 V) power supply for the RGMII Power Group pins	PWR	W4/ W5/ U10
cap_vddram_dspeve2(1)	External capacitor connection for the DSP-EVE SRAM array ldo2 output	CAP	J9
cap_vddram_dspeve1(1)	External capacitor connection for the DSP-EVE SRAM array ldo1 output	CAP	J10
cap_vbbldo_mpu(1)	External capacitor connection for the MPU vbb ldo output	CAP	J16
cap_vddram_core2(1)	External capacitor connection for the Core SRAM array ldo2 output	CAP	J19
cap_vbbldo_dspeve(1)	External capacitor connection for the DSP-EVE vbb ldo output	CAP	K9
cap_vddram_mpu1(1)	External capacitor connection for the MPU SRAM array ldo1 output	CAP	K16
cap_vddram_mpu2(1)	External capacitor connection for the MPU SRAM array ldo2 output	CAP	K19
cap_vddram_core1(1)	External capacitor connection for the Core SRAM array ldo1 output	CAP	L9

Table 4-27. Power Supply Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
cap_vddram_core4[(1)]	External capacitor connection for the Core SRAM array ldo4 output	CAP	P19
cap_vbbldo_iva[(1)]	External capacitor connection for the IVA vbb ldo output	CAP	R20
cap_vddram_iva[(1)]	External capacitor connection for the IVA SRAM array ldo output	CAP	T20
cap_vddram_gpu[(1)]	External capacitor connection for the GPU SRAM array ldo output	CAP	Y13
cap_vbbldo_gpu[(1)]	External capacitor connection for the GPU vbb ldo output	CAP	Y14
cap_vddram_core3[(1)]	External capacitor connection for the Core SRAM array ldo3 output	CAP	Y15
cap_vddram_core5[(1)]	External capacitor connection for the Core SRAM array ldo5 output	CAP	Y16

(1) This pin must always must always be connected via a 1 µF capacitor to vss.

(2) This signal is valid only for High-Security devices. For more details, see Section 5.8, *VPP Specification for One-Time Programmable (OTP) eFUSEs*. For General-purpose devices do not connect any signal, test point, or board trace to this signal.

4.3.21 Test Interfaces

CAUTION

The I/O timings provided in Section 5.10, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the Table 5-168.

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the Device TRM.

Table 4-28. Debug Signal Descriptions

SIGNAL NAME	DESCRIPTION	TYPE	BALL
tms	JTAG test port mode select. An external pullup resistor should be used on this ball.	IO	F18
tdi	JTAG test data	I	D23
tdo	JTAG test port data	O	F19
tclk	JTAG test clock	I	E20
trstn	JTAG test reset	I	D20
rtck	JTAG return clock	O	E18
emu0	Emulator pin 0	IO	G21
emu1	Emulator pin 1	IO	D24
emu2	Emulator pin 2	O	F10
emu3	Emulator pin 3	O	D7
emu4	Emulator pin 4	O	A7
emu5	Emulator pin 5	O	E1/ G11
emu6	Emulator pin 6	O	G2/ E9
emu7	Emulator pin 7	O	H7/ F9
emu8	Emulator pin 8	O	G1/ F8
emu9	Emulator pin 9	O	G6/ E7
emu10	Emulator pin 10	O	F2/ D8
emu11	Emulator pin 11	O	F3/ A5
emu12	Emulator pin 12	O	D1/ C6
emu13	Emulator pin 13	O	E2/ C8
emu14	Emulator pin 14	O	D2/ C7

Table 4-28. Debug Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	TYPE	BALL
emu15	Emulator pin 15	O	F4/ A8
emu16	Emulator pin 16	O	C1/ C9
emu17	Emulator pin 17	O	E4/ A9
emu18	Emulator pin 18	O	F5/ B9
emu19	Emulator pin 19	O	E6/ A10

4.4 Pin Multiplexing

Table 4-29 describes the device pin multiplexing (no characteristics are provided in this table).

NOTE

Table 4-29, *Pin Multiplexing* doesn't take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 4.3, *Signal Descriptions*.

NOTE

For more information, see the Control Module / Control Module Functional Description / PAD Functional Multiplexing and Configuration section of the Device TRM.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (Hi-Z mode is not an input signal).

NOTE

In some cases Table 4-29 may present more than one signal name per muxmode for the same ball. First signal in the list is the dominant function as selected via CTRL_CORE_PAD_* register. All other signals are virtual functions that present alternate multiplexing options. This virtual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT register. For more information on how to use this options, please refer to the Device TRM, Chapter Control Module, Section Pad Configuration Registers.

NOTE

When a pad is set into a pin multiplexing mode which is not defined, that pad’s behavior is undefined. This should be avoided.

CAUTION

The I/O timings provided in Section 5.10, *Timing Requirements and Switching Characteristics* are valid only if signals within a single IOSET are used. The IOSETs are defined in the corresponding tables.

Table 4-29. Pin Multiplexing

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
		P25	ddr2_a6												
		Y23	ddr1_d26												
		Y19	ddr1_d21												
		AE15	xi_osc0												
		AH24	ddr1_nck												
		AG15	ljcb_clkp												
		AF24	ddr1_d4												
		U25	ddr2_wen												
		F27	ddr2_d5												
		V25	ddr1_ecc_d6												
		M27	ddr2_dqsn3												
		G26	ddr2_d12												
		AG19	hdmi1_data2x												
		AF21	ddr1_a4												
		E27	ddr2_d6												
		F24	ddr2_d3												
		H26	ddr2_d11												
		W23	ddr1_ecc_d3												
		Y27	ddr1_dqsn3												
		AC24	ddr1_d14												
		J24	ddr2_d15												
		R26	ddr2_a1												
		G27	ddr2_dqsn0												
		AF28	ddr1_d11												
		AA23	ddr1_d24												
		AD18	ddr1_a15												
		H23	ddr2_d8												
		AH16	hdmi1_clocky												
		AC20	ddr1_a2												
		AA24	ddr1_d27												
		W19	ddr1_ecc_d2												
		L24	ddr2_d20												
		AG11	pcie_rxn1												
		AG21	ddr1_rst												
		AE28	ddr1_dqsn1												
		AC11	usb_txn0												
		L22	ddr2_d16												

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
		U28	ddr2_casn												
		K22	ddr2_d22												
		AG25	ddr1_dqsn0												
		W20	ddr1_d17												
		AF14	rtc_iso												
		AA27	ddr1_dqm3												
		AF25	ddr1_d0												
		AF23	ddr1_d6												
		AG18	hdmi1_data1x												
		AG10	sata1_txn0												
		AF20	ddr1_rasn												
		V26	ddr1_dqm_ecc												
		V20	ddr1_d16												
		G25	ddr2_d1												
		AH13	pcie_rxp0												
		AC18	ddr1_casn												
		AG9	sata1_rxp0												
		AH23	ddr1_csn0												
		AE11	usb2_dp												
		R25	ddr2_a0												
		Y24	ddr1_d28												
		AH15	ljcb_clkn												
		AD20	ddr1_a0												
		AA25	ddr1_d30												
		L23	ddr2_d19												
		AD14	rtc_osc_xo												
		J25	ddr2_d13												
		AC25	ddr1_d13												
		AB23	ddr1_dqm1												
		U22	ddr2_a15												
		T22	ddr2_a13												
		AH19	hdmi1_data2y												
		M26	ddr2_d31												
		AB27	ddr1_d22												
		AG14	pcie_txn0												
		Y28	ddr1_dqs3												
		J20	ddr2_d23												

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
		AB19	ddr1_a3												
		AH10	sata1_txp0												
		G28	ddr2_dqs0												
		AG24	ddr1_ck												
		AE24	ddr1_d5												
		AC15	xi_osc1												
		AC21	ddr1_a12												
		K28	ddr2_dqsn2												
		AF12	usb_rxn0												
		L28	ddr2_d27												
		M24	ddr2_d29												
		AH9	sata1_rxn0												
		AC26	ddr1_dqm2												
		AA28	ddr1_d31												
		H28	ddr2_dqsn1												
		AD23	ddr1_dqm0												
		E26	ddr2_d0												
		AE27	ddr1_dqs1												
		AF27	ddr1_d9												
		V24	ddr1_ecc_d5												
		K23	ddr2_dqm2												
		K20	ddr2_d17												
		T28	ddr2_ck												
		H24	ddr2_d10												
		AG27	ddr1_d10												
		R23	ddr2_odt0												
		U27	ddr2_ba1												
		AF22	ddr1_a8												
		U23	ddr2_ba0												
		AH21	ddr1_wen												
		AE21	ddr1_a7												
		AC12	usb1_dm												
		AH12	pcie_txp1												
		Y20	ddr1_d23												
		AC27	ddr1_d20												
		AE23	ddr1_d7												
		T27	ddr2_nck												
		AG22	ddr1_cke												
		AD27	ddr1_dqs2												

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
		AH14	pcie_txp0												
		AH26	ddr1_d3												
		AD21	ddr1_a10												
		N28	ddr2_a12												
		Y25	ddr1_ecc_d4												
		AE17	ddr1_a14												
		AH18	hdmi1_data1y												
		AH22	ddr1_a5												
		J26	ddr2_d14												
		W22	ddr1_ecc_d0												
		V23	ddr1_ecc_d1												
		AE12	usb_rxp0												
		AE14	rtc_osc_xi_clkin32												
		AH11	pcie_rxp1												
		AG23	ddr1_a6												
		H27	ddr2_dqs1												
		AB18	ddr1_ba2												
		AG17	hdmi1_data0x												
		AF26	ddr1_d1												
		H25	ddr2_d9												
		M25	ddr2_d30												
		AD11	usb_txp0												
		L27	ddr2_d24												
		V27	ddr1_dqs_ecc												
		AF17	ddr1_ba0												
		AE26	ddr1_d12												
		G24	ddr2_dqm1												
		K27	ddr2_dqs2												
		AC19	ddr1_a1												
		AG13	pcie_rxn0												
		L26	ddr2_d25												
		AB28	ddr1_d18												
		N23	ddr2_a10												
		M22	ddr2_dqm3												
		U26	ddr2_ba2												
		Y26	ddr1_ecc_d7												

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
		P24	ddr2_csn0												
		R22	ddr2_a14												
		AD22	ddr1_a11												
		N20	ddr2_a7												
		M23	ddr2_d28												
		AD28	ddr1_dqsn2												
		U24	ddr2_cke												
		P22	ddr2_a5												
0x17D4	CTRL_CORE_PAD_DCAN1_RX	G19	dcan1_rx mcan_rx		uart8_txd	mmc2_sdwp	sata1_led		hdmi1_cec					gpio1_15	Driver off
		AE18	ddr1_ba1												
		F26	ddr2_d4												
		AE20	ddr1_odt0												
		N22	ddr2_vref0												
		E28	ddr2_d7												
		F25	ddr2_d2												
		AF11	usb2_dm												
		R24	ddr2_rst												
		AD15	xo_osc0												
		R27	ddr2_a3												
		AE22	ddr1_a9												
		Y18	ddr1_vref0												
0x17D0	CTRL_CORE_PAD_DCAN1_TX	G20	dcan1_tx mcan_tx		uart8_rxd	mmc2_sdcd			hdmi1_hpd					gpio1_14	Driver off
		AC13	xo_osc1												
		F28	ddr2_dqm0												
		J23	ddr2_d21												
		P26	ddr2_a11												
		M28	ddr2_dqs3												
		AD12	usb1_dp												
		Y22	ddr1_d25												
		T23	ddr2_rasn												
		AH17	hdmi1_data0y												
		N27	ddr2_a9												
		P23	ddr2_a4												
		AG26	ddr1_d2												
		AH25	ddr1_dqs0												
		AG12	pcie_txn1												
		AF18	ddr1_a13												

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
		K21	ddr2_d18												
		AC28	ddr1_d19												
		V28	ddr1_dqsn_ecc												
		P27	ddr2_a8												
		AC23	ddr1_d8												
		F22	porz												
		L25	ddr2_d26												
		AG16	hdmi1_clockx												
		R28	ddr2_a2												
		AA26	ddr1_d29												
		AD25	ddr1_d15												
0x1400	CTRL_CORE_PAD_GPMC_AD0	M6	gpmc_ad0		vin3a_d0	vout3_d0								gpio1_6	sysboot0
0x1404	CTRL_CORE_PAD_GPMC_AD1	M2	gpmc_ad1		vin3a_d1	vout3_d1								gpio1_7	sysboot1
0x1408	CTRL_CORE_PAD_GPMC_AD2	L5	gpmc_ad2		vin3a_d2	vout3_d2								gpio1_8	sysboot2
0x140C	CTRL_CORE_PAD_GPMC_AD3	M1	gpmc_ad3		vin3a_d3	vout3_d3								gpio1_9	sysboot3
0x1410	CTRL_CORE_PAD_GPMC_AD4	L6	gpmc_ad4		vin3a_d4	vout3_d4								gpio1_10	sysboot4
0x1414	CTRL_CORE_PAD_GPMC_AD5	L4	gpmc_ad5		vin3a_d5	vout3_d5								gpio1_11	sysboot5
0x1418	CTRL_CORE_PAD_GPMC_AD6	L3	gpmc_ad6		vin3a_d6	vout3_d6								gpio1_12	sysboot6
0x141C	CTRL_CORE_PAD_GPMC_AD7	L2	gpmc_ad7		vin3a_d7	vout3_d7								gpio1_13	sysboot7
0x1420	CTRL_CORE_PAD_GPMC_AD8	L1	gpmc_ad8		vin3a_d8	vout3_d8								gpio7_18	sysboot8
0x1424	CTRL_CORE_PAD_GPMC_AD9	K2	gpmc_ad9		vin3a_d9	vout3_d9								gpio7_19	sysboot9
0x1428	CTRL_CORE_PAD_GPMC_AD10	J1	gpmc_ad10		vin3a_d10	vout3_d10								gpio7_28	sysboot10
0x142C	CTRL_CORE_PAD_GPMC_AD11	J2	gpmc_ad11		vin3a_d11	vout3_d11								gpio7_29	sysboot11
0x1430	CTRL_CORE_PAD_GPMC_AD12	H1	gpmc_ad12		vin3a_d12	vout3_d12								gpio1_18	sysboot12
0x1434	CTRL_CORE_PAD_GPMC_AD13	J3	gpmc_ad13		vin3a_d13	vout3_d13								gpio1_19	sysboot13
0x1438	CTRL_CORE_PAD_GPMC_AD14	H2	gpmc_ad14		vin3a_d14	vout3_d14								gpio1_20	sysboot14
0x143C	CTRL_CORE_PAD_GPMC_AD15	H3	gpmc_ad15		vin3a_d15	vout3_d15								gpio1_21	sysboot15
0x1440	CTRL_CORE_PAD_GPMC_A0	R6	gpmc_a0		vin3a_d16	vout3_d16	vin4a_d0		vin4b_d0	i2c4_scl	uart5_rxd			gpio7_3 gpmc_a26 gpmc_a16	Driver off
0x1444	CTRL_CORE_PAD_GPMC_A1	T9	gpmc_a1		vin3a_d17	vout3_d17	vin4a_d1		vin4b_d1	i2c4_sda	uart5_txd			gpio7_4	Driver off
0x1448	CTRL_CORE_PAD_GPMC_A2	T6	gpmc_a2		vin3a_d18	vout3_d18	vin4a_d2		vin4b_d2	uart7_rxd	uart5_ctsn			gpio7_5	Driver off
0x144C	CTRL_CORE_PAD_GPMC_A3	T7	gpmc_a3	qspi1_cs2	vin3a_d19	vout3_d19	vin4a_d3		vin4b_d3	uart7_txd	uart5_rtsn			gpio7_6	Driver off
0x1450	CTRL_CORE_PAD_GPMC_A4	P6	gpmc_a4	qspi1_cs3	vin3a_d20	vout3_d20	vin4a_d4		vin4b_d4	i2c5_scl	uart6_rxd			gpio1_26	Driver off
0x1454	CTRL_CORE_PAD_GPMC_A5	R9	gpmc_a5		vin3a_d21	vout3_d21	vin4a_d5		vin4b_d5	i2c5_sda	uart6_txd			gpio1_27	Driver off
0x1458	CTRL_CORE_PAD_GPMC_A6	R5	gpmc_a6		vin3a_d22	vout3_d22	vin4a_d6		vin4b_d6	uart8_rxd	uart6_ctsn			gpio1_28	Driver off
0x145C	CTRL_CORE_PAD_GPMC_A7	P5	gpmc_a7		vin3a_d23	vout3_d23	vin4a_d7		vin4b_d7	uart8_txd	uart6_rtsn			gpio1_29	Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x1460	CTRL_CORE_PAD_GPMC_A8	N7	gpmc_a8		vin3a_hsync0	vout3_hsync			vin4b_hsync1	timer12	spi4_sclk			gpio1_30	Driver off
0x1464	CTRL_CORE_PAD_GPMC_A9	R4	gpmc_a9		vin3a_vsync0	vout3_vsync			vin4b_vsync1	timer11	spi4_d1			gpio1_31	Driver off
0x1468	CTRL_CORE_PAD_GPMC_A10	N9	gpmc_a10		vin3a_de0	vout3_de			vin4b_clk1	timer10	spi4_d0			gpio2_0	Driver off
0x146C	CTRL_CORE_PAD_GPMC_A11	P9	gpmc_a11		vin3a_fld0	vout3_fld	vin4a_fld0		vin4b_de1	timer9	spi4_cs0			gpio2_1	Driver off
0x1470	CTRL_CORE_PAD_GPMC_A12	P4	gpmc_a12				vin4a_clk0	gpmc_a0	vin4b_fld1	timer8	spi4_cs1	dma_evt1		gpio2_2	Driver off
0x1474	CTRL_CORE_PAD_GPMC_A13	R3	gpmc_a13	qspi1_rtclk			vin4a_hsync0			timer7	spi4_cs2	dma_evt2		gpio2_3	Driver off
0x1478	CTRL_CORE_PAD_GPMC_A14	T2	gpmc_a14	qspi1_d3			vin4a_vsync0			timer6	spi4_cs3			gpio2_4	Driver off
0x147C	CTRL_CORE_PAD_GPMC_A15	U2	gpmc_a15	qspi1_d2			vin4a_d8			timer5				gpio2_5	Driver off
0x1480	CTRL_CORE_PAD_GPMC_A16	U1	gpmc_a16	qspi1_d0			vin4a_d9							gpio2_6	Driver off
0x1484	CTRL_CORE_PAD_GPMC_A17	P3	gpmc_a17	qspi1_d1			vin4a_d10							gpio2_7	Driver off
0x1488	CTRL_CORE_PAD_GPMC_A18	R2	gpmc_a18	qspi1_sclk			vin4a_d11							gpio2_8	Driver off
0x148C	CTRL_CORE_PAD_GPMC_A19	K7	gpmc_a19	mmc2_dat4	gpmc_a13		vin4a_d12		vin3b_d0					gpio2_9	Driver off
0x1490	CTRL_CORE_PAD_GPMC_A20	M7	gpmc_a20	mmc2_dat5	gpmc_a14		vin4a_d13		vin3b_d1					gpio2_10	Driver off
0x1494	CTRL_CORE_PAD_GPMC_A21	J5	gpmc_a21	mmc2_dat6	gpmc_a15		vin4a_d14		vin3b_d2					gpio2_11	Driver off
0x1498	CTRL_CORE_PAD_GPMC_A22	K6	gpmc_a22	mmc2_dat7	gpmc_a16		vin4a_d15		vin3b_d3					gpio2_12	Driver off
0x149C	CTRL_CORE_PAD_GPMC_A23	J7	gpmc_a23	mmc2_clk	gpmc_a17		vin4a_fld0		vin3b_d4					gpio2_13	Driver off
0x14A0	CTRL_CORE_PAD_GPMC_A24	J4	gpmc_a24	mmc2_dat0	gpmc_a18				vin3b_d5					gpio2_14	Driver off
0x14A4	CTRL_CORE_PAD_GPMC_A25	J6	gpmc_a25	mmc2_dat1	gpmc_a19				vin3b_d6					gpio2_15	Driver off
0x14A8	CTRL_CORE_PAD_GPMC_A26	H4	gpmc_a26	mmc2_dat2	gpmc_a20				vin3b_d7					gpio2_16	Driver off
0x14AC	CTRL_CORE_PAD_GPMC_A27	H5	gpmc_a27	mmc2_dat3	gpmc_a21				vin3b_hsync1					gpio2_17	Driver off
0x14B0	CTRL_CORE_PAD_GPMC_CS1	H6	gpmc_cs1	mmc2_cmd	gpmc_a22		vin4a_de0		vin3b_vsync1					gpio2_18	Driver off
0x14B4	CTRL_CORE_PAD_GPMC_CS0	T1	gpmc_cs0											gpio2_19	Driver off
0x14B8	CTRL_CORE_PAD_GPMC_CS2	P2	gpmc_cs2	qspi1_cs0										gpio2_20 gpmc_a23 gpmc_a13	Driver off
0x14BC	CTRL_CORE_PAD_GPMC_CS3	P1	gpmc_cs3	qspi1_cs1	vin3a_clk0	vout3_clk		gpmc_a1						gpio2_21 gpmc_a24 gpmc_a14	Driver off
0x14C0	CTRL_CORE_PAD_GPMC_CLK	P7	gpmc_clk	gpmc_cs7	clkout1	gpmc_wait1	vin4a_hsync0	vin4a_de0	vin3b_clk1	timer4	i2c3_scl	dma_evt1		gpio2_22 gpmc_a20	Driver off
0x14C4	CTRL_CORE_PAD_GPMC_ADVN_ALE	N1	gpmc_advn_ale	gpmc_cs6	clkout2	gpmc_wait1	vin4a_vsync0	gpmc_a2	gpmc_a23	timer3	i2c3_sda	dma_evt2		gpio2_23 gpmc_a19	Driver off
0x14C8	CTRL_CORE_PAD_GPMC_OEN_REN	M5	gpmc_oen_ren											gpio2_24	Driver off
0x14CC	CTRL_CORE_PAD_GPMC_WEN	M3	gpmc_wen											gpio2_25	Driver off
0x14D0	CTRL_CORE_PAD_GPMC_BEN0	N6	gpmc_ben0	gpmc_cs4		vin1b_hsync1			vin3b_de1	timer2		dma_evt3		gpio2_26 gpmc_a21	Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x14D4	CTRL_CORE_PAD_GPMC_BEN1	M4	gpmc_ben1	gpmc_cs5		vin1b_de1	vin3b_clk1	gpmc_a3	vin3b_fld1	timer1		dma_evt4		gpio2_27 gpmc_a22	Driver off
0x14D8	CTRL_CORE_PAD_GPMC_WAIT0	N2	gpmc_wait0											gpio2_28 gpmc_a25 gpmc_a15	Driver off
0x14DC	CTRL_CORE_PAD_VIN1A_CLK0	AG8	vin1a_clk0			vout3_d16	vout3_fld							gpio2_30	Driver off
0x14E0	CTRL_CORE_PAD_VIN1B_CLK1	AH7	vin1b_clk1						vin3a_clk0					gpio2_31	Driver off
0x14E4	CTRL_CORE_PAD_VIN1A_DE0	AD9	vin1a_de0	vin1b_hsync1		vout3_d17	vout3_de	uart7_rxd		timer16	spi3_sclk		eQEP1A_in	gpio3_0	Driver off
0x14E8	CTRL_CORE_PAD_VIN1A_FLD0	AF9	vin1a_fld0	vin1b_vsync1			vout3_clk	uart7_txd		timer15	spi3_d1		eQEP1B_in	gpio3_1	Driver off
0x14EC	CTRL_CORE_PAD_VIN1A_HSYNC0	AE9	vin1a_hsync0	vin1b_fld1			vout3_hsync	uart7_ctsn		timer14	spi3_d0		eQEP1_index	gpio3_2	Driver off
0x14F0	CTRL_CORE_PAD_VIN1A_VSYNC0	AF8	vin1a_vsync0	vin1b_de1			vout3_vsync	uart7_rtsn		timer13	spi3_cs0		eQEP1_strobe	gpio3_3	Driver off
0x14F4	CTRL_CORE_PAD_VIN1A_D0	AE8	vin1a_d0			vout3_d7	vout3_d23	uart8_rxd					ehrpwm1A	gpio3_4	Driver off
0x14F8	CTRL_CORE_PAD_VIN1A_D1	AD8	vin1a_d1			vout3_d6	vout3_d22	uart8_txd					ehrpwm1B	gpio3_5	Driver off
0x14FC	CTRL_CORE_PAD_VIN1A_D2	AG7	vin1a_d2			vout3_d5	vout3_d21	uart8_ctsn					ehrpwm1_tripzone_input	gpio3_6	Driver off
0x1500	CTRL_CORE_PAD_VIN1A_D3	AH6	vin1a_d3			vout3_d4	vout3_d20	uart8_rtsn					eCAP1_in_PWM1_out	gpio3_7	Driver off
0x1504	CTRL_CORE_PAD_VIN1A_D4	AH3	vin1a_d4			vout3_d3	vout3_d19						ehrpwm1_synci	gpio3_8	Driver off
0x1508	CTRL_CORE_PAD_VIN1A_D5	AH5	vin1a_d5			vout3_d2	vout3_d18						ehrpwm1_synco	gpio3_9	Driver off
0x150C	CTRL_CORE_PAD_VIN1A_D6	AG6	vin1a_d6			vout3_d1	vout3_d17						eQEP2A_in	gpio3_10	Driver off
0x1510	CTRL_CORE_PAD_VIN1A_D7	AH4	vin1a_d7			vout3_d0	vout3_d16						eQEP2B_in	gpio3_11	Driver off
0x1514	CTRL_CORE_PAD_VIN1A_D8	AG4	vin1a_d8	vin1b_d7			vout3_d15						eQEP2_index	gpio3_12	Driver off
0x1518	CTRL_CORE_PAD_VIN1A_D9	AG2	vin1a_d9	vin1b_d6			vout3_d14						eQEP2_strobe	gpio3_13	Driver off
0x151C	CTRL_CORE_PAD_VIN1A_D10	AG3	vin1a_d10	vin1b_d5			vout3_d13							gpio3_14	Driver off
0x1520	CTRL_CORE_PAD_VIN1A_D11	AG5	vin1a_d11	vin1b_d4			vout3_d12	gpmc_a23						gpio3_15	Driver off
0x1524	CTRL_CORE_PAD_VIN1A_D12	AF2	vin1a_d12	vin1b_d3	usb3_ulpi_d7		vout3_d11	gpmc_a24						gpio3_16	Driver off
0x1528	CTRL_CORE_PAD_VIN1A_D13	AF6	vin1a_d13	vin1b_d2	usb3_ulpi_d6		vout3_d10	gpmc_a25						gpio3_17	Driver off
0x152C	CTRL_CORE_PAD_VIN1A_D14	AF3	vin1a_d14	vin1b_d1	usb3_ulpi_d5		vout3_d9	gpmc_a26						gpio3_18	Driver off
0x1530	CTRL_CORE_PAD_VIN1A_D15	AF4	vin1a_d15	vin1b_d0	usb3_ulpi_d4		vout3_d8	gpmc_a27						gpio3_19	Driver off
0x1534	CTRL_CORE_PAD_VIN1A_D16	AF1	vin1a_d16	vin1b_d7	usb3_ulpi_d3		vout3_d7		vin3a_d0					gpio3_20	Driver off
0x1538	CTRL_CORE_PAD_VIN1A_D17	AE3	vin1a_d17	vin1b_d6	usb3_ulpi_d2		vout3_d6		vin3a_d1					gpio3_21	Driver off
0x153C	CTRL_CORE_PAD_VIN1A_D18	AE5	vin1a_d18	vin1b_d5	usb3_ulpi_d1		vout3_d5		vin3a_d2					gpio3_22	Driver off
0x1540	CTRL_CORE_PAD_VIN1A_D19	AE1	vin1a_d19	vin1b_d4	usb3_ulpi_d0		vout3_d4		vin3a_d3					gpio3_23	Driver off
0x1544	CTRL_CORE_PAD_VIN1A_D20	AE2	vin1a_d20	vin1b_d3	usb3_ulpi_nxt		vout3_d3		vin3a_d4					gpio3_24	Driver off
0x1548	CTRL_CORE_PAD_VIN1A_D21	AE6	vin1a_d21	vin1b_d2	usb3_ulpi_dir		vout3_d2		vin3a_d5					gpio3_25	Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x154C	CTRL_CORE_PAD_VIN1A_D22	AD2	vin1a_d22	vin1b_d1	usb3_ulpi_stp		vout3_d1		vin3a_d6					gpio3_26	Driver off
0x1550	CTRL_CORE_PAD_VIN1A_D23	AD3	vin1a_d23	vin1b_d0	usb3_ulpi_clk		vout3_d0		vin3a_d7					gpio3_27	Driver off
0x1554	CTRL_CORE_PAD_VIN2A_CLK0	E1	vin2a_clk0				vout2_fld	emu5					eQEP1A_in	gpio3_28 gpmc_a27 gpmc_a17	Driver off
0x1558	CTRL_CORE_PAD_VIN2A_DE0	G2	vin2a_de0	vin2a_fld0	vin2b_fld1	vin2b_de1	vout2_de	emu6					eQEP1B_in	gpio3_29	Driver off
0x155C	CTRL_CORE_PAD_VIN2A_FLD0	H7	vin2a_fld0		vin2b_clk1		vout2_clk	emu7					eQEP1_index	gpio3_30 gpmc_a27 gpmc_a18	Driver off
0x1560	CTRL_CORE_PAD_VIN2A_HSYNC0	G1	vin2a_hsync0			vin2b_hsync1	vout2_hsync	emu8		uart9_rxd	spi4_sclk		eQEP1_strobe	gpio3_31 gpmc_a27	Driver off
0x1564	CTRL_CORE_PAD_VIN2A_VSYNC0	G6	vin2a_vsync0			vin2b_vsync1	vout2_vsync	emu9		uart9_txd	spi4_d1		ehrpwm1A	gpio4_0	Driver off
0x1568	CTRL_CORE_PAD_VIN2A_D0	F2	vin2a_d0				vout2_d23	emu10		uart9_ctsn	spi4_d0		ehrpwm1B	gpio4_1	Driver off
0x156C	CTRL_CORE_PAD_VIN2A_D1	F3	vin2a_d1				vout2_d22	emu11		uart9_rtsn	spi4_cs0		ehrpwm1_tripzone_input	gpio4_2	Driver off
0x1570	CTRL_CORE_PAD_VIN2A_D2	D1	vin2a_d2				vout2_d21	emu12			uart10_rxd		eCAP1_in_PWM1_out	gpio4_3	Driver off
0x1574	CTRL_CORE_PAD_VIN2A_D3	E2	vin2a_d3				vout2_d20	emu13			uart10_txd		ehrpwm1_synci	gpio4_4	Driver off
0x1578	CTRL_CORE_PAD_VIN2A_D4	D2	vin2a_d4				vout2_d19	emu14			uart10_ctsn		ehrpwm1_synco	gpio4_5	Driver off
0x157C	CTRL_CORE_PAD_VIN2A_D5	F4	vin2a_d5				vout2_d18	emu15			uart10_rtsn		eQEP2A_in	gpio4_6	Driver off
0x1580	CTRL_CORE_PAD_VIN2A_D6	C1	vin2a_d6				vout2_d17	emu16			mii1_rxd1		eQEP2B_in	gpio4_7	Driver off
0x1584	CTRL_CORE_PAD_VIN2A_D7	E4	vin2a_d7				vout2_d16	emu17			mii1_rxd2		eQEP2_index	gpio4_8	Driver off
0x1588	CTRL_CORE_PAD_VIN2A_D8	F5	vin2a_d8				vout2_d15	emu18			mii1_rxd3		eQEP2_strobe	gpio4_9 gpmc_a26	Driver off
0x158C	CTRL_CORE_PAD_VIN2A_D9	E6	vin2a_d9				vout2_d14	emu19			mii1_rxd0		ehrpwm2A	gpio4_10 gpmc_a25	Driver off
0x1590	CTRL_CORE_PAD_VIN2A_D10	D3	vin2a_d10			mdio_mclk	vout2_d13						ehrpwm2B	gpio4_11 gpmc_a24	Driver off
0x1594	CTRL_CORE_PAD_VIN2A_D11	F6	vin2a_d11			mdio_d	vout2_d12						ehrpwm2_tripzone_input	gpio4_12 gpmc_a23	Driver off
0x1598	CTRL_CORE_PAD_VIN2A_D12	D5	vin2a_d12			rgmii1_txc	vout2_d11				mii1_rxclk		eCAP2_in_PWM2_out	gpio4_13	Driver off
0x159C	CTRL_CORE_PAD_VIN2A_D13	C2	vin2a_d13			rgmii1_txctl	vout2_d10				mii1_rxdv		eQEP3A_in	gpio4_14	Driver off
0x15A0	CTRL_CORE_PAD_VIN2A_D14	C3	vin2a_d14			rgmii1_txd3	vout2_d9				mii1_txclk		eQEP3B_in	gpio4_15	Driver off
0x15A4	CTRL_CORE_PAD_VIN2A_D15	C4	vin2a_d15			rgmii1_txd2	vout2_d8				mii1_txd0		eQEP3_index	gpio4_16	Driver off
0x15A8	CTRL_CORE_PAD_VIN2A_D16	B2	vin2a_d16		vin2b_d7	rgmii1_txd1	vout2_d7		vin3a_d8		mii1_txd1		eQEP3_strobe	gpio4_24	Driver off
0x15AC	CTRL_CORE_PAD_VIN2A_D17	D6	vin2a_d17		vin2b_d6	rgmii1_txd0	vout2_d6		vin3a_d9		mii1_txd2		ehrpwm3A	gpio4_25	Driver off
0x15B0	CTRL_CORE_PAD_VIN2A_D18	C5	vin2a_d18		vin2b_d5	rgmii1_rxc	vout2_d5		vin3a_d10		mii1_txd3		ehrpwm3B	gpio4_26	Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x15B4	CTRL_CORE_PAD_VIN2A_D19	A3	vin2a_d19		vin2b_d4	rgmii1_rxctl	vout2_d4		vin3a_d11		mii1_txer		ehrpwm3_tripzone_input	gpio4_27	Driver off
0x15B8	CTRL_CORE_PAD_VIN2A_D20	B3	vin2a_d20		vin2b_d3	rgmii1_rxd3	vout2_d3	vin3a_de0	vin3a_d12		mii1_rxer		eCAP3_in_PWM3_out	gpio4_28	Driver off
0x15BC	CTRL_CORE_PAD_VIN2A_D21	B4	vin2a_d21		vin2b_d2	rgmii1_rxd2	vout2_d2	vin3a_fld0	vin3a_d13		mii1_col			gpio4_29	Driver off
0x15C0	CTRL_CORE_PAD_VIN2A_D22	B5	vin2a_d22		vin2b_d1	rgmii1_rxd1	vout2_d1	vin3a_hsync0	vin3a_d14		mii1_crs			gpio4_30	Driver off
0x15C4	CTRL_CORE_PAD_VIN2A_D23	A4	vin2a_d23		vin2b_d0	rgmii1_rxd0	vout2_d0	vin3a_vsync0	vin3a_d15		mii1_txen			gpio4_31	Driver off
0x15C8	CTRL_CORE_PAD_VOUT1_CLK	D11	vout1_clk			vin4a_fld0	vin3a_fld0				spi3_cs0			gpio4_19	Driver off
0x15CC	CTRL_CORE_PAD_VOUT1_DE	B10	vout1_de			vin4a_de0	vin3a_de0				spi3_d1			gpio4_20	Driver off
0x15D0	CTRL_CORE_PAD_VOUT1_FLD	B11	vout1_fld			vin4a_clk0	vin3a_clk0				spi3_cs1			gpio4_21	Driver off
0x15D4	CTRL_CORE_PAD_VOUT1_HSYNC	C11	vout1_hsync			vin4a_hsync0	vin3a_hsync0				spi3_d0			gpio4_22	Driver off
0x15D8	CTRL_CORE_PAD_VOUT1_VSYNC	E11	vout1_vsync			vin4a_vsync0	vin3a_vsync0				spi3_sclk			gpio4_23	Driver off
0x15DC	CTRL_CORE_PAD_VOUT1_D0	F11	vout1_d0		uart5_rxd	vin4a_d16	vin3a_d16				spi3_cs2			gpio8_0	Driver off
0x15E0	CTRL_CORE_PAD_VOUT1_D1	G10	vout1_d1		uart5_txd	vin4a_d17	vin3a_d17							gpio8_1	Driver off
0x15E4	CTRL_CORE_PAD_VOUT1_D2	F10	vout1_d2		emu2	vin4a_d18	vin3a_d18	obs0	obs16	obs_irq1				gpio8_2	Driver off
0x15E8	CTRL_CORE_PAD_VOUT1_D3	G11	vout1_d3		emu5	vin4a_d19	vin3a_d19	obs1	obs17	obs_dmarq1				gpio8_3	Driver off
0x15EC	CTRL_CORE_PAD_VOUT1_D4	E9	vout1_d4		emu6	vin4a_d20	vin3a_d20	obs2	obs18					gpio8_4	Driver off
0x15F0	CTRL_CORE_PAD_VOUT1_D5	F9	vout1_d5		emu7	vin4a_d21	vin3a_d21	obs3	obs19					gpio8_5	Driver off
0x15F4	CTRL_CORE_PAD_VOUT1_D6	F8	vout1_d6		emu8	vin4a_d22	vin3a_d22	obs4	obs20					gpio8_6	Driver off
0x15F8	CTRL_CORE_PAD_VOUT1_D7	E7	vout1_d7		emu9	vin4a_d23	vin3a_d23							gpio8_7	Driver off
0x15FC	CTRL_CORE_PAD_VOUT1_D8	E8	vout1_d8		uart6_rxd	vin4a_d8	vin3a_d8							gpio8_8	Driver off
0x1600	CTRL_CORE_PAD_VOUT1_D9	D9	vout1_d9		uart6_txd	vin4a_d9	vin3a_d9							gpio8_9	Driver off
0x1604	CTRL_CORE_PAD_VOUT1_D10	D7	vout1_d10		emu3	vin4a_d10	vin3a_d10	obs5	obs21	obs_irq2				gpio8_10	Driver off
0x1608	CTRL_CORE_PAD_VOUT1_D11	D8	vout1_d11		emu10	vin4a_d11	vin3a_d11	obs6	obs22	obs_dmarq2				gpio8_11	Driver off
0x160C	CTRL_CORE_PAD_VOUT1_D12	A5	vout1_d12		emu11	vin4a_d12	vin3a_d12	obs7	obs23					gpio8_12	Driver off
0x1610	CTRL_CORE_PAD_VOUT1_D13	C6	vout1_d13		emu12	vin4a_d13	vin3a_d13	obs8	obs24					gpio8_13	Driver off
0x1614	CTRL_CORE_PAD_VOUT1_D14	C8	vout1_d14		emu13	vin4a_d14	vin3a_d14	obs9	obs25					gpio8_14	Driver off
0x1618	CTRL_CORE_PAD_VOUT1_D15	C7	vout1_d15		emu14	vin4a_d15	vin3a_d15	obs10	obs26					gpio8_15	Driver off
0x161C	CTRL_CORE_PAD_VOUT1_D16	B7	vout1_d16		uart7_rxd	vin4a_d0	vin3a_d0							gpio8_16	Driver off
0x1620	CTRL_CORE_PAD_VOUT1_D17	B8	vout1_d17		uart7_txd	vin4a_d1	vin3a_d1							gpio8_17	Driver off
0x1624	CTRL_CORE_PAD_VOUT1_D18	A7	vout1_d18		emu4	vin4a_d2	vin3a_d2	obs11	obs27					gpio8_18	Driver off
0x1628	CTRL_CORE_PAD_VOUT1_D19	A8	vout1_d19		emu15	vin4a_d3	vin3a_d3	obs12	obs28					gpio8_19	Driver off
0x162C	CTRL_CORE_PAD_VOUT1_D20	C9	vout1_d20		emu16	vin4a_d4	vin3a_d4	obs13	obs29					gpio8_20	Driver off
0x1630	CTRL_CORE_PAD_VOUT1_D21	A9	vout1_d21		emu17	vin4a_d5	vin3a_d5	obs14	obs30					gpio8_21	Driver off
0x1634	CTRL_CORE_PAD_VOUT1_D22	B9	vout1_d22		emu18	vin4a_d6	vin3a_d6	obs15	obs31					gpio8_22	Driver off
0x1638	CTRL_CORE_PAD_VOUT1_D23	A10	vout1_d23		emu19	vin4a_d7	vin3a_d7				spi3_cs3			gpio8_23	Driver off
0x163C	CTRL_CORE_PAD_MDIO_MCLK	V1	mdio_mclk	uart3_rtsn		mii0_col	vin2a_clk0	vin4b_clk1						gpio5_15	Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x1640	CTRL_CORE_PAD_MDIO_D	U4	mdio_d	uart3_ctsn		mii0_txer	vin2a_d0	vin4b_d0						gpio5_16	Driver off
0x1644	CTRL_CORE_PAD_RMII_MHZ_50_CLK	U3	RMII_MHZ_50_CLK				vin2a_d11							gpio5_17	Driver off
0x1648	CTRL_CORE_PAD_UART3_RXD	V2	uart3_rxd		rmii1_crs	mii0_rxdv	vin2a_d1	vin4b_d1		spi3_sclk				gpio5_18	Driver off
0x164C	CTRL_CORE_PAD_UART3_TXD	Y1	uart3_txd		rmii1_rxer	mii0_rxclk	vin2a_d2	vin4b_d2		spi3_d1	spi4_cs1			gpio5_19	Driver off
0x1650	CTRL_CORE_PAD_RGMII0_TXC	W9	rgmii0_txc	uart3_ctsn	rmii1_rxd1	mii0_rxd3	vin2a_d3	vin4b_d3	usb4_ulpi_clk	spi3_d0	spi4_cs2			gpio5_20	Driver off
0x1654	CTRL_CORE_PAD_RGMII0_TXCTL	V9	rgmii0_txctl	uart3_rtsn	rmii1_rxd0	mii0_rxd2	vin2a_d4	vin4b_d4	usb4_ulpi_stp	spi3_cs0	spi4_cs3			gpio5_21	Driver off
0x1658	CTRL_CORE_PAD_RGMII0_TXD3	V7	rgmii0_txd3	rmii0_crs		mii0_crs	vin2a_de0	vin4b_de1	usb4_ulpi_dir	spi4_sclk	uart4_rxd			gpio5_22	Driver off
0x165C	CTRL_CORE_PAD_RGMII0_TXD2	U7	rgmii0_txd2	rmii0_rxer		mii0_rxer	vin2a_hsync0	vin4b_hsync1	usb4_ulpi_nxt	spi4_d1	uart4_txd			gpio5_23	Driver off
0x1660	CTRL_CORE_PAD_RGMII0_TXD1	V6	rgmii0_txd1	rmii0_rxd1		mii0_rxd1	vin2a_vsync0	vin4b_vsync1	usb4_ulpi_d0	spi4_d0	uart4_ctsn			gpio5_24	Driver off
0x1664	CTRL_CORE_PAD_RGMII0_TXD0	U6	rgmii0_txd0	rmii0_rxd0		mii0_rxd0	vin2a_d10		usb4_ulpi_d1	spi4_cs0	uart4_rtsn			gpio5_25	Driver off
0x1668	CTRL_CORE_PAD_RGMII0_RXC	U5	rgmii0_rxc		rmii1_txen	mii0_txclk	vin2a_d5	vin4b_d5	usb4_ulpi_d2					gpio5_26	Driver off
0x166C	CTRL_CORE_PAD_RGMII0_RXCTL	V5	rgmii0_rxctl		rmii1_txd1	mii0_txd3	vin2a_d6	vin4b_d6	usb4_ulpi_d3					gpio5_27	Driver off
0x1670	CTRL_CORE_PAD_RGMII0_RXD3	V4	rgmii0_rxd3		rmii1_txd0	mii0_txd2	vin2a_d7	vin4b_d7	usb4_ulpi_d4					gpio5_28	Driver off
0x1674	CTRL_CORE_PAD_RGMII0_RXD2	V3	rgmii0_rxd2	rmii0_txen		mii0_txen	vin2a_d8		usb4_ulpi_d5					gpio5_29	Driver off
0x1678	CTRL_CORE_PAD_RGMII0_RXD1	Y2	rgmii0_rxd1	rmii0_txd1		mii0_txd1	vin2a_d9		usb4_ulpi_d6					gpio5_30	Driver off
0x167C	CTRL_CORE_PAD_RGMII0_RXD0	W2	rgmii0_rxd0	rmii0_txd0		mii0_txd0	vin2a_fld0	vin4b_fld1	usb4_ulpi_d7					gpio5_31	Driver off
0x1680	CTRL_CORE_PAD_USB1_DRVVBUS	AB10	usb1_drvvbus							timer16				gpio6_12	Driver off
0x1684	CTRL_CORE_PAD_USB2_DRVVBUS	AC10	usb2_drvvbus							timer15				gpio6_13	Driver off
0x1688	CTRL_CORE_PAD_GPIO6_14	E21	gpio6_14	mcasp1_axr8	dcan2_tx mcan_tx	uart10_rxd			vout2_hsync		vin4a_hsync0	i2c3_sda	timer1	gpio6_14	Driver off
0x168C	CTRL_CORE_PAD_GPIO6_15	F20	gpio6_15	mcasp1_axr9	dcan2_rx mcan_rx	uart10_txd			vout2_vsync		vin4a_vsync0	i2c3_scl	timer2	gpio6_15	Driver off
0x1690	CTRL_CORE_PAD_GPIO6_16	F21	gpio6_16	mcasp1_axr10					vout2_fld		vin4a_fld0	clkout1	timer3	gpio6_16	Driver off
0x1694	CTRL_CORE_PAD_XREF_CLK0	D18	xref_clk0	mcasp2_axr8	mcasp1_axr4	mcasp1_ahclkx	mcasp5_ahclkx					clkout2	timer13	gpio6_17	Driver off
0x1698	CTRL_CORE_PAD_XREF_CLK1	E17	xref_clk1	mcasp2_axr9	mcasp1_axr5	mcasp2_ahclkx	mcasp6_ahclkx						timer14	gpio6_18	Driver off
0x169C	CTRL_CORE_PAD_XREF_CLK2	B26	xref_clk2	mcasp2_axr10	mcasp1_axr6	mcasp3_ahclkx	mcasp7_ahclkx		vout2_clk		vin4a_clk0		timer15	gpio6_19	Driver off
0x16A0	CTRL_CORE_PAD_XREF_CLK3	C23	xref_clk3	mcasp2_axr11	mcasp1_axr7	mcasp4_ahclkx	mcasp8_ahclkx		vout2_de		vin4a_de0	clkout3	timer16	gpio6_20	Driver off
0x16A4	CTRL_CORE_PAD_MCASP1_ACLKX	C14	mcasp1_aclkx										i2c3_sda	gpio7_31	Driver off
0x16A8	CTRL_CORE_PAD_MCASP1_FSX	D14	mcasp1_fsx										i2c3_scl	gpio7_30	Driver off
0x16AC	CTRL_CORE_PAD_MCASP1_ACLKR	B14	mcasp1_aclkr	mcasp7_axr2					vout2_d0		vin4a_d0		i2c4_sda	gpio5_0	Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x16B0	CTRL_CORE_PAD_MCASP1_FSR	J14	mcasp1_fsr	mcasp7_axr3					vout2_d1		vin4a_d1		i2c4_scl	gpio5_1	Driver off
0x16B4	CTRL_CORE_PAD_MCASP1_AXR0	G12	mcasp1_axr0			uart6_rxd							i2c5_sda	gpio5_2	Driver off
0x16B8	CTRL_CORE_PAD_MCASP1_AXR1	F12	mcasp1_axr1			uart6_txd							i2c5_scl	gpio5_3	Driver off
0x16BC	CTRL_CORE_PAD_MCASP1_AXR2	G13	mcasp1_axr2	mcasp6_axr2		uart6_ctsn			vout2_d2		vin4a_d2			gpio5_4	Driver off
0x16C0	CTRL_CORE_PAD_MCASP1_AXR3	J11	mcasp1_axr3	mcasp6_axr3		uart6_rtsn			vout2_d3		vin4a_d3			gpio5_5	Driver off
0x16C4	CTRL_CORE_PAD_MCASP1_AXR4	E12	mcasp1_axr4	mcasp4_axr2					vout2_d4		vin4a_d4			gpio5_6	Driver off
0x16C8	CTRL_CORE_PAD_MCASP1_AXR5	F13	mcasp1_axr5	mcasp4_axr3					vout2_d5		vin4a_d5			gpio5_7	Driver off
0x16CC	CTRL_CORE_PAD_MCASP1_AXR6	C12	mcasp1_axr6	mcasp5_axr2					vout2_d6		vin4a_d6			gpio5_8	Driver off
0x16D0	CTRL_CORE_PAD_MCASP1_AXR7	D12	mcasp1_axr7	mcasp5_axr3					vout2_d7		vin4a_d7		timer4	gpio5_9	Driver off
0x16D4	CTRL_CORE_PAD_MCASP1_AXR8	B12	mcasp1_axr8	mcasp6_axr0		spi3_sclk							timer5	gpio5_10	Driver off
0x16D8	CTRL_CORE_PAD_MCASP1_AXR9	A11	mcasp1_axr9	mcasp6_axr1		spi3_d1							timer6	gpio5_11	Driver off
0x16DC	CTRL_CORE_PAD_MCASP1_AXR10	B13	mcasp1_axr10	mcasp6_aclkx	mcasp6_aclkr	spi3_d0							timer7	gpio5_12	Driver off
0x16E0	CTRL_CORE_PAD_MCASP1_AXR11	A12	mcasp1_axr11	mcasp6_fsx	mcasp6_fsr	spi3_cs0							timer8	gpio4_17	Driver off
0x16E4	CTRL_CORE_PAD_MCASP1_AXR12	E14	mcasp1_axr12	mcasp7_axr0		spi3_cs1							timer9	gpio4_18	Driver off
0x16E8	CTRL_CORE_PAD_MCASP1_AXR13	A13	mcasp1_axr13	mcasp7_axr1									timer10	gpio6_4	Driver off
0x16EC	CTRL_CORE_PAD_MCASP1_AXR14	G14	mcasp1_axr14	mcasp7_aclkx	mcasp7_aclkr								timer11	gpio6_5	Driver off
0x16F0	CTRL_CORE_PAD_MCASP1_AXR15	F14	mcasp1_axr15	mcasp7_fsx	mcasp7_fsr								timer12	gpio6_6	Driver off
0x16F4	CTRL_CORE_PAD_MCASP2_ACLKX	A19	mcasp2_aclkx												Driver off
0x16F8	CTRL_CORE_PAD_MCASP2_FSX	A18	mcasp2_fsx												Driver off
0x16FC	CTRL_CORE_PAD_MCASP2_ACLKR	E15	mcasp2_aclkr	mcasp8_axr2					vout2_d8		vin4a_d8				Driver off
0x1700	CTRL_CORE_PAD_MCASP2_FSR	A20	mcasp2_fsr	mcasp8_axr3					vout2_d9		vin4a_d9				Driver off
0x1704	CTRL_CORE_PAD_MCASP2_AXR0	B15	mcasp2_axr0						vout2_d10		vin4a_d10				Driver off
0x1708	CTRL_CORE_PAD_MCASP2_AXR1	A15	mcasp2_axr1						vout2_d11		vin4a_d11				Driver off
0x170C	CTRL_CORE_PAD_MCASP2_AXR2	C15	mcasp2_axr2	mcasp3_axr2										gpio6_8	Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x1710	CTRL_CORE_PAD_MCASP2_AXR3	A16	mcasp2_axr3	mcasp3_axr3										gpio6_9	Driver off
0x1714	CTRL_CORE_PAD_MCASP2_AXR4	D15	mcasp2_axr4	mcasp8_axr0					vout2_d12		vin4a_d12			gpio1_4	Driver off
0x1718	CTRL_CORE_PAD_MCASP2_AXR5	B16	mcasp2_axr5	mcasp8_axr1					vout2_d13		vin4a_d13			gpio6_7	Driver off
0x171C	CTRL_CORE_PAD_MCASP2_AXR6	B17	mcasp2_axr6	mcasp8_aclkx	mcasp8_aclkr				vout2_d14		vin4a_d14			gpio2_29	Driver off
0x1720	CTRL_CORE_PAD_MCASP2_AXR7	A17	mcasp2_axr7	mcasp8_fsx	mcasp8_fsr				vout2_d15		vin4a_d15			gpio1_5	Driver off
0x1724	CTRL_CORE_PAD_MCASP3_ACLKX	B18	mcasp3_aclkx	mcasp3_aclkr	mcasp2_axr12	uart7_rxd								gpio5_13	Driver off
0x1728	CTRL_CORE_PAD_MCASP3_FSX	F15	mcasp3_fsx	mcasp3_fsr	mcasp2_axr13	uart7_txd								gpio5_14	Driver off
0x172C	CTRL_CORE_PAD_MCASP3_AXR0	B19	mcasp3_axr0		mcasp2_axr14	uart7_ctsn	uart5_rxd								Driver off
0x1730	CTRL_CORE_PAD_MCASP3_AXR1	C17	mcasp3_axr1		mcasp2_axr15	uart7_rtsn	uart5_txd								Driver off
0x1734	CTRL_CORE_PAD_MCASP4_ACLKX	C18	mcasp4_aclkx	mcasp4_aclkr	spi3_sclk	uart8_rxd	i2c4_sda		vout2_d16		vin4a_d16				Driver off
0x1738	CTRL_CORE_PAD_MCASP4_FSX	A21	mcasp4_fsx	mcasp4_fsr	spi3_d1	uart8_txd	i2c4_scl		vout2_d17		vin4a_d17				Driver off
0x173C	CTRL_CORE_PAD_MCASP4_AXR0	G16	mcasp4_axr0		spi3_d0	uart8_ctsn	uart4_rxd		vout2_d18		vin4a_d18				Driver off
0x1740	CTRL_CORE_PAD_MCASP4_AXR1	D17	mcasp4_axr1		spi3_cs0	uart8_rtsn	uart4_txd		vout2_d19		vin4a_d19				Driver off
0x1744	CTRL_CORE_PAD_MCASP5_ACLKX	AA3	mcasp5_aclkx	mcasp5_aclkr	spi4_sclk	uart9_rxd	i2c5_sda		vout2_d20		vin4a_d20				Driver off
0x1748	CTRL_CORE_PAD_MCASP5_FSX	AB9	mcasp5_fsx	mcasp5_fsr	spi4_d1	uart9_txd	i2c5_scl		vout2_d21		vin4a_d21				Driver off
0x174C	CTRL_CORE_PAD_MCASP5_AXR0	AB3	mcasp5_axr0		spi4_d0	uart9_ctsn	uart3_rxd		vout2_d22		vin4a_d22				Driver off
0x1750	CTRL_CORE_PAD_MCASP5_AXR1	AA4	mcasp5_axr1		spi4_cs0	uart9_rtsn	uart3_txd		vout2_d23		vin4a_d23				Driver off
0x1754	CTRL_CORE_PAD_MMC1_CLK	W6	mmc1_clk											gpio6_21	Driver off
0x1758	CTRL_CORE_PAD_MMC1_CMD	Y6	mmc1_cmd											gpio6_22	Driver off
0x175C	CTRL_CORE_PAD_MMC1_DAT0	AA6	mmc1_dat0											gpio6_23	Driver off
0x1760	CTRL_CORE_PAD_MMC1_DAT1	Y4	mmc1_dat1											gpio6_24	Driver off
0x1764	CTRL_CORE_PAD_MMC1_DAT2	AA5	mmc1_dat2											gpio6_25	Driver off
0x1768	CTRL_CORE_PAD_MMC1_DAT3	Y3	mmc1_dat3											gpio6_26	Driver off
0x176C	CTRL_CORE_PAD_MMC1_SDCD	W7	mmc1_sdcd			uart6_rxd	i2c4_sda							gpio6_27	Driver off
0x1770	CTRL_CORE_PAD_MMC1_SDWP	Y9	mmc1_sdwp			uart6_txd	i2c4_scl							gpio6_28	Driver off
0x1774	CTRL_CORE_PAD_GPIO6_10	AC5	gpio6_10	mdio_mclk	i2c3_sda	usb3_ulpi_d7	vin2b_hsync1						ehrpwm2A	gpio6_10	Driver off
0x1778	CTRL_CORE_PAD_GPIO6_11	AB4	gpio6_11	mdio_d	i2c3_scl	usb3_ulpi_d6	vin2b_vsync1						ehrpwm2B	gpio6_11	Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])												
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x177C	CTRL_CORE_PAD_MMC3_CLK	AD4	mmc3_clk			usb3_ulpi_d5	vin2b_d7						ehrpwm2_tripzone_input	gpio6_29	Driver off
0x1780	CTRL_CORE_PAD_MMC3_CMD	AC4	mmc3_cmd	spi3_sclk		usb3_ulpi_d4	vin2b_d6						eCAP2_in_PWM2_out	gpio6_30	Driver off
0x1784	CTRL_CORE_PAD_MMC3_DAT0	AC7	mmc3_dat0	spi3_d1	uart5_rxd	usb3_ulpi_d3	vin2b_d5						eQEP3A_in	gpio6_31	Driver off
0x1788	CTRL_CORE_PAD_MMC3_DAT1	AC6	mmc3_dat1	spi3_d0	uart5_txd	usb3_ulpi_d2	vin2b_d4						eQEP3B_in	gpio7_0	Driver off
0x178C	CTRL_CORE_PAD_MMC3_DAT2	AC9	mmc3_dat2	spi3_cs0	uart5_ctsn	usb3_ulpi_d1	vin2b_d3						eQEP3_index	gpio7_1	Driver off
0x1790	CTRL_CORE_PAD_MMC3_DAT3	AC3	mmc3_dat3	spi3_cs1	uart5_rtsn	usb3_ulpi_d0	vin2b_d2						eQEP3_strobe	gpio7_2	Driver off
0x1794	CTRL_CORE_PAD_MMC3_DAT4	AC8	mmc3_dat4	spi4_sclk	uart10_rxd	usb3_ulpi_nxt	vin2b_d1						ehrpwm3A	gpio1_22	Driver off
0x1798	CTRL_CORE_PAD_MMC3_DAT5	AD6	mmc3_dat5	spi4_d1	uart10_txd	usb3_ulpi_dir	vin2b_d0						ehrpwm3B	gpio1_23	Driver off
0x179C	CTRL_CORE_PAD_MMC3_DAT6	AB8	mmc3_dat6	spi4_d0	uart10_ctsn	usb3_ulpi_stp	vin2b_de1						ehrpwm3_tripzone_input	gpio1_24	Driver off
0x17A0	CTRL_CORE_PAD_MMC3_DAT7	AB5	mmc3_dat7	spi4_cs0	uart10_rtsn	usb3_ulpi_clk	vin2b_clk1						eCAP3_in_PWM3_out	gpio1_25	Driver off
0x17A4	CTRL_CORE_PAD_SPI1_SCLK	A25	spi1_sclk											gpio7_7	Driver off
0x17A8	CTRL_CORE_PAD_SPI1_D1	F16	spi1_d1											gpio7_8	Driver off
0x17AC	CTRL_CORE_PAD_SPI1_D0	B25	spi1_d0											gpio7_9	Driver off
0x17B0	CTRL_CORE_PAD_SPI1_CS0	A24	spi1_cs0											gpio7_10	Driver off
0x17B4	CTRL_CORE_PAD_SPI1_CS1	A22	spi1_cs1		sata1_led	spi2_cs1								gpio7_11	Driver off
0x17B8	CTRL_CORE_PAD_SPI1_CS2	B21	spi1_cs2	uart4_rxd	mmc3_sdcd	spi2_cs2	dcan2_tx	mdio_mclk	hdmi1_hpd					gpio7_12	Driver off
0x17BC	CTRL_CORE_PAD_SPI1_CS3	B20	spi1_cs3	uart4_txd	mmc3_sdwp	spi2_cs3	dcan2_rx	mdio_d	hdmi1_cec					gpio7_13	Driver off
0x17C0	CTRL_CORE_PAD_SPI2_SCLK	A26	spi2_sclk	uart3_rxd										gpio7_14	Driver off
0x17C4	CTRL_CORE_PAD_SPI2_D1	B22	spi2_d1	uart3_txd										gpio7_15	Driver off
0x17C8	CTRL_CORE_PAD_SPI2_D0	G17	spi2_d0	uart3_ctsn	uart5_rxd									gpio7_16	Driver off
0x17CC	CTRL_CORE_PAD_SPI2_CS0	B24	spi2_cs0	uart3_rtsn	uart5_txd									gpio7_17	Driver off
0x17E0	CTRL_CORE_PAD_UART1_RXD	B27	uart1_rxd			mmc4_sdcd								gpio7_22	Driver off
0x17E4	CTRL_CORE_PAD_UART1_TXD	C26	uart1_txd			mmc4_sdwp								gpio7_23	Driver off
0x17E8	CTRL_CORE_PAD_UART1_CTSN	E25	uart1_ctsn		uart9_rxd	mmc4_clk								gpio7_24	Driver off
0x17EC	CTRL_CORE_PAD_UART1_RTSN	C27	uart1_rtsn		uart9_txd	mmc4_cmd								gpio7_25	Driver off
0x17F0	CTRL_CORE_PAD_UART2_RXD	D28		uart3_ctsn	uart3_rctx	mmc4_dat0	uart2_rxd	uart1_dcdn						gpio7_26	Driver off
0x17F4	CTRL_CORE_PAD_UART2_TXD	D26	uart2_txd	uart3_rtsn	uart3_sd	mmc4_dat1	uart2_txd	uart1_dsrn						gpio7_27	Driver off
0x17F8	CTRL_CORE_PAD_UART2_CTSN	D27	uart2_ctsn		uart3_rxd	mmc4_dat2	uart10_rxd	uart1_dtrn						gpio1_16	Driver off
0x17FC	CTRL_CORE_PAD_UART2_RTSN	C28	uart2_rtsn	uart3_txd	uart3_irtx	mmc4_dat3	uart10_txd	uart1_rin						gpio1_17	Driver off
0x1800	CTRL_CORE_PAD_I2C1_SDA	C21	i2c1_sda												
0x1804	CTRL_CORE_PAD_I2C1_SCL	C20	i2c1_scl												
0x1808	CTRL_CORE_PAD_I2C2_SDA	C25	i2c2_sda	hdmi1_ddc_scl											Driver off
0x180C	CTRL_CORE_PAD_I2C2_SCL	F17	i2c2_scl	hdmi1_ddc_sda											Driver off

Table 4-29. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE FIELD SETTINGS (CTRL_CORE_PAD_*[3:0])											
			0*	1	2*	3	4	5	6	7	8	9	10	14*	15
0x1818	CTRL_CORE_PAD_WAKEUP0	AD17	Wakeup0	dcan1_rx										gpio1_0	Driver off
0x181C	CTRL_CORE_PAD_WAKEUP1	AC17	Wakeup1	dcan2_rx										gpio1_1	Driver off
0x1820	CTRL_CORE_PAD_WAKEUP2	AB16	Wakeup2	sys_nirq2										gpio1_2	Driver off
0x1824	CTRL_CORE_PAD_WAKEUP3	AC16	Wakeup3	sys_nirq1										gpio1_3	Driver off
0x1828	CTRL_CORE_PAD_ON_OFF	Y11	on_off												
0x182C	CTRL_CORE_PAD_RTC_PORZ	AB17	rtc_porz												
0x1830	CTRL_CORE_PAD_TMS	F18	tms												
0x1834	CTRL_CORE_PAD_TDI	D23	tdi											gpio8_27	
0x1838	CTRL_CORE_PAD_TDO	F19	tdo											gpio8_28	
0x183C	CTRL_CORE_PAD_TCLK	E20	tclk												
0x1840	CTRL_CORE_PAD_TRSTN	D20	trstn												
0x1844	CTRL_CORE_PAD_RTCK	E18	rtck											gpio8_29	
0x1848	CTRL_CORE_PAD_EMU0	G21	emu0											gpio8_30	
0x184C	CTRL_CORE_PAD_EMU1	D24	emu1											gpio8_31	
0x185C	CTRL_CORE_PAD_RESETN	E23	resetn												
0x1860	CTRL_CORE_PAD_NMIN_DSP	D21	nmin_dsp												
0x1864	CTRL_CORE_PAD_RSTOUTN	F23	rstoutn												

1. NA in this table stands for Not Applicable.

4.5 Connections for Unused Pins

This section describes the Unused/Reserved balls connection requirements.

NOTE

The following balls are reserved: A27 / Y5 / Y10 / AA1 / AA2 / AB1 / AB2 / AC1 / AC2 / B28

These balls must be left unconnected.

NOTE

All unused power supply balls must be supplied with the voltages specified in the Section 5.4, *Recommended Operating Conditions,* unless alternative tie-off options are included in Section 4.3, *Signal Descriptions*.

Table 4-30. Unused Balls Specific Connection Requirements

Balls	Connection Requirements
AE15 / AC15 / AE14 / D20 / AD17 / AC17 / AC16 / AB16 / V27 / AH25 / AE27 / AD27 / Y28 / G28 / H27 / K27 / M28	These balls must be connected to GND through an external pull resistor if unused
V28 / F18 / E20 / E23 / D21 / C20 / C21 / AG25 / AE28 / AD28 / Y27 / G27 / H28 / K28 / M27 / F17 / C25	These balls must be connected to the corresponding power supply through an external pull resistor if unused
AF14 (rtc_iso)	This ball should be connected to the corresponding power supply through an external pull resistor if unused; or can be connected to F22 (porz) when RTC unused (level translation may be needed)
AB17 (rtc_porz)	This ball should be connected to VSS when RTC is unused; or can be connected to F22 (porz) when RTC unused (level translation may be needed)
K14 (vpp)	This ball must be left unconnected if unused.

NOTE

All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their internal pullup or pulldown resistor enabled.

NOTE

All other unused signal balls **without** Pad Configuration Register can be left unconnected.

5 Specifications

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs or Initialization / Preinitialization / Power Requirements section of the Device TRM.

NOTE

The index numbers 1 and 2 which is part of the EMIF1 and EMIF2 signal prefixes (ddr1_* and ddr2_*) listed in Table 4-5, *EMIF Signal Descriptions*, column "SIGNAL NAME" not to be confused with DDR1 and DDR2 types of SDRAM memories.

NOTE

Audio Back End (ABE) module is not supported for this family of devices, but “ABE” name is still present in some clock or DPLL names.

CAUTION

All IO cells are NOT Fail-safe compliant and should not be externally driven in absence of their IO supply.

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER(2)			MIN	MAX	UNIT
V_{SUPPLY} (Steady-State)	Supply Voltage Ranges (Steady-State)	Core (vdd, vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva, vdd_rtc)	-0.3	1.5	V
		Analog (vdda_usb1, vdda_usb2, vdda_abe_per, vdda_ddr, vdda_debug, vdda_dsp_eve, vdda_gmac_core, vdda_gpu, vdda_hdmi, vdda_iva, vdda_pcie, vdda_pcie0, vdda_pcie1, vdda_sata, vdda_usb3, vdda_video, vdda_mpu, vdda_osc, vdda_rtc)	-0.3	2.0	V
		Analog 3.3 V (vdda33v_usb1, vdda33v_usb2)	-0.3	3.8	V
		vdds18v, vdds18v_ddr1, vdds18v_ddr2, vdds_mlbp, vdds_ddr1, vdds_ddr2	-0.3	2.1	V
		vddshv1-11 (1.8 V mode)	-0.3	2.1	V
		vddshv1-7 (3.3 V mode), vddshv9-11 (3.3 V mode)	-0.3	3.8	V
		vddshv8 (3.3 V mode)	-0.3	3.6	V
V_{IO} (Steady-State)	Input and Output Voltage Ranges (Steady-State)	Core I/Os	-0.3	1.5	V
		Analog I/Os (except HDMI)	-0.3	2.0	V
		HDMI I/Os	-0.3	3.5	V
		I/O 1.35 V	-0.3	1.65	V
		I/O 1.5 V	-0.3	1.8	V
		1.8 V I/Os	-0.3	2.1	V
		3.3 V I/Os (except those powered by vddshv8)	-0.3	3.8	V
		3.3 V I/Os (powered by vddshv8)	-0.3	3.6	V
SR	Maximum slew rate, all supplies			10^5	V/s
V_{IO} (Transient Overshoot / Undershoot)	Input and Output Voltage Ranges (Transient Overshoot/Undershoot) Note: valid for up to 20 % of the signal period. See Figure 5-1, $T_{overshoot}$ + $T_{undershoot}$ < 20% of T_{period}			0.2 × VDD (3)	V
T_J	Operating junction temperature range	Automotive	-40	+ 125	°C
T_{STG}	Storage temperature range after soldered onto PC Board		-55	+ 150	°C
Latch-up I-Test	I-test(4), All I/Os (if different then one line per level)		-100	100	mA
Latch-up OV-Test	Over-voltage Test(5), All supplies (if different levels then one line per level)		N/A	1.5 × Vsupply max	V

(1) Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Section 5.4, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) See I/Os supplied by this power pin in Table 4-1, *Pin Attributes*.

(3) VDD is the voltage on the corresponding power-supply pin(s) for the IO.

(4) Per JEDEC JESD78 at 125 °C with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

(5) Per JEDEC JESD78 at 125 °C.

(6) The maximum valid input voltage on an IO pin cannot exceed 0.3 volts when the supply powering the IO is turned off. This requirement applies to all the IO pins which are not fail-safe and for all values of IO supply voltage. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.

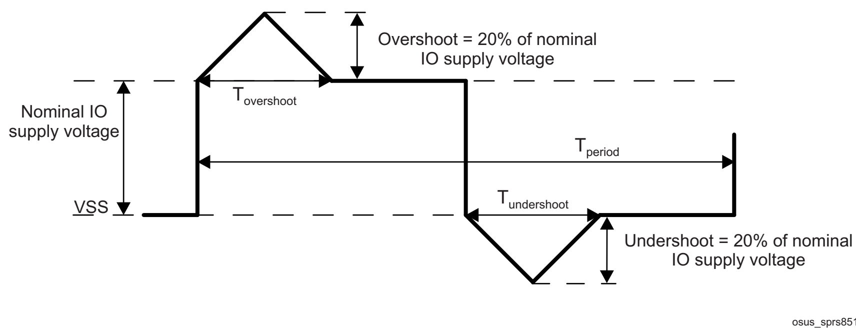


Figure 5-1. $T_{overshoot}$ + $T_{undershoot}$ < 20% of T_{period}

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body model (HBM), per AEC Q100-002[(1)]		±1000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±250	
			Corner pins (A1, AH1, A28, AH28)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Power-On Hours (POH) Limits

IP	Duty Cycle	Voltage Domain	Voltage (V) (max)	Frequency (MHz) (max)	Tj(°C)	POH
All	100%	All	All Supported OPPs		Automotive Profile[(3)]	20000

(1) The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

(2) POH is a functional of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH to achieve the same reliability performance. For assessment of alternate use cases, contact your local TI representative.

(3) Automotive profile is defined as 20000 power on hours with junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, 10%@125°C.

5.4 Recommended Operating Conditions[(5)]

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN [(2)]	NOM	MAX DC [(3)]	MAX [(2)]	UNIT
Input Power Supply Voltage Range						
vdd	Core voltage domain supply		See Section 5.5			V
vdd_mpu	Supply voltage range for MPU domain		See Section 5.5			V
vdd_gpu	GPU voltage domain supply		See Section 5.5			V
vdd_dspeve	DSP-EVE voltage domain supply		See Section 5.5			V
vdd_iva	IVA voltage domain supply		See Section 5.5			V
vdd_rtc	RTC voltage domain supply		See Section 5.5			V
vdda_usb1	DPLL_USB and HS USB1 1.8 V analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_usb2	HS USB2 1.8 V analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}

Recommended Operating Conditions[5] *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN [2]	NOM	MAX DC [3]	MAX [2]	UNIT
vdda33v_usb1	HS USB1 3.3 V analog power supply.If USB1 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb1_dm/usb1_dp pins are left unconnected - The USB1 PHY is kept powered down	3.135	3.3	3.366	3.465	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda33v_usb2	HS USB2 3.3 V analog power supply. If USB2 is not used, this pin can alternatively be connected to VSS if the following requirements are met: - The usb2_dm/usb2_dp pins are left unconnected - The USB2 PHY is kept powered down	3.135	3.3	3.366	3.465	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_abe_per	DPLL_ABE, DPLL_PER, and PER HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_debug	DPLL_DEBUG analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_dsp_eve	DPLL_DSP and DPLL_EVE analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_gmac_core	DPLL_CORE and CORE HSDIVIDER analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_gpu	DPLL_GPU analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_hdmi	PLL_HDMI and HDMI analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_iva	DPLL_IVA analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_pcie	DPLL_PCIe_REF and PCIe analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_pcie0	PCIe ch0 RX/TX analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_pcie1	PCIe ch1 RX/TX analog power supply	1.71	1.80		1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_sata	DPLL_SATA and SATA RX/TX analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}
vdda_usb3	DPLL_USB_OTG_SS and USB3.0 RX/TX analog power supply	1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)		50			mV_{PPmax}

Recommended Operating Conditions[(5)] *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION		MIN [(2)]	NOM	MAX DC [(3)]	MAX [(2)]	UNIT
vdda_video	DPLL_VIDEO1 and DPLL_VIDEO2 analog power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds_mlbp	MLBP IO power supply		1.71	1.80		1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdda_mpu	DPLL_MPU analog power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdda_osc	HFOSC analog power supply		1.71	1.80		1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdda_rtc	RTC bias and RTC LFOSC analog power supply		1.71	1.80		1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds18v	1.8 V power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds18v_ddr1 [(4)]	DDR1 bias power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds18v_ddr2 [(4)]	DDR2 bias power supply		1.71	1.80	1.836	1.89	V
	Maximum noise (peak-peak)			50			mV_{PPmax}
vdds_ddr1 [(4)]	DDR1 power supply (1.8 V for DDR2 mode/ 1.5 V for DDR3 mode / 1.35 V for DDR3L mode)	1.35-V Mode	1.28	1.35	1.377	1.42	V
		1.5-V Mode	1.43	1.50	1.53	1.57	
		1.8-V Mode	1.71	1.80	1.836	1.89	
	Maximum noise (peak-peak)	1.35-V Mode		50			mV_{PPmax}
		1.5-V Mode					
		1.8-V Mode					
vdds_ddr2 [(4)]	DDR2 power supply (1.8 V for DDR2 mode/ 1.5 V for DDR3 mode / 1.35 V for DDR3L mode)	1.35-V Mode	1.28	1.35	1.377	1.42	V
		1.5-V Mode	1.43	1.50	1.53	1.57	
		1.8-V Mode	1.71	1.80	1.836	1.89	
	Maximum noise (peak-peak)	1.35-V Mode		50			mV_{PPmax}
		1.5-V Mode					
		1.8-V Mode					
vddshv5	Dual Voltage (1.8 V or 3.3 V) power supply for the INTC Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv1	Dual Voltage (1.8 V or 3.3 V) power supply for the VIN2 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					

Recommended Operating Conditions[5] *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION		MIN [2]	NOM	MAX DC [3]	MAX [2]	UNIT
vddshv10	Dual Voltage (1.8 V or 3.3 V) power supply for the GPMC Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv11	Dual Voltage (1.8 V or 3.3 V) power supply for the MMC2 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv2	Dual Voltage (1.8 V or 3.3 V) power supply for the VOUT Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv3	Dual Voltage (1.8 V or 3.3 V) power supply for the GENERAL Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv4	Dual Voltage (1.8 V or 3.3 V) power supply for the MMC4 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv6	Dual Voltage (1.8 V or 3.3 V) power supply for the VIN1 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv7	Dual Voltage (1.8 V or 3.3 V) power supply for the WIFI Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv8	Dual Voltage (1.8 V or 3.3 V) power supply for the MMC1 Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vddshv9	Dual Voltage (1.8 V or 3.3 V) power supply for the RGMII Power Group pins	1.8-V Mode	1.71	1.80	1.836	1.89	V
		3.3-V Mode	3.135	3.30	3.366	3.465	
	Maximum noise (peak-peak)	1.8-V Mode		50			mV_{PPmax}
		3.3-V Mode					
vss	Ground supply			0			V

Recommended Operating Conditions[5] *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION		MIN [2]	NOM	MAX DC [3]	MAX [2]	UNIT
vssa_osc0	OSC0 analog ground			0			V
vssa_osc1	OSC1 analog ground			0			V
T_J[1]	Operating junction temperature range	Automotive	-40			125[6]	°C
ddr1_vref0	Reference Power Supply for DDR1			0.5 × vdds_ddr1			V
ddr2_vref0	Reference Power Supply for DDR2			0.5 × vdds_ddr2			V

(1) Refer to Section 5.3, *Power-On Hours (POH)* for limitations.

(2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.

(3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.

(4) If DDR2 type of memories are used, the EMIF power supply (vdds_ddrx) and the corresponding bias power supply (vdds18v_ddrx) must be sourced from single power source.

(5) Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

(6) The TSHUT feature of the SoC resets the device by default when one of the on-die temp sensors reports 123°C. This is intended to protect the device from exceeding 125°C. Though not recommended, the TSHUT temperature threshold can be modified in software if other mechanisms are in place to avoid exceeding 125°C. Refer to the device TRM for details on the TSHUT feature.

5.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each OPP (operating performance point) for processor clocks and device core clocks.

Table 5-1 describes the maximum supported frequency per speed grade for the devices.

Table 5-1. Speed Grade Maximum Frequency

Device Speed	Maximum frequency (MHz)									
	MPU	DSP	EVE	IVA	ISP	GPU	IPU	L3	DDR3/ DDR3L	DDR2
TDA2PxxD	500	500	500	430	532	500	212.8	266	667 (DDR3-1333)	400 (DDR2-800)
TDA2PxxF	650	650	600	532	532	500	212.8	266	667 (DDR3-1333)	400 (DDR2-800)
TDA2PxxR	750	750	650	532	532	500	212.8	266	667 (DDR3-1333)	400 (DDR2-800)
TDA2PxxT	1176	750	650	532	532	532	212.8	266	667 (DDR3-1333)	400 (DDR2-800)
TDA2PxxU	1176	1000	900	532	532	665	212.8	266	667 (DDR3-1333)	400 (DDR2-800)

5.5.1 AVS and ABB Requirements

Adaptive Voltage Scaling (AVS) and Adaptive Body Biasing (ABB) are required on most of the vdd_* supplies as defined in Table 5-2.

Table 5-2. AVS and ABB Requirements per vdd_* Supply

Supply	AVS Required?	ABB Required?
vdd_core	Yes, for all OPPs	No
vdd_mpu	Yes, for all OPPs	Yes, for all OPPs
vdd_iva	Yes, for all OPPs	Yes, for all OPPs
vdd_dspeve	Yes, for all OPPs	Yes, for all OPPs
vdd_gpu	Yes, for all OPPs	Yes, for all OPPs
vdd_rtc	No	No

5.5.2 *Voltage And Core Clock Specifications*

Table 5-3 shows the recommended OPP per voltage domain.

Table 5-3. Voltage Domains Operating Performance Points

DOMAIN	CONDITION	OPP_LOW			OPP_NOM			OPP_OD			OPP_HIGH			
		MIN [2]	NOM [1]	MAX [2]	MIN [2]	NOM [1]	MAX [2]	MIN [2]	NOM [1]	MAX [2]	MIN [2]	NOM [1]	MAX DC [3]	MAX [2]
VD_CORE (V)	BOOT (Before AVS is enabled) [4]	Not Applicable			1.11	1.15	1.2	Not Applicable			Not Applicable			
	After AVS is enabled [4]	Not Applicable			AVS[5] – 3.5%	AVS[5]	1.2	Not Applicable			Not Applicable			
VD_MPU (V)	BOOT (Before AVS is enabled) [4]	Not Applicable			1.11	1.15	1.2	Not Applicable			Not Applicable			
	After AVS is enabled [4]	AVS Voltage [5] – 3.5%	AVS Voltage [5]	AVS Voltage [5] + 5%	AVS Voltage[5] – 3.5%	AVS Voltage[5]	1.2	AVS Voltage[5] – 3.5%	AVS Voltage[5]	AVS Voltage[5] + 5%	AVS Voltage[5] – 3.5%	AVS Voltage[5]	AVS Voltage[5] + 2%	AVS Voltage[5] + 5%
VD_RTC (V) [6]	-	Not Applicable			0.84	0.88 to 1.06	1.2	Not Applicable			Not Applicable			
Others (V)	BOOT (Before AVS is enabled) [4]	Not Applicable			1.02	1.06	1.2	Not Applicable			Not Applicable			
	After AVS is enabled [4]	Not Applicable			AVS Voltage[5] – 3.5%	AVS Voltage[5]	1.2	AVS Voltage[5] – 3.5%	AVS Voltage[5]	AVS Voltage[5] + 5%	AVS Voltage[5] – 3.5%	AVS Voltage[5]	AVS Voltage[5] + 2%	AVS Voltage[5] + 5%

(1) In a typical implementation, the power supply should target the NOM voltage.

(2) The voltage at the device ball should never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, etc.

(3) The DC voltage at the device ball should never be above the MAX DC voltage to avoid impact on device reliability and lifetime POH (Power-On Hours). The MAX DC voltage is defined as the highest allowed DC regulated voltage, without transients, seen at the ball.

(4) For all OPPs, AVS must be enabled to avoid impact on device reliability, lifetime POH (Power-On Hours), and device power.

(5) The AVS voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the STD_FUSE_OPP. For information about STD_FUSE_OPP Registers address, please refer to Control Module section of the Device TRM. The power supply should be adjustable over the following ranges for each required OPP:
   – OPP_LOW for MPU: 0.85 V - 1.15 V
   – OPP_NOM for MPU: 0.85 V - 1.15 V
   – OPP_NOM for CORE and Others: 0.85 V - 1.15 V
   – OPP_OD: 0.885 V - 1.15 V
   – OPP_HIGH: 0.95 V - 1.25 V
   The AVS voltages will be within the above specified ranges.

(6) VD_RTC can optionally be tied to VD_CORE and operate at the VD_CORE AVS voltages.

(7) The power supply must be programmed with the AVS voltages for the MPU and the CORE voltage domain, either just after the ROM boot or at the earliest possible time in the secondary boot loader before there is significant activity seen on these domains.

Table 5-4 describes the standard processor clocks speed characteristics vs OPP of the device.

Table 5-4. Supported OPP vs Max Frequency(1)(2)

DESCRIPTION	OPP_LOW	OPP_NOM	OPP_OD	OPP_HIGH
	Max Freq. (MHz)	Max Freq. (MHz)	Max Freq. (MHz)	Max Freq. (MHz)
VD_MPU				
MPU_CLK	750	1000	1176	1176
VD_DSPEVE				
DSP_CLK	N/A	600	700	750
EVE_FCLK	N/A	535	650	650
ISP_CLK	N/A	355	355	532
VD_IVA				
IVA_GCLK	N/A	388.3	430	532
VD_GPU				
GPU_CLK	N/A	425.6	500	532
VD_CORE				
CORE_IPUx_CLK	N/A	212.8	N/A	N/A
L3_CLK	N/A	266	N/A	N/A
DDR2	N/A	400 (DDR2-800)	N/A	N/A
DDR3 / DDR3L	N/A	667 (DDR3-1333)	N/A	N/A
VD_RTC				
RTC_FCLK	N/A	0.034	N/A	N/A

(1) N/A in this table stands for Not Applicable.

(2) Maximum supported frequency is limited according to the Device Speed Grade (see Table 5-1).

5.5.3 Maximum Supported Frequency

Device modules either receive their clock directly from an external clock input, directly from a PLL, or from a PRCM. Table 5-5 lists the clock source options for each module on this device, along with the maximum frequency that module can accept. To ensure proper module functionality, the device PLLs and dividers must be programmed not to exceed the maximum frequencies listed in this table.

Table 5-5. Maximum Supported Frequency

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
AES1	AES1_L3_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
AES2	AES2_L3_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
BB2D	BB2D_FCLK	Func	354.6	BB2D_GFCLK	BB2D_GFCLK	DPLL_CORE
	BB2D_ICLK	Int	266	DSS_L3_GICLK	CORE_X2_CLK	DPLL_CORE
COUNTER_32K	COUNTER_32K_FCLK	Func	0.032	FUNC_32K_CLK	SYS_CLK1/610	OSC0
	COUNTER_32K_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
CTRL_MODULE_BANDGAP	L3INSTR_TS_GCLK	Int	4.8	L3INSTR_TS_GCLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
CTRL_MODULE_CORE	L4CFG_L4_GICLK	Int	133	L4CFG_L4_GICLK	CORE_X2_CLK	DPLL_CORE
CTRL_MODULE_WKUP	WKUPAON_GICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
DCAN1	DCAN1_FCLK	Func	38.4	DCAN1_SYS_CLK	SYS_CLK1	OSC0
					SYS_CLK2	OSC1
	DCAN1_ICLK	Int	266	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
DCAN2	DCAN2_FCLK	Func	38.4	DCAN2_SYS_CLK	SYS_CLK1	OSC0
	DCAN2_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
DES3DES	DES_CLK_L3	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
DLL	EMIF_DLL_FCLK	Func	EMIF_DLL_FCLK	EMIF_DLL_GCLK	EMIF_DLL_GCLK	DPLL_DDR
DLL_AGING	FCLK	Int	38.4	L3INSTR_DLL_AGING_GCLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
DMA_CRYPTO	DMA_CRYPTO_FCLK	Int & Func	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	DMA_CRYPTO_ICLK	Int	133	L4SEC_L4_GICLK	CORE_X2_CLK	DPLL_CORE
DMM	DMM_CLK	Int	266	EMIF_L3_GICLK	CORE_X2_CLK	DPLL_CORE
DPLL_DEBUG	SYSCLK	Int	38.4	EMU_SYS_CLK	SYS_CLK1	OSC0
DSP1	DSP1_FICLK	Int & Func	DSP_CLK	DSP1_GFCLK	DSP_GFCLK	DPLL_DSP
DSP2	DSP2_FICLK	Int & Func	DSP_CLK	DSP2_GFCLK	DSP_GFCLK	DPLL_DSP

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
DSS	DSS_HDMI_CEC_CLK	Func	0.032	HDMI_CEC_GFCLK	SYS_CLK1/610	OSC0
	DSS_HDMI_PHY_CLK	Func	48	HDMI_PHY_GFCLK	FUNC_192M_CLK	DPLL_PER
	DSS_CLK	Func	192	DSS_GFCLK	DSS_CLK	DPLL_PER
	HDMI_CLKINP	Func	38.4	HDMI_DPLL_CLK	SYS_CLK1	OSC0
					SYS_CLK2	OSC1
	DSS_L3_ICLK	Int	266	DSS_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	VIDEO1_CLKINP	Func	38.4	VIDEO1_DPLL_CLK	SYS_CLK1	OSC0
					SYS_CLK2	OSC1
	VIDEO2_CLKINP	Func	38.4	VIDEO2_DPLL_CLK	SYS_CLK1	OSC0
					SYS_CLK2	OSC1
	DPLL_DSI1_A_CLK1	Func	209.3	N/A	HDMI_CLK	DPLL_HDMI
					VIDEO1_CLKOUT1	DPLL_VIDEO1
	DPLL_DSI1_B_CLK1	Func	209.3	N/A	VIDEO1_CLKOUT3	DPLL_VIDEO1
					VIDEO2_CLKOUT3	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
					DPLL_ABE_X2_CLK	DPLL_ABE
	DPLL_DSI1_C_CLK1	Func	209.3	N/A	HDMI_CLK	DPLL_HDMI
					VIDEO1_CLKOUT3	DPLL_VIDEO1
					VIDEO2_CLKOUT1	DPLL_VIDEO2
	DPLL_HDMI_CLK1	Func	185.6	N/A	HDMI_CLK	DPLL_HDMI
DSS DISPC	LCD1_CLK	Func	209.3	N/A	DPLL_DSI1_A_CLK1	See DSS data in the rows above
					DSS_CLK	
	LCD2_CLK	Func	209.3	N/A	DPLL_DSI1_B_CLK1	
					DSS_CLK	
	LCD3_CLK	Func	209.3	N/A	DPLL_DSI1_C_CLK1	
					DSS_CLK	
	F_CLK	Func	209.3	N/A	DPLL_DSI1_A_CLK1	
					DPLL_DSI1_B_CLK1	
					DPLL_DSI1_C_CLK1	
					DSS_CLK	
					DPLL_HDMI_CLK1	
ISP	ISS_MAIN_FCLK	Func	ISP_CLK	CORE_ISS_MAIN_CLK	CORE_ISS_MAIN_CLK	DPLL_CORE
	PCLK	Func		ISS_MAIN_FCLK	ISS_MAIN_FCLK	
EFUSE_CTRL_CUST	ocp_clk	Int	133	CUSTEFUSE_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	sys_clk	Func	38.4	CUSTEFUSE_SYS_GFCLK	SYS_CLK1	OSC0
ELM	ELM_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
EMIF_OCP_FW	L3_CLK	Int	266	EMIF_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
EMIF_PHY1	EMIF_PHY1_FCLK	Func	DDR	EMIF_PHY_GCLK	EMIF_PHY_GCLK	DPLL_DDR
EMIF_PHY2	EMIF_PHY2_FCLK	Func	DDR	EMIF_PHY_GCLK	EMIF_PHY_GCLK	DPLL_DDR
EMIF1	EMIF1_ICLK	Int	266	EMIF_L3_GICLK	CORE_X2_CLK	DPLL_CORE
EMIF2	EMIF2_ICLK	Int	266	EMIF_L3_GICLK	CORE_X2_CLK	DPLL_CORE
EVE1	EVE1_FCLK	Func	EVE_FCLK	EVE1_GFCLK	-	DPLL_DSP
					EVE_GFCLK	DPLL_EVE
EVE2	EVE2_FCLK	Func	EVE_FCLK	EVE2_GFCLK	-	DPLL_DSP
					EVE_GFCLK	DPLL_EVE
FPKA	PKA_CLK	Int & Func	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
GMAC_SW	CPTS_RFT_CLK	Func	266	GMAC_RFT_CLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
					CORE_X2_CLK	DPLL_CORE
	MAIN_CLK	Int	125	GMAC_MAIN_CLK	GMAC_250M_CLK	DPLL_GMAC
	MHZ_250_CLK	Func	250	GMII_250MHZ_CLK	GMII_250MHZ_CLK	DPLL_GMAC
	MHZ_5_CLK	Func	5	RGMII_5MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC
	MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC
	RMII1_MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC
	RMII2_MHZ_50_CLK	Func	50	RMII_50MHZ_CLK	GMAC_RMII_HS_CLK	DPLL_GMAC
GPIO1	GPIO1_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	GPIO1_DBCLK	Func	0.032	WKUPAON_SYS_GFCLK	WKUPAON_32K_GFCLK	OSC0[1]
GPIO2	GPIO2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO2_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0[1]
GPIO3	GPIO3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO3_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0[1]
GPIO4	GPIO4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO4_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0[1]
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPIO5	GPIO5_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO5_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0[1]
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPIO6	GPIO6_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO6_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0[1]
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPIO7	GPIO7_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO7_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0[1]
	PIDBCLK	Func	0.032	GPIO_GFCLK		

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
GPIO8	GPIO8_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	GPIO8_DBCLK	Func	0.032	GPIO_GFCLK	FUNC_32K_CLK	OSC0[(1)]
	PIDBCLK	Func	0.032	GPIO_GFCLK		
GPMC	GPMC_FCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
GPU	GPU_FCLK1	Func	GPU_CLK	GPU_CORE_GCLK	CORE_GPU_CLK	DPLL_CORE
					PER_GPU_CLK	DPLL_PER
					GPU_GCLK	DPLL_GPU
	GPU_FCLK2	Func	GPU_CLK	GPU_HYD_GCLK	CORE_GPU_CLK	DPLL_CORE
					PER_GPU_CLK	DPLL_PER
					GPU_GCLK	DPLL_GPU
	GPU_ICLK	Int	266	GPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
HDMI PHY	DSS_HDMI_PHY_CLK	Func	38.4	HDMI_PHY_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C1	I2C1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C1_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C2	I2C2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C2_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C3	I2C3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C3_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C4	I2C4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C4_FCLK	Func	96	PER_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
I2C5	I2C5_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	I2C5_FCLK	Func	96	IPU_96M_GFCLK	FUNC_192M_CLK	DPLL_PER
IEEE1500_2_OCP	PI_L3CLK	Int & Func	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
IPU1	IPU1_GFCLK	Int & Func	425.6	IPU1_GFCLK	DPLL_ABE_X2_CLK	DPLL_ABE
					CORE_IPU_ISS_BOOST_CLK	DPLL_CORE
IPU2	IPU2_GFCLK	Int & Func	425.6	IPU2_GFCLK	CORE_IPU_ISS_BOOST_CLK	DPLL_CORE
IVA	IVA_GCLK	Int	IVA_GCLK	IVA_GCLK	IVA_GFCLK	DPLL_IVA
L3_INSTR	L3_CLK	Int	L3_CLK	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L3_MAIN	L3_CLK1	Int	L3_CLK	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	L3_CLK2	Int	L3_CLK	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_CFG	L4_CFG_CLK	Int	133	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER1	L4_PER1_CLK	Int	133	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER2	L4_PER2_CLK	Int	133	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_PER3	L4_PER3_CLK	Int	133	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
L4_WKUP	L4_WKUP_CLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
MAILBOX1	MAILBOX1_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX2	MAILBOX2_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX3	MAILBOX3_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX4	MAILBOX4_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX5	MAILBOX5_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
MAILBOX6	MAILBOX6_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX7	MAILBOX7_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX8	MAILBOX8_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX9	MAILBOX9_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX10	MAILBOX10_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX11	MAILBOX11_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX12	MAILBOX12_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MAILBOX13	MAILBOX13_FLCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
McASP1	MCASP1_AHCLKR	Func	100	MCASP1_AHCLKR	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK0	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK3	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP1_AHCLKX	Func	100	MCASP1_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK0	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK3	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP1_FCLK	Func	192	MCASP1_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	MCASP1_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
McASP2	MCASP2_AHCLKR	Func	100	MCASP2_AHCLKR	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP2_AHCLKX	Func	100	MCASP2_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP2_FCLK	Func	192	MCASP2_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	MCASP2_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
McASP3	MCASP3_AHCLKX	Func	100	MCASP3_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP3_FCLK	Func	192	MCASP3_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	MCASP3_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
McASP4	MCASP4_AHCLKX	Func	100	MCASP4_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP4_FCLK	Func	192	MCASP4_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	MCASP4_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
McASP5	MCASP5_AHCLKX	Func	100	MCASP5_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP5_FCLK	Func	192	MCASP5_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	MCASP5_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
McASP6	MCASP6_AHCLKX	Func	100	MCASP6_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
					ABE_SYS_CLK	OSC0
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
	MCASP6_FCLK	Func	192	MCASP6_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	MCASP6_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
McASP7	MCASP7_AHCLKX	Func	100	MCASP7_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP7_FCLK	Func	192	MCASP7_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	MCASP7_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
McASP8	MCASP8_AHCLKX	Func	100	MCASP8_AHCLKX	ABE_24M_GFCLK	DPLL_ABE
					ABE_SYS_CLK	OSC0
					FUNC_24M_GFCLK	DPLL_PER
					ATL_CLK3	Module ATL
					ATL_CLK2	Module ATL
					ATL_CLK1	Module ATL
					ATL_CLK0	Module ATL
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					MLB_CLK	Module MLB
					MLBP_CLK	Module MLB
	MCASP8_FCLK	Func	192	MCASP8_AUX_GFCLK	PER_ABE_X1_GFCLK	DPLL_ABE
					VIDEO1_CLK	DPLL_ABE
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
	MCASP8_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
McSPI1	SPI1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI1_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
McSPI2	SPI2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI2_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
McSPI3	SPI3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI3_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
McSPI4	SPI4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SPI4_FCLK	Func	48	PER_48M_GFCLK	PER_48M_GFCLK	DPLL_PER
MMC1	MMC1_CLK_32K	Func	0.032	L3INIT_32K_GFCLK	FUNC_32K_CLK	OSC0
	MMC1_FCLK	Func	192	MMC1_GFCLK	FUNC_192M_CLK	DPLL_PER
			128		FUNC_256M_CLK	DPLL_PER
	MMC1_ICLK1	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC1_ICLK2	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
MMC2	MMC2_CLK_32K	Func	0.032	L3INIT_32K_GFCLK	FUNC_32K_CLK	OSC0
	MMC2_FCLK	Func	192	MMC2_GFCLK	FUNC_192M_CLK	DPLL_PER
			128		FUNC_256M_CLK	DPLL_PER
	MMC2_ICLK1	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC2_ICLK2	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
MMC3	MMC3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC3_CLK_32K	Func	0.032	L4PER_32K_GFCLK	FUNC_32K_CLK	OSC0
	MMC3_FCLK	Func	48	MMC3_GFCLK	FUNC_192M_CLK	DPLL_PER
			192			
MMC4	MMC4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	MMC4_CLK_32K	Func	0.032	L4PER_32K_GFCLK	FUNC_32K_CLK	OSC0
	MMC4_FCLK	Func	48	MMC4_GFCLK	FUNC_192M_CLK	DPLL_PER
			192			
MMU_EDMA	MMU1_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MMU_PCIESS	MMU2_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
MPU	MPU_CLK	Int & Func	MPU_CLK	MPU_GCLK	MPU_GCLK	DPLL_MPU
MPU_EMU_DBG	FCLK	Int	38.4	EMU_SYS_CLK	SYS_CLK1	OSC0
					MPU_GCLK	DPLL_MPU
OCMC_RAM1	OCMC1_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCMC_RAM2	OCMC2_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCMC_RAM3	OCMC3_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCMC_ROM	OCMC_L3_CLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCP_WP_NOC	PICLKOCPL3	Int	266	L3INSTR_L3_GICLK	CORE_X2_CLK	DPLL_CORE
OCP2SCP1	L4CFG1_ADAPTER_CLKIN	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE
OCP2SCP2	L4CFG2_ADAPTER_CLKIN	Int	133	L4CFG_L4_GICLK	CORE_X2_CLK	DPLL_CORE
OCP2SCP3	L4CFG3_ADAPTER_CLKIN	Int	133	L3INIT_L4_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
PCIESS1	PCIE1_PHY_WKUP_CLK	Func	0.032	PCIE_32K_GFCLK	FUNC_32K_CLK	OSC0(1)
	PCIe_SS1_FICLK	Int	266	PCIE_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	PCIEPHY_CLK	Func	2500	PCIE_PHY_GCLK	PCIE_PHY_GCLK	APLL_PCIE
	PCIEPHY_CLK_DIV	Func	1250	PCIE_PHY_DIV_GCLK	PCIE_PHY_DIV_GCLK	APLL_PCIE
	PCIE1_REF_CLKIN	Func	34.3	PCIE_REF_GFCLK	CORE_USB_OTG_SS_LFPS_TX_CLK	DPLL_CORE
	PCIE1_PWR_CLK	Func	38.4	PCIE_SYS_GFCLK	SYS_CLK1	OSC0
PCIESS2	PCIE2_PHY_WKUP_CLK	Func	0.032	PCIE_32K_GFCLK	FUNC_32K_CLK	OSC0(1)
	PCIe_SS2_FICLK	Func	266	PCIE_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	PCIEPHY_CLK	Func	2500	PCIE_PHY_GCLK	PCIE_PHY_GCLK	APLL_PCIE
	PCIEPHY_CLK_DIV	Func	1250	PCIE_PHY_DIV_GCLK	PCIE_PHY_DIV_GCLK	APLL_PCIE
	PCIE2_REF_CLKIN	Func	34.3	PCIE_REF_GFCLK	CORE_USB_OTG_SS_LFPS_TX_CLK	DPLL_CORE
	PCIE2_PWR_CLK	Func	38.4	PCIE_SYS_GFCLK	SYS_CLK1	OSC0
PRCM_MPU	32K_CLK	Func	0.032	FUNC_32K_CLK	SYS_CLK1/610	OSC0
	SYS_CLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
PWMSS1	PWMSS1_GICLK	Int & Func	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
PWMSS2	PWMSS2_GICLK	Int & Func	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
PWMSS3	PWMSS3_GICLK	Int & Func	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
QSPI	QSPI_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	QSPI_FCLK	Func	128	QSPI_GFCLK	FUNC_256M_CLK	DPLL_PER
					PER_QSPI_CLK	DPLL_PER
RNG	RNG_ICLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
RTC_SS	RTC_ICLK	Int	133	RTC_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	RTC_FCLK	Func	RTC_FCLK	RTC_AUX_CLK	FUNC_32K_CLK	OSC0(1)
				FUNC_32K_CLK	SYS_CLK1/610	OSC0
SAR_ROM	PRCM_ROM_CLOCK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SATA	SATA_FICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	SATA_PMALIVE_FCLK	Func	48	L3INIT_48M_GFCLK	FUNC_192M_CLK	DPLL_PER
	REF_CLK	Func	38	SATA_REF_GFCLK	SYS_CLK1	OSC0
SDMA	SDMA_FCLK	Int & Func	266	DMA_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SHA2MD51	SHAM_1_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SHA2MD52	SHAM_2_CLK	Int	266	L4SEC_L3_GICLK	CORE_X2_CLK	DPLL_CORE
SL2	IVA_GCLK	Int	IVA_GCLK	IVA_GCLK	IVA_GFCLK	DPLL_IVA

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
SMARTREFLEX_CORE	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SMARTREFLEX_DSPEVE	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SMARTREFLEX_GPU	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SMARTREFLEX_IVAHD	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SMARTREFLEX_MPU	MCLK	Int	133	COREAON_L4_GICLK	CORE_X2_CLK	DPLL_CORE
	SYSCLK	Func	38.4	WKUPAON_ICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
SPINLOCK	SPINLOCK_ICLK	Int	266	L4CFG_L3_GICLK	CORE_X2_CLK	DPLL_CORE
TIMER1	TIMER1_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	TIMER1_FCLK	Func	100	TIMER1_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[1]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
TIMER2	TIMER2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER2_FCLK	Func	100	TIMER2_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[(1)]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
TIMER3	TIMER3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER3_FCLK	Func	100	TIMER3_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[(1)]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
TIMER4	TIMER4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER4_FCLK	Func	100	TIMER4_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[(1)]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
TIMER5	TIMER5_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER5_FCLK	Func	100	TIMER5_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[1]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
					CLKOUTMUX[0]	CLKOUTMUX[0]
TIMER6	TIMER6_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER6_FCLK	Func	100	TIMER6_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[1]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
					CLKOUTMUX[0]	CLKOUTMUX[0]
TIMER7	TIMER7_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER7_FCLK	Func	100	TIMER7_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[1]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
					CLKOUTMUX[0]	CLKOUTMUX[0]

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
TIMER8	TIMER8_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER8_FCLK	Func	100	TIMER8_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[1]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
					CLKOUTMUX[0]	CLKOUTMUX[0]
TIMER9	TIMER9_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER9_FCLK	Func	100	TIMER9_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[1]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
TIMER10	TIMER10_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER10_FCLK	Func	100	TIMER10_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0[1]
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
TIMER11	TIMER11_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER11_FCLK	Func	100	TIMER11_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0(1)
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
TIMER12	TIMER12_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	TIMER12_FCLK	Func	0.032	OSC_32K_CLK	RC_CLK	OSC0(1)
TIMER13	TIMER13_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER13_FCLK	Func	100	TIMER13_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0(1)
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
TIMER14	TIMER14_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER14_FCLK	Func	100	TIMER14_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0(1)
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	Input Clock Name	Clock Type	Max. Clock Allowed (MHz)	PRCM Clock Name	PLL / OSC / Source Clock Name	PLL / OSC / Source Name
TIMER15	TIMER15_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER15_FCLK	Func	100	TIMER15_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0(1)
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
TIMER16	TIMER16_ICLK	Int	266	L4PER3_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	TIMER16_FCLK	Func	100	TIMER16_GFCLK	SYS_CLK1	OSC0
					FUNC_32K_CLK	OSC0(1)
					SYS_CLK2	OSC1
					XREF_CLK0	XREF_CLK0
					XREF_CLK1	XREF_CLK1
					XREF_CLK2	XREF_CLK2
					XREF_CLK3	XREF_CLK3
					DPLL_ABE_X2_CLK	DPLL_ABE
					VIDEO1_CLK	DPLL_VIDEO1
					VIDEO2_CLK	DPLL_VIDEO2
					HDMI_CLK	DPLL_HDMI
TPCC	TPCC_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
TPTC1	TPTC0_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
TPTC2	TPTC1_GCLK	Int	266	L3MAIN1_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART1	UART1_FCLK	Func	48	UART1_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART1_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART2	UART2_FCLK	Func	48	UART2_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART2_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART3	UART3_FCLK	Func	48	UART3_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART3_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART4	UART4_FCLK	Func	48	UART4_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART4_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART5	UART5_FCLK	Func	48	UART5_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART5_ICLK	Int	266	L4PER_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART6	UART6_FCLK	Func	48	UART6_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART6_ICLK	Int	266	IPU_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART7	UART7_FCLK	Func	48	UART7_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART7_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART8	UART8_FCLK	Func	48	UART8_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART8_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE

Table 5-5. Maximum Supported Frequency (continued)

Module				Clock Sources		
Instance Name	**Input Clock Name**	**Clock Type**	**Max. Clock Allowed (MHz)**	**PRCM Clock Name**	**PLL / OSC / Source Clock Name**	**PLL / OSC / Source Name**
UART9	UART9_FCLK	Func	48	UART9_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART9_ICLK	Int	266	L4PER2_L3_GICLK	CORE_X2_CLK	DPLL_CORE
UART10	UART10_FCLK	Func	48	UART10_GFCLK	FUNC_192M_CLK	DPLL_PER
	UART10_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
USB1	USB1_MICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	USB3PHY_REF_CLK	Func	34.3	USB_LFPS_TX_GFCLK	CORE_USB_OTG_SS_LFPS_TX_CLK	DPLL_CORE
	USB2PHY1_TREF_CLK	Func	38.4	USB_OTG_SS_REF_CLK	SYS_CLK1	OSC0
	USB2PHY1_REF_CLK	Func	960	L3INIT_960M_GFCLK	L3INIT_960_GFCLK	DPLL_USB
USB2	USB2_MICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	USB2PHY2_TREF_CLK	Func	38.4	USB_OTG_SS_REF_CLK	SYS_CLK1	OSC0
	USB2PHY2_REF_CLK	Func	960	L3INIT_960M_GFCLK	L3INIT_960_GFCLK	DPLL_USB
USB3	USB3_MICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	USB3PHY_PWRS_CLK	Func	38.4	USB_OTG_SS_REF_CLK	SYS_CLK1	OSC0
USB4	USB4_MICLK	Int	266	L3INIT_L3_GICLK	CORE_X2_CLK	DPLL_CORE
	DPLL_USBSS_REF_CLK	Func	38.4	USB_OTG_SS_REF_CLK	SYS_CLK1	OSC0
USB_PHY1_CORE	USB2PHY1_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC0
USB_PHY2_CORE	USB2PHY2_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC0
USB_PHY3_CORE	USB3PHY_WKUP_CLK	Func	0.032	COREAON_32K_GFCLK	SYS_CLK1/610	OSC0
VIP1	L3_CLK_PROC_CLK	Int & Func	266	VIP1_GCLK	CORE_X2_CLK	DPLL_CORE
					CORE_ISS_MAIN_CLK	DPLL_CORE
VIP2	L3_CLK_PROC_CLK	Int & Func	266	VIP2_GCLK	CORE_X2_CLK	DPLL_CORE
					CORE_ISS_MAIN_CLK	DPLL_CORE
VPE	L3_CLK_PROC_CLK	Int & Func	300	VPE_GCLK	CORE_ISS_MAIN_CLK	DPLL_CORE
					VIDEO1_CLKOUT4	DPLL_VIDEO1
WD_TIMER1	PIOCPCLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	PITIMERCLK	Func	0.032	OSC_32K_CLK	RC_CLK	OSC0[(1)]
WD_TIMER2	WD_TIMER2_ICLK	Int	38.4	WKUPAON_GICLK	SYS_CLK1	OSC0
					DPLL_ABE_X2_CLK	DPLL_ABE
	WD_TIMER2_FCLK	Func	0.032	WKUPAON_SYS_GFCLK	WKUPAON_32K_GFCLK	OSC0[(1)]

(1) RTC oscillator can be used as an optional clock source intead of OSC1.

5.6 Power Consumption Summary

NOTE

Maximum power consumption for this SoC depends on the specific use conditions for the end system. Contact your TI representative for assistance in estimating maximum power consumption for the end system use case.

5.7 Electrical Characteristics

NOTE

The data specified in through Section 5.7.4 are subject to change.

NOTE

The interfaces or signals described in through Section 5.7.4 correspond to the interfaces or signals available in multiplexing mode 0 (Function 1).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

Table 5-6. LVCMOS DDR DC Electrical Characteristics[3]

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0 (Single-Ended Signals): ddr1_d[31:0], ddr1_a[15:0], ddr1_dqm[3:0], ddr1_ba[2:0], ddr1_csn[0], ddr1_cke, ddr1_odt[0], ddr1_casn, ddr1_rasn, ddr1_wen, ddr1_rst, ddr1_ecc_d[7:0], ddr1_dqm_ecc, ddr2_d[31:0], ddr2_a[15:0], ddr2_dqm[3:0], ddr2_ba[2:0], ddr2_csn[0], ddr2_cke, ddr2_odt[0], ddr2_casn, ddr2_rasn, ddr2_wen, ddr2_rst;						
Balls: AA28 / AA25 / AA26 / Y24 / AA24 / Y23 / Y22 / AA23 / Y20 / AB27 / Y19 / AC27 / AC28 / AB28 / W20 / V20 / AD25 / AC24 / AC25 / AE26 / AF28 / AG27 / AF27 / AC23 / AE23 / AF23 / AE24 / AF24 / AH26 / AG26 / AF26 / AF25 / AD18 / AE17 / AF18 / AC21 / AD22 / AD21 / AE22 / AF22 / AE21 / AE21 / AH22 / AF21 / AB19 / AC20 / AC19 / AD20 / AA27 / AC26 / AB23 / AD23 / AB18 / AE18 / AF17 / AH23 / AG22 / AE20 / AC18 / AF20 / AH21 / AG21 / Y26 / V25 / V24 / Y25 / W23 / W19 / V23 / W22 / V26 / M26 / M25 / M24 / M23 / L28 / L25 / L26 / L27 / J20 / K22 / J23 / L24 / L23 / K21 / K20 / L22 / J24 / J26 / J25 / G26 / H26 / H24 / H25 / H23 / E28 / E27 / F27 / F26 / F24 / F25 / G25 / E26 / U22 / R22 / T22 / N28 / P26 / N23 / N27 / P27 / N20 / P25 / P22 / P23 / R27 / R28 / R26 / R25 / M22 / K23 / G24 / F28 / U26 / U27 / U23 / P24 / U24 / R23 / U28 / T23 / U25 / R24;						
Driver Mode						
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9 × VDDS			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)				0.1 × VDDS	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)		80		Ω
		I[2:0] = 001 (Imp60)		60		
		I[2:0] = 010 (Imp48)		48		
		I[2:0] = 011 (Imp40)		40		
		I[2:0] = 100 (Imp34)		34		
Single-Ended Receiver Mode						
V_{IH}	High-level input threshold	DDR3/DDR3L	VREF + 0.1		VDDS + 0.2	V
		DDR2	VREF + 0.125		VDDS + 0.3	

Table 5-6. LVCMOS DDR DC Electrical Characteristics[3] (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{IL}	Low-level input threshold	DDR3/DDR3L	-0.2		VREF-0.1	V
		DDR2	-0.3		VREF-0.125	
V_{CM}	Input common-mode voltage		VREF - 10%VDDS		VREF + 10%VDDS	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Signal Names in MUXMODE 0 (Differential Signals): ddr1_dqs[3:0], ddr1_dqsn[3:0], ddr1_ck, ddr1_nck, ddr2_dqs[3:0], ddr2_dqsn[3:0], ddr2_ck, ddr2_nck, ddr1_dqs_ecc, ddr1_dqsn_ecc						
Bottom Balls: Y28 / AD27 / AE27 / AH25 / Y27 / AD28 / AE28 / AG25 / AG24 / AH24 / M28 / K27 / H27 / G28 / M27 / K28 / H28 / G27 / T28 / T27 / V27 / V28						
Driver Mode						
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9 × VDDS[1]			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)				0.1 × VDDS[1]	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)		80		Ω
		I[2:0] = 001 (Imp60)		60		
		I[2:0] = 010 (Imp48)		48		
		I[2:0] = 011 (Imp40)		40		
		I[2:0] = 100 (Imp34)		34		
Single-Ended Receiver Mode						
V_{IH}	High-level input threshold	DDR3/DDR3L	VREF[2] + 0.1		VDDS[1] + 0.2	V
		DDR2	VREF[2] + 0.125		VDDS[1] + 0.3	
V_{IL}	Low-level input threshold	DDR3/DDR3L	-0.2		VREF[2]-0.1	V
		DDR2	-0.3		VREF[2]-0.125	
V_{CM}	Input common-mode voltage		VREF[2] - 10%VDDS[1]		VREF[2] + 10%VDDS[1]	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Differential Receiver Mode						
V_{SWING}	Input voltage swing	DDR3/DDR3L	0.2		VDDS + 0.4	V
		DDR2	0.25		VDDS + 0.6	
V_{CM}	Input common-mode voltage		VREF[2] - 10%VDDS[1]		VREF[2] + 10%VDDS[1]	
C_{PAD}	Pad capacitance (including package capacitance)				3	pF

(1) VDDS in this table stands for corresponding power supply (i.e. vdds_ddr1 or vdds_ddr2). For more information on the power supply name and the corresponding ball, see Table 4-1, POWER [11] column.

(2) VREF in this table stands for corresponding Reference Power Supply (i.e. ddr1_vref0 or ddr2_vref0). For more information on the power supply name and the corresponding ball, see Table 4-1, POWER [11] column.

(3) For more information on the I/O cell configurations (i[2:0], sr[1:0]), see chapter Control Module of the Device TRM.

Table 5-7. Dual Voltage LVCMOS I2C DC Electrical Characteristics[2]

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: i2c1_sda, i2c1_scl, i2c2_sda, i2c2_scl;				
Balls: F17 / C20 / C21 / C25				
I^2C Standard Mode – 1.8 V				

Table 5-7. Dual Voltage LVCMOS I2C DC Electrical Characteristics(2) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{IH}	Input high-level threshold	0.7 × VDDS(1)			V
V_{IL}	Input low-level threshold			0.3 × VDDS(1)	V
V_{hys}	Hysteresis	0.1 × VDDS(1)			V
I_{IN}	Input current at each I/O pin with an input voltage between 0.1 × VDDS to 0.9 × VDDS			12	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			12	µA
C_{IN}	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.2 × VDDS(1)	V
I_{OLmin}	Low-level output current @V_{OL} = 0.2 × VDDS	3			mA
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 5 pF to 400 pF			250	ns
I^2C Fast Mode – 1.8 V					
V_{IH}	Input high-level threshold	0.7 × VDDS(1)			V
V_{IL}	Input low-level threshold			0.3 × VDDS(1)	V
V_{hys}	Hysteresis	0.1 × VDDS(1)			V
I_{IN}	Input current at each I/O pin with an input voltage between 0.1 × VDDS to 0.9 × VDDS			12	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			12	µA
C_{IN}	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.2 × VDDS(1)	V
I_{OLmin}	Low-level output current @V_{OL} = 0.2 × VDDS	3			mA
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 10 pF to 400 pF	20 + 0.1 × C_B		250	ns
I^2C Standard Mode – 3.3 V					
V_{IH}	Input high-level threshold	0.7 × VDDS(1)			V
V_{IL}	Input low-level threshold			0.3 × VDDS(1)	V
V_{hys}	Hysteresis	0.05 × VDDS(1)			V
I_{IN}	Input current at each I/O pin with an input voltage between 0.1 × VDDS to 0.9 × VDDS	31		80	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}	31		80	µA
C_{IN}	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.4	V
I_{OLmin}	Low-level output current @V_{OL} = 0.4 V	3			mA
I_{OLmin}	Low-level output current @V_{OL} = 0.6 V for full drive load (400 pF / 400 kHz)	6			mA
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 5 pF to 400 pF			250	ns
I^2C Fast Mode – 3.3 V					

Table 5-7. Dual Voltage LVCMOS I2C DC Electrical Characteristics[(2)] (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{IH}	Input high-level threshold	0.7 × VDDS[(1)]			V
V_{IL}	Input low-level threshold			0.3 × VDDS[(1)]	V
V_{hys}	Hysteresis	0.05 × VDDS[(1)]			V
I_{IN}	Input current at each I/O pin with an input voltage between 0.1 × VDDS to 0.9 × VDDSS	31		80	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}	31		80	µA
C_{IN}	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current			0.4	V
I_{OLmin}	Low-level output current @V_{OL} = 0.4 V	3			mA
I_{OLmin}	Low-level output current @V_{OL} = 0.6 V for full drive load (400 pF/400 kHz)	6			mA
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 10 pF to 200 pF (Proper External Resistor Value should be used as per I2C spec)	20 + 0.1 × C_B		250	ns
	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 300 pF to 400 pF (Proper External Resistor Value should be used as per I2C spec)	40		290	

(1) VDDS in this table stands for corresponding power supply (i.e. vddshv3). For more information on the power supply name and the corresponding ball, see Table 4-1, POWER [11] column.

(2) For more information on the I/O cell configurations, see the Control Module section of the Device TRM.

Table 5-8. IQ1833 Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: tclk;					
Balls: E20;					
1.8-V Mode					
V_{IH}	Input high-level threshold (Does not meet JEDEC V_{IH})	0.75 × VDDS			V
V_{IL}	Input low-level threshold (Does not meet JEDEC V_{IL})			0.25 × VDDS	V
V_{HYS}	Input hysteresis voltage	100			mV
I_{IN}	Input current at each I/O pin	2		11	µA
C_{PAD}	Pad capacitance (including package capacitance)			1	pF
3.3-V Mode					
V_{IH}	Input high-level threshold (Does not meet JEDEC V_{IH})	2.0			V
V_{IL}	Input low-level threshold (Does not meet JEDEC V_{IL})			0.6	V
V_{HYS}	Input hysteresis voltage	400			mV
I_{IN}	Input current at each I/O pin	5		11	µA
C_{PAD}	Pad capacitance (including package capacitance)			1	pF

(1) VDDS in this table stands for corresponding power supply (i.e. vddshv3). For more information on the power supply name and the corresponding ball, see Table 4-1, POWER [11] column.

Table 5-9. IHHV1833 Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: porz / rtc_iso / rtc_porz / wakeup [3:0];					
Balls: F22 / AF14 / AB17 / AD17 / AC17 / AB16 / AC16;					
1.8-V Mode					
V_{IH}	Input high-level threshold	1.2			V
V_{IL}	Input low-level threshold			0.4	V
V_{HYS}	Input hysteresis voltage	40			mV
I_{IN}	Input current at each I/O pin	0.02		1	µA
C_{PAD}	Pad capacitance (including package capacitance)			1	pF
3.3-V Mode					
V_{IH}	Input high-level threshold	1.2			V
V_{IL}	Input low-level threshold			0.4	V
V_{HYS}	Input hysteresis voltage	40			mV
I_{IN}	Input current at each I/O pin	5		8	µA
C_{PAD}	Pad capacitance (including package capacitance)			1	pF

Table 5-10. LVCMOS OSC Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: rtc_osc_xi_clkin32 / rtc_osc_xo;					
Balls: AE14 / AD14;					
1.8-V Mode					
V_{IH}	Input high-level threshold	0.65 × VDDS			V
V_{IL}	Input low-level threshold			0.35 × VDDS	V
V_{HYS}	Input hysteresis voltage	150			mV
C_{PAD}	Pad capacitance (including package capacitance)			3	pF

(1) VDDS in this table stands for corresponding power supply (i.e. vdda_rtc). For more information on the power supply name and the corresponding ball, see Table 4-1, POWER [11] column.

Table 5-11. BC1833IHHV Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in MUXMODE 0: on_off;					
Balls: Y11;					
1.8-V Mode					
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)	VDDS(1) - 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)			0.45	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45 V or VDDS - 0.45 V	6			mA
I_{IN}	Input current at each I/O pin	6		12	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			6	µA
C_{PAD}	Pad capacitance (including package capacitance)			4	pF
3.3-V Mode					
V_{OH}	Output high-level threshold (I_{OH} = 100 µA)	VDDS(1) - 0.2			V

Table 5-11. BC1833IHHV Buffers DC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{OL}	Output low-level threshold (I_{OL} = 100 µA)			0.2	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45 V or VDDS - 0.45 V	6			mA
I_{IN}	Input current at each I/O pin			60	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			60	µA
C_{PAD}	Pad capacitance (including package capacitance)			4	pF

(1) VDDS in this table stands for corresponding power supply (i.e. vddshv5). For more information on the power supply name and the corresponding ball, see Table 4-1, POWER [11] column.

Table 5-12. Dual Voltage SDIO1833 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in Mode 0: mmc1_clk, mmc1_cmd, mmc1_data[3:0]					
Bottom Balls: W6 / Y6 / AA6 / Y4 / AA5 / Y3					
1.8-V Mode					
V_{IH}	Input high-level threshold	1.27			V
V_{IL}	Input low-level threshold			0.58	V
V_{HYS}	Input hysteresis voltage	50 (2)			mV
I_{IN}	Input current at each I/O pin			30	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as I_{OZ} .			30	µA
I_{IN} with pulldown enabled	Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS	50	120	210	µA
I_{IN} with pullup enabled	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	60	120	200	µA
C_{PAD}	Pad capacitance (including package capacitance)			5	pF
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)	1.4			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)			0.45	V
3.3-V Mode					
V_{IH}	Input high-level threshold	0.625 × VDDS(1)			V
V_{IL}	Input low-level threshold			0.25 × VDDS(1)	V
V_{HYS}	Input hysteresis voltage	40 (2)			mV
I_{IN}	Input current at each I/O pin			110	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max(I(PAD)) is measured and is reported as I_{OZ} .			110	µA
I_{IN} with pulldown enabled	Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS	40	100	290	µA
I_{IN} with pullup enabled	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	10	100	290	µA
C_{PAD}	Pad capacitance (including package capacitance)			5	pF

Table 5-12. Dual Voltage SDIO1833 DC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)	0.75 × VDDS(1)			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)			0.125 × VDDS(1)	V

(1) VDDS in this table stands for corresponding power supply (i.e. vddshv8). For more information on the power supply name and the corresponding ball, see Table 4-1, POWER [11] column.

(2) Hysteresis is enabled/disabled with CTRL_CORE_CONTROL_HYST_1.SDCARD_HYST register.

Table 5-13. Dual Voltage LVCMOS DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
1.8-V Mode					
V_{IH}	Input high-level threshold	0.65 × VDDS			V
V_{IL}	Input low-level threshold			0.35 × VDDS	V
V_{HYS}	Input hysteresis voltage	100			mV
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)	VDDS - 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)			0.45	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45 V or VDDS - 0.45 V	6			mA
I_{IN}	Input current at each I/O pin			16	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			16	µA
$I_{IN\ with\ pulldown\ enabled}$	Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS	50	120	210	µA
$I_{IN\ with\ pullup\ enabled}$	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	60	120	200	µA
C_{PAD}	Pad capacitance (including package capacitance)			4	pF
Z_O	Output impedance (drive strength)		40		Ω
3.3-V Mode					
V_{IH}	Input high-level threshold	2			V
V_{IL}	Input low-level threshold			0.8	V
V_{HYS}	Input hysteresis voltage	200			mV
V_{OH}	Output high-level threshold (I_{OH} = 100 µA)	VDDS - 0.2			V
V_{OL}	Output low-level threshold (I_{OL} = 100 µA)			0.2	V
I_{DRIVE}	Pin Drive strength at PAD Voltage = 0.45 V or VDDS - 0.45 V	6			mA
I_{IN}	Input current at each I/O pin			65	µA
I_{OZ}	I_{OZ}(I_{PAD} Current) for BIDI cell. This current is contributed by the tristated driver leakage + input current of the Rx + weak pullup/pulldown leakage. PAD is swept from 0 to VDDS and the Max($I_{(PAD)}$) is measured and is reported as I_{OZ}			65	µA
$I_{IN\ with\ pulldown\ enabled}$	Input current at each I/O pin with weak pulldown enabled measured when PAD = VDDS	40	100	200	µA
$I_{IN\ with\ pullup\ enabled}$	Input current at each I/O pin with weak pullup enabled measured when PAD = 0	10	100	290	µA
C_{PAD}	Pad capacitance (including package capacitance)			4	pF
Z_O	Output impedance (drive strength)		40		Ω

Table 5-13. Dual Voltage LVCMOS DC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

(1) VDDS in this table stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see Table 4-1, POWER [11] column.

5.7.1 HDMIPHY DC Electrical Characteristics

The HDMIPHY DC Electrical Characteristics are compliant with the HDMI 1.4a specification and are not reproduced here.

5.7.2 SATAPHY DC Electrical Characteristics

NOTE

The SATA module is compliant with the electrical parameters specified in the *SATA-IO SATA Specification*, Revision 3.2, August 7, 2013.

5.7.3 USBPHY DC Electrical Characteristics

NOTE

USB1 instance is compliant with the USB3.0 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the USB3.0 Specification Rev 1.0 dated Jun 6, 2011.

NOTE

USB1 and USB2 Electrical Characteristics are compliant with USB2.0 Specification Rev 2.0 dated April 27, 2000 including ECNs and Errata as applicable.

5.7.4 PCIEPHY DC Electrical Characteristics

NOTE

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 3.0.

5.8 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

Table 5-14. Recommended Operating Conditions for OTP eFuse Programming

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
vdd_core	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)	1.11	1.15	1.2	V
vpp	Supply voltage range for the eFuse ROM domain during normal operation		NC		V
	Supply voltage range for the eFuse ROM domain during OTP programming(1)(2)		1.8		V
I(vpp)				100	mA
Tj	Temperature (junction)	0	25	85	ºC

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions TLV70018-Q1 from the TLV700xx family meet the supply voltage range needed for vpp.

Recommended Operating Conditions for OTP eFuse Programming *(continued)*

over operating free-air temperature range (unless otherwise noted)

(2) During normal operation, no voltage should be applied to vpp. This can be typically achieved by disabling the regulator attached to the vpp terminal. For more details, see TLV700xx-Q1 300-mA, Low-IQ, Low-Dropout Regulator.

5.8.1 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The vpp power supply must be disabled when not programming OTP registers.
- The vpp power supply must be ramped up after the proper device power-up sequence (for more details, see Section 5.10.3).

5.8.2 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the vpp terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the vpp terminal according to the specification in Table 5-14.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the vpp terminal.

5.8.3 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

5.9 Thermal Resistance Characteristics

For reliability and operability concerns, the maximum junction temperature of the Device has to be at or below the T_J value identified in , *Recommended Operating Conditions*.

A BCI compact thermal model for this Device is available and recommended for use when modeling thermal performance in a system.

Therefore, it is recommended to perform thermal simulations at the system level with the worst case device power consumption.

5.9.1 Package Thermal Characteristics

Table 5-15 provides the thermal resistance characteristics for the package used on this device.

NOTE

Power dissipation of 1.5 W and an ambient temperature of 85ºC is assumed for ABZ package.

Table 5-15. Thermal Resistance Characteristics

NO.	PARAMETER	DESCRIPTION	°C/W[(1) (3)]	AIR FLOW (m/s)[(2)]
T1	$R\Theta_{JC}$	Junction-to-case	0.16	N/A
T2	$R\Theta_{JB}$	Junction-to-board	3.12	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	13.02	0
T4		Junction-to-moving air	7.71	1
T5			6.76	2
T6			6.24	3
T7	Ψ_{JT}	Junction-to-package top	0.09	0
T8			0.09	1
T9			0.09	2
T10			0.09	3
T11	Ψ_{JB}	Junction-to-board	2.88	0
T12			2.74	1
T13			2.67	2
T14			2.61	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

– JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
– JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
– JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
– JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
– JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.

(3) °C/W = degrees Celsius per watt.

5.10 Timing Requirements and Switching Characteristics

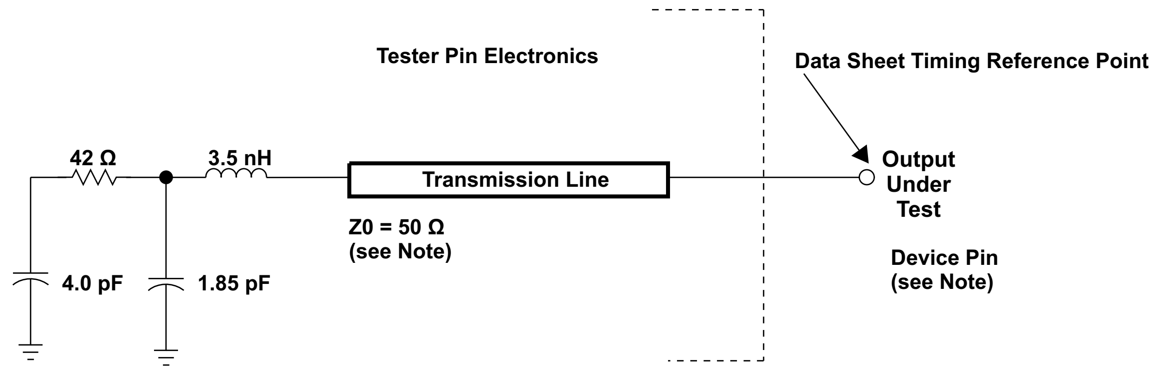
5.10.1 Timing Parameters and Information

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

Table 5-16. Timing Parameters

SUBSCRIPTS	
SYMBOL	**PARAMETER**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

5.10.1.1 Parameter Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

pm_tstcirc_prs403

Figure 5-2. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals.

This load capacitance value does not indicate the maximum load the device is capable of driving.

5.10.1.1.1 1.8V and 3.3V Signal Transition Levels

All input and output timing parameters are referenced to V_{ref} for both "0" and "1" logic levels. V_{ref} = (VDD I/O)/2.

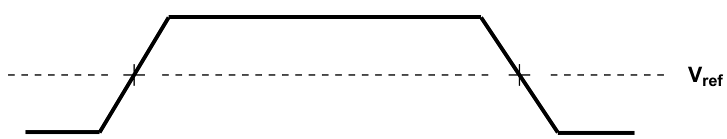


Figure 5-3. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

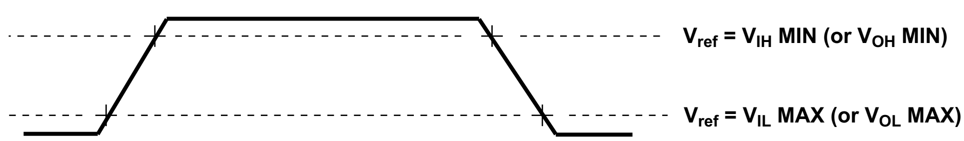


Figure 5-4. Rise and Fall Transition Time Voltage Reference Levels

5.10.1.1.2 1.8V and 3.3V Signal Transition Rates

The default SLEWCONTROL settings in each pad configuration register must be used to guarantee timings, unless specific instructions otherwise are given in the individual timing subsections of the datasheet.

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

5.10.1.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this Data Manual do not include delays by board routes. As a good board design practice, such delays must always be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends using the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

5.10.2 Interface Clock Specifications

5.10.2.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

5.10.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the Device IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and the Device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

5.10.3 Power Supply Sequences

This section describes the power-up and power-down sequence required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules. Refer to Section 4.2, *Pin Attributes* for a specific device to determine which power supplies are applicable.

NOTE

For more information, see Power, Reset and Clock Management / Reset Management Functional Description / Reset Sequences of the Device TRM.

Figure 5-5 and Figure 5-6, describes the device power sequencing.

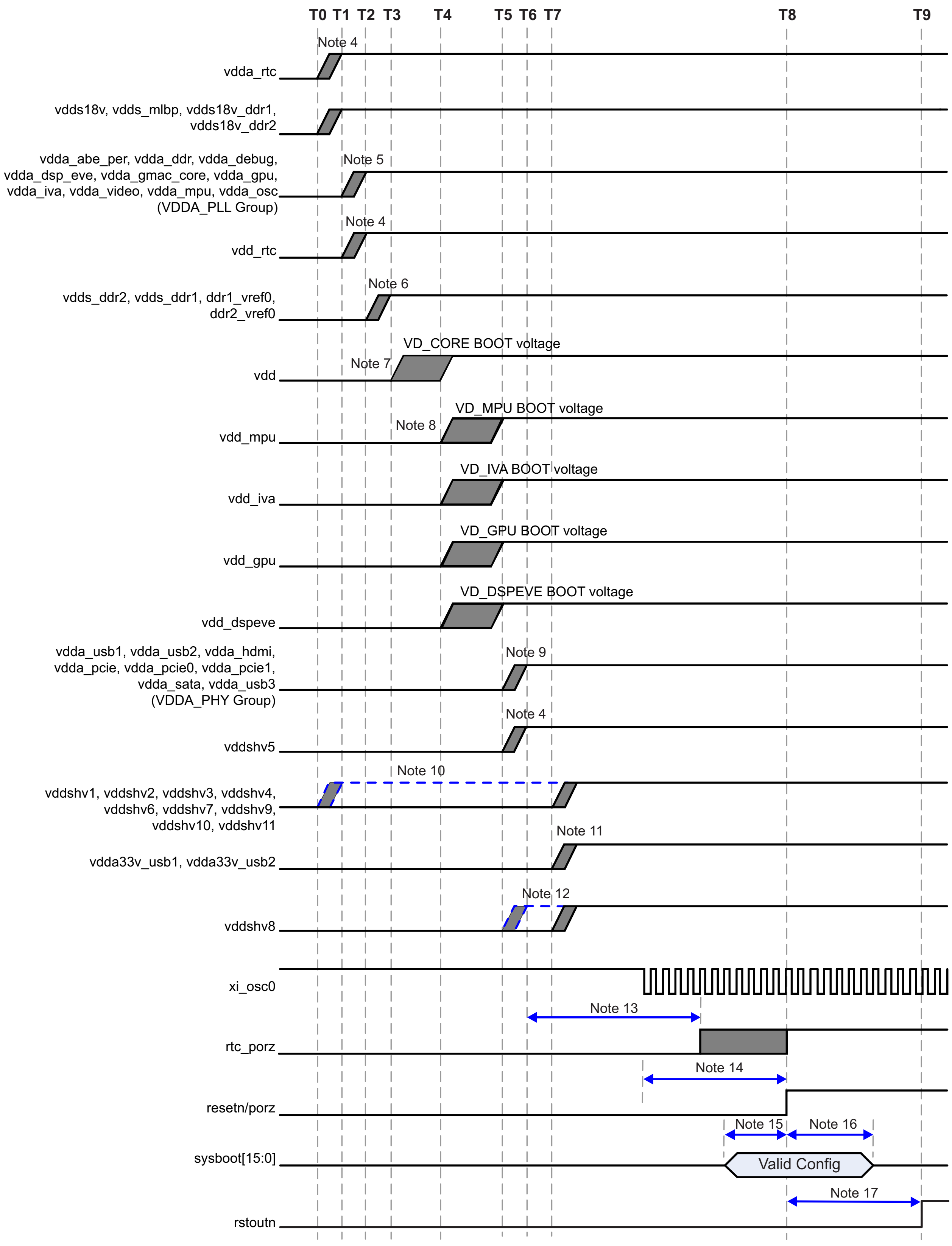


Figure 5-5. Recommended Power-Up Sequencing

(1) Time stamps:

– T0 = 0 ms; T1 = 0.55 ms; T2 = 1.1 ms; T3 = 1.65 ms; T4 = 2.2 ms; T5 = 2.75 ms; T6 = 3.3 ms; T7 = 5.85 ms; T8 = 6.4 ms; T9 = 8.4

ms. All “Tn” markers show total elapsed time from T0.

(2) Terminology:
- $V_{OPR\ MIN}$ = Minimum Operational Voltage level that ensures device functionality and specified performance per Section 5.4, *Recommended Operating Conditions*.
- Ramp Up = transition time from V_{OFF} to $V_{OPR\ MIN}$.

(3) General timing diagram items:
- Grey shaded areas show valid transition times for supplies between $V_{OPR\ MIN}$ and V_{OFF}.
- Dashed horizontal lines are not valid ramp times but show alternate transition times based upon common sources and clarified in associated note.
- Dashed vertical lines show approximate elapse times based upon TI recommended PMIC power sequencer circuit performance.

(4) vddshv5, vdd_rtc, and vdda_rtc domains:
- If RTC mode is used, then vdda_rtc, vdd_rtc and vddshv5 must be individually powered with separate power supplies and cannot be combined with other rails.
- If RTC-mode is not supported then the following combinations are approved:
  - vdda_rtc can be combined with vdds18v
  - vdd_rtc can be combined with vdd
  - vddshv5 can be combined with other 1.8 V or 3.3 V vddshvn rails

  If combinations listed above are not followed then sequencing for these 3 voltage rails should follow the RTC mode timing requirements.

(5) vdda_* rails should not be combined with vdds18v_* for best performance to avoid transient switching noise impacts on analog domains. vdda_* should not ramp-up before vdds18v_* but could ramp concurrently if design ensures final operational voltage will not be reached until after vdds18v. The preferred sequence is to follow all vdds18v_* to ensure circuit components and PCB design do not cause an inadvertent violation.

(6) vdds_ddr* should not ramp-up before vdds18v_*. The preferred sequence has vdds_ddr1 following vdds18v_* to ensure circuit components and PCB design do not cause an inadvertent violation. vdds_ddr1 can ramp-up before, concurrently or after vdda_*, there are no dependencies between vdds_ddr1 and vdda_* domains.

(7) vdd should not ramp-up before vdds18v_* or vdds_ddr* domains have reached $V_{OPR\ MIN}$.

(8) vdd_mpu, vdd_iva, vdd_gpu, vdd_dspeve domains should follow vdd core supply as preferred sequence. If vdd_mpu, vdd_iva, vdd_gpu, vdd_dspeve domains ramp concurrently or quicker than vdd core, then vdd core must remain at least 150 mV greater than vdd_mpu, vdd_iva, vdd_gpu, vdd_dspeve domains during ramp. Circuit design (components and PCB) must ensure vdd reaches final operational voltage before any of the vdd_mpu, vdd_iva, vdd_gpu, vdd_dspeve domains.

(9) VDDA_PHY group should not be combined with VDDA_PLL group to avoid transient switching noise impacts.

(10) vddshv[1-4, 6, 7, 9-11] domains:
- If 1.8 V I/O signaling is needed, then 1.8 V must be sourced from common vdds18v supply and ramp up concurrently with vdds18v.
- If 3.3 V I/O signaling is needed, then 3.3 V vddshvx rails must ramp up after vdd_mpu, vdd_iva, vdd_gpu, vdd_dspeve, and VDDA_PHY group domains.

(11) vdda33v_usb[1-2] domain:
- If USB1 and USB2 interfaces are used, should be supplied from independent analog supply.
- If USB1/USB2 interface is not used, could be connected to VSS/GND if both conditions are met:
  - USB1/USB2 diff pair (usb1_dm/usb1_dp; usb2_dm/usb2_dp) pins are left unconnected
  - vdda_usb1 and/or vdda_usb2 PHY is not energized

(12) vddshv8 shows two ramp up options for 1.8 V I/O or 3.3 V I/O or SD Card operation:
- If 1.8 V I/O signaling is needed, then vddshv8 must ramp up after vdd and before or concurrently with 3.3 V vddshv* rails.
- If 3.3 V I/O signaling is needed, then vddshv8 must be combined with other 3.3 V vddshv* rails.
- If SD Card operation is needed, then vddshv8 must be sourced from a dual voltage (3.3 V / 1.8 V) power source per SDIO specifications and ramp up concurrently with 3.3 V vddshv* rails.

(13) Pulse duration: rtc_porz must remain low 1ms after vdda_rtc, vddshv5, and vdd_rtc are ramped and stable or can be de-asserted before but no later than porz. The FUNK_32K_CLK source must be stable and at a valid frequency 1 ms prior to de-asserting rtc_porz high.

(14) porz must remain asserted low until both of the following conditions are met:
- Minimum of 12 × P, where P = 1 / (SYS_CLK1 / 610), units in ns.
- All device supply rails reach stable operational levels.

(15) Setup time: sysboot[15:0] pins must be valid 2P[14] before porz is de-asserted high.

(16) Hold time: sysboot[15:0] pins must be valid 15P[14] after porz is de-asserted high.

(17) rstoutn will be set high after global reset, due to porz, is de-asserted following an internal 2 ms delay. rstoutn is only valid after vddshv3 reaches an operational level. If used as a peripheral component reset, it should be AND gated with porz to avoid possible reset glitches during power up.

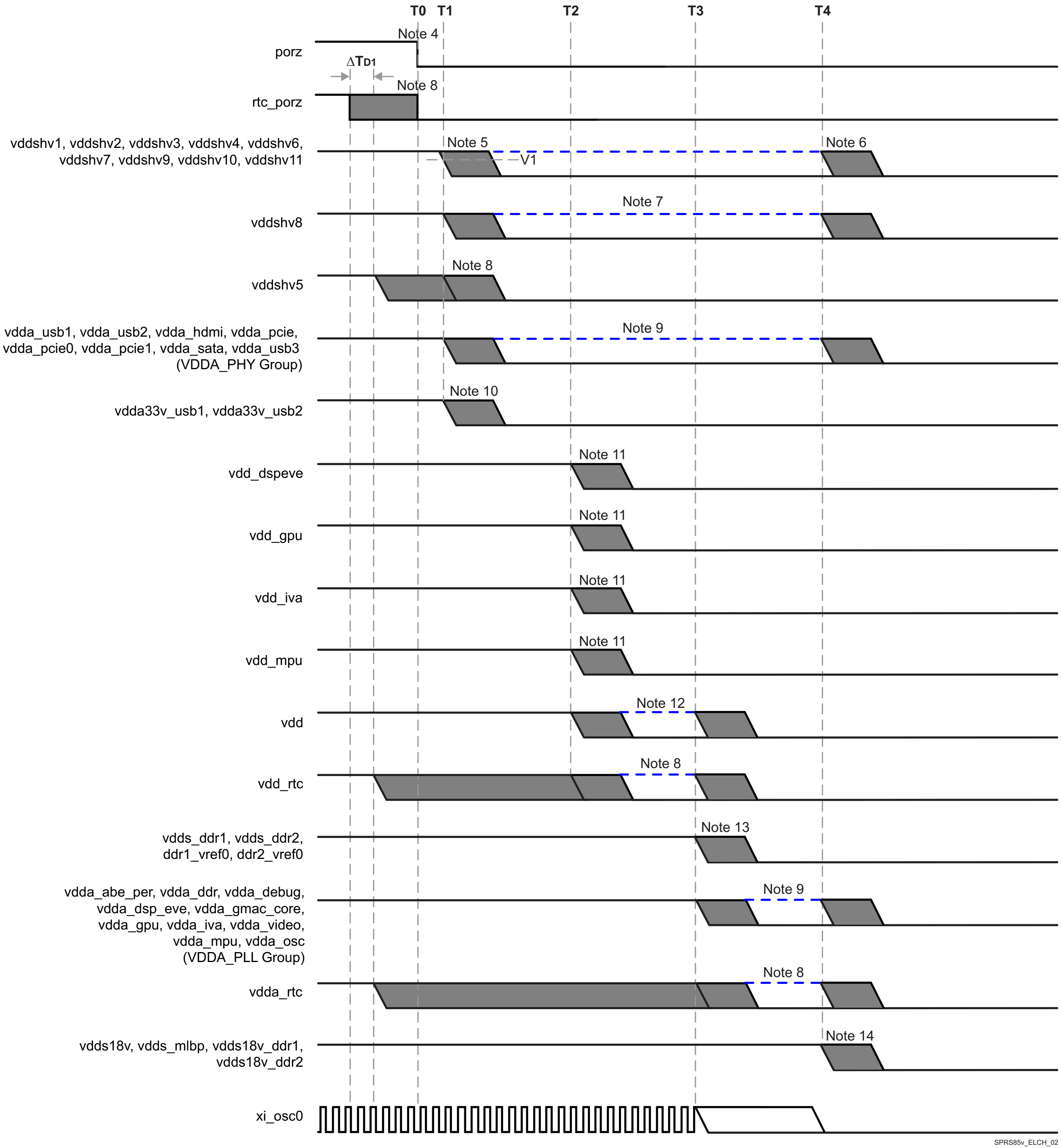


Figure 5-6. Recommended Power-Down Sequencing

(1) Time stamps:

– T0 = 0 ms, T1 > 100 µs, T2 = 0.5 ms, T3 = 1.0 ms, T4 = 1.5 ms; V1 = 2.7 V. All "Tn" markers are intended to show elapsed times from T0. Delta time: ΔT_{D1} > 100 µs.

(2) Terminology:

– $V_{OPR\ MIN}$ = Minimum Operational Voltage level that ensures device functionality and specified performance per Section 5.4, *Recommended Operating Conditions*.
– V_{OFF} = OFF Voltage level is defined to be less than 0.6 V where any current draw has no impact to POH.
– Ramp Down = transition time from $V_{OPR\ MIN}$ to V_{OFF} and is slew rate independent.

(3) General timing diagram items:

- Grey shaded areas show valid transition times for supplies between $V_{OPR\ MIN}$ and V_{OFF}.
- Dashed horizontal lines are not valid ramp times but show alternate transition times based upon common sources and clarified in associated note.
- Dashed vertical lines show approximate elapse times based upon TI recommended PMIC power-down sequencer circuit performance.

(4) porz signals must be asserted low for 100 µs min to ensure SoC is set to a safe functional state before any voltage begins to ramp down.

(5) vddshv* domains supplied by 3.3 V:

- must remain greater than 2.7 V to enable Dual Voltage GPIO selector circuit operation for 100 µs min after porz is asserted low.
- must be in first group of supplies ramping down after porz has been asserted low for 100 µs min.
- must not exceed vdds18v by more than 2 V during ramp down, see Figure 5-10 "vdds18v and vdda_* Discharge Relationship".

(6) vddshv* domains supplied by 1.8 V:

- must ramp down concurrently with vdds18v and be sourced from the same vdds18v supply.

(7) vddshv8 domain:

- must be in first group of supplies to ramp down after porz has been asserted low for 100 µs min.
- if SDIO operation is needed, must be sourced from independent power resource that can provide dual voltage (3.3 V / 1.8 V) operation as required to be compliant to SDIO specification
- if SDIO operation is not needed, must be grouped and ramped down with other vddshv* domains as noted above.

(8) RTC domains (vddshv5, vdd_rtc, and vdda_rtc):

- If RTC mode is used:
  - rtc_porz can be asserted low before porz and RTC domains can be ramped down after 100 µs elapsed time.
  - must be sourced from independent supplies and must not be combined with other rails.
  - timing diagram shows this mode of operation.
- If RTC mode is not used, then:
  - rtc_porz must be connected to porz signal.
  - vddshv5 must be grouped and ramped down with other vddshv* domains as noted above.
  - vdd_rtc must be grouped and ramped down with vdd.
  - vdda_rtc must be grouped and ramped down with either VDDA_PHY group or vdds18v.

(9) vdda_* domains:

- should not be combined with vdds18v for best performance to avoid transient switching noise impacts on analog domains.
- can ramp down before or concurrently with vdds18v.
- must satisfy the vdds18v and vdda_* Discharge Relationship (see Figure 5-10) if vdda_* disable point is later or discharge rate is slower than vdds18v.
- can ramp down before, concurrently or after vdds_ddr*, there is no dependency between these supplies.

(10) vdda33v_usb* domains:

- can start ramping down 100 µs after low assertion of porz
- can ramp down concurrently or before VDDA_PHY group

(11) vdd_dspeve, vdd_gpu, vdd_iva, vdd_mpu domains can ramp down before or concurrently with vdd.

(12) vdd can ramp down concurrently or after with vdd_dspeve, vdd_gpu, vdd_iva, vdd_mpu domains.

(13) vdds_ddr* domains:

- should ramp down after vdd begins ramping down.

(14) vdds18v domain:

- should maintain $V_{OPR\ MIN}$ (V_{NOM} -5% = 1.71 V) until all other supplies start to ramp down.
- must satisfy the vdds18v versus vddshv[1-7, 9-11] Discharge Relationship (see Figure 5-8) if vddshv* is operating at 3.3 V
- must satisfy the vdds18v and vdds_ddr* Discharge Relationship (see Figure 5-9) if vdds_ddr* discharge rate is slower than vdds18v.

Figure 5-7 describes the RTC-mode power sequencing.

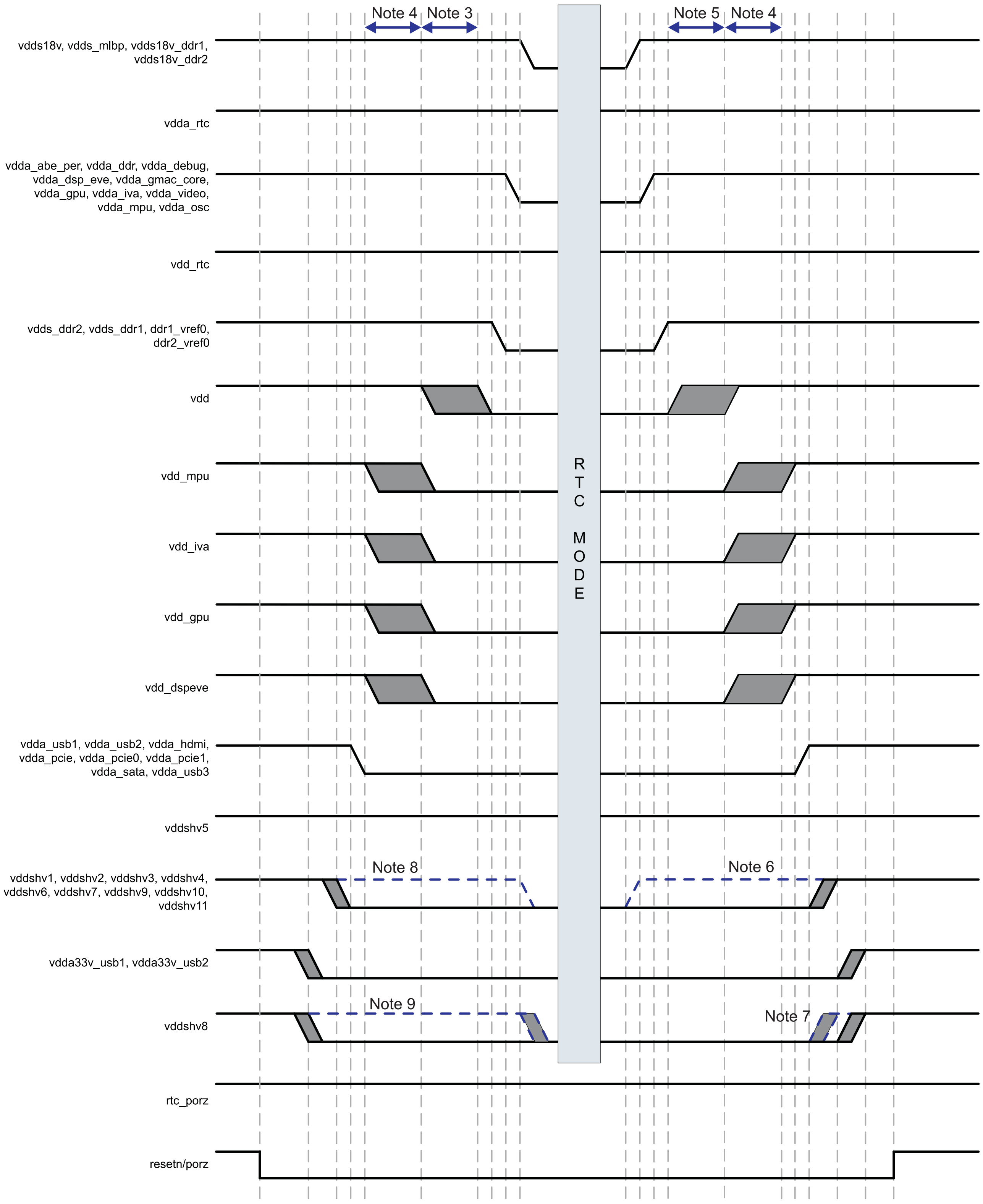


Figure 5-7. RTC Mode Sequencing

(1) Grey shaded areas are windows where it is valid to ramp the voltage rail.

(2) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.

(3) vdd must ramp down after or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.

(4) vdd_mpu, vdd_gpu, vdd_dspeve, vdd_iva can be ramped at the same time or can be staggered.

(5) vdd must ramp up before or at the same time as vdd_mpu, vdd_gpu, vdd_dspeve and vdd_iva.

(6) If any of the vddshv[1-7,9-11] rails (not including vddshv8) are used as 1.8 V only, then these rails can be combined with vdds18v.

(7) vddshv8 is separated out to show support for dual voltage. If single voltage is used then vddshv8 can be combined with other vddshvn rails but vddshv8 must ramp down before vdd and must ramp up after vdd.

(8) If any of the vddshv[1-7,9-11] rails (not including vddshv8) are used as 1.8 V only, then these rails can be combined with vdds18v. vddshv[1-7,9-11] is allowed to ramp down at either of the two points shown in the timing diagram in either 1.8 V mode or in 3.3 V mode. If vddshv[1-7,9-11] ramps down at the later time in the diagram then the board design must guarantee that the vddshvn rail is never higher than 2.0 V above the vdds18v rail.

(9) vddshv8 is separated out to show support for dual voltage. If a dedicated LDO/supply source is used for vddshv8, then vddshv8 ramp down should occur at one of the two earliest points in the timing diagram. If vddshv8 is powered by the same supply source as the other vddshvn rails, then it is allowed to ramp down at either of the last two points in the timing diagram.

Figure 5-8 describes vddshv[1-7,9-11] supplies falling before vdds18v supplies delta.

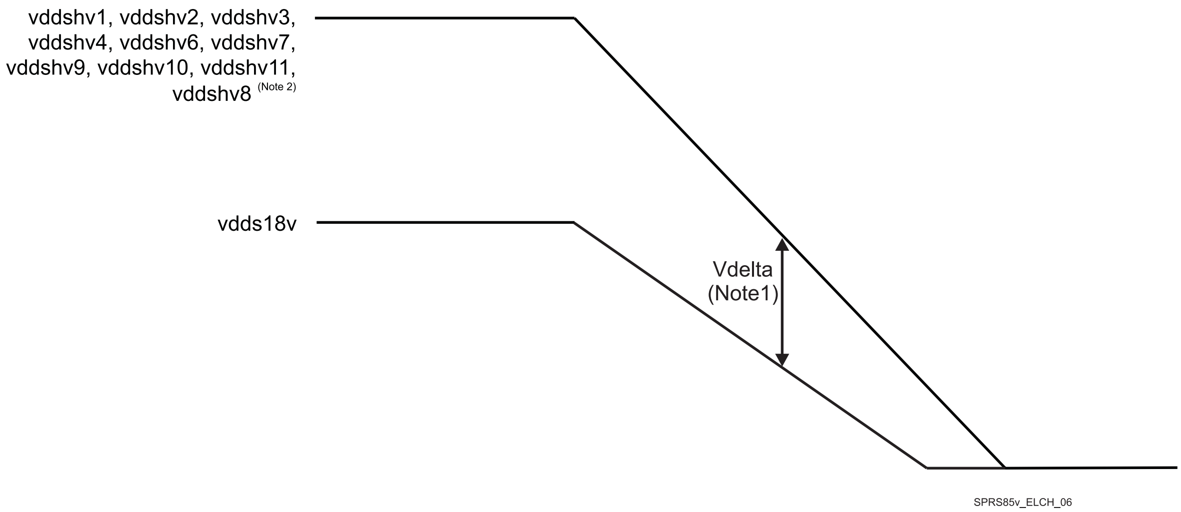


Figure 5-8. vdds18v versus vddshv[1-7, 9-11] Discharge Relationship

(1) Vdelta MAX = 2 V.

(2) If vddshv8 is powered by the same supply source as the other vddshv[1-7,9-11] rails.

If vdds18v and vdds_ddr* are disabled at the same time due to a loss of input power event or if vdds_ddr* discharges more slowly than vdds18v, analysis has shown no reliability impacts when the elapsed time period beginning with vdds18v dropping below 1.0 V and ending with vdds_ddr* dropping below 0.6 V is less than 10 ms (Figure 5-9).

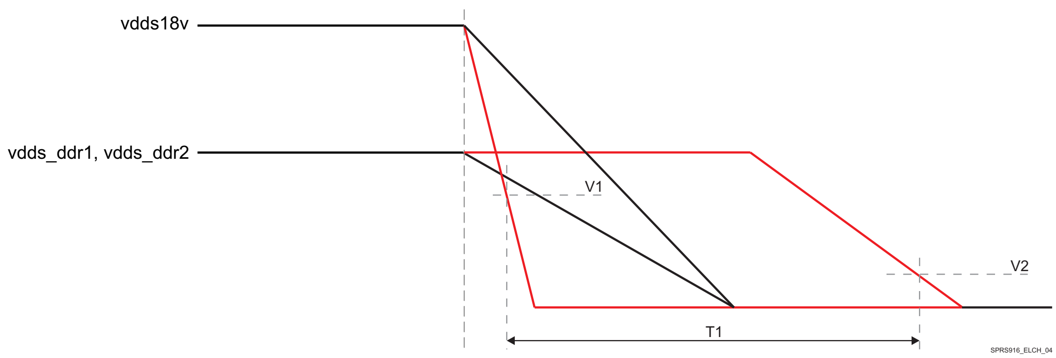


Figure 5-9. vdds18v and vdds_ddr* Discharge Relationship[(1)]

(1) V1 > 1.0 V; V2 < 0.6V; T1 < 10ms.

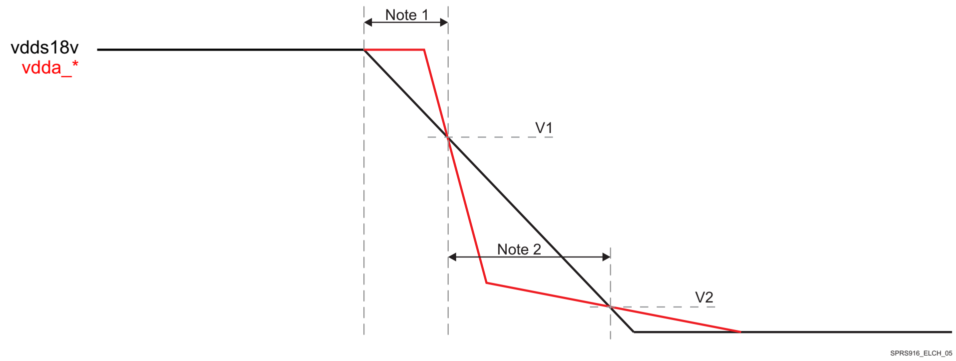


Figure 5-10. vdds18v and vdda_* Discharge Relationship(3)

(1) vdda_* can be ≥ vdds18v, until vdds18v drops below 1.62 V.

(2) vdds18v must be ≥ vdda_*, until vdds18v reaches 0.6 V.

(3) V1 = 1.62 V; V2 < 0.6 V.

Figure 5-8 through Figure 5-11 and associated notes described the device abrupt power down sequence.

A "loss of input power event" occurs when the system's input power is unexpectedly removed. Normally, the recommended power-down sequence should be followed and can be accomplished within 1.5-2 ms of elapsed time. This is the typical range of elapsed time available following a loss of power event, see Section 7.3.7 for design recommendations. If sufficient elapse time is not provided, then an "abrupt" power down sequence can be supported without impacting POH reliability if all of the following conditions are met (Figure 5-11).

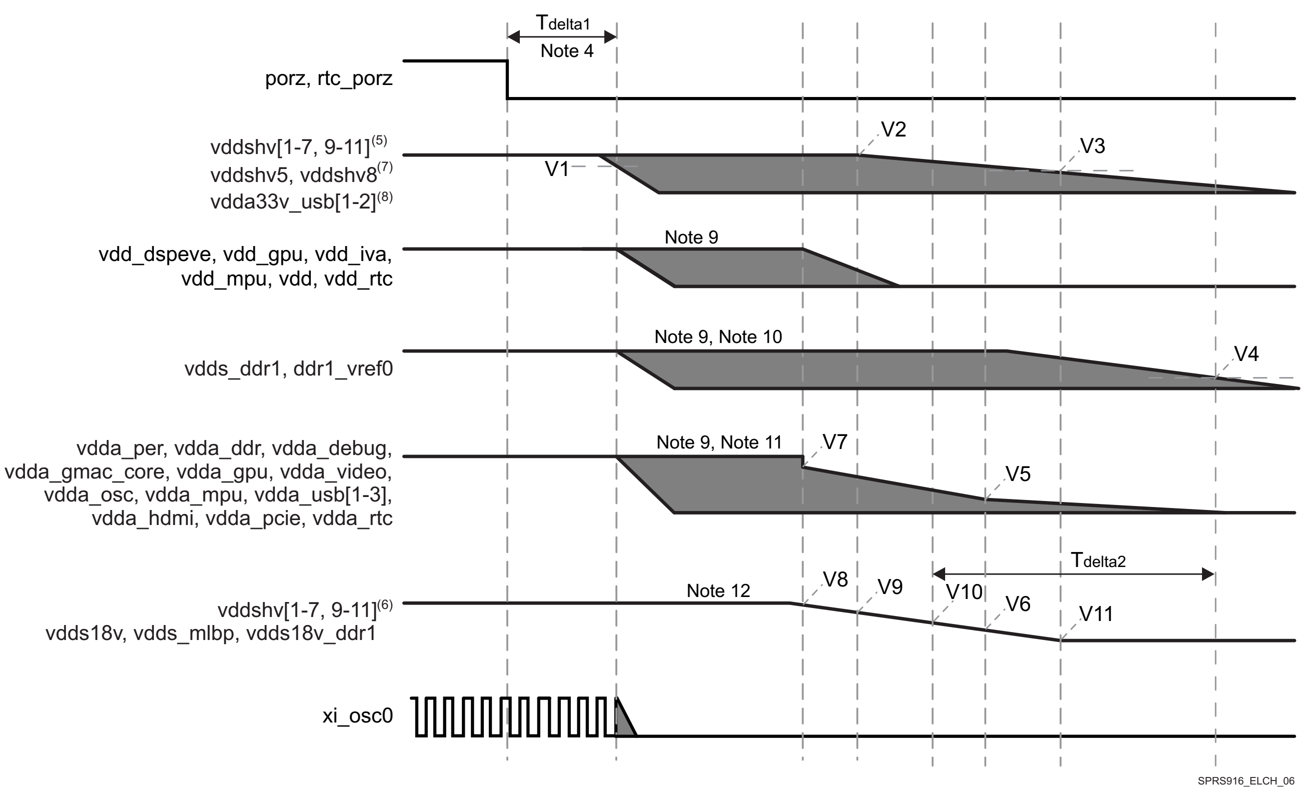


Figure 5-11. Abrupt Power-Down Sequencing(1)

(1) Time stamps:

– V1 = 2.7 V; V2 = 3.3 V; V3 = 2.0 V; V4 = V5 = V6 = 0.6 V; V7 = V8 = 1.62 V; V9 = 1.3 V; V10 = 1.0 V; V11 = 0.0 V; T_{delta1} > 100 µs; T_{delta2} < 10 ms.

(2) Terminology:

- $V_{OPR\ MIN}$ = Minimum Operational Voltage level that ensures device functionality and specified performance in Section 5.4, *Recommended Operating Conditions table*.
- V_{OFF} = OFF Voltage level is defined to be less than 0.6 V, where any current draw has no impact to POH.
- Ramp Down = transition time from $V_{OPR\ MIN}$ to V_{OFF} and is slew rate independent.

(3) General timing diagram items:

- Grey shaded areas show valid transition times for supplies between $V_{OPR\ MIN}$ and V_{OFF}.
- Dashed vertical lines show approximate elapse times based upon TI recommended PMIC power-down sequencer circuit performance.

(4) porz and rtc_porz must be asserted low for 100 µs min to ensure SoC is set to a safe functional state before any voltage begins to ramp down.

- Only if using RTC-mode with an independent RTC input power source, then rtc_porz can remain high and RTC-domains (vdd_rtc, vdda_rtc, and vddshv5) can remain energized while all other domains sourced from the system input power are powered down.

(5) vddshv[1-7, 9-11] domains supplied by 3.3 V:

- must remain greater than 2.7 V to enable Dual Voltage GPIO selector circuit operation for 100 µs min, after porz is asserted low.
- must not exceed vdds18v voltage level by more than 2 V during ramp down, until vdds18v drops below V_{OFF} (0.6 V).

(6) vddshv[1-7, 9-11] domains supplied by 1.8 V must ramp down concurrently with vdds18v and be sourced from common vdds18v supply.

(7) vddshv8 supporting SD Card:

- must be in first group of supplies to ramp down after porz has been asserted low for 100 µs min.
- must be sourced from independent power resource that can provide dual voltage (3.3 V / 1.8 V) operation as required to be compliant to SDIO specification.
- if SDIO operation is not needed, must be grouped with other vddshv[1-7, 9-11] domains.

(8) vdda33v_usb[1-2] domains must be in first group of supplies to ramp down after porz has been asserted low for 100 µs min.

(9) vdd_dspeve, vdd_gpu, vdd_iva, vdd_mpu, vdd, vdd_rtc, vdds_ddr1, vdda_* domains can all start to ramp down in any order after 100 µs low assertion of porz.

(10) vdds_ddr1 domains:

- can remain at $V_{OPR\ MIN}$ or a level greater than vdds18v during ramp down.
- elapsed time from vdds18v dropping below 1.0 V to vdds_ddr[1-3] dropping below 0.6 V must not exceed 10 ms.

(11) vdda_* domains:

- can start to ramp down before or concurrently with vdds18v.
- must not exceed vdds18v voltage level after vdds18v drops below 1.62 V until vdds18v drops below V_{OFF} (0.6 V).

(12) vdds18v domain should maintain a minimum level of 1.62 V (V_{NOM} – 10%) until vdd_dspeve and vdd start to ramp down.

5.10.4 Clock Specifications

NOTE

For more information, see Power, Reset, and Clock Management / PRCM Environment / External Clock Signal and Power Reset / PRCM Functional Description / PRCM Clock Manager Functional Description section of the Device TRM.

NOTE

Audio Back End (ABE) module is not supported for this family of devices, but “ABE” name is still present in some clock or DPLL names.

The device operation requires the following clocks:

- The 32 kHz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. This is an optional clock and will be supplied by on chip divider + mux (FUNC_32K_CLK) incase it is not available on external pin.
- The system clocks, SYS_CLK1 (Mandatory) and SYS_CLK2 (Optional) are the main clock sources of the device. They supply the reference clock to the DPLLs as well as functional clock to several modules.

The Device also embeds an internal free-running 32-kHz oscillator that is always active as long as the the wake-up (WKUP) domain is supplied.

Figure 5-12 shows the external input clock sources and the output clocks to peripherals.

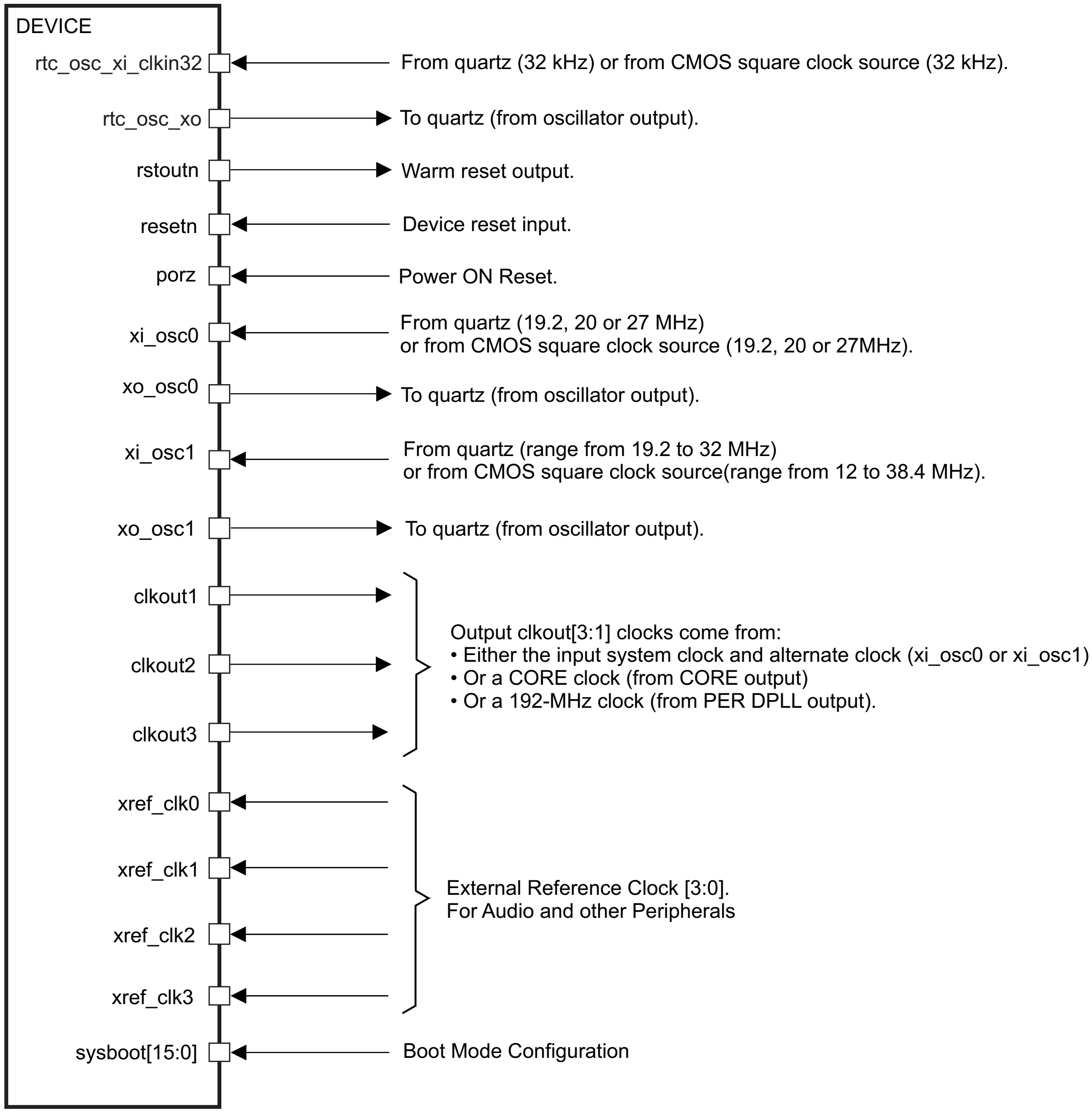


Figure 5-12. Clock Interface

5.10.4.1 Input Clocks / Oscillators

- The source of the internal system clock (SYS_CLK1) could be either:
  - A CMOS clock that enters on the xi_osc0 ball (with xo_osc0 left unconnected on the CMOS clock case).
  - A crystal oscillator clock managed by xi_osc0 and xo_osc0.
- The source of the internal system clock (SYS_CLK2) could be either:
  - A CMOS clock that enters on the xi_osc1 ball (with xo_osc1 left unconnected on the CMOS clock case).
  - A crystal oscillator clock managed by xi_osc1 and xo_osc1.
- The source of the internal system clock (FUNC_32K_CLK) could be either:
  - A CMOS clock that enters on the rtc_osc_xi_clkin32 ball and supports external LVCMOS clock generators
  - A crystal oscillator clock managed by rtc_osc_xi_clkin32 and rtc_osc_xo.

5.10.4.1.1 OSC0 External Crystal

An external crystal is connected to the device pins. Figure 5-13 describes the crystal implementation.

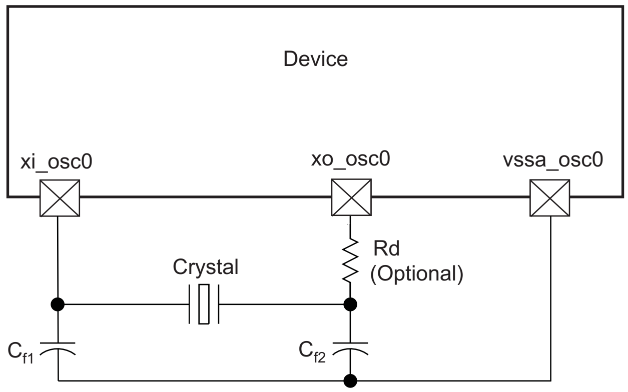


Figure 5-13. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-13, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi_osc0, xo_osc0, and vssa_osc0 pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 5-14. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 5-17 summarizes the required electrical constraints.

Table 5-17. OSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency				19.2, 20, 27		MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$			12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$			12		24	pF
$ESR(C_{f1},C_{f2})$	Crystal ESR					100	Ω
C_O	Crystal shunt capacitance	ESR = 30 Ω ESR = 40 Ω	19.2 MHz, 20 MHz, 27 MHz			7	pF
		ESR = 50 Ω	19.2 MHz, 20 MHz			7	pF
			27 MHz			5	pF
		ESR = 60 Ω	19.2 MHz, 20 MHz			7	pF
			27 MHz		Not Supported		-
		ESR = 80 Ω	19.2 MHz, 20 MHz			5	pF
			27 MHz		Not Supported		-
		ESR = 100 Ω	19.2 MHz, 20 MHz			3	pF
			27 MHz		Not Supported		-
L_M	Crystal motional inductance for f_p = 20 MHz				10.16		mH
C_M	Crystal motional capacitance				3.42		fF

Table 5-17. OSC0 Crystal Electrical Characteristics (continued)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{j(xiosc0)}$	Frequency accuracy [(1)](#), xi_osc0	Ethernet and MLB not used			±200	ppm
		Ethernet RGMII and RMII using derived clock			±50	
		Ethernet MII using derived clock			±100	
		MLB using derived clock			±50	

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 5-18 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 5-18. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency		19.2, 20, 27 MHz		MHz
t_{sX}	Start-up time			4	ms

5.10.4.1.2 OSC0 Input Clock

A 1.8-V LVCMOS-compatible clock input can be used instead of the internal oscillator to provide the SYS_CLK1 clock input to the system. The external connections to support this are shown in Figure 5-15. The xi_osc0 pin is connected to the 1.8-V LVCMOS-compatible clock source. The xi_osc0 pin is left unconnected. The vssa_osc0 pin is connected to board ground (VSS).

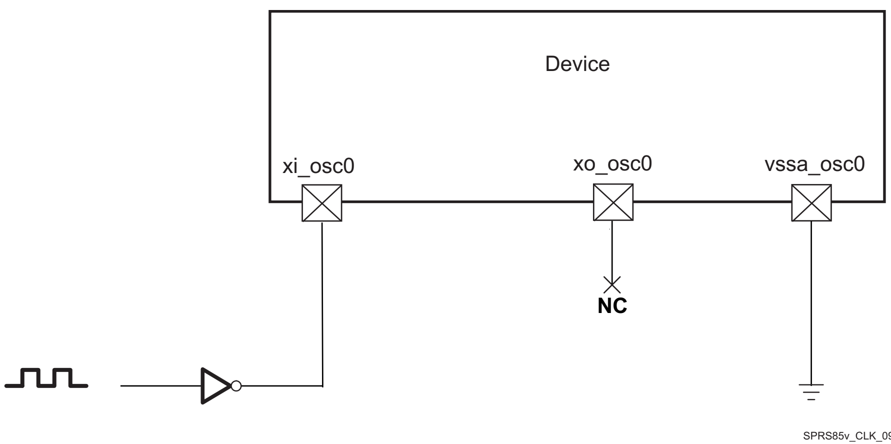


Figure 5-15. 1.8-V LVCMOS-Compatible Clock Input

Table 5-19 summarizes the OSC0 input clock electrical characteristics.

Table 5-19. OSC0 Input Clock Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		19.2, 20, 27		MHz
C_{IN}	Input capacitance	2.184	2.384	2.584	pF
I_{IN}	Input current (3.3V mode)	4	6	10	µA

Table 5-20 details the OSC0 input clock timing requirements.

Table 5-20. OSC0 Input Clock Timing Requirements

NAME		DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$1 / t_{c(xiosc0)}$	Frequency, xi_osc0		19.2, 20, 27			MHz
CK1	$t_{w(xiosc0)}$	Pulse duration, xi_osc0 low or high		0.45 × $t_{c(xiosc0)}$		0.55 × $t_{c(xiosc0)}$	ns
	$t_{j(xiosc0)}$	Period jitter[(1)], xi_osc0				0.01 × $t_{c(xiosc0)}$	ns
	$t_{R(xiosc0)}$	Rise time, xi_osc0				5	ns
	$t_{F(xiosc0)}$	Fall time, xi_osc0				5	ns
	$t_{j(xiosc0)}$	Frequency accuracy[(2)], xi_osc0	Ethernet and MLB not used			±200	ppm
			Ethernet RGMII and RMII using derived clock			±50	
			Ethernet MII using derived clock			±100	
			MLB using derived clock			±50	

(1) Period jitter is meant here as follows:

– The maximum value is the difference between the longest measured clock period and the expected clock period

– The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.

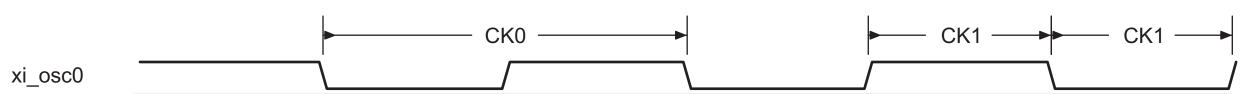


Figure 5-16. xi_osc0 Input Clock

5.10.4.1.3 Auxiliary Oscillator OSC1 Input Clock

SYS_CLK2 is received directly from oscillator OSC1. For more information about SYS_CLK2, see the Power, Reset, and Clock Management chapter of the Device TRM.

5.10.4.1.3.1 OSC1 External Crystal

An external crystal is connected to the device pins. Figure 5-17 describes the crystal implementation.

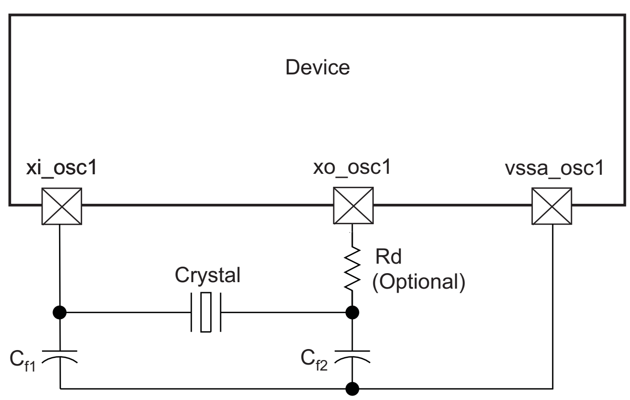


Figure 5-17. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-17, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator xi_osc1, xo_osc1, and vssa_osc1 pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 5-18. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 5-21 summarizes the required electrical constraints.

Table 5-21. OSC1 Crystal Electrical Characteristics

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency			Range from 19.2 to 32			MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$			12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$			12		24	pF
ESR(C_{f1},C_{f2})	Crystal ESR					100	Ω
C_O	Crystal shunt capacitance	ESR = 30 Ω	19.2 MHz ≤ f_p ≤ 32 MHz			7	pF
		ESR = 40 Ω	19.2 MHz ≤ f_p ≤ 32 MHz			5	pF
		ESR = 50 Ω	19.2 MHz ≤ f_p ≤ 25 MHz			7	pF
			25 MHz < f_p ≤ 27 MHz			5	pF
			27 MHz < f_p ≤ 32 MHz	Not Supported			-
		ESR = 60 Ω	19.2 MHz ≤ f_p ≤ 23 MHz			7	pF
			23 MHz < f_p ≤ 25 MHz			5	pF
			25 MHz < f_p ≤ 32 MHz	Not Supported			-
		ESR = 80 Ω	19.2 MHz ≤ f_p ≤ 23 MHz			5	pF
			23 MHz ≤ f_p ≤ 25 MHz			3	pF
			25 MHz < f_p ≤ 32 MHz	Not Supported			-
		ESR = 100 Ω	19.2 MHz ≤ f_p ≤ 20 MHz			3	pF
			20 MHz < f_p ≤ 32 MHz	Not Supported			-
L_M	Crystal motional inductance for f_p = 20 MHz				10.16		mH
C_M	Crystal motional capacitance				3.42		fF
$t_{j(xiosc1)}$	Frequency accuracy(1), xi_osc1		Ethernet and MLB not used			±200	ppm
			Ethernet RGMII and RMII using derived clock			±50	
			Ethernet MII using derived clock			±100	
			MLB using derived clock			±50	

(1) Crystal characteristics should account for tolerance+stability+aging.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

Table 5-22 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 5-22. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency	Range from 19.2 to 32			MHz

Table 5-22. Oscillator Switching Characteristics—Crystal Mode (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SX}	Start-up time			4	ms

5.10.4.1.3.2 OSC1 Input Clock

A 1.8-V LVCMOS-compatible clock input can be used instead of the internal oscillator to provide the SYS_CLK2 clock input to the system. The external connections to support this are shown in Figure 5-19. The xi_osc1 pin is connected to the 1.8-V LVCMOS-compatible clock sources. The xo_osc1 pin is left unconnected. The vssa_osc1 pin is connected to board ground (vss).

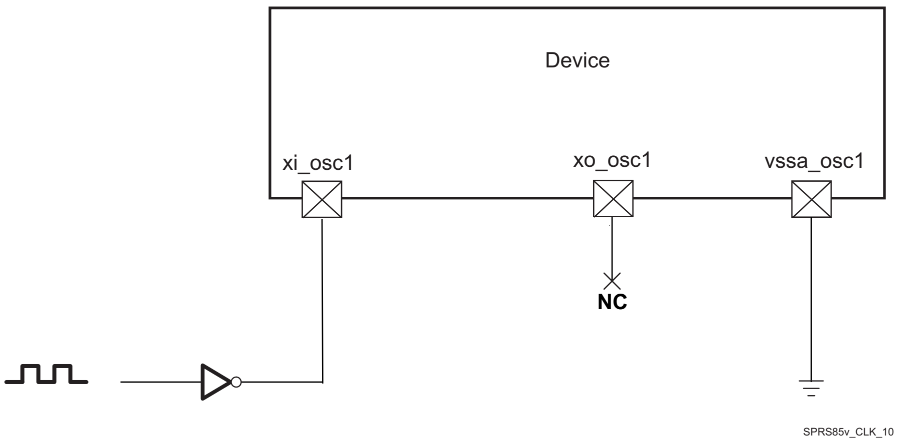


Figure 5-19. 1.8-V LVCMOS-Compatible Clock Input

Table 5-23 summarizes the OSC1 input clock electrical characteristics.

Table 5-23. OSC1 Input Clock Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency	Range from 12 to 38.4			MHz
C_{IN}	Input capacitance	2.819	3.019	3.219	pF
I_{IN}	Input current (3.3V mode)	4	6	10	µA
t_{SX}	Start-up time(1)	See(2)			ms

(1) To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 µs; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in Table 5-22, t_{SX} parameter.

(2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a wave. The switching time in this case is about 100 µs.

Table 5-24 details the OSC1 input clock timing requirements.

Table 5-24. OSC1 Input Clock Timing Requirements

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
CK0	$1 / t_{c(xiosc1)}$	Frequency, xi_osc1		Range from 12 to 38.4			MHz
CK1	$t_{w(xiosc1)}$	Pulse duration, xi_osc1 low or high		$0.45 \times t_{c(xiosc1)}$		$0.55 \times t_{c(xiosc1)}$	ns
	$t_{j(xiosc1)}$	Period jitter(1), xi_osc1				$0.01 \times t_{c(xiosc1)}$ (3)	ns
	$t_{R(xiosc1)}$	Rise time, xi_osc1				5	ns
	$t_{F(xiosc1)}$	Fall time, xi_osc1				5	ns

Table 5-24. OSC1 Input Clock Timing Requirements (continued)

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
	$t_{j(xiosc1)}$	Frequency accuracy[(2)], xi_osc1	Ethernet and MLB not used			±200	ppm
			Ethernet RGMII and RMII using derived clock			±50	
			Ethernet MII using derived clock			±100	
			MLB using derived clock			±50	

(1) Period jitter is meant here as follows:
- The maximum value is the difference between the longest measured clock period and the expected clock period
- The minimum value is the difference between the shortest measured clock period and the expected clock period

(2) Crystal characteristics should account for tolerance+stability+aging.

(3) The Period jitter requirement for osc1 can be relaxed to 0.02×$t_{c(xiosc1)}$ under the following constraints:
a.The osc1/SYS_CLK2 clock bypasses all device PLLs
b.The osc1/SYS_CLK2 clock is only used to source the DSS pixel clock outputs

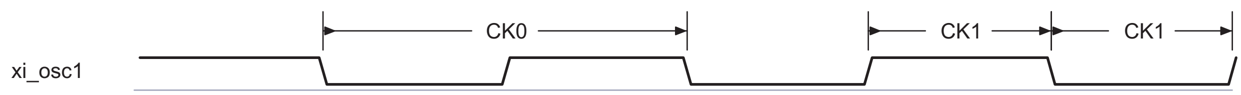


Figure 5-20. xi_osc1 Input Clock

5.10.4.1.4 *RTC Oscillator Input Clock*

FUNC_32K_CLK is received directly from RTC Oscillator. For more information about FUNC_32K_CLK, see the Power, Reset, and Clock Management chapter of the Device TRM.

5.10.4.1.4.1 *RTC Oscillator External Crystal*

An external crystal is connected to the device pins. Figure 5-13 describes the crystal implementation.

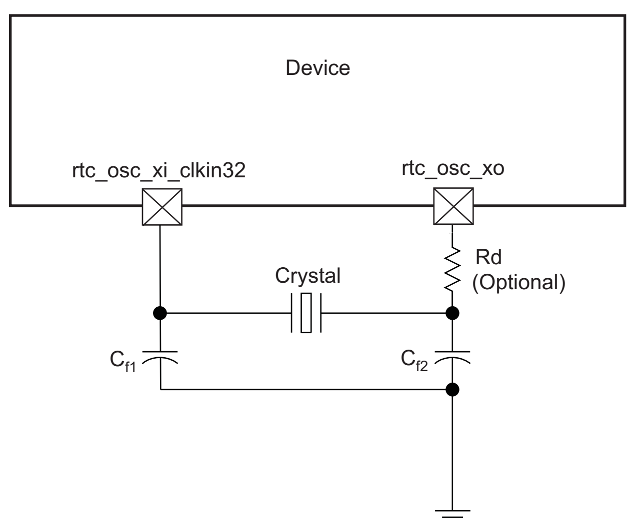


Figure 5-21. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-21, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator rtc_osc_xi_clkin32 and rtc_osc_xo pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 5-22. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 5-25 summarizes the required electrical constraints.

Table 5-25. RTC Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		32.768		kHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
$ESR(C_{f1},C_{f2})$	Crystal ESR			80	kΩ
C_O	Crystal shunt capacitance			5	pF
L_M	Crystal motional inductance for f_p = 32,768 kHz		10.7		mH
C_M	Crystal motional capacitance		2.2		fF
$t_{j(rtc\_osc\_xi\_clkin32)}$	Frequency accuracy, rtc_osc_xi_clkin32			±200	ppm

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 5-26 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 5-26. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency		32.768		kHz
t_{sX}	Start-up time			4	ms

5.10.4.1.4.2 RTC Oscillator Input Clock

A 1.8-V LVCMOS-compatible clock input can be used instead of the internal oscillator to provide the FUNC_32K_CLK clock input to the system. The external connections to support this are shown in Figure 5-23. The rtc_osc_xi_clkin32 pin is connected to the 1.8-V LVCMOS-compatible clock sources. The rtc_osc_xo pin is left unconnected.

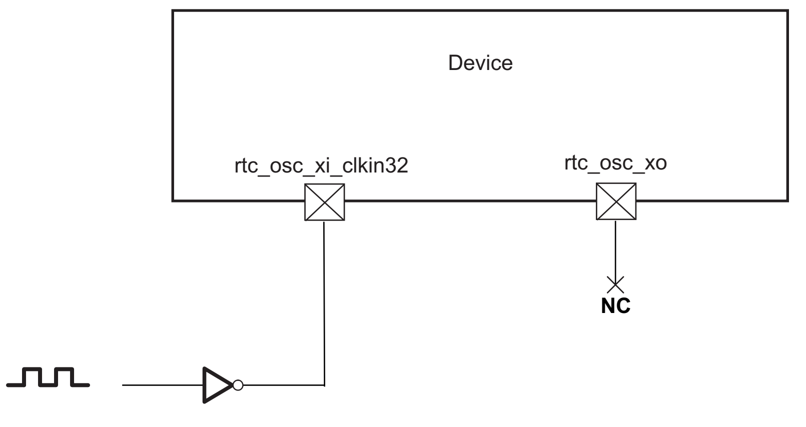


Figure 5-23. LVCMOS-Compatible Clock Input

Table 5-27 summarizes the RTC Oscillator input clock electrical characteristics.

Table 5-27. RTC Oscillator Input Clock Electrical Characteristics—Bypass Mode

NAME		DESCRIPTION	MIN	TYP	MAX	UNIT
CK0	$1/t_{c(rtc\_osc\_xi\_clkin32)}$	Frequency, rtc_osc_xi_clkin32		32.768		kHz
CK1	$t_{w(rtc\_osc\_xi\_clkin32)}$	Pulse duration, rtc_osc_xi_clkin32 low or high	0.45 × $t_{c(rtc\_osc\_xi\_clkin32)}$		0.55 × $t_{c(rtc\_osc\_xi\_clkin32)}$	ns
	C_{IN}	Input capacitance	2.178	2.378	2.578	pF
	I_{IN}	Input current (3.3V mode)	4	6	10	µA
	t_{sX}	Start-up time		See [(1)]		ms

(1) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is inapplication mode and receives a wave. The switching time in this case is about 100 µs.

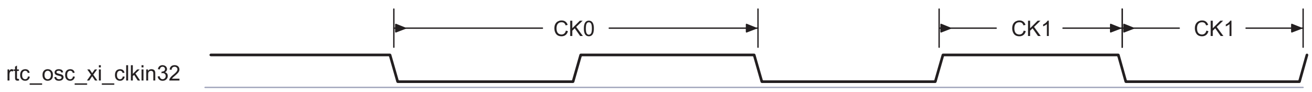


Figure 5-24. rtc_osc_xi_clkin32 Input Clock

5.10.4.2 RC On-die Oscillator Clock

NOTE

The OSC_32K_CLK clock, provided by the On-die 32K RC oscillator, inside of the SoC, is not accurate 32 kHz clock.

The frequency may significantly vary with temperature and silicon characteristics.

For more information about OSC_32K_CLK see the Device TRM, Chapter: *Power, Reset, and Clock Management*.

5.10.4.3 Output Clocks

The device provides three output clocks. Summary of these output clocks are as follows:

- clkout1 - Device Clock output 1. Can be used as a system clock for other devices. The source of the clkout1 could be either:
  - The input system clock and alternate clock (xi_osc0 or xi_osc1)
  - CORE clock (from CORE output)
  - 192-MHz clock (from PER DPLL output)
- clkout2 - Device Clock output 2. Can be used as a system clock for other devices. The source of the clkout2 could be either:
  - The input system clock and alternate clock (xi_osc0 or xi_osc1)
  - CORE clock (from CORE output)
  - 192-MHz clock (from PER DPLL output)
- clkout3 - Device Clock output 3. Can be used as a system clock for other devices. The source of the clkout3 could be either:
  - The input system clock and alternate clock (xi_osc0 or xi_osc1)
  - CORE clock (from CORE output)
  - 192-MHz clock (from PER DPLL output)

For more information about Output Clocks see Device TRM, Chapter: *Power, Reset, and Clock Management*.

5.10.4.4 DPLLs, DLLs

NOTE

For more information, see:

- Power, Reset, and Clock Management / Clock Management Functional / Internal Clock Sources / Generators / Generic DPLL Overview Section

  and

- Display Subsystem / Display Subsystem Overview section of the Device TRM.

To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module. They are of two types: type A and type B DPLLs.

- They have their own independent power domain (each one embeds its own switch and can be controlled as an independent functional power domain)
- They are fed with ALWAYS ON system clock, with independent control per DPLL.

The different DPLLs managed by the PRCM are listed below:

- DPLL_MPU: It supplies the MPU subsystem clocking internally.
- DPLL_IVA: It feeds the IVA subsystem clocking.
- DPLL_CORE: It supplies all interface clocks and also few module functional clocks.
- DPLL_PER: It supplies several clock sources: a 192-MHz clock for the display functional clock, a 96-MHz functional clock to subsystems and peripherals.
- DPLL_ABE: It provides clocks to various modules within the device.
- DPLL_USB: It provides 960M clock for USB modules (USB1/2/3/4).
- DPLL_GMAC: It supplies several clocks for the Gigabit Ethernet Switch (GMAC_SW).
- DPLL_EVE: It provides the Embedded Vision Engine Subsystem (EVE1 and EVE2) clocking.
- DPLL_DSP: It feeds the DSP Subsystem clocking.
- DPLL_GPU: It supplies clock for the GPU Subsystem.
- DPLL_DDR: It generates clocks for the two External Memory Interface (EMIF) controllers and their associated EMIF PHYs.
- DPLL_PCIE_REF: It provides reference clock for the APLL_PCIE in PCIE Subsystem.
- APLL_PCIE: It feeds clocks for the device Peripheral Component Interconnect Express (PCIe) controllers.

NOTE

The following DPLLs are controlled by the clock manager located in the always-on Core power domain (CM_CORE_AON):

- DPLL_MPU, DPLL_IVA, DPLL_CORE, DPLL_ABE, DPLL_DDR, DPLL_GMAC, DPLL_PCIE_REF, DPLL_PER, DPLL_USB, DPLL_EVE, DPLL_DSP, DPLL_GPU, APLL_PCIE_REF.

For more information on CM_CORE_AON and CM_CORE or PRCM DPLLs, see Power, Reset, and Clock Management (PRCM) chapter of the Device TRM.

The following DPLLs are not managed by the PRCM:

- DPLL_VIDEO1; (It is controlled from DSS)
- DPLL_VIDEO2; (It is controlled from DSS)
- DPLL_HDMI; (It is controlled from DSS)
- DPLL_SATA; (It is controlled from SATA)
- DPLL_DEBUG; (It is controlled from DEBUGSS)
- DPLL_USB_OTG_SS; (It is controlled from OCP2SCP1)

NOTE

For more information for not controlled from PRCM DPLL's see the related chapters in TRM.

5.10.4.4.1 DPLL Characteristics

The DPLL has three relevant input clocks. One of them is the reference clock (CLKINP) used to generated the synthesized clock but can also be used as the bypass clock whenever the DPLL enters a bypass mode. It is therefore mandatory. The second one is a fast bypass clock (CLKINPULOW) used when selected as the bypass clock and is optional. The third clock (CLKINPHIF) is explained in the next paragraph.

The DPLL has three output clocks (namely CLKOUT, CLKOUTX2, and CLKOUTHIF). CLKOUT and CLKOUTX2 run at the bypass frequency whenever the DPLL enters a bypass mode. Both of them are generated from the lock frequency divided by a post-divider (namely M2 post-divider). The third clock, CLKOUTHIF, has no automatic bypass capability. It is an output of a post-divider (M3 post-divider) with the input clock selectable between the internal lock clock (Fdpll) and CLKINPHIF input of the PLL through an asynchronous multplexing.

For more information, see the Power Reset Controller Management chapter of the Device TRM.

Table 5-28 summarizes DPLL type described in Section 5.10.4.4, *DPLLs, DLLs Specifications* introduction.

Table 5-28. DPLL Control Type

DPLL NAME	TYPE	CONTROLLED BY PRCM
DPLL_ABE	Table 5-29 (Type A)	Yes(1)
DPLL_CORE	Table 5-29 (Type A)	Yes(1)
DPLL_DEBUGSS	Table 5-29 (Type A)	No(2)
DPLL_DSP	Table 5-29 (Type A)	Yes(1)
DPLL_EVE	Table 5-29 (Type A)	Yes(1)
DPLL_GMAC	Table 5-29 (Type A)	Yes(1)
DPLL_HDMI	Table 5-30 (Type B)	No(2)
DPLL_IVA	Table 5-29 (Type A)	Yes(1)
DPLL_MPU	Table 5-29 (Type A)	Yes(1)
DPLL_PER	Table 5-29 (Type A)	Yes(1)
APLL_PCIE	Table 5-29 (Type A)	Yes(1)
DPLL_PCIE_REF	Table 5-30 (Type B)	Yes(1)
DPLL_SATA	Table 5-30 (Type B)	No(2)
DPLL_USB	Table 5-30 (Type B)	Yes(1)
DPLL_USB_OTG_SS	Table 5-30 (Type B)	No(2)
DPLL_VIDEO1	Table 5-29 (Type A)	No(2)
DPLL_VIDEO2	Table 5-29 (Type A)	No(2)
DPLL_DDR	Table 5-29 (Type A)	Yes(1)
DPLL_GPU	Table 5-29 (Type A)	Yes(1)

(1) DPLL is in the always-on domain.

(2) DPLL is not controlled by the PRCM.

Table 5-29 and Table 5-30 summarize the DPLL characteristics and assume testing over recommended operating conditions.

Table 5-29. DPLL Type A Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
f_{input}	CLKINP input frequency	0.032		52	MHz	F_{INP}

Table 5-29. DPLL Type A Characteristics (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
$f_{internal}$	Internal reference frequency	0.15		52	MHz	REFCLK
$f_{CLKINPHIF}$	CLKINPHIF input frequency	10		1400	MHz	F_{INPHIF}
$f_{CLKINPULOW}$	CLKINPULOW input frequency	0.001		600	MHz	Bypass mode: f_{CLKOUT} = $f_{CLKINPULOW}$ / (M1 + 1) if ulowclken = 1(6)
f_{CLKOUT}	CLKOUT output frequency	20(1)		1800(2)	MHz	[M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
$f_{CLKOUTx2}$	CLKOUTx2 output frequency	40(1)		2200(2)	MHz	2 × [M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
$f_{CLKOUTHIF}$	CLKOUTHIF output frequency	20(3)		1400(4)	MHz	F_{INPHIF} / M3 if clkinphifsel = 1
		40(3)		2200(4)	MHz	2 × [M / (N + 1)] × F_{INP} × [1 / M3] if clkinphifsel = 0
$f_{CLKDCOLDO}$	DCOCLKLDO output frequency	40		2800	MHz	2 × [M / (N + 1)] × F_{INP} (in locked condition)
t_{lock}	Frequency lock time			6 + 350 × REFCLK	µs	
p_{lock}	Phase lock time			6 + 500 × REFCLK	µs	
$t_{relock-L}$	Relock time—Frequency lock(5) (LP relock time from bypass)			6 + 70 × REFCLK	µs	DPLL in LP relock time: lowcurrstdby = 1
$p_{relock-L}$	Relock time—Phase lock(5) (LP relock time from bypass)			6 + 120 × REFCLK	µs	DPLL in LP relock time: lowcurrstdby = 1
$t_{relock-F}$	Relock time—Frequency lock(5) (fast relock time from bypass)			3.55 + 70 × REFCLK	µs	DPLL in fast relock time: lowcurrstdby = 0
$p_{relock-F}$	Relock time—Phase lock(5) (fast relock time from bypass)			3.55 + 120 × REFCLK	µs	DPLL in fast relock time: lowcurrstdby = 0

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10 °C maximum temperature drift.

(6) Bypass mode: f_{CLKOUT} = F_{INP} if ulowclken = 0. For more information, see the Device TRM.

Table 5-30. DPLL Type B Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
f_{input}	CLKINP input clock frequency	0.62		60	MHz	F_{INP}
$f_{internal}$	REFCLK internal reference clock frequency	0.62		2.5	MHz	[1 / (N + 1)] × F_{INP}
$f_{CLKINPULOW}$	CLKINPULOW bypass input clock frequency	0.001		600	MHz	Bypass mode: f_{CLKOUT} = $f_{CLKINPULOW}$ / (M1 + 1) If ulowclken = 1(4)
$f_{CLKLDOOUT}$	CLKOUTLDO output clock frequency	20(1)(5)		2500(2)(5)	MHz	M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
f_{CLKOUT}	CLKOUT output clock frequency	20(1)(5)		1450(2)(5)	MHz	[M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
$f_{CLKDCOLDO}$	Internal oscillator (DCO) output clock frequency	750(5)		1500(5)	MHz	[M / (N + 1)] × F_{INP} (in locked condition)
		1250(5)		2500(5)	MHz	

Table 5-30. DPLL Type B Characteristics (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
t_J	CLKOUTLDO period jitter	–2.5 %		2.5 %		The period jitter at the output clocks is ± 2.5 % peak to peak
	CLKOUT period jitter					
	CLKDCOLDO period jitter					
t_{lock}	Frequency lock time			350 × REFCLKs	µs	
p_{lock}	Phase lock time			500 × REFCLKs	µs	
$t_{relock-L}$	Relock time—Frequency lock(3) (LP relock time from bypass)			9 + 30 × REFCLKs	µs	
$p_{relock-L}$	Relock time—Phase lock(3) (LP relock time from bypass)			9 + 125 × REFCLKs	µs	

(1) The minimum frequency on CLKOUT is assuming M2 = 1.

For M2 > 1, the minimum frequency on this clock will further scale down by factor of M2.

(2) The maximum frequency on CLKOUT is assuming M2 = 1.

(3) Relock time assumes typical operating conditions, 10 °C maximum temperature drift.

(4) Bypass mode: $f_{CLKOUT} = F_{INP}$ if ULOWCLKEN = 0. For more information, see the Device TRM.

(5) For output clocks, there are two frequency ranges according to the SELFREQDCO setting. For more information, see the Device TRM.

5.10.4.4.2 DLL Characteristics

Table 5-31 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

Table 5-31. DLL Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{input}	Input clock frequency (EMIF_DLL_FCLK)			266	MHz
t_{lock}	Lock time			50k	cycles
t_{relock}	Relock time (a change of the DLL frequency implies that DLL must relock)			50k	cycles

5.10.4.4.3 DPLL and DLL Noise Isolation

NOTE

For more information on DPLL and DLL decoupling capacitor requirements, see the External Capacitors / Voltage Decoupling Capacitors / I/O and Analog Voltage Decoupling / VDDA Power Domain section.

5.10.5 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Monotonic transitions are more easily guaranteed with faster switching signals. Slower input transitions are more susceptible to glitches due to noise and special care should be taken for slow input clocks.

5.10.6 Peripherals

5.10.6.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

5.10.6.2 Virtual and Manual I/O Timing Modes

Some of the timings described in the following sections require the use of Virtual or Manual I/O Timing Modes. Table 5-32 provides a summary of the Virtual and Manual I/O Timing Modes across all device interfaces. The individual interface timing sections found later in this document provide the full description of each applicable Virtual and Manual I/O Timing Mode. Refer to the Pad Configuration section of the Device TRM for the procedure on implementing the Virtual and Manual Timing Modes in a system.

Table 5-32. Modes Summary

Virtual or Manual IO Mode Name	Datasheet Timing Mode
VIP	
VIP1_MANUAL1	VIN1A/1B/2A Rise-Edge Capture Mode Timings
VIP1_2B_MANUAL1	VIN2B Rise-Edge Capture Mode Timings
VIP1_MANUAL2	VIN1A/1B/2A Fall-Edge Capture Mode Timings
VIP1_2B_MANUAL2	VIN2B Fall-Edge Capture Mode Timings
VIP2_MANUAL1	VIN3A and VIN3B IOSET1 Rise-Edge Capture Mode Timings
VIP2_4A_MANUAL1	VIN4A IOSET1/2 Rise-Edge Capture Mode Timings
VIP2_4A_IOSET3_MANUAL1	VIN4A IOSET3 Rise-Edge Capture Mode Timings
VIP2_4B_MANUAL1	VIN4B Rise-Edge Capture Mode Timings
VIP2_3B_IOSET2_MANUAL1	VIN3B IOSET2 Rise-Edge Capture Mode Timings
VIP2_3B_IOSET2_MANUAL2	VIN3B IOSET2 Fall-Edge Capture Mode Timings
VIP2_MANUAL2	VIN3A, VIN3B IOSET1 Fall-Edge Capture Mode Timings
VIP2_4A_MANUAL2	VIN4A IOSET1/2 Fall-Edge Capture Mode Timings
VIP2_4A_IOSET3_MANUAL2	VIN4A IOSET3 Fall-Edge Capture Mode Timings
VIP2_4B_MANUAL2	VIN4B Fall-Edge Capture Mode Timings
DPI Video Output	
VOUT1_MANUAL1	DPI1 Video Output Alternate Timings
VOUT1_MANUAL2	DPI1 Video Output Default Timings
VOUT1_MANUAL3	DPI1 Video Output MANUAL3 Timings
VOUT1_MANUAL4	DPI1 Video Output MANUAL4 Timings
VOUT2_IOSET1_MANUAL1	DPI2 Video Output IOSET1 Alternate Timings
VOUT2_IOSET1_MANUAL2	DPI2 Video Output IOSET1 Default Timings
VOUT2_IOSET1_MANUAL3	DPI2 Video Output IOSET1 MANUAL3 Timings
VOUT2_IOSET1_MANUAL4	DPI2 Video Output IOSET1 MANUAL4 Timings
VOUT2_IOSET2_MANUAL1	DPI2 Video Output IOSET2 Alternate Timings
VOUT2_IOSET2_MANUAL2	DPI2 Video Output IOSET2 Default Timings
VOUT2_IOSET2_MANUAL3	DPI2 Video Output IOSET2 MANUAL3 Timings
VOUT2_IOSET2_MANUAL4	DPI2 Video Output IOSET2 MANUAL4 Timings
VOUT3_MANUAL1	DPI3 Video Output Alternate Timings
VOUT3_MANUAL2	DPI3 Video Output Default Timings
VOUT3_MANUAL3	DPI3 Video Output MANUAL3 Timings
VOUT3_MANUAL4	DPI3 Video Output MANUAL4 Timings
GPMC	
No Virtual or Manual IO Timing Mode Required	GPMC Asyncronous Mode Timings and Synchronous Mode - Default Timings
GPMC_VIRTUAL1	GPMC Synchronous Mode - Alternate Timings
McASP	
No Virtual or Manual IO Timing Mode Required	McASP1 Synchronous Transmit Timings
MCASP1_VIRTUAL1_ASYNC_TX	See Table 5-80
MCASP1_VIRTUAL2_SYNC_RX	See Table 5-80
MCASP1_VIRTUAL3_ASYNC_RX	See Table 5-80

Table 5-32. Modes Summary (continued)

Virtual or Manual IO Mode Name	Datasheet Timing Mode
No Virtual or Manual IO Timing Mode Required	McASP2 Synchronous Transmit Timings
MCASP2_VIRTUAL1_ASYNC_RX_80M	See Table 5-81
MCASP2_VIRTUAL2_ASYNC_RX	See Table 5-81
MCASP2_VIRTUAL3_ASYNC_TX	See Table 5-81
MCASP2_VIRTUAL4_SYNC_RX	See Table 5-81
MCASP2_VIRTUAL5_SYNC_RX_80M	See Table 5-81
No Virtual or Manual IO Timing Mode Required	McASP3 Synchronous Transmit Timings
MCASP3_VIRTUAL2_SYNC_RX	See Table 5-82
No Virtual or Manual IO Timing Mode Required	McASP4 Synchronous Transmit Timings
MCASP4_VIRTUAL1_SYNC_RX	See Table 5-83
No Virtual or Manual IO Timing Mode Required	McASP5 Synchronous Transmit Timings
MCASP5_VIRTUAL1_SYNC_RX	See Table 5-84
No Virtual or Manual IO Timing Mode Required	McASP6 Synchronous Transmit Timings
MCASP6_VIRTUAL1_SYNC_RX	See Table 5-85
No Virtual or Manual IO Timing Mode Required	McASP7 Synchronous Transmit Timings
MCASP7_VIRTUAL2_SYNC_RX	See Table 5-86
No Virtual or Manual IO Timing Mode Required	McASP8 Synchronous Transmit Timings
MCASP8_VIRTUAL1_SYNC_RX	See Table 5-87
eMMC/SD/SDIO	
No Virtual or Manual IO Timing Mode Required	MMC1 DS (Pad Loopback) and SDR12 (Pad Loopback) Timings
MMC1_VIRTUAL1	MMC1 HS (Internal Loopback and Pad Loopback), SDR12 (Internal Loopback), SDR25 Timings (Internal Loopback and Pad Loopback)
MMC1_VIRTUAL2	SDR50 (Pad Loopback) Timings
MMC1_VIRTUAL5	MMC1 DS (Internal Loopback) Timings
MMC1_VIRTUAL6	MMC1 SDR50 (Internal Loopback) Timings
MMC1_VIRTUAL7	MMC1 DDR50 (Internal Loopback) Timings
MMC1_DDR_MANUAL1	MMC1 DDR50 (Pad Loopback) Timings
MMC1_SDR104_MANUAL1	MMC1 SDR104 Timings
No Virtual or Manual IO Timing Mode Required	MMC2 Standard (Pad Loopback), High Speed (Pad Loopback), and DDR (Pad Loopback) Timings
MMC2_DDR_LB_MANUAL1	MMC2 DDR (Internal Loopback) Timings
MMC2_HS200_MANUAL1	MMC2 HS200 Timings
MMC2_STD_HS_LB_MANUAL1	MMC2 Standard (Internal Loopback), High Speed (Internal Loopback) Timings
MMC3_MANUAL1	MMC3 DS, SDR12, HS, SDR25 Timings
MMC3_MANUAL2	MMC3 SDR50 Timings
MMC4_MANUAL1	MMC4 SDR12, HS, SDR25 Timings
MMC4_DS_MANUAL1	MMC4 DS Timings
QSPI	
No Virtual or Manual IO Timing Mode Required	QSPI Mode 3 Boot Timing Mode
QSPI_MODE3_MANUAL1	QSPI Mode 3 Default Timing Mode
QSPI_MODE0_MANUAL1	QSPI Mode 0 Default Timing Mode
GMAC	
No Virtual or Manual IO Timing Mode Required	GMAC MII0/1 Timings
GMAC_RMII0_MANUAL1	GMAC RMII0 Timings
GMAC_RMII1_MANUAL1	GMAC RMII1 Timings
GMAC_RGMII0_MANUAL1	GMAC RGMII0 Internal Delay Enabled Timings
GMAC_RGMII1_MANUAL1	GMAC RGMII1 Internal Delay Enabled Timings
HDMI, EMIF, Timers, I2C, UART, McSPI, USB, SATA, PCIe, DCAN, GPIO, PWM, JTAG, TPIU, RTC, SDMA, INTC	

Table 5-32. Modes Summary (continued)

Virtual or Manual IO Mode Name	Datasheet Timing Mode
No Virtual or Manual IO Timing Mode Required	All Modes

5.10.6.3 VIP

The Device includes 2 Video Input Ports (VIP).

Table 5-33, Figure 5-25 and Figure 5-26 present timings and switching characteristics of the VIPs.

CAUTION

The IO timings provided in this section are applicable for all combinations of signals for vin1. However, the timings are only valid for vin2, vin3, and vin4 if signals within a single IOSET are used. The IOSETs are defined in the Table 5-34.

Table 5-33. Timing Requirements for VIP (3)(4)(5)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
V1	$t_{c(CLK)}$	Cycle time, vinx_clki (3) (5)		6.06		ns
V2	$t_{w(CLKH)}$	Pulse duration, vinx_clki high (3) (5)		0.45P (2)		ns
V3	$t_{w(CLKL)}$	Pulse duration, vinx_clki low (3) (5)		0.45P (2)		ns
V4	$t_{su(CTL/DATA-CLK)}$	Input setup time, Control (vinx_dei, vinx_vsynci, vinx_fldi, vinx_hsynci) and Data (vinx_dn) valid to vinx_clki transition (3) (4) (5)	vin1x, vin2x	2.93		ns
			vin3x, vin4x	3.11		ns
V5	$t_{h(CLK-CTL/DATA)}$	Input hold time, Control (vinx_dei, vinx_vsynci, vinx_fldi, vinx_hsynci) and Data (vinx_dn) valid from vinx_clki transition (3) (4) (5)		-0.05		ns

(1) For maximum frequency of 165 MHz.
(2) P = vinx_clki period.
(3) x in vinx = 1a, 1b, 2a, 2b, 3a, 3b, 4a, 4b.
(4) n in dn = 0 to 7 when x = 1b, 2b, 3b and 4b;
n = 0 to 23 when x = 1a, 2a, 3a and 4a;
(5) i in clki, dei, vsynci, hsynci and fldi = 0 or 1.

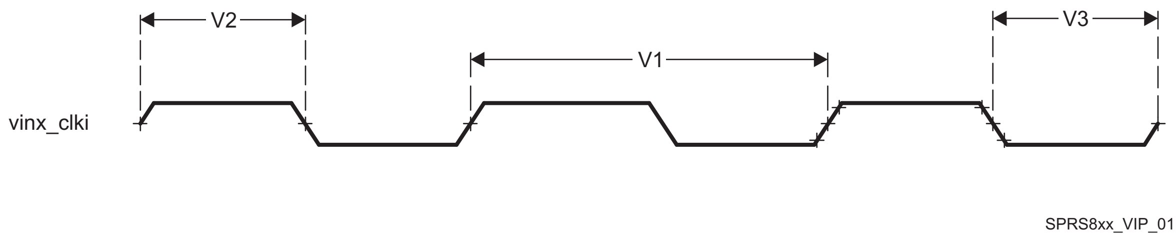


Figure 5-25. Video Input Ports clock signal

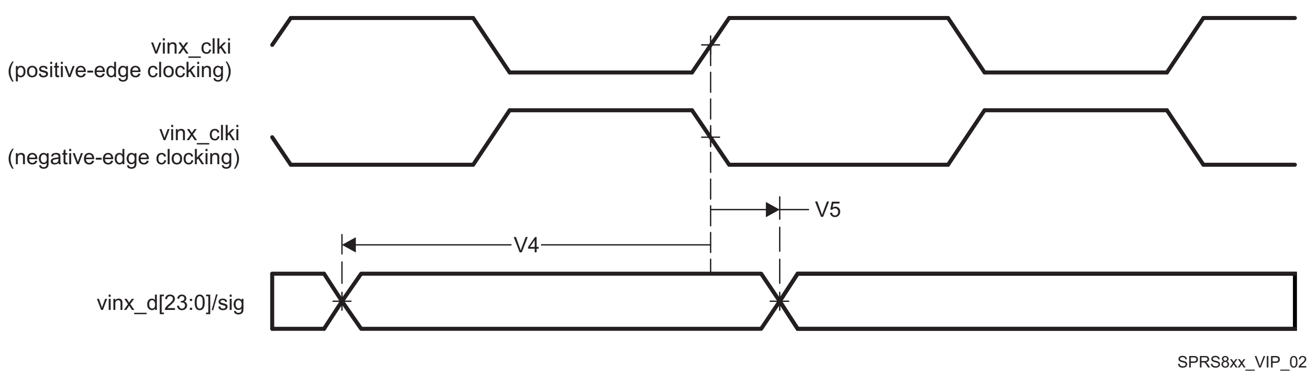


Figure 5-26. Video Input Ports timings

In Table 5-34, Table 5-35 and Table 5-36 are presented the specific groupings of signals (IOSET) for use with vin2, vin3, and vin4.

Table 5-34. VIN2 IOSETs

Signals	IOSET1		IOSET2		IOSET3	
	BALL	MUX	BALL	MUX	BALL	MUX
vin2a						
vin2a_d0	F2	0	F2	0	U4	4
vin2a_d1	F3	0	F3	0	V2	4
vin2a_d2	D1	0	D1	0	Y1	4
vin2a_d3	E2	0	E2	0	W9	4
vin2a_d4	D2	0	D2	0	V9	4
vin2a_d5	F4	0	F4	0	U5	4
vin2a_d6	C1	0	C1	0	V5	4
vin2a_d7	E4	0	E4	0	V4	4
vin2a_d8	F5	0	F5	0	V3	4
vin2a_d9	E6	0	E6	0	Y2	4
vin2a_d10	D3	0	D3	0	U6	4
vin2a_d11	F6	0	F6	0	U3	4
vin2a_d12	D5	0	D5	0	-	-
vin2a_d13	C2	0	C2	0	-	-
vin2a_d14	C3	0	C3	0	-	-
vin2a_d15	C4	0	C4	0	-	-
vin2a_d16	B2	0	B2	0	-	-
vin2a_d17	D6	0	D6	0	-	-
vin2a_d18	C5	0	C5	0	-	-
vin2a_d19	A3	0	A3	0	-	-
vin2a_d20	B3	0	B3	0	-	-
vin2a_d21	B4	0	B4	0	-	-
vin2a_d22	B5	0	B5	0	-	-
vin2a_d23	A4	0	A4	0	-	-
vin2a_hsync0	G1	0	G1	0	U7	4
vin2a_vsync0	G6	0	G6	0	V6	4
vin2a_de0	G2	0	-	-	V7	4
vin2a_fld0	H7	0	G2	1	W2	4
vin2a_clk0	E1	0	E1	0	V1	4
vin2b						
vin2b_clk1	H7	2	H7	2	AB5	4
vin2b_de1	-	-	G2	3	AB8	4
vin2b_fld1	G2	2	-	-	-	-
vin2b_d0	A4	2	A4	2	AD6	4
vin2b_d1	B5	2	B5	2	AC8	4
vin2b_d2	B4	2	B4	2	AC3	4
vin2b_d3	B3	2	B3	2	AC9	4
vin2b_d4	A3	2	A3	2	AC6	4
vin2b_d5	C5	2	C5	2	AC7	4
vin2b_d6	D6	2	D6	2	AC4	4
vin2b_d7	B2	2	B2	2	AD4	4
vin2b_hsync1	G1	3	G1	3	AC5	4

Table 5-34. VIN2 IOSETs (continued)

Signals	IOSET1		IOSET2		IOSET3	
	BALL	MUX	BALL	MUX	BALL	MUX
vin2b_vsync1	G6	3	G6	3	AB4	4

Table 5-35. VIN3 IOSETs

Signals	IOSET1		IOSET2		IOSET3		IOSET4	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin3a								
vin3a_d0	M6	2	AF1	6	AF1	6	B7	4
vin3a_d1	M2	2	AE3	6	AE3	6	B8	4
vin3a_d2	L5	2	AE5	6	AE5	6	A7	4
vin3a_d3	M1	2	AE1	6	AE1	6	A8	4
vin3a_d4	L6	2	AE2	6	AE2	6	C9	4
vin3a_d5	L4	2	AE6	6	AE6	6	A9	4
vin3a_d6	L3	2	AD2	6	AD2	6	B9	4
vin3a_d7	L2	2	AD3	6	AD3	6	A10	4
vin3a_d8	L1	2	B2	6	B2	6	E8	4
vin3a_d9	K2	2	D6	6	D6	6	D9	4
vin3a_d10	J1	2	C5	6	C5	6	D7	4
vin3a_d11	J2	2	A3	6	A3	6	D8	4
vin3a_d12	H1	2	B3	6	-	-	A5	4
vin3a_d13	J3	2	B4	6	-	-	C6	4
vin3a_d14	H2	2	B5	6	-	-	C8	4
vin3a_d15	H3	2	A4	6	-	-	C7	4
vin3a_d16	R6	2	-	-	-	-	F11	4
vin3a_d17	T9	2	-	-	-	-	G10	4
vin3a_d18	T6	2	-	-	-	-	F10	4
vin3a_d19	T7	2	-	-	-	-	G11	4
vin3a_d20	P6	2	-	-	-	-	E9	4
vin3a_d21	R9	2	-	-	-	-	F9	4
vin3a_d22	R5	2	-	-	-	-	F8	4
vin3a_d23	P5	2	-	-	-	-	E7	4
vin3a_hsync0	N7	2	N7	2	B5	5	C11	4
vin3a_vsync0	R4	2	R4	2	A4	5	E11	4
vin3a_de0	N9	2	N9	2	B3	5	B10	4
vin3a_fld0	P9	2	P9	2	B4	5	D11	4
vin3a_clk0	P1	2	AH7	6	AH7	6	B11	4
vin3b								
vin3b_clk1	P7	6	M4	4	-	-	-	-
vin3b_de1	N6	6	N6	6	-	-	-	-
vin3b_fld1	M4	6	-	-	-	-	-	-
vin3b_d0	K7	6	K7	6	-	-	-	-
vin3b_d1	M7	6	M7	6	-	-	-	-
vin3b_d2	J5	6	J5	6	-	-	-	-
vin3b_d3	K6	6	K6	6	-	-	-	-
vin3b_d4	J7	6	J7	6	-	-	-	-
vin3b_d5	J4	6	J4	6	-	-	-	-
vin3b_d6	J6	6	J6	6	-	-	-	-

Table 5-35. VIN3 IOSETs (continued)

Signals	IOSET1		IOSET2		IOSET3		IOSET4	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
vin3b_d7	H4	6	H4	6	-	-	-	-
vin3b_hsync1	H5	6	H5	6	-	-	-	-
vin3b_vsync1	H6	6	H6	6	-	-	-	-

Table 5-36. VIN4 IOSETs

Signals	IOSET1		IOSET2		IOSET3	
	BALL	MUX	BALL	MUX	BALL	MUX
vin4a						
vin4a_d0	R6	4	B7	3	B14	8
vin4a_d1	T9	4	B8	3	J14	8
vin4a_d2	T6	4	A7	3	G13	8
vin4a_d3	T7	4	A8	3	J11	8
vin4a_d4	P6	4	C9	3	E12	8
vin4a_d5	R9	4	A9	3	F13	8
vin4a_d6	R5	4	B9	3	C12	8
vin4a_d7	P5	4	A10	3	D12	8
vin4a_d8	U2	4	E8	3	E15	8
vin4a_d9	U1	4	D9	3	A20	8
vin4a_d10	P3	4	D7	3	B15	8
vin4a_d11	R2	4	D8	3	A15	8
vin4a_d12	K7	4	A5	3	D15	8
vin4a_d13	M7	4	C6	3	B16	8
vin4a_d14	J5	4	C8	3	B17	8
vin4a_d15	K6	4	C7	3	A17	8
vin4a_d16	-	-	F11	3	C18	8
vin4a_d17	-	-	G10	3	A21	8
vin4a_d18	-	-	F10	3	G16	8
vin4a_d19	-	-	G11	3	D17	8
vin4a_d20	-	-	E9	3	AA3	8
vin4a_d21	-	-	F9	3	AB9	8
vin4a_d22	-	-	F8	3	AB3	8
vin4a_d23	-	-	E7	3	AA4	8
vin4a_hsync0	R3/ P7	4 / 4	C11	3	E21	8
vin4a_vsync0	T2/ N1	4 / 4	E11	3	F20	8
vin4a_de0	H6/ P7	4 / 5	B10	3	C23	8
vin4a_fld0	P9/ J7	4 / 4	D11	3	F21	8
vin4a_clk0	P4	4	B11	3	B26	8
vin4b						
vin4b_clk1	N9	6	V1	5	-	-
vin4b_de1	P9	6	V7	5	-	-
vin4b_fld1	P4	6	W2	5	-	-
vin4b_d0	R6	6	U4	5	-	-
vin4b_d1	T9	6	V2	5	-	-
vin4b_d2	T6	6	Y1	5	-	-
vin4b_d3	T7	6	W9	5	-	-
vin4b_d4	P6	6	V9	5	-	-

Table 5-36. VIN4 IOSETs (continued)

Signals	IOSET1		IOSET2		IOSET3	
	BALL	MUX	BALL	MUX	BALL	MUX
vin4b_d5	R9	6	U5	5	-	-
vin4b_d6	R5	6	V5	5	-	-
vin4b_d7	P5	6	V4	5	-	-
vin4b_hsync1	N7	6	U7	5	-	-
vin4b_vsync1	R4	6	V6	5	-	-

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "*Manual IO Timing Modes*" of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information please see the *Control Module Chapter* in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for VIP1. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-37, *Manual Functions Mapping for VIP1* for a definition of the Manual modes.

Table 5-37 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-37. Manual Functions Mapping for VIP1

BALL	BALL NAME	VIP1_MANUAL1		VIP1_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
U3	RMII_MHZ_50_CLK	1973	184	2257	0	CFG_RMII_MHZ_50_CLK_IN	-	-	-	-	vin2a_d11
N6	gpmc_ben0	2133	486	2582	77	CFG_GPMC_BEN0_IN	-	-	-	vin1b_hsync1	-
M4	gpmc_ben1	2034	577	2545	109	CFG_GPMC_BEN1_IN	-	-	-	vin1b_de1	-
U4	mdio_d	1897	35	1999	0	CFG_MDIO_D_IN	-	-	-	-	vin2a_d0
V1	mdio_mclk	0	0	0	0	CFG_MDIO_MCLK_IN	-	-	-	-	vin2a_clk0
U5	rgmii0_rxc	1945	97	2072	0	CFG_RGMII0_RXC_IN	-	-	-	-	vin2a_d5
V5	rgmii0_rxctl	1939	440	2326	93	CFG_RGMII0_RXCTL_IN	-	-	-	-	vin2a_d6
W2	rgmii0_rxd0	1990	141	2147	0	CFG_RGMII0_RXD0_IN	-	-	-	-	vin2a_fld0
Y2	rgmii0_rxd1	1928	527	2298	246	CFG_RGMII0_RXD1_IN	-	-	-	-	vin2a_d9
V3	rgmii0_rxd2	1901	425	2280	134	CFG_RGMII0_RXD2_IN	-	-	-	-	vin2a_d8
V4	rgmii0_rxd3	1972	637	2331	362	CFG_RGMII0_RXD3_IN	-	-	-	-	vin2a_d7
W9	rgmii0_txc	1933	382	2347	28	CFG_RGMII0_TXC_IN	-	-	-	-	vin2a_d3
V9	rgmii0_txctl	2019	479	2372	217	CFG_RGMII0_TXCTL_IN	-	-	-	-	vin2a_d4
U6	rgmii0_txd0	1934	203	2205	0	CFG_RGMII0_TXD0_IN	-	-	-	-	vin2a_d10
V6	rgmii0_txd1	2015	604	2360	362	CFG_RGMII0_TXD1_IN	-	-	-	-	vin2a_vsync0
U7	rgmii0_txd2	1839	496	2249	158	CFG_RGMII0_TXD2_IN	-	-	-	-	vin2a_hsync0
V7	rgmii0_txd3	2087	423	2426	108	CFG_RGMII0_TXD3_IN	-	-	-	-	vin2a_de0
V2	uart3_rxd	1578	0	1530	0	CFG_UART3_RXD_IN	-	-	-	-	vin2a_d1
Y1	uart3_txd	1869	99	1967	0	CFG_UART3_TXD_IN	-	-	-	-	vin2a_d2
AG8	vin1a_clk0	0	0	0	0	CFG_VIN1A_CLK0_IN	vin1a_clk0	-	-	-	-
AE8	vin1a_d0	2051	708	2439	275	CFG_VIN1A_D0_IN	vin1a_d0	-	-	-	-
AD8	vin1a_d1	1931	812	2337	447	CFG_VIN1A_D1_IN	vin1a_d1	-	-	-	-
AG3	vin1a_d10	2049	804	2420	448	CFG_VIN1A_D10_IN	vin1a_d10	vin1b_d5	-	-	-
AG5	vin1a_d11	1921	766	2331	438	CFG_VIN1A_D11_IN	vin1a_d11	vin1b_d4	-	-	-
AF2	vin1a_d12	2078	1220	2397	915	CFG_VIN1A_D12_IN	vin1a_d12	vin1b_d3	-	-	-
AF6	vin1a_d13	1986	1138	2366	788	CFG_VIN1A_D13_IN	vin1a_d13	vin1b_d2	-	-	-
AF3	vin1a_d14	2077	1242	2403	947	CFG_VIN1A_D14_IN	vin1a_d14	vin1b_d1	-	-	-
AF4	vin1a_d15	2070	1581	2337	1407	CFG_VIN1A_D15_IN	vin1a_d15	vin1b_d0	-	-	-
AF1	vin1a_d16	2008	1432	2321	1202	CFG_VIN1A_D16_IN	vin1a_d16	vin1b_d7	-	-	-
AE3	vin1a_d17	2077	1571	2370	1351	CFG_VIN1A_D17_IN	vin1a_d17	vin1b_d6	-	-	-
AE5	vin1a_d18	2075	1527	2357	1292	CFG_VIN1A_D18_IN	vin1a_d18	vin1b_d5	-	-	-

Table 5-37. Manual Functions Mapping for VIP1 (continued)

BALL	BALL NAME	VIP1_MANUAL1		VIP1_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
AE1	vin1a_d19	2055	1636	2358	1422	CFG_VIN1A_D19_IN	vin1a_d19	vin1b_d4	-	-	-
AG7	vin1a_d2	1871	1037	2301	620	CFG_VIN1A_D2_IN	vin1a_d2	-	-	-	-
AE2	vin1a_d20	2046	1452	2351	1163	CFG_VIN1A_D20_IN	vin1a_d20	vin1b_d3	-	-	-
AE6	vin1a_d21	2135	1292	2405	1024	CFG_VIN1A_D21_IN	vin1a_d21	vin1b_d2	-	-	-
AD2	vin1a_d22	2034	1430	2348	1206	CFG_VIN1A_D22_IN	vin1a_d22	vin1b_d1	-	-	-
AD3	vin1a_d23	2191	813	2502	447	CFG_VIN1A_D23_IN	vin1a_d23	vin1b_d0	-	-	-
AH6	vin1a_d3	1938	984	2299	658	CFG_VIN1A_D3_IN	vin1a_d3	-	-	-	-
AH3	vin1a_d4	2034	597	2424	178	CFG_VIN1A_D4_IN	vin1a_d4	-	-	-	-
AH5	vin1a_d5	1961	927	2359	554	CFG_VIN1A_D5_IN	vin1a_d5	-	-	-	-
AG6	vin1a_d6	1909	930	2323	549	CFG_VIN1A_D6_IN	vin1a_d6	-	-	-	-
AH4	vin1a_d7	1999	901	2383	557	CFG_VIN1A_D7_IN	vin1a_d7	-	-	-	-
AG4	vin1a_d8	2040	856	2426	448	CFG_VIN1A_D8_IN	vin1a_d8	vin1b_d7	-	-	-
AG2	vin1a_d9	2133	799	2472	388	CFG_VIN1A_D9_IN	vin1a_d9	vin1b_d6	-	-	-
AD9	vin1a_de0	1842	861	2258	352	CFG_VIN1A_DE0_IN	vin1a_de0	vin1b_hsync1	-	-	-
AF9	vin1a_fld0	1968	1029	2347	622	CFG_VIN1A_FLD0_IN	vin1a_fld0	vin1b_vsync1	-	-	-
AE9	vin1a_hsync0	1871	1264	2257	881	CFG_VIN1A_HSYNC0_IN	vin1a_hsync0	vin1b_fld1	-	-	-
AF8	vin1a_vsync0	1798	1000	2243	649	CFG_VIN1A_VSYNC0_IN	vin1a_vsync0	vin1b_de1	-	-	-
AH7	vin1b_clk1	160	0	227	0	CFG_VIN1B_CLK1_IN	vin1b_clk1	-	-	-	-
E1	vin2a_clk0	0	0	0	0	CFG_VIN2A_CLK0_IN	vin2a_clk0	-	-	-	-
F2	vin2a_d0	1920	227	2180	0	CFG_VIN2A_D0_IN	vin2a_d0	-	-	-	-
F3	vin2a_d1	1957	476	2326	309	CFG_VIN2A_D1_IN	vin2a_d1	-	-	-	-
D3	vin2a_d10	1865	337	2297	110	CFG_VIN2A_D10_IN	vin2a_d10	-	-	-	-
F6	vin2a_d11	1753	19	1938	0	CFG_VIN2A_D11_IN	vin2a_d11	-	-	-	-
D5	vin2a_d12	1654	487	2135	182	CFG_VIN2A_D12_IN	vin2a_d12	-	-	-	-
C2	vin2a_d13	1927	132	2134	0	CFG_VIN2A_D13_IN	vin2a_d13	-	-	-	-
C3	vin2a_d14	1715	0	1753	0	CFG_VIN2A_D14_IN	vin2a_d14	-	-	-	-
C4	vin2a_d15	1745	381	2222	63	CFG_VIN2A_D15_IN	vin2a_d15	-	-	-	-
B2	vin2a_d16	1670	319	2137	58	CFG_VIN2A_D16_IN	vin2a_d16	-	vin2b_d7	-	-
D6	vin2a_d17	1709	409	2192	79	CFG_VIN2A_D17_IN	vin2a_d17	-	vin2b_d6	-	-
C5	vin2a_d18	2033	334	2378	21	CFG_VIN2A_D18_IN	vin2a_d18	-	vin2b_d5	-	-
A3	vin2a_d19	1957	193	2207	0	CFG_VIN2A_D19_IN	vin2a_d19	-	vin2b_d4	-	-
D1	vin2a_d2	1912	5	2057	0	CFG_VIN2A_D2_IN	vin2a_d2	-	-	-	-

Table 5-37. Manual Functions Mapping for VIP1 (continued)

BALL	BALL NAME	VIP1_MANUAL1		VIP1_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0	1	2	3	4
B3	vin2a_d20	1938	619	2325	388	CFG_VIN2A_D20_IN	vin2a_d20	-	vin2b_d3	-	-
B4	vin2a_d21	1899	546	2320	221	CFG_VIN2A_D21_IN	vin2a_d21	-	vin2b_d2	-	-
B5	vin2a_d22	1800	272	2219	30	CFG_VIN2A_D22_IN	vin2a_d22	-	vin2b_d1	-	-
A4	vin2a_d23	1807	476	2225	200	CFG_VIN2A_D23_IN	vin2a_d23	-	vin2b_d0	-	-
E2	vin2a_d3	2095	421	2440	257	CFG_VIN2A_D3_IN	vin2a_d3	-	-	-	-
D2	vin2a_d4	2008	0	2142	0	CFG_VIN2A_D4_IN	vin2a_d4	-	-	-	-
F4	vin2a_d5	2137	406	2455	252	CFG_VIN2A_D5_IN	vin2a_d5	-	-	-	-
C1	vin2a_d6	1717	0	1883	0	CFG_VIN2A_D6_IN	vin2a_d6	-	-	-	-
E4	vin2a_d7	1850	171	2229	0	CFG_VIN2A_D7_IN	vin2a_d7	-	-	-	-
F5	vin2a_d8	1841	340	2250	151	CFG_VIN2A_D8_IN	vin2a_d8	-	-	-	-
E6	vin2a_d9	1836	289	2279	27	CFG_VIN2A_D9_IN	vin2a_d9	-	-	-	-
G2	vin2a_de0	1772	316	2202	0	CFG_VIN2A_DE0_IN	vin2a_de0	vin2a_fld0	vin2b_fld1	vin2b_de1	-
H7	vin2a_fld0	2117	507	2453	357	CFG_VIN2A_FLD0_IN	vin2a_fld0	-	vin2b_clk1	-	-
G1	vin2a_hsync0	1969	231	2233	0	CFG_VIN2A_HSYNC0_IN	vin2a_hsync0	-	-	vin2b_hsync1	-
G6	vin2a_vsync0	1793	110	1936	0	CFG_VIN2A_VSYNC0_IN	vin2a_vsync0	-	-	vin2b_vsync1	-

Manual IO Timings Modes must be used to guarantee some IO timings for VIP1. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-38, *Manual Functions Mapping for VIP1 2B* for a definition of the Manual modes.

Table 5-38 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-38. Manual Functions Mapping for VIP1 2B

BALL	BALL NAME	VIP1_2B_MANUAL1		VIP1_2B_MANUAL2		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4
AC5	gpio6_10	2207	0	2288	0	CFG_GPIO6_10_IN	-	-	vin2b_hsync1
AB4	gpio6_11	2183	225	2486	77	CFG_GPIO6_11_IN	-	-	vin2b_vsync1
AD4	mmc3_clk	2262	114	2452	0	CFG_MMC3_CLK_IN	-	-	vin2b_d7
AC4	mmc3_cmd	2228	108	2425	0	CFG_MMC3_CMD_IN	-	-	vin2b_d6
AC7	mmc3_dat0	2137	170	2463	0	CFG_MMC3_DAT0_IN	-	-	vin2b_d5
AC6	mmc3_dat1	2116	154	2393	0	CFG_MMC3_DAT1_IN	-	-	vin2b_d4
AC9	mmc3_dat2	1891	0	1945	0	CFG_MMC3_DAT2_IN	-	-	vin2b_d3
AC3	mmc3_dat3	2202	197	2516	22	CFG_MMC3_DAT3_IN	-	-	vin2b_d2
AC8	mmc3_dat4	1966	0	1991	0	CFG_MMC3_DAT4_IN	-	-	vin2b_d1

Table 5-38. Manual Functions Mapping for VIP1 2B (continued)

BALL	BALL NAME	VIP1_2B_MANUAL1		VIP1_2B_MANUAL2		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4
AD6	mmc3_dat5	2163	15	2361	0	CFG_MMC3_DAT5_IN	-	-	vin2b_d0
AB8	mmc3_dat6	2162	51	2319	0	CFG_MMC3_DAT6_IN	-	-	vin2b_de1
AB5	mmc3_dat7	0	0	0	0	CFG_MMC3_DAT7_IN	-	-	vin2b_clk1
B2	vin2a_d16	1175	0	1413	0	CFG_VIN2A_D16_IN	vin2b_d7	-	-
D6	vin2a_d17	1323	0	1522	0	CFG_VIN2A_D17_IN	vin2b_d6	-	-
C5	vin2a_d18	1513	0	1580	0	CFG_VIN2A_D18_IN	vin2b_d5	-	-
A3	vin2a_d19	1278	0	1396	0	CFG_VIN2A_D19_IN	vin2b_d4	-	-
B3	vin2a_d20	1676	0	1895	0	CFG_VIN2A_D20_IN	vin2b_d3	-	-
B4	vin2a_d21	1610	0	1774	0	CFG_VIN2A_D21_IN	vin2b_d2	-	-
B5	vin2a_d22	1250	0	1497	0	CFG_VIN2A_D22_IN	vin2b_d1	-	-
A4	vin2a_d23	1434	0	1643	0	CFG_VIN2A_D23_IN	vin2b_d0	-	-
G2	vin2a_de0	1539	147	1793	0	CFG_VIN2A_DE0_IN	vin2b_fld1	vin2b_de1	-
H7	vin2a_fld0	0	0	0	0	CFG_VIN2A_FLD0_IN	vin2b_clk1	-	-
G1	vin2a_hsync0	1475	0	1542	0	CFG_VIN2A_HSYNC0_IN	-	vin2b_hsync1	-
G6	vin2a_vsync0	1163	0	1218	0	CFG_VIN2A_VSYNC0_IN	-	vin2b_vsync1	-

(1) The CFG_MMC3_CLK_IN register should remain at its Default value, which is programmed automatically by hardware during the recalibration process.

Manual IO Timings Modes must be used to guarantee some IO timings for VIP2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-39, *Manual Functions Mapping for VIP2* for a definition of the Manual modes.

Table 5-39 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-39. Manual Functions Mapping for VIP2

BALL	BALL NAME	VIP2_MANUAL 1		VIP2_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4	5	6
R6	gpmc_a0	2558	565	2920	260	CFG_GPMC_A0_IN	vin3a_d16	-	vin4a_d0	-	-
T9	gpmc_a1	2421	648	2782	349	CFG_GPMC_A1_IN	vin3a_d17	-	vin4a_d1	-	-
N9	gpmc_a10	2378	477	2765	0	CFG_GPMC_A10_IN	vin3a_de0	-	-	-	-
P9	gpmc_a11	2409	579	2783	295	CFG_GPMC_A11_IN	vin3a_fld0	-	vin4a_fld0	-	-
K7	gpmc_a19	1887	0	1735	0	CFG_GPMC_A19_IN	-	-	vin4a_d12	-	vin3b_d0
T6	gpmc_a2	2624	893	2882	682	CFG_GPMC_A2_IN	vin3a_d18	-	vin4a_d2	-	-
M7	gpmc_a20	1670	0	1508	0	CFG_GPMC_A20_IN	-	-	vin4a_d13	-	vin3b_d1
J5	gpmc_a21	1925	0	1763	0	CFG_GPMC_A21_IN	-	-	vin4a_d14	-	vin3b_d2

Table 5-39. Manual Functions Mapping for VIP2 (continued)

BALL	BALL NAME	VIP2_MANUAL 1		VIP2_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4	5	6
K6	gpmc_a22	1777	0	1631	0	CFG_GPMC_A22_IN	-	-	vin4a_d15	-	vin3b_d3
J7	gpmc_a23	1716	0	1717	0	CFG_GPMC_A23_IN	-	-	vin4a_fld0	-	vin3b_d4
J4	gpmc_a24	1758	111	1756	0	CFG_GPMC_A24_IN	-	-	-	-	vin3b_d5
J6	gpmc_a25	1805	0	1667	0	CFG_GPMC_A25_IN	-	-	-	-	vin3b_d6
H4	gpmc_a26	1800	54	1699	0	CFG_GPMC_A26_IN	-	-	-	-	vin3b_d7
H5	gpmc_a27	1661	0	1540	0	CFG_GPMC_A27_IN	-	-	-	-	vin3b_hsync1
T7	gpmc_a3	2589	902	2855	715	CFG_GPMC_A3_IN	vin3a_d19	-	vin4a_d3	-	-
P6	gpmc_a4	2616	808	2874	597	CFG_GPMC_A4_IN	vin3a_d20	-	vin4a_d4	-	-
R9	gpmc_a5	2514	733	2842	491	CFG_GPMC_A5_IN	vin3a_d21	-	vin4a_d5	-	-
R5	gpmc_a6	2511	417	2837	146	CFG_GPMC_A6_IN	vin3a_d22	-	vin4a_d6	-	-
P5	gpmc_a7	2752	618	3035	325	CFG_GPMC_A7_IN	vin3a_d23	-	vin4a_d7	-	-
N7	gpmc_a8	2457	603	2812	203	CFG_GPMC_A8_IN	vin3a_hsync0	-	-	-	-
R4	gpmc_a9	2536	749	2857	409	CFG_GPMC_A9_IN	vin3a_vsync0	-	-	-	-
M6	gpmc_ad0	2139	232	2444	0	CFG_GPMC_AD0_IN	vin3a_d0	-	-	-	-
M2	gpmc_ad1	2429	212	2711	0	CFG_GPMC_AD1_IN	vin3a_d1	-	-	-	-
J1	gpmc_ad10	2294	337	2703	16	CFG_GPMC_AD10_IN	vin3a_d10	-	-	-	-
J2	gpmc_ad11	2184	327	2600	0	CFG_GPMC_AD11_IN	vin3a_d11	-	-	-	-
H1	gpmc_ad12	2222	182	2471	0	CFG_GPMC_AD12_IN	vin3a_d12	-	-	-	-
J3	gpmc_ad13	2179	152	2421	0	CFG_GPMC_AD13_IN	vin3a_d13	-	-	-	-
H2	gpmc_ad14	2166	16	2263	0	CFG_GPMC_AD14_IN	vin3a_d14	-	-	-	-
H3	gpmc_ad15	2191	254	2535	0	CFG_GPMC_AD15_IN	vin3a_d15	-	-	-	-
L5	gpmc_ad2	2412	314	2776	41	CFG_GPMC_AD2_IN	vin3a_d2	-	-	-	-
M1	gpmc_ad3	2249	227	2503	0	CFG_GPMC_AD3_IN	vin3a_d3	-	-	-	-
L6	gpmc_ad4	2317	256	2613	0	CFG_GPMC_AD4_IN	vin3a_d4	-	-	-	-
L4	gpmc_ad5	2254	108	2441	0	CFG_GPMC_AD5_IN	vin3a_d5	-	-	-	-
L3	gpmc_ad6	2164	279	2533	0	CFG_GPMC_AD6_IN	vin3a_d6	-	-	-	-
L2	gpmc_ad7	2278	230	2597	0	CFG_GPMC_AD7_IN	vin3a_d7	-	-	-	-
L1	gpmc_ad8	2246	449	2701	84	CFG_GPMC_AD8_IN	vin3a_d8	-	-	-	-
K2	gpmc_ad9	2222	298	2607	0	CFG_GPMC_AD9_IN	vin3a_d9	-	-	-	-
N6	gpmc_ben0	1767	0	1686	0	CFG_GPMC_BEN0_IN	-	-	-	-	vin3b_de1
M4	gpmc_ben1	1838	0	1766	0	CFG_GPMC_BEN1_IN	-	-	vin3b_clk1	-	vin3b_fld1
P7	gpmc_clk	0	0	0	0	CFG_GPMC_CLK_IN	-	-	vin4a_hsync0	vin4a_de0	vin3b_clk1

Table 5-39. Manual Functions Mapping for VIP2 (continued)

BALL	BALL NAME	VIP2_MANUAL 1		VIP2_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4	5	6
H6	gpmc_cs1	1611	0	1450	0	CFG_GPMC_CS1_IN	-	-	vin4a_de0	-	vin3b_vsync1
P1	gpmc_cs3	0	0	0	0	CFG_GPMC_CS3_IN	vin3a_clk0	-	-	-	-
AF1	vin1a_d16	2152	1311	2633	790	CFG_VIN1A_D16_IN	-	-	-	-	vin3a_d0
AE3	vin1a_d17	2211	1381	2690	849	CFG_VIN1A_D17_IN	-	-	-	-	vin3a_d1
AE5	vin1a_d18	2220	1393	2669	879	CFG_VIN1A_D18_IN	-	-	-	-	vin3a_d2
AE1	vin1a_d19	2186	1418	2680	870	CFG_VIN1A_D19_IN	-	-	-	-	vin3a_d3
AE2	vin1a_d20	2183	1292	2666	707	CFG_VIN1A_D20_IN	-	-	-	-	vin3a_d4
AE6	vin1a_d21	2280	1155	2721	601	CFG_VIN1A_D21_IN	-	-	-	-	vin3a_d5
AD2	vin1a_d22	2144	1098	2664	517	CFG_VIN1A_D22_IN	-	-	-	-	vin3a_d6
AD3	vin1a_d23	2355	643	2816	0	CFG_VIN1A_D23_IN	-	-	-	-	vin3a_d7
AH7	vin1b_clk1	0	0	0	0	CFG_VIN1B_CLK1_IN	-	-	-	-	vin3a_clk0
B2	vin2a_d16	1624	239	1772	0	CFG_VIN2A_D16_IN	-	-	-	-	vin3a_d8
D6	vin2a_d17	1541	406	1838	0	CFG_VIN2A_D17_IN	-	-	-	-	vin3a_d9
C5	vin2a_d18	1942	313	2047	0	CFG_VIN2A_D18_IN	-	-	-	-	vin3a_d10
A3	vin2a_d19	1851	0	1667	0	CFG_VIN2A_D19_IN	-	-	-	-	vin3a_d11
B3	vin2a_d20	1837	430	2187	0	CFG_VIN2A_D20_IN	-	-	-	vin3a_de0	vin3a_d12
B4	vin2a_d21	1805	400	2042	0	CFG_VIN2A_D21_IN	-	-	-	vin3a_fld0	vin3a_d13
B5	vin2a_d22	1667	213	1786	0	CFG_VIN2A_D22_IN	-	-	-	vin3a_hsync0	vin3a_d14
A4	vin2a_d23	1700	408	2010	0	CFG_VIN2A_D23_IN	-	-	-	vin3a_vsync0	vin3a_d15
D11	vout1_clk	2405	379	2780	257	CFG_VOUT1_CLK_IN	-	vin4a_fld0	vin3a_fld0	-	-
F11	vout1_d0	2475	548	2806	469	CFG_VOUT1_D0_IN	-	vin4a_d16	vin3a_d16	-	-
G10	vout1_d1	2382	554	2771	418	CFG_VOUT1_D1_IN	-	vin4a_d17	vin3a_d17	-	-
D7	vout1_d10	2379	420	2784	267	CFG_VOUT1_D10_IN	-	vin4a_d10	vin3a_d10	-	-
D8	vout1_d11	2472	453	2810	367	CFG_VOUT1_D11_IN	-	vin4a_d11	vin3a_d11	-	-
A5	vout1_d12	2370	401	2777	247	CFG_VOUT1_D12_IN	-	vin4a_d12	vin3a_d12	-	-
C6	vout1_d13	2437	375	2819	229	CFG_VOUT1_D13_IN	-	vin4a_d13	vin3a_d13	-	-
C8	vout1_d14	2466	433	2785	342	CFG_VOUT1_D14_IN	-	vin4a_d14	vin3a_d14	-	-
C7	vout1_d15	2465	383	2846	255	CFG_VOUT1_D15_IN	-	vin4a_d15	vin3a_d15	-	-
B7	vout1_d16	2411	236	2733	167	CFG_VOUT1_D16_IN	-	vin4a_d0	vin3a_d0	-	-
B8	vout1_d17	2541	435	2840	379	CFG_VOUT1_D17_IN	-	vin4a_d1	vin3a_d1	-	-
A7	vout1_d18	2451	244	2761	186	CFG_VOUT1_D18_IN	-	vin4a_d2	vin3a_d2	-	-
A8	vout1_d19	2366	0	2564	0	CFG_VOUT1_D19_IN	-	vin4a_d3	vin3a_d3	-	-

Table 5-39. Manual Functions Mapping for VIP2 (continued)

BALL	BALL NAME	VIP2_MANUAL 1		VIP2_MANUAL2		CFG REGISTER	MUXMODE				
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		2	3	4	5	6
F10	vout1_d2	2373	639	2740	526	CFG_VOUT1_D2_IN	-	vin4a_d18	vin3a_d18	-	-
C9	vout1_d20	2381	578	2758	454	CFG_VOUT1_D20_IN	-	vin4a_d4	vin3a_d4	-	-
A9	vout1_d21	2349	104	2706	0	CFG_VOUT1_D21_IN	-	vin4a_d5	vin3a_d5	-	-
B9	vout1_d22	2372	248	2745	127	CFG_VOUT1_D22_IN	-	vin4a_d6	vin3a_d6	-	-
A10	vout1_d23	2088	392	2608	124	CFG_VOUT1_D23_IN	-	vin4a_d7	vin3a_d7	-	-
G11	vout1_d3	2475	523	2771	475	CFG_VOUT1_D3_IN	-	vin4a_d19	vin3a_d19	-	-
E9	vout1_d4	2481	458	2772	410	CFG_VOUT1_D4_IN	-	vin4a_d20	vin3a_d20	-	-
F9	vout1_d5	2335	451	2711	328	CFG_VOUT1_D5_IN	-	vin4a_d21	vin3a_d21	-	-
F8	vout1_d6	2485	461	2739	459	CFG_VOUT1_D6_IN	-	vin4a_d22	vin3a_d22	-	-
E7	vout1_d7	2496	514	2767	495	CFG_VOUT1_D7_IN	-	vin4a_d23	vin3a_d23	-	-
E8	vout1_d8	2459	492	2789	414	CFG_VOUT1_D8_IN	-	vin4a_d8	vin3a_d8	-	-
D9	vout1_d9	2463	532	2790	441	CFG_VOUT1_D9_IN	-	vin4a_d9	vin3a_d9	-	-
B10	vout1_de	2326	134	2713	0	CFG_VOUT1_DE_IN	-	vin4a_de0	vin3a_de0	-	-
B11	vout1_fld	0	0	0	0	CFG_VOUT1_FLD_IN	-	vin4a_clk0	vin3a_clk0	-	-
C11	vout1_hsync	2058	180	2456	0	CFG_VOUT1_HSYNC_IN	-	vin4a_hsync0	vin3a_hsync0	-	-
E11	vout1_vsync	2226	18	2332	0	CFG_VOUT1_VSYNC_IN	-	vin4a_vsync0	vin3a_vsync0	-	-

Manual IO Timings Modes must be used to guarantee some IO timings for VIP2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-40, *Manual Functions Mapping for VIP2 4A* for a definition of the Manual modes.

Table 5-40 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-40. Manual Functions Mapping for VIP2 4A

BALL	BALL NAME	VIP2_4A_MANUAL1		VIP2_4A_MANUAL2		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4	5
R6	gpmc_a0	2108	183	2229	0	CFG_GPMC_A0_IN	-	vin4a_d0	-
T9	gpmc_a1	1977	152	2082	0	CFG_GPMC_A1_IN	-	vin4a_d1	-
P9	gpmc_a11	1973	0	1964	0	CFG_GPMC_A11_IN	-	vin4a_fld0	-
P4	gpmc_a12	0	0	0	0	CFG_GPMC_A12_IN	-	vin4a_clk0	-
R3	gpmc_a13	2042	263	2251	0	CFG_GPMC_A13_IN	-	vin4a_hsync0	-
T2	gpmc_a14	2124	726	2678	158	CFG_GPMC_A14_IN	-	vin4a_vsync0	-
U2	gpmc_a15	1922	307	2226	0	CFG_GPMC_A15_IN	-	vin4a_d8	-
U1	gpmc_a16	2082	318	2340	0	CFG_GPMC_A16_IN	-	vin4a_d9	-

Table 5-40. Manual Functions Mapping for VIP2 4A (continued)

BALL	BALL NAME	VIP2_4A_MANUAL1		VIP2_4A_MANUAL2		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4	5
P3	gpmc_a17	1987	328	2216	0	CFG_GPMC_A17_IN	-	vin4a_d10	-
R2	gpmc_a18	1428	0	1323	0	CFG_GPMC_A18_IN	-	vin4a_d11	-
K7	gpmc_a19	1755	0	1599	0	CFG_GPMC_A19_IN	-	vin4a_d12	-
T6	gpmc_a2	2202	359	2518	0	CFG_GPMC_A2_IN	-	vin4a_d2	-
M7	gpmc_a20	1561	0	1394	0	CFG_GPMC_A20_IN	-	vin4a_d13	-
J5	gpmc_a21	1795	41	1665	0	CFG_GPMC_A21_IN	-	vin4a_d14	-
K6	gpmc_a22	1637	0	1454	0	CFG_GPMC_A22_IN	-	vin4a_d15	-
J7	gpmc_a23	1489	0	1492	0	CFG_GPMC_A23_IN	-	vin4a_fld0	-
T7	gpmc_a3	2131	389	2502	0	CFG_GPMC_A3_IN	-	vin4a_d3	-
P6	gpmc_a4	2179	275	2403	0	CFG_GPMC_A4_IN	-	vin4a_d4	-
R9	gpmc_a5	2013	281	2248	0	CFG_GPMC_A5_IN	-	vin4a_d5	-
R5	gpmc_a6	1989	0	1920	0	CFG_GPMC_A6_IN	-	vin4a_d6	-
P5	gpmc_a7	2338	106	2348	0	CFG_GPMC_A7_IN	-	vin4a_d7	-
N1	gpmc_advn_ale	1960	0	1927	0	CFG_GPMC_ADVN_ALE_IN	-	vin4a_vsync0	-
P7	gpmc_clk	1941	0	1901	0	CFG_GPMC_CLK_IN	-	vin4a_hsync0	vin4a_de0
H6	gpmc_cs1	1412	0	1282	0	CFG_GPMC_CS1_IN	-	vin4a_de0	-
D11	vout1_clk	2425	88	2765	20	CFG_VOUT1_CLK_IN	vin4a_fld0	-	-
F11	vout1_d0	2460	555	2772	515	CFG_VOUT1_D0_IN	vin4a_d16	-	-
G10	vout1_d1	2307	500	2725	354	CFG_VOUT1_D1_IN	vin4a_d17	-	-
D7	vout1_d10	2367	275	2755	160	CFG_VOUT1_D10_IN	vin4a_d10	-	-
D8	vout1_d11	2480	337	2788	301	CFG_VOUT1_D11_IN	vin4a_d11	-	-
A5	vout1_d12	2344	290	2744	162	CFG_VOUT1_D12_IN	vin4a_d12	-	-
C6	vout1_d13	2381	184	2779	56	CFG_VOUT1_D13_IN	vin4a_d13	-	-
C8	vout1_d14	2459	533	2752	512	CFG_VOUT1_D14_IN	vin4a_d14	-	-
C7	vout1_d15	2386	263	2811	111	CFG_VOUT1_D15_IN	vin4a_d15	-	-
B7	vout1_d16	2378	197	2705	142	CFG_VOUT1_D16_IN	vin4a_d0	-	-
B8	vout1_d17	2538	171	2837	133	CFG_VOUT1_D17_IN	vin4a_d1	-	-
A7	vout1_d18	2433	69	2749	25	CFG_VOUT1_D18_IN	vin4a_d2	-	-
A8	vout1_d19	2158	0	2412	0	CFG_VOUT1_D19_IN	vin4a_d3	-	-
F10	vout1_d2	2401	291	2753	211	CFG_VOUT1_D2_IN	vin4a_d18	-	-
C9	vout1_d20	2361	401	2741	295	CFG_VOUT1_D20_IN	vin4a_d4	-	-
A9	vout1_d21	2181	0	2454	0	CFG_VOUT1_D21_IN	vin4a_d5	-	-

Table 5-40. Manual Functions Mapping for VIP2 4A (continued)

BALL	BALL NAME	VIP2_4A_MANUAL1		VIP2_4A_MANUAL2		CFG REGISTER	MUXMODE		
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4	5
B9	vout1_d22	2276	0	2548	0	CFG_VOUT1_D22_IN	vin4a_d6	-	-
A10	vout1_d23	2070	274	2591	26	CFG_VOUT1_D23_IN	vin4a_d7	-	-
G11	vout1_d3	2419	403	2749	341	CFG_VOUT1_D3_IN	vin4a_d19	-	-
E9	vout1_d4	2465	311	2754	294	CFG_VOUT1_D4_IN	vin4a_d20	-	-
F9	vout1_d5	2306	319	2696	201	CFG_VOUT1_D5_IN	vin4a_d21	-	-
F8	vout1_d6	2450	312	2716	318	CFG_VOUT1_D6_IN	vin4a_d22	-	-
E7	vout1_d7	2477	403	2747	405	CFG_VOUT1_D7_IN	vin4a_d23	-	-
E8	vout1_d8	2407	425	2744	360	CFG_VOUT1_D8_IN	vin4a_d8	-	-
D9	vout1_d9	2512	277	2783	278	CFG_VOUT1_D9_IN	vin4a_d9	-	-
B10	vout1_de	2266	36	2576	0	CFG_VOUT1_DE_IN	vin4a_de0	-	-
B11	vout1_fld	0	0	0	0	CFG_VOUT1_FLD_IN	vin4a_clk0	-	-
C11	vout1_hsync	2016	50	2300	0	CFG_VOUT1_HSYNC_IN	vin4a_hsync0	-	-
E11	vout1_vsync	1953	0	2088	0	CFG_VOUT1_VSYNC_IN	vin4a_vsync0	-	-

Manual IO Timings Modes must be used to guarantee some IO timings for VIP2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-41, *Manual Functions Mapping for VIP2 4A IOSET3* for a definition of the Manual modes.

Table 5-41 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-41. Manual Functions Mapping for VIP2 4A IOSET3

BALL	BALL NAME	VIP2_4A_IOSET3_MANUAL1		VIP2_4A_IOSET3_MANUAL2		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		8
E21	gpio6_14	599	0	901	0	CFG_GPIO6_14_IN	vin4a_hsync0
F20	gpio6_15	1291	0	1593	0	CFG_GPIO6_15_IN	vin4a_vsync0
F21	gpio6_16	926	0	1228	0	CFG_GPIO6_16_IN	vin4a_fld0
B14	mcasp1_aclkr	1768	0	2071	0	CFG_MCASP1_ACLKR_IN	vin4a_d0
G13	mcasp1_axr2	2326	851	2737	792	CFG_MCASP1_AXR2_IN	vin4a_d2
J11	mcasp1_axr3	2406	562	2858	434	CFG_MCASP1_AXR3_IN	vin4a_d3
E12	mcasp1_axr4	2219	678	2742	464	CFG_MCASP1_AXR4_IN	vin4a_d4
F13	mcasp1_axr5	2226	676	2728	517	CFG_MCASP1_AXR5_IN	vin4a_d5
C12	mcasp1_axr6	2265	510	2806	271	CFG_MCASP1_AXR6_IN	vin4a_d6
D12	mcasp1_axr7	2302	781	2708	726	CFG_MCASP1_AXR7_IN	vin4a_d7
J14	mcasp1_fsr	1901	184	2386	0	CFG_MCASP1_FSR_IN	vin4a_d1

Table 5-41. Manual Functions Mapping for VIP2 4A IOSET3 (continued)

BALL	BALL NAME	VIP2_4A_IOSET3_MANUAL1		VIP2_4A_IOSET3_MANUAL2		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		8
E15	mcasp2_aclkr	1555	0	1857	0	CFG_MCASP2_ACLKR_IN	vin4a_d8
B15	mcasp2_axr0	1790	658	2407	343	CFG_MCASP2_AXR0_IN	vin4a_d10
A15	mcasp2_axr1	1939	279	2527	0	CFG_MCASP2_AXR1_IN	vin4a_d11
D15	mcasp2_axr4	1924	369	2541	53	CFG_MCASP2_AXR4_IN	vin4a_d12
B16	mcasp2_axr5	1719	400	2337	84	CFG_MCASP2_AXR5_IN	vin4a_d13
B17	mcasp2_axr6	1116	0	1418	0	CFG_MCASP2_AXR6_IN	vin4a_d14
A17	mcasp2_axr7	1477	362	2094	47	CFG_MCASP2_AXR7_IN	vin4a_d15
A20	mcasp2_fsr	1521	8	1830	0	CFG_MCASP2_FSR_IN	vin4a_d9
C18	mcasp4_aclkx	1258	0	1418	0	CFG_MCASP4_ACLKX_IN	vin4a_d16
G16	mcasp4_axr0	2334	227	2813	26	CFG_MCASP4_AXR0_IN	vin4a_d18
D17	mcasp4_axr1	2334	529	2777	437	CFG_MCASP4_AXR1_IN	vin4a_d19
A21	mcasp4_fsx	2293	0	2570	0	CFG_MCASP4_FSX_IN	vin4a_d17
AA3	mcasp5_aclkx	3053	2527	3352	2409	CFG_MCASP5_ACLKX_IN	vin4a_d20
AB3	mcasp5_axr0	3058	3254	3315	3285	CFG_MCASP5_AXR0_IN	vin4a_d22
AA4	mcasp5_axr1	3090	3358	3331	3446	CFG_MCASP5_AXR1_IN	vin4a_d23
AB9	mcasp5_fsx	3060	2699	3329	2686	CFG_MCASP5_FSX_IN	vin4a_d21
B26	xref_clk2	0	0	0	0	CFG_XREF_CLK2_IN	vin4a_clk0
C23	xref_clk3	962	0	1265	0	CFG_XREF_CLK3_IN	vin4a_de0

Manual IO Timings Modes must be used to guarantee some IO timings for VIP2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-42, *Manual Functions Mapping for VIP2 4B* for a definition of the Manual modes.

Table 5-42 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-42. Manual Functions Mapping for VIP2 4B

BALL	BALL NAME	VIP2_4B_MANUAL1		VIP2_4B_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		5	6
R6	gpmc_a0	2199	621	2416	398	CFG_GPMC_A0_IN	-	vin4b_d0
T9	gpmc_a1	1989	612	2267	323	CFG_GPMC_A1_IN	-	vin4b_d1
N9	gpmc_a10	0	0	0	0	CFG_GPMC_A10_IN	-	vin4b_clk1
P9	gpmc_a11	2133	859	2303	720	CFG_GPMC_A11_IN	-	vin4b_de1
P4	gpmc_a12	2258	562	2399	393	CFG_GPMC_A12_IN	-	vin4b_fld1
T6	gpmc_a2	2218	912	2365	720	CFG_GPMC_A2_IN	-	vin4b_d2

Table 5-42. Manual Functions Mapping for VIP2 4B (continued)

BALL	BALL NAME	VIP2_4B_MANUAL1		VIP2_4B_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		5	6
T7	gpmc_a3	2168	963	2341	781	CFG_GPMC_A3_IN	-	vin4b_d3
P6	gpmc_a4	2196	813	2362	594	CFG_GPMC_A4_IN	-	vin4b_d4
R9	gpmc_a5	2082	782	2329	525	CFG_GPMC_A5_IN	-	vin4b_d5
R5	gpmc_a6	2098	407	2320	171	CFG_GPMC_A6_IN	-	vin4b_d6
P5	gpmc_a7	2343	585	2522	305	CFG_GPMC_A7_IN	-	vin4b_d7
N7	gpmc_a8	2030	685	2290	284	CFG_GPMC_A8_IN	-	vin4b_hsync1
R4	gpmc_a9	2116	832	2335	548	CFG_GPMC_A9_IN	-	vin4b_vsync1
U4	mdio_d	1860	189	2164	0	CFG_MDIO_D_IN	vin4b_d0	-
V1	mdio_mclk	0	0	0	0	CFG_MDIO_MCLK_IN	vin4b_clk1	-
U5	rgmii0_rxc	1965	550	2306	279	CFG_RGMII0_RXC_IN	vin4b_d5	-
V5	rgmii0_rxctl	1911	605	2235	369	CFG_RGMII0_RXCTL_IN	vin4b_d6	-
W2	rgmii0_rxd0	1954	304	2294	26	CFG_RGMII0_RXD0_IN	vin4b_fld1	-
V4	rgmii0_rxd3	1925	835	2252	613	CFG_RGMII0_RXD3_IN	vin4b_d7	-
W9	rgmii0_txc	1937	849	2291	633	CFG_RGMII0_TXC_IN	vin4b_d3	-
V9	rgmii0_txctl	1997	872	2272	744	CFG_RGMII0_TXCTL_IN	vin4b_d4	-
V6	rgmii0_txd1	1989	771	2264	643	CFG_RGMII0_TXD1_IN	vin4b_vsync1	-
U7	rgmii0_txd2	1788	682	2193	334	CFG_RGMII0_TXD2_IN	vin4b_hsync1	-
V7	rgmii0_txd3	2091	591	2345	411	CFG_RGMII0_TXD3_IN	vin4b_de1	-
V2	uart3_rxd	1711	0	1699	0	CFG_UART3_RXD_IN	vin4b_d1	-
Y1	uart3_txd	1830	318	2176	0	CFG_UART3_TXD_IN	vin4b_d2	-

Manual IO Timings Modes must be used to guarantee some IO timings for VIP2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-43, *Manual Functions Mapping for VIP2 3B IOSET2* for a definition of the Manual modes.

Table 5-43 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-43. Manual Functions Mapping for VIP2 3B IOSET2

BALL	BALL NAME	VIP2_3B_IOSET2_MANUAL1		VIP2_3B_IOSET2_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4	6
K7	gpmc_a19	1801	826	2145	501	CFG_GPMC_A19_IN	-	vin3b_d0
M7	gpmc_a20	1706	697	2037	373	CFG_GPMC_A20_IN	-	vin3b_d1
J5	gpmc_a21	1767	937	2101	612	CFG_GPMC_A21_IN	-	vin3b_d2
K6	gpmc_a22	1678	895	1998	584	CFG_GPMC_A22_IN	-	vin3b_d3

Table 5-43. Manual Functions Mapping for VIP2 3B IOSET2 (continued)

BALL	BALL NAME	VIP2_3B_IOSET2_MANUAL1		VIP2_3B_IOSET2_MANUAL2		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4	6
J7	gpmc_a23	1680	769	2016	619	CFG_GPMC_A23_IN	-	vin3b_d4
J4	gpmc_a24	1585	1015	1931	690	CFG_GPMC_A24_IN	-	vin3b_d5
J6	gpmc_a25	1643	893	2001	531	CFG_GPMC_A25_IN	-	vin3b_d6
H4	gpmc_a26	1627	958	1978	586	CFG_GPMC_A26_IN	-	vin3b_d7
H5	gpmc_a27	1709	686	2036	412	CFG_GPMC_A27_IN	-	vin3b_hsync1
N6	gpmc_ben0	1993	579	2297	340	CFG_GPMC_BEN0_IN	-	vin3b_de1
M4	gpmc_ben1	0	0	0	0	CFG_GPMC_BEN1_IN	vin3b_clk1	vin3b_fld1
H6	gpmc_cs1	1492	850	1829	486	CFG_GPMC_CS1_IN	-	vin3b_vsync1

5.10.6.4 DSS

Three Display Parallel Interfaces (DPI) channels are available in DSS named DPI Video Output 1, DPI Video Output 2 and DPI Video Output 3.

NOTE

The DPI Video Output i (i = 1 to 3) interface is also referred to as VOUTi.

Every VOUT interface consists of:

- 24-bit data bus (data[23:0])
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Field ID (FID)
- Pixel clock (CLK)

NOTE

For more information, see the Display Subsystem chapter of the Device TRM.

CAUTION

The I/O timings provided in this section are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 5-48 and Table 5-49.

CAUTION

The I/O Timings provided in this section are valid only for some DSS usage modes when the corresponding Virtual I/O Timings or Manual I/O Timings are configured as described in the tables found in this section.

CAUTION

All pads/balls configured as vouti_* signals are recommended to use slow slew rate by setting the corresponding CTRL_CORE_PAD_*[SLEWCONTROL] register field to SLOW (0b1). FAST slew setting is allowed, but results in faster edge rates on the VOUTn bus, higher power/ground noise, and higher EMI emissions compared to SLOW slew rate.

Table 5-44, Table 5-45 and Figure 5-27 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-44. DPI Video Output i (i = 1..3) Default Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock vouti_clk		11.76 (2)		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock vouti_clk low		P*0.5-1 (1)		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock vouti_clk high		P*0.5-1 (1)		ns

Table 5-44. DPI Video Output i (i = 1..3) Default Switching Characteristics (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D5	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid		-2.5	2.5	ns
D6	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid		-2.5	2.5	ns

(1) P = output vouti_clk period in ns.

(2) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note **SPRAC62** for additional guidance.

Table 5-45. DPI Video Output i (i = 1..3) Alternate Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock vouti_clk		6.06 (2)		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock vouti_clk low		P*0.5-1 (1)		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock vouti_clk high		P*0.5-1 (1)		ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid		1.51	4.55	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid		1.51	4.55	ns

(1) P = output vouti_clk period in ns.

(2) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note **SPRAC62** for additional guidance.

Table 5-46. DPI Video Output i (i = 1..3) MANUAL3 Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock vouti_clk		6.06 (2)		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock vouti_clk low		P*0.5-1 (1)		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock vouti_clk high		P*0.5-1 (1)		ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid		2.85	5.56	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid		2.85	5.56	ns

(1) P = output vouti_clk period in ns.

(2) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note **SPRAC62** for additional guidance.

Table 5-47. DPI Video Output i (i = 1..3) MANUAL4 Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{c(clk)}$	Cycle time, output pixel clock vouti_clk		6.06 (2)		ns
D2	$t_{w(clkL)}$	Pulse duration, output pixel clock vouti_clk low		P*0.5-1 (1)		ns
D3	$t_{w(clkH)}$	Pulse duration, output pixel clock vouti_clk high		P*0.5-1 (1)		ns
D5	$t_{d(clk-ctlV)}$	Delay time, output pixel clock vouti_clk transition to output data vouti_d[23:0] valid		3.55	6.61	ns
D6	$t_{d(clk-dV)}$	Delay time, output pixel clock vouti_clk transition to output control signals vouti_vsync, vouti_hsync, vouti_de, and vouti_fld valid		3.55	6.61	ns

(1) P = output vouti_clk period in ns.
(2) SERDES transceivers may be sensitive to the jitter profile of vouti_clk. See Application Note **SPRAC62** for additional guidance.

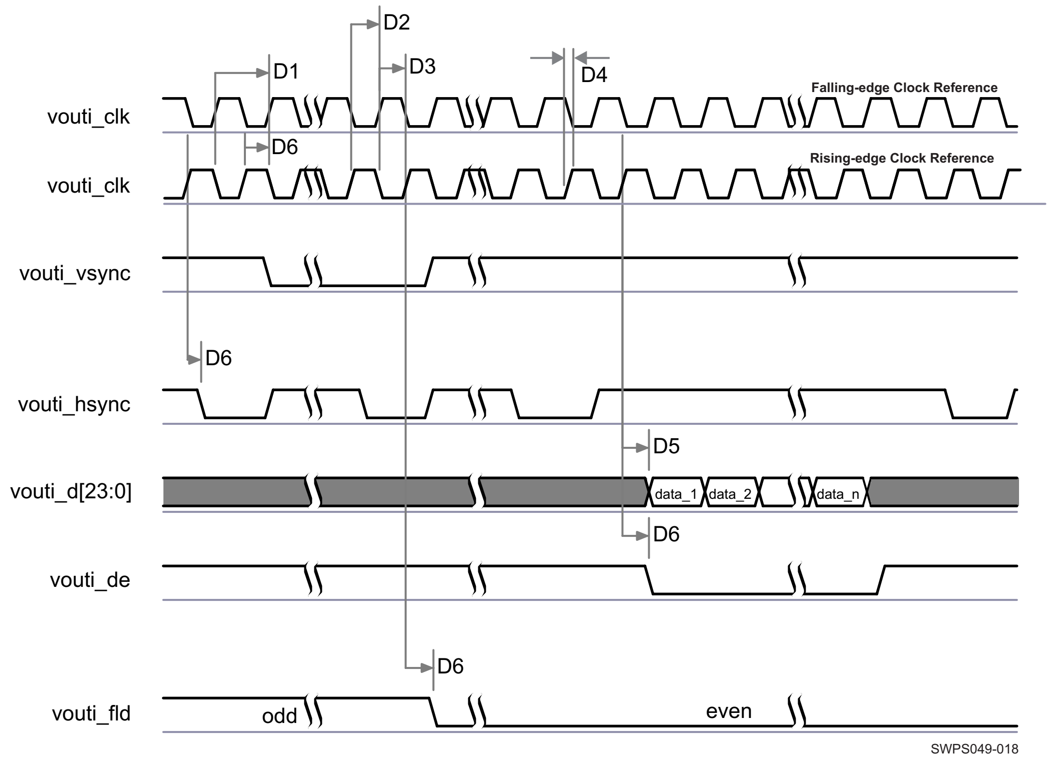


Figure 5-27. DPI Video Output(1)(2)(3)

(1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
(2) The polarity and the pulse width of vouti_hsync and vouti_vsync are programmable, refer to the DSS section of the Device TRM.
(3) The vouti_clk frequency can be configured, refer to the DSS section of the Device TRM.

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presentsed Table 4-29 and described in Device TRM, *Control Module Chapter*.

In Table 5-48 are presented the specific groupings of signals (IOSET) for use with VOUT2.

Table 5-48. VOUT2 IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
vout2_d23	F2	4	AA4	6
vout2_d22	F3	4	AB3	6
vout2_d21	D1	4	AB9	6
vout2_d20	E2	4	AA3	6
vout2_d19	D2	4	D17	6
vout2_d18	F4	4	G16	6
vout2_d17	C1	4	A21	6
vout2_d16	E4	4	C18	6
vout2_d15	F5	4	A17	6

Table 5-48. VOUT2 IOSETs (continued)

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
vout2_d14	E6	4	B17	6
vout2_d13	D3	4	B16	6
vout2_d12	F6	4	D15	6
vout2_d11	D5	4	A15	6
vout2_d10	C2	4	B15	6
vout2_d9	C3	4	A20	6
vout2_d8	C4	4	E15	6
vout2_d7	B2	4	D12	6
vout2_d6	D6	4	C12	6
vout2_d5	C5	4	F13	6
vout2_d4	A3	4	E12	6
vout2_d3	B3	4	J11	6
vout2_d2	B4	4	G13	6
vout2_d1	B5	4	J14	6
vout2_d0	A4	4	B14	6
vout2_vsync	G6	4	F20	6
vout2_hsync	G1	4	E21	6
vout2_clk	H7	4	B26	6
vout2_fld	E1	4	F21	6
vout2_de	G2	4	C23	6

In Table 5-49 are presented the specific groupings of signals (IOSET) for use with VOUT3.

Table 5-49. VOUT3 IOSETs

SIGNALS	IOSET1		IOSET2		IOSET3	
	BALL	MUX	BALL	MUX	BALL	MUX
vout3_d23	P5	3	AE8	4		
vout3_d22	R5	3	AD8	4		
vout3_d21	R9	3	AG7	4		
vout3_d20	P6	3	AH6	4		
vout3_d19	T7	3	AH3	4		
vout3_d18	T6	3	AH5	4		
vout3_d17	T9	3	AG6	4	AD9	3
vout3_d16	R6	3	AH4	4	AG8	3
vout3_d15	H3	3	AG4	4	AG4	4
vout3_d14	H2	3	AG2	4	AG2	4
vout3_d13	J3	3	AG3	4	AG3	4
vout3_d12	H1	3	AG5	4	AG5	4
vout3_d11	J2	3	AF2	4	AF2	4
vout3_d10	J1	3	AF6	4	AF6	4
vout3_d9	K2	3	AF3	4	AF3	4
vout3_d8	L1	3	AF4	4	AF4	4
vout3_d7	L2	3	AF1	4	AE8	3
vout3_d6	L3	3	AE3	4	AD8	3
vout3_d5	L4	3	AE5	4	AG7	3
vout3_d4	L6	3	AE1	4	AH6	3
vout3_d3	M1	3	AE2	4	AH3	3

Table 5-49. VOUT3 IOSETs (continued)

SIGNALS	IOSET1		IOSET2		IOSET3	
	BALL	MUX	BALL	MUX	BALL	MUX
vout3_d2	L5	3	AE6	4	AH5	3
vout3_d1	M2	3	AD2	4	AG6	3
vout3_d0	M6	3	AD3	4	AH4	3
vout3_de	N9	3	AD9	4		
vout3_vsync	R4	3	AF8	4	AF8	4
vout3_clk	P1	3	AF9	4	AF9	4
vout3_hsync	N7	3	AE9	4	AE9	4
vout3_fld	P9	3	AG8	4		

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section *"Manual IO Timing Modes"* of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information please see the *Control Module Chapter* in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for VOUT1. See Table 5-32 *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-50 *Manual Functions Mapping for DSS VOUT1* for a definition of the Manual modes.

Table 5-50 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-50. Manual Functions Mapping for DSS VOUT1

BALL	BALL NAME	VOUT1_MANUAL1		VOUT1_MANUAL2		VOUT1_MANUAL3		VOUT1_MANUAL4		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0
D11	vout1_clk	0	29	1281	497	0	0	0	0	CFG_VOUT1_CLK_OUT	vout1_clk
F11	vout1_d0	1878	0	379	0	3126	0	4185	0	CFG_VOUT1_D0_OUT	vout1_d0
G10	vout1_d1	1978	0	475	0	3226	0	4284	0	CFG_VOUT1_D1_OUT	vout1_d1
D7	vout1_d10	1943	0	441	0	3191	0	4249	0	CFG_VOUT1_D10_OUT	vout1_d10
D8	vout1_d11	1964	0	461	0	3212	0	4271	0	CFG_VOUT1_D11_OUT	vout1_d11
A5	vout1_d12	2726	0	1189	0	3974	0	5033	0	CFG_VOUT1_D12_OUT	vout1_d12
C6	vout1_d13	1807	0	312	0	3055	0	4114	0	CFG_VOUT1_D13_OUT	vout1_d13
C8	vout1_d14	1793	0	298	0	3041	0	4099	0	CFG_VOUT1_D14_OUT	vout1_d14
C7	vout1_d15	1778	0	284	0	3026	0	4085	0	CFG_VOUT1_D15_OUT	vout1_d15
B7	vout1_d16	1652	0	152	0	2887	0	3946	0	CFG_VOUT1_D16_OUT	vout1_d16
B8	vout1_d17	1706	0	216	0	2954	0	4013	0	CFG_VOUT1_D17_OUT	vout1_d17
A7	vout1_d18	1908	0	408	0	3156	0	4215	0	CFG_VOUT1_D18_OUT	vout1_d18
A8	vout1_d19	2024	0	519	0	3272	0	4330	0	CFG_VOUT1_D19_OUT	vout1_d19
F10	vout1_d2	1757	0	264	0	3005	0	4064	0	CFG_VOUT1_D2_OUT	vout1_d2
C9	vout1_d20	1811	0	316	0	3059	0	4118	0	CFG_VOUT1_D20_OUT	vout1_d20
A9	vout1_d21	1640	0	59	0	2814	0	3850	0	CFG_VOUT1_D21_OUT	vout1_d21
B9	vout1_d22	1712	0	221	0	2960	0	4019	0	CFG_VOUT1_D22_OUT	vout1_d22
A10	vout1_d23	1581	0	96	0	2829	0	3888	0	CFG_VOUT1_D23_OUT	vout1_d23
G11	vout1_d3	1921	0	421	0	3169	0	4228	0	CFG_VOUT1_D3_OUT	vout1_d3
E9	vout1_d4	2797	0	1257	0	4045	0	5104	0	CFG_VOUT1_D4_OUT	vout1_d4
F9	vout1_d5	1933	0	432	0	3181	0	4240	0	CFG_VOUT1_D5_OUT	vout1_d5
F8	vout1_d6	1937	0	436	0	3185	0	4244	0	CFG_VOUT1_D6_OUT	vout1_d6
E7	vout1_d7	1941	0	440	0	3189	0	4248	0	CFG_VOUT1_D7_OUT	vout1_d7
E8	vout1_d8	1701	0	81	100	2918	0	3977	0	CFG_VOUT1_D8_OUT	vout1_d8
D9	vout1_d9	1973	0	471	0	3221	0	4280	0	CFG_VOUT1_D9_OUT	vout1_d9
B10	vout1_de	1573	0	0	0	2747	0	3725	0	CFG_VOUT1_DE_OUT	vout1_de
B11	vout1_fld	1709	0	224	0	2983	0	4004	0	CFG_VOUT1_FLD_OUT	vout1_fld
C11	vout1_hsync	1514	0	0	0	2688	0	3666	0	CFG_VOUT1_HSYNC_OUT	vout1_hsync
E11	vout1_vsync	2316	0	815	0	3564	0	4623	0	CFG_VOUT1_VSYNC_OUT	vout1_vsync

Manual IO Timings Modes must be used to guarantee some IO timings for VOUT2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-51, *Manual Functions Mapping for DSS VOUT2* for a definition of the Manual modes.

Table 5-51 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-51. Manual Functions Mapping for DSS VOUT2 IOSET1

BALL	BALL NAME	VOUT2_IOSET1 _MANUAL1		VOUT2_IOSET1 _MANUAL2		VOUT2_IOSET1 _MANUAL3		VOUT2_IOSET1 _MANUAL4		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4
E1	vin2a_clk0	2587	0	1178	0	3748	0	4694	0	CFG_VIN2A_CLK0_OUT	vout2_fld
F2	vin2a_d0	2199	0	449	337	3360	0	4306	0	CFG_VIN2A_D0_OUT	vout2_d23
F3	vin2a_d1	2141	0	731	0	3302	0	4248	0	CFG_VIN2A_D1_OUT	vout2_d22
D3	vin2a_d10	1449	0	261	0	2810	0	3756	0	CFG_VIN2A_D10_OUT	vout2_d13
F6	vin2a_d11	2010	0	425	181	3171	0	4117	0	CFG_VIN2A_D11_OUT	vout2_d12
D5	vin2a_d12	2487	291	1649	73	3864	475	4680	605	CFG_VIN2A_D12_OUT	vout2_d11
C2	vin2a_d13	2235	363	1594	148	3812	548	4629	677	CFG_VIN2A_D13_OUT	vout2_d10
C3	vin2a_d14	2211	364	1456	167	3688	548	4504	678	CFG_VIN2A_D14_OUT	vout2_d9
C4	vin2a_d15	2462	128	1542	0	3839	312	4656	441	CFG_VIN2A_D15_OUT	vout2_d8
B2	vin2a_d16	2396	56	1554	0	3923	240	4740	370	CFG_VIN2A_D16_OUT	vout2_d7
D6	vin2a_d17	2426	130	1510	0	3803	314	4620	444	CFG_VIN2A_D17_OUT	vout2_d6
C5	vin2a_d18	2022	0	617	0	3183	0	4129	0	CFG_VIN2A_D18_OUT	vout2_d5
A3	vin2a_d19	1826	0	430	0	2987	0	3933	0	CFG_VIN2A_D19_OUT	vout2_d4
D1	vin2a_d2	1973	0	571	0	3134	0	4080	0	CFG_VIN2A_D2_OUT	vout2_d21
B3	vin2a_d20	1514	0	110	0	2668	0	3618	0	CFG_VIN2A_D20_OUT	vout2_d3
B4	vin2a_d21	1454	0	36	0	2608	0	3558	0	CFG_VIN2A_D21_OUT	vout2_d2
B5	vin2a_d22	1432	0	0	0	2586	0	3536	0	CFG_VIN2A_D22_OUT	vout2_d1
A4	vin2a_d23	1452	0	20	0	2606	0	3556	0	CFG_VIN2A_D23_OUT	vout2_d0
E2	vin2a_d3	2007	0	603	0	3168	0	4114	0	CFG_VIN2A_D3_OUT	vout2_d20
D2	vin2a_d4	2306	0	1366	0	3967	0	4913	0	CFG_VIN2A_D4_OUT	vout2_d19
F4	vin2a_d5	2122	0	904	0	3483	0	4429	0	CFG_VIN2A_D5_OUT	vout2_d18
C1	vin2a_d6	1867	0	660	0	3228	0	4174	0	CFG_VIN2A_D6_OUT	vout2_d17
E4	vin2a_d7	1940	0	539	0	3101	0	4047	0	CFG_VIN2A_D7_OUT	vout2_d16
F5	vin2a_d8	1752	0	359	0	2913	0	3859	0	CFG_VIN2A_D8_OUT	vout2_d15
E6	vin2a_d9	1631	0	46	198	2792	0	3738	0	CFG_VIN2A_D9_OUT	vout2_d14
G2	vin2a_de0	2136	0	726	0	3297	0	4243	0	CFG_VIN2A_DE0_OUT	vout2_de
H7	vin2a_fld0	0	274	1409	698	0	161	0	55	CFG_VIN2A_FLD0_OUT	vout2_clk

Table 5-51. Manual Functions Mapping for DSS VOUT2 IOSET1 (continued)

BALL	BALL NAME	VOUT2_IOSET1 _MANUAL1		VOUT2_IOSET1 _MANUAL2		VOUT2_IOSET1 _MANUAL3		VOUT2_IOSET1 _MANUAL4		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		4
G1	vin2a_hsync0	2610	0	1200	0	3771	0	4717	0	CFG_VIN2A_HSYNC0_OUT	vout2_hsync
G6	vin2a_vsync0	2214	0	822	0	3375	0	4321	0	CFG_VIN2A_VSYNC0_OUT	vout2_vsync

Manual IO Timings Modes must be used to guarantee some IO timings for VOUT2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-52, *Manual Functions Mapping for DSS VOUT2 IOSET2* for a definition of the Manual modes.

Table 5-52 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-52. Manual Functions Mapping for DSS VOUT2 IOSET2

BALL	BALL NAME	VOUT2_IOSET2 _MANUAL1		VOUT2_IOSET2 _MANUAL2		VOUT2_IOSET2 _MANUAL3		VOUT2_IOSET2 _MANUAL4		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		6
E21	gpio6_14	1193	0	274	0	2474	0	3298	0	CFG_GPIO6_14_OUT	vout2_hsync
F20	gpio6_15	1006	0	27	0	2226	0	3039	0	CFG_GPIO6_15_OUT	vout2_vsync
F21	gpio6_16	921	0	0	0	2141	0	2955	0	CFG_GPIO6_16_OUT	vout2_fld
B14	mcasp1_aclkr	3224	0	2192	0	4505	0	5328	0	CFG_MCASP1_ACLKR_OUT	vout2_d0
G13	mcasp1_axr2	2197	0	1211	0	3478	0	4302	0	CFG_MCASP1_AXR2_OUT	vout2_d2
J11	mcasp1_axr3	1989	0	1013	0	3271	0	4094	0	CFG_MCASP1_AXR3_OUT	vout2_d3
E12	mcasp1_axr4	2452	0	1455	0	3733	0	4557	0	CFG_MCASP1_AXR4_OUT	vout2_d4
F13	mcasp1_axr5	2507	0	1507	0	3788	0	4612	0	CFG_MCASP1_AXR5_OUT	vout2_d5
C12	mcasp1_axr6	2212	0	1225	0	3493	0	4316	0	CFG_MCASP1_AXR6_OUT	vout2_d6
D12	mcasp1_axr7	2204	0	1218	0	3485	0	4309	0	CFG_MCASP1_AXR7_OUT	vout2_d7
J14	mcasp1_fsr	1933	0	959	0	3214	0	4037	0	CFG_MCASP1_FSR_OUT	vout2_d1
E15	mcasp2_aclkr	3074	0	2048	0	4355	0	5178	0	CFG_MCASP2_ACLKR_OUT	vout2_d8
B15	mcasp2_axr0	1798	0	830	0	3080	0	3903	0	CFG_MCASP2_AXR0_OUT	vout2_d10
A15	mcasp2_axr1	2031	0	542	510	3312	0	4135	0	CFG_MCASP2_AXR1_OUT	vout2_d11
D15	mcasp2_axr4	2050	0	1071	0	3331	0	4155	0	CFG_MCASP2_AXR4_OUT	vout2_d12
B16	mcasp2_axr5	1627	0	667	0	2908	0	3732	0	CFG_MCASP2_AXR5_OUT	vout2_d13
B17	mcasp2_axr6	2924	0	1905	0	4205	0	5028	0	CFG_MCASP2_AXR6_OUT	vout2_d14
A17	mcasp2_axr7	1555	0	598	0	2836	0	3660	0	CFG_MCASP2_AXR7_OUT	vout2_d15
A20	mcasp2_fsr	1689	0	188	539	2971	0	3794	0	CFG_MCASP2_FSR_OUT	vout2_d9

Table 5-52. Manual Functions Mapping for DSS VOUT2 IOSET2 (continued)

BALL	BALL NAME	VOUT2_IOSET2 _MANUAL1		VOUT2_IOSET2 _MANUAL2		VOUT2_IOSET2 _MANUAL3		VOUT2_IOSET2 _MANUAL4		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		6
C18	mcasp4_aclkx	2607	0	1603	0	3889	0	4712	0	CFG_MCASP4_ACLKX_OUT	vout2_d16
G16	mcasp4_axr0	1690	0	727	0	2971	0	3795	0	CFG_MCASP4_AXR0_OUT	vout2_d18
D17	mcasp4_axr1	1408	0	457	0	2689	0	3512	0	CFG_MCASP4_AXR1_OUT	vout2_d19
A21	mcasp4_fsx	1564	0	606	0	2845	0	3668	0	CFG_MCASP4_FSX_OUT	vout2_d17
AA3	mcasp5_aclkx	4355	1633	3732	1100	5399	1869	6062	2030	CFG_MCASP5_ACLKX_OUT	vout2_d20
AB3	mcasp5_axr0	4307	1362	3675	853	5352	1599	6014	1759	CFG_MCASP5_AXR0_OUT	vout2_d22
AA4	mcasp5_axr1	4276	971	3633	492	5321	1208	5984	1369	CFG_MCASP5_AXR1_OUT	vout2_d23
AB9	mcasp5_fsx	4272	981	3628	503	5317	1217	5980	1378	CFG_MCASP5_FSX_OUT	vout2_d21
B26	xref_clk2	0	51	2016	507	0	0	0	0	CFG_XREF_CLK2_OUT	vout2_clk
C23	xref_clk3	2331	0	1339	0	3612	0	4436	0	CFG_XREF_CLK3_OUT	vout2_de

Manual IO Timings Modes must be used to guarantee some IO timings for VOUT3. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-53, *Manual Functions Mapping for DSS VOUT3* for a definition of the Manual modes.

Table 5-53 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-53. Manual Functions Mapping for DSS VOUT3

BALL	BALL NAME	VOUT3_MANUAL1		VOUT3_MANUAL2		VOUT3_MANUAL3		VOUT3_MANUAL4		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4
R6	gpmc_a0	1627	0	787	0	2798	0	3781	0	CFG_GPMC_A0_OUT	vout3_d16	-
T9	gpmc_a1	1527	0	592	0	2698	0	3680	0	CFG_GPMC_A1_OUT	vout3_d17	-
N9	gpmc_a10	1907	0	1181	0	3122	0	4194	0	CFG_GPMC_A10_OUT	vout3_de	-
P9	gpmc_a11	2406	0	1676	0	3622	0	4693	0	CFG_GPMC_A11_OUT	vout3_fld	-
T6	gpmc_a2	1508	0	641	0	2679	0	3661	0	CFG_GPMC_A2_OUT	vout3_d18	-
T7	gpmc_a3	2222	0	1481	0	3437	0	4508	0	CFG_GPMC_A3_OUT	vout3_d19	-
P6	gpmc_a4	2529	0	1775	0	3744	0	4815	0	CFG_GPMC_A4_OUT	vout3_d20	-
R9	gpmc_a5	1492	0	785	0	2708	0	3779	0	CFG_GPMC_A5_OUT	vout3_d21	-
R5	gpmc_a6	1578	0	848	0	2774	0	3845	0	CFG_GPMC_A6_OUT	vout3_d22	-
P5	gpmc_a7	1586	0	851	0	2778	0	3849	0	CFG_GPMC_A7_OUT	vout3_d23	-
N7	gpmc_a8	2519	0	1783	0	3734	0	4805	0	CFG_GPMC_A8_OUT	vout3_hsync	-
R4	gpmc_a9	1886	0	951	0	2864	0	3935	0	CFG_GPMC_A9_OUT	vout3_vsync	-

Table 5-53. Manual Functions Mapping for DSS VOUT3 (continued)

BALL	BALL NAME	VOUT3_MANUAL1		VOUT3_MANUAL2		VOUT3_MANUAL3		VOUT3_MANUAL4		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4
M6	gpmc_ad0	1813	0	1091	0	3028	0	4099	0	CFG_GPMC_AD0_OUT	vout3_d0	-
M2	gpmc_ad1	1652	0	937	0	2868	0	3939	0	CFG_GPMC_AD1_OUT	vout3_d1	-
J1	gpmc_ad10	1746	0	1027	0	2962	0	4033	0	CFG_GPMC_AD10_OUT	vout3_d10	-
J2	gpmc_ad11	1534	0	824	0	2749	0	3820	0	CFG_GPMC_AD11_OUT	vout3_d11	-
H1	gpmc_ad12	1923	0	1196	0	3138	0	4209	0	CFG_GPMC_AD12_OUT	vout3_d12	-
J3	gpmc_ad13	1496	0	754	0	2676	0	3747	0	CFG_GPMC_AD13_OUT	vout3_d13	-
H2	gpmc_ad14	1379	0	665	0	2582	0	3653	0	CFG_GPMC_AD14_OUT	vout3_d14	-
H3	gpmc_ad15	1746	0	1027	0	2961	0	4032	0	CFG_GPMC_AD15_OUT	vout3_d15	-
L5	gpmc_ad2	1894	0	1168	0	3110	0	4181	0	CFG_GPMC_AD2_OUT	vout3_d2	-
M1	gpmc_ad3	1584	0	872	0	2800	0	3871	0	CFG_GPMC_AD3_OUT	vout3_d3	-
L6	gpmc_ad4	1815	0	1092	0	3030	0	4101	0	CFG_GPMC_AD4_OUT	vout3_d4	-
L4	gpmc_ad5	1436	0	576	0	2607	0	3589	0	CFG_GPMC_AD5_OUT	vout3_d5	-
L3	gpmc_ad6	1837	0	1113	0	3052	0	4123	0	CFG_GPMC_AD6_OUT	vout3_d6	-
L2	gpmc_ad7	1658	0	943	0	2874	0	3945	0	CFG_GPMC_AD7_OUT	vout3_d7	-
L1	gpmc_ad8	515	0	0	0	1686	0	2757	0	CFG_GPMC_AD8_OUT	vout3_d8	-
K2	gpmc_ad9	853	0	0	0	2024	0	3006	0	CFG_GPMC_AD9_OUT	vout3_d9	-
P1	gpmc_cs3	0	234	1801	948	0	167	0	177	CFG_GPMC_CS3_OUT	vout3_clk	-
AG8	vin1a_clk0	1954	0	1244	0	3240	0	4298	0	CFG_VIN1A_CLK0_OUT	vout3_d16	vout3_fld
AE8	vin1a_d0	1991	0	1261	0	3277	0	4336	0	CFG_VIN1A_D0_OUT	vout3_d7	vout3_d23
AD8	vin1a_d1	1911	0	1185	0	3197	0	4256	0	CFG_VIN1A_D1_OUT	vout3_d6	vout3_d22
AG3	vin1a_d10	2460	0	1647	0	3754	0	4813	0	CFG_VIN1A_D10_OUT	-	vout3_d13
AG5	vin1a_d11	2098	0	1302	0	3392	0	4451	0	CFG_VIN1A_D11_OUT	-	vout3_d12
AF2	vin1a_d12	2703	0	1880	0	3997	0	5056	0	CFG_VIN1A_D12_OUT	-	vout3_d11
AF6	vin1a_d13	2049	0	1255	0	3343	0	4402	0	CFG_VIN1A_D13_OUT	-	vout3_d10
AF3	vin1a_d14	2815	0	1987	0	4109	0	5131	37	CFG_VIN1A_D14_OUT	-	vout3_d9
AF4	vin1a_d15	1973	0	1183	0	3267	0	4326	0	CFG_VIN1A_D15_OUT	-	vout3_d8
AF1	vin1a_d16	2084	0	1289	0	3379	0	4437	0	CFG_VIN1A_D16_OUT	-	vout3_d7
AE3	vin1a_d17	2100	0	1304	0	3394	0	4453	0	CFG_VIN1A_D17_OUT	-	vout3_d6
AE5	vin1a_d18	2069	0	1274	0	3363	0	4422	0	CFG_VIN1A_D18_OUT	-	vout3_d5
AE1	vin1a_d19	2171	0	1372	0	3465	0	4524	0	CFG_VIN1A_D19_OUT	-	vout3_d4
AG7	vin1a_d2	1956	0	1227	0	3241	0	4300	0	CFG_VIN1A_D2_OUT	vout3_d5	vout3_d21
AE2	vin1a_d20	2251	0	1448	0	3546	0	4604	0	CFG_VIN1A_D20_OUT	-	vout3_d3

Table 5-53. Manual Functions Mapping for DSS VOUT3 (continued)

BALL	BALL NAME	VOUT3_MANUAL1		VOUT3_MANUAL2		VOUT3_MANUAL3		VOUT3_MANUAL4		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3	4
AE6	vin1a_d21	2252	0	1449	0	3546	0	4605	0	CFG_VIN1A_D21_OUT	-	vout3_d2
AD2	vin1a_d22	2199	0	1187	211	3494	0	4552	0	CFG_VIN1A_D22_OUT	-	vout3_d1
AD3	vin1a_d23	2316	0	1510	0	3610	0	4669	0	CFG_VIN1A_D23_OUT	-	vout3_d0
AH6	vin1a_d3	2053	0	1320	0	3338	0	4397	0	CFG_VIN1A_D3_OUT	vout3_d4	vout3_d20
AH3	vin1a_d4	2760	0	1995	0	4045	0	5015	89	CFG_VIN1A_D4_OUT	vout3_d3	vout3_d19
AH5	vin1a_d5	1755	0	1007	0	3010	0	4069	0	CFG_VIN1A_D5_OUT	vout3_d2	vout3_d18
AG6	vin1a_d6	1948	0	1220	0	3233	0	4292	0	CFG_VIN1A_D6_OUT	vout3_d1	vout3_d17
AH4	vin1a_d7	1925	0	1198	0	3211	0	4270	0	CFG_VIN1A_D7_OUT	vout3_d0	vout3_d16
AG4	vin1a_d8	2104	0	1307	0	3398	0	4457	0	CFG_VIN1A_D8_OUT	-	vout3_d15
AG2	vin1a_d9	2192	0	1392	0	3487	0	4545	0	CFG_VIN1A_D9_OUT	-	vout3_d14
AD9	vin1a_de0	2202	0	1462	0	3487	0	4546	0	CFG_VIN1A_DE0_OUT	vout3_d17	vout3_de
AF9	vin1a_fld0	0	0	2007	454	0	0	0	0	CFG_VIN1A_FLD0_OUT	-	vout3_clk
AE9	vin1a_hsync0	2015	0	1240	0	3309	0	4367	0	CFG_VIN1A_HSYNC0_OUT	-	vout3_hsync
AF8	vin1a_vsync0	1829	0	1063	0	3123	0	4182	0	CFG_VIN1A_VSYNC0_OUT	-	vout3_vsync

5.10.6.5 HDMI

The High-Definition Multimedia Interface is provided for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. The HDMI interface is aligned with the HDMI TMDS single stream standard v1.4a (720p @60Hz to 1080p @24Hz) and the HDMI v1.3 (1080p @60Hz): 3 data channels, plus 1 clock channel is supported (differential).

NOTE

For more information, see the High-Definition Multimedia Interface chapter of the Device TRM.

5.10.6.6 EMIF

The device has a dedicated interface to DDR3 and DDR2 SDRAM. It supports JEDEC standard compliant DDR2 and DDR3 SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: 128Mb, 256Mb, 512Mb, 1Gb, 2Gb, 4Gb and 8Gb devices (Single die only)
- One interface with associated DDR2/DDR3 PHYs

NOTE

For more information, see the EMIF Controller section of the Device TRM.

5.10.6.7 GPMC

The GPMC is the unified memory controller that interfaces external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

NOTE

For more information, see the General-Purpose Memory Controller section of the Device TRM.

5.10.6.7.1 GPMC/NOR Flash Interface Synchronous Timing

CAUTION

The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-54 and Table 5-55 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 5-28, Figure 5-29, Figure 5-30, Figure 5-31, Figure 5-32, and Figure 5-33).

Table 5-54. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Default

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_clk high	1.9		ns
F13	$t_{h(clkH-dV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_clk high	1		ns
F21	$t_{su(waitV-clkH)}$	Setup time, gpmc_wait[1:0] valid before gpmc_clk high	1.9		ns

Table 5-54. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Default (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F22	$t_{h(clkH-waitV)}$	Hold Time, gpmc_wait[1:0] valid after gpmc_clk high	1		ns

NOTE

Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see General-Purpose Memory Controller section in the Device TRM.

Table 5-55. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Default

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F0	$t_{c(clk)}$	Cycle time, output clock gpmc_clk period	11.3		ns
F2	$t_{d(clkH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition	F[(6)]-0.8	F[(6)]+3.17	ns
F3	$t_{d(clkH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid	E[(5)]-0.8	E[(5)]+3.1	ns
F4	$t_{d(ADDV-clk)}$	Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge	B[(2)]-0.8	B[(2)]+3.43	ns
F5	$t_{d(clkH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid	-0.8		ns
F6	$t_{d(nBEV-clk)}$	Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge	B[(2)]-3.8	B[(2)]+2.37	ns
F7	$t_{d(clkH-nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid	D[(4)]-0.4	D[(4)]+1.1	ns
F8	$t_{d(clkH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale transition	G[(7)]-0.8	G[(7)]+3.1	ns
F9	$t_{d(clkH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid	D[(4)]-0.8	D[(4)]+3.1	ns
F10	$t_{d(clkH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren transition	H[(8)]-0.8	H[(8)]+2.45	ns
F11	$t_{d(clkH-nOEIV)}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid	E[(5)]-0.8	E[(5)]+2.1	ns
F14	$t_{d(clkH-nWE)}$	Delay time, gpmc_clk rising edge to gpmc_wen transition	I[(9)]-0.8	I[(9)]+3.1	ns
F15	$t_{d(clkH-Data)}$	Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition	J[(10)]-1.1	J[(10)]+4.89	ns
F17	$t_{d(clkH-nBE)}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition	J[(10)]-1.1	J[(10)]+3.8	ns
F18	$t_{w(nCSV)}$	Pulse duration, gpmc_cs[7:0] low	A[(1)]		ns
F19	$t_{w(nBEV)}$	Pulse duration, gpmc_ben[1:0] low	C[(3)]		ns
F20	$t_{w(nADVV)}$	Pulse duration, gpmc_advn_ale low	K[(11)]		ns
F23	$t_{d(CLK-GPIO)}$	Delay time, gpmc_clk transition to gpio6_16 transition	1.2	6.1	ns

Table 5-56. GPMC/NOR Flash Interface Timing Requirements - Synchronous Mode - Alternate

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_clk high	2.5		ns
F13	$t_{h(clkH-dV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_clk high	1.9		ns
F21	$t_{su(waitV-clkH)}$	Setup time, gpmc_wait[1:0] valid before gpmc_clk high	2.5		ns
F22	$t_{h(clkH-waitV)}$	Hold Time, gpmc_wait[1:0] valid after gpmc_clk high	1.9		ns

Table 5-57. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F0	$t_{c(clk)}$	Cycle time, output clock gpmc_clk period [(12)]	15.04		ns
F2	$t_{d(clkH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] transition [(14)]	F[(6)]-0.13	F[(6)]+6.1	ns
F3	$t_{d(clkH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_cs[7:0] invalid [(14)]	E[(5)]+0.7	E[(5)]+6.1	ns
F4	$t_{d(ADDV-clk)}$	Delay time, gpmc_a[27:0] address bus valid to gpmc_clk first edge	B[(2)]+0.21	B[(2)]+6.1	ns
F5	$t_{d(clkH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[27:0] gpmc address bus invalid	0.7		ns
F6	$t_{d(nBEV-clk)}$	Delay time, gpmc_ben[1:0] valid to gpmc_clk rising edge	B[(2)]-4.9	B[(2)]+0.4	ns

Table 5-57. GPMC/NOR Flash Interface Switching Characteristics - Synchronous Mode - Alternate (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
F7	$t_{d(clkH-nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] invalid	D[4]-0.4	D[4]+4.9	ns
F8	$t_{d(clkH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale transition [14]	G[7]+0.7	G[7]+6.1	ns
F9	$t_{d(clkH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_advn_ale invalid [14]	D[4]+0.7	D[4]+6.1	ns
F10	$t_{d(clkH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren transition [14]	H[8]+0.42	H[8]+5.1	ns
F11	$t_{d(clkH-nOEIV)}$	Delay time, gpmc_clk rising edge to gpmc_oen_ren invalid [14]	E[5]+0.7	E[5]+5.1	ns
F14	$t_{d(clkH-nWE)}$	Delay time, gpmc_clk rising edge to gpmc_wen transition [14]	I[9]+0.46	I[9]+6.1	ns
F15	$t_{d(clkH-Data)}$	Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition	J[10]-0.4	J[10]+4.9	ns
F17	$t_{d(clkH-nBE)}$	Delay time, gpmc_clk rising edge to gpmc_ben[1:0] transition	J[10]-0.4	J[10]+5.63	ns
F18	$t_{w(nCSV)}$	Pulse duration, gpmc_cs[7:0] low	A[1]		ns
F19	$t_{w(nBEV)}$	Pulse duration, gpmc_ben[1:0] low	C[3]		ns
F20	$t_{w(nADVV)}$	Pulse duration, gpmc_advn_ale low	K[11]		ns
F23	$t_{d(CLK-GPIO)}$	Delay time, gpmc_clk transition to gpio6_16 transition [13]	0.96	6.1	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK period
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK period
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK period
with n the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK

(3) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For Burst write: C = (WrCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK with n the page burst access number.

(4) For single read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst write: D = (WrCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(5) For single read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst write: E = (CSWrOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(6) For nCS falling edge (CS activated):
Case GpmcFCLKDivider = 0 :
F = 0.5 × CSExtraDelay × GPMC_FCLK Case GpmcFCLKDivider = 1:
F = 0.5 × CSExtraDelay × GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
F = 0.5 × CSExtraDelay × GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
F = 0.5 × CSExtraDelay × GPMC_FCLK if ((CSOnTime - ClkActivationTime) is a multiple of 4)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime - ClkActivationTime - 1) is a multiple of 4)
F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime - ClkActivationTime - 2) is a multiple of 4)
F = (3 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime - ClkActivationTime - 3) is a multiple of 4)

(7) For ADV falling edge (ADV activated):
Case GpmcFCLKDivider = 0 :
G = 0.5 × ADVExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)
For ADV rising edge (ADV deactivated) in Reading mode:
Case GpmcFCLKDivider = 0:
G = 0.5 × ADVExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)

G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 4)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 4)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 4)
G = (3 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 3) is a multiple of 4)
For ADV rising edge (ADV deactivated) in Writing mode:
Case GpmcFCLKDivider = 0:
G = 0.5 × ADVExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 4)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 4)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 4)
G = (3 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 3) is a multiple of 4)

(8) For OE falling edge (OE activated):
Case GpmcFCLKDivider = 0:
- H = 0.5 × OEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
- H = 0.5 × OEExtraDelay × GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
- H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
- H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOnTime - ClkActivationTime) is a multiple of 4)
- H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime - ClkActivationTime - 1) is a multiple of 4)
- H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime - ClkActivationTime - 2) is a multiple of 4)
- H = (3 + 0.5 × OEExtraDelay)) × GPMC_FCLK if ((OEOnTime - ClkActivationTime - 3) is a multiple of 4)
For OE rising edge (OE deactivated):
Case GpmcFCLKDivider = 0:
- H = 0.5 × OEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
- H = 0.5 × OEExtraDelay × GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
- H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
- H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 4)
- H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 4)
- H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 4)
- H = (3 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 3) is a multiple of 4)

(9) For WE falling edge (WE activated):
Case GpmcFCLKDivider = 0:
- I = 0.5 × WEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
- I = 0.5 × WEExtraDelay × GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
- I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- I = 0.5 × WEExtraDelay × GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
- I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- I = 0.5 × WEExtraDelay × GPMC_FCLK if ((WEOnTime - ClkActivationTime) is a multiple of 4)
- I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOnTime - ClkActivationTime - 1) is a multiple of 4)

- I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOnTime - ClkActivationTime - 2) is a multiple of 4)
- I = (3 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOnTime - ClkActivationTime - 3) is a multiple of 4)
For WE rising edge (WE deactivated):
Case GpmcFCLKDivider = 0:
- I = 0.5 × WEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
- I = 0.5 × WEExtraDelay × GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
- I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
- I = 0.5 × WEExtraDelay × GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
- I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)
Case GpmcFCLKDivider = 3:
- I = 0.5 × WEExtraDelay × GPMC_FCLK if ((WEOffTime - ClkActivationTime) is a multiple of 4)
- I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOffTime - ClkActivationTime - 1) is a multiple of 4)
- I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOffTime - ClkActivationTime - 2) is a multiple of 4)
- I = (3 + 0.5 × WEExtraDelay) × GPMC_FCLK if ((WEOffTime - ClkActivationTime - 3) is a multiple of 4)

(10) J = GPMC_FCLK period, where GPMC_FCLK is the General Purpose Memory Controller internal functional clock

(11) For read:
K = (ADVRdOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For write: K = (ADVWrOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(12) The gpmc_clk output clock maximum and minimum frequency is programmable in the I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider

(13) gpio6_16 programmed to MUXMODE=9 (clkout1), CM_CLKSEL_CLKOUTMUX1 programmed to 7 (CORE_DPLL_OUT_DCLK), CM_CLKSEL_CORE_DPLL_OUT_CLK_CLKOUTMUX programmed to 1.

(14) CSEXTRADELAY = 0, ADVEXTRADELAY = 0, WEEXTRADELAY = 0, OEEXTRADELAY = 0. Extra half-GPMC_FCLK cycle delay mode is not timed.

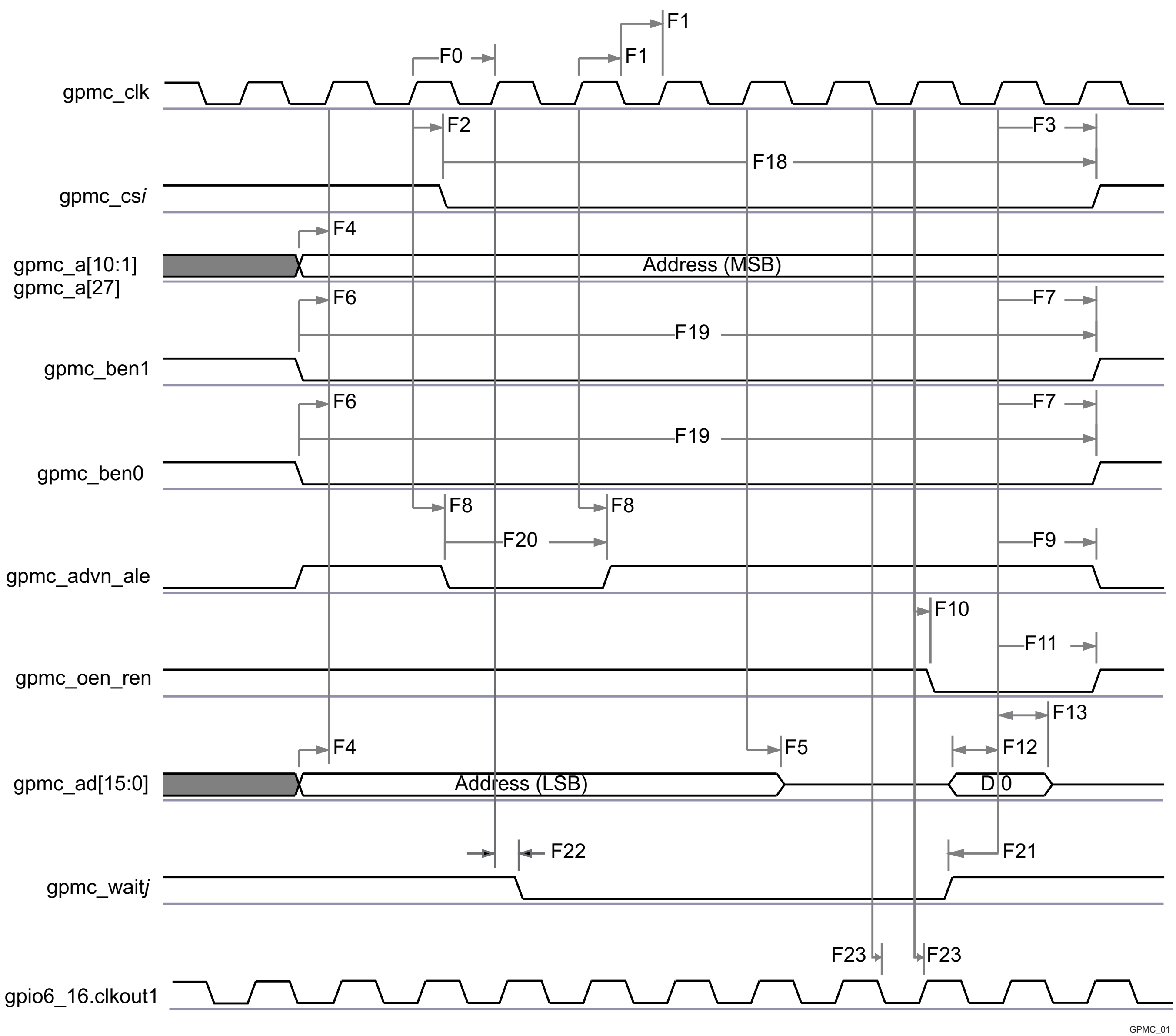


Figure 5-28. GPMC / Multiplexed 16bits NOR Flash - Synchronous Single Read - (GpmcFCLKDivider = 0)[(1)(2)]

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_wait*j*, j = 0 to 1.

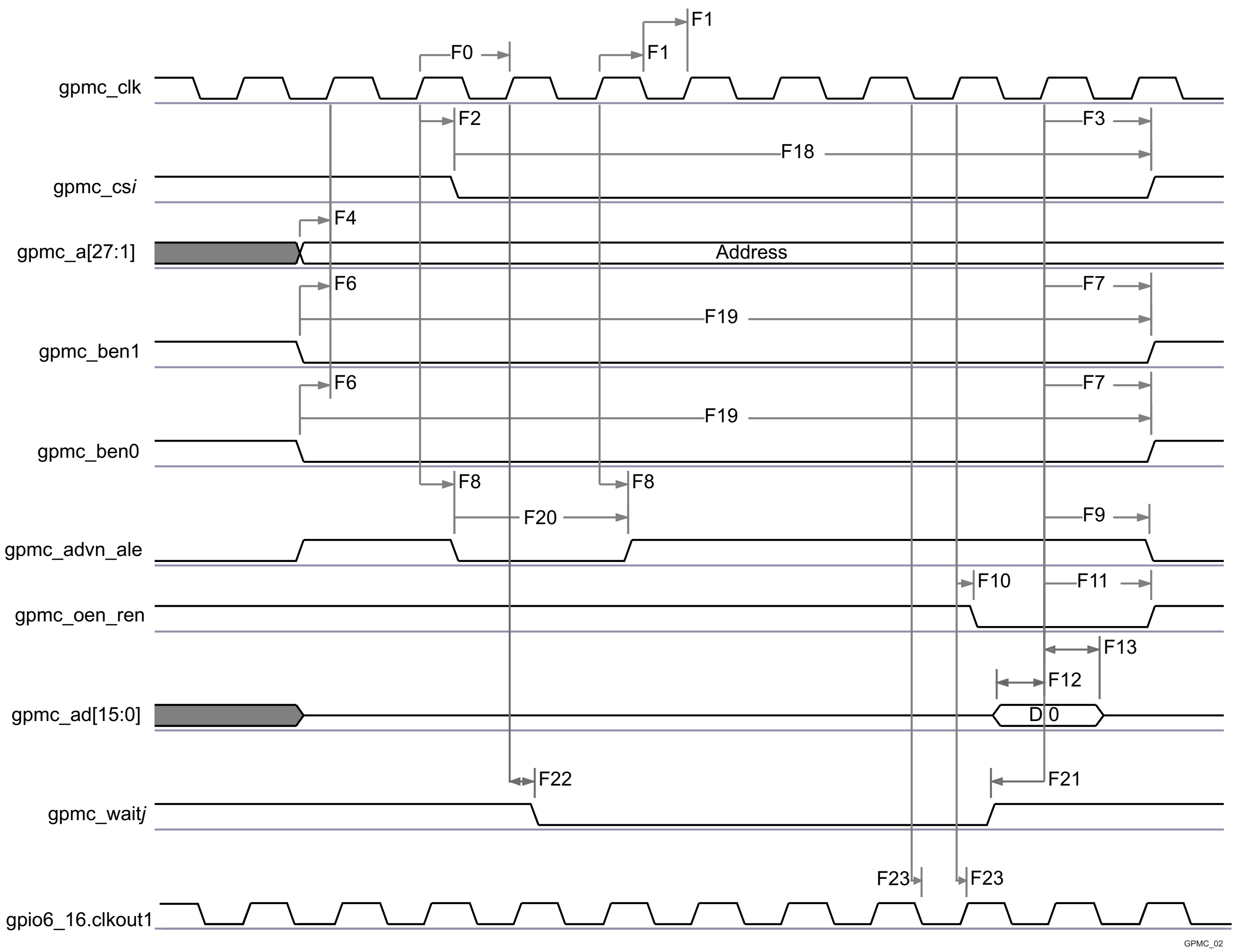


Figure 5-29. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Single Read - (GpmcFCLKDivider = 0)(1)(2)

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_wait*j*, j = 0 to 1.

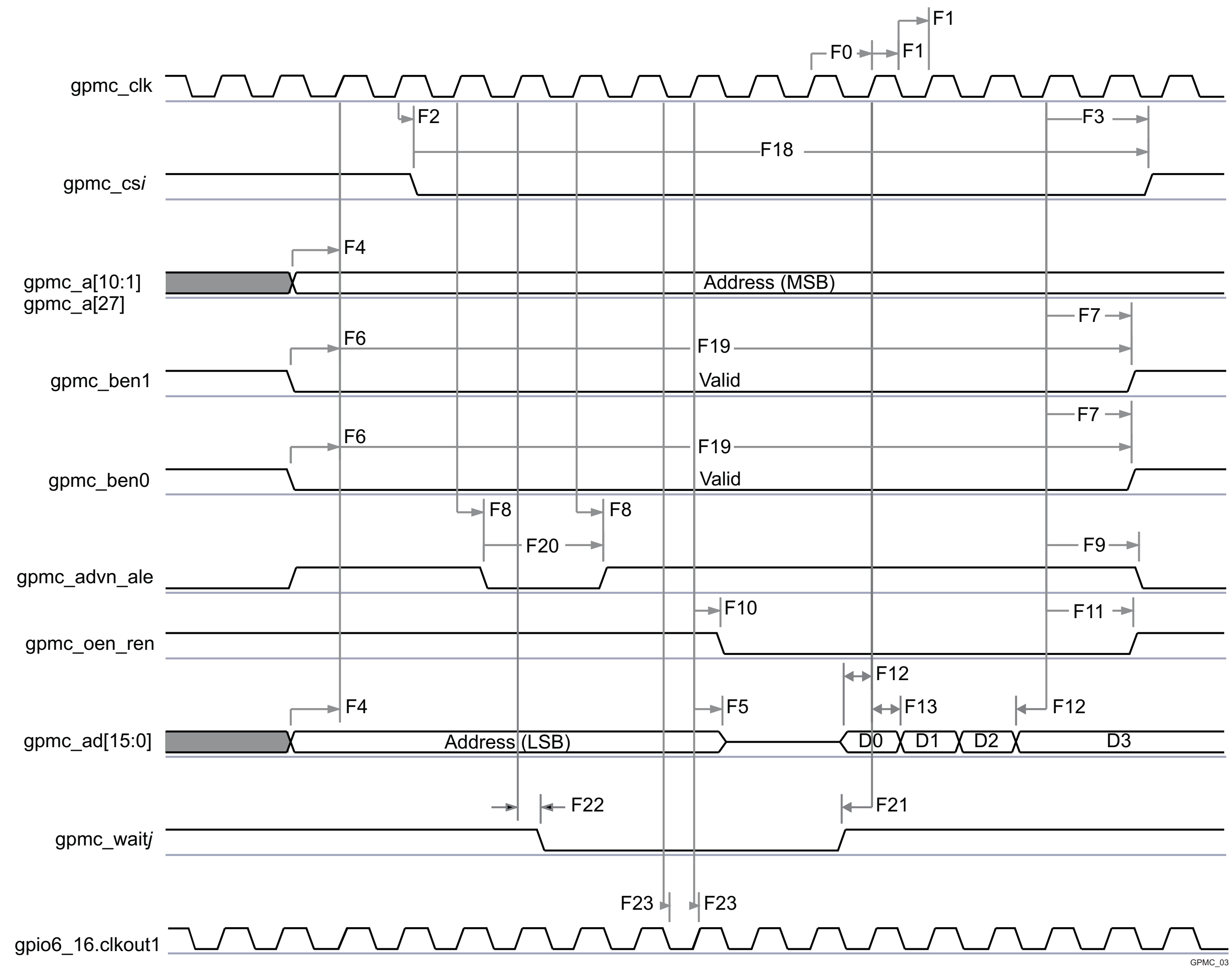


Figure 5-30. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)(1)(2)

(1) In gpmc_cs*i*, i= 0 to 7.

(2) In gpmc_wait*j*, j = 0 to 1.

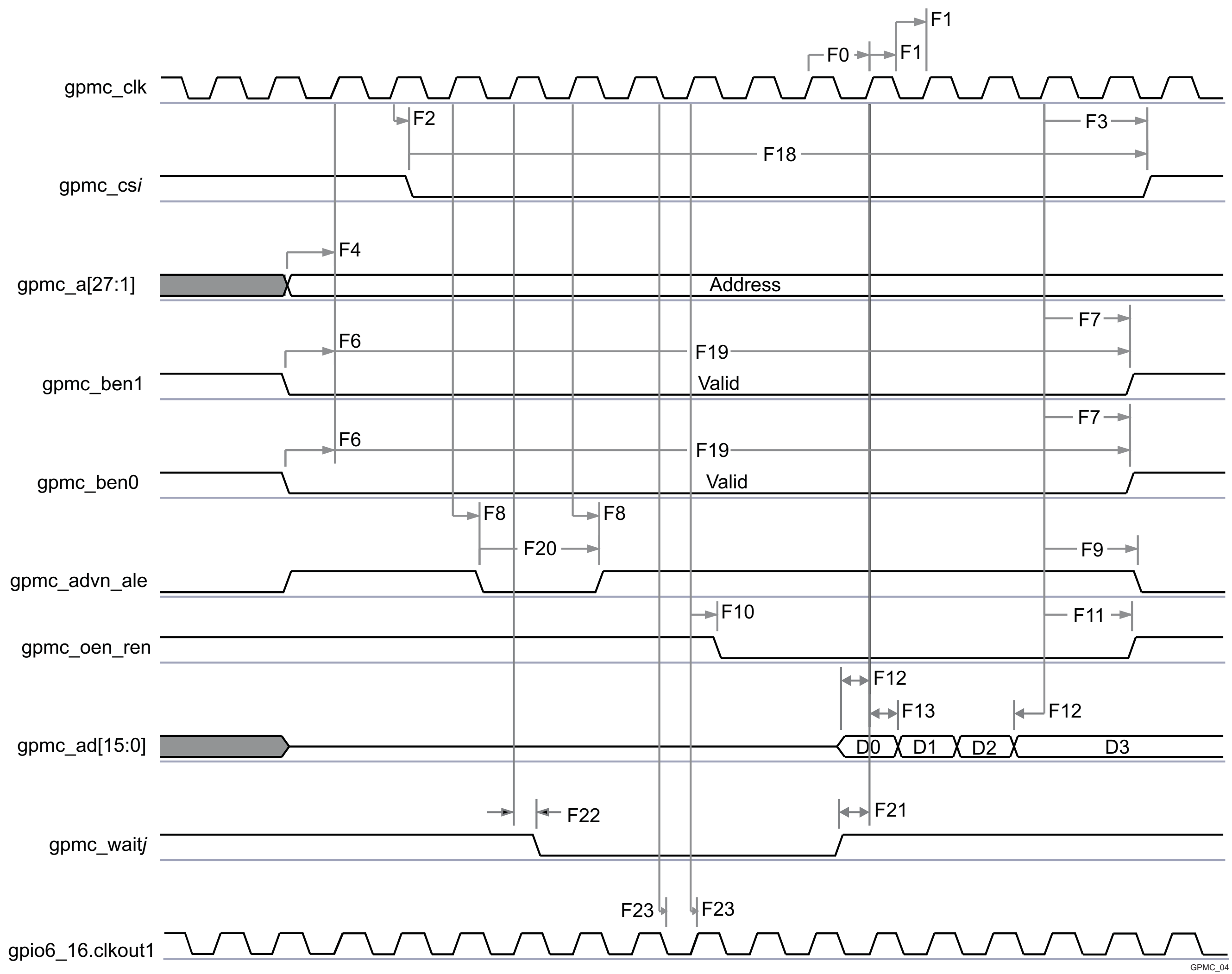


Figure 5-31. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Burst Read 4x16 bits - (GpmcFCLKDivider = 0)[(1)(2)]

(1) In gpmc_csi, i = 0 to 7.

(2) In gpmc_waitj, j = 0 to 1.

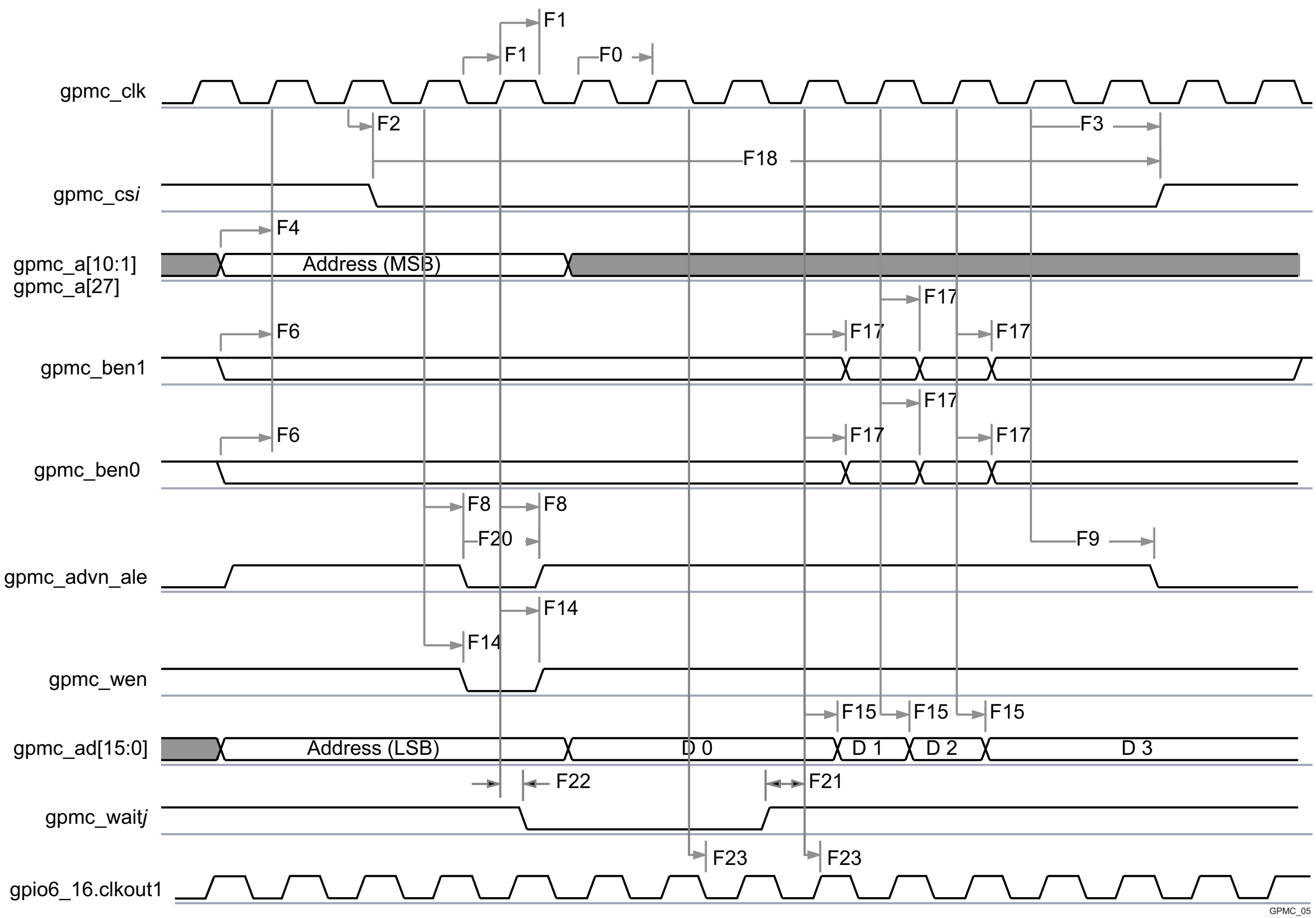


Figure 5-32. GPMC / Multiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)(1)(2)

(1) In gpmc_cs*i*, i = 0 to 7.

(2) In gpmc_wait*j*, j = 0 to 1.

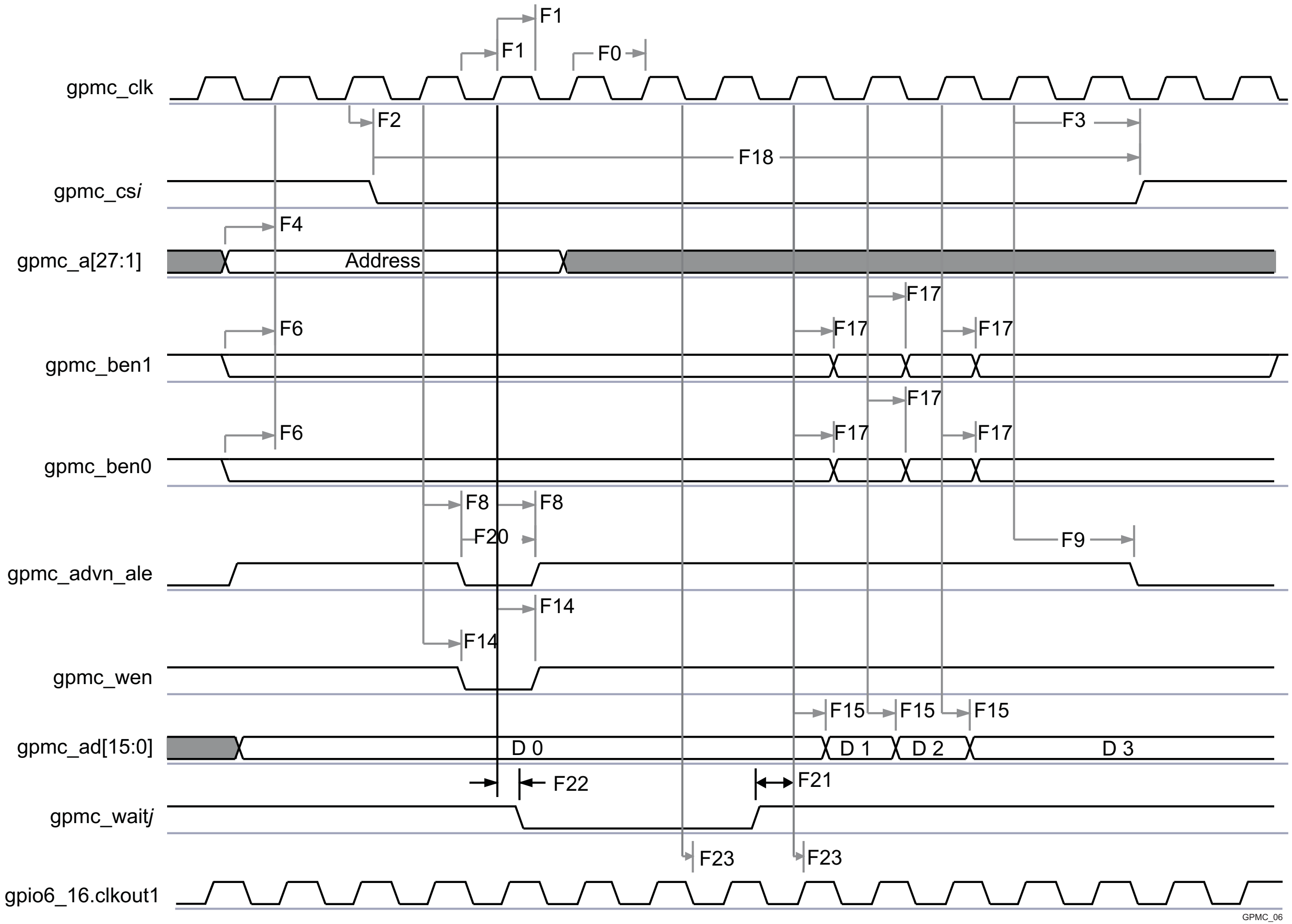


Figure 5-33. GPMC / Nonmultiplexed 16bits NOR Flash - Synchronous Burst Write 4x16bits - (GpmcFCLKDivider = 0)(1)(2)

(1) In gpmc_cs*i*, i = 1 to 7.

(2) In gpmc_wait*j*, j = 0 to 1.

5.10.6.7.2 GPMC/NOR Flash Interface Asynchronous Timing

CAUTION

The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-58 and Table 5-59 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 5-34, Figure 5-35, Figure 5-36, Figure 5-37, Figure 5-38, and Figure 5-39).

Table 5-58. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FA5	$t_{acc(DAT)}$	Data Maximum Access Time (GPMC_FCLK cycles)		H (1)	cycles
FA20	$t_{acc1\text{-}pgmode(DAT)}$	Page Mode Successive Data Maximum Access Time (GPMC_FCLK cycles)		P (2)	cycles

Table 5-58. GPMC/NOR Flash Interface Timing Requirements - Asynchronous Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FA21	$t_{acc2\text{-}pgmode(DAT)}$	Page Mode First Data Maximum Access Time (GPMC_FCLK cycles)		H (1)	cycles
-	$t_{su(DV\text{-}OEH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high	1.9		ns
-	$t_{h(OEH\text{-}DV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high	1		ns

(1) H = Access Time × (TimeParaGranularity + 1)

(2) P = PageBurstAccessTime × (TimeParaGranularity + 1)

Table 5-59. GPMC/NOR Flash Interface Switching Characteristics - Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FA0	$t_{w(nBEV)}$	Pulse duration, gpmc_ben[1:0] valid time		N (1)	ns
FA1	$t_{w(nCSV)}$	Pulse duration, gpmc_cs[7:0] low		A (2)	ns
FA3	$t_{d(nCSV\text{-}nADVIV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale invalid	B - 2 (3)	B + 4 (3)	ns
FA4	$t_{d(nCSV\text{-}nOEIV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Single read)	C - 2 (4)	C + 4 (4)	ns
FA9	$t_{d(AV\text{-}nCSV)}$	Delay time, address bus valid to gpmc_cs[7:0] valid	J - 2 (5)	J + 4 (5)	ns
FA10	$t_{d(nBEV\text{-}nCSV)}$	Delay time, gpmc_ben[1:0] valid to gpmc_cs[7:0] valid	J - 2 (5)	J + 4 (5)	ns
FA12	$t_{d(nCSV\text{-}nADVV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_advn_ale valid	K - 2 (6)	K + 4 (6)	ns
FA13	$t_{d(nCSV\text{-}nOEV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid	L - 2 (7)	L + 4 (7)	ns
FA16	$t_{w(AIV)}$	Pulse duration, address invalid between 2 successive R/W accesses	G (8)		ns
FA18	$t_{d(nCSV\text{-}nOEIV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren invalid (Burst read)	I - 2 (9)	I + 4 (9)	ns
FA20	$t_{w(AV)}$	Pulse duration, address valid : 2nd, 3rd and 4th accesses	D (10)		ns
FA25	$t_{d(nCSV\text{-}nWEV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_wen valid	E - 2 (11)	E + 4 (11)	ns
FA27	$t_{d(nCSV\text{-}nWEIV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_wen invalid	F - 2 (12)	F + 4 (12)	ns
FA28	$t_{d(nWEV\text{-}DV)}$	Delay time, gpmc_ wen valid to data bus valid		2	ns
FA29	$t_{d(DV\text{-}nCSV)}$	Delay time, data bus valid to gpmc_cs[7:0] valid	J - 2 (5)	J + 4 (5)	ns
FA37	$t_{d(nOEV\text{-}AIV)}$	Delay time, gpmc_oen_ren valid to gpmc_ad[15:0] multiplexed address bus phase end		2	ns

(1) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(2) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(3) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK

(4) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK

(5) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK

(6) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK

(7) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK

(8) G = Cycle2CycleDelay × GPMC_FCLK × (TimeParaGranularity +1)

(9) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK

(10) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK

(11) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK

(12) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK

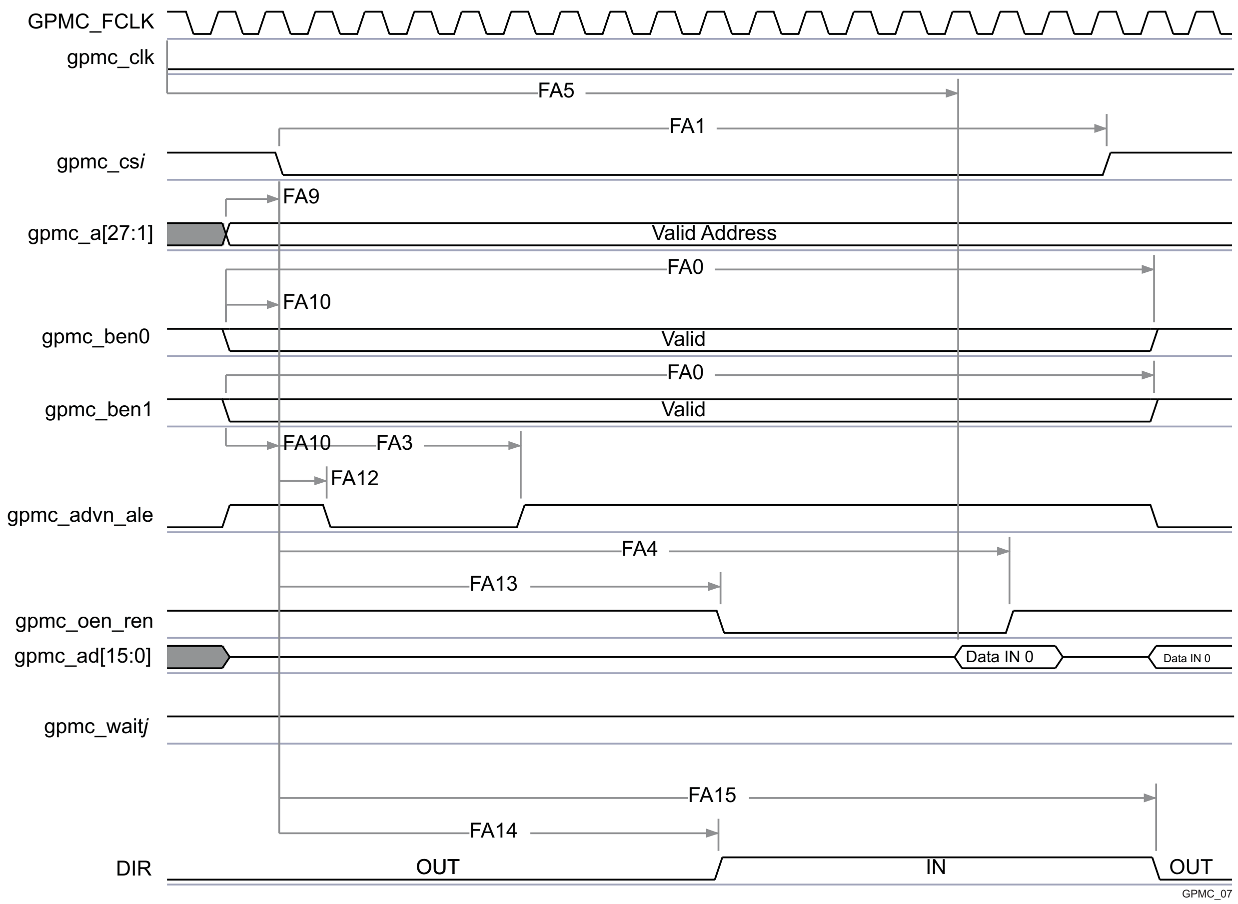


Figure 5-34. GPMC / NOR Flash - Asynchronous Read - Single Word Timing(1)(2)(3)(4)

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_wait*j*, j = 0 to 1.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

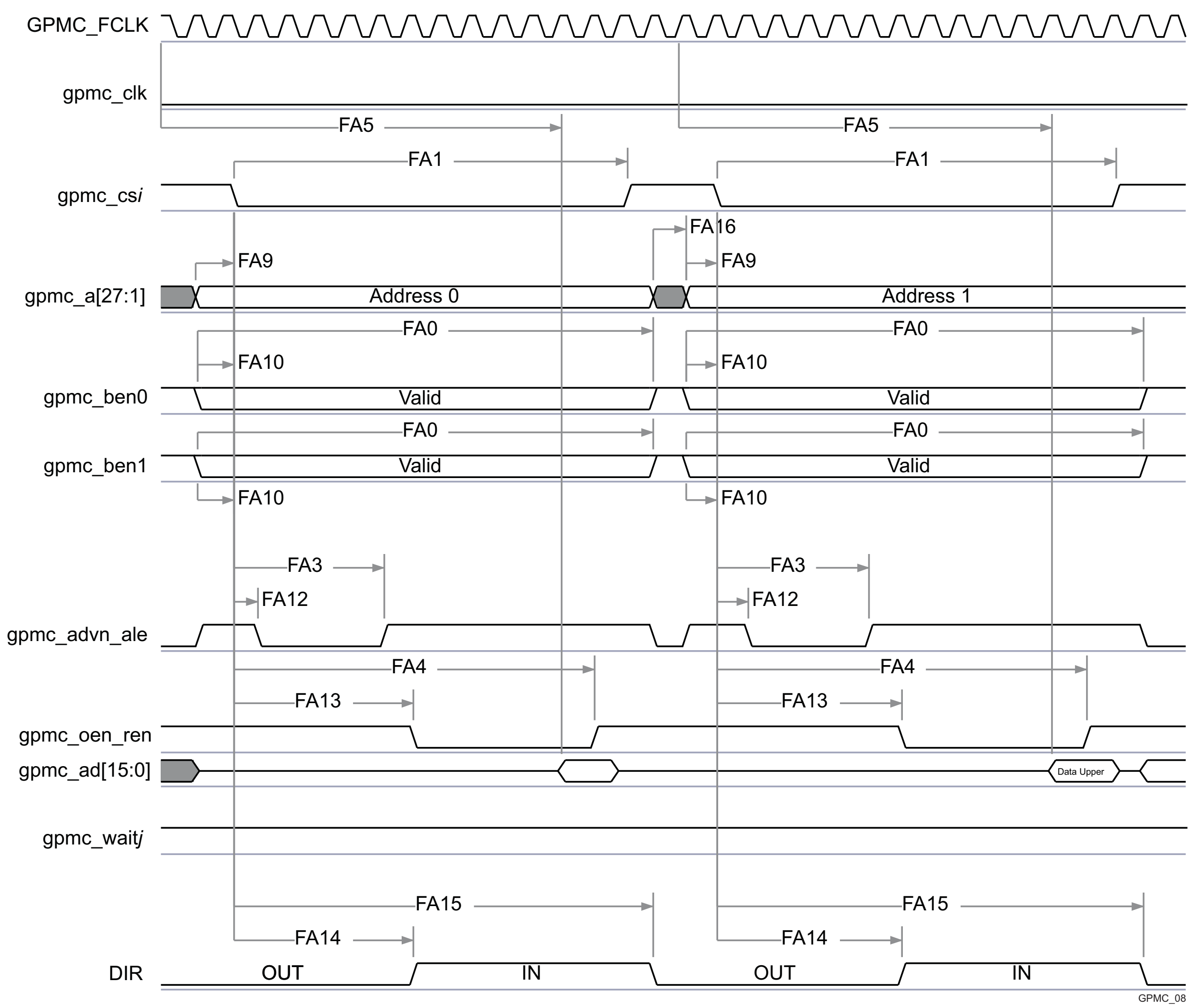


Figure 5-35. GPMC / NOR Flash - Asynchronous Read - 32-bit Timing(1)(2)(3)(4)

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_wait*j*, j = 0 to 1.

(2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

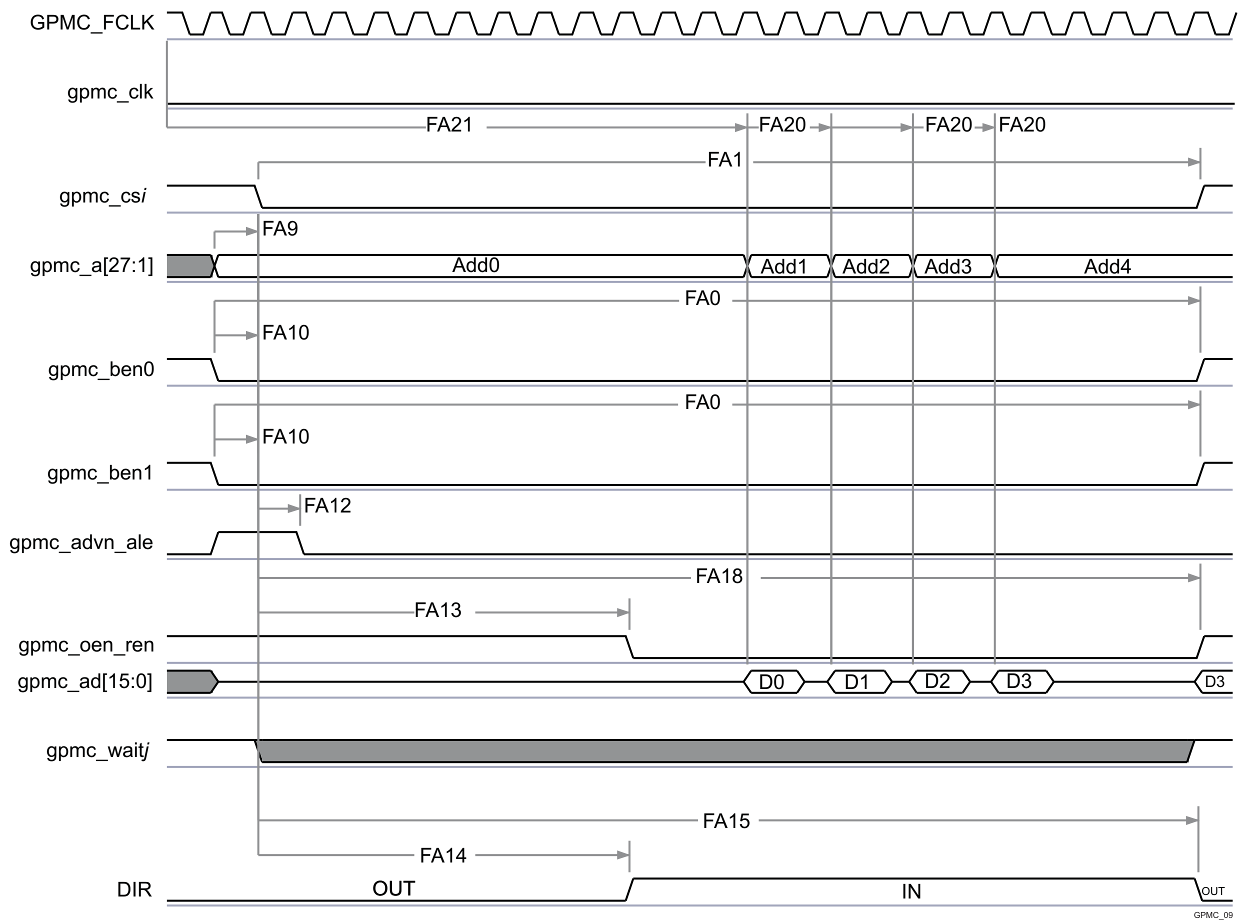


Figure 5-36. GPMC / NOR Flash - Asynchronous Read - Page Mode 4x16-bit Timing(1)(2)(3)(4)(5)

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_wait*j*, j = 0 to 1.

(2) FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data will be internally sampled by active functional clock edge. FA21 calculation is detailled in a separated application note and should be stored inside AccessTime register bits field.

(3) FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input Page Data (excluding first input Page Data). FA20 value should be stored in PageBurstAccessTime register bits field.

(4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(5) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

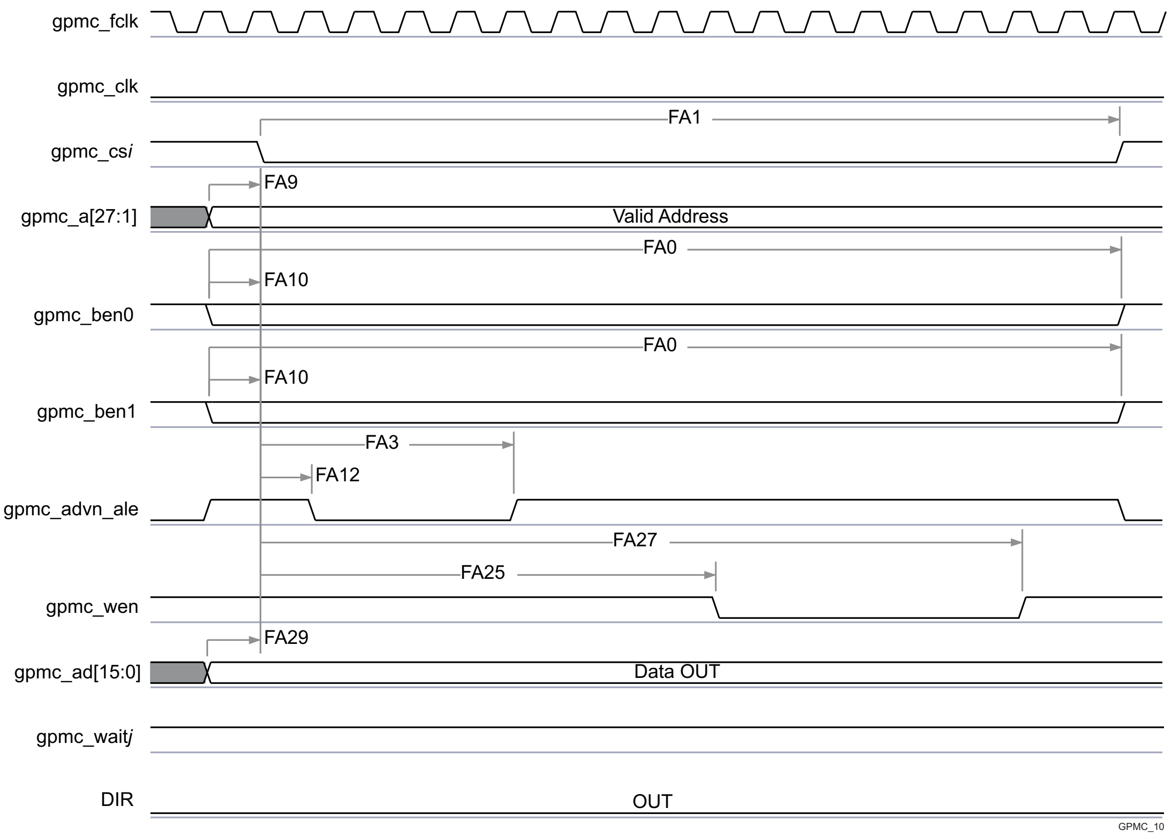


Figure 5-37. GPMC / NOR Flash - Asynchronous Write - Single Word Timing(1)(2)

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_wait*j*, j = 0 to 1.

(2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

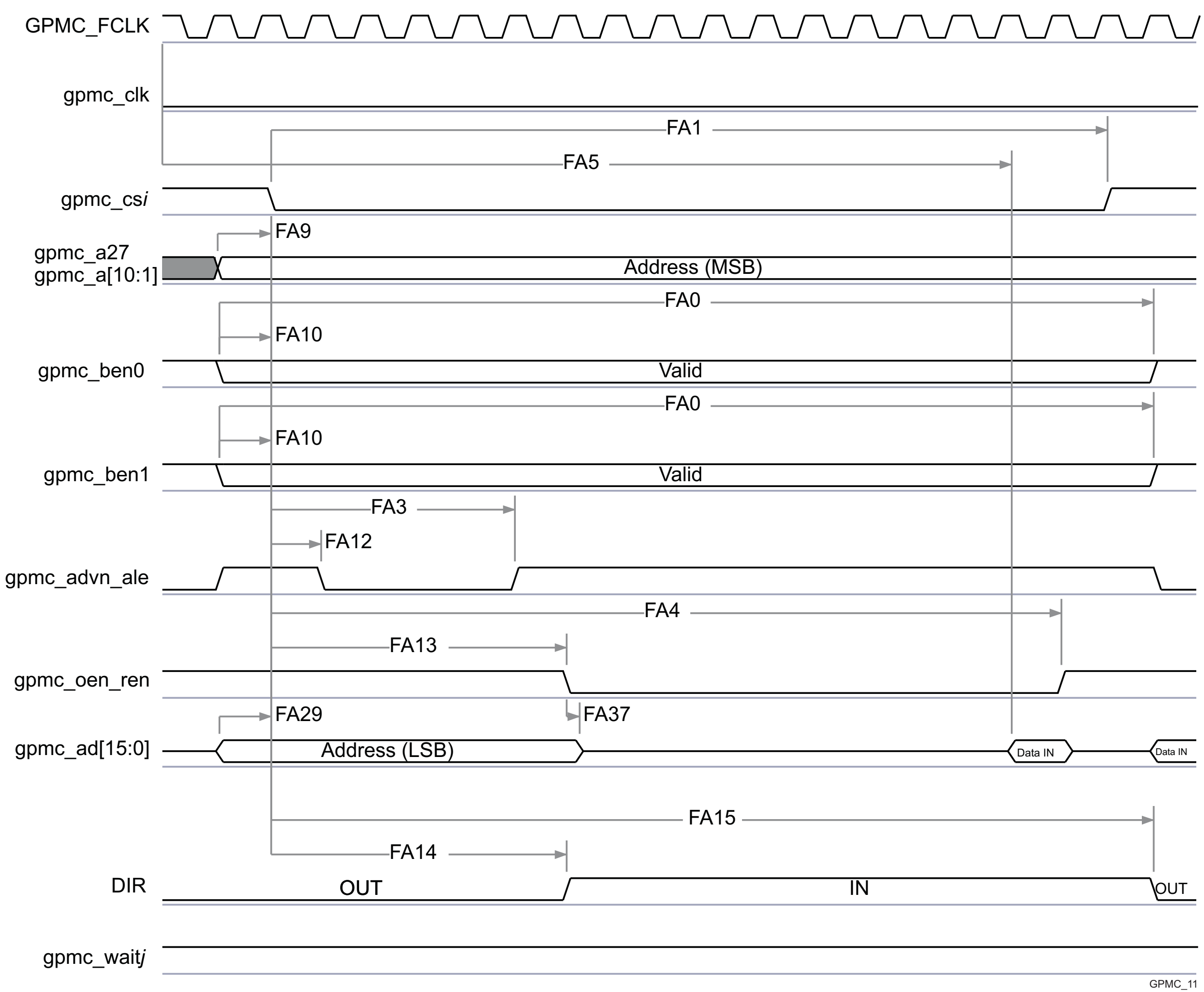


Figure 5-38. GPMC / Multiplexed NOR Flash - Asynchronous Read - Single Word Timing(1)(2)(3)(4)

(1) In gpmc_cs*i*, i = 0 to 7. In gpmc_waitj, j = 0 to 1

(2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value should be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally

(4) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

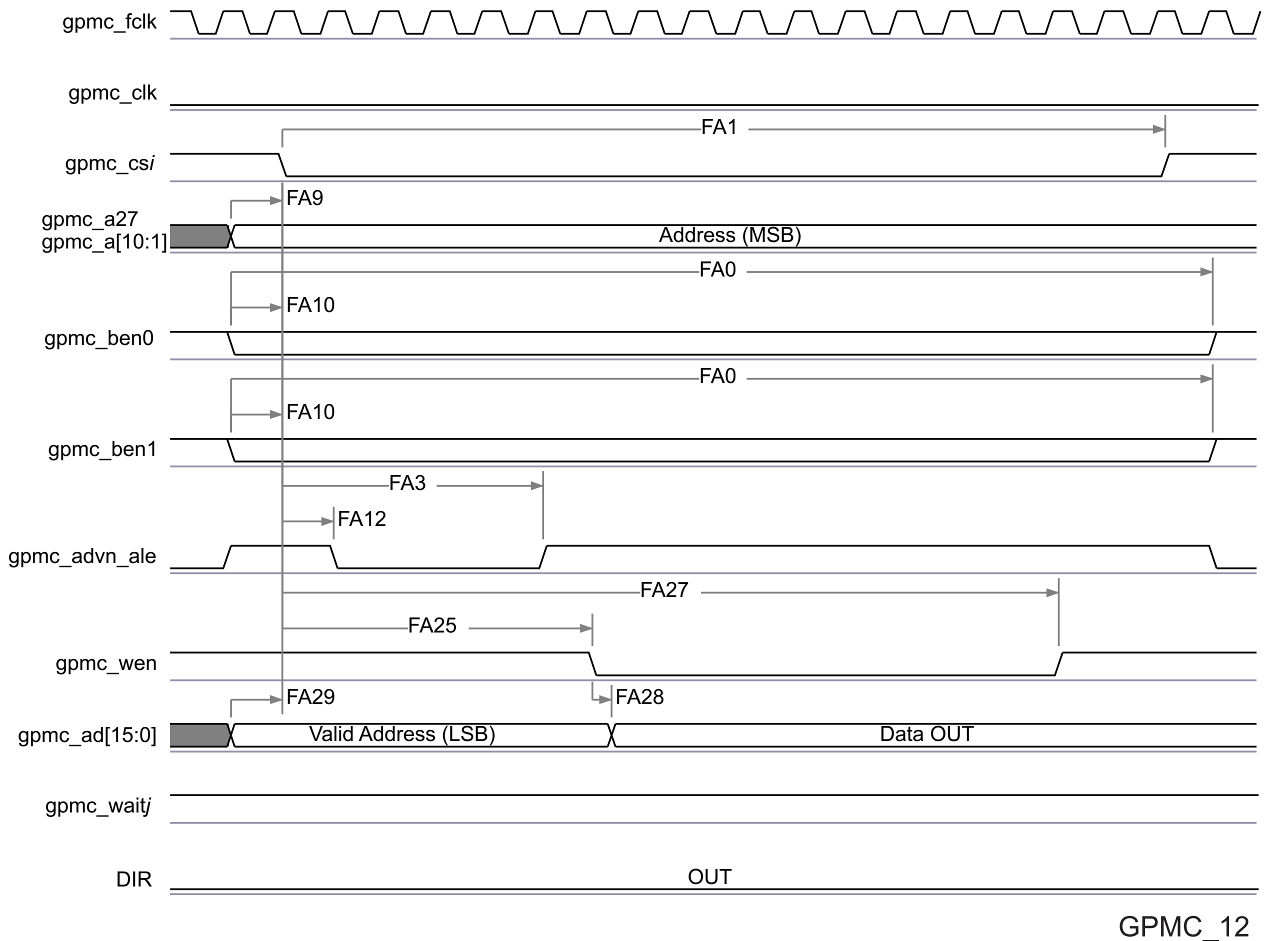


Figure 5-39. GPMC / Multiplexed NOR Flash - Asynchronous Write - Single Word Timing(1)(2)

(1) In gpmc_csi, i = 0 to 7. In gpmc_waitj, j = 0 to 1.

(2) The "DIR" (direction control) output signal is NOT pinned out on any of the device pads. It is an internal signal only representing a signal direction on the GPMC data bus.

5.10.6.7.3 GPMC/NAND Flash Interface Asynchronous Timing

> **CAUTION**
>
> The IO Timings provided in this section are only valid for some GPMC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-60 and Table 5-61 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 5-40, Figure 5-41, Figure 5-42, and Figure 5-43).

Table 5-60. GPMC/NAND Flash Interface Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GNF12	$t_{acc(DAT)}$	Data maximum access time (GPMC_FCLK Cycles)		J [1]	cycles
-	$t_{su(DV-OEH)}$	Setup time, read gpmc_ad[15:0] valid before gpmc_oen_ren high	1.9		ns
-	$t_{h(OEH-DV)}$	Hold time, read gpmc_ad[15:0] valid after gpmc_oen_ren high	1		ns

(1) J = AccessTime * (TimeParaGranularity + 1)

Table 5-61. GPMC/NAND Flash Interface Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GNF0	$t_{w(nWEV)}$	Pulse duration, gpmc_wen valid time		A (1)	ns
GNF1	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_wen valid	B - 2 (2)	B + 4 (2)	ns
GNF2	$t_{d(CLEH-nWEV)}$	Delay time, gpmc_ben[1:0] high to gpmc_wen valid	C - 2 (3)	C + 4 (3)	ns
GNF3	$t_{d(nWEV-DV)}$	Delay time, gpmc_ad[15:0] valid to gpmc_wen valid	D - 2 (4)	D + 4 (4)	ns
GNF4	$t_{d(nWEIV-DIV)}$	Delay time, gpmc_wen invalid to gpmc_ad[15:0] invalid	E - 2 (5)	E + 4 (5)	ns
GNF5	$t_{d(nWEIV-CLEIV)}$	Delay time, gpmc_wen invalid to gpmc_ben[1:0] invalid	F - 2 (6)	F + 4 (6)	ns
GNF6	$t_{d(nWEIV-nCSIV)}$	Delay time, gpmc_wen invalid to gpmc_cs[7:0] invalid	G - 2 (7)	G + 4 (7)	ns
GNF7	$t_{d(ALEH-nWEV)}$	Delay time, gpmc_advn_ale high to gpmc_wen valid	C - 2 (3)	C + 4 (3)	ns
GNF8	$t_{d(nWEIV-ALEIV)}$	Delay time, gpmc_wen invalid to gpmc_advn_ale invalid	F - 2 (6)	F + 4 (6)	ns
GNF9	$t_{c(nWE)}$	Cycle time, write cycle time		H (8)	ns
GNF10	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_cs[7:0] valid to gpmc_oen_ren valid	I - 2 (9)	I + 4 (9)	ns
GNF13	$t_{w(nOEV)}$	Pulse duration, gpmc_oen_ren valid time		K(10)	ns
GNF14	$t_{c(nOE)}$	Cycle time, read cycle time		L(11)	ns
GNF15	$t_{d(nOEIV-nCSIV)}$	Delay time, gpmc_oen_ren invalid to gpmc_cs[7:0] invalid	M - 2(12)	M + 4 (12)	ns

(1) A = (WEOffTime – WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK
(2) B = ((WEOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – CSExtraDelay)) × GPMC_FCLK
(3) C = ((WEOnTime – ADVOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – ADVExtraDelay)) × GPMC_FCLK
(4) D = (WEOnTime × (TimeParaGranularity + 1) + 0.5 × WEExtraDelay) × GPMC_FCLK
(5) E = (WrCycleTime – WEOffTime × (TimeParaGranularity + 1) – 0.5 × WEExtraDelay) × GPMC_FCLK
(6) F = (ADVWrOffTime – WEOffTime × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – WEExtraDelay) × GPMC_FCLK
(7) G = (CSWrOffTime – WEOffTime × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay – WEExtraDelay) × GPMC_FCLK
(8) H = WrCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK
(9) I = ((OEOffTime + (n – 1) × PageBurstAccessTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay – CSExtraDelay)) × GPMC_FCLK
(10) K = (OEOffTime – OEOnTime) × (1 + TimeParaGranularity) × GPMC_FCLK
(11) L = RdCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK
(12) M = (CSRdOffTime – OEOffTime × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay – OEExtraDelay) × GPMC_FCLK

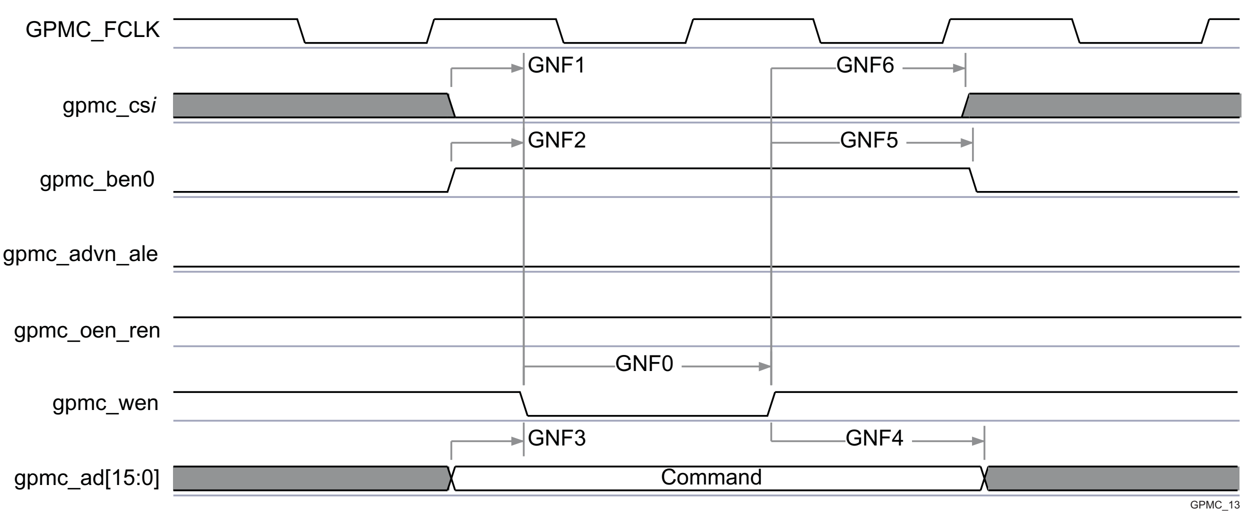


Figure 5-40. GPMC / NAND Flash - Command Latch Cycle Timing(1)

(1) In gpmc_cs*i*, i = 0 to 7.

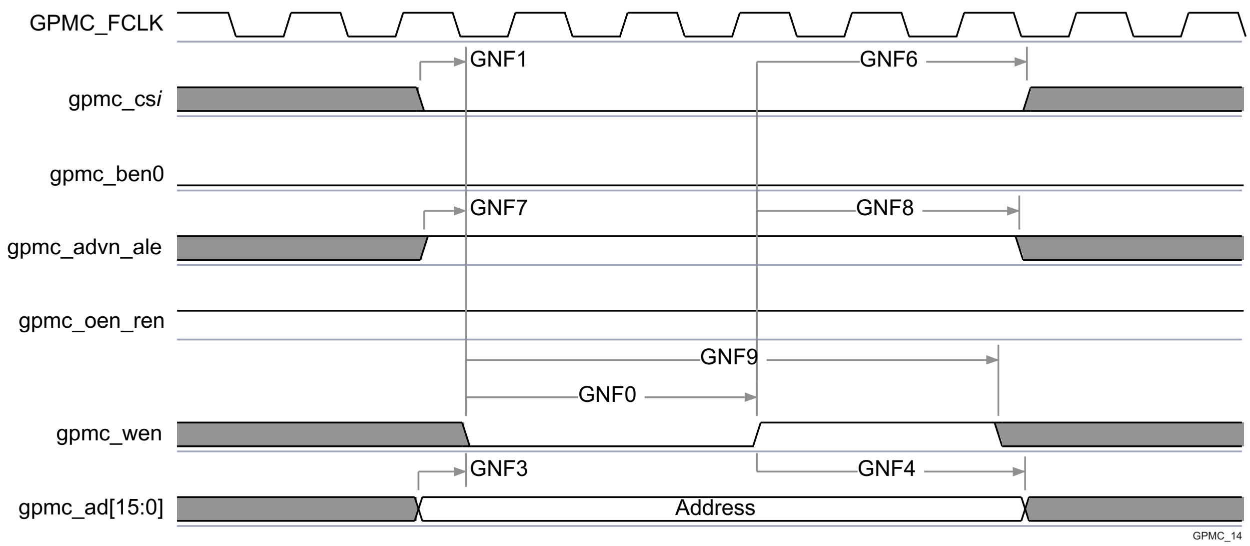


Figure 5-41. GPMC / NAND Flash - Address Latch Cycle Timing[(1)]

(1) In gpmc_cs*i*, i = 0 to 7.

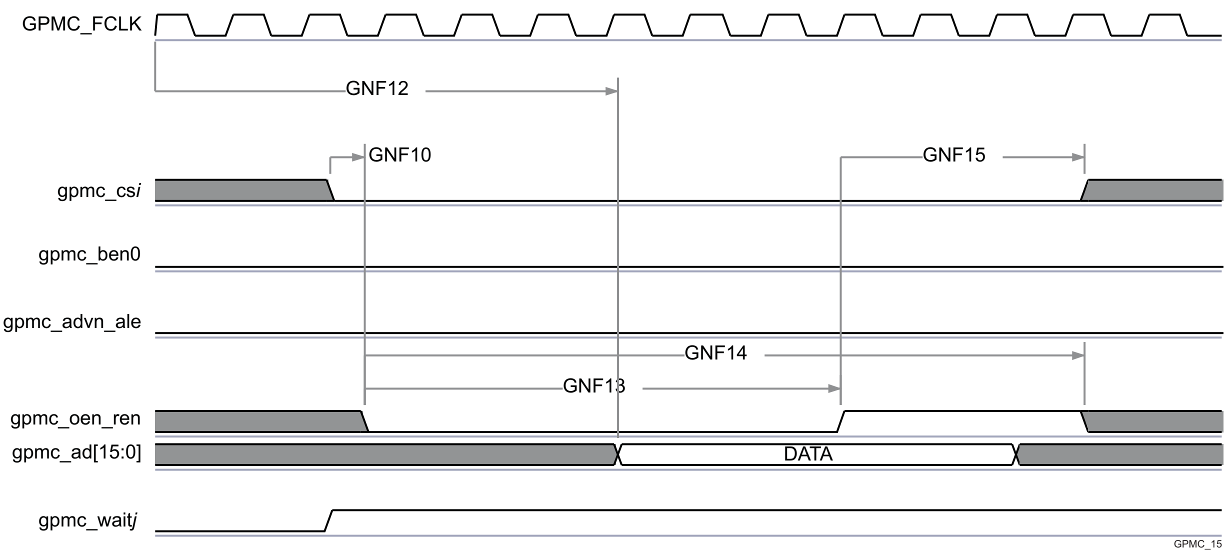


Figure 5-42. GPMC / NAND Flash - Data Read Cycle Timing[(1)(2)(3)]

(1) GNF12 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.

(2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(3) In gpmc_cs*i*, i = 0 to 7. In gpmc_wait*j*, j = 0 to 1.

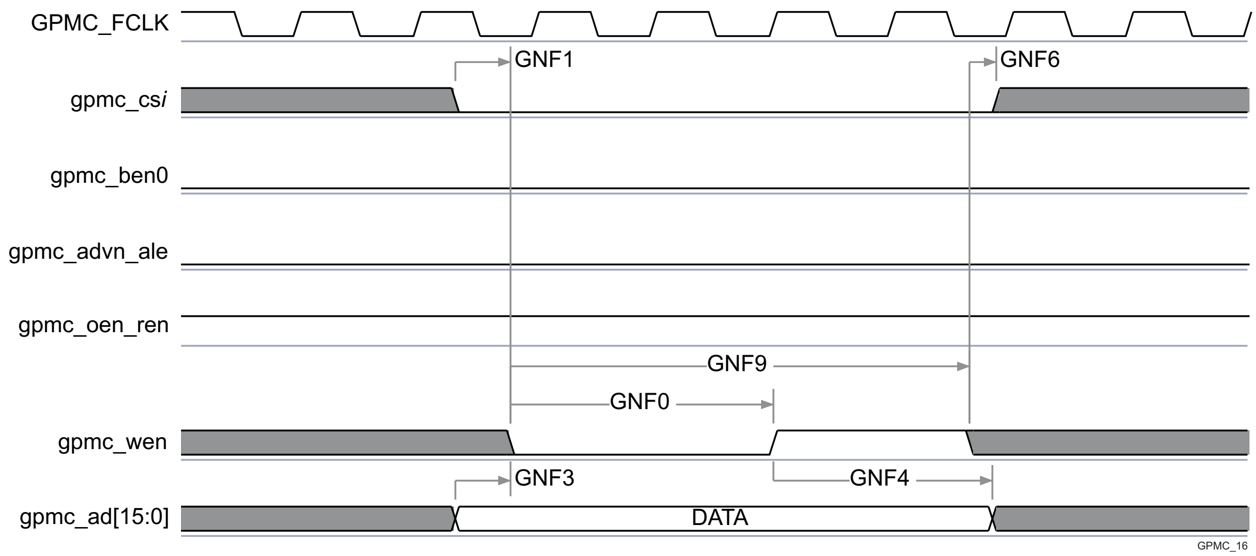


Figure 5-43. GPMC / NAND Flash - Data Write Cycle Timing(1)

(1) In gpmc_cs*i*, i = 0 to 7.

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in Table 4-29 and described in Device TRM, *Chapter 18 - Control Module*.

Virtual IO Timings Modes must be used to guarantee some IO timings for GPMC. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 5-62, *Virtual Functions Mapping for GPMC* for a definition of the Virtual modes.

Table 5-62 presents the values for DELAYMODE bitfield.

Table 5-62. Virtual Functions Mapping for GPMC

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]							
		GPMC_VIRTUAL1	0	1	2	3	5	6	14[1]	14[1]
M6	gpmc_ad0	11	gpmc_ad0							
M2	gpmc_ad1	11	gpmc_ad1							
L5	gpmc_ad2	11	gpmc_ad2							
M1	gpmc_ad3	11	gpmc_ad3							
L6	gpmc_ad4	11	gpmc_ad4							
L4	gpmc_ad5	11	gpmc_ad5							
L3	gpmc_ad6	11	gpmc_ad6							
L2	gpmc_ad7	11	gpmc_ad7							
L1	gpmc_ad8	11	gpmc_ad8							
K2	gpmc_ad9	11	gpmc_ad9							
J1	gpmc_ad10	11	gpmc_ad10							
J2	gpmc_ad11	11	gpmc_ad11							
H1	gpmc_ad12	11	gpmc_ad12							
J3	gpmc_ad13	11	gpmc_ad13							
H2	gpmc_ad14	11	gpmc_ad14							
H3	gpmc_ad15	11	gpmc_ad15							
R6	gpmc_a0	11	gpmc_a0						gpmc_a26	gpmc_a16
T9	gpmc_a1	11	gpmc_a1							
T6	gpmc_a2	11	gpmc_a2							
T7	gpmc_a3	10	gpmc_a3							
P6	gpmc_a4	10	gpmc_a4							
R9	gpmc_a5	11	gpmc_a5							
R5	gpmc_a6	11	gpmc_a6							
P5	gpmc_a7	11	gpmc_a7							
N7	gpmc_a8	12	gpmc_a8							
R4	gpmc_a9	12	gpmc_a9							
N9	gpmc_a10	12	gpmc_a10							
P9	gpmc_a11	11	gpmc_a11							
P4	gpmc_a12	13	gpmc_a12				gpmc_a0			
R3	gpmc_a13	12	gpmc_a13							
T2	gpmc_a14	12	gpmc_a14							
U2	gpmc_a15	12	gpmc_a15							

Table 5-62. Virtual Functions Mapping for GPMC (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]							
		GPMC_VIRTUAL1	0	1	2	3	5	6	14[(1)]	14[(1)]
U1	gpmc_a16	12	gpmc_a16							
P3	gpmc_a17	12	gpmc_a17							
R2	gpmc_a18	12	gpmc_a18							
K7	gpmc_a19	11	gpmc_a19		gpmc_a13					
M7	gpmc_a20	11	gpmc_a20		gpmc_a14					
J5	gpmc_a21	11	gpmc_a21		gpmc_a15					
K6	gpmc_a22	11	gpmc_a22		gpmc_a16					
J7	gpmc_a23	11	gpmc_a23		gpmc_a17					
J4	gpmc_a24	11	gpmc_a24		gpmc_a18					
J6	gpmc_a25	11	gpmc_a25		gpmc_a19					
H4	gpmc_a26	11	gpmc_a26		gpmc_a20					
H5	gpmc_a27	11	gpmc_a27		gpmc_a21					
H6	gpmc_cs1	11	gpmc_cs1		gpmc_a22					
T1	gpmc_cs0	14	gpmc_cs0							
P2	gpmc_cs2	12	gpmc_cs2						gpmc_a23	gpmc_a13
P1	gpmc_cs3	10	gpmc_cs3				gpmc_a1		gpmc_a24	gpmc_a14
P7	gpmc_clk	12	gpmc_clk	gpmc_cs7		gpmc_wait1			gpmc_a20	
N1	gpmc_advn_ale	13	gpmc_advn_ale	gpmc_cs6		gpmc_wait1	gpmc_a2	gpmc_a23	gpmc_a19	
M5	gpmc_oen_ren	14	gpmc_oen_ren							
M3	gpmc_wen	14	gpmc_wen							
N6	gpmc_ben0	11	gpmc_ben0	gpmc_cs4					gpmc_a21	
M4	gpmc_ben1	11	gpmc_ben1	gpmc_cs5			gpmc_a3		gpmc_a22	
N2	gpmc_wait0	14	gpmc_wait0						gpmc_a25	gpmc_a15
E1	vin2a_clk0	11							gpmc_a27	gpmc_a17
H7	vin2a_fld0	11							gpmc_a27	gpmc_a18
G1	vin2a_hsync0	9							gpmc_a27	
F5	vin2a_d8	9							gpmc_a26	
E6	vin2a_d9	9							gpmc_a25	
D3	vin2a_d10	9							gpmc_a24	
F6	vin2a_d11	9							gpmc_a23	
F6	vin2a_d11	9							gpmc_a23	
AG5	vin1a_d11	9					gpmc_a23			

Table 5-62. Virtual Functions Mapping for GPMC (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]							
		GPMC_VIRTUAL1	0	1	2	3	5	6	14[(1)]	14[(1)]
AF2	vin1a_d12	9					gpmc_a24			
AF6	vin1a_d13	9					gpmc_a25			
AF3	vin1a_d14	9					gpmc_a26			
AF4	vin1a_d15	9					gpmc_a27			

(1) Some signals listed are virtual functions that present alternate multiplexing options. These virtual functions are controlled via CTRL_CORE_ALT_SELECT_MUX or CTRL_CORE_VIP_MUX_SELECT registers. For more information on how to use these options, please refer to Device TRM, chapter Control Module, section Pad Configuration Registers.

5.10.6.8 Timers

The device has 16 general-purpose (GP) timers (TIMER1 - TIMER16), two watchdog timers, and a 32-kHz synchronized timer (COUNTER_32K) that have the following features:

- Dedicated input trigger for capture mode and dedicated output trigger/pulse width modulation (PWM) signal
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- On-the-fly read/write register (while counting)

The device has two system watchdog timer (WD_TIMER1 and WD_TIMER2) that have the following features:

- Free-running 32-bit upward counter
- On-the-fly read/write register (while counting)
- Reset upon occurrence of a timer overflow condition

The device includes one instance of the 32-bit watchdog timer: WD_TIMER2, also called the MPU watchdog timer.

The watchdog timer is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

NOTE

For additional information on the Timer Module, see the Device TRM.

5.10.6.9 I2C

The device includes 5 inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module.

NOTE

Note that, on I2C1 and I2C2, due to characteristics of the open drain IO cells, HS mode is not supported

NOTE

Inter-integrated circuit i (i=1 to 5) module is also referred to as I2Ci

NOTE

For more information, see the Multimaster High-Speed I2C Controller section of the Device TRM.

Table 5-63, Table 5-64 and Figure 5-44 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-63. Timing Requirements for I2C Input Timings(1)

NO.	PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
I1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
I2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
I3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
I4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
I5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
I6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100(2)		ns
I7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0(3)	3.45(4)	0(3)	0.9(4)	µs
I8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
I9	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ (5)	300(3)	ns
I10	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ (5)	300(3)	ns
I11	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ (5)	300(3)	ns
I12	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$ (5)	300(3)	ns
I13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
I14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
I15	C_B (5)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

(2) A Fast-mode I^2C-bus™ device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-Bus Specification) before the SCL line is released.

(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

(5) C_B = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

Table 5-64. Timing Requirements for I^2C HS-Mode (I^2C3/4/5 Only)(1)

NO.	PARAMETER	DESCRIPTION	C_b = 100 pF MAX		C_b = 400 pF (2)		UNIT
			MIN	MAX	MIN	MAX	
I1	$t_{c(SCL)}$	Cycle time, SCL	0.294		0.588		µs
I2	$t_{su(SCLH-SDAL)}$	Set-up time, SCL high before SDA low (for a repeated START condition)	160		160		ns
I3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a repeated START condition)	160		160		ns
I4	$t_{w(SCLL)}$	LOW period of the SCLH clock	160		320		ns
I5	$t_{w(SCLH)}$	HIGH period of the SCLH clock	60		120		ns
I6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid vefore SCL high	10		10		ns
I7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0 (3)	70	0 (3)	150	ns
I13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for a STOP condition)	160		160		ns

Table 5-64. Timing Requirements for I²C HS-Mode (I²C3/4/5 Only)[(1)] (continued)

NO.	PARAMETER	DESCRIPTION	C_b = 100 pF MAX		C_b = 400 pF [(2)]		UNIT
			MIN	MAX	MIN	MAX	
I14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	0	10	0	10	ns
I15	C_B [(2)]	Capacitive load for SDAH and SCLH lines		100		400	pF
I16	C_B	Capacitive load for SDAH + SDA line and SCLH + SCL line		400		400	pF

(1) I²C HS-Mode is only supported on I²C3/4/5. I2C HS-Mode is not supported on I²C1/2.

(2) For bus line loads C_B between 100 pF and 400 pF the timing parameters must be linearly interpolated.

(3) A device must internally provide a Data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

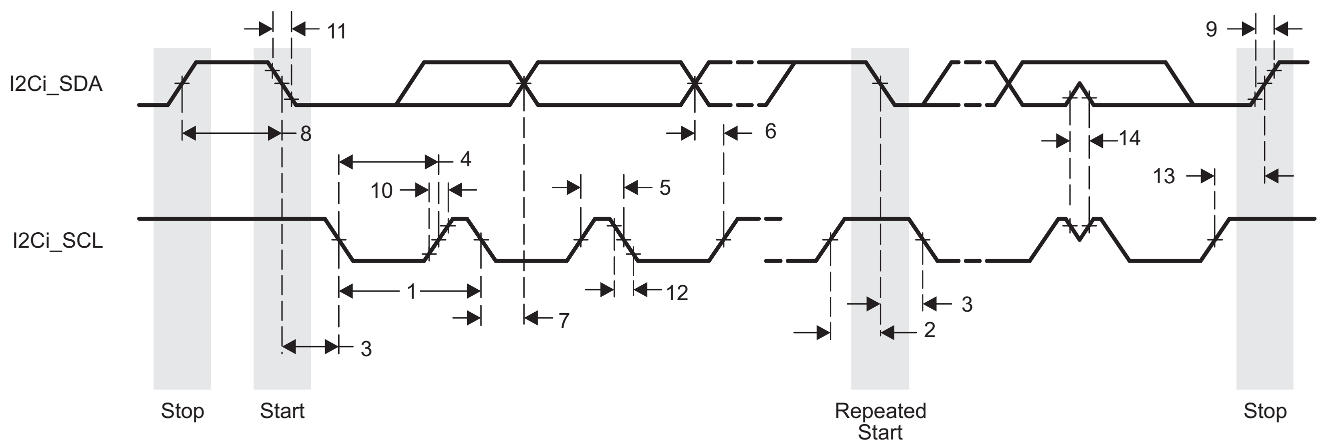


Figure 5-44. I2C Receive Timing

Table 5-65 and Figure 5-45 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-65. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings[(2)]

NO.	PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
I16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
I17	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
I18	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
I19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
I20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
I21	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100		ns
I22	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low (for I2C bus devices)	0	3.45	0	0.9	µs
I23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
I24	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ [(1)] [(3)]	300[(3)]	ns
I25	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ [(1)] [(3)]	300[(3)]	ns
I26	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ [(1)] [(3)]	300[(3)]	ns

Table 5-65. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings(2) (continued)

NO.	PARAMETER	DESCRIPTION	STANDARD MODE MIN	STANDARD MODE MAX	FAST MODE MIN	FAST MODE MAX	UNIT
I27	$t_{f(SCL)}$	Fall time, SCL		300	20 + $0.1C_b$ (1) (3)	300(3)	ns
I28	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
I29	C_p	Capacitance for each I2C pin		10		10	pF

(1) C_B = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

(2) Software must properly configure the I2C module registers to achieve the timings shown in this table. For more details, see the Device TRM.

(3) These timings apply only to I2C1 and I2C2. I2C3, I2C4, and I2C5 use standard LVCMOS buffers to emulate open-drain buffers and their rise/fall times should be referenced in the device IBIS model.

NOTE

I2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic-1.

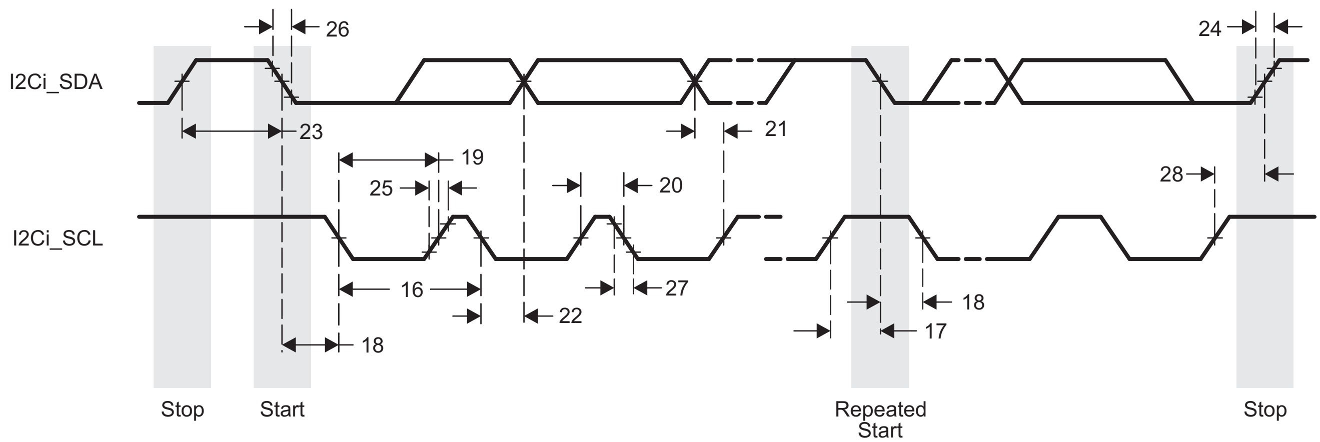


Figure 5-45. I2C Transmit Timing

5.10.6.10 UART

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. There are 10 UART modules in the device. Only one UART supports IrDA features. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices

The UARTi (where i = 1 to 10) include the following features:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Baud generation based on programmable divisors N (where N = 1…16 384) operating from a fixed functional clock of 48 MHz or 192 MHz
- Break character detection and generation
- Configurable data format:
  - Data bit: 5, 6, 7, or 8 bits
  - Parity bit: Even, odd, none
  - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)

- Only UART1 module has extended modem control signals (CD, RI, DTR, DSR)
- Only UART3 supports IrDA

NOTE

For more information, see the UART section of the Device TRM.

Table 5-66, Table 5-67 and Figure 5-46 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-66. Timing Requirements for UART

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
U1	$t_{w(RX)}$	Pulse width, receive data bit, 15/30/100pF high or low	0.96U(1)	1.05U(1)	ns
U2	$t_{w(CTS)}$	Pulse width, receive start bit, 15/30/100pF high or low	0.96U(1)	1.05U(1)	ns
U3	$t_{d(RTS-TX)}$	Delay time, transmit start bit to transmit data	P(2)		ns
U4	$t_{d(CTS-TX)}$	Delay time, receive start bit to transmit data	P(2)		ns

(1) U = UART baud time = 1/programmed baud rate

(2) P = Clock period of the reference clock (FCLK, usually 48 MHz or 192MHz).

Table 5-67. Switching Characteristics Over Recommended Operating Conditions for UART

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
	$f_{(baud)}$	Maximum programmable baud rate	15 pF		12	MHz
			30 pF		0.23	
			100 pF		0.115	
U5	$t_{w(TX)}$	Pulse width, transmit data bit, 15/30/100 pF high or low		U(1) - 2	U(1) + 2	ns
U6	$t_{w(RTS)}$	Pulse width, transmit start bit, 15/30/100 pF high or low		U(1) - 2	U(1) + 2	ns

(1) U = UART baud time = 1/programmed baud rate

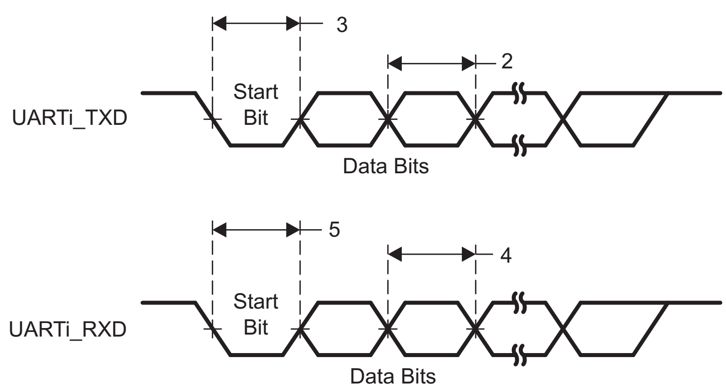


Figure 5-46. UART Timing

5.10.6.11 McSPI

The McSPI is a master/slave synchronous serial bus. There are four separate McSPI modules (SPI1, SPI2, SPI3, and SPI4) in the device. All these four modules support up to four external devices (four chip selects) and are able to work as both master and slave.

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode

- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - SPI configuration per channel. This means, clock definition, polarity enabling and word width
- Power management through wake-up capabilities
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.
- Each SPI module supports multiple chip select pins spim_cs[i], where i = 1 to 4.

NOTE

For more information, see the Serial Communication Interface section of the Device TRM.

NOTE

The McSPIm module (m = 1 to 4) is also referred to as SPIm.

CAUTION

The IO timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are only valid for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETS are defined in the Table 5-70.

Table 5-68, Figure 5-47 and Figure 5-48 present timing requirements for McSPI - Master Mode.

Table 5-68. Timing Requirements for SPI - Master Mode (1)(8)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, spi_sclk (1) (2)	SPI1/2/3/4	20.8 (3)		ns
SM2	$t_{w(SPICLKL)}$	Typical Pulse duration, spi_sclk low (1)		0.5*P-1 (4)		ns
SM3	$t_{w(SPICLKH)}$	Typical Pulse duration, spi_sclk high (1)		0.5*P-1 (4)		ns
SM4	$t_{su(MISO-SPICLK)}$	Setup time, spi_d[x] valid before spi_sclk active edge (1)		4.4		ns
SM5	$t_{h(SPICLK-MISO)}$	Hold time, spi_d[x] valid after spi_sclk active edge (1)		3.9		ns
SM6	$t_{d(SPICLK-SIMO)}$	Delay time, spi_sclk active edge to spi_d[x] transition (1)	SPI1	-4.27	4.27	ns
			SPI2	-4.32	4.32	ns
			SPI3	-5.37	4.23	ns
			SPI4	-3.81	4.41	ns
SM7	$t_{d(CS-SIMO)}$	Delay time, spi_cs[x] active edge to spi_d[x] transition			5	ns
SM8	$t_{d(CS-SPICLK)}$	Delay time, spi_cs[x] active to spi_sclk first edge (1)	MASTER_PHA0 (5)	B-4.6 (6)		ns
			MASTER_PHA1 (5)	A-4.6 (7)		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, spi_sclk last edge to spi_cs[x] inactive (1)	MASTER_PHA0 (5)	A-4.6 (7)		ns
			MASTER_PHA1 (5)	B-4.6 (6)		ns

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) Related to the SPI_CLK maximum frequency.
(3) 20.8 ns cycle time = 48 MHz
(4) P = SPICLK period.
(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.
(6) B = (TCS + 0.5) × TSPICLKREF × Fratio, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even ≥ 2.
(7) When P = 20.8 ns, A = (TCS + 1) × TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) × Fratio × TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(8) The IO timings provided in this section are applicable for all combinations of signals for spi1 and spi2. However, the timings are only valid for spi3 and spi4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.

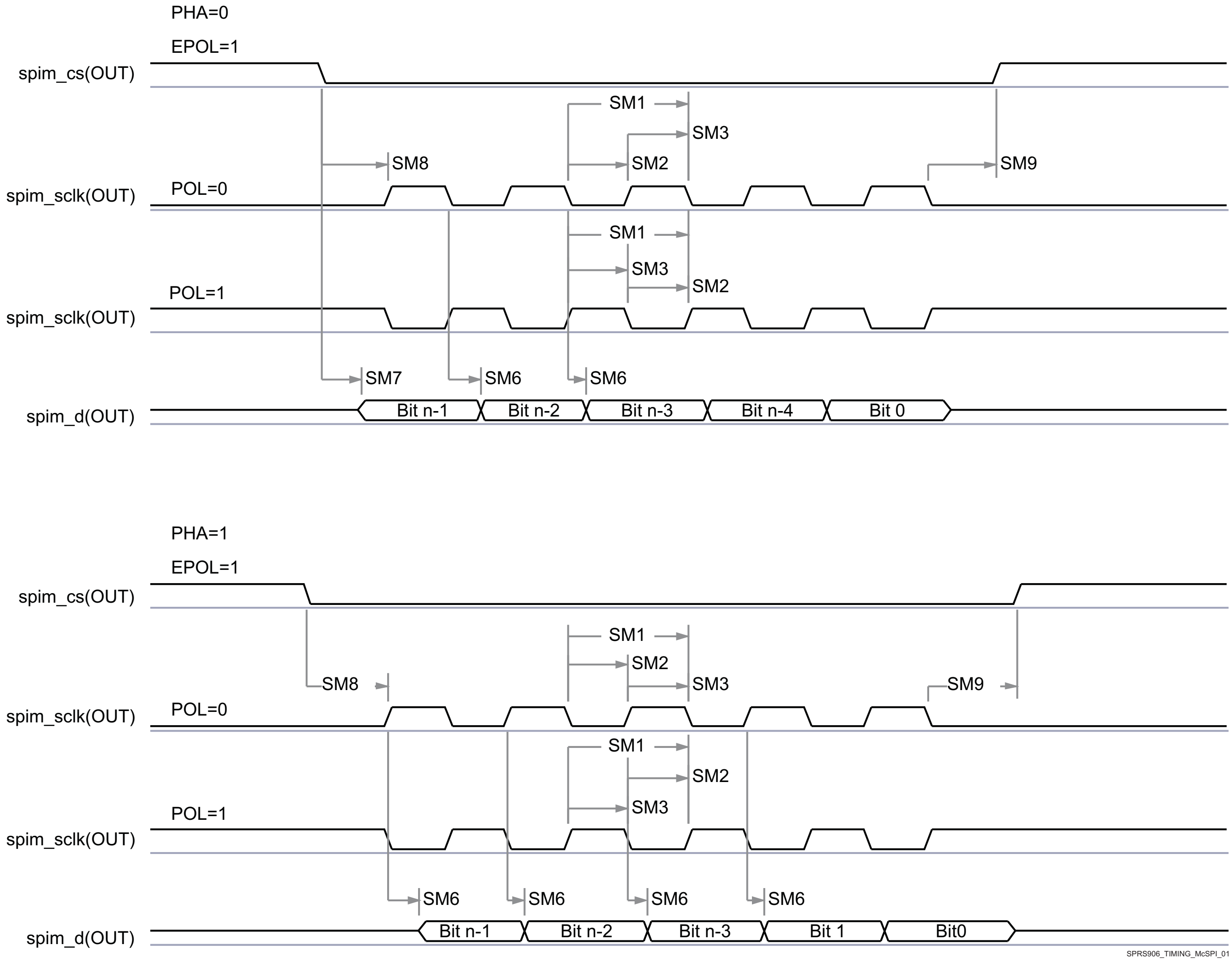


Figure 5-47. McSPI - Master Mode Transmit

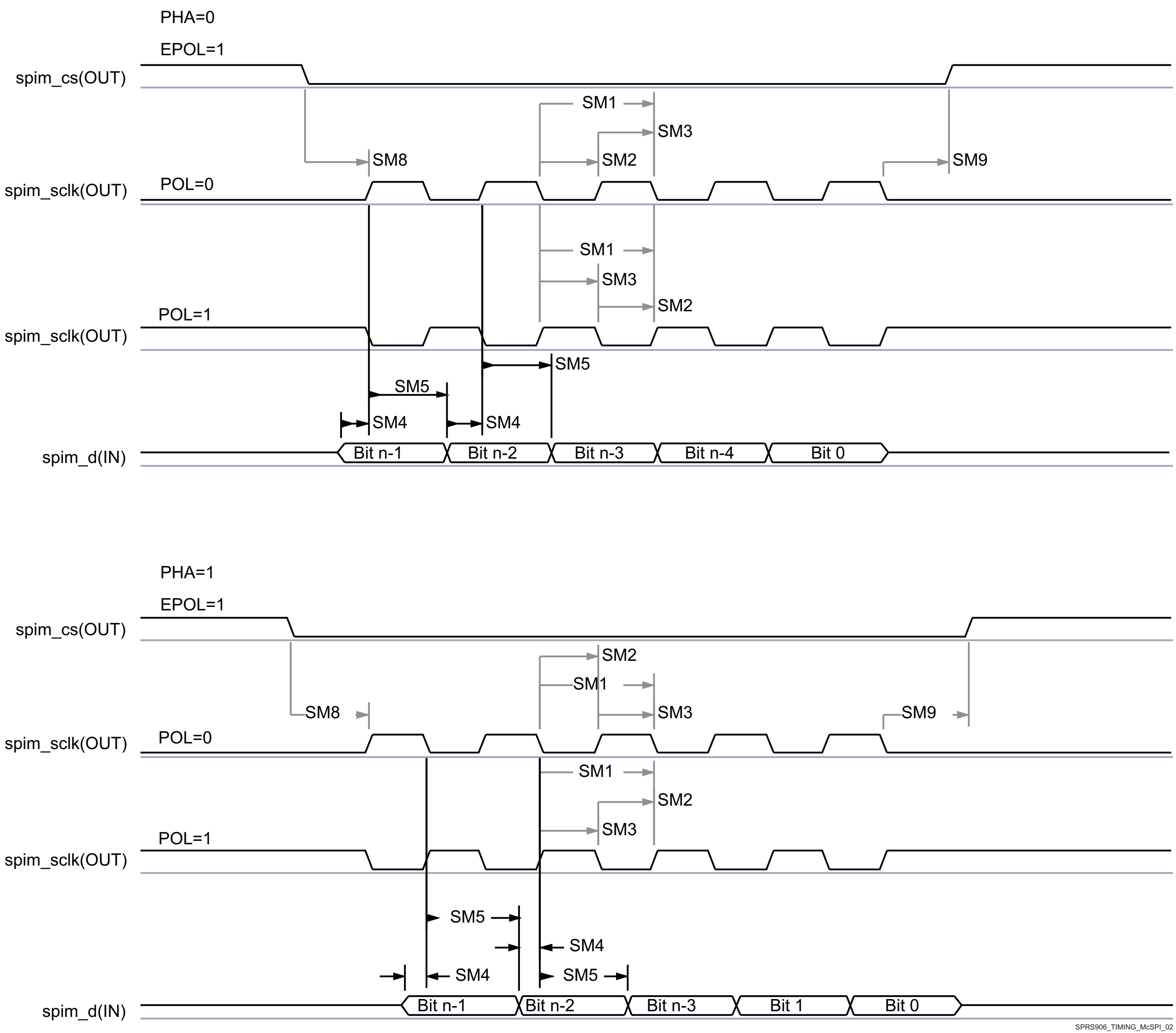


Figure 5-48. McSPI - Master Mode Receive

Table 5-69, Figure 5-49 and Figure 5-50 present timing requirements for McSPI - Slave Mode.

Table 5-69. Timing Requirements for SPI - Slave Mode(6)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, spi_sclk (1) (2)		62.5(3)		ns
SS2	$t_{w(SPICLKL)}$	Typical Pulse duration, spi_sclk low (1)		0.45P (4)		ns
SS3	$t_{w(SPICLKH)}$	Typical Pulse duration, spi_sclk high (1)		0.45P (4)		ns
SS4(1)	$t_{su(SIMO-SPICLK)}$	Setup time, spi_d[x] valid before spi_sclk active edge		5		ns
SS5(1)	$t_{h(SPICLK-SIMO)}$	Hold time, spi_d[x] valid after spi_sclk active edge		5		ns
SS6(1)	$t_{d(SPICLK-SOMI)}$	Delay time, spi_sclk active edge to mcspi_somi transition	SPI1/2/3	2	26.1	ns
			SPI4	2	18	ns
SS7(5)	$t_{d(CS-SOMI)}$	Delay time, spi_cs[x] active edge to mcspi_somi transition			20.95	ns
SS8(1)	$t_{su(CS-SPICLK)}$	Setup time, spi_cs[x] valid before spi_sclk first edge		5		ns
SS9(1)	$t_{h(SPICLK-CS)}$	Hold time, spi_cs[x] valid after spi_sclk last edge		5		ns

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) When operating the SPI interface in RX-only mode, the minimum Cycle time is 26 ns (38.4 MHz)
(3) 62.5 ns Cycle time = 16 MHz
(4) P = SPICLK period.
(5) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.
(6) The IO timings provided in this section are applicable for all combinations of signals for spi1 and spi2. However, the timings are only valid for spi3 and spi4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.

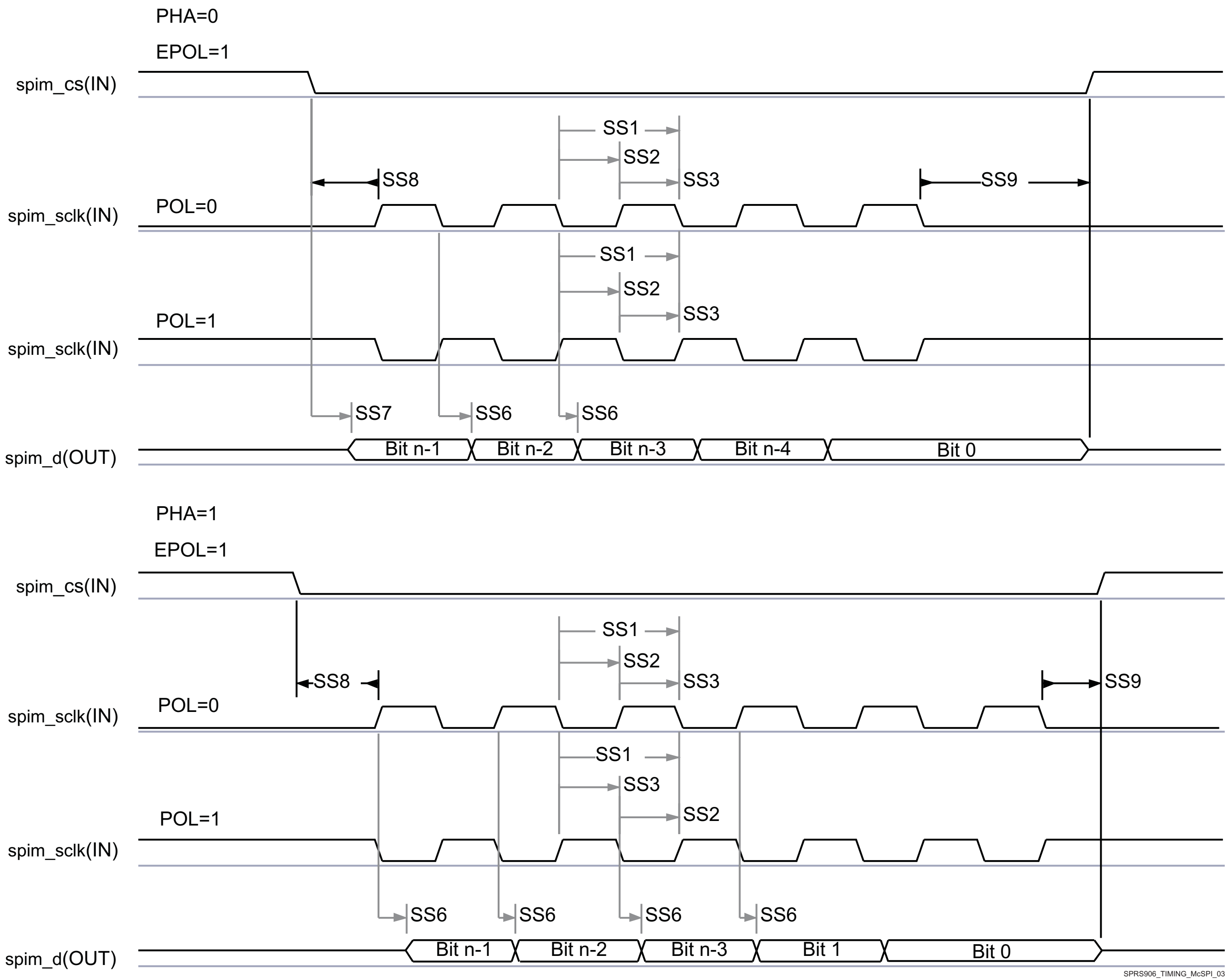


Figure 5-49. McSPI - Slave Mode Transmit

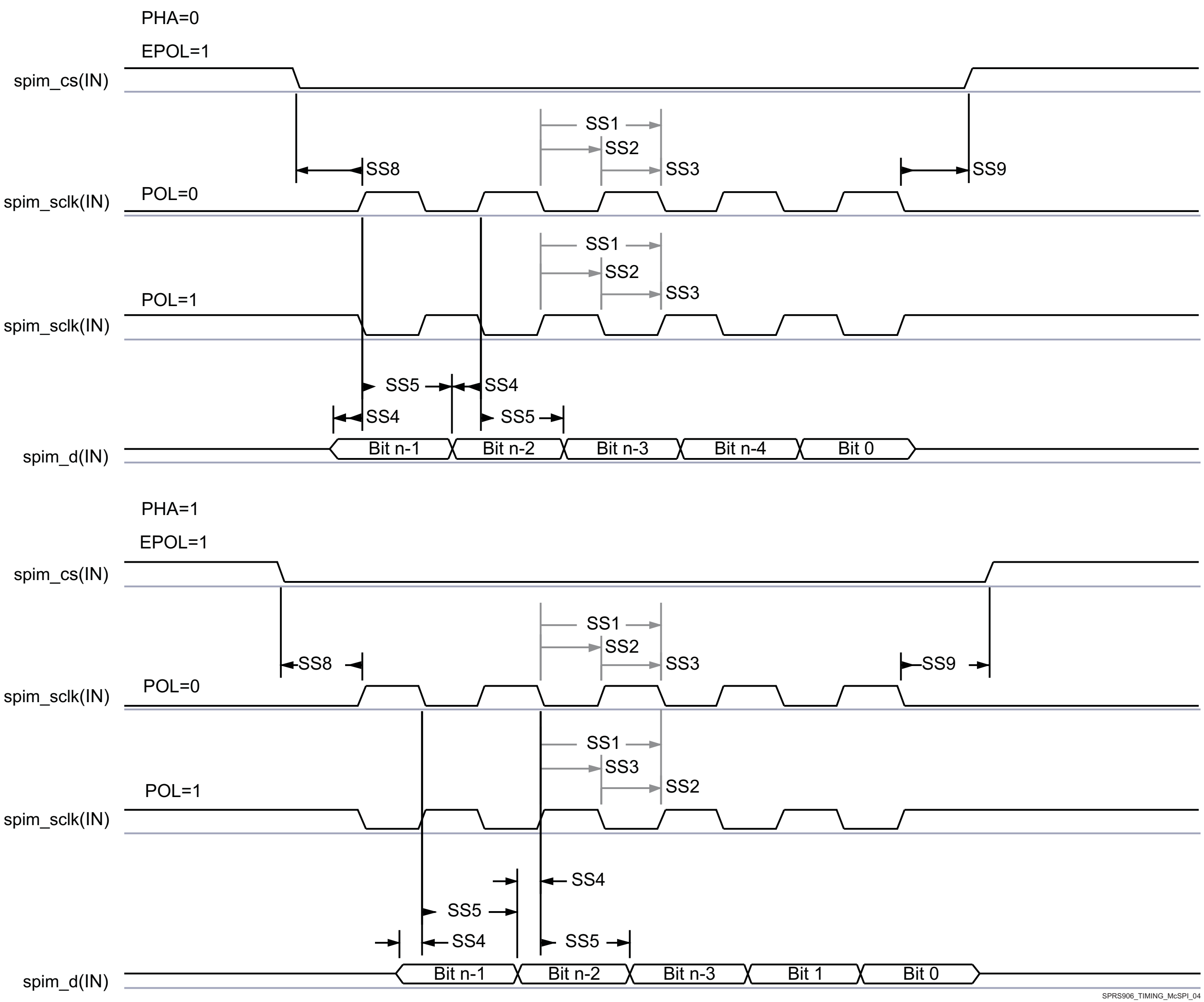


Figure 5-50. McSPI - Slave Mode Receive

In Table 5-70 are presented the specific groupings of signals (IOSET) for use with SPI3 and SPI4.

Table 5-70. McSPI3/4 IOSETs

Signal	IOSET1		IOSET2		IOSET3		IOSET4		IOSET5		IOSET6	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
SPI3												
spi3_sclk	AD9	8	E11	8	V2	7	B12	3	C18	2	AC4	1
spi3_d1	AF9	8	B10	8	Y1	7	A11	3	A21	2	AC7	1
spi3_d0	AE9	8	C11	8	W9	7	B13	3	G16	2	AC6	1
spi3_cs0	AF8	8	D11	8	V9	7	A12	3	D17	2	AC9	1
spi3_cs1	AC3	1	B11	8	AC3	1	E14	3	B11	8	AC3	1
spi3_cs2	-	-	F11	8	-	-	F11	8	F11	8	-	-
spi3_cs3	-	-	A10	8	-	-	A10	8	A10	8	-	-
SPI4												
spi4_sclk	N7	8	G1	8	V7	7	AA3	2	AC8	1	-	-

Table 5-70. McSPI3/4 IOSETs (continued)

Signal	IOSET1		IOSET2		IOSET3		IOSET4		IOSET5		IOSET6	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
spi4_d1	R4	8	G6	8	U7	7	AB9	2	AD6	1	-	-
spi4_d0	N9	8	F2	8	V6	7	AB3	2	AB8	1	-	-
spi4_cs0	P9	8	F3	8	U6	7	AA4	2	AB5	1	-	-
spi4_cs1	P4	8	P4	8	Y1	8	Y1	8	Y1	8	-	-
spi4_cs2	R3	8	R3	8	W9	8	W9	8	W9	8	-	-
spi4_cs3	T2	8	T2	8	V9	8	V9	8	V9	8	-	-

5.10.6.12 QSPI

The Quad SPI (QSPI) module is a type of SPI module that allows single, dual or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. It works as a master only. There is one QSPI module in the device and it is primary intended for fast booting from quad-SPI flash memories.

General SPI features:

- Programmable clock divider
- Six pin interface (DCLK, CS_N, DOUT, DIN, QDIN1, QDIN2)
- 4 external chip select signals
- Support for 3-, 4- or 6-pin SPI interface
- Programmable CS_N to DOUT delay from 0 to 3 DCLKs
- Programmable signal polarities
- Programmable active clock edge
- Software controllable interface allowing for any type of SPI transfer

NOTE

For more information, see the Quad Serial Peripheral Interface section of the Device TRM.

CAUTION

The IO Timings provided in this section are only valid for some QSPI usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

CAUTION

The IO Timings provided in this section are only valid when all QSPI Chip Selects used in a system are configured to use the same Clock Mode (either Clock Mode 0 or Clock Mode3).

Table 5-71 and Table 5-72 present timing and switching characteristics for Quad SPI interface.

Table 5-71. Switching Characteristics for QSPI

No	PARAMETER	DESCRIPTION	Mode	MIN	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	Manual IO Timing Modes, Clock Mode 0	10.41		ns
			Manual IO Timing Modes, Clock Mode 3	13.02		ns
			Bootmode, Clock Mode 3	20.8		
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	All	Y×P-1 (1)		ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	All	Y×P-1 (1)		ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge, CS3:0	Manual IO Timing Modes	-M×P-1 (2) (3)	-M×P+2 (2) (3)	ns
			Bootmode	-M×P-2.5 (2) (3)	-M×P+2.5 (2) (3)	
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge, CS3:0	Manual IO Timing Modes	N×P-1 (2) (3)	N×P+2 (2) (3)	ns
			Bootmode	N×P-2.5 (2) (3)	N×P+2.5 (2) (3)	
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[0] transition	Manual IO Timing Modes	-1	2	ns
			Bootmode	-2.5	2.5	
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)	All	-P-3.5	-P+2.5	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[0] tri-stated (Hi-Z)	All	-P-2.5	-P+2.0	ns
Q9	$t_{d(SCLK-D0)}$	Delay time, sclk first falling edge to first d[0] transition	Manual IO Timing Modes, PHA=0 Only	-1-P	2-P	ns
			Bootmode, PHA=0 Only	-2.5-P	2.5-P	

(1) The Y parameter is defined as follows:
If DCLK_DIV is 0 or ODD then, Y equals 0.5.
If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1).
For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2_H13 output of DPLL_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK_DIV can be found in the Device TRM.

(2) P = SCLK period.

(3) M = QSPI_SPI_DC_REG.DDx + 1 when Clock Mode 0.
M = QSPI_SPI_DC_REG.DDx when Clock Mode 3.
N = 2 when Clock Mode 0.
N = 3 when Clock Mode 3.

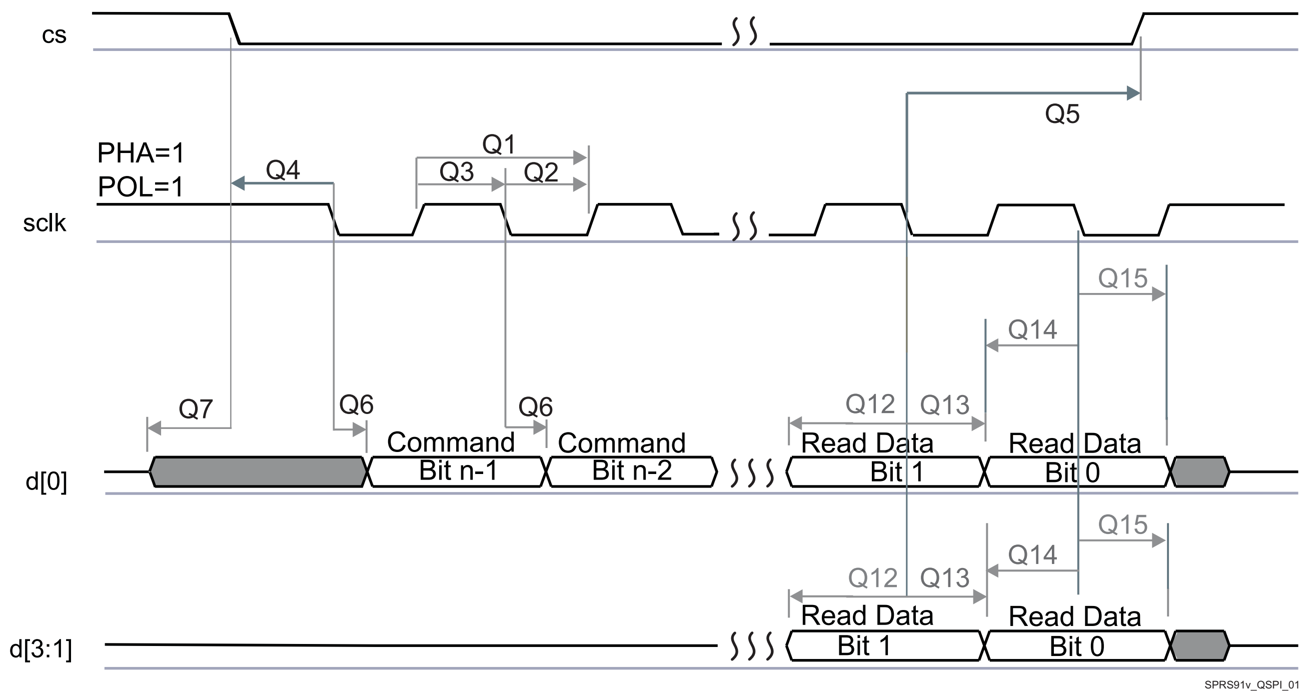


Figure 5-51. QSPI Read (Clock Mode 3)

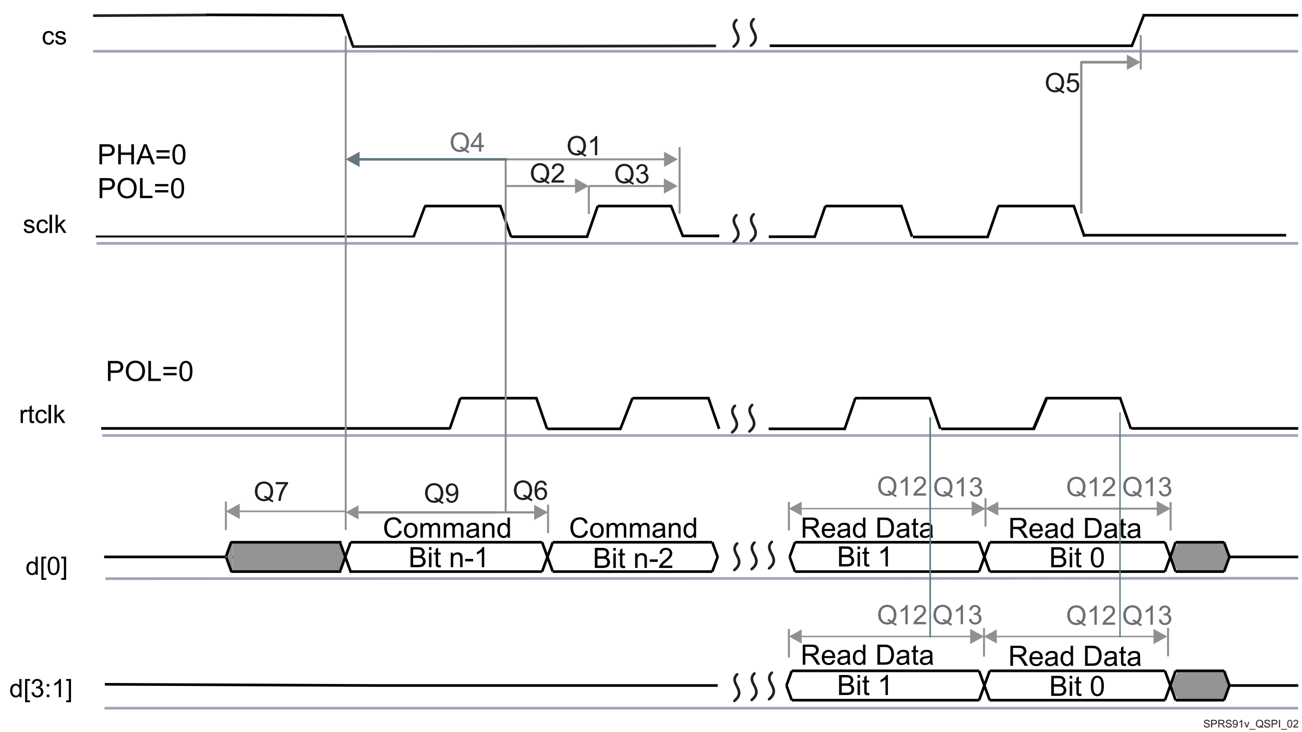


Figure 5-52. QSPI Read (Clock Mode 0)

CAUTION

The IO Timings provided in this section are only valid for some QSPI usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-72. Timing Requirements for QSPI(2)(3)

No	PARAMETER	DESCRIPTION	Mode	MIN	MAX	UNIT
Q12	$t_{su(D-RTCLK)}$	Setup time, d[3:0] valid before falling rtclk edge	Manual IO Timing Modes, Clock Mode 0	2.9		ns
	$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge	Manual IO Timing Modes, Clock Mode 3	5.7		ns
			Boot Mode, Clock Mode 3	12.3		ns
Q13	$t_{h(RTCLK-D)}$	Hold time, d[3:0] valid after falling rtclk edge	Manual IO Timing Mode, Clock Mode 0	-0.1		ns
	$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge	Manual IO Timing Mode, Clock Mode 3	0.1		ns
			Boot Mode, Clock Mode 3	0.1		ns
Q14	$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	Manual IO Timing Mode, Clock Mode 3	5.7-P (1)		ns
			Boot Mode, Clock Mode 3	12.3-P (1)		ns
Q15	$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	Manual IO Timing Mode, Clock Mode 3	0.1+P (1)		ns
			Boot Mode, Clock Mode 3	0.1+P (1)		ns

(1) P = SCLK period.

(2) Clock Modes 1 and 2 are not supported.

(3) The Device captures data on the falling clock edge in Clock Mode 0 and 3, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Modes 0 and 3.

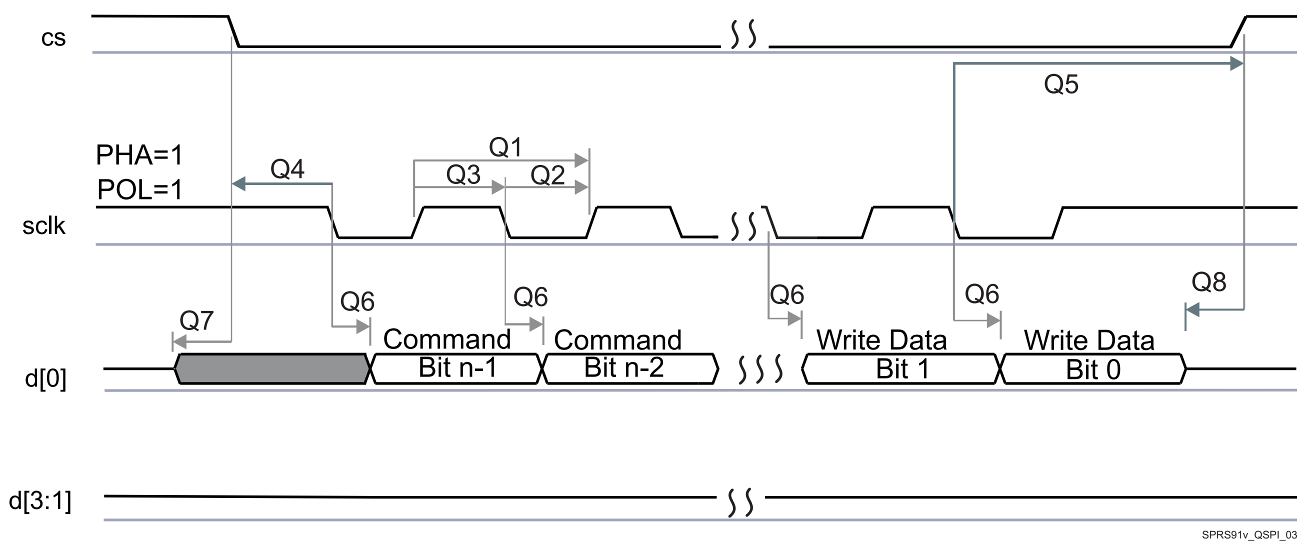


Figure 5-53. QSPI Write (Clock Mode 3)

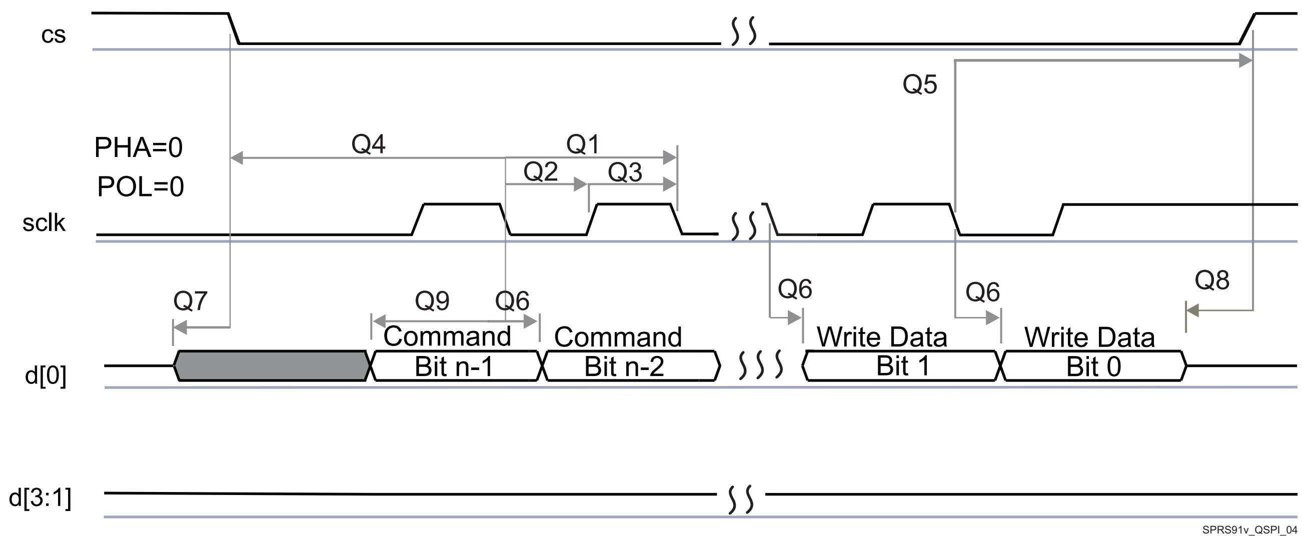


Figure 5-54. QSPI Write (Clock Mode 0)

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for QSPI. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-73, *Manual Functions Mapping for QSPI* for a definition of the Manual modes.

Table 5-73 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-73. Manual Functions Mapping for QSPI

BALL	BALL NAME	QSPI_MODE0_MANUAL1		QSPI_MODE3_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		1
R3	gpmc_a13	0	0	0	0	CFG_GPMC_A13_IN	qspi1_rtclk
T2	gpmc_a14	2149	1052	0	0	CFG_GPMC_A14_IN	qspi1_d3
U2	gpmc_a15	2121	997	0	0	CFG_GPMC_A15_IN	qspi1_d2
U1	gpmc_a16	2159	1134	0	0	CFG_GPMC_A16_IN	qspi1_d0
U1	gpmc_a16	0	0	0	0	CFG_GPMC_A16_OUT	qspi1_d0
P3	gpmc_a17	2135	1085	0	0	CFG_GPMC_A17_IN	qspi1_d1
R2	gpmc_a18	0	0	151	0	CFG_GPMC_A18_OUT	qspi1_sclk
T7	gpmc_a3	0	0	0	0	CFG_GPMC_A3_OUT	qspi1_cs2
P6	gpmc_a4	0	0	0	0	CFG_GPMC_A4_OUT	qspi1_cs3
P2	gpmc_cs2	0	0	0	0	CFG_GPMC_CS2_OUT	qspi1_cs0
P1	gpmc_cs3	0	0	22	0	CFG_GPMC_CS3_OUT	qspi1_cs1

5.10.6.13 McASP

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

The device have integrated 8 McASP modules (McASP1-McASP8) with:configure the desired virtual

- McASP1 and McASP2 modules supporting 16 channels with independent TX/RX clock/sync domain
- McASP3 through McASP8 modules supporting 4 channels with independent TX/RX clock/sync domain

NOTE

For more information, see the Multichannel Audio Serial Port section of the Device TRM.

CAUTION

The IO Timings provided in this section are only valid for some McASP usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-74, Table 5-75, Table 5-76, and Figure 5-55 present timing requirements for McASP1 to McASP8.

Table 5-74. Timing Requirements for McASP1 (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
ASP2	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.35P (2)		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R(3) - 3		ns
ASP5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSR/X input valid before ACLKR/X	ACLKR/X int	20		ns
			ACLKR/X ext in ACLKR/X ext out	4		ns
ASP6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSR/X input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	2.21		ns
ASP7	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKR/X	ACLKR/X int	21.9		ns
			ACLKR/X ext in ACLKR/X ext out	4.42		ns
ASP8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	2.52		ns

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

Table 5-75. Timing Requirements for McASP2 (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
ASP2	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.35P (2)		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X	Any Other Conditions	20		ns
			ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs "80M" Virtual IO Timing Mode	12.5		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low	Any Other Conditions	0.5R(3) - 3		ns
			ACLKX/AFSX (In Sync Mode), ACLKR/AFSR (In Async Mode), and AXR are all inputs "80M" Virtual IO Timing Modes	0.38R (3)		ns
ASP5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSR/X input valid before ACLKR/X	ACLKR/X int	20.7		ns
			ACLKR/X ext in ACLKR/X ext out	3.9		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns
ASP6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSR/X input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	3.2		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns

Table 5-75. Timing Requirements for McASP2 (1) (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP7	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKR/X	ACLKR/X int	21.4		ns
			ACLKR/X ext in ACLKR/X ext out	3.9		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns
ASP8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	3.2		ns
			ACLKR/X ext in ACLKR/X ext out "80M" Virtual IO Timing Modes	3		ns

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

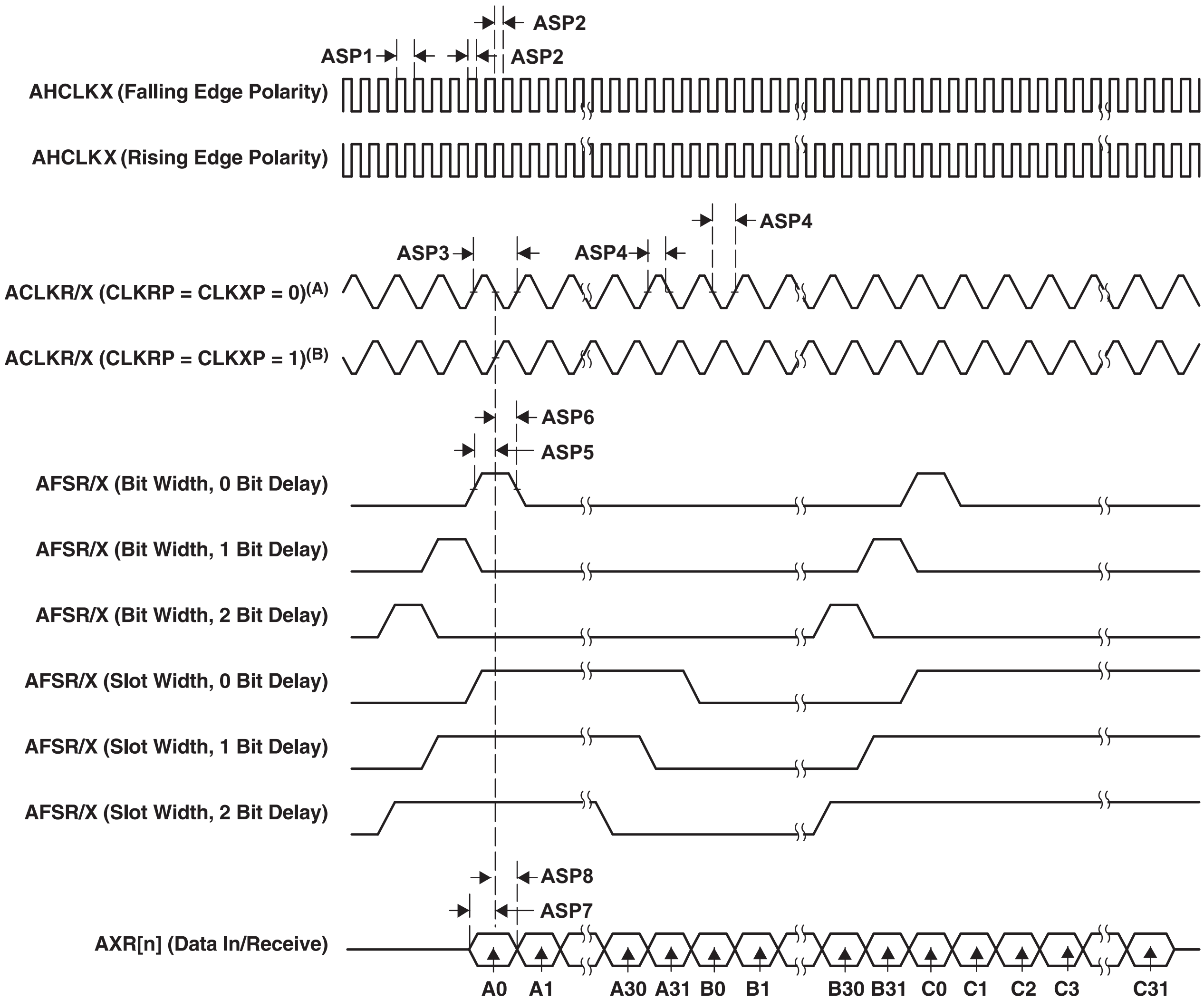
Table 5-76. Timing Requirements for McASP3/4/5/6/7/8 (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
ASP2	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.35P (2)		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R(3) - 3		ns
ASP5	$t_{su(AFSRX-ACLK)}$	Setup time, AFSR/X input valid before ACLKR/X	ACLKR/X int	20.2		ns
			ACLKR/X ext in ACLKR/X ext out	4.9		ns
ASP6	$t_{h(ACLK-AFSRX)}$	Hold time, AFSR/X input valid after ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in ACLKR/X ext out	2.26		ns
ASP7	$t_{su(AXR-ACLK)}$	Setup time, AXR input valid before ACLKX	ACLKX int (ASYNC = 0)	20.8		ns
			ACLKR/X ext in ACLKR/X ext out	5.75		ns
ASP8	$t_{h(ACLK-AXR)}$	Hold time, AXR input valid after ACLKX	ACLKX int (ASYNC = 0)	-0.9		ns
			ACLKR/X ext in ACLKR/X ext out	2.87		ns

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1 (NOT SUPPORTED)
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.



A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

Figure 5-55. McASP Input Timing

CAUTION

The IO Timings provided in this section are only valid for some McASP usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-77, Table 5-78, Table 5-79, and Figure 5-56 present switching characteristics over recommended operating conditions for McASP1 to McASP8.

Table 5-77. Switching Characteristics Over Recommended Operating Conditions for McASP1 (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
ASP10	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.5P - 2.5 (2)		ns

Table 5-77. Switching Characteristics Over Recommended Operating Conditions for McASP1 [(1)] (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP11	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R[(3)] - 2.5		ns
ASP13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int	-0.21	6	ns
			ACLKR/X ext in ACLKR/X ext out	2	23.9	ns
ASP14	$t_{d(ACLK-AXR)}$	Delay time, ACLKR/X transmit edge to AXR output valid	ACLKR/X int	-1.8	6.9	ns
			ACLKR/X ext in ACLKR/X ext out	2	25.6	ns

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

Table 5-78. Switching Characteristics Over Recommended Operating Conditions for McASP2 [(1)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
ASP10	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.5P - 2.5 [(2)]		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R[(3)] - 2.5		ns
ASP13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int	0	6	ns
			ACLKR/X ext in ACLKR/X ext out	2	25.2	ns
ASP14	$t_{d(ACLK-AXR)}$	Delay time, ACLKR/X transmit edge to AXR output valid	ACLKR/X int	-1.29	6.11	ns
			ACLKR/X ext in ACLKR/X ext out	2	24.8	ns

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.

Table 5-79. Switching Characteristics Over Recommended Operating Conditions for McASP3/4/5/6/7/8 [(1)]

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKX)}$	Cycle time, AHCLKX		20		ns
ASP10	$t_{w(AHCLKX)}$	Pulse duration, AHCLKX high or low		0.5P - 2.5 [(2)]		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, ACLKR/X		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, ACLKR/X high or low		0.5R[(3)] - 2.5		ns
ASP13	$t_{d(ACLK-AFSXR)}$	Delay time, ACLKR/X transmit edge to AFSX/R output valid	ACLKR/X int	-0.74	6	ns
			ACLKR/X ext in ACLKR/X ext out	2	26.4	ns

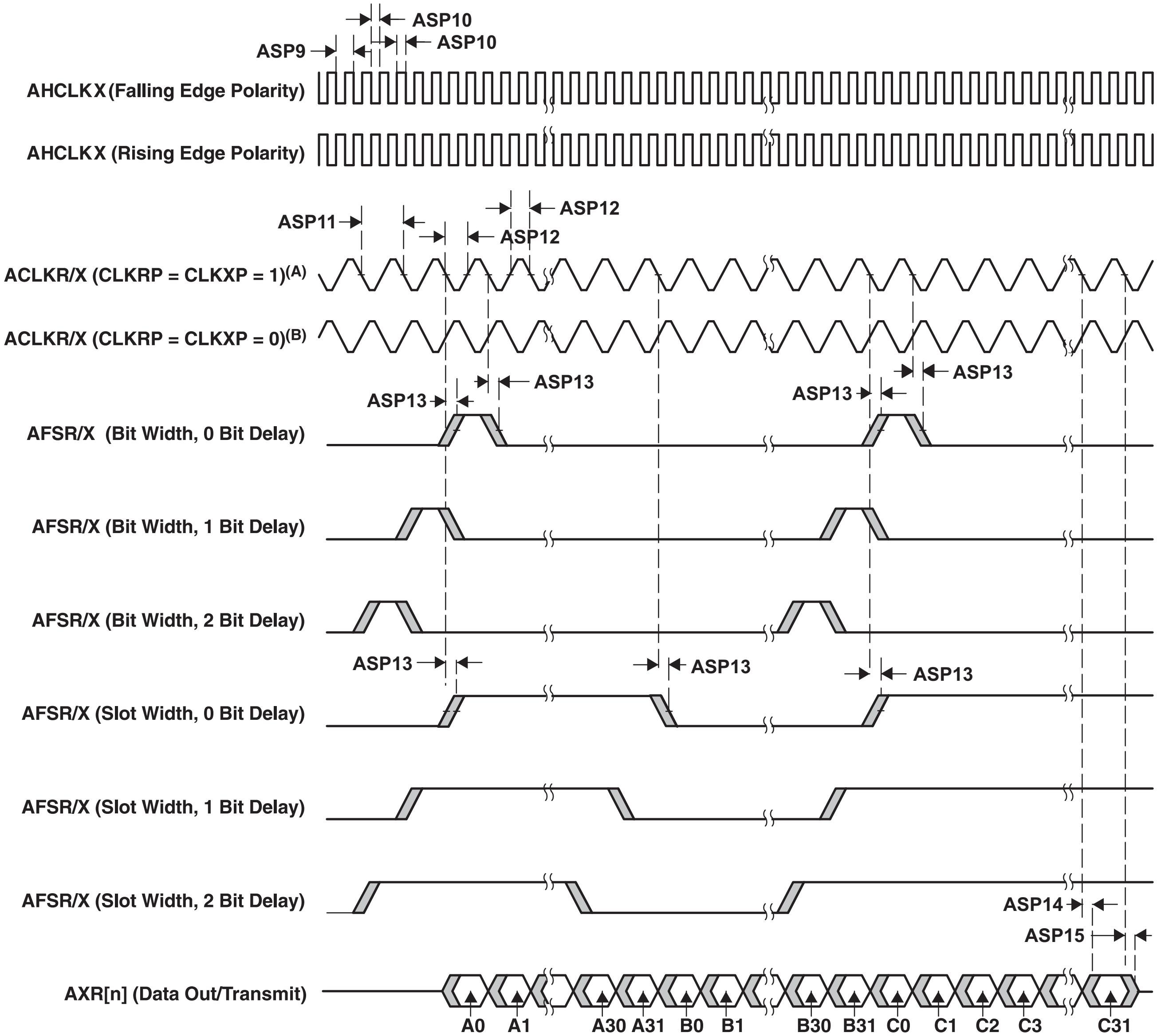
Table 5-79. Switching Characteristics Over Recommended Operating Conditions for McASP3/4/5/6/7/8 [(1)] (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
ASP14	$t_{d(ACLK-AXR)}$	Delay time, ACLKR/X transmit edge to AXR output valid	ACLKR/X int	-1.68	6.97	ns
			ACLKR/X ext in ACLKR/X ext out	1.07	25.9	ns

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = AHCLKX period in ns.

(3) R = ACLKR/X period in ns.



A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 5-56. McASP Output Timing

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in Table 4-29 and described in chapter Control Module of the Device TRM.

Table 5-80 through Table 5-87 explain all cases with Virtual Mode Details for McASP1/2/3/4/5/6/7/8 (see Figure 5-57 through Figure 5-64).

Table 5-80. Virtual Mode Case Details for McASP1

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-57
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL3_ASYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-58
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL3_ASYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL3_ASYNC_RX	See Figure 5-59
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL1_ASYNC_TX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL3_ASYNC_RX	See Figure 5-60
			AXR(Inputs)/CLKR/FSR	MCASP1_VIRTUAL1_ASYNC_TX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-61
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL2_SYNC_RX	See Figure 5-62
			AXR(Inputs)/CLKX/FSX	MCASP1_VIRTUAL2_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP1_VIRTUAL2_SYNC_RX	See Figure 5-63
			AXR(Inputs)/CLKX/FSX	MCASP1_VIRTUAL2_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-64
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 5-81. Virtual Mode Case Details for McASP2

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)(1)	See Figure 5-57
			AXR(Inputs)/CLKR/FSR	Default (No Virtual Mode)(1)	
			AXR(Inputs)/CLKR/FSR	MCASP2_VIRTUAL1_ASYNC_RX_80M(2)	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-58
			AXR(Inputs)/CLKR/FSR	MCASP2_VIRTUAL2_ASYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL2_ASYNC_RX	See Figure 5-59
			AXR(Inputs)/CLKR/FSR	MCASP2_VIRTUAL3_ASYNC_TX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL2_ASYNC_RX	See Figure 5-60
			AXR(Inputs)/CLKR/FSR	MCASP2_VIRTUAL3_ASYNC_TX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-61
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL4_SYNC_RX	See Figure 5-62
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL4_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP2_VIRTUAL4_SYNC_RX(1)	See Figure 5-63
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL4_SYNC_RX(1)	
			AXR(Inputs)/CLKX/FSX	MCASP2_VIRTUAL5_SYNC_RX_80M(2)	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-64
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

(1) Used up to 50 MHz. Should also be used in a CI-FI- mixed case where AXR operate as both inputs and outputs (that is, AXR are bidirectional).

(2) Used in 80 MHz input only mode when AXR, CLKX and FSX are all inputs.

Table 5-82. Virtual Mode Case Details for McASP3

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-57
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-58
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 5-59
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 5-60
			AXR(Inputs)/CLKR/FSR	MCASP3_VIRTUAL2_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-61
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 5-62
			AXR(Inputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	See Figure 5-63
			AXR(Inputs)/CLKX/FSX	MCASP3_VIRTUAL2_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-64
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 5-83. Virtual Mode Case Details for McASP4

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-57
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-58
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 5-59
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 5-60
			AXR(Inputs)/CLKR/FSR	MCASP4_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-61
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 5-62
			AXR(Inputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	See Figure 5-63
			AXR(Inputs)/CLKX/FSX	MCASP4_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-64
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 5-84. Virtual Mode Case Details for McASP5

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-57
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-58
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 5-59
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 5-60
			AXR(Inputs)/CLKR/FSR	MCASP5_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-61
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 5-62
			AXR(Inputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	See Figure 5-63
			AXR(Inputs)/CLKX/FSX	MCASP5_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-64
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 5-85. Virtual Mode Case Details for McASP6

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-57
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-58
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 5-59
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 5-60
			AXR(Inputs)/CLKR/FSR	MCASP6_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-61
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 5-62
			AXR(Inputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	See Figure 5-63
			AXR(Inputs)/CLKX/FSX	MCASP6_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-64
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 5-86. Virtual Mode Case Details for McASP7

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-57
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-58
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 5-59
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 5-60
			AXR(Inputs)/CLKR/FSR	MCASP7_VIRTUAL2_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-61
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 5-62
			AXR(Inputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	See Figure 5-63
			AXR(Inputs)/CLKX/FSX	MCASP7_VIRTUAL2_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-64
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

Table 5-87. Virtual Mode Case Details for McASP8

No.	CASE	CASE Description	Virtual Mode Settings		Notes
			Signals	Virtual Mode Value	
IP Mode : ASYNC					
1	COIFOI	CLKX / FSX: Output CLKR / FSR: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-57
			AXR(Inputs)/CLKR/FSR	MCASP8_VIRTUAL1_SYNC_RX	
2	COIFIO	CLKX / FSR: Output CLKR / FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-58
			AXR(Inputs)/CLKR/FSR	MCASP8_VIRTUAL1_SYNC_RX	
3	CIOFIO	CLKR / FSR: Output CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	See Figure 5-59
			AXR(Inputs)/CLKR/FSR	MCASP8_VIRTUAL1_SYNC_RX	
4	CIOFOI	CLKR / FSX: Output CLKX / FSR: Input	AXR(Outputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	See Figure 5-60
			AXR(Inputs)/CLKR/FSR	MCASP8_VIRTUAL1_SYNC_RX	
IP Mode : SYNC (CLKR / FSR internally generated from CLKX / FSX)					
5	CO-FO-	CLKX / FSX: Output	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-61
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	
6	CI-FO-	FSX: Output CLKX: Input	AXR(Outputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	See Figure 5-62
			AXR(Inputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	
7	CI-FI-	CLKX / FSX: Input	AXR(Outputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	See Figure 5-63
			AXR(Inputs)/CLKX/FSX	MCASP8_VIRTUAL1_SYNC_RX	
8	CO-FI-	CLKX: Output FSX: Input	AXR(Outputs)/CLKX/FSX	Default (No Virtual Mode)	See Figure 5-64
			AXR(Inputs)/CLKX/FSX	Default (No Virtual Mode)	

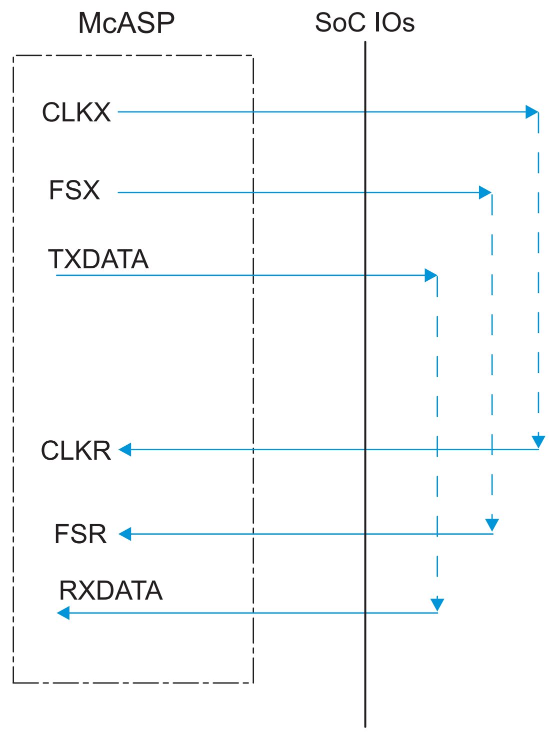


Figure 5-57. McASP1-8 COIFOI – ASYNC Mode

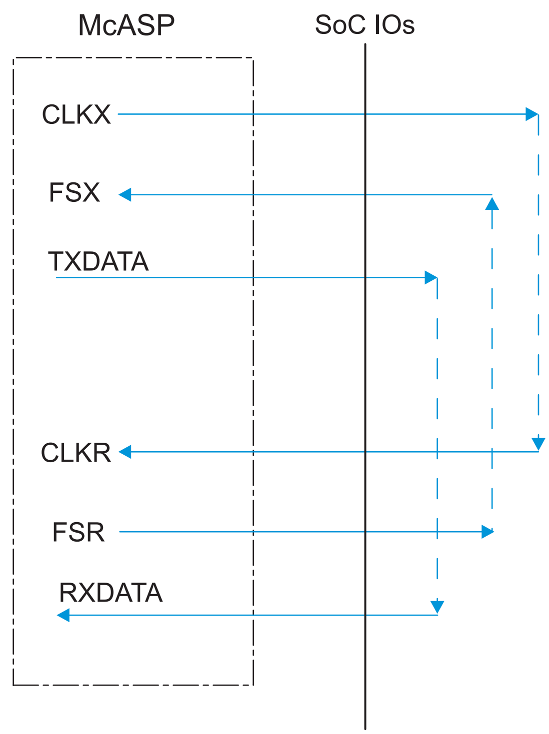


Figure 5-58. McASP1-8 COIFIO – ASYNC Mode

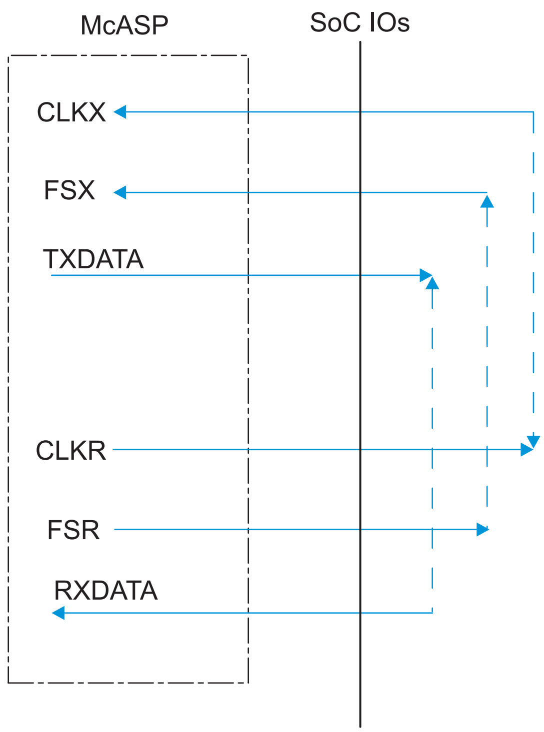


Figure 5-59. McASP1-8 CIOFIO – ASYNC Mode

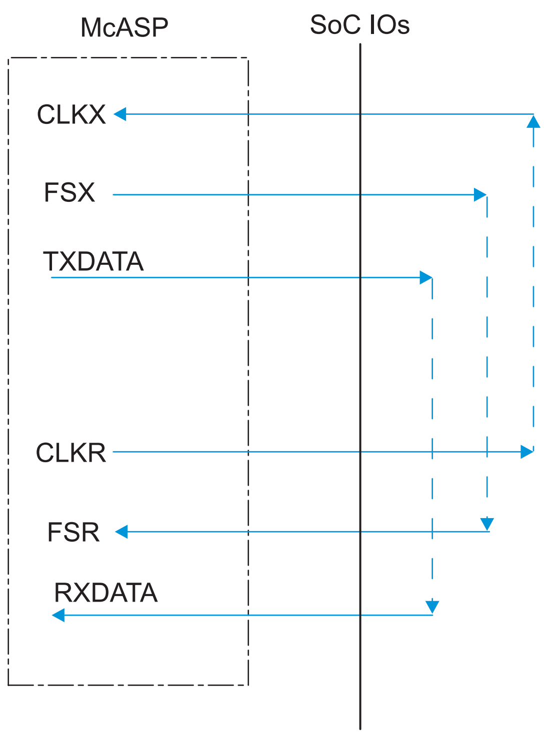


Figure 5-60. McASP1-8 CIOFOI – ASYNC Mode

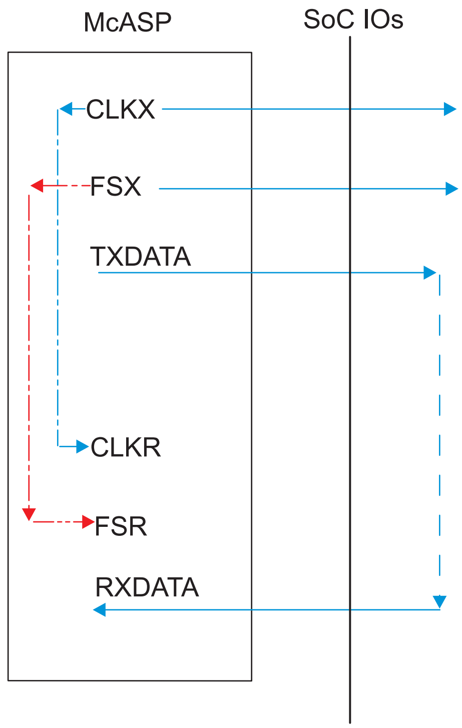


Figure 5-61. McASP1-8 CO-FO- – SYNC Mode

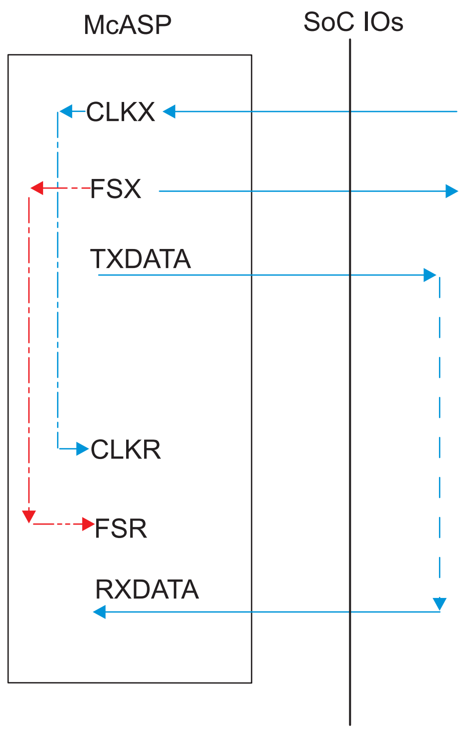


Figure 5-62. McASP1-8 CI-FO- – SYNC Mode

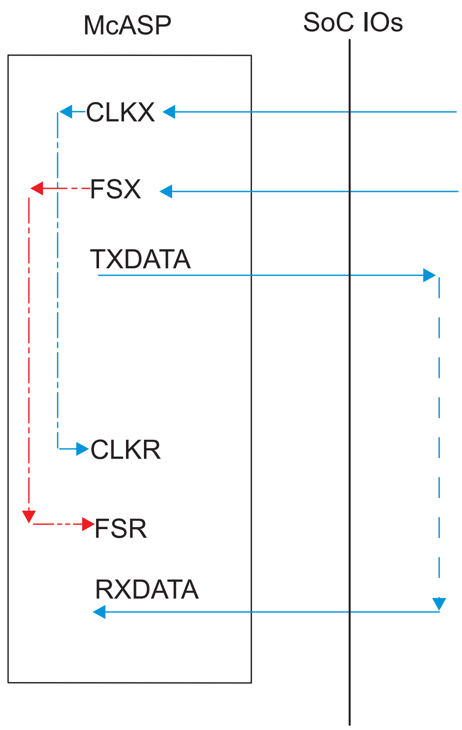


Figure 5-63. McASP1-8 CI-FI- – SYNC Mode

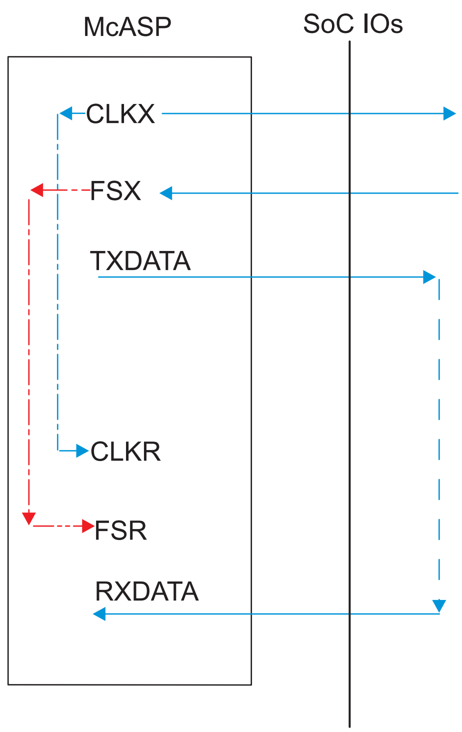


Figure 5-64. McASP1-8 CO-FI- – SYNC Mode

Virtual IO Timings Modes must be used to guarantee some IO timings for McASP1. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 5-88, *Virtual Functions Mapping for McASP1* for a definition of the Virtual modes.

Table 5-88 presents the values for DELAYMODE bitfield.

Table 5-88. Virtual Functions Mapping for McASP1

BALL	BALL NAME	Delay Mode Value			MUXMODE[15:0]		
		MCASP1_VIRTUAL1_ASYNC_TX	MCASP1_VIRTUAL2_SYNC_RX	MCASP1_VIRTUAL3_ASYNC_RX	0	1	2
E21	gpio6_14	11	15	14		mcasp1_axr8	
F20	gpio6_15	11	15	14		mcasp1_axr9	
F21	gpio6_16	11	15	14		mcasp1_axr10	
D18	xref_clk0	0	15	14			mcasp1_axr4
E17	xref_clk1	0	15	14			mcasp1_axr5
B26	xref_clk2	5	15	14			mcasp1_axr6
C23	xref_clk3	5	15	14			mcasp1_axr7
C14	mcasp1_aclkx	8	15	14	mcasp1_aclkx		
D14	mcasp1_fsx	12	15	14	mcasp1_fsx		
B14	mcasp1_aclkr	11	N/A	15	mcasp1_aclkr		
J14	mcasp1_fsr	11	N/A	15	mcasp1_fsr		
G12	mcasp1_axr0	8	15	14	mcasp1_axr0		
F12	mcasp1_axr1	8	15	14	mcasp1_axr1		
G13	mcasp1_axr2	10	15	14	mcasp1_axr2		
J11	mcasp1_axr3	10	15	14	mcasp1_axr3		
E12	mcasp1_axr4	10	15	14	mcasp1_axr4		
F13	mcasp1_axr5	10	15	14	mcasp1_axr5		
C12	mcasp1_axr6	10	15	14	mcasp1_axr6		
D12	mcasp1_axr7	10	15	14	mcasp1_axr7		
B12	mcasp1_axr8	6	15	14	mcasp1_axr8		
A11	mcasp1_axr9	6	15	14	mcasp1_axr9		
B13	mcasp1_axr10	6	15	14	mcasp1_axr10		
A12	mcasp1_axr11	6	15	14	mcasp1_axr11		
E14	mcasp1_axr12	6	15	14	mcasp1_axr12		
A13	mcasp1_axr13	6	15	14	mcasp1_axr13		
G14	mcasp1_axr14	6	15	14	mcasp1_axr14		
F14	mcasp1_axr15	6	15	14	mcasp1_axr15		

1. NA in this table stands for Not Applicable.

Virtual IO Timings Modes must be used to guarantee some IO timings for McASP2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 5-89, *Virtual Functions Mapping for McASP2* for a definition of the Virtual modes.

Table 5-89 presents the values for DELAYMODE bitfield.

Table 5-89. Virtual Functions Mapping for McASP2

BALL	BALL NAME	Delay Mode Value					MUXMODE[15:0]		
		MCASP2_VIRTUAL1_ASYNC_RX_80M	MCASP2_VIRTUAL2_ASYNC_RX	MCASP2_VIRTUAL3_ASYNC_TX	MCASP2_VIRTUAL4_SYNC_RX	MCASP2_VIRTUAL5_SYNC_RX_80M	0	1	2
D18	xref_clk0	10	9	4	8	6		mcasp2_axr8	
E17	xref_clk1	10	9	4	8	6		mcasp2_axr9	
B26	xref_clk2	13	12	0	11	10		mcasp2_axr10	
C23	xref_clk3	13	12	0	11	10		mcasp2_axr11	
A19	mcasp2_aclkx	15	14	5	10	9	mcasp2_aclkx		
A18	mcasp2_fsx	15	14	5	10	9	mcasp2_fsx		
E15	mcasp2_aclkr	15	14	10	N/A	N/A	mcasp2_aclkr		
A20	mcasp2_fsr	15	14	10	N/A	N/A	mcasp2_fsr		
B15	mcasp2_axr0	15	14	9	13	12	mcasp2_axr0		
A15	mcasp2_axr1	15	14	9	13	12	mcasp2_axr1		
C15	mcasp2_axr2	15	14	4	10	9	mcasp2_axr2		
A16	mcasp2_axr3	15	14	4	10	9	mcasp2_axr3		
D15	mcasp2_axr4	15	14	7	13	12	mcasp2_axr4		
B16	mcasp2_axr5	15	14	7	13	12	mcasp2_axr5		
B17	mcasp2_axr6	15	14	7	13	12	mcasp2_axr6		
A17	mcasp2_axr7	15	14	7	13	12	mcasp2_axr7		
B18	mcasp3_aclkx	15	14	5	10	9			mcasp2_axr12
F15	mcasp3_fsx	15	14	4	10	9			mcasp2_axr13
B19	mcasp3_axr0	15	14	4	10	9			mcasp2_axr14
C17	mcasp3_axr1	15	14	3	10	8			mcasp2_axr15

1. NA in this table stands for Not Applicable.

Virtual IO Timings Modes must be used to guarantee some IO timings for McASP3/4/5/6/7/8. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 5-90, *Virtual Functions Mapping for McASP3/4/5/6/7/8* for a definition of the Virtual modes.

Table 5-90 presents the values for DELAYMODE bitfield.

Table 5-90. Virtual Functions Mapping for McASP3/4/5/6/7/8

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]		
			0	1	2
MCASP3_VIRTUAL2_SYNC_RX					
C15	mcasp2_axr2	8		mcasp3_axr2	
A16	mcasp2_axr3	8		mcasp3_axr3	
B18	mcasp3_aclkx	8	mcasp3_aclkx	mcasp3_aclkr	
F15	mcasp3_fsx	8	mcasp3_fsx	mcasp3_fsr	
B19	mcasp3_axr0	8	mcasp3_axr0		
C17	mcasp3_axr1	6	mcasp3_axr1		
MCASP4_VIRTUAL1_SYNC_RX					
E12	mcasp1_axr4	13		mcasp4_axr2	
F13	mcasp1_axr5	13		mcasp4_axr3	
C18	mcasp4_aclkx	15	mcasp4_aclkx	mcasp4_aclkr	
A21	mcasp4_fsx	15	mcasp4_fsx	mcasp4_fsr	
G16	mcasp4_axr0	15	mcasp4_axr0		
D17	mcasp4_axr1	15	mcasp4_axr1		
MCASP5_VIRTUAL1_SYNC_RX					
C12	mcasp1_axr6	13		mcasp5_axr2	
D12	mcasp1_axr7	13		mcasp5_axr3	
AA3	mcasp5_aclkx	15	mcasp5_aclkx	mcasp5_aclkr	
AB9	mcasp5_fsx	15	mcasp5_fsx	mcasp5_fsr	
AB3	mcasp5_axr0	15	mcasp5_axr0		
AA4	mcasp5_axr1	15	mcasp5_axr1		
MCASP6_VIRTUAL1_SYNC_RX					
G13	mcasp1_axr2	13		mcasp6_axr2	
J11	mcasp1_axr3	13		mcasp6_axr3	
B12	mcasp1_axr8	10		mcasp6_axr0	
A11	mcasp1_axr9	10		mcasp6_axr1	
B13	mcasp1_axr10	10		mcasp6_aclkx	mcasp6_aclkr
A12	mcasp1_axr11	10		mcasp6_fsx	mcasp6_fsr
MCASP7_VIRTUAL2_SYNC_RX					
B14	mcasp1_aclkr	14		mcasp7_axr2	
J14	mcasp1_fsr	14		mcasp7_axr3	
E14	mcasp1_axr12	10		mcasp7_axr0	

Table 5-90. Virtual Functions Mapping for McASP3/4/5/6/7/8 (continued)

BALL	BALL NAME	Delay Mode Value	MUXMODE[15:0]		
			0	1	2
A13	mcasp1_axr13	10		mcasp7_axr1	
G14	mcasp1_axr14	10		mcasp7_aclkx	mcasp7_aclkr
F14	mcasp1_axr15	10		mcasp7_fsx	mcasp7_fsr
MCASP8_VIRTUAL1_SYNC_RX					
E15	mcasp2_aclkr	13		mcasp8_axr2	
A20	mcasp2_fsr	13		mcasp8_axr3	
D15	mcasp2_axr4	11		mcasp8_axr0	
B16	mcasp2_axr5	11		mcasp8_axr1	
B17	mcasp2_axr6	11		mcasp8_aclkx	mcasp8_aclkr
A17	mcasp2_axr7	11		mcasp8_fsx	mcasp8_fsr

5.10.6.14 USB

SuperSpeed USB DRD Subsystem has four instances in the device providing the following functions:

- USB1: SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with integrated SS (USB3.0) PHY and HS/FS (USB2.0) PHY.
- USB2: High-Speed (HS) USB 2.0 Dual-Role-Device (DRD) subsystem with integrated HS/FS PHY.
- USB3: HS USB 2.0 Dual-Role-Device (DRD) subsystem with ULPI (SDR) interface to external HS/FS PHYs.
- USB4: HS USB 2.0 Dual-Role-Device (DRD) subsystem with ULPI (SDR) interface to external HS/FS PHYs.

NOTE

For more information, see the SuperSpeed USB DRD section of the Device TRM.

5.10.6.14.1 USB1 DRD PHY

The USB1 DRD interface supports the following applications:

- USB2.0 High-Speed PHY port (1.8 V and 3.3 V): this asynchronous high-speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps.
- USB3.0 Super-Speed PHY port (1.8 V): this asynchronous differential super-speed interface is compliant with the USB3.0 RX/TX PHY standard (USB3.0 standard v1.0) for a maximum data bit rate of 5Gbps.

5.10.6.14.2 USB2 PHY

The USB2 interface supports the following applications:

- USB2.0 High-Speed PHY port (1.8 V and 3.3 V): this asynchronous high-speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps.

5.10.6.14.3 USB3 and USB4 DRD ULPI—SDR—Slave Mode—12-pin Mode

TheUSB3 and USB4 DRD interfaces support the following application:

- USB ULPI port: this synchronous interface is compliant with the USB2.0 ULPI SDR standard (UTMI+ v1.22), for alternative off-chip USB2.0 PHY interface; that is, with external transceiver with a maximum frequency of 60 MHz (synchronous slave mode, SDR, 12-pin, 8-data-bit).

NOTE

The Universal Serial Bus k ULPI modules are also refered as USBk where k = 3, 4.

Table 5-91, Table 5-92 and Figure 5-65 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-91. Timing Requirements for ULPI SDR Slave Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
US1	$t_{c(clk)}$	Cycle time, usb_ulpi_clk period	16.66		ns
US5	$t_{su(ctrlV-clkH)}$	Setup time, usb_ulpi_dir/usb_ulpi_nxt valid before usb_ulpi_clk rising edge	6.73		ns
US6	$t_{h(clkH-ctrlV)}$	Hold time, usb_ulpi_dir/usb_ulpi_nxt valid after usb_ulpi_clk rising edge	-0.41		ns

Table 5-91. Timing Requirements for ULPI SDR Slave Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
US7	$t_{su(dV-clkH)}$	Setup time, usb_ulpi_d[7:0] valid before usb_ulpi_clk rising edge	6.73		ns
US8	$t_{h(clkH-dV)}$	Hold time, usb_ulpi_d[7:0] valid after usb_ulpi_clk rising edge	-0.41		ns

Table 5-92. Switching Characteristics for ULPI SDR Slave Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
US4	$t_{d(clkH-stpV)}$	Delay time, usb_ulpi_clk rising edge high to output usb_ulpi_stp valid	0.44	8.35	ns
US9	$t_{d(clkL-doV)}$	Delay time, usb_ulpi_clk rising edge high to output usb_ulpi_d[7:0] valid	0.44	8.35	ns

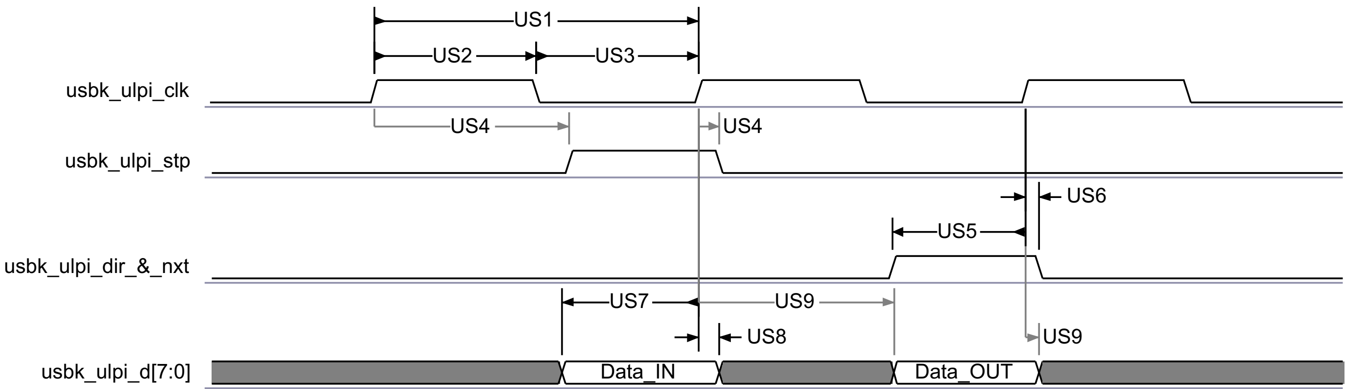


Figure 5-65. HS USB3 and USB4 ULPI —SDR—Slave Mode—12-pin Mode

In Table 5-93 are presented the specific groupings of signals (IOSET) for use with USB3 and USB4 signals.

Table 5-93. USB3 and USB4 IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
USB3				
usb3_ulpi_d0	AE1	2	AC3	3
usb3_ulpi_d1	AE5	2	AC9	3
usb3_ulpi_d2	AE3	2	AC6	3
usb3_ulpi_d3	AF1	2	AC7	3
usb3_ulpi_d4	AF4	2	AC4	3
usb3_ulpi_d5	AF3	2	AD4	3
usb3_ulpi_d6	AF6	2	AB4	3
usb3_ulpi_d7	AF2	2	AC5	3
usb3_ulpi_nxt	AE2	2	AC8	3
usb3_ulpi_dir	AE6	2	AD6	3
usb3_ulpi_stp	AD2	2	AB8	3
usb3_ulpi_clk	AD3	2	AB5	3
USB4				
usb4_ulpi_d0			V6	6
usb4_ulpi_d1			U6	6
usb4_ulpi_d2			U5	6
usb4_ulpi_d3			V5	6

Table 5-93. USB3 and USB4 IOSETs (continued)

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
usb4_ulpi_d4			V4	6
usb4_ulpi_d5			V3	6
usb4_ulpi_d6			Y2	6
usb4_ulpi_d7			W2	6
usb4_ulpi_stp			V9	6
usb4_ulpi_clk			W9	6
usb4_ulpi_dir			V7	6
usb4_ulpi_nxt			U7	6

5.10.6.15 SATA

The SATA RX/TX PHY interface is compliant with the SATA standard v2.6 for a maximum data rate:

- Gen2i, Gen2m, Gen2x: 3Gbps.
- Gen1i, Gen1m, Gen1x: 1.5Gbps.

NOTE

For more information, see the SATA Controller section of the Device TRM.

5.10.6.16 PCIe

The device supports connections to PCIe-compliant devices via the integrated PCIe master/slave bus interface. The PCIe module is comprised of a dual-mode PCIe core and a SerDes PHY. Each PCIe subsystem controller has support for PCIe Gen-II mode (5.0 Gbps /lane) and Gen-I mode (2.5 Gbps/lane) (Single Lane and Flexible dual lane configuration).

The device PCIe supports the following features:

- 16-bit operation @250 MHz on PIPE interface (per 16-bit lane)
- Supports 1 ports x 1 lane configuration
- Single virtual channel (VC0), single traffic class (TC0)
- Single function in end-point mode
- Automatic width and speed negotiation
- Max payload: 128 byte outbound, 256 byte inbound
- Automatic credit management
- ECRC generation and checking
- Configurable BAR filtering
- Legacy interrupt reception (RC) and generation (EP)
- MSI generation and reception
- PCI Express Active State Power Management (ASPM) state L0s and L1 (with exceptions)
- All PCI Device Power Management D-states with the exception of $D3_{cold}$ / L2 state

The PCIe controller on this device conforms to the PCI Express Base 3.0 Specification, revision 1.0 and the PCI Local Bus Specification, revision 3.0.

NOTE

For more information, see the PCIe Controller section of the Device TRM.

5.10.6.17 CAN

5.10.6.17.1 DCAN

The device provides two DCAN interfaces for supporting distributed realtime control with a high level of security.

The DCAN interface implements the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM single error correction and double error detection (SECDED) mechanism
- Direct access to Message RAM during test mode
- Support for two interrupt lines: Level 0 and Level 1, plus separate ECC interrupt line
- Local power down and wakeup support
- Automatic message RAM initialization
- Support for DMA access

5.10.6.17.2 MCAN-FD

The device supports one MCAN module connecting to the CAN network through external (for the device) transceiver for connection to the physical layer. The MCAN module supports up to 5 Mbit/s data rate and is compliant to ISO 11898-1:2015.

The MCAN-FD module implements the following features:

- Conforms with ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Internal Loopback mode for self-test
- Maskable interrupts, two interrupt lines
- Two clock domains (CAN clock/Host clock)
- Parity/ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Local power-down and wakeup support
- Timestamp Counter

NOTE

For more information, see the Serial Communication Interfaces / DCAN and MCAN sections of the Device TRM.

NOTE

The Controller Area Network Interface x (x = 1 to 2) is also referred to as CANx.

NOTE

Refer to the CAN Specification for calculations necessary to validate timing compliance. Jitter tolerance calculations must be performed to validate the implementation.

Table 5-94 and Table 5-95 present timing and switching characteristics for CANx Interface.

Table 5-94. Timing Requirements for CANx Receive

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
-	f(baud)	Maximum programmable baud rate		1	Mbps
-	$t_{d(CANnRX)}$	Delay time, CANnRX pin to receive shift register		12	ns

Table 5-95. Switching Characteristics Over Recommended Operating Conditions for CANx Transmit

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
-	f(baud)	Maximum programmable baud rate		1	Mbps
-	$t_{d(CANnTX)}$	Delay time, Transmit shift register to CANnTX pin[(1)]		12	ns

(1) These values do not include rise/fall times of the output buffer.

5.10.6.18 GMAC_SW

The three-port gigabit ethernet switch subsystem (GMAC_SW) provides ethernet packet communication and can be configured as an ethernet switch. It provides the Gigabit Media Independent Interface (G/MII) in MII mode, Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) for physical layer device (PHY) management.

NOTE

For more information, see the Ethernet Subsystem section of the Device TRM.

NOTE

The Gigabit, Reduced and Media Independent Interface n (n = 0 to 1) are also referred to as MIIn, RMIIn and RGMIIn

CAUTION

The IO timings provided in this section are only valid if signals within a single IOSET are used. The IOSETs are defined in the Table 5-100, Table 5-103, Table 5-108, and Table 5-115.

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-96 and Figure 5-66 present timing requirements for MIIn in receive operation.

5.10.6.18.1 GMAC MII Timings

Table 5-96. Timing Requirements for miin_rxclk - MII Operation

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
MII1	$t_{c(RX\_CLK)}$	Cycle time, miin_rxclk	10 Mbps	400		ns
			100 Mbps	40		ns
MII2	$t_{w(RX\_CLKH)}$	Pulse duration, miin_rxclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
MII3	$t_{w(RX\_CLKL)}$	Pulse duration, miin_rxclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
MII4	$t_{t(RX\_CLK)}$	Transition time, miin_rxclk	10 Mbps		3	ns
			100 Mbps		3	ns

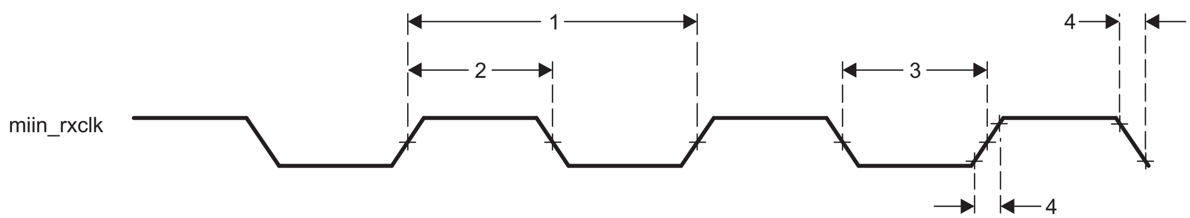


Figure 5-66. Clock Timing (GMAC Receive) - MIIn Operation

Table 5-97 and Figure 5-67 present timing requirements for MIIn in transmit operation.

Table 5-97. Timing Requirements for miin_txclk - MII Operation

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
MII1	$t_{c(TX\_CLK)}$	Cycle time, miin_txclk	10 Mbps	400		ns
			100 Mbps	40		ns
MII2	$t_{w(TX\_CLKH)}$	Pulse duration, miin_txclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
MII3	$t_{w(TX\_CLKL)}$	Pulse duration, miin_txclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
MII4	$t_{t(TX\_CLK)}$	Transition time, miin_txclk	10 Mbps		3	ns
			100 Mbps		3	ns

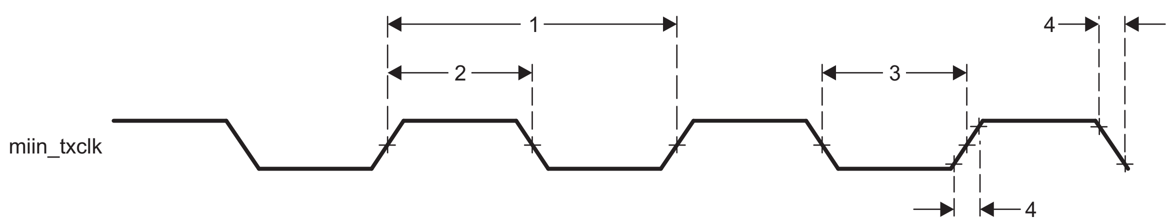


Figure 5-67. Clock Timing (GMAC Transmit) - MIIn Operation

Table 5-98 and Figure 5-68 present timing requirements for GMAC MIIn Receive 10/100Mbit/s.

Table 5-98. Timing Requirements for GMAC MIIn Receive 10/100 Mbit/s

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MII1	$t_{su(RXD-RX\_CLK)}$	Setup time, receive selected signals valid before miin_rxclk	8		ns
	$t_{su(RX\_DV-RX\_CLK)}$				
	$t_{su(RX\_ER-RX\_CLK)}$				
MII2	$t_{h(RX\_CLK-RXD)}$	Hold time, receive selected signals valid after miin_rxclk	8		ns
	$t_{h(RX\_CLK-RX\_DV)}$				
	$t_{h(RX\_CLK-RX\_ER)}$				

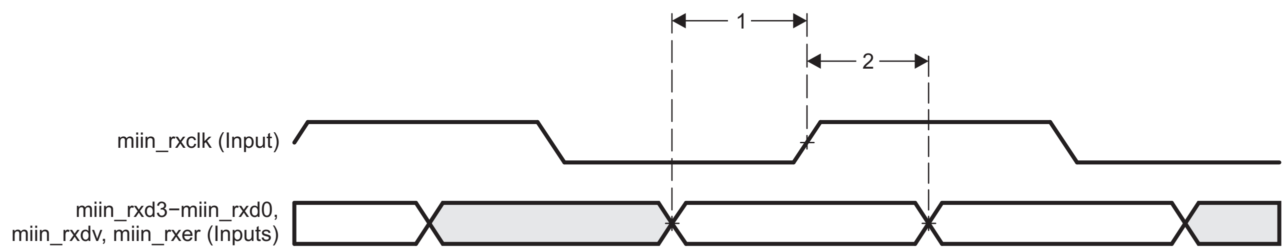


Figure 5-68. GMAC Receive Interface Timing MIIn Operation

Table 5-99 and Figure 5-69 present timing requirements for GMAC MIIn Transmit 10/100Mbit/s.

Table 5-99. Switching Characteristics Over Recommended Operating Conditions for GMAC MIIn Transmit 10/100 Mbits/s

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MII1	$t_{d(TX\_CLK-TXD)}$	Delay time, miin_txclk to transmit selected signals valid	0	25	ns
	$t_{d(TX\_CLK-TX\_EN)}$				

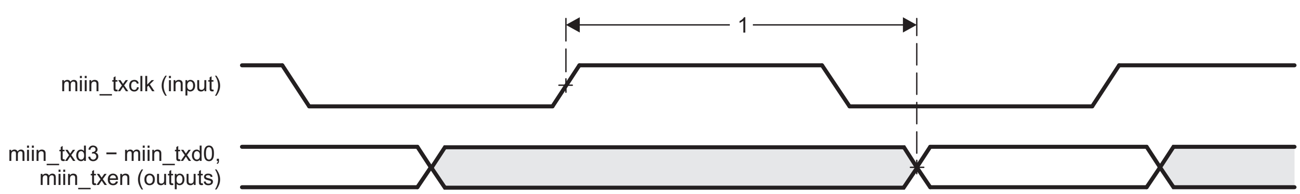


Figure 5-69. GMAC Transmit Interface Timing MIIn Operation

In Table 5-100 are presented the specific groupings of signals (IOSET) for use with GMAC MII signals.

Table 5-100. GMAC MII IOSETs

SIGNALS	IOSET5		IOSET6	
	BALL	MUX	BALL	MUX
GMAC MII1				
mii1_txd3	C5	8		
mii1_txd2	D6	8		
mii1_txd1	B2	8		
mii1_txd0	C4	8		
mii1_rxd3	F5	8		
mii1_rxd2	E4	8		
mii1_rxd1	C1	8		
mii1_rxd0	E6	8		

Table 5-100. GMAC MII IOSETs (continued)

SIGNALS	IOSET5		IOSET6	
	BALL	MUX	BALL	MUX
mii1_col	B4	8		
mii1_rxer	B3	8		
mii1_txer	A3	8		
mii1_txen	A4	8		
mii1_crs	B5	8		
mii1_rxclk	D5	8		
mii1_txclk	C3	8		
mii1_rxdv	C2	8		
GMAC MII0				
mii0_txd3			V5	3
mii0_txd2			V4	3
mii0_txd1			Y2	3
mii0_txd0			W2	3
mii0_rxd3			W9	3
mii0_rxd2			V9	3
mii0_rxd1			V6	3
mii0_rxd0			U6	3
mii0_txclk			U5	3
mii0_txer			U4	3
mii0_rxer			U7	3
mii0_rxdv			V2	3
mii0_crs			V7	3
mii0_col			V1	3
mii0_rxclk			Y1	3
mii0_txen			V3	3

5.10.6.18.2 GMAC MDIO Interface Timings

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-101, Table 5-101 and Figure 5-70 present timing requirements for MDIO.

Table 5-101. Timing Requirements for MDIO Input

No	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{c(MDC)}$	Cycle time, MDC	400		ns
MDIO2	$t_{w(MDCH)}$	Pulse Duration, MDC High	160		ns
MDIO3	$t_{w(MDCL)}$	Pulse Duration, MDC Low	160		ns
MDIO4	$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC High	90		ns
MDIO5	$t_{h(MDIO\_MDC)}$	Hold time, MDIO valid from MDC High	0		ns

Table 5-102. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

NO	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO6	$t_{t(MDC)}$	Transition time, MDC		5	ns
MDIO7	$t_{d(MDC-MDIO)}$	Delay time, MDC High to MDIO valid	10	390	ns

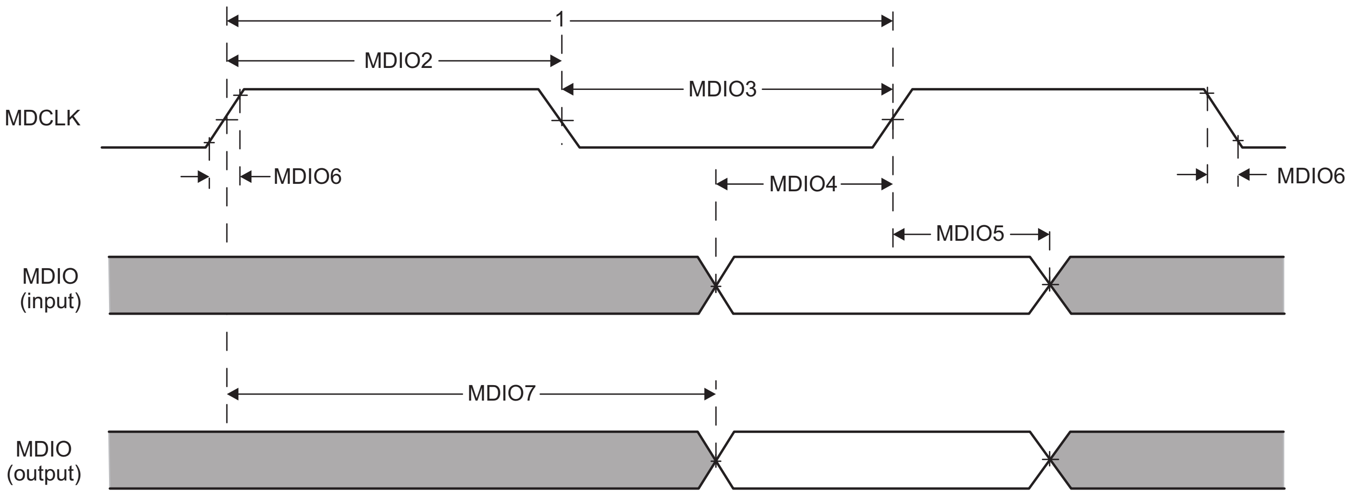


Figure 5-70. GMAC MDIO Diagrams

In Table 5-103 are presented the specific groupings of signals (IOSET) for use with GMAC MDIO signals.

Table 5-103. GMAC MDIO IOSETs

SIGNALS	IOSET7		IOSET8		IOSET9		IOSET10	
	BALL	MUX	BALL	MUX	BALL	MUX	BALL	MUX
mdio_d	F6	3	U4	0	AB4	1	B20	5
mdio_mclk	D3	3	V1	0	AC5	1	B21	5

5.10.6.18.3 GMAC RMII Timings

The main reference clock REF_CLK (RMII_50MHZ_CLK) of RMII interface is internally supplied from PRCM. The source of this clock could be either externally sourced from the RMII_MHZ_50_CLK pin of the device or internally generated from DPLL_GMAC output clock GMAC_RMII_HS_CLK. Please see the PRCM chapter of the Device TRM for full details about RMII reference clock.

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-104, Table 5-105 and Figure 5-71 present timing requirements for GMAC RMIIn Receive.

Table 5-104. Timing Requirements for GMAC REF_CLK - RMII Operation

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	20		ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII4	$t_{tt(REF\_CLK)}$	Transistion time, REF_CLK		3	ns

Table 5-105. Timing Requirements for GMAC RMIIn Receive

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII5	$t_{su(RXD-REF\_CLK)}$	Setup time, receive selected signals valid before REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$				
	$t_{su(RX\_ER-REF\_CLK)}$				
RMII6	$t_{h(REF\_CLK-RXD)}$	Hold time, receive selected signals valid after REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$				
	$t_{h(REF\_CLK-RX\_ER)}$				

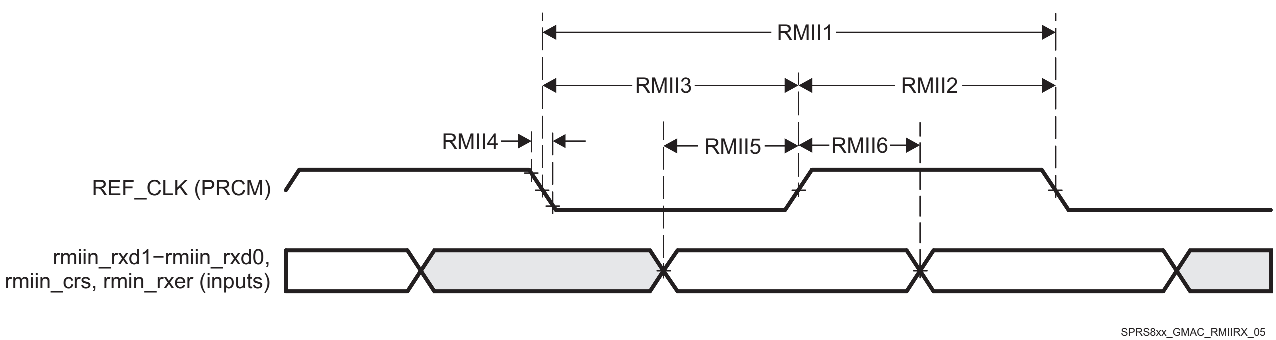


Figure 5-71. GMAC Receive Interface Timing RMIIn Operation

Table 5-106, Table 5-106 and Figure 5-72 present switching characteristics

for GMAC RMIIn Transmit 10/100Mbit/s.

Table 5-106. Switching Characteristics Over Recommended Operating Conditions for GMAC REF_CLK - RMII Operation

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII7	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	20		ns
RMII8	$t_{w(REF\_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns

Table 5-106. Switching Characteristics Over Recommended Operating Conditions for GMAC REF_CLK - RMII Operation (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII9	$t_{w(REF\_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII10	$t_{t(REF\_CLK)}$	Transistion time, REF_CLK		3	ns

Table 5-107. Switching Characteristics Over Recommended Operating Conditions for GMAC RMIIn Transmit 10/100 Mbits/s

NO.	PARAMETER	DESCRIPTION	RMIIn	MIN	MAX	UNIT
RMII11	$t_{d(REF\_CLK-TXD)}$	Delay time, REF_CLK high to selected transmit signals valid	RMII0	2	13.5	ns
	$t_{dd(REF\_CLK-TXEN)}$					
	$t_{d(REF\_CLK-TXD)}$		RMII1	2	13.8	ns
	$t_{dd(REF\_CLK-TXEN)}$					

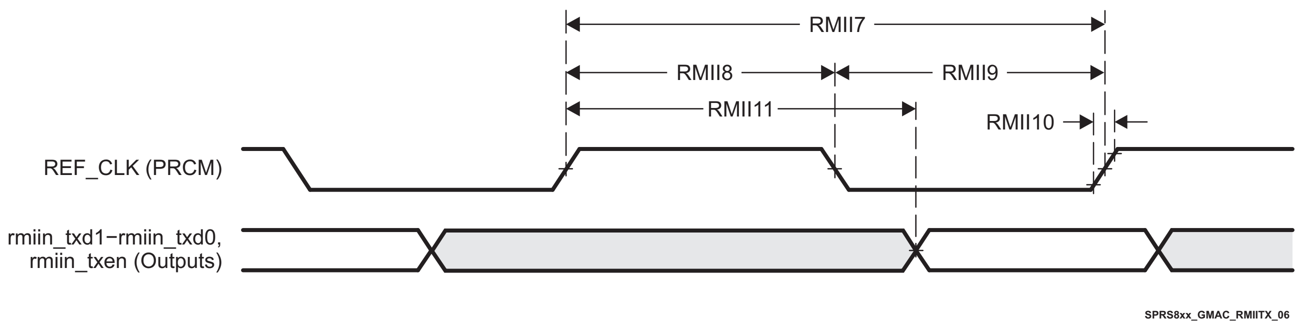


Figure 5-72. GMAC Transmit Interface Timing RMIIn Operation

In Table 5-108 are presented the specific groupings of signals (IOSET) for use with GMAC RMII signals.

Table 5-108. GMAC RMII IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
GMAC RMII1				
RMII_MHZ_50_CLK	U3	0		
rmii1_txd1	V5	2		
rmii1_txd0	V4	2		
rmii1_rxd1	W9	2		
rmii1_rxd0	V9	2		
rmii1_rxer	Y1	2		
rmii1_txen	U5	2		
rmii1_crs	V2	2		
GMAC RMII0				
RMII_MHZ_50_CLK			U3	0
rmii0_txd1			Y2	1
rmii0_txd0			W2	1
rmii0_rxd1			V6	1
rmii0_rxd0			U6	1
rmii0_txen			V3	1
rmii0_rxer			U7	1
rmii0_crs			V7	1

Manual IO Timings Modes must be used to guarantee some IO timings for GMAC. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-109, *Manual Functions Mapping for GMAC RMII0* for a definition of the Manual modes.

Table 5-109 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-109. Manual Functions Mapping for GMAC RMII0

BALL	BALL NAME	GMAC_RMII0_MANUAL1		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)		0	1
U3	RMII_MHZ_50_CLK	0	0	CFG_RMII_MHZ_50_CLK_IN	RMII_MHZ_50_CLK	
U6	rgmii0_txd0	500	500	CFG_RGMII0_TXD0_IN		rmii0_rxd0
V6	rgmii0_txd1	840	1000	CFG_RGMII0_TXD1_IN		rmii0_rxd1
U7	rgmii0_txd2	360	840	CFG_RGMII0_TXD2_IN		rmii0_rxer
V7	rgmii0_txd3	600	1000	CFG_RGMII0_TXD3_IN		rmii0_crs

Manual IO Timings Modes must be used to guarantee some IO timings for GMAC. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-110, *Manual Functions Mapping for GMAC RMII1* for a definition of the Manual modes.

Table 5-110 list the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-110. Manual Functions Mapping for GMAC RMII1

BALL	BALL NAME	GMAC_RMII1_MANUAL1		CFG REGISTER	MUXMODE	
		A_DELAY (ps)	G_DELAY (ps)		0	2
U3	RMII_MHZ_50_CLK	0	0	CFG_RMII_MHZ_50_CLK_IN	RMII_MHZ_50_CLK	
W9	rgmii0_txc	300	1200	CFG_RGMII0_TXC_IN		rmii1_rxd1
V9	rgmii0_txctl	300	1000	CFG_RGMII0_TXCTL_IN		rmii1_rxd0
V2	uart3_rxd	400	700	CFG_UART3_RXD_IN		rmii1_crs
Y1	uart3_txd	300	500	CFG_UART3_TXD_IN		rmii1_rxer

5.10.6.18.4 GMAC RGMII Timings

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 5-111, Table 5-112 and Figure 5-73 present timing requirements for receive RGMIIn operation.

Table 5-111. Timing Requirements for rgmiin_rxc - RGMIIn Operation

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, rgmiin_rxc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, rgmiin_rxc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns

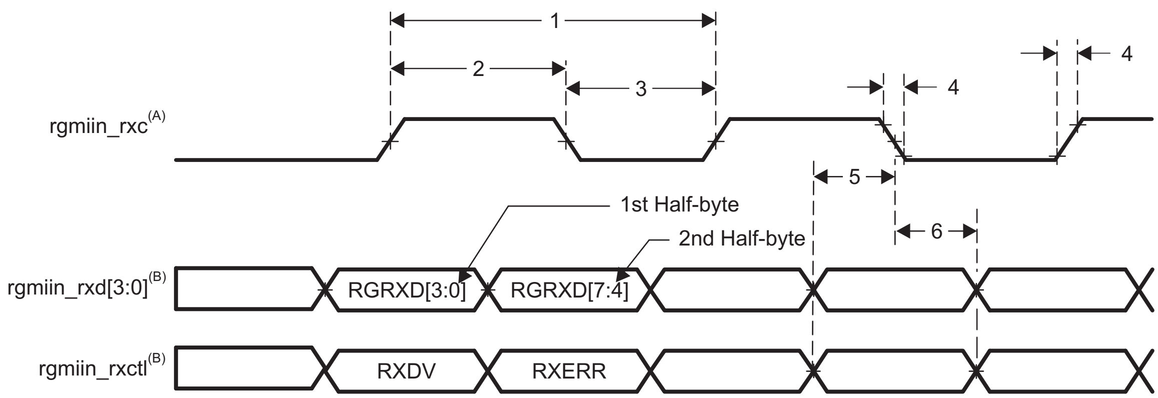
Table 5-111. Timing Requirements for rgmiin_rxc - RGMIIn Operation (continued)

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
RGMII3	$t_{w(RXCL)}$	Pulse duration, rgmiin_rxc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII4	$t_{t(RXC)}$	Transition time, rgmiin_rxc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns
			1000 Mbps		0.75	ns

Table 5-112. Timing Requirements for GMAC RGMIIn Input Receive for 10/100/1000 Mbps (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RGMII5	$t_{su(RXD-RXCH)}$	Setup time, receive selected signals valid before rgmiin_rxc high/low	1		ns
RGMII6	$t_{h(RXCH-RXD)}$	Hold time, receive selected signals valid after rgmiin_rxc high/low	1		ns

(1) For RGMII, receive selected signals include: rgmiin_rxd[3:0] and rgmiin_rxctl.



A. rgmiin_rxc must be externally delayed relative to the data and control pins.
B. Data and control information is received using both edges of the clocks. rgmiin_rxd[3:0] carries data bits 3-0 on the rising edge of rgmiin_rxc and data bits 7-4 on the falling edge ofrgmiin_rxc. Similarly, rgmiin_rxctl carries RXDV on rising edge of rgmiin_rxc and RXERR on falling edge of rgmiin_rxc.

Figure 5-73. GMAC Receive Interface Timing, RGMIIn Operation

Table 5-113, Table 5-114 and Figure 5-74 present switching characteristics for transmit - RGMIIn for 10/100/1000Mbit/s.

Table 5-113. Switching Characteristics Over Recommended Operating Conditions for rgmiin_txctl - RGMIIn Operation for 10/100/1000 Mbit/s

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
RGMII1	$t_{c(TXC)}$	Cycle time, rgmiin_txc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
RGMII2	$t_{w(TXCH)}$	Pulse duration, rgmiin_txc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII3	$t_{w(TXCL)}$	Pulse duration, rgmiin_txc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII4	$t_{t(TXC)}$	Transition time, rgmiin_txc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns
			1000 Mbps		0.75	ns

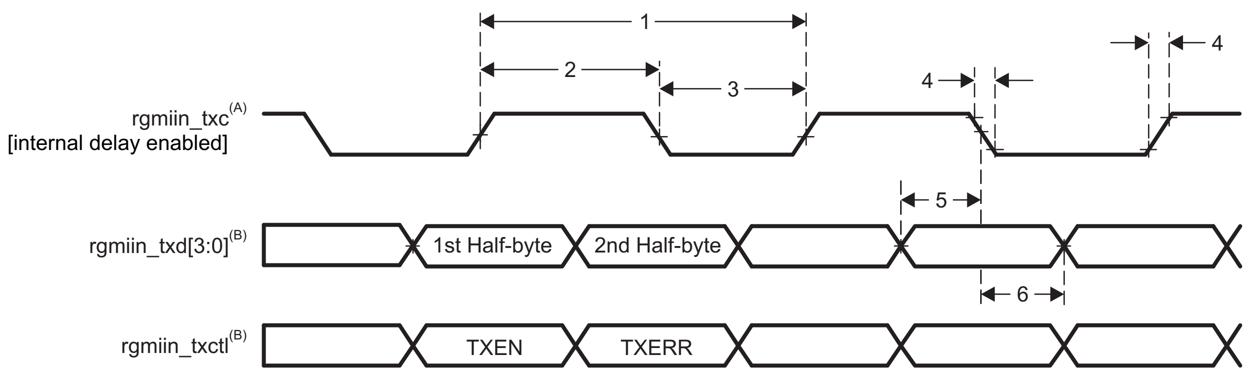
Table 5-114. Switching Characteristics for GMAC RGMIIn Output Transmit for 10/100/1000 Mbps (1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII5	$t_{osu(TXD-TXC)}$	Output Setup time, transmit selected signals valid to rgmiin_txc high/low	RGMII0, Internal Delay Enabled, 1000 Mbps	1.05 (2)		ns
			RGMII0, Internal Delay Enabled, 10/100 Mbps	1.2		ns
			RGMII1, Internal Delay Enabled, 1000 Mbps	1.05 (3)		ns
			RGMII1, Internal Delay Enabled, 10/100 Mbps	1.2		ns
RGMII6	$t_{oh(TXC-TXD)}$	Output Hold time, transmit selected signals valid after rgmiin_txc high/low	RGMII0, Internal Delay Enabled, 1000 Mbps	1.05 (2)		ns
			RGMII0, Internal Delay Enabled, 10/100 Mbps	1.2		ns
			RGMII1, Internal Delay Enabled, 1000 Mbps	1.05 (3)		ns
			RGMII1, Internal Delay Enabled, 10/100 Mbps	1.2		ns

(1) For RGMII, transmit selected signals include: rgmiin_txd[3:0] and rgmiin_txctl.

(2) RGMII0 1000Mbps operation requires that the 4 data pins rgmii0_txd[3:0] and rgmii0_txctl have their board propagation delays matched within 50pS of rgmii0_txc.

(3) RGMII1 1000Mbps operation requires that the 4 data pins rgmii1_txd[3:0] and rgmii1_txctl have their board propagation delays matched within 50pS of rgmii1_txc.



A. TXC is delayed internally before being driven to the rgmiin_txc pin. This internal delay is always enabled.

B. Data and control information is transmitted using both edges of the clocks. rgmiin_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin_txc and data bits 7-4 on the falling edge of rgmiin_txc. Similarly, rgmiin_txctl carries TXEN on rising edge of rgmiin_txc and TXERR of falling edge of rgmiin_txc.

Figure 5-74. GMAC Transmit Interface Timing RGMIIn Operation

In Table 5-115 are presented the specific groupings of signals (IOSET) for use with GMAC RGMII signals.

Table 5-115. GMAC RGMII IOSETs

SIGNALS	IOSET3		IOSET4	
	BALL	MUX	BALL	MUX
GMAC RGMII1				
rgmii1_txd3	C3	3		
rgmii1_txd2	C4	3		
rgmii1_txd1	B2	3		
rgmii1_txd0	D6	3		
rgmii1_rxd3	B3	3		
rgmii1_rxd2	B4	3		
rgmii1_rxd1	B5	3		

Table 5-115. GMAC RGMII IOSETs (continued)

SIGNALS	IOSET3		IOSET4	
	BALL	MUX	BALL	MUX
rgmii1_rxd0	A4	3		
rgmii1_rxctl	A3	3		
rgmii1_txc	D5	3		
rgmii1_txctl	C2	3		
rgmii1_rxc	C5	3		
GMAC RGMII0				
rgmii0_txd3			V7	0
rgmii0_txd2			U7	0
rgmii0_txd1			V6	0
rgmii0_txd0			U6	0
rgmii0_rxd3			V4	0
rgmii0_rxd2			V3	0
rgmii0_rxd1			Y2	0
rgmii0_rxd0			W2	0
rgmii0_txc			W9	0
rgmii0_rxctl			V5	0
rgmii0_rxc			U5	0
rgmii0_txctl			V9	0

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section "*Manual IO Timing Modes*" of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information please see the *Control Module Chapter* in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for GMAC. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-116, *Manual Functions Mapping for GMAC RGMII0* for a definition of the Manual modes.

Table 5-117 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-116. Manual Functions Mapping for GMAC RGMII0

BALL	BALL NAME	GMAC_RGMII0_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		0
U5	rgmii0_rxc	451	0	CFG_RGMII0_RXC_IN	rgmii0_rxc
V5	rgmii0_rxctl	127	1571	CFG_RGMII0_RXCTL_IN	rgmii0_rxctl
W2	rgmii0_rxd0	165	1178	CFG_RGMII0_RXD0_IN	rgmii0_rxd0
Y2	rgmii0_rxd1	136	1302	CFG_RGMII0_RXD1_IN	rgmii0_rxd1
V3	rgmii0_rxd2	0	1520	CFG_RGMII0_RXD2_IN	rgmii0_rxd2
V4	rgmii0_rxd3	28	1690	CFG_RGMII0_RXD3_IN	rgmii0_rxd3
W9	rgmii0_txc	121	0	CFG_RGMII0_TXC_OUT	rgmii0_txc
V9	rgmii0_txctl	410	0	CFG_RGMII0_TXCTL_OUT	rgmii0_txctl
U6	rgmii0_txd0	483	0	CFG_RGMII0_TXD0_OUT	rgmii0_txd0
V6	rgmii0_txd1	335	0	CFG_RGMII0_TXD1_OUT	rgmii0_txd1
U7	rgmii0_txd2	330	0	CFG_RGMII0_TXD2_OUT	rgmii0_txd2

Table 5-116. Manual Functions Mapping for GMAC RGMII0 (continued)

BALL	BALL NAME	GMAC_RGMII0_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		0
V7	rgmii0_txd3	522	0	CFG_RGMII0_TXD3_OUT	rgmii0_txd3

Manual IO Timings Modes must be used to guarantee some IO timings for GMAC. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-117, *Manual Functions Mapping for GMAC RGMII1* for a definition of the Manual modes.

Table 5-117 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-117. Manual Functions Mapping for GMAC RGMII1

BALL	BALL NAME	GMAC_RGMII1_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)		3
C5	vin2a_d18	417	0	CFG_VIN2A_D18_IN	rgmii1_rxc
A3	vin2a_d19	156	843	CFG_VIN2A_D19_IN	rgmii1_rxctl
B3	vin2a_d20	223	1413	CFG_VIN2A_D20_IN	rgmii1_rxd3
B4	vin2a_d21	169	1415	CFG_VIN2A_D21_IN	rgmii1_rxd2
B5	vin2a_d22	43	1150	CFG_VIN2A_D22_IN	rgmii1_rxd1
A4	vin2a_d23	0	1210	CFG_VIN2A_D23_IN	rgmii1_rxd0
D5	vin2a_d12	147	0	CFG_VIN2A_D12_OUT	rgmii1_txc
C2	vin2a_d13	480	0	CFG_VIN2A_D13_OUT	rgmii1_txctl
C3	vin2a_d14	378	0	CFG_VIN2A_D14_OUT	rgmii1_txd3
C4	vin2a_d15	562	0	CFG_VIN2A_D15_OUT	rgmii1_txd2
B2	vin2a_d16	483	0	CFG_VIN2A_D16_OUT	rgmii1_txd1
D6	vin2a_d17	380	0	CFG_VIN2A_D17_OUT	rgmii1_txd0

5.10.6.19 eMMC/SD/SDIO

The Device includes the following external memory interfaces 4 MultiMedia Card/Secure Digital/Secure Digital Input Output Interface (MMC/SD/SDIO).

NOTE

The eMMC/SD/SDIOi (i = 1 to 4) controller is also referred to as MMCi.

5.10.6.19.1 MMC1—SD Card Interface

MMC1 interface is compliant with the SD Standard v3.01 and it supports the following SD Card applications:

- Default speed, 4-bit data, SDR, half-cycle
- High speed, 4-bit data, SDR, half-cycle
- SDR12, 4-bit data, half-cycle
- SDR25, 4-bit data, half-cycle
- UHS-I SDR50, 4-bit data, half-cycle
- UHS-I SDR104, 4-bit data, half-cycle
- UHS-I DDR50, 4-bit data

NOTE

For more information, see the eMMC/SD/SDIO chapter of the Device TRM.

5.10.6.19.1.1 Default speed, 4-bit data, SDR, half-cycle

Table 5-118 and Table 5-119 present Timing requirements and Switching characteristics for MMC1 - Default Speed in receiver and transmitter mode (see Figure 5-75 and Figure 5-76)

Table 5-118. Timing Requirements for MMC1 - SD Card Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DSSD5	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	5.11		ns
DSSD6	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	20.46		ns
DSSD7	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge	5.11		ns
DSSD8	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge	20.46		ns

Table 5-119. Switching Characteristics for MMC1 - SD Card Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DSSD0	fop(clk)	Operating frequency, mmc1_clk		24	MHz
DSSD1	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5P-0.185[(1)]		ns
DSSD2	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5P-0.185 [(1)]		ns
DSSD3	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-14.93	14.93	ns
DSSD4	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-14.93	14.93	ns

(1) P = output mmc1_clk period in ns

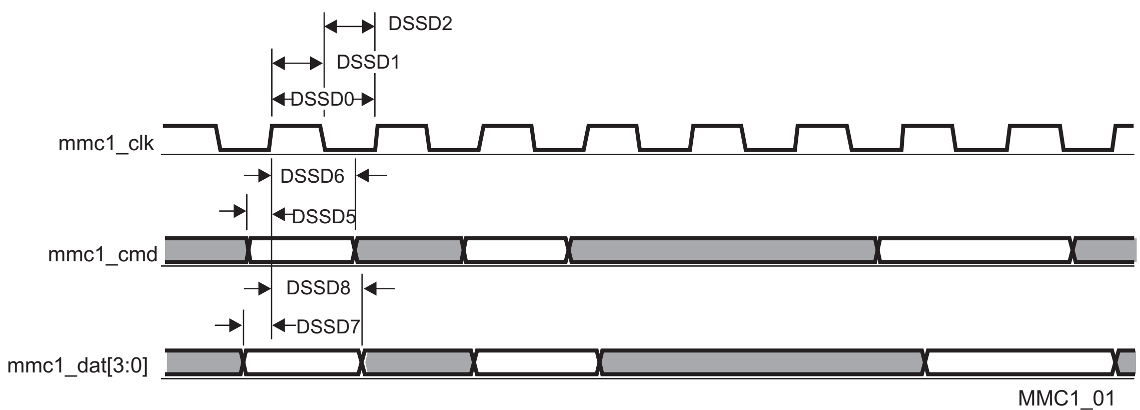


Figure 5-75. MMC/SD/SDIO in - Default Speed - Receiver Mode

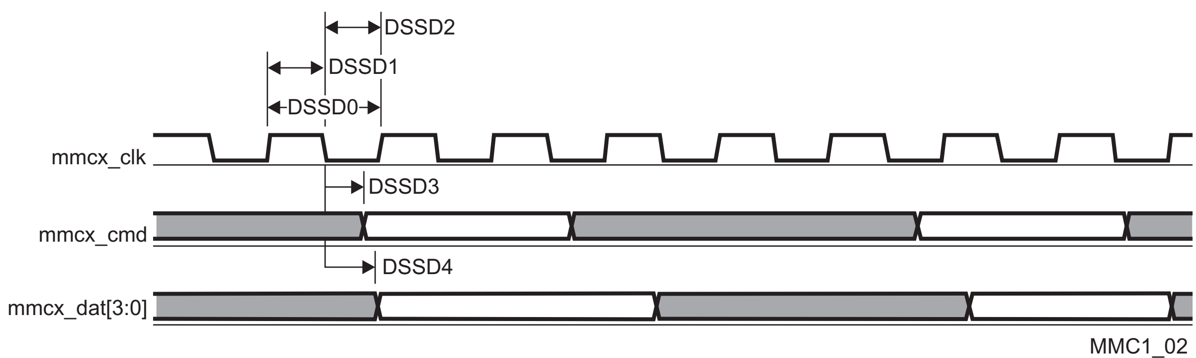


Figure 5-76. MMC/SD/SDIO in - Default Speed - Transmitter Mode

5.10.6.19.1.2 High speed, 4-bit data, SDR, half-cycle

Table 5-120 and Table 5-121 present Timing requirements and Switching characteristics for MMC1 - High Speed in receiver and transmitter mode (see Figure 5-77 and Figure 5-78)

Table 5-120. Timing Requirements for MMC1 - SD Card High Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HSSD3	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge	5.3		ns
HSSD4	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge	2.6		ns
HSSD7	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge	5.3		ns
HSSD8	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge	2.6		ns

Table 5-121. Switching Characteristics for MMC1 - SD Card High Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HSSD1	fop(clk)	Operating frequency, mmc1_clk		48	MHz
HSSD2H	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5P-0.185 (1)		ns
HSSD2L	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5P-0.185 (1)		ns
HSSD5	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-7.6	3.6	ns
HSSD6	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-7.6	3.6	ns

(1) P = output mmc1_clk period in ns

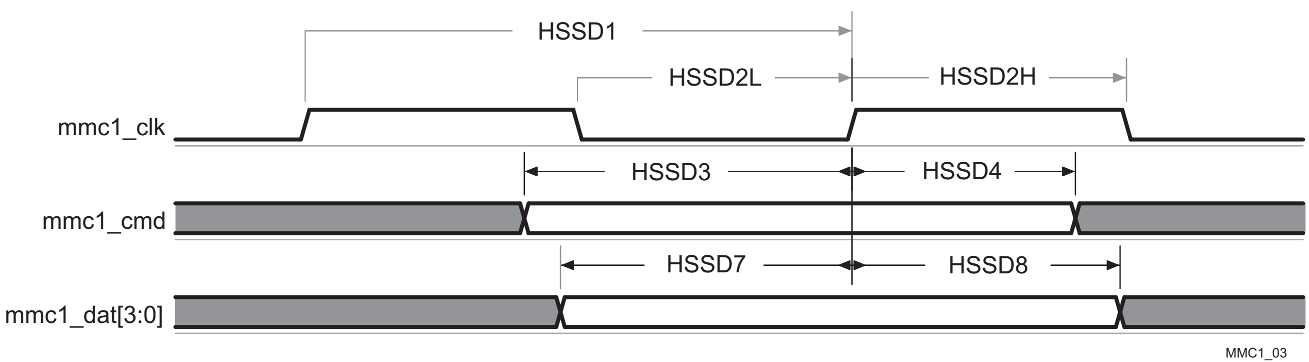


Figure 5-77. MMC/SD/SDIO in - High Speed - Receiver Mode

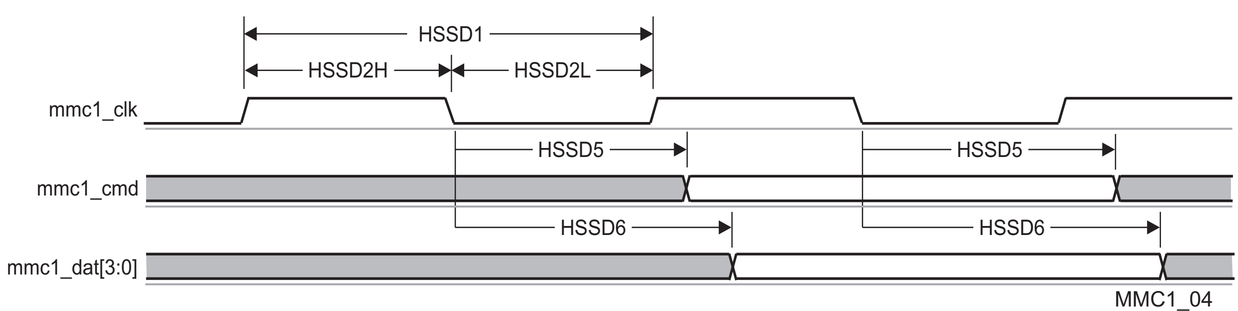


Figure 5-78. MMC/SD/SDIO in - High Speed - Transmitter Mode

5.10.6.19.1.3 SDR12, 4-bit data, half-cycle

Table 5-122 and Table 5-123 present Timing requirements and Switching characteristics for MMC1 - SDR12 in receiver and transmitter mode (see Figure 5-79 and Figure 5-80).

Table 5-122. Timing Requirements for MMC1 - SD Card SDR12 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge		25.99		ns
SDR126	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge		1.6		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge		25.99		ns
SDR128	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge		1.6		ns

Table 5-123. Switching Characteristics for MMC1 - SD Card SDR12 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	fop(clk)	Operating frequency, mmc1_clk		24	MHz
SDR121	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5P-0.185 (1)		ns
SDR122	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5P-0.185 (1)		ns
SDR123	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-19.13	16.93	ns
SDR124	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-19.13	16.93	ns

(1) P = output mmc1_clk period in ns

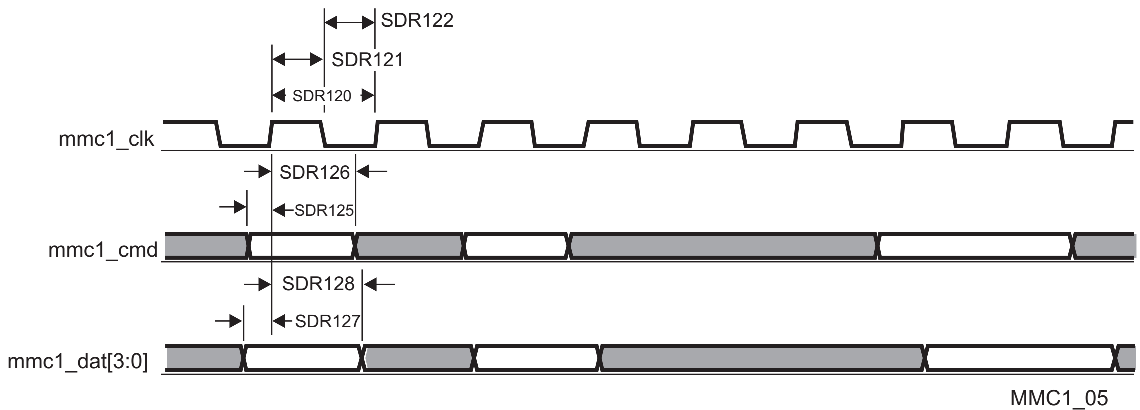


Figure 5-79. MMC/SD/SDIO in - High Speed SDR12 - Receiver Mode

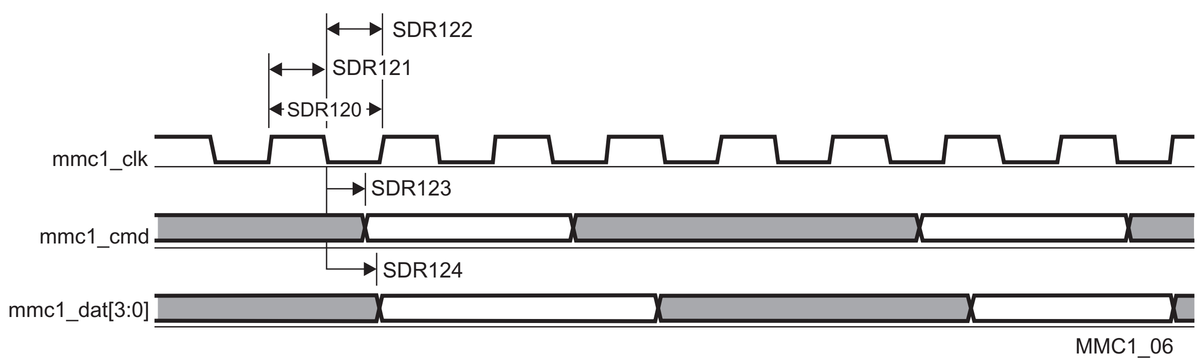


Figure 5-80. MMC/SD/SDIO in - High Speed SDR12 - Transmitter Mode

5.10.6.19.1.4 SDR25, 4-bit data, half-cycle

Table 5-124 and Table 5-125 present Timing requirements and Switching characteristics for MMC1 - SDR25 in receiver and transmitter mode (see Figure 5-81 and Figure 5-82).

Table 5-124. Timing Requirements for MMC1 - SD Card SDR25 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SDR253	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge		5.3		ns
SDR254	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge		1.6		ns
SDR257	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge		5.3		ns
SDR258	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge		1.6		ns

Table 5-125. Switching Characteristics for MMC1 - SD Card SDR25 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	fop(clk)	Operating frequency, mmc1_clk		48	MHz
SDR252H	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5P-0.185 (1)		ns
SDR252L	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5P-0.185 (1)		ns
SDR255	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-8.8	6.6	ns
SDR256	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-8.8	6.6	ns

(1) P = output mmc1_clk period in ns

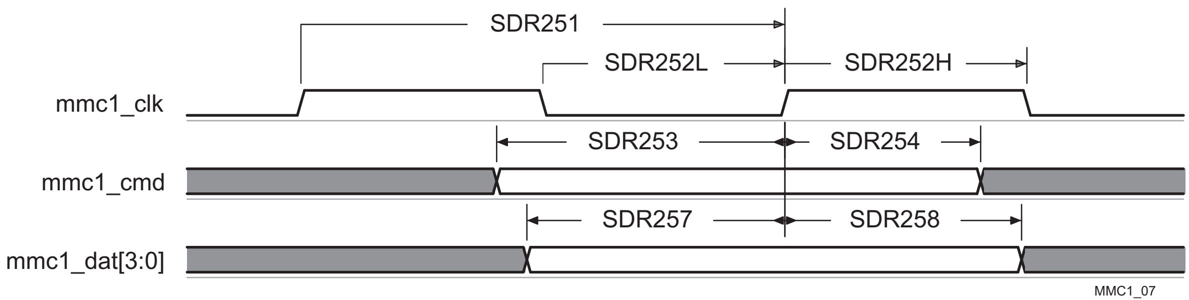


Figure 5-81. MMC/SD/SDIO in - High Speed SDR25 - Receiver Mode

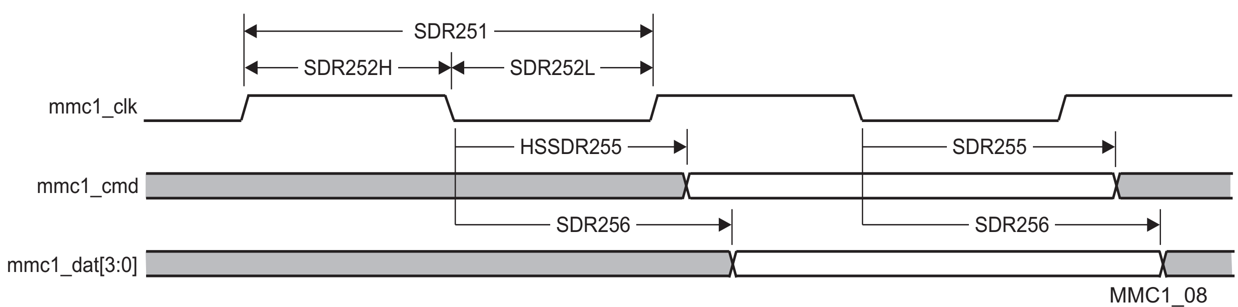


Figure 5-82. MMC/SD/SDIO in - High Speed SDR25 - Transmitter Mode

5.10.6.19.1.5 UHS-I SDR50, 4-bit data, half-cycle

Table 5-126 and Table 5-127 present Timing requirements and Switching characteristics for MMC1 - SDR50 in receiver and transmitter mode (see Figure 5-83 and Figure 5-84).

Table 5-126. Timing Requirements for MMC1 - SD Card SDR50 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SDR503	$t_{su(cmdV-clkH)}$	Setup time, mmc1_cmd valid before mmc1_clk rising clock edge		1.48		ns

Table 5-126. Timing Requirements for MMC1 - SD Card SDR50 Mode (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SDR504	$t_{h(clkH-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk rising clock edge		1.6		ns
SDR507	$t_{su(dV-clkH)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk rising clock edge		1.48		ns
SDR508	$t_{h(clkH-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk rising clock edge		1.6		ns

Table 5-127. Switching Characteristics for MMC1 - SD Card SDR50 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR501	fop(clk)	Operating frequency, mmc1_clk		96	MHz
SDR502H	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5P-0.185 (1)		ns
SDR502L	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5P-0.185 (1)		ns
SDR505	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-3.66	1.46	ns
SDR506	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-3.66	1.46	ns

(1) P = output mmc1_clk period in ns

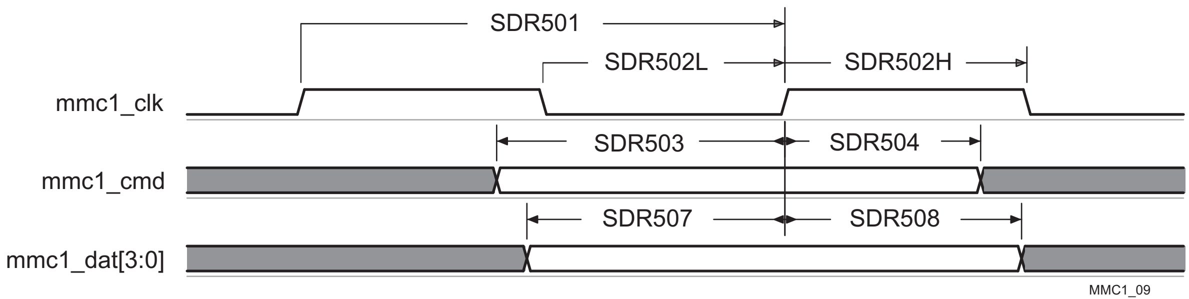


Figure 5-83. MMC/SD/SDIO in - High Speed SDR50 - Receiver Mode

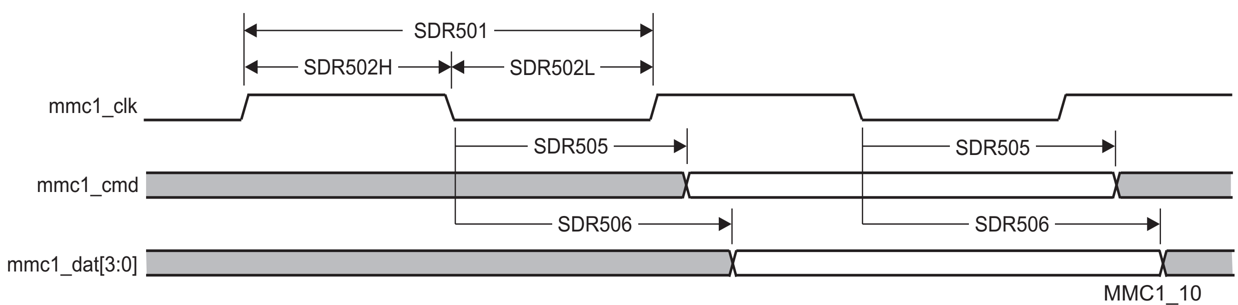


Figure 5-84. MMC/SD/SDIO in - High Speed SDR50 - Transmitter Mode

5.10.6.19.1.6 UHS-I SDR104, 4-bit data, half-cycle

Table 5-128 presents Timing requirements and Switching characteristics for MMC1 - SDR104 in receiver and transmitter mode (see Figure 5-85 and Figure 5-86)

Table 5-128. Switching Characteristics for MMC1 - SD Card SDR104 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR1041	fop(clk)	Operating frequency, mmc1_clk		192	MHz
SDR1042H	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5P-0.185 (1)		ns

Table 5-128. Switching Characteristics for MMC1 - SD Card SDR104 Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR1042L	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5P-0.185 (1)		ns
SDR1045	$t_{d(clkL-cmdV)}$	Delay time, mmc1_clk falling clock edge to mmc1_cmd transition	-1.09	0.49	ns
SDR1046	$t_{d(clkL-dV)}$	Delay time, mmc1_clk falling clock edge to mmc1_dat[3:0] transition	-1.09	0.49	ns

(1) P = output mmc1_clk period in ns

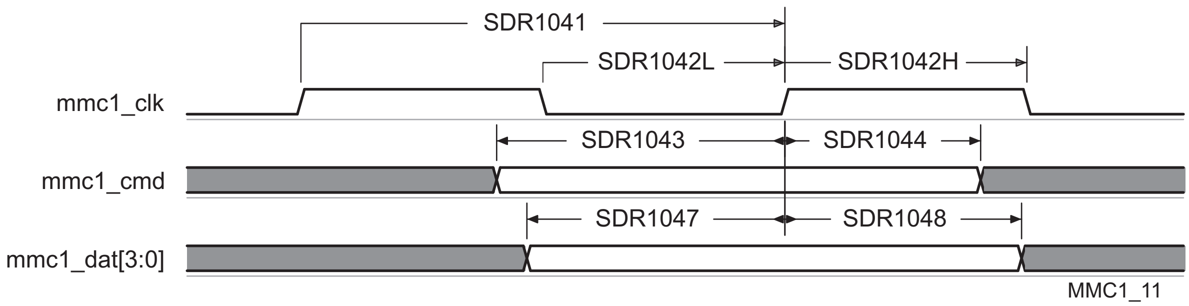


Figure 5-85. MMC/SD/SDIO in - High Speed SDR104 - Receiver Mode

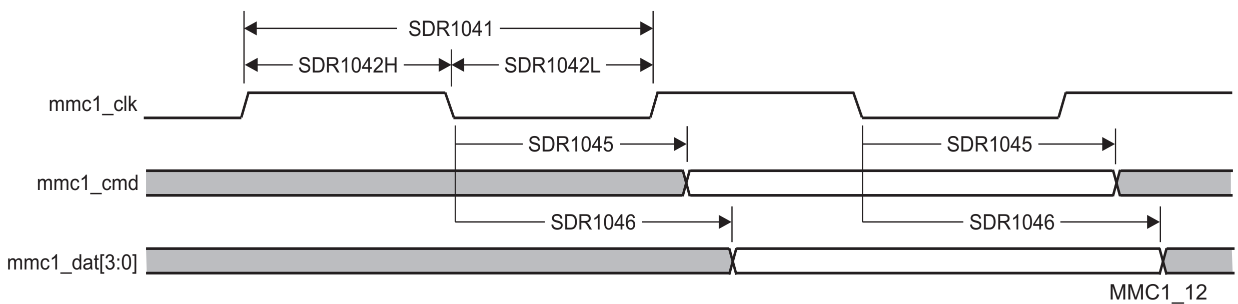


Figure 5-86. MMC/SD/SDIO in - High Speed SDR104 - Transmitter Mode

5.10.6.19.1.7 UHS-I DDR50, 4-bit data

Table 5-129 and Table 5-130 present Timing requirements and Switching characteristics for MMC1 - DDR50 in receiver and transmitter mode (see Figure 5-87 and Figure 5-88).

Table 5-129. Timing Requirements for MMC1 - SD Card DDR50 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR505	$t_{su(cmdV-clk)}$	Setup time, mmc1_cmd valid before mmc1_clk transition		1.79		ns
DDR506	$t_{h(clk-cmdV)}$	Hold time, mmc1_cmd valid after mmc1_clk transition		1.6		ns
DDR507	$t_{su(dV-clk)}$	Setup time, mmc1_dat[3:0] valid before mmc1_clk transition		1.79		ns
DDR508	$t_{h(clk-dV)}$	Hold time, mmc1_dat[3:0] valid after mmc1_clk transition		1.6		ns

Table 5-130. Switching Characteristics for MMC1 - SD Card DDR50 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR500	fop(clk)	Operating frequency, mmc1_clk		48	MHz
DDR501	$t_{w(clkH)}$	Pulse duration, mmc1_clk high	0.5P-0.185 (1)		ns
DDR502	$t_{w(clkL)}$	Pulse duration, mmc1_clk low	0.5P-0.185 (1)		ns
DDR503	$t_{d(clk-cmdV)}$	Delay time, mmc1_clk transition to mmc1_cmd transition	1.225	6.6	ns
DDR504	$t_{d(clk-dV)}$	Delay time, mmc1_clk transition to mmc1_dat[3:0] transition	1.225	6.6	ns

(1) P = output mmc1_clk period in ns

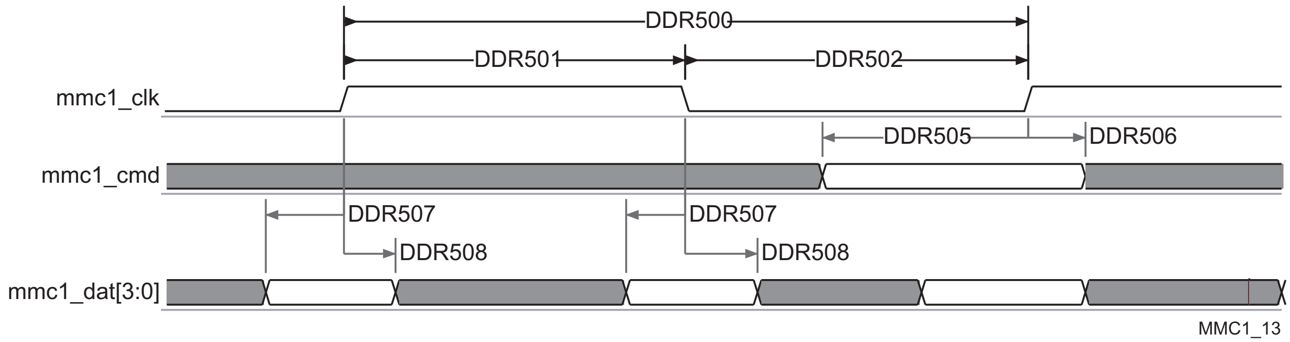


Figure 5-87. SDMMC - High Speed SD - DDR - Data/Command Receive

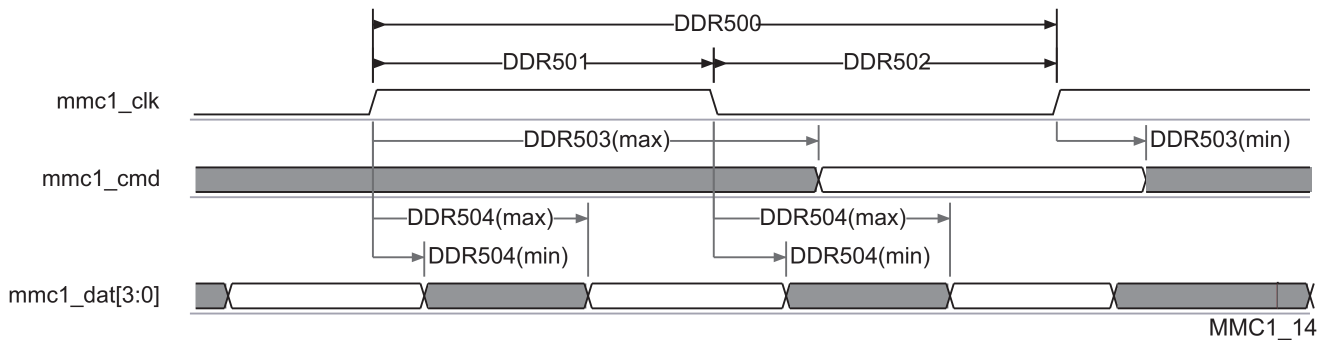


Figure 5-88. SDMMC - High Speed SD - DDR - Data/Command Transmit

NOTE

To configure the desired virtual mode the user must set MODESELECT bit and DELAYMODE bitfield for each corresponding pad control register.

The pad control registers are presented in Table 4-29 and described in Device TRM, *Control Module Chapter*.

Virtual IO Timings Modes must be used to guarantee some IO timings for MMC1. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Virtual IO Timings Modes. See Table 5-131, *Virtual Functions Mapping for MMC1* for a definition of the Virtual modes.

Table 5-131 presents the values for DELAYMODE bitfield.

Table 5-131. Virtual Functions Mapping for MMC1

BALL	BALL NAME	Delay Mode Value					MUXMODE[15:0]
		MMC1_VIRTUAL1	MMC1_VIRTUAL2	MMC1_VIRTUAL5	MMC1_VIRTUAL6	MMC1_VIRTUAL7	0
W6	mmc1_clk	11	10	7	6	5	mmc1_clk
W5	mmc1_cmd	11	10	7	6	5	mmc1_cmd
V5	mmc1_dat0	11	10	7	6	5	mmc1_dat0
Y4	mmc1_dat1	11	10	7	6	5	mmc1_dat1
AA5	mmc1_dat2	11	10	7	6	5	mmc1_dat2
Y3	mmc1_dat3	11	10	7	6	5	mmc1_dat3

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for MMC1. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-132, *Manual Functions Mapping for MMC1* for a definition of the Manual modes.

Table 5-132 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-132. Manual Functions Mapping for MMC1

BALL	BALL NAME	MMC1_DDR_MANUAL1		MMC1_SDR104_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0
W6	mmc1_clk	489	0	-	-	CFG_MMC1_CLK_IN	mmc1_clk
W5	mmc1_cmd	0	0	-	-	CFG_MMC1_CMD_IN	mmc1_cmd
V5	mmc1_dat0	374	0	-	-	CFG_MMC1_DAT0_IN	mmc1_dat0
Y4	mmc1_dat1	31	0	-	-	CFG_MMC1_DAT1_IN	mmc1_dat1
AA5	mmc1_dat2	56	0	-	-	CFG_MMC1_DAT2_IN	mmc1_dat2
Y3	mmc1_dat3	0	0	-	-	CFG_MMC1_DAT3_IN	mmc1_dat3
W6	mmc1_clk	1355	0	892	0	CFG_MMC1_CLK_OUT	mmc1_clk
W5	mmc1_cmd	0	0	0	0	CFG_MMC1_CMD_OEN	mmc1_cmd
W5	mmc1_cmd	0	0	0	0	CFG_MMC1_CMD_OUT	mmc1_cmd
V5	mmc1_dat0	0	0	0	0	CFG_MMC1_DAT0_OEN	mmc1_dat0
V5	mmc1_dat0	0	4	0	0	CFG_MMC1_DAT0_OUT	mmc1_dat0
Y4	mmc1_dat1	0	0	0	0	CFG_MMC1_DAT1_OEN	mmc1_dat1
Y4	mmc1_dat1	0	0	0	0	CFG_MMC1_DAT1_OUT	mmc1_dat1
AA5	mmc1_dat2	0	0	0	0	CFG_MMC1_DAT2_OEN	mmc1_dat2
AA5	mmc1_dat2	0	0	0	0	CFG_MMC1_DAT2_OUT	mmc1_dat2
Y3	mmc1_dat3	0	0	0	0	CFG_MMC1_DAT3_OEN	mmc1_dat3
Y3	mmc1_dat3	0	0	0	0	CFG_MMC1_DAT3_OUT	mmc1_dat3

5.10.6.19.2 MMC2 — eMMC

MMC2 interface is compliant with the JC64 eMMC Standard v4.5 and it supports the following eMMC applications:

- Standard JC64 SDR, 8-bit data, half cycle
- High-speed JC64 SDR, 8-bit data, half cycle
- High-speed JC64 DDR, 8-bit data
- High-speed HS200 JC64 SDR, 8-bit data, half cycle

NOTE

For more information, see the eMMC/SD/SDIO chapter of the Device TRM.

5.10.6.19.2.1 Standard JC64 SDR, 8-bit data, half cycle

Table 5-133 and Table 5-134 present Timing requirements and Switching characteristics for MMC2 - Standard SDR in receiver and Transmitter mode (see Figure 5-89 and Figure 5-90).

Table 5-133. Timing Requirements for MMC2 - JC64 Standard SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SSDR5	$t_{su(cmdV-clkH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	13.19		ns
SSDR6	$t_{h(clkH-cmdV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	8.4		ns
SSDR7	$t_{su(dV-clkH)}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk rising clock edge	13.19		ns
SSDR8	$t_{h(clkH-dV)}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk rising clock edge	8.4		ns

Table 5-134. Switching Characteristics for MMC2 - JC64 Standard SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SSDR1	$f_{op(clk)}$	Operating frequency, mmc2_clk		24	MHz
SSDR2H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5P-0.172 (1)		ns
SSDR2L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5P-0.172 (1)		ns
SSDR3	$t_{d(clkL-cmdV)}$	Delay time, mmc2_clk falling clock edge to mmc2_cmd transition	-16.96	16.96	ns
SSDR4	$t_{d(clkL-dV)}$	Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition	-16.96	16.96	ns

(1) P = output mmc2_clk period in ns

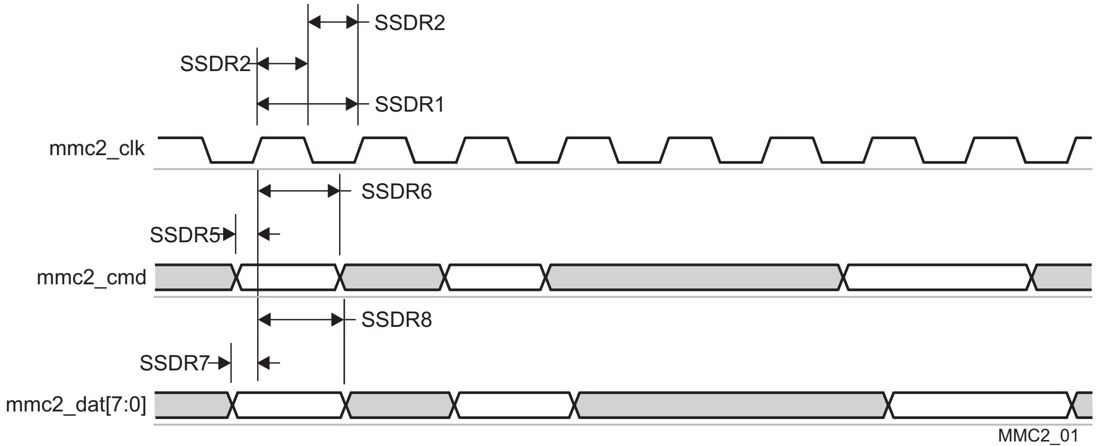


Figure 5-89. MMC/SD/SDIO in - Standard JC64 - Receiver Mode

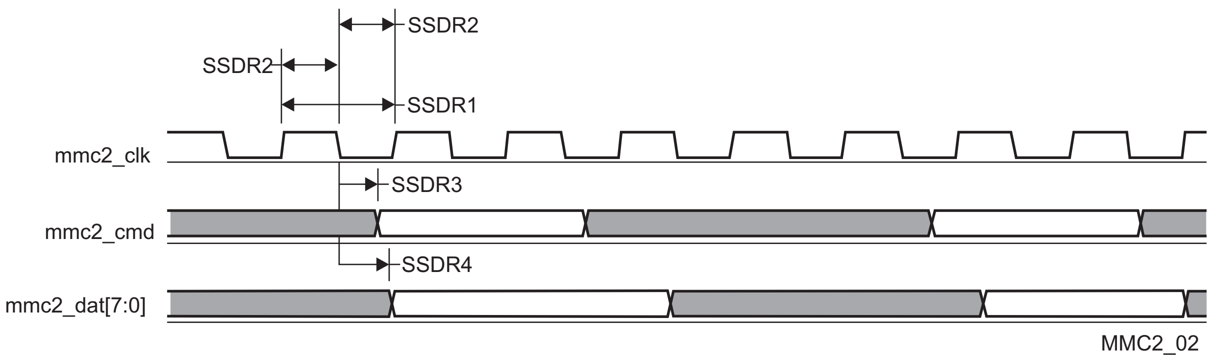


Figure 5-90. MMC/SD/SDIO in - Standard JC64 - Transmitter Mode

5.10.6.19.2.2 High-Speed JC64 SDR, 8-bit data, half cycle

Table 5-135 and Table 5-136 present Timing requirements and Switching characteristics for MMC2 - High speed SDR in receiver and transmitter mode (see Figure 5-91 and Figure 5-92).

Table 5-135. Timing Requirements for MMC2 - JC64 High-Speed SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
JC643	$t_{su(cmdV-clkH)}$	Setup time, mmc2_cmd valid before mmc2_clk rising clock edge	5.6		ns
JC644	$t_{h(clkH-cmdV)}$	Hold time, mmc2_cmd valid after mmc2_clk rising clock edge	2.6		ns
JC647	$t_{su(dV-clkH)}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk rising clock edge	5.6		ns
JC648	$t_{h(clkH-dV)}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk rising clock edge	2.6		ns

Table 5-136. Switching Characteristics for MMC2 - JC64 High-Speed SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
JC641	$f_{op(clk)}$	Operating frequency, mmc2_clk		48	MHz
JC642H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5P-0.172 (1)		ns
JC642L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5P-0.172 (1)		ns
JC645	$t_{d(clkL-cmdV)}$	Delay time, mmc2_clk falling clock edge to mmc2_cmd transition	-6.64	6.64	ns
JC646	$t_{d(clkL-dV)}$	Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition	-6.64	6.64	ns

(1) P = output mmc2_clk period in ns

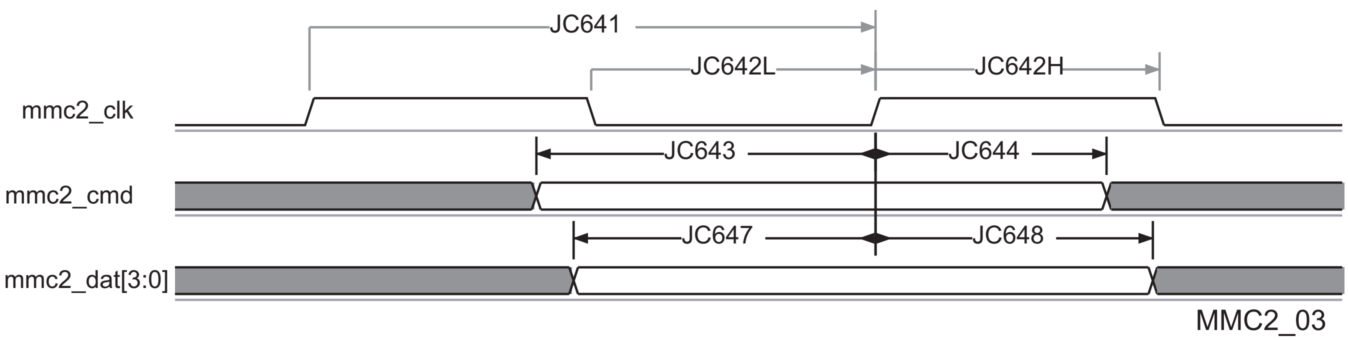


Figure 5-91. MMC/SD/SDIO in - High-Speed JC64 - Receiver Mode

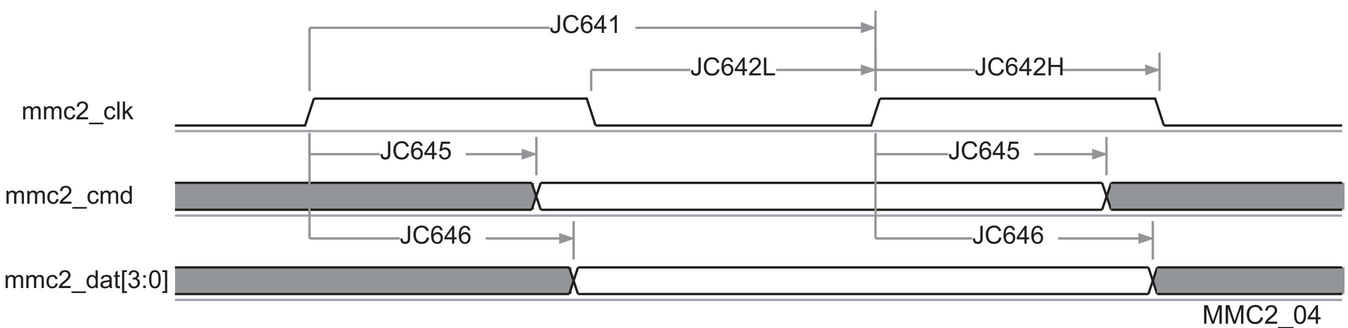


Figure 5-92. MMC/SD/SDIO in - High-Speed JC64 - Transmitter Mode

5.10.6.19.2.3 High-Speed HS200 JC64 SDR, 8-bit data, half cycle

Table 5-137 presents Timing requirements and Switching characteristics for MMC2 - HS200 in receiver and transmitter mode (see Figure 5-93).

Table 5-137. Switching Characteristics for MMC2 - JEDS84 HS200 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS2001	fop(clk)	Operating frequency, mmc2_clk		192	MHz
HS2002H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5P-0.172 (1)		ns
HS2002L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5P-0.172 (1)		ns
HS2005	$t_{d(clkL-cmdV)}$	Delay time, mmc2_clk falling clock edge to mmc2_cmd transition	-1.136	0.536	ns
HS2006	$t_{d(clkL-dV)}$	Delay time, mmc2_clk falling clock edge to mmc2_dat[7:0] transition	-1.136	0.536	ns

(1) P = output mmc2_clk period in ns

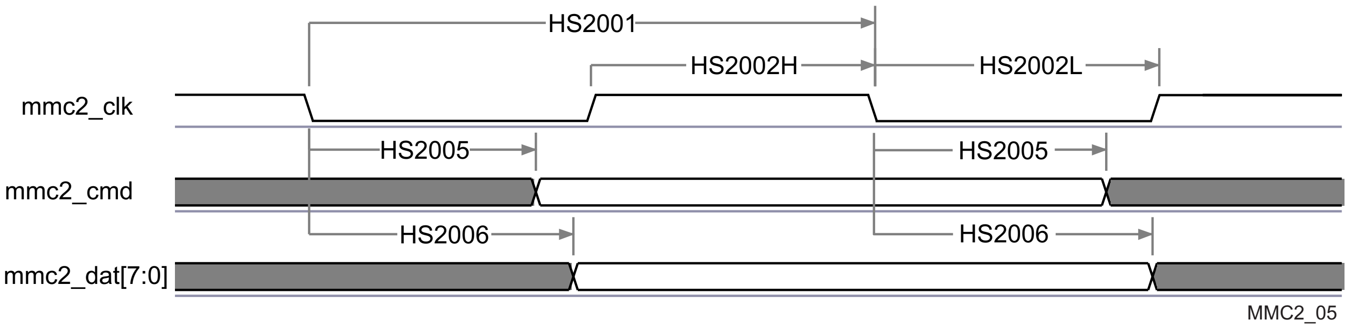


Figure 5-93. eMMC in - HS200 SDR - Transmitter Mode

5.10.6.19.2.4 High-Speed JC64 DDR, 8-bit data

Table 5-138 and Table 5-139 present Timing requirements and Switching characteristics for MMC2 - High speed DDR in receiver and transmitter mode (see Figure 5-94 and Figure 5-95).

Table 5-138. Timing Requirements for MMC2 - JC64 High-Speed DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR3	$t_{su(cmdV-clk)}$	Setup time, mmc2_cmd valid before mmc2_clk transition		1.8		ns
DDR4	$t_{h(clk-cmdV)}$	Hold time, mmc2_cmd valid after mmc2_clk transition		1.6		ns
DDR7	$t_{su(dV-clk)}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk transition		1.8		ns
DDR8	$t_{h(clk-dV)}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk transition		1.6		ns

Table 5-139. Switching Characteristics for MMC2 - JC64 High-Speed DDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR1	$f_{op(clk)}$	Operating frequency, mmc2_clk		48	MHz
DDR2H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	0.5P-0.172 (1)		ns
DDR2L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	0.5P-0.172 (1)		ns
DDR5	$t_{d(clk-cmdV)}$	Delay time, mmc2_clk transition to mmc2_cmd transition	2.9	7.14	ns
DDR6	$t_{d(clk-dV)}$	Delay time, mmc2_clk transition to mmc2_dat[7:0] transition	2.9	7.14	ns

(1) P = output mmc2_clk period in ns

Table 5-140 and Table 5-141 present Timing requirements and Switching characteristics for MMC2 - High speed DDR in receiver and transmitter mode During Boot (see Figure 5-94 and Figure 5-95).

Table 5-140. Timing Requirements for MMC2 - JC64 High-Speed DDR Mode During Boot

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR3	$t_{su(cmdV-clk)}$	Setup time, mmc2_cmd valid before mmc2_clk transition	Boot	1.8		ns
DDR4	$t_{h(clk-cmdV)}$	Hold time, mmc2_cmd valid after mmc2_clk transition	Boot	1.8(1)		ns
DDR7	$t_{su(dV-clk)}$	Setup time, mmc2_dat[7:0] valid before mmc2_clk transition	Boot	1.8		ns
DDR8	$t_{h(clk-dV)}$	Hold time, mmc2_dat[7:0] valid after mmc2_clk transition	Boot	1.8(1)		ns

(1) This Hold time requirement is larger than the Hold time provided by a typical eMMC component. Therefore, the trace length between the Device and eMMC component must be sufficiently long enough to ensure that the Hold time is met at the Device.

Table 5-141. Switching Characteristics for MMC2 - JC64 High-Speed DDR Mode During Boot

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR1	fop(clk)	Operating frequency, mmc2_clk	Boot		48	MHz

Table 5-141. Switching Characteristics for MMC2 - JC64 High-Speed DDR Mode During Boot (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DDR2H	$t_{w(clkH)}$	Pulse duration, mmc2_clk high	Boot	0.5P-0.172 (1)		ns
DDR2L	$t_{w(clkL)}$	Pulse duration, mmc2_clk low	Boot	0.5P-0.172 (1)		ns
DDR5	$t_{d(clk-cmdV)}$	Delay time, mmc2_clk transition to mmc2_cmd transition	Boot	2.9	7.14	ns
DDR6	$t_{d(clk-dV)}$	Delay time, mmc2_clk transition to mmc2_dat[7:0] transition	Boot	2.9	7.14	ns

(1) P = output mmc2_clk period in ns

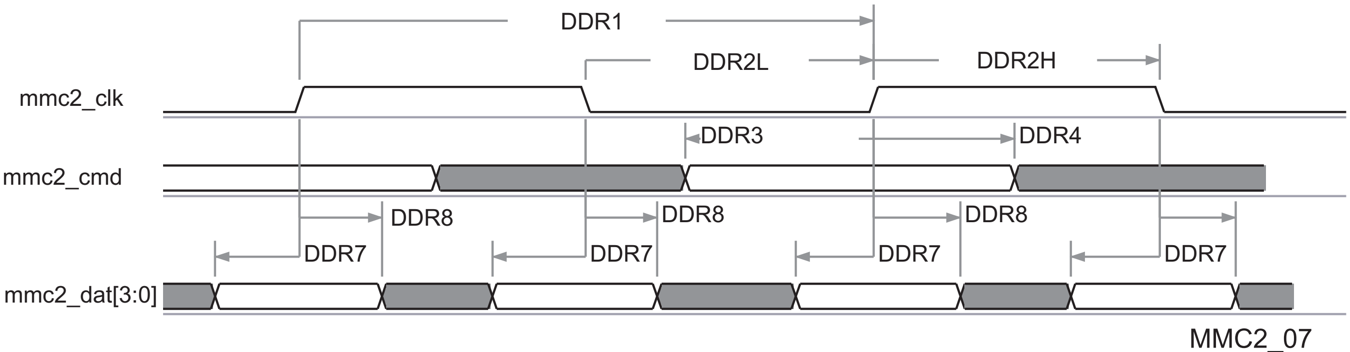


Figure 5-94. MMC/SD/SDIO in - High-Speed DDR JC64 - Receiver Mode

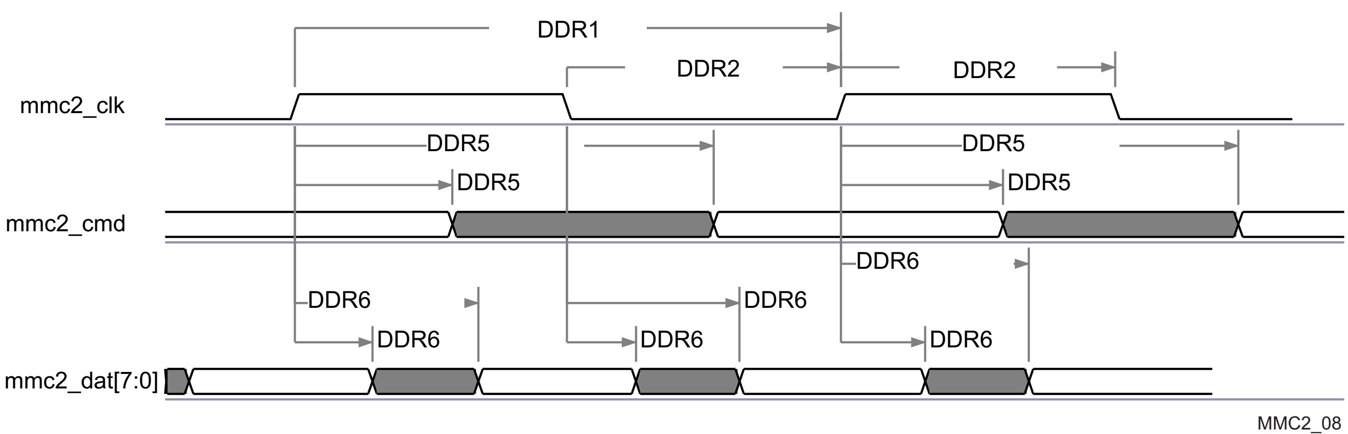


Figure 5-95. MMC/SD/SDIO in - High-Speed DDR JC64 - Transmitter Mode

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for MMC2. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-142, *Manual Functions Mapping for MMC2 with Internal Loopback Clock and for HS200* for a definition of the Manual modes.

Table 5-142 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-142. Manual Functions Mapping for MMC2 With Internal Loopback Clock and for HS200

BALL	BALL NAME	MMC2_DDR_LB_MANUAL1		MMC2_STD_HS_LB_MANUAL1		MMC2_HS200_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		1
K7	gpmc_a19	124	0	850	0	-	-	CFG_GPMC_A19_IN	mmc2_dat4
M7	gpmc_a20	62	0	1264	0	-	-	CFG_GPMC_A20_IN	mmc2_dat5
J5	gpmc_a21	0	0	786	0	-	-	CFG_GPMC_A21_IN	mmc2_dat6
K6	gpmc_a22	0	0	902	0	-	-	CFG_GPMC_A22_IN	mmc2_dat7
J7	gpmc_a23	645	3054	0	2764	-	-	CFG_GPMC_A23_IN	mmc2_clk
J4	gpmc_a24	48	0	1185	0	-	-	CFG_GPMC_A24_IN	mmc2_dat0
J6	gpmc_a25	0	0	670	0	-	-	CFG_GPMC_A25_IN	mmc2_dat1
H4	gpmc_a26	0	0	972	0	-	-	CFG_GPMC_A26_IN	mmc2_dat2
H5	gpmc_a27	0	0	1116	0	-	-	CFG_GPMC_A27_IN	mmc2_dat3
H6	gpmc_cs1	0	0	250	0	-	-	CFG_GPMC_CS1_IN	mmc2_cmd
K7	gpmc_a19	0	0	0	0	384	0	CFG_GPMC_A19_OEN	mmc2_dat4
K7	gpmc_a19	135	0	0	0	350	174	CFG_GPMC_A19_OUT	mmc2_dat4
M7	gpmc_a20	0	0	0	0	410	0	CFG_GPMC_A20_OEN	mmc2_dat5
M7	gpmc_a20	47	0	0	0	335	0	CFG_GPMC_A20_OUT	mmc2_dat5
J5	gpmc_a21	0	0	0	0	468	0	CFG_GPMC_A21_OEN	mmc2_dat6
J5	gpmc_a21	101	0	0	0	339	0	CFG_GPMC_A21_OUT	mmc2_dat6
K6	gpmc_a22	0	0	0	0	676	0	CFG_GPMC_A22_OEN	mmc2_dat7
K6	gpmc_a22	30	0	0	0	219	0	CFG_GPMC_A22_OUT	mmc2_dat7
J7	gpmc_a23	423	0	0	0	1062	154	CFG_GPMC_A23_OUT	mmc2_clk
J4	gpmc_a24	0	0	0	0	640	0	CFG_GPMC_A24_OEN	mmc2_dat0
J4	gpmc_a24	0	0	0	0	150	0	CFG_GPMC_A24_OUT	mmc2_dat0
J6	gpmc_a25	0	0	0	0	356	0	CFG_GPMC_A25_OEN	mmc2_dat1
J6	gpmc_a25	0	0	0	0	150	0	CFG_GPMC_A25_OUT	mmc2_dat1
H4	gpmc_a26	0	0	0	0	579	0	CFG_GPMC_A26_OEN	mmc2_dat2
H4	gpmc_a26	0	0	0	0	200	0	CFG_GPMC_A26_OUT	mmc2_dat2
H5	gpmc_a27	0	0	0	0	435	0	CFG_GPMC_A27_OEN	mmc2_dat3
H5	gpmc_a27	0	0	0	0	236	0	CFG_GPMC_A27_OUT	mmc2_dat3
H6	gpmc_cs1	0	0	0	0	759	0	CFG_GPMC_CS1_OEN	mmc2_cmd
H6	gpmc_cs1	0	0	0	0	372	0	CFG_GPMC_CS1_OUT	mmc2_cmd

5.10.6.19.3 MMC3 and MMC4—SDIO/SD

MMC3 and MMC4 interfaces are compliant with the SDIO3.0 standard v1.0, SD Part E1 and for generic SDIO devices, it supports the following applications:

- MMC3 8-bit data and MMC4 4-bit data, SD Default speed, SDR
- MMC3 8-bit data and MMC4 4-bit data, SD High speed, SDR
- MMC3 8-bit data and MMC4 4-bit data, UHS-1 SDR12 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC3 8-bit data and MMC4 4-bit data, UHS-I SDR25 (SD Standard v3.01), 4-bit data, SDR, half cycle
- MMC3 8-bit data, UHS-I SDR50

NOTE
The eMMC/SD/SDIOj (j = 3 to 4) controller is also referred to as MMCj.

NOTE
For more information, see the MMC/SDIO chapter of the Device TRM.

5.10.6.19.3.1 MMC3 and MMC4, SD Default Speed

Figure 5-96, Figure 5-97, and Table 5-143 through Table 5-146 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD Default speed in receiver and transmitter mode.

Table 5-143. Timing Requirements for MMC3 - Default Speed Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS5	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.11		ns
DS6	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	20.46		ns
DS7	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.11		ns
DS8	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	20.46		ns

(1) i in [i:0] = 7

Table 5-144. Switching Characteristics for MMC3 - SD/SDIO Default Speed Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS0	fop(clk)	Operating frequency, mmc3_clk		24	MHz
DS1	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5P-0.270 (1)		ns
DS2	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5P-0.270 (1)		ns
DS3	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-14.93	14.93	ns
DS4	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-14.93	14.93	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

Table 5-145. Timing Requirements for MMC4 - Default Speed Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS5	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.11		ns
DS6	$t_{h(clkH-cmdV)}$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	20.46		ns
DS7	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.11		ns
DS8	$t_{h(clkH-dV)}$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	20.46		ns

(1) i in [i:0] = 3

Table 5-146. Switching Characteristics for MMC4 - Default Speed Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS0	fop(clk)	Operating frequency, mmc4_clk		24	MHz
DS1	$t_{w(clkH)}$	Pulse duration, mmc4_clk high	0.5P-0.270 (1)		ns
DS2	$t_{w(clkL)}$	Pulse duration, mmc4_clk low	0.5P-0.270 (1)		ns
DS3	$t_{d(clkL-cmdV)}$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-14.93	14.93	ns
DS4	$t_{d(clkL-dV)}$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-14.93	14.93	ns

(1) P = output mmc4_clk period in ns

(2) i in [i:0] = 3

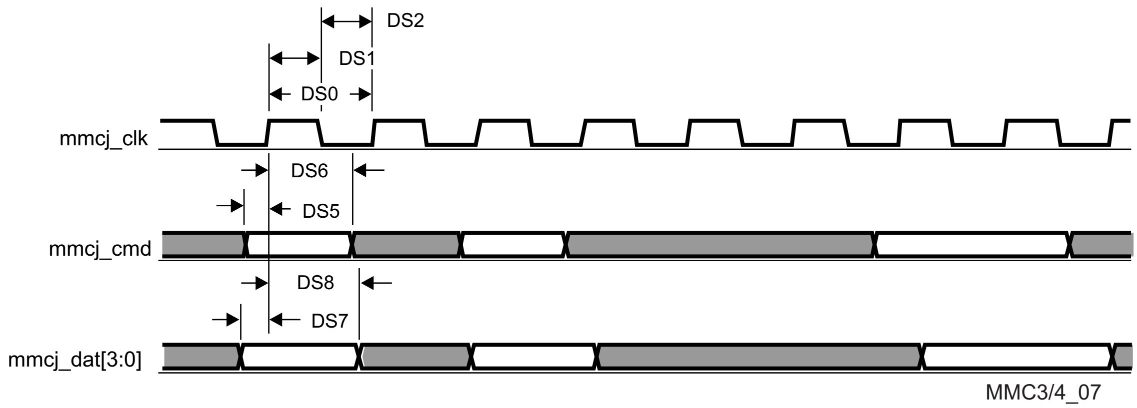


Figure 5-96. MMC/SD/SDIOj in - Default Speed - Receiver Mode

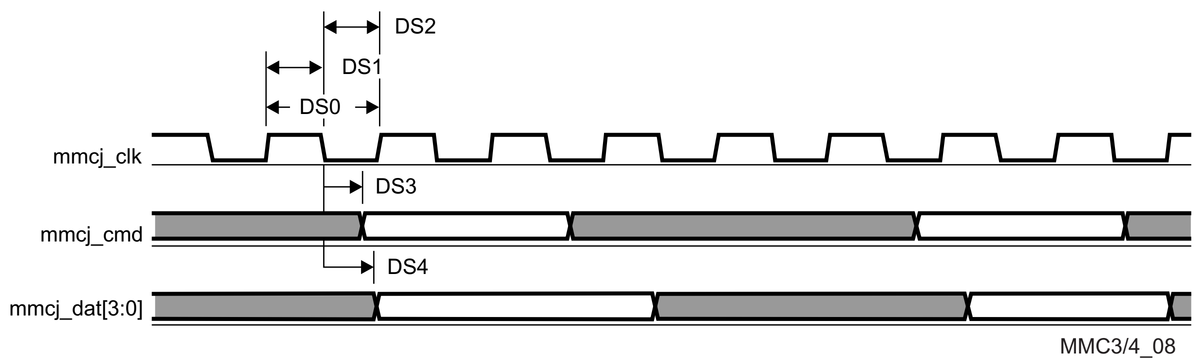


Figure 5-97. MMC/SD/SDIOj in - Default Speed - Transmitter Mode

5.10.6.19.3.2 MMC3 and MMC4, SD High Speed

Figure 5-98, Figure 5-99, and Table 5-147 through Table 5-150 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO High speed in receiver and transmitter mode.

Table 5-147. Timing Requirements for MMC3 - SD/SDIO High Speed Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS3	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.3		ns
HS4	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	2.6		ns
HS7	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.3		ns

Table 5-147. Timing Requirements for MMC3 - SD/SDIO High Speed Mode [(1)] (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS8	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	2.6		ns

(1) i in [i:0] = 7

Table 5-148. Switching Characteristics for MMC3 - SD/SDIO High Speed Mode [(2)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS1	fop(clk)	Operating frequency, mmc3_clk		48	MHz
HS2H	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5P-0.270 [(1)]		ns
HS2L	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5P-0.270 [(1)]		ns
HS5	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-7.6	3.6	ns
HS6	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-7.6	3.6	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

Table 5-149. Timing Requirements for MMC4 - High Speed Mode [(1)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS3	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.3		ns
HS4	$t_{h(clkH-cmdV)}$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
HS7	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.3		ns
HS8	$t_{h(clkH-dV)}$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

(1) i in [i:0] = 3

Table 5-150. Switching Characteristics for MMC4 - High Speed Mode [(2)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS1	fop(clk)	Operating frequency, mmc4_clk		48	MHz
HS2H	$t_{w(clkH)}$	Pulse duration, mmc4_clk high	0.5P-0.270 [(1)]		ns
HS2L	$t_{w(clkL)}$	Pulse duration, mmc4_clk low	0.5P-0.270 [(1)]		ns
HS5	$t_{d(clkL-cmdV)}$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-8.8	6.6	ns
HS6	$t_{d(clkL-dV)}$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-8.8	6.6	ns

(1) P = output mmc4_clk period in ns

(2) i in [i:0] = 3

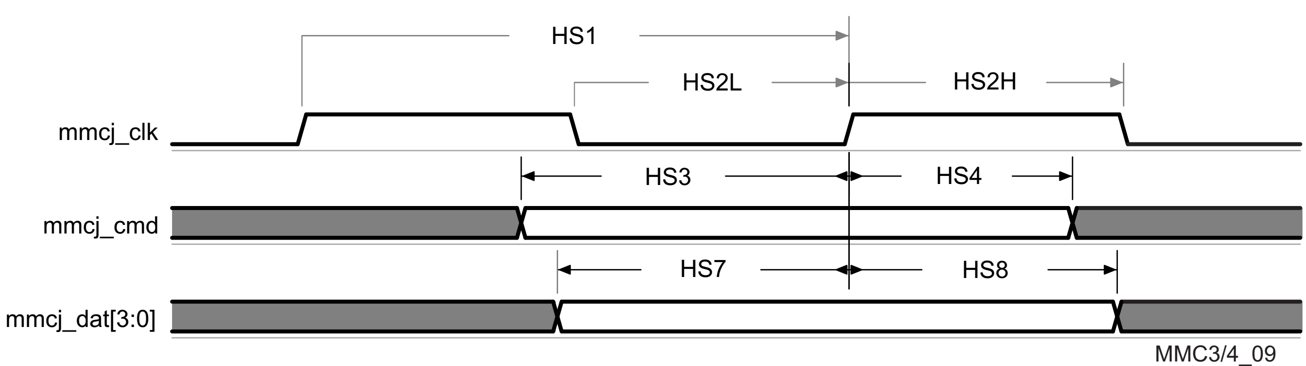


Figure 5-98. MMC/SD/SDIOj in - High Speed - Receiver Mode

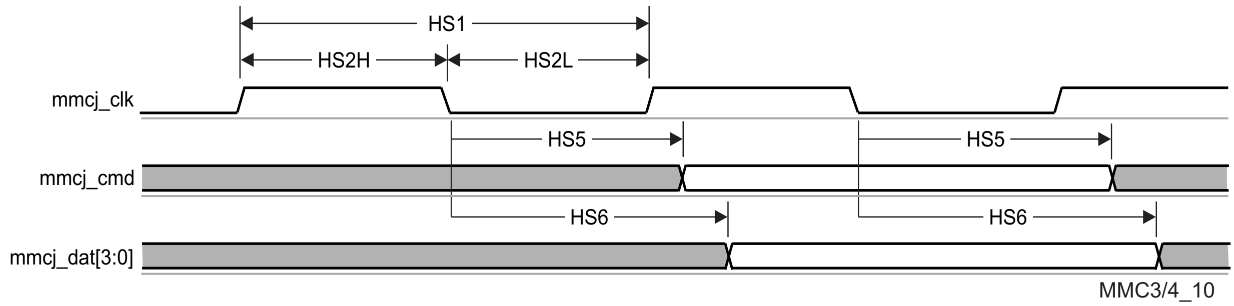


Figure 5-99. MMC/SD/SDIOj in - High Speed - Transmitter Mode

5.10.6.19.3.3 MMC3 and MMC4, SD and SDIO SDR12 Mode

Figure 5-100, Figure 5-101, and Table 5-151, through Table 5-154 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO SDR12 in receiver and transmitter mode.

Table 5-151. Timing Requirements for MMC3 - SDR12 Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	25.99		ns
SDR126	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	25.99		ns
SDR128	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

(1) i in [i:0] = 7

Table 5-152. Switching Characteristics for MMC3 - SDR12 Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	fop(clk)	Operating frequency, mmc3_clk		24	MHz
SDR121	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5P-0.270 (1)		ns
SDR122	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5P-0.270 (1)		ns
SDR123	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-19.13	16.93	ns
SDR124	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-19.13	16.93	ns

(1) P = output mmc3_clk period in ns

(2) i in [i:0] = 7

Table 5-153. Timing Requirements for MMC4 - SDR12 Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	25.99		ns
SDR126	$t_{h(clkH-cmdV)}$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	25.99		ns
SDR128	$t_{h(clkH-dV)}$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

(1) j in [i:0] = 3

Table 5-154. Switching Characteristics for MMC4 - SDR12 Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	fop(clk)	Operating frequency, mmc4_clk		24	MHz
SDR121	$t_{w(clkH)}$	Pulse duration, mmc4_clk high	0.5P-0.270 (1)		ns
SDR122	$t_{w(clkL)}$	Pulse duration, mmc4_clk low	0.5P-0.270 (1)		ns

Table 5-154. Switching Characteristics for MMC4 - SDR12 Mode (2) (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR125	$t_{d(clkL-cmdV)}$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-19.13	16.93	ns
SDR126	$t_{d(clkL-dV)}$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-19.13	16.93	ns

(1) P = output mmc4_clk period in ns
(2) j in [i:0] = 3

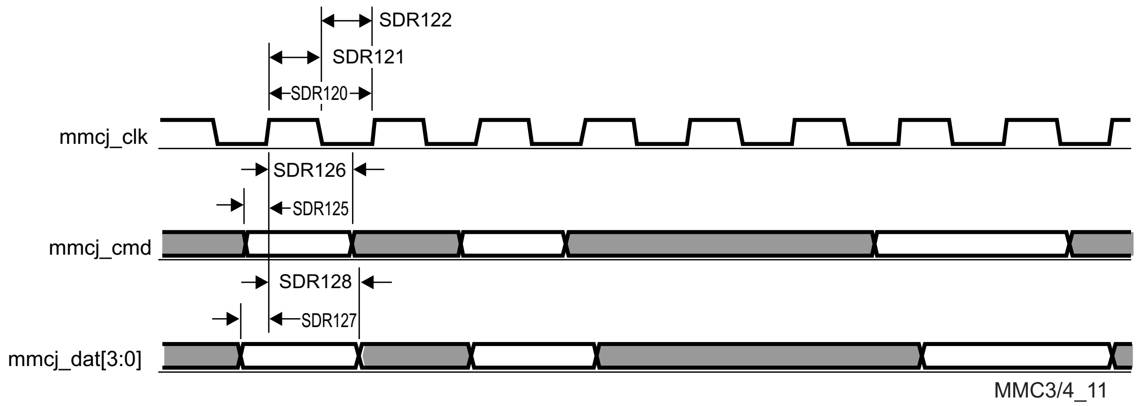


Figure 5-100. MMC/SD/SDIOj in - SDR12 - Receiver Mode

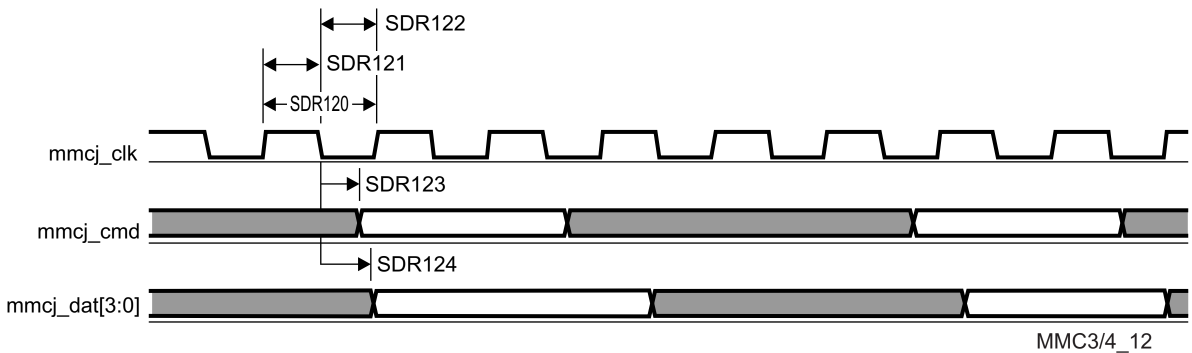


Figure 5-101. MMC/SD/SDIOj in - SDR12 - Transmitter Mode

5.10.6.19.3.4 MMC3 and MMC4, SD SDR25 Mode

Figure 5-102, Figure 5-103, and Table 5-155 through Table 5-158 present Timing requirements and Switching characteristics for MMC3 and MMC4 - SD and SDIO SDR25 in receiver and transmitter mode.

Table 5-155. Timing Requirements for MMC3 - SDR25 Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR253	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	5.3		ns
SDR254	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR257	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	5.3		ns
SDR258	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

(1) i in [i:0] = 7

Table 5-156. Switching Characteristics for MMC3 - SDR25 Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	fop(clk)	Operating frequency, mmc3_clk		48	MHz

Table 5-156. Switching Characteristics for MMC3 - SDR25 Mode [(2)] (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR252H	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5P[(1)]-0.270		ns
SDR252L	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5P[(1)]-0.270		ns
SDR255	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-8.8	6.6	ns
SDR256	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-8.8	6.6	ns

(1) P = output mmc3_clk period in ns
(2) i in [i:0] = 7

Table 5-157. Timing Requirements for MMC4 - SDR25 Mode [(1)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR255	$t_{su(cmdV-clkH)}$	Setup time, mmc4_cmd valid before mmc4_clk rising clock edge	5.3		ns
SDR256	$t_{h(clkH-cmdV)}$	Hold time, mmc4_cmd valid after mmc4_clk rising clock edge	1.6		ns
SDR257	$t_{su(dV-clkH)}$	Setup time, mmc4_dat[i:0] valid before mmc4_clk rising clock edge	5.3		ns
SDR258	$t_{h(clkH-dV)}$	Hold time, mmc4_dat[i:0] valid after mmc4_clk rising clock edge	1.6		ns

(1) i in [i:0] = 3

Table 5-158. Switching Characteristics for MMC4 - SDR25 Mode [(2)]

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	fop(clk)	Operating frequency, mmc4_clk		48	MHz
SDR252H	$t_{w(clkH)}$	Pulse duration, mmc4_clk high	0.5P-0.270 [(1)]		ns
SDR252L	$t_{w(clkL)}$	Pulse duration, mmc4_clk low	0.5P-0.270 [(1)]		ns
SDR255	$t_{d(clkL-cmdV)}$	Delay time, mmc4_clk falling clock edge to mmc4_cmd transition	-8.8	6.6	ns
SDR256	$t_{d(clkL-dV)}$	Delay time, mmc4_clk falling clock edge to mmc4_dat[i:0] transition	-8.8	6.6	ns

(1) P = output mmc4_clk period in ns
(2) i in [i:0] = 3

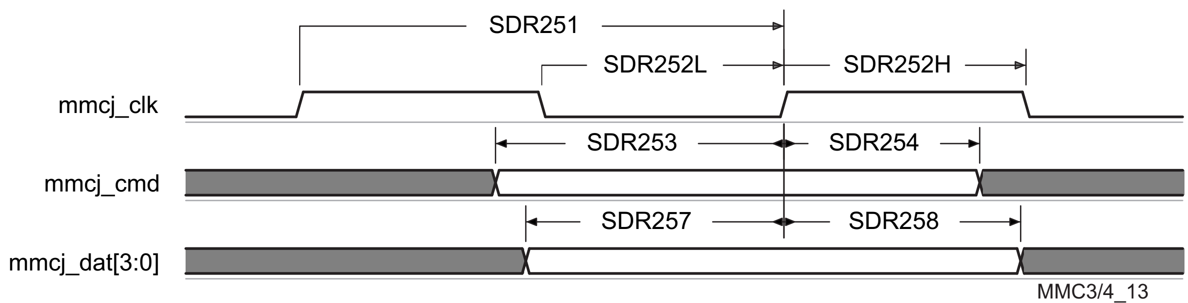


Figure 5-102. MMC/SD/SDIOj in - SDR25 - Receiver Mode

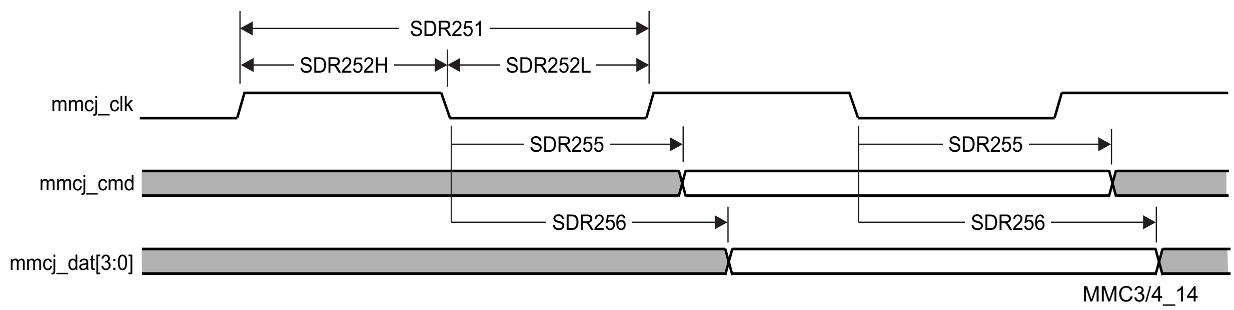


Figure 5-103. MMC/SD/SDIOj in - SDR25 - Transmitter Mode

5.10.6.19.3.5 MMC3 SDIO High-Speed UHS-I SDR50 Mode, Half Cycle

Figure 5-104, Figure 5-105, Table 5-159, and Table 5-160 present Timing requirements and Switching characteristics for MMC3 - SDIO High speed SDR50 in receiver and transmitter mode.

Table 5-159. Timing Requirements for MMC3 - SDR50 Mode (1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR503	$t_{su(cmdV-clkH)}$	Setup time, mmc3_cmd valid before mmc3_clk rising clock edge	1.48		ns
SDR504	$t_{h(clkH-cmdV)}$	Hold time, mmc3_cmd valid after mmc3_clk rising clock edge	1.6		ns
SDR507	$t_{su(dV-clkH)}$	Setup time, mmc3_dat[i:0] valid before mmc3_clk rising clock edge	1.48		ns
SDR508	$t_{h(clkH-dV)}$	Hold time, mmc3_dat[i:0] valid after mmc3_clk rising clock edge	1.6		ns

(1) i in [i:0] = 7

Table 5-160. Switching Characteristics for MMC3 - SDR50 Mode (2)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR501	fop(clk)	Operating frequency, mmc3_clk		96	MHz
SDR502H	$t_{w(clkH)}$	Pulse duration, mmc3_clk high	0.5P-0.270 (1)		ns
SDR502L	$t_{w(clkL)}$	Pulse duration, mmc3_clk low	0.5P-0.270 (1)		ns
SDR505	$t_{d(clkL-cmdV)}$	Delay time, mmc3_clk falling clock edge to mmc3_cmd transition	-3.66	1.46	ns
SDR506	$t_{d(clkL-dV)}$	Delay time, mmc3_clk falling clock edge to mmc3_dat[i:0] transition	-3.66	1.46	ns

(1) P = output mmc3_clk period in ns
(2) i in [i:0] = 7

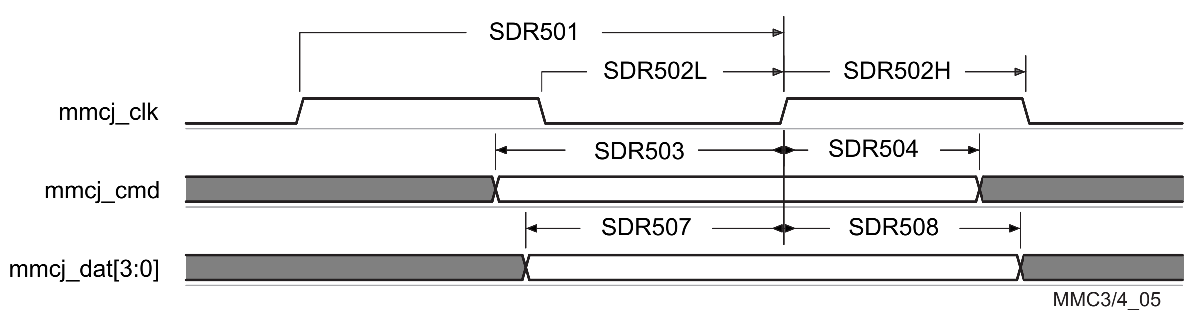


Figure 5-104. MMC/SD/SDIOj in - High Speed SDR50 - Receiver Mode

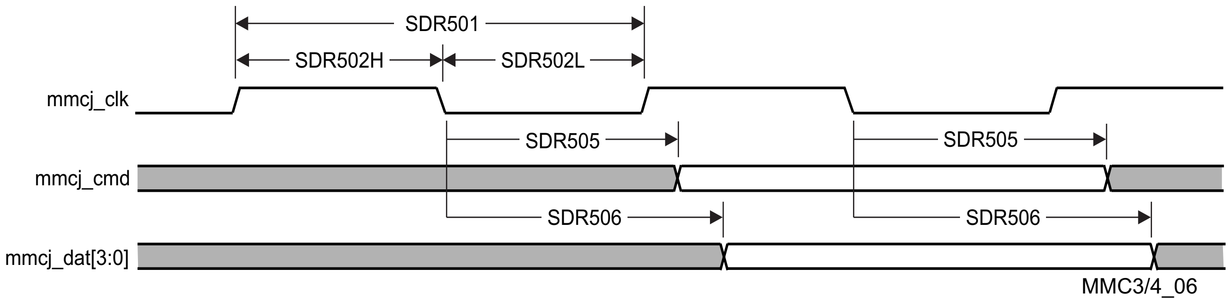


Figure 5-105. MMC/SD/SDIOj in - High Speed SDR50 - Transmitter Mode

NOTE

To configure the desired Manual IO Timing Mode the user must follow the steps described in section Manual IO Timing Modes of the Device TRM.

The associated registers to configure are listed in the **CFG REGISTER** column. For more information see the Control Module chapter in the Device TRM.

Manual IO Timings Modes must be used to guarantee some IO timings for MMC3. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-161, *Manual Functions Mapping for MMC3* for a definition of the Manual modes.

Table 5-161 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-161. Manual Functions Mapping for MMC3

BALL	BALL NAME	MMC3_MANUAL1		MMC3_MANUAL2		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0
AD4	mmc3_clk	0	386	852	0	CFG_MMC3_CLK_IN	mmc3_clk
AD4	mmc3_clk	605	0	94	0	CFG_MMC3_CLK_OUT	mmc3_clk
AC4	mmc3_cmd	0	0	122	0	CFG_MMC3_CMD_IN	mmc3_cmd
AC4	mmc3_cmd	0	0	0	0	CFG_MMC3_CMD_OEN	mmc3_cmd
AC4	mmc3_cmd	0	0	0	0	CFG_MMC3_CMD_OUT	mmc3_cmd
AC7	mmc3_dat0	171	0	91	0	CFG_MMC3_DAT0_IN	mmc3_dat0
AC7	mmc3_dat0	0	0	0	0	CFG_MMC3_DAT0_OEN	mmc3_dat0
AC7	mmc3_dat0	0	0	0	0	CFG_MMC3_DAT0_OUT	mmc3_dat0
AC6	mmc3_dat1	221	0	57	0	CFG_MMC3_DAT1_IN	mmc3_dat1
AC6	mmc3_dat1	0	0	0	0	CFG_MMC3_DAT1_OEN	mmc3_dat1
AC6	mmc3_dat1	0	0	0	0	CFG_MMC3_DAT1_OUT	mmc3_dat1
AC9	mmc3_dat2	0	0	0	0	CFG_MMC3_DAT2_IN	mmc3_dat2
AC9	mmc3_dat2	0	0	0	0	CFG_MMC3_DAT2_OEN	mmc3_dat2
AC9	mmc3_dat2	0	0	0	0	CFG_MMC3_DAT2_OUT	mmc3_dat2
AC3	mmc3_dat3	474	0	375	0	CFG_MMC3_DAT3_IN	mmc3_dat3
AC3	mmc3_dat3	0	0	0	0	CFG_MMC3_DAT3_OEN	mmc3_dat3
AC3	mmc3_dat3	0	0	0	0	CFG_MMC3_DAT3_OUT	mmc3_dat3
AC8	mmc3_dat4	792	0	213	0	CFG_MMC3_DAT4_IN	mmc3_dat4
AC8	mmc3_dat4	0	0	0	0	CFG_MMC3_DAT4_OEN	mmc3_dat4
AC8	mmc3_dat4	0	0	0	0	CFG_MMC3_DAT4_OUT	mmc3_dat4
AD6	mmc3_dat5	782	0	355	0	CFG_MMC3_DAT5_IN	mmc3_dat5
AD6	mmc3_dat5	0	0	0	0	CFG_MMC3_DAT5_OEN	mmc3_dat5
AD6	mmc3_dat5	0	0	0	0	CFG_MMC3_DAT5_OUT	mmc3_dat5

Table 5-161. Manual Functions Mapping for MMC3 (continued)

BALL	BALL NAME	MMC3_MANUAL1		MMC3_MANUAL2		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		0
AB8	mmc3_dat6	942	0	437	0	CFG_MMC3_DAT6_IN	mmc3_dat6
AB8	mmc3_dat6	0	0	0	0	CFG_MMC3_DAT6_OEN	mmc3_dat6
AB8	mmc3_dat6	0	0	0	0	CFG_MMC3_DAT6_OUT	mmc3_dat6
AB5	mmc3_dat7	636	0	224	0	CFG_MMC3_DAT7_IN	mmc3_dat7
AB5	mmc3_dat7	0	0	0	0	CFG_MMC3_DAT7_OEN	mmc3_dat7
AB5	mmc3_dat7	0	0	0	0	CFG_MMC3_DAT7_OUT	mmc3_dat7

Manual IO Timings Modes must be used to guarantee some IO timings for MMC4. See Table 5-32, *Modes Summary* for a list of IO timings requiring the use of Manual IO Timings Modes. See Table 5-162, *Manual Functions Mapping for MMC4* for a definition of the Manual modes.

Table 5-162 lists the A_DELAY and G_DELAY values needed to calculate the correct values to be set in the CFG_x registers.

Table 5-162. Manual Functions Mapping for MMC4

BALL	BALL NAME	MMC4_MANUAL1		MMC4_DS_MANUAL1		CFG REGISTER	MUXMODE
		A_DELAY (ps)	G_DELAY (ps)	A_DELAY (ps)	G_DELAY (ps)		3
E25	uart1_ctsn	0	0	0	0	CFG_UART1_CTSN_IN	mmc4_clk
E25	uart1_ctsn	1147	0	0	0	CFG_UART1_CTSN_OUT	mmc4_clk
C27	uart1_rtsn	1834	0	307	0	CFG_UART1_RTSN_IN	mmc4_cmd
C27	uart1_rtsn	0	0	0	0	CFG_UART1_RTSN_OEN	mmc4_cmd
C27	uart1_rtsn	0	0	0	0	CFG_UART1_RTSN_OUT	mmc4_cmd
D27	uart2_ctsn	2165	0	785	0	CFG_UART2_CTSN_IN	mmc4_dat2
D27	uart2_ctsn	0	0	0	0	CFG_UART2_CTSN_OEN	mmc4_dat2
D27	uart2_ctsn	0	0	0	0	CFG_UART2_CTSN_OUT	mmc4_dat2
C28	uart2_rtsn	1929	64	613	0	CFG_UART2_RTSN_IN	mmc4_dat3
C28	uart2_rtsn	0	0	0	0	CFG_UART2_RTSN_OEN	mmc4_dat3
C28	uart2_rtsn	0	0	0	0	CFG_UART2_RTSN_OUT	mmc4_dat3
D28	uart2_rxd	1935	128	683	0	CFG_UART2_RXD_IN	mmc4_dat0
D28	uart2_rxd	0	0	0	0	CFG_UART2_RXD_OEN	mmc4_dat0
D28	uart2_rxd	0	0	0	0	CFG_UART2_RXD_OUT	mmc4_dat0
D26	uart2_txd	2172	44	835	0	CFG_UART2_TXD_IN	mmc4_dat1
D26	uart2_txd	0	0	0	0	CFG_UART2_TXD_OEN	mmc4_dat1
D26	uart2_txd	0	0	0	0	CFG_UART2_TXD_OUT	mmc4_dat1

5.10.6.20 GPIO

The general-purpose interface combines eight general-purpose input/output (GPIO) banks. Each GPIO module provides 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 247 pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations
- Wake-up request generation in idle mode upon the detection of external events

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NOTE

For more information, see the General-Purpose Interface chapter of the Device TRM.

NOTE

The general-purpose input/output i (i = 1 to 8) bank is also referred to as GPIOi.

5.10.6.21 System and Miscellaneous interfaces

The Device includes the following System and Miscellaneous interfaces:

- Sysboot Interface
- Enhanced DMA Interface
- Interrupt Controllers (INTC) Interface
- Observability Signal (OBS) Interface

5.10.7 Emulation and Debug Subsystem

The Device includes the following test interfaces:

- IEEE 1149.1 Standard-Test-Access Port (JTAG)
- Trace Port Interface Unit (TPIU)
- Advanced Event Triggering Interface (AET)

5.10.7.1 JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture) interface is used for BSDL testing and emulation of the device. The trstn pin only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. For maximum reliability, the device includes an Internal Pulldown (IPD) on the trstn pin to ensure that trstn is always asserted upon power up and the device's internal emulation logic is always properly initialized. JTAG controllers from Texas Instruments actively drive trstn high. However, some third-party JTAG controllers may not drive trstn high but expect the use of a Pullup resistor on trstn. When using this type of JTAG controller, assert trstn to initialize the device after powerup and externally drive trstn high before attempting any emulation or boundary-scan operations.

The main JTAG features include:

- 32 KB embedded trace buffer (ETB)
- 5-pin system trace interface for debug
- Supports Advanced Event Triggering (AET)
- All processors can be emulated via JTAG ports
- All functions on EMU pins of the device:
  - EMU[1:0] - cross-triggering, boot mode (WIR), STM trace
  - EMU[4:2] - STM trace only (single direction)

5.10.7.1.1 JTAG Electrical Data/Timing

Table 5-163, Table 5-164 and Figure 5-106 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-163. Timing Requirements for IEEE 1149.1 JTAG

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time, TCK	62.29		ns
J1H	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	24.92		ns
J1L	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	24.92		ns

Table 5-163. Timing Requirements for IEEE 1149.1 JTAG (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J3	$t_{su(TDI-TCK)}$	Input setup time, TDI valid to TCK high	6.23		ns
	$t_{su(TMS-TCK)}$	Input setup time, TMS valid to TCK high	6.23		ns
J4	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	31.15		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	31.15		ns

Table 5-164. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	30.5	ns

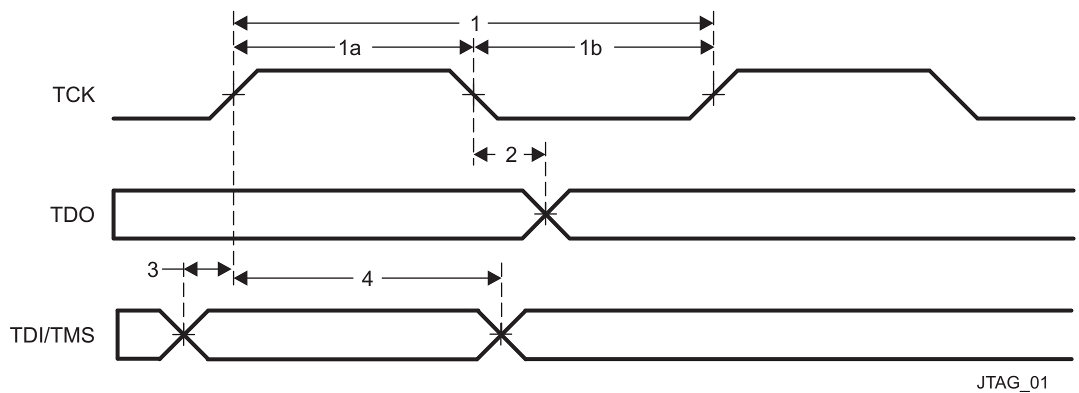

Figure 5-106. JTAG Timing

Table 5-165, Table 5-166 and Figure 5-107 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-165. Timing Requirements for IEEE 1149.1 JTAG With RTCK

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
JR1	$t_{c(TCK)}$	Cycle time, TCK	62.29		ns
JR1H	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	24.92		ns
JR1L	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	24.92		ns
JR3	$t_{su(TDI-TCK)}$	Input setup time, TDI valid to TCK high	6.23		ns
	$t_{su(TMS-TCK)}$	Input setup time, TMS valid to TCK high	6.23		ns
JR4	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	31.15		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	31.15		ns

Table 5-166. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG With RTCK

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
JR5	$t_{d(TCK-RTCK)}$	Delay time, TCK to RTCK with no selected subpaths (i.e. ICEPick is the only tap selected - when the Arm is in the scan chain, the delay time is a function of the Arm functional clock).	0	27	ns
JR6	$t_{c(RTCK)}$	Cycle time, RTCK	62.29		ns
JR7	$t_{w(RTCKH)}$	Pulse duration, RTCK high (40% of t_c)	24.92		ns
JR8	$t_{w(RTCKL)}$	Pulse duration, RTCK low (40% of t_c)	24.92		ns

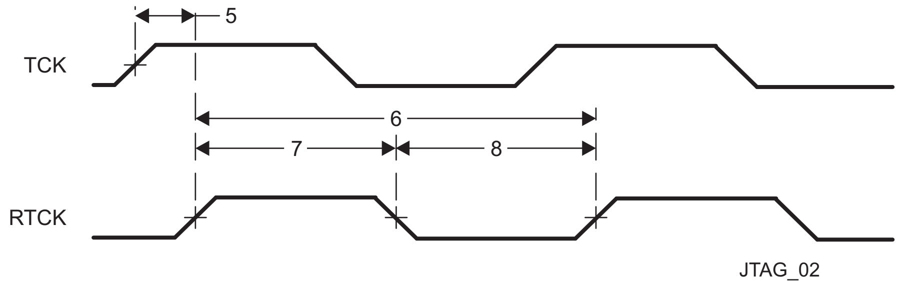

Figure 5-107. JTAG With RTCK Timing

5.10.7.2 Trace Port Interface Unit (TPIU)

CAUTION

The I/O timings provided in this section are valid only if signals within a single IOSET are used. The IOSETs are defined in Table 5-168.

5.10.7.2.1 TPIU PLL DDR Mode

Table 5-167 and Figure 5-108 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-167. Switching Characteristics for TPIU

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
TPIU1	$t_{c(clk)}$	Cycle time, TRACECLK period	5.56		ns
TPIU4	$t_{d(clk-ctlV)}$	Skew time, TRACECLK transition to TRACECTL transition	-0.96	0.96	ns
TPIU5	$t_{d(clk-dataV)}$	Skew time, TRACECLK transition to TRACEDATA[17:0]	-0.96	0.96	ns

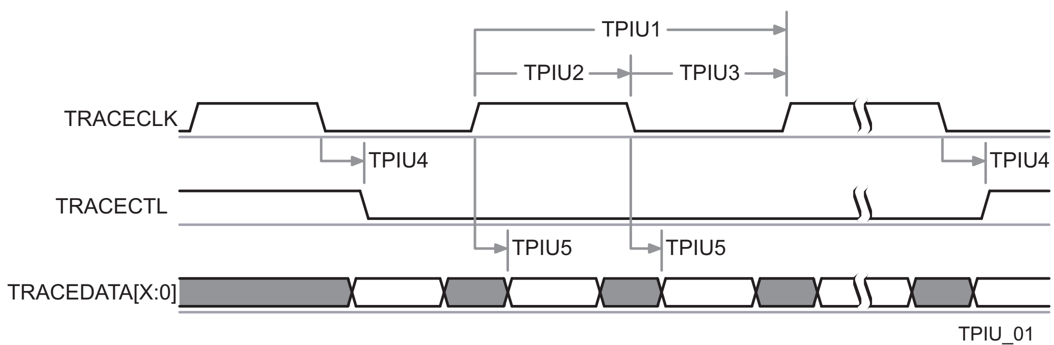

Figure 5-108. TPIU—PLL DDR Transmit Mode(1)

(1) In d[X:0], X is equal to 15 or 17.

In Table 5-168 are presented the specific groupings of signals (IOSET) for use with TPIU signals.

Table 5-168. TPIU IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
emu0	G21	0	G21	0
emu1	D24	0	D24	0
emu2	F10	2	F10	2

Table 5-168. TPIU IOSETs (continued)

SIGNALS	IOSET1		IOSET2	
	BALL	MUX	BALL	MUX
emu3	D7	2	D7	2
emu4	A7	2	A7	2
emu5	E1	5	G11	2
emu6	G2	5	E9	2
emu7	H7	5	F9	2
emu8	G1	5	F8	2
emu9	G6	5	E7	2
emu10	F2	5	D8	2
emu11	F3	5	A5	2
emu12	D1	5	C6	2
emu13	E2	5	C8	2
emu14	D2	5	C7	2
emu15	F4	5	A8	2
emu16	C1	5	C9	2
emu17	E4	5	A9	2
emu18	F5	5	B9	2
emu19	E6	5	A10	2

6 Detailed Description

6.1 Description

TI's new TDA2Px System-on-Chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS). The TDA2Px family enables broad ADAS applications in automobiles by integrating an optimal mix of performance, low power and ADAS vision analytics processing that aims to facilitate a more autonomous and collision-free driving experience.

The TDA2Px SoC enables sophisticated embedded vision technology in automobiles by broadest range of ADAS applications including front camera, park assist, surround view and sensor fusion on a single architecture.

The TDA2Px SoC incorporates a heterogeneous, scalable architecture that includes a mix of TI's fixed and floating-point TMS320C66x digital signal processor (DSP) generation cores, Vision AccelerationPac, Arm Cortex-A15 MPCore and dual-Cortex-M4 processors. The integration of a video accelerator for decoding multiple video streams over an Ethernet AVB network, along with graphics accelerators for rendering virtual views, enable a 3D viewing experience. And the TDA2Px SoC also integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and GigB Ethernet AVB.

The Vision AccelerationPac for this family of products includes multiple embedded vision engines (EVEs) offloading the vision analytics functionality from the application processor while also reducing the power footprint. The Vision AccelerationPac is optimized for vision processing with a 32-bit RISC core for efficient program execution and a vector coprocessor for specialized vision processing.

Additionally, TI provides a complete set of development tools for the Arm, DSP, and EVE coprocessor, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

Cryptographic acceleration is available in all devices. All other supported security features, including support for secure boot, debug security and support for trusted execution environment are available on High-Security (HS) devices. For more information about HS devices, contact your TI representative.

The TDA2Px ADAS processor is qualified according to the AEC-Q100 standard.

6.2 Functional Block Diagram

Figure 6-1 is functional block diagram for the device.

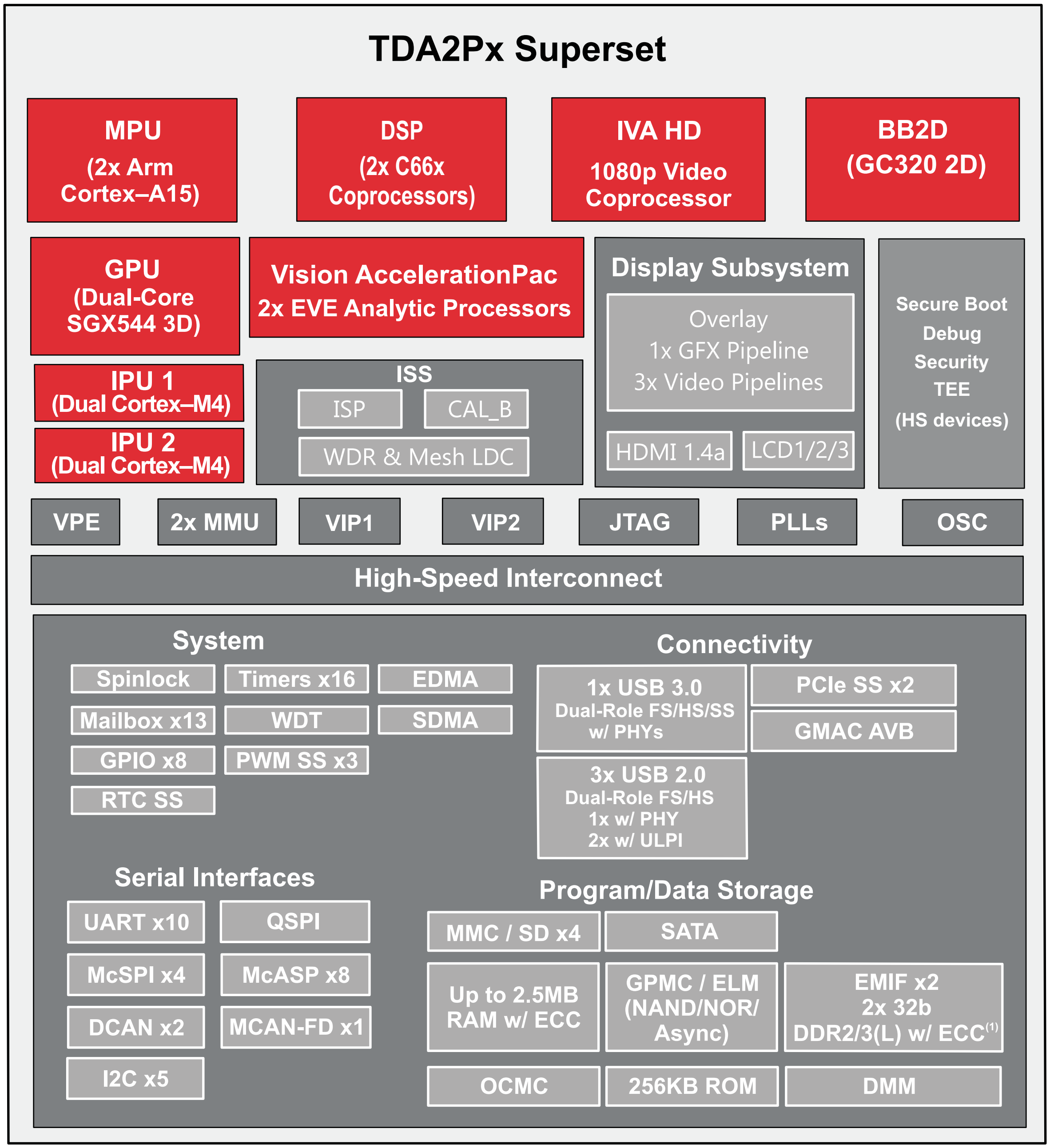

Figure 6-1. TDA2Px Block Diagram

(1) ECC is only available on EMIF1.

6.3 MPU

The dual Cortex®-A15 microprocessor unit (MPU) subsystem serves the applications processing role by running the high-level operating system (HLOS) and application code.

The MPU subsystem incorporates two Cortex-A15 MPU cores (MPU_C0 and MPU_C1), individual level 1 (L1) caches, level 2 (L2) cache (MPU_L2CACHE) shared between them, and various other shared peripherals. To aid software development, the processor cores can be kept cache-coherent with each other and with the L2 cache.

The MPU subsystem provides a high-performance computing platform with high peak-computing performance and low memory latency.

The MPU subsystem integrates the following:

- Arm Cortex-A15 MP Core (MPU_CLUSTER)
  - Two Cortex-A15 MPU cores (revision r2p2, SMP architecture), each of them having the following features:
    - Superscalar, dynamic multi-issue technology
      - Out-of-order (OoO) instruction dispatch and completion
      - Dynamic branch prediction with branch target buffer (BTB), global history buffer (GHB), and 48-entry return stack
      - Continuous fetch and decoding of three instructions per clock cycle
      - Dispatch of up to four instructions and completion of eight instructions per clock cycle
      - Provides optimal performance from binaries compiled for previous Arm processors
      - Five execution units handle simple instructions, branch instructions, Neon™ and floating point instructions, multiply instructions, and load and store instructions.
      - Simple instructions take two cycles from dispatch, while complex instructions take up to 11 cycles.
      - Can issue two simple instructions in a cycle
      - Can issue a load and a store instruction in the same cycle
    - Integrated Neon processing engine to include the Arm Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
    - Includes VFPv4-compatible hardware to support single- and double-precision add, subtract, divide, multiply and accumulate, and square root operations
    - Extensive support to accelerate virtualization using a hypervisor
    - 32-KiB L1 instruction (L1I) and 32-KiB L1 data (L1D) cache:
      - 64-byte line size
      - 2-way set associative
    - Memory management unit (MMU):
      - Two-level translation lookaside buffer (TLB) organization
        - First level is an 32-entry, fully associative micro-TLB implemented for each of instruction fetch, load, and store.
        - Second level is a unified, 4-way associative, 512-entry main TLB
      - Supports hardware TLB table-walk for backward-compatible and new 64-bit entry page table formats
      - New page table format can produce 40-bit physical addresses
      - Two-stage translation where first stage is HLOS-controlled and the second level may be controlled by a hypervisor. Second stage always uses the new page table format
  - Integrated L2 cache (MPU_L2CACHE) and snoop control unit (SCU):
    - 2-MiB of unified (instructions and data) cache organized as 16 ways of 2048 sets of 64-byte lines
    - Redundant L1 data (cache) tags to perform snoop filtering (L1 instruction cache tags are not duplicated)
    - Operates at Cortex-A15 MPU core clock rate
    - Integrated L2 cache controller (MPU_L2CACHE_CTRL):
      - Sixteen 64-byte line buffers that handle evictions, line fills and snoop transfers
      - One 128-bit AMBA4 Coherent Bus (AXI4-ACE) port
      - Auto-prefetch buffer for up to 16 streams per core and detecting forward and backward strides
  - Generalized interrupt controller (GIC, also referred to as MPU_INTC): An interrupt controller supplied by Arm. The single GIC in the MPU_CLUSTER routes interrupts to each of the MPU cores. The GIC supports:
    - Number of shared peripheral interrupts (SPI): 160

    - Number of software generated interrupts (SGI): 16
    - Number of CPU interfaces: 2
    - Virtual CPU interface for virtualization support. This allows the majority of guest operating system (OS) interactions with the GIC to be handled in hardware, but with physical interrupts still requiring hypervisor intervention to assign them to the appropriate virtual machine.
  - Integrated timer counter and one timer block per MPU core
  - Arm CoreSight™ debug and trace modules. For more information, see chapter On-Chip Debug Support of the Device TRM.
- MPU_AXI2OCP bridge (local interconnect):
  - Connected to Memory Adapter (MPU_MA), which routes the non-EMIF address space transactions to MPU_AXI2OCP
  - Single request multiple data (SRMD) protocol on L3_MAIN port
  - Multiple targets:
    - 64-bit port to the L3_MAIN interconnect. Interface frequency is 1/4 or 1/8 of core frequency
    - MPU_ROM
    - Internal MPU subsystem peripheral targets, including Memory Adapter LISA Section Manager (MA_LSM), wake-up generator (MPU_WUGEN), watchdog timer (MPU_WD_TIMER), and local PRCM module (MPU_PRCM) configuration
    - Internal AXI target, CoreSight System Trace Module (CS_STM)
- Memory adapter (MPU_MA): Helps decrease the latency of accesses between the MPU_L2CACHE and the two EMIFs (EMIF0 and EMIF1) by providing a direct path between the MPU subsystem and the EMIFs:
  - Connected to 128-bit AMBA4 interface of MPU_CLUSTER
  - Direct 128-bit interface to each of EMIF0 and EMIF1
  - Interface speed between MPU_CLUSTER and MPU_MA is at half-speed of MPU_CLUSTER internal core frequency
  - Quarter-speed interface to EMIF
  - Uses firewall logic to check access rights of incoming addressess
- Local PRCM (MPU_PRCM):
  - Handles MPU_C0 and MPU_C1 power domains
  - Supports SR3-APG (SmartReflex3 Automatic Power Gating) power management technology inside the MPU_CLUSTER
  - MPU subsystem has six power domains
- Wake-up generator (MPU_WUGEN)
  - Responsible for waking up the MPU cores
- Standby controller: Handles the power transitions inside the MPU subsystem
- Realtime (master) counter (COUNTER_REALTIME): Produces the count used by the private timer peripherals in the MPU_CLUSTER
- Watchdog timer (MPU_WD_TIMER): Used to generate a chip-level watchdog reset request to global PRCM
- On-chip boot ROM (MPU_ROM): The MPU_ROM size is 48-KiB, and the address range is from 0x4003 8000 to 0x4004 3FFF. For more information about booting from this memory, see chapter *Initialization* of the Device TRM.

- Interfaces:
  – 128-bit interface to each of EMIF0 and EMIF1
  – 64-bit master port to the L3_MAIN interconnect
  – 32-bit slave port from the L4_CFG_EMU interconnect (debug subsystem) for configuration of the MPU subsystem debug modules
  – 32-bit slave port from the L4_CFG interconnect for memory adapter firewall (MPU_MA_NTTP_FW) configuration
  – 32-bit ATB output for transmitting debug and trace data
  – 160 peripheral interrupt inputs

For more information, see chapter *Dual Cortex-A15 MPU Subsystem* of the Device TRM.

6.4 DSP Subsystem

The device includes two identical instances (DSP1 and DSP2) of a digital signal processor (DSP) subsystem, based on the TI's standard TMS320C66x™ DSP CorePac core.

The TMS320C66x DSP core enhances the TMS320C674x™ core, which merges the C674x™ floating point and the C64x+™ fixed-point instruction set architectures. The C66x DSP is object-code compatible with the C64x+/C674x DSPs.

For more information on the TMS320C66x core CPU, see the *TMS320C66x DSP CPU and Instruction Set Reference Guide* (SPRUGH7).

The DSP subsystem integrated in the device includes the following components:

- A TMS320C66x™ CorePac DSP core that encompasses:
  – L1 program-dedicated (L1P) cacheable memory
  – L1 data-dedicated (L1D) cacheable memory
  – L2 (program and data) cacheable memory
  – Extended Memory Controller (XMC)
  – External Memory Controller (EMC)
  – DSP CorePac located interrupt controller (INTC)
  – DSP CorePac located power-down controller (PDC)
- Dedicated enhanced data memory access engine - EDMA, to transfer data from/to memories and peripherals external to the DSP subsystems and to local DSP memory (most commonly L2 SRAM). The external DMA requests are passed through DSP system level (SYS) wakeup logic, and collected from the DSP1 / DSP2 dedicated outputs of the device DMA Events Crossbar for each of the two subsystems.
- A level 2 (L2) interconnect network (DSP NoC) to allow connectivity between different modules of the subsystem or the remainder of the device via the device L3_MAIN interconnect.
- Two memory management units (on EDMA L2 interconnect and DSP MDMA paths) for accessing the device L3_MAIN interconnect address space
- Dedicated system control logic (DSP_SYSTEM) responsible for power management, clock generation, and connection to the device power, reset, and clock management (PRCM) module

The TMS320C66x Instruction Set Architecture (ISA) is the latest for the C6000 family. As with its predecessors (C64x, C64x+ and C674x), the C66x is an advanced VLIW architecture with 8 functional units (two multiplier units and six arithmetic logic units) that operate in parallel. The C66x CPU has a total of 64 general-purpose 32-bit registers.

Some features of the DSP C6000 family devices are:

- Advanced VLIW CPU with eight functional units (two multipliers and six ALUs) which:
  – Executes up to eight instructions per cycle for up to ten times the performance of typical DSPs
  – Allows designers to develop highly effective RISC-like code for fast development time

- Instruction packing
  - Gives code size equivalence for eight instructions executed serially or in parallel
  - Reduces code size, program fetches, and power consumption
- Conditional execution of most instructions
  - Reduces costly branching
  - Increases parallelism for higher sustained performance
- Efficient code execution on independent functional units
  - Industry's most efficient C compiler on DSP benchmark suite
  - Industry's first assembly optimizer for fast development and improved parallelization
- 8-/16-/32-bit/64-bit data support, providing efficient memory support for a variety of applications
- 40-bit arithmetic options which add extra precision for vocoders and other computationally intensive applications
- Saturation and normalization to provide support for key arithmetic operations
- Field manipulation and instruction extract, set, clear, and bit counting support common operation found in control and data manipulation applications.

The C66x CPU has the following additional features:

- Each multiplier can perform two 16 × 16-bit or four 8 × 8 bit multiplies every clock cycle.
- Quad 8-bit and dual 16-bit instruction set extensions with data flow support
- Support for non-aligned 32-bit (word) and 64-bit (double word) memory accesses
- Special communication-specific instructions have been added to address common operations in error-correcting codes.
- Bit count and rotate hardware extends support for bit-level algorithms.
- Compact instructions: Common instructions (AND, ADD, LD, MPY) have 16-bit versions to reduce code size.
- Protected mode operation: A two-level system of privileged program execution to support higher-capability operating systems and system features such as memory protection.
- Exceptions support for error detection and program redirection to provide robust code execution
- Hardware support for modulo loop operation to reduce code size and allow interrupts during fully-pipelined code
- Each multiplier can perform 32 × 32 bit multiplies
- Additional instructions to support complex multiplies allowing up to eight 16-bit multiply/add/subtracts per clock cycle

The TMS320C66x has the following key improvements to the ISA:

- 4x Multiply Accumulate improvement for both fixed and floating point
- Improvement of the floating point arithmetic
- Enhancement of the vector processing capability for fixed and floating point
- Addition of domain-specific instructions for complex arithmetic and matrix operations

On the C66x ISA, the vector processing capability is improved by extending the width of the SIMD instructions. The C674x DSP supports 2-way SIMD operations for 16-bit data and 4-way SIMD operations for 8-bit data. C66x enhances this capabilities with the addition of SIMD instructions for 32-bit data allowing operation on 128-bit vectors. For example the QMPY32 instruction is able to perform the element to element multiplication between two vectors of four 32-bit data each.

C66x ISA includes a set of specific instructions to handle complex arithmetic and matrix operations.

- **TMS320C66x DSP CorePac memory components:**
  - A 32-KiB L1 program memory (L1P) configurable as cache and/or SRAM:
    - When configured as a cache, the L1P is a 1-way set-associative cache with a 32-byte cache line
    - The DSP CorePac L1P memory controller provides bandwidth management, memory protection, and power-down functions
    - The L1P is capable of cache block and global coherence operations
    - The L1P controller has an Error Detection (ED) mechanism, including necessary SRAM
    - The L1P memory can be fully configured as a cache or SRAM
    - Page size for L1P memory is 2KB
  - A 32-KiB L1 data memory (L1D) with ECC, configurable as cache and / or SRAM:
    - When configured as a cache, the L1D is a 2-way set-associative cache with a 64-byte cache line
    - The DSP CorePac L1D memory controller provides bandwidth management, memory protection, and power-down functions
    - The L1D memory can be fully configured as a cache or SRAM
    - No support for error correction or detection
    - Page size for L1D memory is 2KB
  - A 288-KiB (program and data) L2 memory, only part of which is cacheable:
    - When configured as a cache, the L2 memory is a 4-way set associative cache with a 128-byte cache line
    - Only 256 KiB of L2 memory can be configured as cache or SRAM
    - 32 KiB of the L2 memory is always mapped as SRAM
    - The L2 memory controller has an Error Correction Code (ECC) and ED mechanism, including necessary SRAM
    - The L2 memory controller supports hardware prefetching and also provides bandwidth management, memory protection, and power-down functions.
    - Page size for L2 memory is 16KB
- The **External Memory Controller (EMC)** is a bridge from the C66x CorePac to the rest of the DSP subsystem and device. It has :
  - a 32-bit configuration port (CFG) providing access to local subsystem resources (like DSP_EDMA, DSP_SYSTEM, and so forth) or to L3_MAIN resources accessible via the CFG address range.
  - a 128-bit slave-DMA port (SDMA) which provides accesses of system masters outside the DSP subsystem to resources inside the DSP subsystem or C66x DSP CorePac memories, i.e. when the DSP subsystem is the slave in a transaction.
- The **Extended Memory Controller (XMC)** processes requests from the L2 Cache Controller (which are a result of CPU instruction fetches, load/store commands, cache operations) to device resources via the C66x DSP CorePac 128-bit master DMA (MDMA) port:
  - Memory protection for addresses outside C66x DSP CorePac generated over device L3_MAIN on the MDMA port
  - Prefetch, multi-in-flight requests
- A DSP local **Interrupt Controller (INTC)** in the DSP C66x CorePac, interfaces the system events to the DSP C66x core CPU interrupt and exceptions inputs. Each DSP subsystem C66x CorePac interrupt controller supports up to 128 system events of which 64 interrupts are external to DSP subsystems, collected from the DSP1 /DSP2 dedicated outputs of the device Interrupt Crossbar.

- **Local Enhanced Direct Memory Access (EDMA) controller features:**
  - Channel controller (CC) : 64-channel, 128 PaRAM, 2 Queues
  - 2 x Third-party Transfer Controllers (TPTC0 and TPTC1):
    - Each TC has a 128-bit read port and a 128-bit write port
    - 2KiB FIFOs on each TPTC
  - 1-dimensional/2-dimensional (1D/2D) addressing
  - Chaining capability
- **DSP subsystem integrated MMUs**:
  - Two MMUs are integrated:
    - The MMU0 is located between DSP MDMA master port and the device L3_MAIN interconnect and can be optionally bypassed
    - The MMU1 is located between the EDMA master port and the device L3_MAIN interconnect
- A DSP local **Power-Down Controller (PDC)** is responsible to power-down various parts of the DSP C66x CorePac, or the entire DSP C66x CorePac.
- The DSP subsystem **System Control logic** provides:
  - Slave idle and master standby protocols with device PRCM for powerdown
  - OCP Disconnect handshake for init and target busses
  - Asynchronous reset
  - Power-down modes:
    - "Clockstop" mode featuring wake-up on interrupt event. The DMA event wake-up is managed in software.
- The device DSP subsystems are supplied by a PRCM DPLL, but each DSP1/2 **has integrated its own PLL module** outside the C66x CorePac for clock gating and division.
- **The device DSP subsystem has following port instances** to connect to remaining part of the device. See also :
  - A 128-bit initiator (DSP MDMA master) port for MDMA/Cache requests
  - A 128-bit initiator (DSP EDMA master) port for EDMA requests
  - A 32-bit initiator (DSP CFG master) port for configuration requests
  - A 128-bit target (DSP slave) port for requests to DSP memories and various peripherals
- **C66x DSP subsystem (DSPSS) safety aspects**:
  - Above mentioned memory ECC/ED mechanisms
  - MMUs enable mapping of only the necessary application space to the processor
  - Memory Protection Units internal to the DSPSS (in L1P, L1D and L2 memory controllers) and external to DSPSS (firewalls) to help define legal accesses and raise exceptions on illegal accesses
  - Exceptions: Memory errors, various DSP errors, MMU errors and some system errors are detected and cause exceptions. The exceptions could be handled by the DSP or by a designated safety processor at the chip level. Note that it may not be possible for the safety processor to completely handle some exceptions

Unsupported features on the C66x DSP core for the device are:

- The Extended Memory Controller MPAX (memory protection and address extension) 36-bit addressing is NOT supported

Known DSP subsystem powermode restrictions for the device are:

- "Full logic / RAM retention" mode featuring wake-up on both interrupt or DMA event (logic in “always on” domain). Only OFF mode is supported by DSP subsystem, **requiring full boot.**

For more information about C66x debug/trace support, see chapter *On-Chip Debug Support* of the Device TRM.

6.5 ISS

The imaging subsystem (ISS) deals with the processing of pixel data coming from external image sensor or data from memory (image format encoding and decoding can be done to and from memory). ISS is tightly coupled with a low-interrupt latency microprocessor subsystem (Cortex-M4 IPU), which runs a real-time operating system (OS) to reach optimal performance, and can quickly change the ISS configuration during frame blanking periods and run some sequencing tasks.

ISS is a key component for Rear View Camera, Front View Stereo Camera, and Surround View Camera applications.

ISS targets the following major use cases:

- Video / Preview
  - Up to 1080p60
  - Up to 2x 1080p30
- Stereo Video / Preview
  - Up to 2x 1080p30
- Multi-camera use cases, with capabilty of up to 4 simultaneous cameras (ISP is time shared)

ISS offers the following main features:

- ISS interfaces:
  - One Camera Adapter Layer (CAL) module supporting DMA function for data read from system memory
  - 128-bit data interface to L3_MAIN system interconnect
- Image Signal Processor (ISP):
  - Memory-to-memory processing
  - Up to 532 MPix/s throughput
  - Statistic data collection
  - Image pipe interface (IPIPEIF) front-end RAW data processing
  - IPIPE back-end RGB and YUV data processing
  - High-ISO video noise filtering (NSF3V)
  - Global and local contrast enhancement accelerator (GLBCE)
  - Two image continuous real-time resizers (RSZ)
  - Chroma noise filter (CNF)
- Still Image Coprocessor (SIMCOP):
  - Memory-to-memory operation
  - Warping accelerator (LDC)
  - Temporal video noise filter (VTNF)
  - Direct memory access (DMA) controller
  - Hardware sequencer
  - Mesh based lens distortion and perspective correction

For more information, see chapter *Imaging Subsystem* of the Device TRM.

6.6 IVA

The IVA supports resolutions up to 1080 p/i with full performance of 60 fps (or 120 fields), achievable for encode or decode only (not for simultaneous encode and decode).

The IVA subsystem is composed of:

- A primary sequencer, including its memories and an imaging controller: ICONT1
- A video direct memory access (VDMA) processor, which can be used as a secondary sequencer: ICONT2

- A VDMA engine: DMA_IVA
- An entropy codec: ECD3
- A motion compensation engine: MC3
- A transform and quantization calculation engine: CALC3
- A loop filter acceleration engine: ILF3
- A motion estimation acceleration engine: IME3
- An intraprediction estimation engine: IPE3
- Shared level 2 (L2) interface and memory
- Local interconnect (L4_IVA)
- A message interface for communication between SYNCBOXes
- Mailbox
- A debug module for trace event and software instrumentation: SMSET

For more information, see chapter *IVA Subsystem* of the Device TRM.

6.7 EVE

The embedded vision engine (EVE) module is a programmable imaging and vision processing engine, intended for use in devices that serve customer electronics imaging and vision applications. Its programmability meets late-in-development or post-silicon processing requirements, and lets third parties or customers add differentiating features in imaging and vision products.

The device includes two instances of the EVE engine. A single EVE module consists of an ARP32 scalar core, a vector coprocessor (VCOP) vector core, and an Enhanced DMA (EDMA3) controller.

The EVE engine includes the following main features:

- Two 128-bit interconnect initiator ports used for:
  - Paging between system-level memory (L3 SRAM/DDR) and EVE memory (primarily IBUF, WBUF)
  - ARP32 program fetches to system memory (through program cache)
  - ARP32 load or store requests to system memory
  - ARP32 program cache-related read requests, including prefetch/preload requests
- 128-bit interconnect target port used for system-level host or DMA access to EVE memory or MMR space
- Scalar core (ARP32) with the following features:
  - 32KB program cache (direct mapped and prefetch)
  - 32KB data memory (DMEM)
- Vector core (VCOP):
  - 32KB working buffer (WBUF)
  - 16KB image buffer low copy A (IBUFLA)
  - 16KB image buffer low copy B (IBUFLB)
  - 16KB image buffer high copy A (IBUFHA)
  - 16KB image buffer high copy B (IBUFHB)
- EDMA channel controller (EDMACC): 128 PaRAM entries, 2 Queues
- EDMA transfer controllers: two instances, 2k FIFO each
- Memory Management Units (MMUs):
  - 32-entry TLB per MMU
  - Page walking with hardware
  - EDMA accesses and ARP32 program or data accesses to system memory space
  - Can limit EVE accesses to desired subset of system addresses
- Configuration interconnect for MMR and debug accesses

- High-performance interconnect for high throughput and high concurrency data transfers between connected endpoints
- Multiple interrupts for interrupt mapping, DMA event mapping, and interprocessor handshaking
- Support for slave idle and master standby protocols for clock gating
- No support for retention and memory array off modes
- Error detection on all memories:
  - Single bit error detect on DMEM, WBUF, IBUFLA, IBUFLB, IBUFHA, and IBUFHB
  - Double bit error detect on program cache
- Invalid instruction detection in the two processor units (ARP32 and VCOP)
- Debug support:
  - Subsystem Counter Timer Module (SCTM) for counting and measuring of VCOP, EVE program cache, and EDMA performance-related state
  - Software Messaging System Event Trace (SMSET) for trace of software messages and hardware events
  - ARP32 debug support: State visibility, breakpoint, run control, cross-triggering
  - VCOP debug support: State visibility and run control
- Interprocessor communication: Internal Mailbox for DSP/EVE communication

For more information, see chapter *Embedded Vision Engine (EVE)* of the Device TRM.

6.8 IPU

Each IPU subsystem contains two Arm® Cortex-M4 processors (IPUx_C0 and IPUx_C1) that share a common level 1 (L1) cache (called unicache [IPUx_UNICACHE]). The two Cortex-M4 cores are completely homogeneous to one another. Any task possible using one Cortex-M4 core is also possible using the other Cortex-M4 core. It is software responsibility to distribute the various tasks between each Cortex-M4 core for optimal performance.

The key features of the IPU subsystem are:

- Two Arm Cortex-M4 microprocessors (IPUx_C0 and IPUx_C1):
  - Armv7-M and Thumb®-2 instruction set architecture (ISA)
  - Armv6 SIMD and digital signal processor (DSP) extensions
  - Single-cycle MAC
  - Integrated nested vector interrupt controller (NVIC) (also called IPUx_Cx_INTC, where x = 0, 1)
  - Integrated bus matrix
  - Registers:
    - Thirteen general-purpose 32-bit registers
    - Link register (LR)
    - Program counter (PC)
    - Program status register, xPSR
    - Two banked SP registers
  - Integrated power management
  - Extensive debug capabilities
- Unicache interface:
  - Instruction and data interface
  - Supports paralleled accesses
- Level 2 (L2) master interface (MIF) splitter for access to memory or configuration port
- Configuration port: Used for unicache maintenance and unicache memory management unit (IPUx_UNICACHE_MMU) configuration

- Unicache:
  - 32 KiB divided into 16 banks
  - 4-way
  - Cache configuration lock/freeze/preload
  - Internal MMU:
    - 16-entry region-based address translation
    - Read/write control and access type control
    - Execute Never (XN) MMU protection policy
    - Little-endian format
- Subsystem counter timer module (IPUx_UNICACHE_SCTM, or just SCTM)
- On-chip ROM (IPUx_ROM) and banked RAM (IPUx_RAM) memory
- Emulation/debug: Emulation feature embedded in Cortex-M4
- L2 MMU (IPUx_MMU): 32 entries with table walking logic
- Wake-up generator (IPUx_WUGEN): Generates wake-up request from external interrupts
- Power management:
  - Local power-management control: Configurable through the IPUx_WUGEN registers.
  - Three sleep modes supported, controlled by the local power-management module.
  - IPUx is clock-gated in all sleep modes.
  - IPUx_Cx_INTC interrupt interface stays awake.

For more information, see chapter *Dual Cortex-M4 IPU Subsystem* of the Device TRM.

6.9 VPE

VPE Features:

- Supports memory to memory operations only.
- VPE consist of a single memory to memory path which can perform the following operations:
  - Read of raster or tiled YUV420 coplanar, YUV422 coplanar or YUV422 interleaved video
  - Deinterlacing of the input video using a 4 field motion based algorithm
  - Scaling of the input video up to 1080p (1920x1080) resolution
  - Write of the resulting video in YUV420 coplanar (raster or tiled), YUV422 coplanar (raster or tiled), YUV422 interleaved (raster or tiled), YUV444 single plane (raster only) or RGB888 (raster only)
  - Deinterlacing up to two 1080i video sources.
  - The single data path performs operations in the following order
    - Chroma Upsampling from 420 to 422 (if needed)
    - Deinterlacing of 422 video from interlaced to progressive (if needed)
    - Scaling of 422 video after deinterlace
    - Conversion of 422 video to 420, 444 or RGB (if needed)
  - VC-1 Range Mapping and Range Reduction support on input video before Chroma Upsampling (if needed)
- Chroma Upsampling Features
  - 4 line Catmull-Rom based implementation
  - Programmable coefficients for interlaced or progressive conversion. Separate coefficients can be provided for top and bottom fields

- Deinterlacer Features
  - 8-bit, YCbCr 4:2:2
  - Motion-adaptive deinterlacing (MDT)
    - Motion detection is based on Luma only
    - 4-field data is used
    - Motion values adaptive to the frequency of luma texture
  - Edge-Directed Interpolation (EDI)
    - Edge detection using luma pixels in a 2x7 window
    - Seven edge vectors: -1.5, -1, -0.5, 0, 0.5, 1, 1.5
    - Edge-directed chroma interpolation
    - Soft-switch between edge directed interpolation and vertical interpolation depending on the confidence factor
  - Film Mode Detection (FMD
    - 3-2 pull down detection
    - 2-2 pull down detection
    - Hysteresis controls how fast FMD can enter/exit film mode (software function)
    - Bad Edit Detection (BED)
  - Progessive Inpu
    - For Progressive Input, the module passes input to output. No internal processing is performed. This is essentially a bypass mode
  - Interlace Bypass
    - For Interlace Input, the module can pass the inputs data directly to the outputs in a bypass configuration. No internal processing is performed
- Scaler Features
  - Vertical and horizontal up/down scaling
    - Polyphase filter upscaling
  - Running average vertical down scaling for memory optimization
  - Decimation and polyphase filtering for horizontal scaling
  - Non-linear scaling for stretched/compressed left and right sides
  - Input image trimmer for pan/scan support
  - Pre-scaling peaking filter for enhanced sharpness
  - Scale field as frame
  - Interlacing of scaled output
  - Full 1080p input and output support
  - YCbCr422 input and output
  - Minimum horizontal scaling ratio = 1/8x
  - Maximum horizontal scaling ratio – limited by output line buffer (2014 pixels)
  - Scaling filter Coefficient memory download
- Chroma Downsampler Features
  - Simple two-line averager capable of converting from YUV422 to YUV420 space
- 422 to 444 Features
  - Catmull-Rom based filter
  - 4 pixel, fixed coefficient
- Color Space Converter Features
  - Fully programmable 3x3 matrix multiplier with offset control

For more information, see chapter *Video Processing Engine* of the Device TRM.

6.10 GPU

The 3D graphics processing unit (GPU) accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics and compute applications. It is based on the POWERVR® SGX544-MP2 core from Imagination Technologies. The SGX544-MP2 core is a multicore (dual-core) evolution of the POWERVR SGX544 GPU.

SGX is a new generation of programmable POWERVR graphics and video IP cores. The POWERVR SGX is a scalable architecture which efficiently processes a number of differing multimedia data types concurrently:

- Pixel Data
- Vertex Data
- General Purpose Processing

The dual core GPU splits geometry and pixel rendering among the cores to improve performance proportional to the number of cores.

GPU Features:

- Multicore GPU architecture:
  - 2 × SGX544 cores
  - Shared system level cache of 128 KiB (64 KiB per SGX-544 core)
- Tile-based deferred rendering architecture:
  - Reduces external bandwidth to SDRAM
- Universal Scalable Shader Engine (USSE™):
  - Multithreaded engine incorporating vertex and pixel shader functionality
  - Automatic load balancing of vertex and pixel processing tasks
- Present and texture load accelerator (PTLA):
  - Enables to move, rotate, twiddle, and scale texture surfaces
  - Supports RGB, ARGB, YUV4:2:2, and YUV4:2:0 surface formats
  - Supports bilinear upscale
  - Supports source color key
- Fully virtualized memory addressing for operating system (OS) in a unified memory architecture:
  - Memory management unit (MMU)
  - Up to 4-GiB virtual address space

For more information, see chapter *3D Graphics Accelerator* of the Device TRM.

6.11 Memory Subsystem

6.11.1 EMIF

The EMIF module provides connectivity between DDR memory types and manages data bus read/write accesses between external memory and device subsystems which have master access to the L3_MAIN interconnect and DMA capability.

The EMIF module has the following capabilities:

- Supports JEDEC standard-compliant DDR3/DDR3L-SDRAM memory types
- 2-GiB SDRAM address range over one chip-select. This range is configurable through the dynamic memory manager (DMM) module
- Supports SDRAM devices with one, two, four or eight internal banks
- Supports SDRAM devices with single or dual die packages
- Data bus widths:
  - 128-bit L3_MAIN (system) interconnect data bus width
  - 128-bit port for direct connection with MPU subsystem
  - 32-bit SDRAM data bus width
  - 16-bit SDRAM data bus width used in narrow mode
- Supported CAS latencies:
  - DDR3: 5, 6, 7, 8, 9, 10 and 11
- Supports 256-, 512-, 1024-, and 2048-word page sizes
- Supported burst length: 8
- Supports sequential burst type
- SDRAM auto initialization from reset or configuration change
- Supports self refresh and power-down modes for low power
- Partial array self-refresh mode for low power.
- Output impedance (ZQ) calibration for DDR3
- Supports on-die termination (ODT) DDR3
- Supports prioritized refresh
- Programmable SDRAM refresh rate and backlog counter
- Programmable SDRAM timing parameters
- Write and read leveling/calibration and data eye training for DDR3

The EMIF module does not support:

- Burst chop for DDR3
- Interleave burst type
- Auto precharge because of better Bank Interleaving performance
- DLL disabling from EMIF side
- SDRAM devices with more than one die, or topologies which require more than one chip select on a single EMIF channel

For more information, see section *EMIF Controller* in chapter *Memory Subsystem* of the Device TRM.

6.11.2 GPMC

The General Purpose Memory Controller (GPMC) is an external memory controller of the device. Its data access engine provides a flexible programming model for communication with all standard memories.

The GPMC supports the following various access types:

- Asynchronous read/write access
- Asynchronous read page access (4, 8, and 16 Word16)

- Synchronous read/write access
- Synchronous read/write burst access without wrap capability (4, 8 and 16 Word16)
- Synchronous read/write burst access with wrap capability (4, 8 and 16 Word16)
- Address-data-multiplexed (AD) access
- Address-address-data (AAD) multiplexed access
- Little- and big-endian access

The GPMC can communicate with a wide range of external devices:

- External asynchronous or synchronous 8-bit wide memory or device (non burst device)
- External asynchronous or synchronous 16-bit wide memory or device
- External 16-bit non-multiplexed NOR flash device
- External 16-bit address and data multiplexed NOR Flash device
- External 8-bit and 16-bit NAND flash device
- External 16-bit pseudo-SRAM (pSRAM) device

The main features of the GPMC are:

- 8- or 16-bit-wide data path to external memory device
- Supports up to eight CS regions of programmable size and programmable base addresses in a total address space of 1 GiB
- Supports transactions controlled by a firewall
- On-the-fly error code detection using the Bose-ChaudhurI-Hocquenghem (BCH) (t = 4, 8, or 16) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)
- Fully pipelined operation for optimal memory bandwidth use
- The clock to the external memory is provided from GPMC functional clock divided by 1, 2, 3, or 4
- Supports programmable autoclock gating when no access is detected
- Independent and programmable control signal timing parameters for setup and hold time on a per-chip basis. Parameters are set according to the memory device timing parameters, with a timing granularity of one GPMC functional clock cycle.
- Flexible internal access time control (WAIT state) and flexible handshake mode using external WAIT pin monitoring
- Support bus keeping
- Support bus turnaround
- Prefetch and write posting engine associated with to achieve full performance from the NAND device with minimum effect on NOR/SRAM concurrent access

For more information, see section *General-Purpose Memory Controller* in chapter *Memory Subsystem* of the Device TRM.

6.11.3 ELM

In the case of NAND modules with no internal correction capability, sometimes referred to as bare NAND, the correction process can be delegated to the error location module (ELM) used in conjunction with the GPMC.

The ELM supports the following features:

- 4, 8, and 16 bits per 512-byte block error location based on BCH algorithm
- Eight simultaneous processing contexts
- Page-based and continuous modes

- Interrupt generation when error location process completes:
  - When the full page has been processed in page mode
  - For each syndrome polynomial (checksum-like information) in continuous mode

For more information, see section *Error Location Module* in chapter *Memory Subsystem* of the Device TRM.

6.11.4 OCMC

There is one on-chip memory controller (OCMC) in the device.

The OCM Controller supports the following features:

- L3_MAIN data interface:
  - Used for maximum throughput performance
  - 128-bit data bus width
  - Burst supported
- L4 interface (OCMC_RAM only):
  - Used for access to configuration registers
  - 32-bit data bus width
  - Only single accesses supported
  - The L4 associated OCMC clock is two times lower than the L3 associated OCMC clock
- Error correction and detection:
  - Single error correction and dual error detection
  - 9-bit Hamming error correction code (ECC) calculated on 128-bit data word which is concatenated with memory address bits
  - Hamming distance of 4
  - Enable/Disable mode control through a dedicated register
  - Single bit error correction on a read transaction
  - Exclusion of repeated addresses from correctable error address trace history
  - ECC valid for all write transactions to an enabled region
  - Sub-128-bit writes supported via read modify write
- ECC Error Status Reporting:
  - Trace history buffer (FIFO) with depth of 4 for corrected error address
  - Trace history buffer with depth of 4 for non correctable error address and also including double error detection
  - Interrupt generation for correctable and uncorrectable detected errors
- ECC Diagnostics Configuration:
  - Counters for single error correction (SEC), double error detection (DED) and address error events (AEE)
  - Programmable threshold registers for exeptions associated with SEC, DED and AEE counters
  - Register control for enabling and disabling of diagnostics
  - Configuration registers and ECC status accessible through L4 interconnect
- Circular buffer for sliced based VIP frame transfers:
  - Up to 12 programmable circular buffers mapped with unique virtual frame addresses
  - On the fly (with no additional latency) address translation from virtual to OCMC circular buffer memory space
  - Virtual frame size up to 8 MiB and circular buffer size up to 1 MiB
  - Error handling and reporting of illegal CBUF addressing
  - Underflow and Overflow status reporting and error handling
  - Last access read/write address history

- Two Interrupt outputs configured independently to service either ECC or CBUF interrupt events

The OCM controller does not have a memory protection logic and does not support endianism conversion.

For more information, see section *On-Chip Memory (OCM) Subsystem* in chapter *Memory Subsystem* of the Device TRM.

6.12 Interprocessor Communication

6.12.1 Mailbox

Communication between the on-chip processors of the device uses a queued mailbox-interrupt mechanism.

The queued mailbox-interrupt mechanism allows the software to establish a communication channel between two processors through a set of registers and associated interrupt signals by sending and receiving messages (mailboxes).

The device implements the following mailbox types:

- System mailbox:
  – Number of instances: 13
  – Used for communication between: MPU, DSP1, IPU1, and IPU2 subsystems
  – Reference name: MAILBOX(1..13)
- IVA mailbox:
  – Number of instances: 1
  – Used for communication between: IVA local user (ICONT1, or ICONT2) and three external users (selected among MPU, DSP1, IPU1, and IPU2 subsystems)
  – Reference name: IVA_MBOX

Each mailbox module supports the following features:

- Parameters configurable at design time
  – Number of users
  – Number of mailbox message queues
  – Number of messages (FIFO depth) for each message queue
- 32-bit message width
- Message reception and queue-not-full notification using interrupts
- Support of 16-/32-bit addressing scheme
- Power management support

For more information, see chapter *Mailbox* of the Device TRM.

6.12.2 Spinlock

The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device:

- Dual Cortex®-A15 microprocessor unit (MPU) subsystem
- Digital signal processor (DSP) subsystems – DSP1 and DSP2
- Dual Cortex-M4 image processing unit (IPU) subsystems – IPU1 and IPU2

  The Spinlock module implements 256 spinlocks (or hardware semaphores), which provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need of a readmodify- write bus transfer that the programmable cores are not capable of.

For more information, see chapter *Spinlock* of the Device TRM.

6.13 Interrupt Controller

The device has a large number of interrupts to service the needs of its many peripherals and subsystems. The MPU, DSP (x2), and IPU (x2) subsystems are capable of servicing these interrupts via their integrated interrupt controllers. In addition, each processor's interrupt controller is preceded by an Interrupt Controller Crossbar (IRQ_CROSSBAR) that provides flexibility in mapping the device interrupts to processor interrupt inputs. For more information about IRQ crossbar, see chapter *Control Module* of the Device TRM.

Dual Cortex®-A15 MPU Subsystem Interrupt Controller (MPU_INTC)

The MPU_INTC module (also called Generalized Interrupt Controller [GIC]) is a single functional unit that is integrated in the Arm® Cortex-A15 multiprocessor core (MPCore) alongside Cortex-A15 processors. It provides:

- 160 hardware interrupt inputs
- Generation of interrupts by software
- Prioritization of interrupts
- Masking of any interrupts
- Distribution of the interrupts to the target Cortex-A15 processor(s)
- Tracking the status of interrupts

Each Cortex-A15 processor supports three main groups of interrupt sources, with each interrupt source having a unique ID:

- *Software Generated Interrupts (SGIs):* SGIs are generated by writing to the Cortex-A15 Software Generated Interrupt Register (GICD_SGIR). A maximum of 16 SGIs (ID0–ID15) can be generated for each CPU interface. An SGI has edge-triggered properties. The software triggering of the interrupt is equivalent to the edge transition of the interrupt signal on a peripheral input.
- *Private Peripheral Interrupts (PPIs):* A PPI is an interrupt generated by a peripheral that is specific to a single processor. Although interrupts ID16–ID31 are dedicated to PPIs in general, only seven PPIs are actually used for each CPU interface (ID25–ID31). Interrupts ID16–ID24 are reserved (not used).
- *Shared Peripheral Interrupts (SPIs):* SPIs are triggered by events generated on associated interrupt input lines. In this device, the GIC is configured to support 160 SPIs corresponding to its external IRQS[159:0] signals.

For detailed information about this module and description of SGIs and PPIs, see the Arm *Cortex-A15 MP Core Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

C66x DSP Subsystem Interrupt Controller (DSPx_INTC, where x = 1, 2)

There are two Digital Signal Processing (DSP) subsystems in the device - DSP1, and DSP2. Each DSP subsystem integrates an interrupt controller - DSPx_INTC, which interfaces the system events to the C66x core interrupt and exceptions inputs. It combines up to 128 interrupts into 12 prioritized interrupts presented to the C66x CPU.

For detailed information about this module, see chapter *DSP Subsystems* of the Device TRM.

Dual Cortex-M4 IPU Subsystem Interrupt Controller (IPUx_Cx_INTC, where x = 1, 2)

There are two Image Processing Unit (IPU) subsystems in the device - IPU1, and IPU2. Each IPU subsystem integrates two Arm Cortex-M4 cores.

A Nested Vectored Interrupt Controller (NVIC) is integrated within each Cortex-M4. The interrupt mapping is the same (per IPU) for the two cores to facilitate parallel processing. The NVIC supports:

- 64 external interrupts (in addition to 16 Cortex-M4 internal interrupts), which are dynamically prioritized with 16 levels of priority defined for each core
- Low-latency exception and interrupt handling
- Prioritization and handling of exceptions
- Control of the local power management
- Debug accesses to the processor core

For detailed information about this module, refer to Arm *Cortex-M4 Technical Reference Manual* (available at infocenter.arm.com/help/index.jsp).

6.14 EDMA

The primary purpose of the Enhanced Direct Memory Access (EDMA) controller is to service user-programmed data transfers between two memory-mapped slave endpoints on the device.

Typical usage of the EDMA controller includes:

- Servicing software-driven paging transfers (for example, data movement between external memory [such as SDRAM] and internal memory [such as DSP L2 SRAM])
- Servicing event-driven peripherals, such as a serial port
- Performing sorting or sub-frame extraction of various data structures
- Offloading data transfers from the main device CPUs, such as the C66x DSP CorePac or the Arm CorePac

The EDMA controller consists of two major principle blocks:

- EDMA Channel Controller
- EDMA Transfer Controller(s)

The EDMA Channel Controller (EDMACC) serves as the user interface for the EDMA controller. The EDMACC includes parameter RAM (PaRAM), channel control registers, and interrupt control registers. The EDMACC serves to prioritize incoming software requests or events from peripherals and submits transfer requests (TR) to the EDMA transfer controller.

The EDMA Transfer Controller (EDMATC) is responsible for data movement. The transfer request packets (TRP) submitted by the EDMACC contain the transfer context, based on which the transfer controller issues read/write commands to the source and destination addresses programmed for a given transfer.

There are two EDMA controllers present on this device:

- EDMA_0, integrating:
  - 1 Channel Controller, referenced as: EDMACC_0
  - 2 Transfer Controllers, referenced as: EDMACC_0_TC_0 (or EDMATC_0) and EDMACC_0_TC_1 (or EDMATC_1)
- EDMA_1, integrating:
  - 1 Channel Controller, referenced as: EDMACC_1
  - 2 Transfer Controllers, referenced as: EDMACC_1_TC_0 (or EDMATC_2) and EDMACC_1_TC_1 (or EDMATC_3)

The two EDMA channel controllers (EDMACC_0 and EDMACC_1) are functionally identical. For simplification, the unified name EDMACC shall be regularly used throughout this chapter when referring to EDMA Channel Controllers functionality and features.

The four EDMA transfer controllers (EDMACC_0_TC_0, EDMACC_0_TC_1, EDMACC_1_TC_0 and EDMACC_1_TC_1) are functionally identical. For simplification, the unified name EDMATC shall be regularly used throughout this chapter when referring to EDMA Transfer Controllers functionality and features.

Each EDMACC has the following features:

- Fully orthogonal transfer description
  - 3 transfer dimensions:
    - Array (multiple bytes)
    - Frame (multiple arrays)
    - Block (multiple frames)
  - Single event can trigger transfer of array, frame, or entire block
  - Independent indexes on source and destination

- Flexible transfer definition
  - Increment or constant addressing modes
  - Linking mechanism allows automatic PaRAM set update
  - Chaining allows multiple transfers to execute with one event
- 64 DMA channels
  - Channels triggered by either:
    - Event synchronization
    - Manual synchronization (CPU write to event set register)
    - Chain synchronization (completion of one transfer triggers another transfer)
  - Support for programmable DMA Channel to PaRAM mapping
- 8 Quick DMA (QDMA) channels
  - QDMA channels are triggered automatically upon writing to PaRAM set entry
  - Support for programmable QDMA channel to PaRAM mapping
- 512 PaRAM sets
  - Each PaRAM set can be used for a DMA channel, QDMA channel, or link set
- 2 transfer controllers/event queues
  - 16 event entries per event queue
- Interrupt generation based on:
  - Transfer completion
  - Error conditions
- Debug visibility
  - Queue water marking/threshold
  - Error and status recording to facilitate debug
- Memory protection support
  - Proxied memory protection for TR submission
  - Active memory protection for accesses to PaRAM and registers

Each EDMATC has the following features:

- Supports 2-dimensional (2D) transfers with independent indexes on source and destination (EDMACC manages the 3rd dimension)
- Up to 4 in-flight transfer requests (TR)
- Programmable priority levels
- Support for increment or constant addressing mode transfers
- Interrupt and error support
- Supports only little-endian operation in this device
- Memory mapped register (MMR) bit fields are fixed position in 32-bit MMR

For more information, see section *Enhanced DMA* in chapter *DMA Controllers* of the Device TRM.

6.15 Peripherals

6.15.1 VIP

The VIP module provides video capture functions for the device. VIP incorporates a multi-channel raw video parser, various video processing blocks, and a flexible Video Port Direct Memory Access (VPDMA) engine to store incoming video in various formats. The device uses three instantiations of the VIP module giving the ability of capturing up to six video streams.

A VIP module includes the following main features:

- Two independently configurable external video input capture slices (Slice 0 and Slice 1) each of which has two video input ports, Port A and Port B, where Port A can be configured as a 24/16/8-bit port, and Port B is a fixed 8-bit port.
- Each video Port A can be operated as a port with clock independent input channels (with interleaved or separated Y/C data input). Embedded sync and external sync modes are supported for all input configurations.
- Support for a single external asynchronous pixel clock, up to 165MHz per port.
- Pixel Clock Input Domain Port A supports up to one 24-bit input data bus, including BT.1120 style embedded sync for 16-bit and 24-bit data.
- Embedded Sync data interface mode supports single or multiplexed sources
- Discrete Sync data interface mode supports only single source input
- 24-bit data input plus discrete syncs can be configured to include:
  - 8-bit YUV422 (Y and U/V time interleaved)
  - 16-bit YUV422 (CbY and CrY time interleaved)
  - 24-bit YUV444
  - 16-bit RGB565
  - 24-bit RGB888
  - 12/16-bit RAW Capture
  - 24-bit RAW capture
- Discrete sync modes include:
  - VSYNC + HSYNC (FID determined by FID signal pin or HSYNC/VSYNC skew)
  - VSYNC + ACTVID + FID
  - VBLANK + ACTVID (ACTVID toggles in VBLANK) + FID
  - VBLANK + ACTVID (no ACTVID toggles in VBLANK) + FID
- VBLANK + ACTVID (no ACTVID toggles in VBLANK) + FID
  - Embedded syncs only
  - Pixel (2x or 4x) or Line multiplexed modes supported
  - Performs demultiplexing and basic error checking
  - Supports maximum of 9 channels in Line Mux (8 normal + 1 split line)
- Ancillary data capture support
  - For 16-bit or 24-bit input, ancillary data may be extracted from any single channel
  - For 8-bit time interleaved input, ancillary data can be chosen from the Luma channel, the Chroma channel, or both channels
  - Horizontal blanking interval data capture only supported when using discrete syncs (VSYNC + HSYNC or VSYNC + HBLANK)
  - Ancillary data extraction supported on multichannel capture as well as single source streams

- Format conversion and scaling
  - Programmable color space conversion
  - YUV422 to YUV444 conversion
  - YUV444 to YUV422 conversion
  - YUV422 to YUV420 conversion
  - YUV444 Source: YUV444 to YUV444, YUV444 to RGB888, YUV444 to YUV422, YUV444 to YUV420
  - RGB888 Source: RGB888 to RGB888, RGB888 to YUV444, RGB888 to YUV422, RGB888 to YUV420
  - YUV422 Source: YUV422 to YUV422, YUV422 to YUV420, YUV422 to YUV444, YUV422 to RGB888
  - Supports RAW to RAW (no processing)
  - Scaling and format conversions do not work for multiplexed input
- Supports up to 2047 pixels wide input - when scaling is engaged
- Supports up to 3840 pixels wide input - when only chroma up/down sampling is engaged, without scaling
- Supports up to 4095 pixels wide input - without scaling and chroma up/down sampling
- The maximum supported input resolution is further limited by:
  - Pixel clock and feature-dependent constraints
  - For RGB24-bit format (RAW data), the maximum frame width is limited to 2730 pixels

A VPDMA module includes the following main features:

- VPDMA output buffer size restriction feature, which ensures that writes do not exceed allocated memory buffer size
- Support for Tiled (2D) and raster addressing without bandwidth penalty
- Dual clients per channel allows for capture of scaled and nonscaled versions of the data stream (nonmultiplexed mode only)
- Start on new frame capability
- Interrupt every X number of frames
- Interrupt every X lines (synced to frame start)

For more information, see chapter *Video Input Port* of the Device TRM.

6.15.2 DSS

Display Port Interfaces (DPI) is available in DSS named DPI Video Output (VOUT).

VOUT interface consists of:

- 24-bit data bus (data[23:0])
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Field ID (FID)
- Pixel clock (CLK)

For more information, see section *Display Subsystem* of the Device TRM.

6.15.3 Timers

The device has 16 general-purpose (GP) timers (TIMER1 - TIMER16), two watchdog timers, and a 32-kHz synchronized timer (COUNTER_32K) that have the following features:

- Dedicated input trigger for capture mode and dedicated output trigger/pulse width modulation (PWM) signal

- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- On-the-fly read/write register (while counting)

The device has two system watchdog timer (WD_TIMER1 and WD_TIMER2) that have the following features:

- Free-running 32-bit upward counter
- On-the-fly read/write register (while counting)
- Reset upon occurrence of a timer overflow condition

The device includes one instance of the 32-bit watchdog timer: WD_TIMER2, also called the MPU watchdog timer.

The watchdog timer is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

For more information, see section *General-Purpose Timers* in chapter *Timers* of the Device TRM.

6.15.4 I2C

The device contains five multimaster high-speed (HS) inter-integrated circuit (I^2C) controllers (I2C*i* modules, where *i* = 1, 2, 3, 4, 5) each of which provides an interface between a local host (LH), such as a digital signal processor (DSP), and any I^2C-bus-compatible device that connects through the I^2C serial bus. External components attached to the I^2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I^2C interface.

Each multimaster HS I^2C controller can be configured to act like a slave or master I^2C-compatible device.

I2C1 and I2C2 controllers have dedicated I2C compliant open drain buffers, and support Fast mode (up to 400Kbps). I2C3, I2C4 and I2C5 controllers are multiplexed with standard LVCMOS IO and connected to emulate open drain. I^2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic 1. These controllers support HS mode (up to 3.4Mbps).

For more information, see section *Multimaster High-Speed I2C Controller (I2C)* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.5 UART

The UART is a simple L4 slave peripheral that utilizes the DMA_SYSTEM or EDMA for data transfer or IRQ polling via CPU. There are 10 UART modules in the device. Only one UART supports IrDA features. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

6.15.5.1 UART Features

The UARTi (where i = 1 to 10) include the following features:

- 16C750 compatibility
- 64-byte FIFO buffer for receiver and 64-byte FIFO for transmitter
- Programmable interrupt trigger levels for FIFOs
- Baud generation based on programmable divisors N (where N = 1…16,384) operating from a fixed functional clock of 48 MHz or 192 MHz

Oversampling is programmed by software as 16 or 13. Thus, the baud rate computation is one of two options:

- Baud rate = (functional clock / 16) / N
- Baud rate = (functional clock / 13) / N
- This software programming mode enables higher baud rates with the same error amount without changing the clock source
- Break character detection and generation
- Configurable data format:
  – Data bit: 5, 6, 7, or 8 bits
  – Parity bit: Even, odd, none
  – Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- The 48 MHz functional clock option allows baud rates up to 3.6Mbps
- The 192 MHz functional clock option allows baud rates up to 12Mbps
- UART1 module has extended modem control signals (DCD, RI, DTR, DSR)
- UART3 supports IrDA

6.15.5.2 IrDA Features

UART3 supports the following IrDA key features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications:
  – Frame formatting: Addition of variable beginning-of-frame (xBOF) characters and end-of-frame (EOF) characters
  – Uplink/downlink cyclic redundancy check (CRC) generation/detection
  – Asynchronous transparency (automatic insertion of break character)
  – Eight-entry status FIFO (with selectable trigger levels) to monitor frame length and frame errors
  – Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection

6.15.5.3 CIR Features

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable *t* period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on a user-definable frame structure and packet content.

The CIR (UART3 only) includes the following features to provide CIR support for remote-control applications:

- Transmit mode only (receive mode is not supported)
- Free data format (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency
- 1/2, 5/12, 1/3, or 1/4 carrier duty cycle

For more information, see section *UART/IrDA/CIR* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.6 McSPI

The McSPI is a master/slave synchronous serial bus. There are four separate McSPI modules (McSPI1, McSPI2, McSPI3, and McSPI4) in the device. All these four modules support up to four external devices (four chip selects) and are able to work as both master and slave.

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel

- Wide selection of McSPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode
- Master multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - McSPI configuration per channel. This means, clock definition, polarity enabling and word width
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for McSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel

For more information, see section *Multichannel Serial Peripheral Interface* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.7 QSPI

The quad serial peripheral interface (QSPI™) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only.

The QSPI supports the following features:

- General SPI features:
  - Programmable clock divider
  - Six pin interface
  - Programmable length (from 1 to 128 bits) of the words transferred
  - Programmable number (from 1 to 4096) of the words transferred
  - 4 external chip-select signals
  - Support for 3-, 4-, or 6-pin SPI interface
  - Optional interrupt generation on word or frame (number of words) completion
  - Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles
  - Programmable signal polarities
  - Programmable active clock edge
  - Software-controllable interface allowing for any type of SPI transfer
  - Control through L3_MAIN configuration port
- Serial flash interface (SFI) features:
  - Serial flash read/write interface
  - Additional registers for defining read and write commands to the external serial flash device
  - 1 to 4 address bytes
  - Fast read support, where fast read requires dummy bytes after address bytes; 0 to 3 dummy bytes can be configured.
  - Dual read support
  - Quad read support
  - Little-endian support only
  - Linear increment addressing mode only

The QSPI supports only dual and quad reads. Dual or quad writes are not supported. In addition, there is no "pass through" mode supported where the data present on the QSPI input is sent to its output.

For more information, see section *Quad Serial Peripheral Interface* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.8 McASP

The McASP functions as a general-purpose audio serial port optimized to the requirements of various audio applications. The McASP module can operate in both transmit and receive modes. The McASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an intercomponent digital audio interface transmission (DIT). The McASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although intercomponent digital audio interface reception (DIR) mode (i.e. S/PDIF stream receiving) is not natively supported by the McASP module, a specific TDM mode implementation for the McASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

The device have integrated 8 McASP modules (McASP1-McASP8) with:

- McASP1 and McASP2 supporting 16 channels with independent TX/RX clock/sync domain
- McASP3 through McASP8 modules supporting 4 channels with independent TX/RX clock/sync domain

For more information, see section *Multichannel Audio Serial Port* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.9 USB

SuperSpeed USB DRD Subsystem has three instances in the device providing the following functions:

- USB1: SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with integrated SS (USB3.0) PHY and HS/FS (USB2.0) PHY
- USB2: High-Speed (HS) USB 2.0 Dual-Role-Device (DRD) subsystem with integrated HS/FS PHY

SuperSpeed USB DRD Subsystem has the following features:

- Dual-role-device (DRD) capability:
  – Supports USB Peripheral (or Device) mode at speeds SS (5Gbps)(USB1 only), HS (480 Mbps), and FS (12 Mbps)
  – Supports USB Host mode at speeds SS (5Gbps)(USB1 only), HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps)
  – USB static peripheral operation
  – USB static host operation
  – Flexible stream allocation
  – Stream priority
  – External Buffer Control
- Each instance contains single xHCI controller with the following features:
  – Internal DMA controller
  – Descriptor caching and data prefetching
  – Interrupt moderation and blocking
  – Power management USB3.0 states for U0, U1, U2, and U3
  – Dynamic FIFO memory allocation for all endpoints
  – Supports all modes of transfers (control, bulk, interrupt, and isochronous)
  – Supports high bandwidth ISO mode
- Connects to an external charge pump for VBUS 5 V generation
- USB-HS PHY (USB2PHY1 and USB2PHY2 for USB1 and USB2, respectively): contain the USB functions, drivers, receivers, and pads for correct D+/D– signalling

For more information, see section *SuperSpeed USB DRD* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.10 SATA

The SATA host controller handles data interactions between a local host system memory and a SATA mass storage device with minimal local host (LH) intervention.

In contrast to the parallel 16-bit - ATA (PATA) interface, the SATA interface takes advantage of serial data transmission/reception over a differential pair of conductors. SATA uses the command set from the ATA/ATAPI-6 standard augmented with native command queuing (NCQ) commands optimized for the serialized interface.

The device has one embedded SATA host bus adapter (HBA) controller with a single port.

For more information, see section *SATA Controller* in chapter *Serial Communication Interface* of the Device TRM.

6.15.11 PCIe

The Peripheral Component Interconnect Express (PCIe) module is a multi-lane I/O interconnect that provides low pin-count, high reliability, and high-speed data transfer at rates of up to 5.0 Gbps per lane, per direction, for serial links on backplanes and printed wiring boards. It is a 3-rd Generation I/O Interconnect technology succeeding PCI and ISA bus that is designed to be used as a general-purpose serial I/O interconnect. It is also used as a bridge to other interconnects like USB2/3.0, GbE MAC, and so forth.

The PCI Express standard predecessor - PCI, is a parallel bus architecture that is increasingly difficult to scale-up in bandwidth, which is usually performed by increasing the number of data signal lines. The PCIe architecture was developed to help minimize I/O bus bottlenecks within systems and to provide the necessary bandwidth for high-speed, chip-to-chip, and board-to-board communications within a system. It is designed to replace the PCI-based shared, parallel bus signaling technology that is approaching its practical performance limits while simplifying the interface design.

The device instantiates two PCIe subsystems (PCIe_SS1 and PCIe_SS2). The PCIe controller is capable to operate either in Root Complex (RC) or in End Point (EP) PCIe mode. The device PCIe_SS1 controller supports up to two 16-bit data lanes on its PIPE port. The device PCIe_SS2 controller supports only one 16-bit data lane on its PIPE port.

When the PCIe_SS1 controller PIPE port is configured to operate in a single-lane mode, it operates on a single pair of PCIe PHY serializer and deserializer - PCIe1_PHY_TX/PCIe1_PHY_RX. When PCIe_SS1 PIPE is configured to operate in dual-lane mode, it operates on two pairs of PCIe PHY serializer and deserializer - PCIe1_PHY_TX/PCIe1_PHY_RX and PCIe2_PHY_TX/PCIe2_PHY_RX, respectively. The single-lane PCIe_SS2 controller PIPE port (if enabled) can operate only on the PCIe2_PHY_TX/PCIe2_PHY_RX pair. Hereby, if PCIe_SS2 controller is used, the PCIe_SS1 can operate only in a single-lane mode on the PCIe1_PHY_TX/PCIe1_PHY_RX. In addition, PCIe PHY subsystem encompasses a PCIe PCS (physical coding sublayer), a PCIe power management logic, APLL, a DPLL reference clock generator and an APLL clock low-jitter buffer.

- The PCIe Controller implements the transport and link layers of the PCIe interface protocol.
- PCIe PCS (a physical coding sublayer component) converts a 8-bit portion of parallel data over a PCIe lane to a 10-bit parallel data to adapt the process of serialization and deserialization in the TX/RX PHYs to various requirements. At the same time it transforms the transmission rate to maintain the PCIe Gen2 bandwidth (5 Gbps) on both sides (PCIe controller and PHY).
- A multiplexer logic which adds flexibility to connect a PCIe controller hardware mapped PCS logic output to a single (for the single-lane PCIe_SS2 controller) or to a couple (for the 2-lane PCIe_SS1 controller) of PHY ports at a time

- Physical layer (PHY) serializer/deserializer components with associated power control logic, building the so called PMA (physical media attachment) part of the PCIe_PHY transceiver, as follows:
  - PCIe physical port 0 associated serializer (TX) - PCIe1_PHY_TX and deserializer (RX) - PCIe1_PHY_RX
  - PCIe physical port 1 associated serializer (TX) - PCIe2_PHY_TX and deserializer (RX) - PCIe2_PHY_RX
- DPLL_PCIe_REF is a DPLL clock source, controlled from the device PRCM, that provides a 100-MHz clock to the PCIe PHY serializer/deserializer components reference clock inputs.
- Both the PCIe_SS1 and PCIe_SS2 share the same APLL (APLLPCIe) which by default multiplies the DPLL_PCIe_REF (typically 100 MHz or 20 MHz) clock to 2.5 GHz.
- The APLLPCIe low-jitter buffer (ACSPCIE) and additional logic takes care to provide the PCIe APLL reference input clock.

PCIe module supports the following features:

- PCI Local Bus Specification revision 3.0
- PCI Express Base 3.0 Specification, revision 1.0.

At system level the device supports PCI express interface in the following configurations:

- Each PCIe subsystem controller has support for PCIe Gen2 mode (5.0 Gbps per lane) and Gen1 mode (2.5 Gbps per lane).
- One PCIe (PCIe_SS1) operates as Gen2 2-lanes supporting in either root-complex (RC) or end-point EP.
- Two PCIe (PCIe_SS1 and PCIe_SS2) operates Gen2 1-lane supporting either RC or EP with the possibility of one operating in Gen1 and one in Gen2.
- PCIe_SS1 can be configured to operate in either 2-Lane (dual lane) or 1-Lane (single lane) mode, as follows:
  - Single Lane - lane 0 mapped to the PCIe port 0 of the device
  - Flexible dual lane configuration - lanes 0 and 1 can be swapped on the two PCIe ports
- PCIe_SS2 can only operate in 1-Lane mode, as follows:
  - Single Lane - lane 0 mapped to the device PCIe port 1

  When PCie_SS1 is configured to operate in dual-lane mode, PCIe_SS2 is in-operable as both PCIe1_PHY_RX/TX and PCIe2_PHY_RX/TX are assigned to PCIe_SS1, and thereby NOT available to PCIe_SS2.

The main features of a device PCIe controller are:

- 16-bit operation at 250 MHz on PIPE interface (per 16-bit lane)
- One master port on the L3_MAIN supporting 32-bit address and 64-bit data bus.
- PCIe_SS1 master port dedicated MMU (device MMU2) on L3_MAIN path, to which PCIe traffic can be optionally mapped.
- One slave port on the L3_MAIN supporting 29-bit address and 64-bit data bus.
- Maximum outbound payload size of 64 Bytes (the L3 Interconnect PCIe1/2 target ports split bursts of size >64 Bytes to the into multiple 64 Byte bursts)
- Maximum inbound payload size of 256 Bytes (internally converted to 128 Byte - bursts)
- No remote read request size limit: implicit support for 4 KiB-size and greater
- Support of EP legacy mode
- Support of inbound I/O accesses in EP legacy mode
- PIPE interface features fixed-width (16-bit data per lane) and dynamic frequency to switch between PCIe Gen1 and Gen2.
- Ultra-low transmit and receive latency
- Automatic Lane reversal as specified in the PCI Express Base 3.0 Specification, revision 1.0 (transmit and receive)

- Polarity inversion on receive
- Single Virtual Channel (VC0) and Single Traffic Class (TC0)
- Single Function in End point mode
- Automatic credit management
- ECRC generation and checking
- All PCI Device Power Management D-states with the exception of $D3_{cold}$/L2 state
- PCI Express Active State Power Management (ASPM) state L0s and L1 (with exceptions)
- PCI Express Link Power Management states except for L2 state
- PCI Express Advanced Error Reporting (AER)
- PCI Express messages for both transmit and receive
- Filtering for Posted, Non-Posted, and Completion traffic
- Configurable BAR filtering, I/O filtering, configuration filtering and completion lookup/timeout
- Access to configuration space registers and external application memory mapped registers through ECAM mechanism.
- Legacy PCI Interrupts reception (RC) and generation (EP)
- 2 x hardware interrupts per PCIe_SS1 and PCIe_SS2 controller mapped via the device Interrupt Crossbar (IRQ_CROSSBAR) to multiple device host (MPU, DSP, and so forth) interrupt controllers in the device
- MSIs generation and reception
- PCIe_PHY Loopback in RC mode

For more information, see section *PCIe Controller* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.12 CAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time applications. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The device provides two DCAN interfaces for supporting distributed realtime control with a high level of security. The DCAN interfaces implement the following features:

- Support one CAN 2.0B Protocol
- Support one CAN 2.0B Protocol with available FD (Flexible Data Rate) functionality
- Bit rates up to 1 MBit/s
- 64 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Direct access to Message RAM during test mode
- CAN Rx/Tx pins are configurable as general-purpose IO pins
- Two interrupt lines (plus additional parity-error interrupts line)
- RAM initialization
- DMA support

For more information, see section *DCAN* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.13 GMAC_SW

The three-port gigabit ethernet switch subsystem (GMAC_SW) provides ethernet packet communication and can be configured as an ethernet switch. It provides the gigabit media independent interface (G/MII) in MII mode, reduced gigabit media independent interface (RGMII), reduced media independent interface (RMII), and the management data input output (MDIO) for physical layer device (PHY) management.

The GMAC_SW subsystem provides the following features:

- Two Ethernet ports (port 1 and port 2) with selectable RGMII, RMII, and G/MII (in MII mode only) interfaces plus internal Communications Port Programming Interface (CPPI 3.1) on port 0
- Synchronous 10/100/1000 Mbit operation
- Wire rate switching (802.1d)
- Non-blocking switch fabric
- Flexible logical FIFO-based packet buffer structure
- Four priority level Quality Of Service (QOS) support (802.1p)
- CPPI 3.1 compliant DMA controllers
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D and Annex F)
  - Timing FIFO and time stamping logic embedded in the subsystem
- Device Level Ring (DLR) Support
- Energy Efficient Ethernet (EEE) support (802.3az)
- Flow Control Support (802.3x)
- Address Lookup Engine (ALE)
  - 1024 total address entries plus VLANs
  - Wire rate lookup
  - Host controlled time-based aging
  - Multiple spanning tree support (spanning tree per VLAN)
  - L2 address lock and L2 filtering support
  - MAC authentication (802.1x)
  - Receive-based or destination-based multicast and broadcast rate limits
  - MAC address blocking
  - Source port locking
  - OUI (Vendor ID) host accept/deny feature
  - Remapping of priority level of VLAN or ports
- VLAN support
  - 802.1Q compliant
    - Auto add port VLAN for untagged frames on ingress
    - Auto VLAN removal on egress and auto pad to minimum frame size
- Ethernet Statistics:
  - EtherStats and 802.3Stats Remote network Monitoring (RMON) statistics gathering (shared)
  - Programmable statistics interrupt mask when a statistic is above one half its 32-bit value
- • Flow Control Support (802.3x)
- Digital loopback and FIFO loopback modes supported
- Maximum frame size 2016 bytes (2020 with VLAN)
- 8k (2048 × 32) internal CPPI buffer descriptor memory
- Management Data Input/Output (MDIO) module for PHY Management
- Programmable interrupt control with selected interrupt pacing
- Emulation support

- Programmable Transmit Inter Packet Gap (IPG)
- Reset isolation (switch function remains active even in case of all device resets except for POR pin reset and ICEPICK cold reset)
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps.
- IEEE 802.3 gigabit Ethernet conformant

For more information, see section *Gigabit Ethernet Switch (GMAC_SW)* in chapter *Serial Communication Interfaces* of the Device TRM.

6.15.14 eMMC/SD/SDIO

The eMMC/SD/SDIO host controller provides an interface between a local host (LH) such as a microprocessor unit (MPU) or digital signal processor (DSP) and either eMMC, SD® memory cards, or SDIO cards and handles eMMC/SD/SDIO transactions with minimal LH intervention.

Optionally, the controller is connected to the L3_MAIN interconnect to have a direct access to system memory. It also supports two direct memory access (DMA) slave channels or a DMA master access (in this case, slave DMA channels are deactivated) depending on its integration.

The eMMC/SD/SDIO host controller deals with eMMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit, and checking for syntactical correctness.

The application interface can send every eMMC/SD/SDIO command and poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.

The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The eMMC/SD/SDIO host controller also supports two DMA channels.

There are four eMMC/SD/SDIO host controllers inside the device. gives an overview of the eMMC/SD/SDIOi (i = 1 to 4) controllers.

Each controller has the following data width:

- eMMC/SD/SDIO1 - 4-bit wide data bus
- eMMC/SD/SDIO2 - 8-bit wide data bus
- eMMC/SD/SDIO3 - 8-bit wide data bus
- eMMC/SD/SDIO4 - 4-bit wide data bus

The eMMC/SD/SDIOi controller is also referred to as MMCi.

Compliance with standards:

- Full compliance with MMC/eMMC command/response sets as defined in the JC64 MMC/eMMC Standard Specification, v4.5.
- Full compliance with SD command/response sets as defined in the SD Physical Layer Specification v3.01
- Full compliance with SDIO command/response sets and interrupt/read-wait suspend-resume operations as defined in the SD part E1 Specification v3.00
- Full compliance with SD Host Controller Standard Specification sets as defined in the SD card Specification Part A2 v3.00

Main features of the eMMC/SD/SDIO host controllers:

- Flexible architecture allowing support for new command structure
- 32-bit wide access bus to maximize bus throughput
- Designed for low power
- Programmable clock generation
- Dedicated DLL to support SDR104 mode (MMC1 only)
- Dedicated DLL to support HS200 mode (MMC2 only)

- Card insertion/removal detection and write protect detection
- L4 slave interface supports:
  - 32-bit data bus width
  - 8/16/32 bit access supported
  - 9-bit address bus width
  - Streaming burst supported only with burst length up to 7
  - WNP supported
- L3 initiator interface Supports:
  - 32-bit data bus width
  - 8/16/32 bit access supported
  - 32-bit address bus width
  - Burst supported
- Built-in 1024-byte buffer for read or write
- Two DMA channels, one interrupt line
- Support JC 64 v4.4.1 boot mode operations
- Support SDA 3.00 Part A2 programming model
- Support SDA 3.00 Part A2 DMA feature (ADMA2)
- Supported data transfer rates:
  - MMCi supports the following SD v3.0 data transfer rates:
    - DS mode (3.3V IOs): up to 12 MBps (24 MHz clock)
    - HS mode (3.3V IOs): up to 24 MBps (48 MHz clock)
    - SDR12 (1.8V IOs): up to 12 MBps (24 MHz clock)
    - SDR25 (1.8V IOs): up to 24 MBps (48 MHz clock)
    - SDR50 (1.8V IOs): up to 48 MBps (96 MHz clock) - MMC1 and MMC3 only
    - DDR50 (1.8V IOs): up to 48 MBps (48 MHz clock) - MMC1 only
    - SDR104 (1.8V IOs) cards can be supported up to 192 MHz clock (96 MBps max) - MMC1 only
  - MMCi supports the Default SD mode 1-bit data transfer up to 24Mbps (3MBps)
  - Only MMC2 supports also the following JC64 v4.5 data transfer rates:
    - Up to 192 MBps in eMMC mode, 8-bit SDR mode (192 MHz clock frequency)
    - Up to 96 MBps in eMMC mode, 8-bit DDR mode (48 MHz clock frequency)
- All eMMC/SD/SDIO controllers are connected to 1.8V/3.3V compatible I/Os to support 1.8V/3.3V signaling

NOTE

eMMC functionality is supported fully by MMC2 only. The other MMC modules are capable of eMMC functionality, but are not timing-optimized for eMMC.

The differences between the eMMC/SD/SDIO host controllers and a standard SD host controller defined by the *SD Card Specification, Part A2, SD Host Controller Standard Specification*, v3.0 are:

- The clock divider in the eMMC/SD/SDIO host controller supports a wider range of frequency than specified in the *SD Memory Card Specifications*, v3.0. The eMMC/SD/SDIO host controller supports odd and even clock ratio.
- The eMMC/SD/SDIO host controller supports configurable busy time-out.
- ADMA2 64-bit mode is not supported.
- There is no external LED control.

NOTE

Only even ratios are supported in DDR mode.

For more information, see chapter *eMMC/SD/SDIO* of the Device TRM.

6.15.15 GPIO

The general-purpose interface combines eight general-purpose input/output (GPIO) banks.

Each GPIO module provides 32 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 247 pins.

These pins can be configured for the following applications:

- Data input (capture)/output (drive)
- Keyboard interface with a debounce cell
- Interrupt generation in active mode upon the detection of external events. Detected events are processed by two parallel independent interrupt-generation submodules to support biprocessor operations
- Wake-up request generation in idle mode upon the detection of external events

NOTE

The general-purpose input/output i (i = 1 to 8) bank is also referred to as GPIOi.

For more information, see chapter *General-Purpose Interface* of the Device TRM.

6.15.16 ePWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The ePWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the ePWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

Each ePWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software.
- Programmable phase-control support for lag or lead operation relative to other ePWM modules.
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis.
- Dead-band generation with independent rising and falling edge delay control.
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions.
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs.
- Programmable event prescaling minimizes CPU overhead on interrupts.
- PWM chopping by high-frequency carrier signal, useful for pulse transformer gate drives.

For more information, see section *Enhanced PWM (ePWM) Module* in chapter *Pulse-Width Modulation Subsystem* of the Device TRM.

6.15.17 eCAP

Uses for eCAP include:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- 4 stage sequencer (Mod4 counter) which is synchronized to external events (ECAPx pin edges)
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module includes the following features:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event time-stamps
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output

For more information, see section *Enhanced Capture (eCAP) Module* in chapter *Pulse-Width Modulation Subsystem* of the Device TRM.

6.15.18 eQEP

A single track of slots patterns the periphery of an incremental encoder disk. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position, and zero reference.

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 kHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

For more information, see section *Enhanced Quadrature Encoder Pulse (eQEP) Module* in chapter *Pulse-Width Modulation Subsystem* of the Device TRM.

6.16 On-Chip Debug

Debugging a system that contains an embedded processor involves an environment that connects high-level debugging software running on a host computer to a low-level debug interface supported by the target device. Between these levels, a debug and trace controller (DTC) facilitates communication between the host debugger and the debug support logic on the target chip.

The DTC is a combination of hardware and software that connects the host debugger to the target system. The DTC uses one or more hardware interfaces and/or protocols to convert actions dictated by the debugger user to JTAG commands and scans that execute the core hardware.

The debug software and hardware components let the user control multiple central processing unit (CPU) cores embedded in the device in a global or local manner. This environment provides:

- Synchronized global starting and stopping of multiple processors
- Starting and stopping of an individual processor
- Each processor can generate triggers that can be used to alter the execution flow of other processors

System topics include but are not limited to:

- System clocking and power-down issues
- Interconnection of multiple devices
- Trigger channels

For more information, see chapter *On-chip Debug* of the Device TRM.

The device deploys Texas Instrument's CTools debug technology for on-chip debug and trace support. It provides the following features:

- External debug interfaces:
  - Primary debug interface - IEEE1149.1 (JTAG) or IEEE1149.7 (complementary superset of JTAG)
    - Used for debugger connection
    - Default mode is IEEE1149.1 but debugger can switch to IEEE1149.7 via an IEEE1149.7 adapter module
    - Controls ICEPick™ (generic test access port [TAP] for dynamic TAP insertion) to allow the debugger to access several debug resources through its secondary (output) JTAG ports (for more information, see *ICEPick Secondary TAPs* section of the Device TRM).
  - Debug (trace) port
    - Can be used to export processor or system trace off-chip (to an external trace receiver)
    - Can be used for cross-triggering with an external device
    - Configured through debug resources manager (DRM) module instantiated in the debug subsystem
    - For more information about debug (trace) port, see *Debug (Trace) Port* and *Concurrent Debug Modes* sections of the Device TRM.
- JTAG based processor debug on:
  - Cortex-A15 in MPU
  - C66x in DSP1
  - Cortex-M4 (x2) in IPU1, IPU2
  - Arm968 (x2) in IVA
- Dynamic TAP insertion
  - Controlled by ICEPick
  - For more information, see , *Dynamic TAP Insertion.*
- Power and clock management
  - Debugger can get the status of the power domain associated to each TAP.
  - Debugger may prevent the application software switching off the power domain.
  - Application power management behavior can be preserved during debug across power transitions.
  - For more information, see *Power and Clock Management* section of the Device TRM.

- Reset management
  - Debugger can configure ICEPick to assert, block, or extend the reset of a given subsystem.
  - For more information, see *Reset Management* section of the Device TRM.
- Cross-triggering
  - Provides a way to propagate debug (trigger) events from one processor, subsystem, or module to another:
    - Subsystem A can be programmed to generate a debug event, which can then be exported as a global trigger across the device.
    - Subsystem B can be programmed to be sensitive to the trigger line input and to generate an action on trigger detection.
  - Two global trigger lines are implemented
  - Device-level cross-triggering is handled by the XTRIG (TI cross-trigger) module implemented in the debug subsystem
  - Various Arm® CoreSight™ cross-trigger modules implemented to provide support for CoreSight triggers distribution
    - CoreSight Cross-Trigger Interface (CS_CTI) modules
    - CoreSight Cross-Trigger Matrix (CS_CTM) modules
  - For more information about cross-triggering, see *Cross-Triggering* section of the Device TRM.
- Suspend
  - Provides a way to stop a closely coupled hardware process running on a peripheral module when the host processor enters debug state
  - For more information about suspend, see *Suspend* section of the Device TRM.
- MPU watchpoint
  - Embedded in MPU subsystem
  - Provides visibility on MPU to EMIF direct paths
  - For more information, see *MPU Memory Adaptor (MPU_MA) Watchpoint* section of the Device TRM.
- Processor trace
  - Cortex-A15 (MPU) and C66x (DSP) processor trace is supported
  - Program trace only for MPU (no data trace)
  - MPU trace supported by a CoreSight Program Trace Macrocell (CS_PTM) module
  - Three exclusive trace sinks:
    - CoreSight Trace Port Interface Unit (CS_TPIU) – trace export to an external trace receiver
    - CTools Trace Buffer Router (CT_TBR) in system bridge mode – trace export through USB
    - CT_TBR in buffer mode – trace history store into on-chip trace buffer
  - For more information, see *Processor Trace* section of the Device TRM.

- System instrumentation (trace)
  - Supported by a CTools System Trace Module (CT_STM), implementing MIPI System Trace Protocol (STP) (rev 2.0)
  - Real-time software trace
    - MPU software instrumentation through CoreSight STM (CS_STM) (STP2.0)
    - System-on-chip (SoC) software instrumentation through CT_STM (STP2.0)
  - OCP watchpoint (OCP_WP_NOC)
    - OCP target traffic monitoring: OCP_WP_NOC can be configured to generate a trigger upon watchpoint match (that is, when target transaction attributes match the user-defined attributes).
    - SoC events trace
    - DMA transfer profiling
  - Statistics collector (performance probes)
    - Computes traffic statistics within a user-defined window and periodically reports to the user through the CT_STM interface
    - Embedded in the L3_MAIN interconnect
    - 10 instances:
      - 1 instance dedicated to target (SDRAM) load monitoring
      - 9 instances dedicated to master latency monitoring
  - IVA instrumentation (hardware accelerator [HWA] profiling)
    - Supported through a software message and system trace event (SMSET) module embedded in the IVA subsystem
  - Power-management events profiling (PM instrumentation [PMI])
    - Monitoring major power-management events. The PM state changes are handled as generic events and encapsulated in STP messages.
  - Clock-management events profiling (CM instrumentation [CMI])
    - Monitoring major clock management events. The CM state changes are handled as generic events and encapsulated in STP messages.
    - Two instances, one per CM
      - CM1 Instrumentation (CMI1) module mapped in the PD_CORE_AON power domain
      - CM2 Instrumentation (CMI2) module mapped in the PD_CORE power domain
  - For more information, see *System Instrumentation* section of the Device TRM.
- Performance monitoring
  - Supported by subsystem counter timer module (SCTM) for IPU
  - Supported by performance monitoring unit (PMU) for MPU subsystem

For more information, see chapter *On-Chip Debug Support* of the Device TRM.

7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

7.1 Introduction

This chapter is intended to communicate, guide and illustrate a PCB design strategy resulting in a PCB that can support TI's latest Application Processor. This Processor is a high-performance processor designed for automotive Infotainment and Advanced Driver Assistance Systems based on enhanced OMAP™ architecture integrated on a 28-nm CMOS process technology.

These guidelines first focus on designing a robust Power Delivery Network (PDN) which is essential to achieve the desirable high performance processing available on Device. The general principles and step-by-step approach for implementing good power integrity (PI) with specific requirements will be described for the key Device power domains.

TI strongly believes that simulating a PCB's proposed PDN is required for first pass PCB design success. Key Device processor high-current power domains need to be evaluated for Power Rail IR Drop, Decoupling Capacitor Loop-Inductance and Power Rail Target Impedance. Only then can a PCB's PDN performance be truly accessed by comparing these model PI parameters vs. TI's recommended values. Ultimately for any high-volume product, TI recommends conducting a “Processor PDN Validation” test on prototype PCBs across processor “split lots” to verify PDN robustness meets desired performance goals for each customer's worst-case scenario. Please contact your TI representative to receive guidance on PDN PI modeling and validation testing.

Likewise, the methodology and requirements needed to route Device high-speed, differential interfaces (i.e. USB2.0, USB3.0, HDMI, PCI, SATA), single-ended interfaces (i.e. DDR2/DDR3, QSPI) and general purpose interfaces using LVCMOS drivers that meet timing requirements while minimizing signal integrity (SI) distortions on the PCB's signaling traces. Signal trace lengths and flight times are aligned with FR-4 standard specification for PCBs.

Several different PCB layout stack-up examples have been presented to illustrate a typical number of layers, signal assignments and controlled impedance requirements. Different Device interface signals demand more or less complexity for routing and controlled impedance stack-ups. Optimizing the PCB's PDN stack-up needs with all of these different types of signal interfaces will ultimately determine the final layer count and layer assignments in each customer's PCB design.

This guideline must be used as a supplement in complement to TI's Application Processor, Power Management IC (PMIC) and Audio Companion components along with other TI component technical documentation (i.e. Technical Reference Manual, Data Manual, Data Sheets, Silicon Errata, Pin-Out Spreadsheet, Application Notes, etc.).

NOTE

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for customer boards. The data described in this appendix are intended as guidelines only.

NOTE

These PCB guidelines are in a draft maturity and consequently, are subject to change depending on design verification testing conducted during IC development and validation. Note also that any references to Application Processor's ballout or pin muxing are subject to change following the processor's ballout maturity.

7.1.1 Initial Requirements and Guidelines

Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35 Ω and 65 Ω to minimize the overshoot or undershoot on far-end loads.

Characteristic impedance for differential interfaces must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the recommended differential impedance. For more information see Section 7.5.1.

The PDN must be optimized for low trace resistance and low trace inductance for all high-current power nets from PMIC to the device.

An external interface using a connector must be protected following the IEC61000-4-2 level 4 system ESD.

7.2 Power Optimizations

This section describes the necessary steps for designing a robust Power Distribution Network (PDN):

- **Section 7.2.1**, **Step 1:** PCB Stack-up
- **Section 7.2.2**, **Step 2:** Physical Placement
- **Section 7.2.3**, **Step 3:** Static Analysis
- **Section 7.2.4**, **Step 4:** Frequency Analysis

7.2.1 Step 1: PCB Stack-up

The PCB stack-up (layer assignment) is an important factor in determining the optimal performance of the power distribution system. An optimized PCB stack-up for higher power integrity performance can be achieved by following these recommendations:

- Power and ground plane pairs must be closely coupled together. The capacitance formed between the planes can decouple the power supply at high frequencies. Whenever possible, the power and ground planes must be solid to provide continuous return path for return current.
- Use a thin dielectric between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (the dielectric thickness) maximizes the capacitance.
- Optimize the power and ground plane pair carrying high current supplies to key component power domains as close as possible to the same surface where these components are placed (see Figure 7-1). This will help to minimize "loop inductance" encountered between supply decoupling capacitors and component supply inputs and between power and ground plane pairs.

NOTE

1-2oz Cu weight for power / ground plane is preferred to enable better PCB heat spreading, helping to reduce Processor junction temperatures. In addition, it is preferable to have the power / ground planes be adjacent to the PCB surface on which the Processor is mounted.

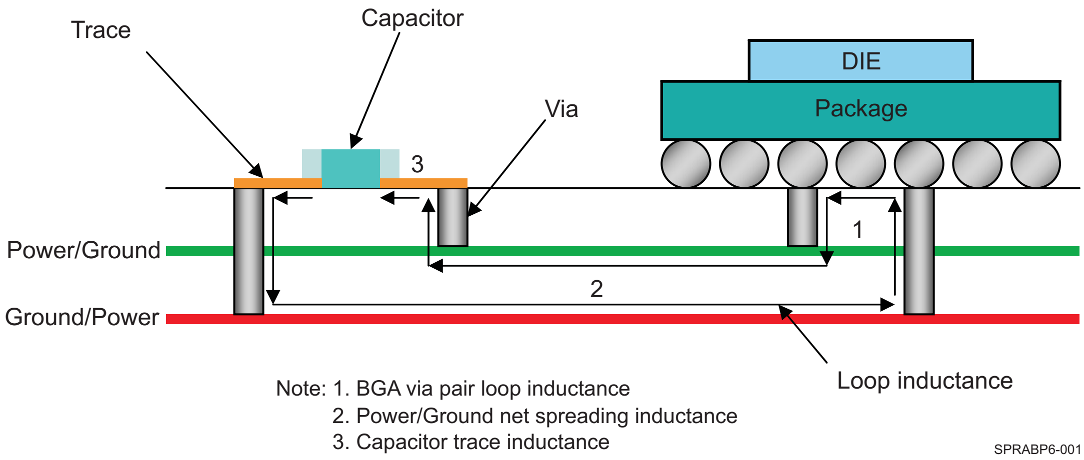

Figure 7-1. Minimize Loop Inductance With Proper Layer Assignment

The placement of power and ground planes in the PCB stackup (determined by layer assignment) has a significant impact on the parasitic inductances of power current path as shown in Figure 7-1. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high-priority supplies in the top half of the stackup (assuming high load and priority components are mounted on the top-side of PCB) and low-priority supplies in the bottom half of the stackup as shown in the examples below (vias have parasitic inductances which impact the bottom layers more, so it is advised to put the sensitive and high-priority power supplies on the top/same layers).

Two PCB stack-ups with layer assignments and via types that can enable an optimize PDN are shown in Figure 7-2 and Figure 7-3.

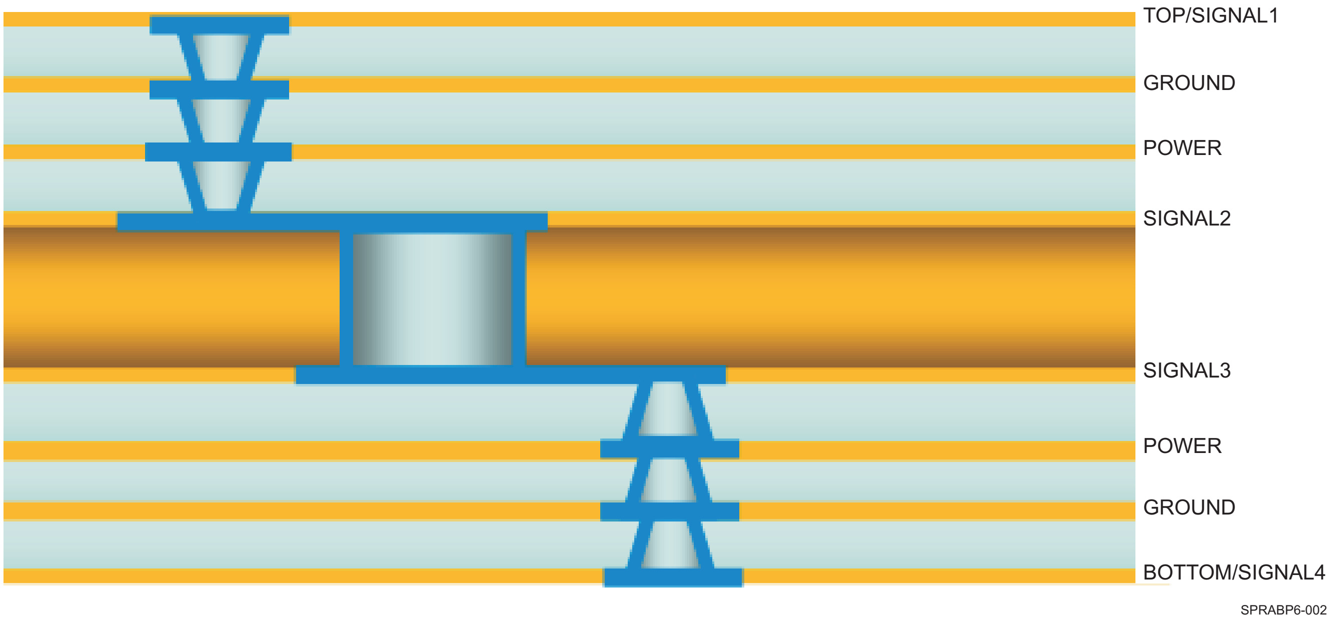

Figure 7-2. Layer PCB With High Density Interconnect (HDI) Vias

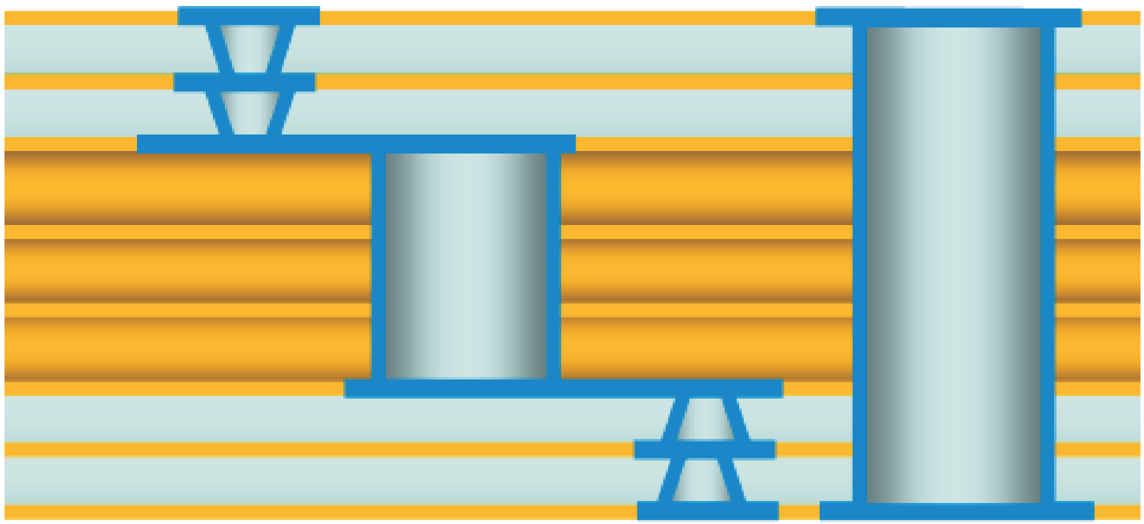

Figure 7-3. Layer PCB With Plated Through Holes (PTH) Vias

7.2.2 Step 2: Physical Placement

A critical step in designing an optimized PDN is that proper care must be taken to making sure that the initial floor planning of the PCB layout is done with good power integrity design guidelines in mind. The following points are important for optimizing a PCB's PDN:

- Minimizing the physical distance between power sources and key high load components is the first step toward optimization. Placing source and load components on the same side of the PCB is desirable. This will minimize via inductance impact for high current loads and steps
- External trace routing between components must be as wide as possible. The wider the traces, the lower the DC resistance and consequently the lower the static IR drop.
- Whenever possible for the internal layers (routing and plane), wide traces and copper area fills are preferred for PDN layout. The routing of power nets in plane provide for more interplane capacitance and improved high frequency performance of the PDN.
- Whenever possible, use a via to component pin/pad ratio of 1:1 or better (i.e. especially decoupling capacitors, power inductors and current sensing resistors). Do not share vias among multiple capacitors for connecting power supply and ground planes.
- Placement of vias must be as close as possible or even within a component's solder pad if the PCB technology you are using provides this capability.

  Figure 7-4 shows an example of acceptable width for power net routing but with poor via placement.

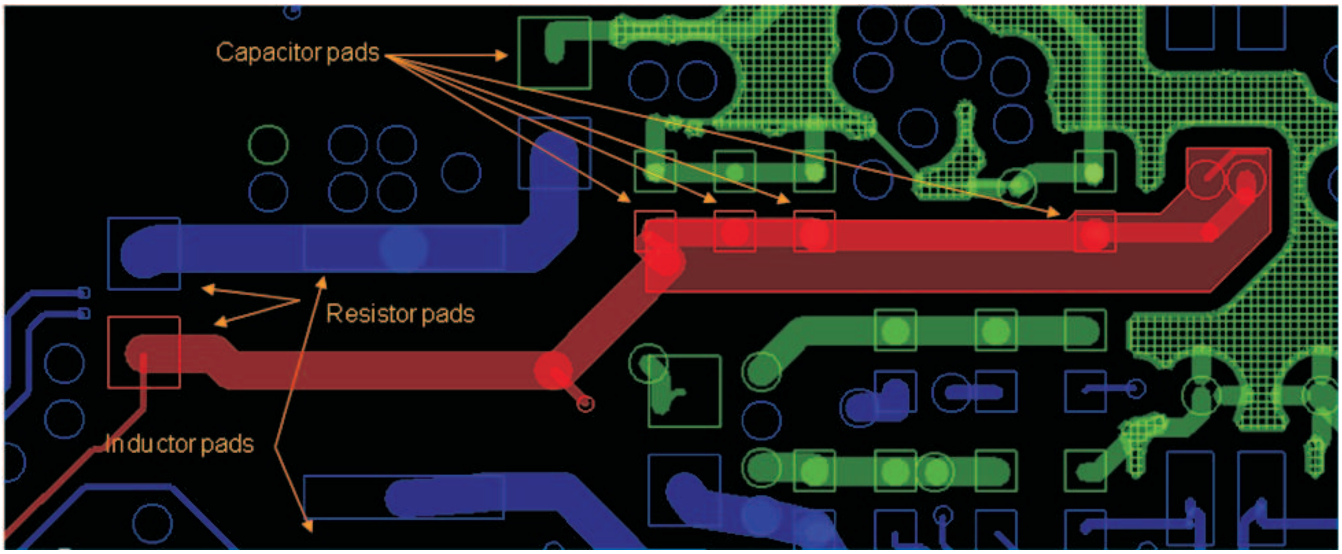

Figure 7-4. Poor Via Assignment for PDN

Figure 7-5 shows an improved power net routing with better via assignment and placement, respectively.

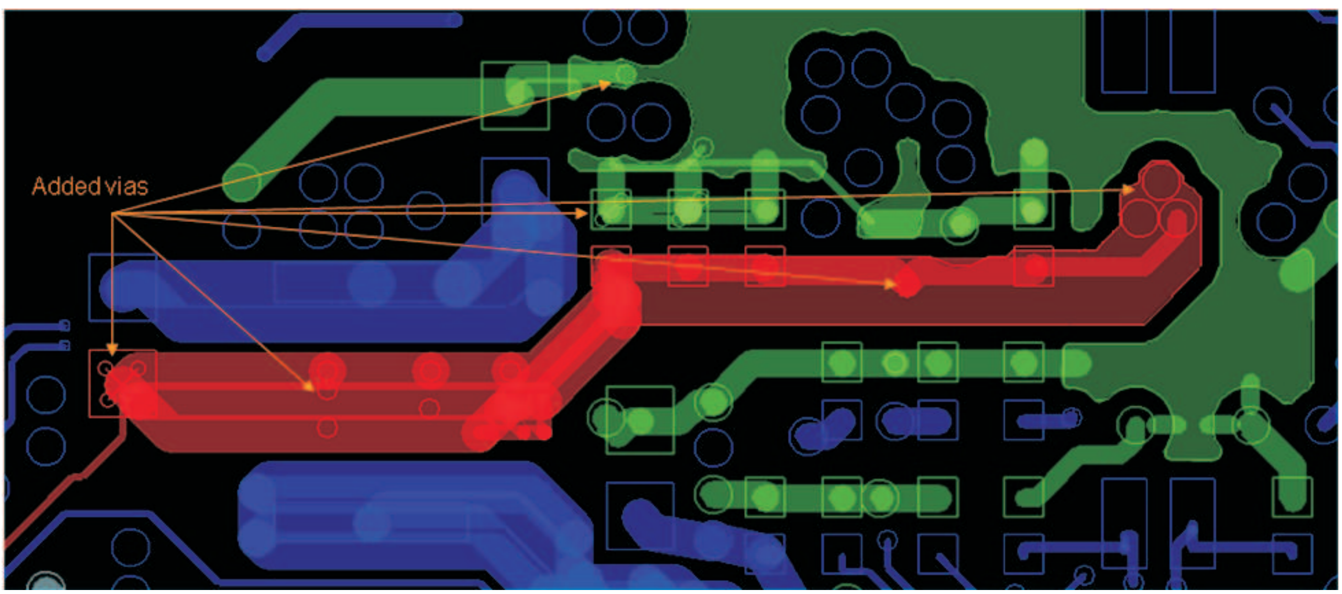

Figure 7-5. Improved Via Assignment for PDN

- To avoid any "ampacity" issue – maximum current-carrying capacity of each transitional via should be evaluated to determine the appropriate number of vias required to connect components.

  Figure 7-6 and Figure 7-7 show examples of "via starvation" on a power net transitioning from top routing layer to internal layers and the improved layout, respectively. Adding vias to bring the "via-to-pad" ratio to 1:1 will improve PDN performance.

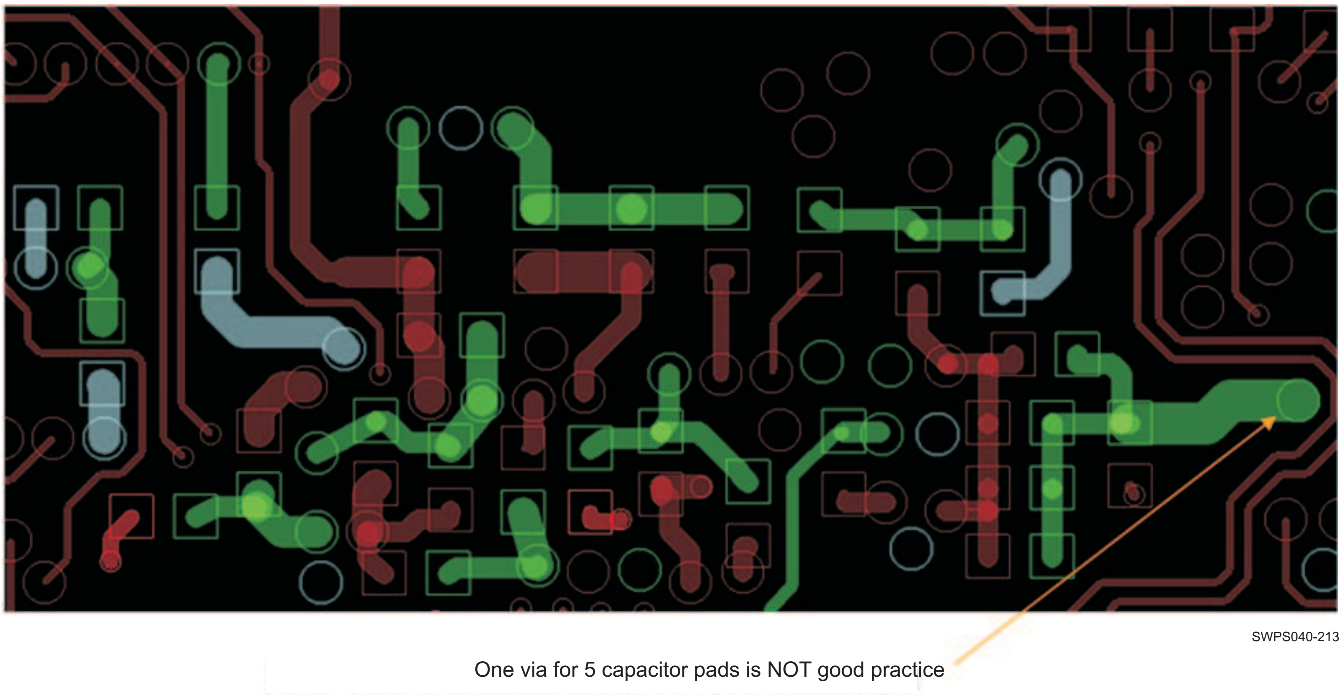

Figure 7-6. Via Starvation

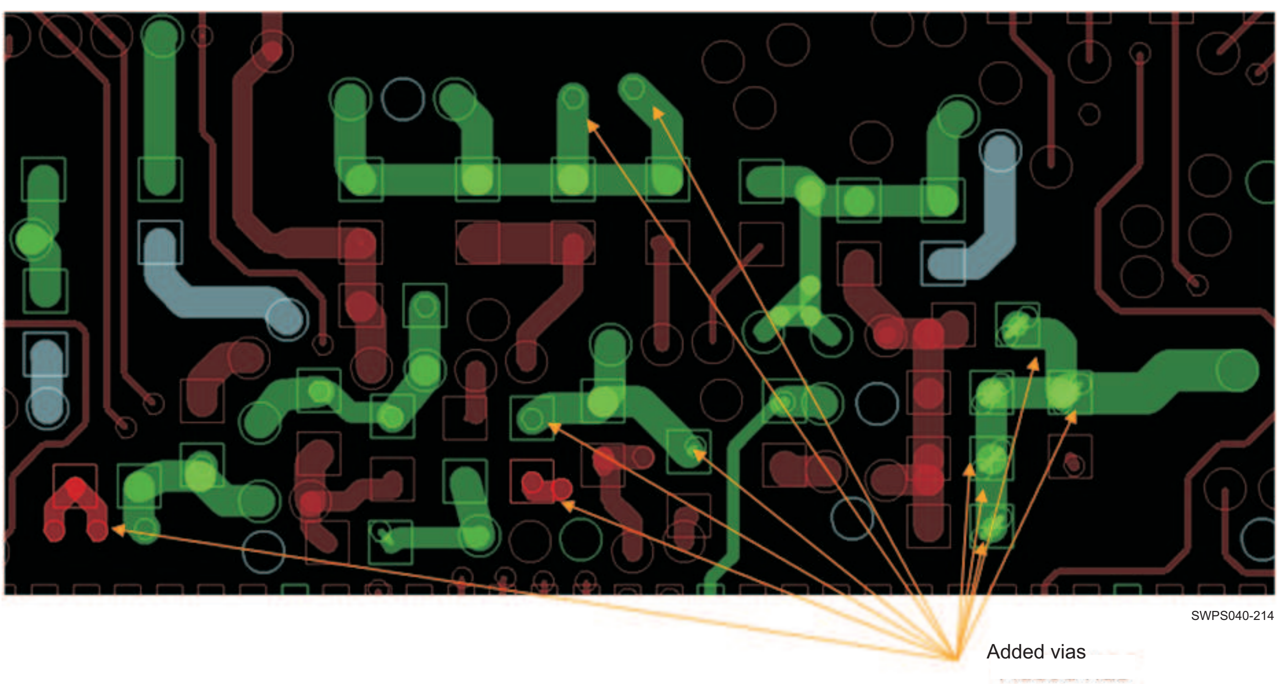

Figure 7-7. Improved Layout With More Transitional Vias

- For noise sensitive power supplies (i.e. Phase Lock-Loops, analog signals like audio and video), a Gnd shield can be used to isolate coplanar supplies that may have high step currents or high frequency switching transitions from coupling into low-noise supplies.

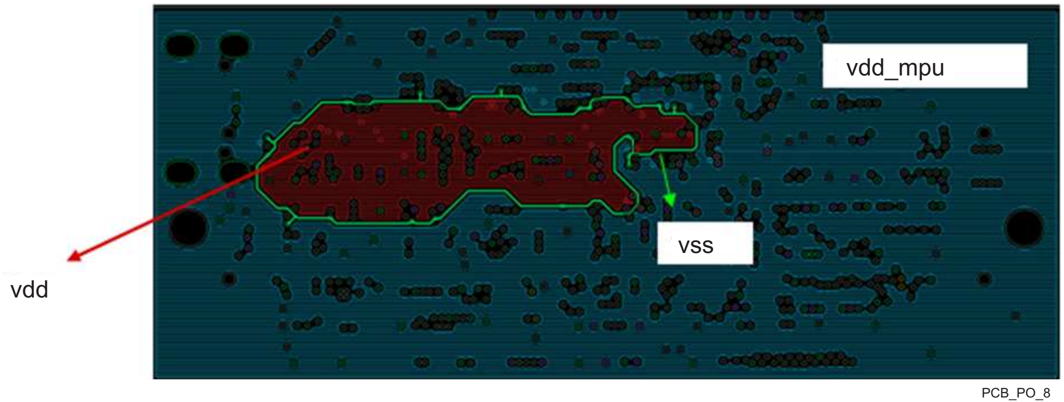

Figure 7-8. Coplanar Shielding of Power Net Using Ground Guard-band

7.2.3 Step 3: Static Analysis

Delivering reliable power to circuits is always of critical importance because voltage drops (also known as IR drops) can happen at every level within an electronic system, on-chip, within a package, and across the board. Robust system performance can only be ensured by understanding how the system elements will perform under typical stressful Use Cases. Therefore, it is a good practice to perform a Static or DC Analysis.

Static or DC analysis and design methodology results in a PDN design that minimizes voltage or IR drops across power and ground planes, traces and vias. This ensures the application processor's internal transistors will be operating within their specified voltage ranges for proper functionality. The amount of IR drop that will be encounter is based upon amount power drawn for a desired Use Case and PCB trace (widths, geometry and number of parallel traces) and via (size, type and number) characteristics.

Components that are distant from their power source are particularly susceptible to IR drop. Designs that rely on battery power must minimize voltage drops to avoid unacceptable power loss that can negatively impact system performance. Early assessments a PDN's static (DC) performance helps to determine basic power distribution parameters such as best system input power point, optimal PCB layer stackup, and copper area needed for load currents.

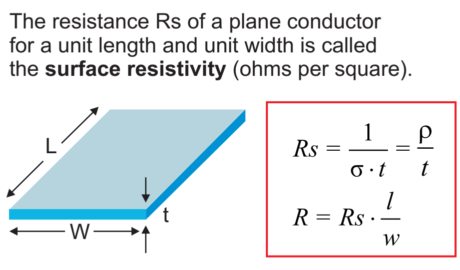

Figure 7-9. Depiction of Sheet Resistivity and Resistance

Ohm's Law (V = I × R) relates conduction current to voltage drop. At DC, the relation coefficient is a constant and represents the resistance of the conductor. Even current carrying conductors will dissipate power at high currents even though their resistance may be very small. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

Figure 7-10 shows a PCB-level static IR drop budget defined between the power management device (PMIC) pins and the application processor's balls when the PMIC is supplying power.

- It is highly recommended to physically place the PMIC as close as possible to the processor and on the same side. The orientation of the PMIC vs. processor should be aligned to minimize distance for the highest current rail.

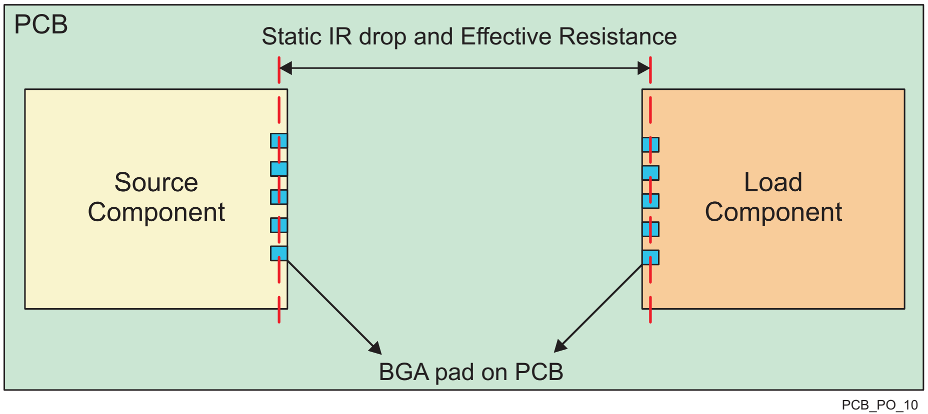

Figure 7-10. Static IR Drop Budget for PCB Only

The system-level IR drop budget is made up of three portions: on-chip, package, and PCB board. Static IR or DC analysis/design methodology consists of designing the PDN such that the voltage drop (under DC operating conditions) across power and ground pads of the transistors of the application processor device is within a specified value of the nominal voltage for proper functionality of the device.

A PCB system-level voltage drop budget for proper device functionality is typically 1.5 % of nominal voltage. For a 1.35-V supply, this would be ≤ 20 mV.

To accurately analyze PCB static IR drop, the actual geometry of the PDN must be modeled properly and simulated to accurately characterize long distribution paths, copper weight impacts, electro-migration violations of current-carrying vias, and “Swiss-cheese” effects via placement has on power rails. It is recommended to perform the following analyses:

- Lumped resistance/IR drop analysis
- Distributed resistance/IR drop analysis

NOTE

The PMIC companion device supporting Processor has been designed with voltage sensing feedback loop capabilities that enable a remote sense of the SMPS output voltage at the point of use.

The NOTE above means the SMPS feedback signals and returns must be routed across PCB and connected to the Device input power ball for which a particular SMPS is supplying power. This feedback loop provides compensation for some of the voltage drop encountered across the PDN within limits. As such, the effective resistance of the PDN within this loop should be determined in order to optimize voltage compensation loop performance. The resistance of two PDN segments are of interest: one from the power inductor/bulk power filtering capacitor node to the Processor’s input power and second is the entire PDN route from SMPS output pin/ball to the Processor input power.

In the following sections each methodology is described in detail and an example has been provided of analysis flow that can be used by the PCB designer to validate compliance to the requirements on their PCB PDN design.

7.2.3.1 PDN Resistance and IR Drop

Lumped methodology consists of grouping all of the power pins on both the PMIC (voltage source) and processor (current sink) devices. Then the PMIC source is set to an expected Use Case voltage level and the processor load has its Use Case current sink value set as well. Now the lumped/effective resistance for the power rail trace/plane routes can be determine based upon the actual layout’s power rail etch wide, shape, length, via count and placement Figure 7-11 illustrates the pin-grouping/lumped concept.

The lumped methodology consists of importing the PCB layout database (from Cadence Allegro tool or any other layout design tool) into the static IR drop modeling and simulation tool of preference for the PCB designer. This is followed by applying the correct PCB stack-up information (thickness, material properties) of the PCB dielectric and metallization layers. The material properties of dielectric consist of permittivity (Dk) and loss tangent (Df).

For the conductor layers, the correct conductivity needs to be programmed into the simulation tool. This is followed by pin-grouping of the power and ground nets, and applying appropriate voltage/current sources. The current and voltage information can be obtained from the power and voltage specifications of the device under different operating conditions / Use Cases.

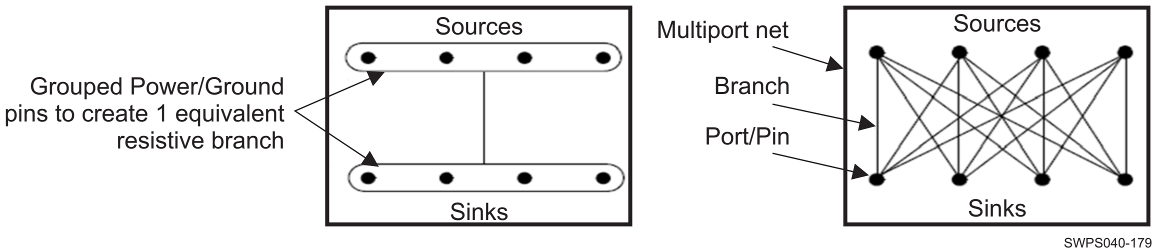

Figure 7-11. Pin-grouping concept: Lumped and Distributed Methodologies

7.2.4 Step 4: Frequency Analysis

Delivering low noise voltage sources are very important to allowing a system to operate at the lowest possible Operational Performance Point (OPP) for any one Use Case. An OPP is a combination of the supply voltage level and clocking rate for key internal processor domains. A SCH and PCB designed to provide low noise voltage supplies will then enable the processor to enter optimal OPPs for each Use Case that in turn will minimize power dissipation and junction temperatures on-die. Therefore, it is a good engineering practice to perform a Frequency Analysis over the key power domains.

Frequency analysis and design methodology results in a PDN design that minimizes transient noise voltages at the processor’s input power balls. This allows the processor’s internal transistors to operate near the minimum specified operating supply voltage levels. To accomplish this one must evaluate how a voltage supply will change due to impedance variations over frequency. This analysis will focus on the decoupling capacitor network (VDD_xxx and VSS/Gnd rails) at the load. Sufficient capacitance with a distribution of self-resonant points will provide for an overall lower impedance vs frequency response for each power domain.

Decoupling components that are distant from their load’s input power are susceptible to encountering spreading loop inductance from the PCB design. Early analysis of each key power domain’s frequency response helps to determine basic decoupling capacitor placement, optimal footprint, layer assignment, and types needed for minimizing supply voltage noise/fluctuations due to switching and load current transients.

NOTE

Evaluation of loop inductance values for decoupling capacitors placed ~300 mils closer to the load’s input power balls has shown an 18 % reduction in loop inductance due to reduced distance.

- Decoupling capacitors must be carefully placed in order to minimize loop inductance impact on supply voltage transients. A real capacitor has characteristics not only of capacitance but also inductance and resistance.

  Figure 7-12 shows the parasitic model of a real capacitor. A real capacitor must be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).

Figure 7-12. Characteristics of a Real Capacitor With ESL and ESR

The magnitude of the impedance of this series model is given as:

$$|Z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2}$$

$$\text{where : } \quad \omega = 2\pi f$$

SWPS040-e002

Figure 7-13. Series Model Impedance Equation

Figure 7-14 shows the resonant frequency response of a typical capacitor with a self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance and reactive capacitance and inductance as shown in the equation above.

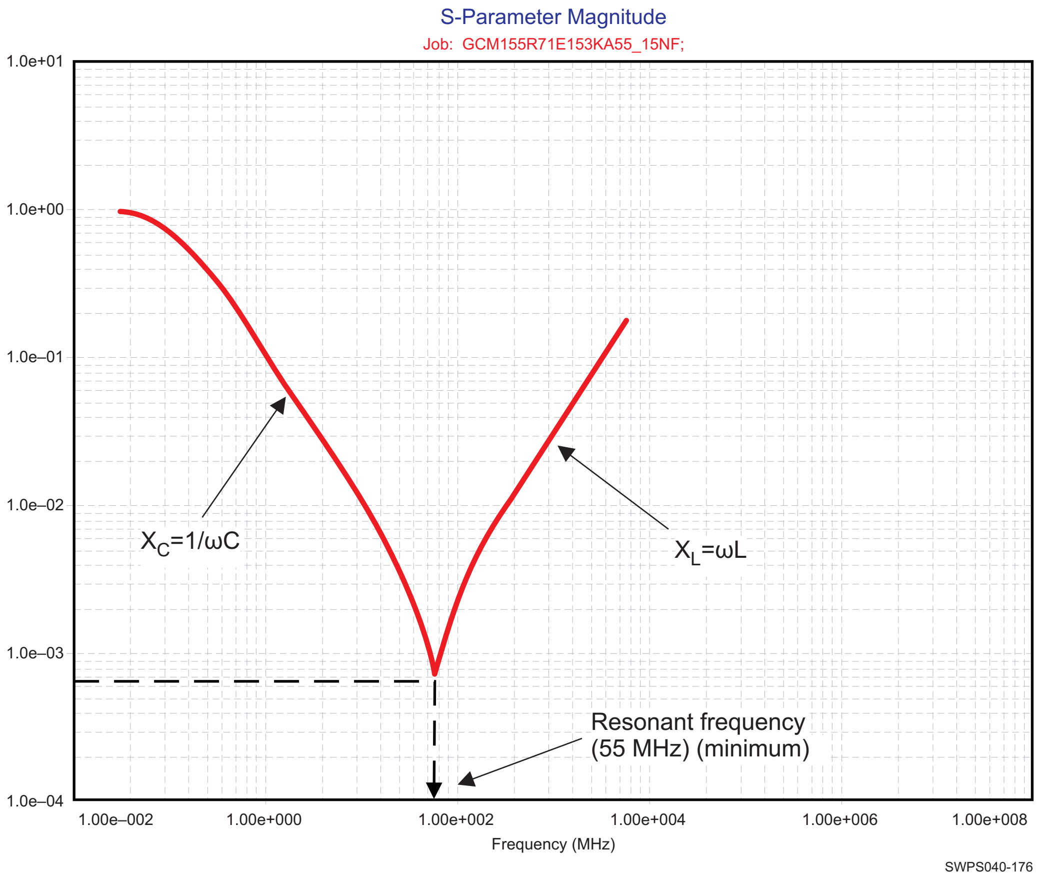

Figure 7-14. Typical Impedance Profile of a Capacitor

Because a capacitor has series inductance and resistance that impacts its effectiveness, it is important that the following recommendations are adopted in placing capacitors on the PDN.

Wherever possible, mount the capacitor with the geometry that minimizes the mounting inductance and resistance. This was shown earlier in Figure 7-1. The capacitor mounting inductance and resistance values include the inductance and resistance of the pads, trace, and vias. Whenever possible, use footprints that have the lowest inductance configuration as shown in Figure 7-15

The length of a trace used to connect a capacitor has a big impact on parasitic inductance and resistance of the mounting. This trace must be as short and as wide as possible. wherever possible, minimize distance to supply and Gnd vias by locating vias nearby or within the capacitor's solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or doubling the number of vias as shown in Figure 7-15. If the PCB manufacturing processes allow it and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up. Therefore, try to minimize X, Y and Z dimensions where the Z is due to PCB thickness (as shown in Figure 7-2).

From left (highest inductance) to right (lowest inductance) the capacitor footprint types shown in Figure 7-15 are known as:

- 2-via, Skinny End Exit (2vSEE)
- 2-via, Wide End Exit (2vWEE)
- 2-via, Wide Side Exit (2vWSE)
- 4-via, Wide Side Exit (4vWSE)
- 2-via, In-Pad (2vIP)

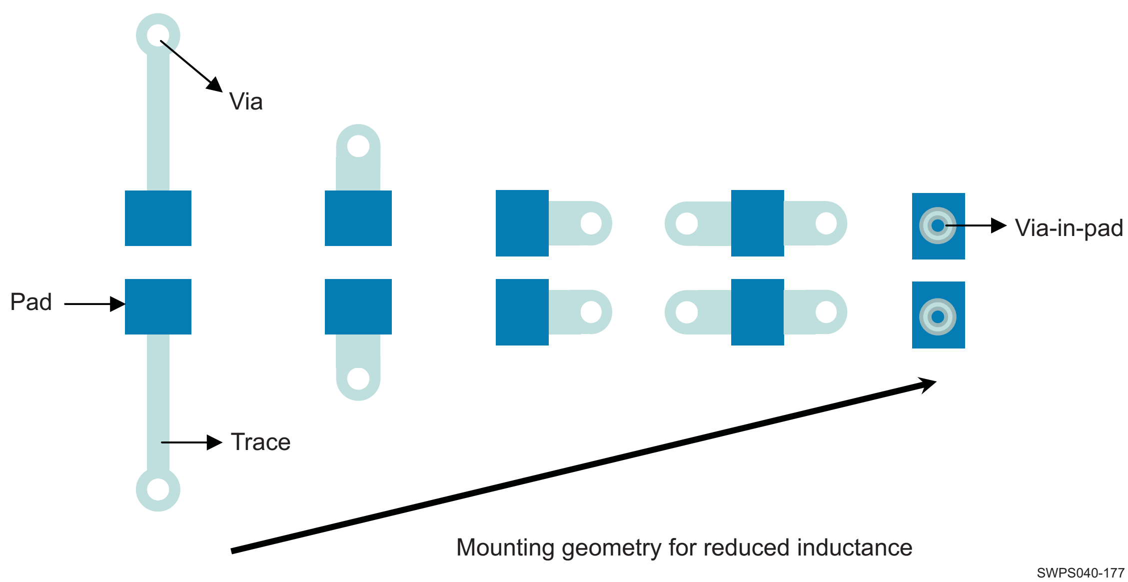

Figure 7-15. Capacitor Placement Geometry for Improved Mounting Inductance

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NOTE

Evaluation of loop inductance values for decoupling capacitor footprints 2vSEE (worst case) vs 4vWSE (2nd best) has shown a 30 % reduction in inductance when 4vWSE footprint was used in place of 2vSEE.

Decoupling Capacitor (Dcap) Strategy:

1. Use lowest inductance footprint and trace connection scheme possible for given PCB technology and layout area in order to minimize Dcap loop inductance to power pin as much as possible (see Figure 7-15).
2. Place Dcaps on "same-side" as component within their power plane outline to minimize "decoupling loop inductance". Target distance to power pin should be less than ~500 mils depending upon PCB layout characteristics (plane's layer assignment and solid nature). Use PI modeling CAD tool to verify

minimum inductance for top vs bottom-side placement.

3. Place Dcaps on "opposite-side" as component within their power plane outline if "same-side" is not feasible or if distance to power pin is greater than ~500 mils for top-side location. Use PI modeling CAD tool to verify minimum inductance for top vs bottom-side placement.
4. Use minimum 10mil trace width for all voltage and gnd planes connections (i.e. Dcap pads, component power pins, etc.).
5. Place all voltage and gnd plane vias "as close as possible" to point of use (i.e. Dcap pads, component power pins, etc.).
6. Use a "Power/Gnd pad/pin to via" ratio of 1:1 whenever possible. Do not exceed 2:1 ratio for small number of vias within restricted PCB areas (i.e. underneath BGA components).

Frequency analysis for the MPU power domain has yielded the vdd_mpu Impedance vs Frequency response shown in Section 7.3.8.2, vdd_mpu Example Analysis. As the example shows the overall MPU PDN R_{eff} meets the maximum recommended PDN resistance of 10 mΩ.

7.2.5 System ESD Generic Guidelines

7.2.5.1 System ESD Generic PCB Guideline

Protection devices must be placed close to the ESD source which means close to the connector. This allows the device to subtract the energy associated with an ESD strike before it reaches the internal circuitry of the application board.

To help minimize the residual voltage pulse that will be built-up at the protection device due to its nonzero turn-on impedance, it is mandatory to route the ESD device with minimum stub length so that the low-resistive, low-inductive path from the signal to the ground is granted and not increasing the impedance between signal and ground.

For ESD protection array being railed to a power supply when no decoupling capacitor is available in close vicinity, consider using a decoupling capacitor (≥ 0.1 µF) tight to the VCC pin of the ESD protection. A positive strike will be partially diverted to this capacitance resulting in a lower residual voltage pulse.

Ensure that there is sufficient metallization for the supply of signals at the interconnect side (VCC and GND in Figure 7-16) from connector to external protection because the interconnect may see between 15-A to 30-A current in a short period of time during the ESD event.

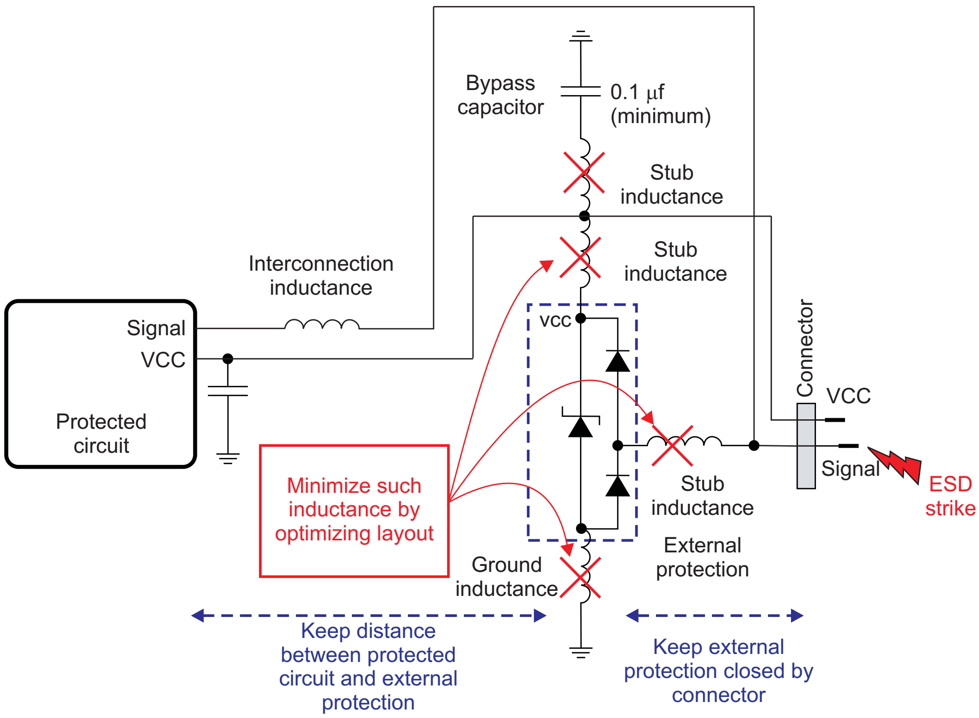


Figure 7-16. Placement Recommendation for an ESD External Protection

NOTE

To ensure normal behavior of the ESD protection (unwanted leakage), it is better to ground the ESD protection to the board ground rather than any local ground (example isolated shield or audio ground).

7.2.5.2 Miscellaneous EMC Guidelines to Mitigate ESD Immunity

- Avoid running critical signal traces (clocks, resets, interrupts, control signals, and so forth) near PCB edges.
- Add high frequency filtering: Decoupling capacitors close to the receivers rather than close to the drivers to minimize ESD coupling.
- Put a ground (guard) ring around the entire periphery of the PCB to act as a lightning rod.
- Connect the guard ring to the PCB ground plane to provide a low impedance path for ESD-coupled current on the ring.
- Fill unused portions of the PCB with ground plane.
- Minimize circuit loops between power and ground by using multilayer PCB with dedicated power and ground planes.
- Shield long line length (strip lines) to minimize radiated ESD.
- Avoid running traces over split ground planes. It is better to use a bridge connecting the two planes in one area.

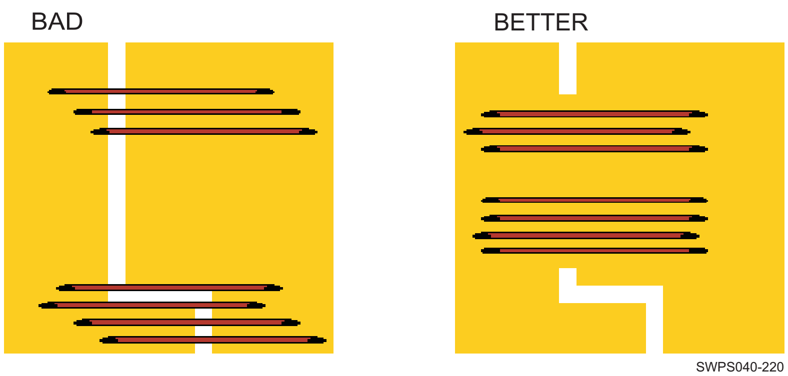


Figure 7-17. Trace Examples

- Always route signal traces and their associated ground returns as close to one another as possible to minimize the loop area enclosed by current flow:
  – At high frequencies current follows the path of least inductance.
  – At low frequencies current flows through the path of least resistance.

7.2.6 EMI / EMC Issues Prevention

All high-speed digital integrated circuits can be sources of unwanted radiation, which can affect nearby sensitive circuitry and cause the final product to have radiated emissions levels above the limits allowed by the EMC regulations if some preventative steps are not taken.

Likewise, analog and digital circuits can be susceptible to interference from the outside world and picked up by the circuitry interconnections.

To minimize the potential for EMI/EMC issues, the following guidelines are recommended to be followed.

7.2.6.1 Signal Bandwidth

To evaluate the frequency of a digital signal, an estimated rule of thumb is to consider its bandwidth f_{BW} with respect to its rise time, t_R:

$f_{BW} \approx 0.35 / t_R$

This frequency actually corresponds to the break point in the signal spectrum, where the harmonics start to decay at 40 dB per decade instead of 20 dB per decade.

7.2.6.2 Signal Routing

7.2.6.2.1 Signal Routing—Sensitive Signals and Shielding

Keep radio frequency (RF) sensitive circuitry (like GPS receivers, GSM/WCDMA, Bluetooth/WLAN transceivers, frequency modulation (FM) radio) away from high-speed ICs (the device, power and audio manager, chargers, memories, and so forth) and ideally on the opposite side of the PCB. For improved protection it is recommended to place these emission sources in a shield can. If the shield can have a removable lid (two-piece shield), ensure there is low contact impedance between the fence and the lid. Leave some space between the lid and the components under it to limit the high-frequency currents induced in the lid. Limit the shield size to put any potential shield resonances above the frequencies of interest; see Figure 7-14, *Typical Impedance Profile of a Capacitor*.

7.2.6.2.2 Signal Routing—Outer Layer Routing

In case there is a need to use the outer layers for routing outside of shielded areas, it is recommended to route only static signals and ensure that these static signals do not carry any high-frequency components (due to parasitic coupling with other signals). In case of long traces, make provision for a bypass capacitor near the signal source.

Routing of high-frequency clock signals on outer layers, even for a short distance, is discouraged, because their emissions energy is concentrated at the discrete harmonics and can become significant even with poor radiators.

Coplanar shielding of traces on outer layers (placing ground near the sides of a track along its length) is effective only if the distance between the trace sides and the ground is smaller that the trace height above the ground reference plane. For modern multilayer PCBs this is often not possible, so coplanar shielding will not be effective. Do not route high-frequency traces near the periphery of the PCB, as the lack of a ground reference near the trace edges can increase EMI: see Section 7.2.6.3, *Ground Guidelines*.

7.2.6.3 Ground Guidelines

7.2.6.3.1 PCB Outer Layers

Ideally the areas on the top and bottom layers of the PCB that are not enclosed by a shield should be filled with ground after the routing is completed and connected with an adequate number of vias to the ground on the inner ground planes.

7.2.6.3.2 Metallic Frames

Ensure that all metallic parts are well connected to the PCB ground (like LCD screens metallic frames, antennas reference planes, connector cages, flex cables grounds, and so forth). If using flex PCB ribbon cables to bring high-frequency signals off the PCB, ensure they are adequately shielded (coaxial cables or flex ribbons with a solid reference ground).

7.2.6.3.3 Connectors

For high-frequency signals going to connectors choose a fully shielded connector, if possible (for example, SD card connectors). For signals going to external connectors or which are routed over long distances, it is recommended to reduce their bandwidth by using low-pass filters (resistor, capacitor (RC) combinations or lossy ferrite inductors). These filters will help to prevent emissions from the board and can also improve the immunity from external disturbances.

7.2.6.3.4 Guard Ring on PCB Edges

The major advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace.

As shown in Figure 7-18 the field lines of the signal return to PCB ground as long as an infinite ground is available.

Traces near the PCB-edges do not have this infinite ground and therefore may radiate more than the others. Thus, signals (clocks) or power traces (core power) identified to be critical must not be routed in the vicinity of PCB edges, or, if not avoidable, must be accompanied by a guard ring on the PCB edge.

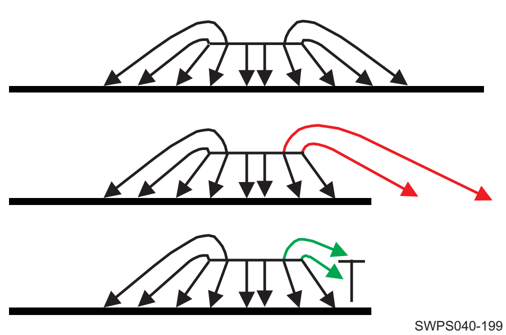


Figure 7-18. Field Lines of a Signal Above Ground

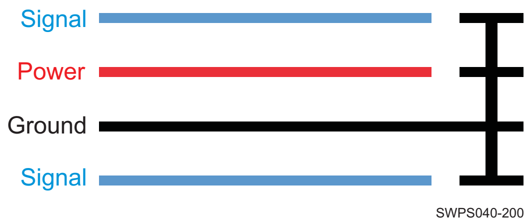


Figure 7-19. Guard Ring Routing

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) must be applied as shown in Figure 7-19.

As these traces must have the same (HF–) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

7.2.6.3.5 Analog and Digital Ground

For the optimum solution, the AGND and the DGND planes must be connected together at the power supply source in a same point. This ensures that both planes are at the same potential, while the transfer of noise from the digital to the analog domain is minimized.

7.3 Core Power Domains

This section provides boundary conditions and theoretical background to be applied as a guide for optimizing a PCB design. The decoupling capacitor and PDN characteristics tables shown below give recommended capacitors and PCB parameters to be followed for schematic and PCB designs. Board designs that meet the static and dynamic PDN characteristics shown in tables below will be aligned to the expected PDN performance needed to optimize SoC performance.

7.3.1 General Constraints and Theory

- Max PCB static/DC voltage drop (IRd) budget can be relaxed to **7.5 % of supply voltage** when using PMICs **with remote sensing at the load** as measured from PMIC's power inductor and filter capacitor node to Device's supply input including any ground return losses. TI highly recommends remote sensing.
- Max PCB static/DC voltage drop (IRd) budget of **1.5 % of supply voltage** when using PMICs **without remote sensing** as measured from PMIC's power inductor and filter capacitor node to Processor input including any ground return losses.
- PMIC component DM and guidelines should be referenced for the following:
  - Routing remote feedback sensing to optimize per each SMPS's implementation
  - Selecting power filtering capacitor values and PCB placement.
- Max Effective Resistance (Reff) budget can range from **4 mΩ – 100 mΩ** for key Device power rails not including ground returns depending upon maximum load currents and maximum DC voltage drop budget (as discussed above).
- Max Device supply input voltage difference budget of **5 mV** under max current loading shall be maintained across all balls connected to a common power rail. This represents any voltage difference that may exist between a remote sense point to any power input.
- Max PCB Loop Inductance (LL) budget between Device's power inputs and local bulk and high frequency decoupling capacitors including ground returns should range from **0.4 nH – 2.5 nH depending upon maximum transient load currents.**

- Max PCB dynamic/AC peak-to-peak transient noise voltage budgets between PMIC and Device including ground returns are as follows:
  - **+/-3 % of nominal supply voltage** for frequencies below the PMIC bandwidth (typ Fpmic ~ 200 kHz)
  - **+/-5 % of nominal supply voltage** for frequencies between Fpmic to Fpcb (typ 20 MHz – 100 MHz)
- Max PCB Impedance (Z) vs Frequency (F) budget between Device's power inputs and PMIC's output power filter node including ground return is determined by applying the Frequency Domain Target Impedance Method to determine the PCB's maximum frequency of interest (Fpcb). Ideally a properly designed and decoupled PDN will exhibit smoothly increasing Z vs. F curve. There are 2 general regions of interest as can be seen in Figure 7-20.
  - 1st area is from DC (0 Hz) up to Fpmic (typ a few 100 kHz) where a PMIC's transient response characteristic (i.e. Switching Freq, Compensation Loop BW) dominate. A PDN's Z is typically very low due to power filtering and bulk capacitor values when PDN has very low trace resistance (i.e. good Reff performance). The goal is to maintain a smoothly increasing Z that is less than Zt1 over this low frequency range. This will ensure that a max transient current event will not cause a voltage drop more than the PMIC's current step response can support (typ 3 %).
  - 2nd area is from Fpmic up to Fpcb (typ 20 MHz – 100 MHz) where a PCB's inherent characteristics (i.e. parasitic capacitance, planar spreading inductances) dominate. A PDN's Z will naturally increase with frequency. At frequencies between Fpmic up to Fpcb, the goal is to maintain a smoothly increasing Z to be less than Zt2. This will ensue that the high frequency content of a max transient current event will not cause a voltage drop to be more than 5 % of the min supply voltage.

$$Z_T = \frac{\text{Max Voltage Rail Drop}^{\text{Note1}}}{\text{Max Transient Current}^{\text{Note2}}}$$

$$Z_{T1} = \frac{\text{(Min Voltage) x (PMIC's Step Responce)}}{\text{(\textasciitilde 50\% of Max DC Current)}} = \frac{\text{Vmin x 3\%(typ)}}{\text{Imax x \textasciitilde 50\%}}$$

$$Z_{T2} = \frac{\text{(Min Voltage) x (High-Freq Transient Noise)}}{\text{(\textasciitilde 50\% of Max DC Current)}} = \frac{\text{Vmin x 5\%(typ)}}{\text{Imax x \textasciitilde 50\%}}$$

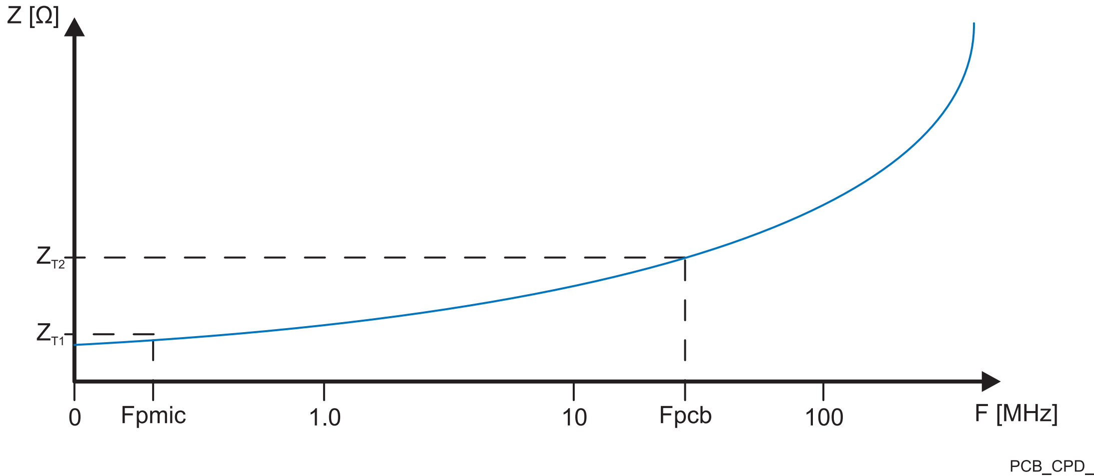


Figure 7-20. PDN's Target impedance

1.Voltage Rail Drop includes regulation accuracy, voltage distribution drops, and all dynamic events such as transient noise, AC ripple, voltage dips etc.

2.Typical max transient current is defined as 50 % of max current draw possible.

7.3.2 Voltage Decoupling

Recommended power supply decoupling capacitors main characteristics for commercial products whose ambient temperature is not to exceed +85C are shown in table below:

Table 7-1. Commercial Applications Recommended Decoupling Capacitors Characteristics[(1)(2)(3)]

Value	Voltage [V]	Package	Stability	Dielectric	Capacitance Tolerance	Temp Range [°C]	Temp Sensitivity [%]	REFERENCE
22 µF	6,3	0603	Class 2	X5R	- / + 20 %	-55 to + 85	- / + 15	GRM188R60J226MEA0L
10 µF	4,0	0402	Class 2	X5R	- / + 20 %	-55 to + 85	- / + 15	GRM155R60G106ME44
4.7 µF	6,3	0402	Class 2	X5R	- / + 20 %	-55 to + 85	- / + 15	GRM155R60J475ME95
2.2 µF	6,3	0402	Class 2	X5R	- / + 20 %	-55 to + 85	- / + 15	GRM155R60J225ME95
1 µF	6,3	0201	Class 2	X5R	- / + 20 %	-55 to + 85	- / + 15	GRM033R60J105MEA2

Table 7-1. Commercial Applications Recommended Decoupling Capacitors Characteristics(1)(2)(3) (continued)

Value	Voltage [V]	Package	Stability	Dielectric	Capacitance Tolerance	Temp Range [°C]	Temp Sensitivity [%]	REFERENCE
470 nF	6,3	0201	Class 2	X5R	- / + 20 %	-55 to + 85	- / + 15	GRM033R60G474ME90
220 nF	6,3	0201	Class 2	X5R	- / + 20 %	-55 to + 85	- / + 15	GRM033R60J224ME90
100 nF	6,3	0201	Class 2	X5R	- / + 20 %	-55 to + 85	- / + 15	GRM033R60J104ME19

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

(3) In comparison with the EIA Class 1 dielectrics, Class 2 dielectric capacitors tend to have severe temperature drift, high dependence of capacitance on applied voltage, high voltage coefficient of dissipation factor, high frequency coefficient of dissipation, and problems with aging due to gradual change of crystal structure. Aging causes gradual exponential loss of capacitance and decrease of dissipation factor.

Recommended power supply decoupling capacitors main characteristics for automotive products are shown in table below:

Table 7-2. Automotive Applications Recommended Decoupling Capacitors Characteristics (1)(2)

Value	Voltage [V]	Package	Stability	Dielectric	Capacitance Tolerance	Temp Range [°C]	Temp Sensitivity [%]	REFERENCE
22 µF	6,3	1206	Class 2	X7R	- / + 20 %	-55 to + 125	- / + 15	GCM31CR70J226ME23
10 µF	6,3	0805	Class 2	X7R	- / + 20 %	-55 to + 125	- / + 15	GCM21BR70J106ME22
4.7 µF	10	0805	Class 2	X7R	- / + 20 %	-55 to + 125	- / + 15	GCM21BC71A475MA73
2.2 µF	6,3	0603	Class 2	X7R	- / + 20 %	-55 to + 125	- / + 15	GCM188R70J225ME22
1 µF	16	0603	Class 2	X7R	- / + 20 %	-55 to + 125	- / + 15	GCM188R71C105MA64
470 nF	16	0603	Class 2	X7R	- / + 20 %	-55 to + 125	- / + 15	GCM188R71C474MA55
220 nF	25	0603	Class 2	X7R	- / + 20 %	-55 to + 125	- / + 15	GCM188L81C224MA37
100 nF	16	0402	Class 2	X7R	- / + 20 %	-55 to + 125	- / + 15	GCM155R71C104MA55

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

7.3.3 Static PDN Analysis

One power net parameter derived from a PCB's PDN static analysis is the Effective Resistance (Reff). This is the total PCB power net routing resistance that is the sum of all the individual power net segments used to deliver a supply voltage to the point of load and includes any series resistive elements (i.e. current sensing resistor) that may be installed between the PMIC outputs and Processor inputs

7.3.4 Dynamic PDN Analysis

Three power net parameters derived from a PCB's PDN dynamic analysis are the Loop Inductance (LL), Impedance (Z) and PCB Frequency of Interest (Fpcb).

- LL values shown are the recommended max PCB trace inductance between a decoupling capacitor's power supply and ground reference terminals when viewed from the decoupling capacitor with a "theoretical shorted" applied across the Processor's supply inputs to ground reference.
- Z values shown are the recommended max PCB trace impedances allowed between Fpmic up to Fpcb frequency range that limits transient noise drops to no more than 5 % of min supply voltage during max transient current events.
- Fpcb (Frequency of Interest) is defined to be a power rail's max frequency after which adding a reasonable number of decoupling capacitors no longer significantly reduces the power rail impedance below the desired impedance target (Zt2). This is due to the dominance of the PCB's parasitic planar spreading and internal package inductances.

Table 7-3. Recommended PDN Characteristics and EVM Decoupling Capacitors [(1)(2)(3)(4)(5)]

PDN Analysis:	Static	Dynamic			EVM Decoupling Capacitor Scheme per Supply[(6)]							
Supply	Max R_{eff} [(7)] [mΩ]	Max Dec. Cap. LL [nH]	Max Impedance[(8)] [mΩ]	Frequency of Interest [MHz]	100 nF	220 nF	470 nF	1µF	2.2 µF	4.7 µF	10 µF	22 µF
vdd_mpu	18	2	57	20	12	2	2	3	1	1		1
vdd_dspeve	22	2.5	54	20	8	1	1	2	1	1	1	
vdd	32	2	87	50	6	1	1	1	1	1		
vdd_gpu	22	2.5	207	50	6	1	1	1	1	1		
vdd_iva	48	2	800	100	5		1			1		
vdds_ddr1	18	2.5	200	100	8	4		2		2		1
vdds_ddr2	18	2.5	200	100	8	4		2		2		1
cap_vbbldo_dspeve	N/A	6	N/A	N/A				1				
cap_vbbldo_gpu	N/A	6	N/A	N/A				1				
cap_vbbldo_iva	N/A	6	N/A	N/A				1				
cap_vbbldo_mpu	N/A	6	N/A	N/A				1				
cap_vddram_core1	N/A	6	N/A	N/A				1				
cap_vddram_core2	N/A	6	N/A	N/A				1				
cap_vddram_core3	N/A	6	N/A	N/A				1				
cap_vddram_core4	N/A	6	N/A	N/A				1				
cap_vddram_core5	N/A	6	N/A	N/A				1				
cap_vddram_dspeve1	N/A	6	N/A	N/A				1				
cap_vddram_dspeve2	N/A	6	N/A	N/A				1				
cap_vddram_gpu	N/A	6	N/A	N/A				1				
cap_vddram_iva	N/A	6	N/A	N/A				1				
cap_vddram_mpu1	N/A	6	N/A	N/A				1				
cap_vddram_mpu2	N/A	6	N/A	N/A				1				

(1) For more information on peak-to-peak noise values, see the Recommended Operating Conditions table of the Specifications chapter.
(2) ESL must be as low as possible and must not exceed 0.5 nH.
(3) The PDN (Power Delivery Network) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the Recommended Operating Conditions table of the Specifications chapter.
(4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
(5) Assuming that the external SMPS (power IC) feedback sense is taken close to processor power balls.
(6) Decoupling capacitor (Dcap) scheme optimized for EVM PCB design. Each PCB design could have a different optimal Dcap scheme depending upon stackup, routing, placement and Dcap footprint to via connections.
(7) Maximum R_{eff} from SMPS to Processor.
(8) Maximum impedance value at the Frequency of Interest and below.

NOTE

For power IC which can support more than 10 µF close to processor, a bulk capacitor of at least 22 µF is strongly recommended for VDD_MPU power domains.

7.3.5 *Power Supply Mapping*

TPS65917 and LP87565 are the Power Management ICs (PMICs) that are used on the TI EVM. TI recommends use of these PMICs on customer designs for the following reasons:

- TI has validated their use with the Device
- Board level margins including transient response and output accuracy are analyzed and optimized for the entire system
- Support for power sequencing requirements (refer to Section 5.10.3 *Power Supply Sequences*)

- Support for Adaptive Voltage Scaling (AVS) Class 0 requirements, including TI provided software

Other PMIC combinations have been analyzed and are recommended by TI in order to optimize for particular use cases. These options require additional analysis and validation to be performed by the customer. Contact your TI representative for additional details. In all cases, the customer's specific use case power estimate should be analyzed, and confirmed to be supported for any chosen implementation.

If multiple SoC voltage domains are allowed to be combined into a common board power rail, the most stringent recommended PDN guidelines (Table 7-3) should be applied to the common power rail.

It is possible that some voltage domains on the device are unused in some systems. In such cases, to ensure device reliability, it is still required that the supply pins for the specific voltage domains are connected to some core power supply output.

These unused supplies though can be combined with any of the core supplies that are used (active) in the system. For example: if IVA and GPU domains are not used, they can be combined with the CORE domain, thereby having a single power supply driving the combined CORE, IVA and GPU domains.

For the combined rail, the following relaxations do apply:

- The AVS voltage of active rail in the combined rail needs to be used to set the power supply
- The decoupling capacitance should be set according to the active rail in the combined rail

7.3.6 DPLL Voltage Requirement

The voltage input to the DPLLs has a low noise requirement. Board designs should supply these voltage inputs with a low noise LDO to ensure they are isolated from any potential digital switching noise. The TPS65917 and TPS659039 PMIC LDOLN outputs are specifically designed to meet this low noise requirement.

NOTE

For more information about Input Voltage Sources, see Section 5.10.4.4, *DPLLs, DLLs Specifications*.

---

present the voltage inputs that supply the DPLLs.

Table 7-4. Input Voltage Power Supplies for the DPLLs

POWER SUPPLY	DPLLs
vdda_abe_per	DPLL_PER, DPLL_ABE and PER HSDIVIDER analog power supply
vdda_ddr	DPLL_DDR and DDR HSDIVIDER analog power supply
vdda_debug	DPLL_DEBUG analog power supply
vdda_dsp_eve	DPLL_DSP and DPLL_EVE analog power supply
vdda_gmac_core	DPLL_CORE and HSDIVIDER analog power supply
vdda_gpu	DPLL_GPU analog power supply
vdda_iva	DPLL_IVA analog power supply
vdda_video	DPLL_VIDEO1 and DPLL_VIDEO2 analog power supply
vdda_mpu	DPLL_MPU analog power supply
vdda_osc	not DPLL input but is required to be supplied by low noise input voltage

7.3.7 Loss of Input Power Event

A few key PDN design items needed to enable a controlled and compliant SoC power down sequence for a "Loss of Input Power" event are:

- “Loss of Input Power” early warning.
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using the First Stage Converter’s (i.e. LM536033-Q1) Power Good status output to enable and disable the Second Stage PMIC devices (i.e. TPS65917/919, LP8733, and LP8732). If a different First Stage Converter is used, care must be taken to ensure an adequate “PG_Status” or “Vbatt_Status” signal is provided that can disable Second Stage PMIC to begin a controlled and compliant SoC power down sequence. The total elapsed time from asserting “PG_Status” low until SoC’s PMIC input voltage reaches minimum level of 2.75 V should be minimum of 1.5 ms and 2 ms preferred.
- Maximize discharge time of First Stage Vout (VSYS_3V3 power rail = input voltage to SoC PMIC).
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by opening an in-line load switch immediately upon “PG_Status” low assertion in order to remove the SoC’s 3.3 V IO load current from VSYS_3V3. This will extend the VSYS_3V3 power rail’s discharge time in order to maximize elapsed time for allowing SoC PMIC to execute a controlled and compliant power down sequence. Care should be taken to either disable or isolate any additional peripheral components that may be loading the VSYS_3V3 rail as well.
- Sufficient bulk decoupling capacitance on the First Stage Vout (VSYS_3V3 per PDN) that allows for desired 1.5 – 2 ms elapsed time as described above.
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using 200 μF of total capacitance on VSYS_3V3. The First Stage Converter (i.e. LM536033-Q1) can typically drive a max of 400 μF to help extend VSYS_3V3 discharge time for a compliant SoC power down sequence.
- Optimizing the Second Stage SoC PMIC’s OTP settings that determines SoC power up and down sequences and total elapsed time needed for a controlled sequence.
  - TI EVM and Reference Design Study SCHs and PDNs achieve this by using optimized OTPs per the SCH and components used. The definition of these OTPs is captured in the detailed timing diagrams for both power up and down sequences. The PDN diagram typically shows a recommended PMIC OTP ID based upon the SoC and DDR memory types.

7.3.8 *Example PCB Design*

The following sections describe an example PCB design and its resulting PDN performance for the vdd_mpu key processor power domain.

7.3.8.1 Example Stack-up

Layer Assignments:

- Layer Top: Signal and Segmented Power Plane
  - Processor and PMIC components placed on Top-side
- Layer 2: Gnd Plane1
- Layer 3: Signals
- Layer n: Power Plane1
- Layer n+1: Power Plane 2
- Layer n+2: Signal
- Layer n+3: Gnd Plane2
- Layer Bottom: Signal and Segmented Power Planes
  - Decoupling caps, etc.

Via Technology: Through-hole

Copper Weight:

- ½ oz for all signal layers.
- 1-2oz for all power plane for improved PCB heat spreading.
- Total PCB Thickness 0.080 inches.

7.3.8.2 vdd_mpu Example Analysis

Maximum acceptable PCB resistance (R_{eff}) between the PMIC and Processor input power balls should not exceed 10 mΩ.

Maximum decoupling capacitance loop inductance (LL) between Processor input power balls and decoupling capacitances should not exceed 2.0 nH (ESL NOT included)

Impedance target for key frequency of interest between Processor input power balls and PMIC’s SMPS output power balls should not exceed 57 mΩ at 20 MHz.

Table 7-5. Example PCB vdd_mpu PI Analysis Summary

Parameter	Recommendation	Example PCB
Processor OPP	High	
Clocking Rate	1.5 GHz	
Voltage Level	1.22 V	1.22 V
Max Current Draw	5.12 A	5.12 A
Max Effective Resistance: Power Inductor Segment Total R_{eff}	10 mΩ	9.0 mΩ
Max Loop Inductance	2.0 nH	1.0 nH – 1.4 nH
Impedance Target	57 mΩ F < 20 MHz	57 mΩ F < 20 MHz

Figure 7-21, Figure 7-22, Figure 7-23, and Figure 7-24 show a PCB layout example and the resulting PI analysis results.

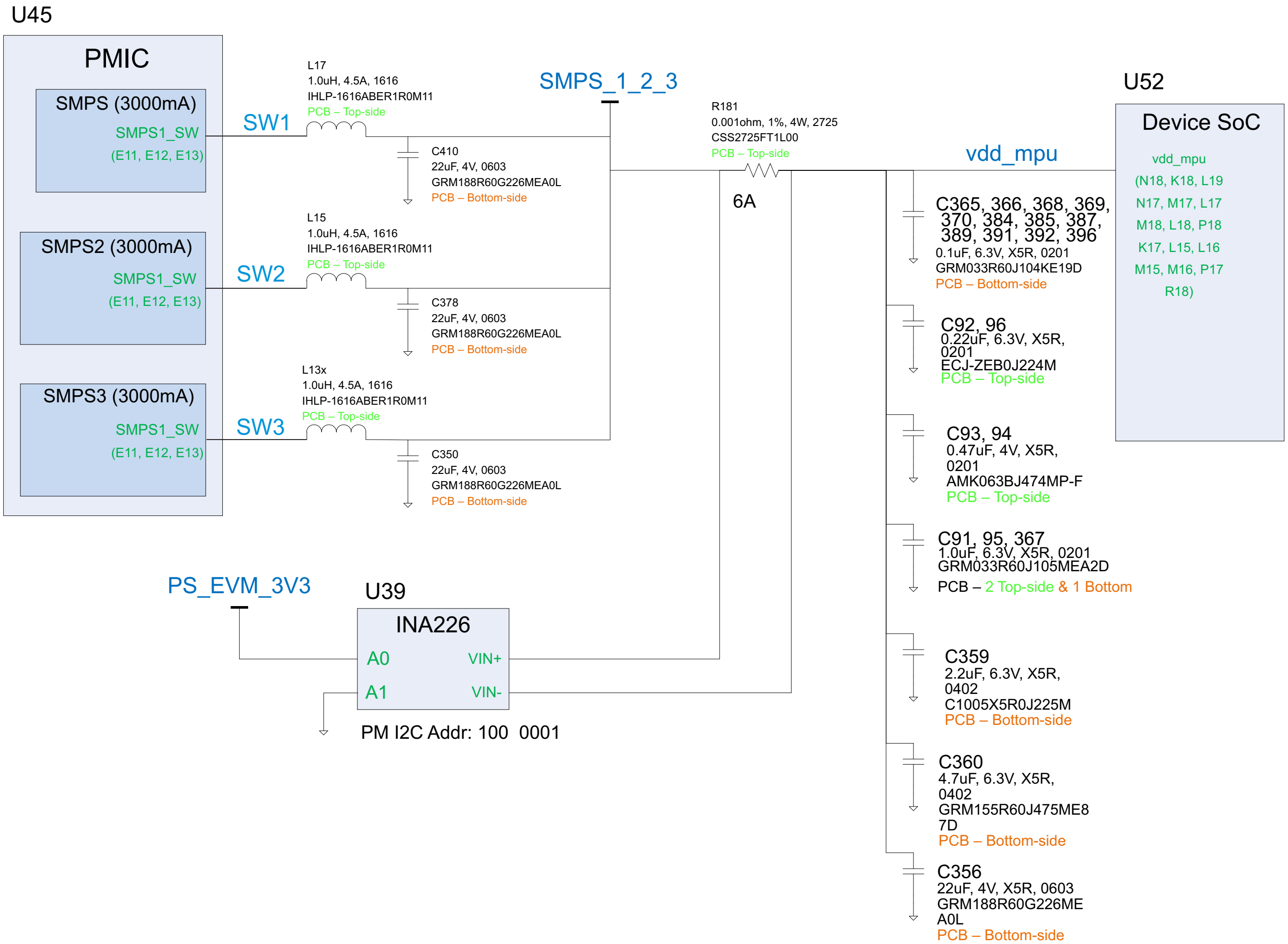


Figure 7-21. vdd_mpu Simplified SCH Diagram

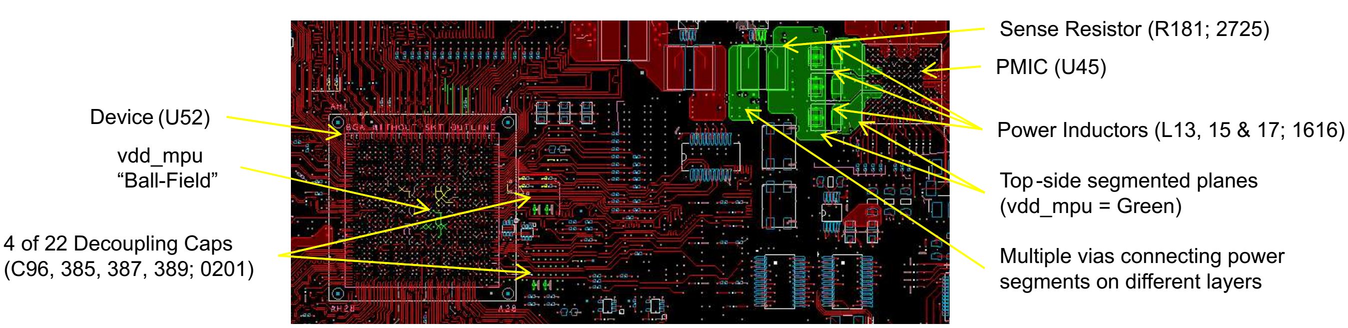


Figure 7-22. vdd_mpu routing [Top Layer]

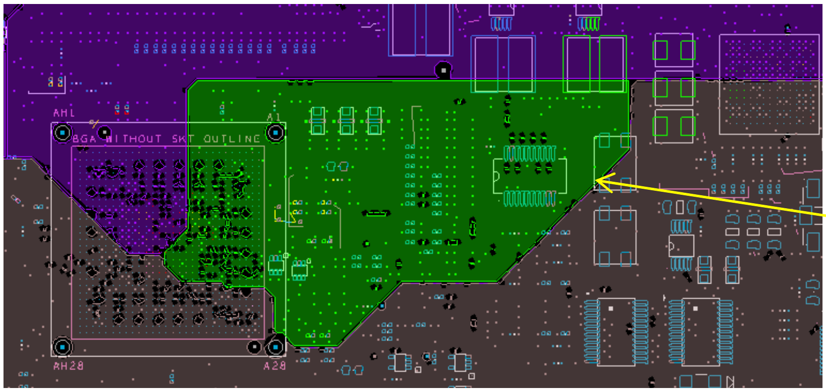


Figure 7-23. vdd_mpu routing [Internal Power Plane #2]

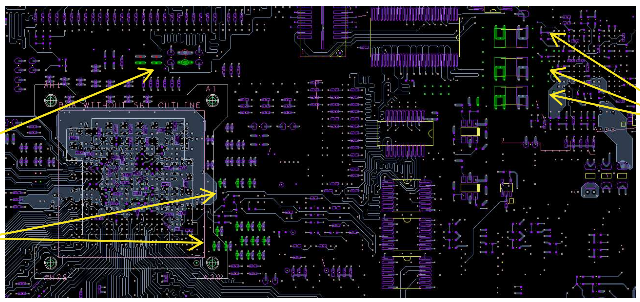


Figure 7-24. vdd_mpu routing and cap placements [Bottom Layer]

Table 7-6. PCB Etch Resistance Breakdown - From PMIC Source to Device Load

Net[from]	Component [from]:	Net[to]	Component [to]:	Etch Resistance (Ω)	% of Total Etch Resistance
SW1	L17	SW1	U45	0,001038	13 %
SW2	L15	SW2	U45	0,000898	12 %
SW3	L13	SW3	U45	0,000861	11 %
SW1	L17	SMPS_1_2_3	R181	0,000696	9 %
SW2	L15	SMPS_1_2_3	R181	0,000541	7 %
SW3	L13	SMPS_1_2_3	R181	0,000526	7 %
vdd_mpu	R181	vdd_mpu	U52	0,006311	78 %
vdd_mpu	R181	vdd_mpu	U52	0,006311	81 %
vdd_mpu	R181	vdd_mpu	U52	0,006311	82 %
			Total Etch Resistance from SW1 =	**0,008045**	**100 %**
			Total Etch Resistance from SW2 =	**0,00775**	**100 %**
			Total Etch Resistance from SW3 =	**0,007698**	**100 %**
			Max Value =	**0,008045**	

Table 7-7. PCB Etch Resistance Breakdown - From Power Inductor to Device Load

Net[from]	Component [from]:	Net[to]	Component [to]:	Etch Resistance (Ω)	% of Total Etch Resistance
SMPS_1_2_3	L17	SMPS_1_2_3	R181	0,000696	10 %
SMPS_1_2_3	L15	SMPS_1_2_3	R181	0,000541	8 %
SMPS_1_2_3	L13	SMPS_1_2_3	R181	0,000526	8 %

Table 7-7. PCB Etch Resistance Breakdown - From Power Inductor to Device Load (continued)

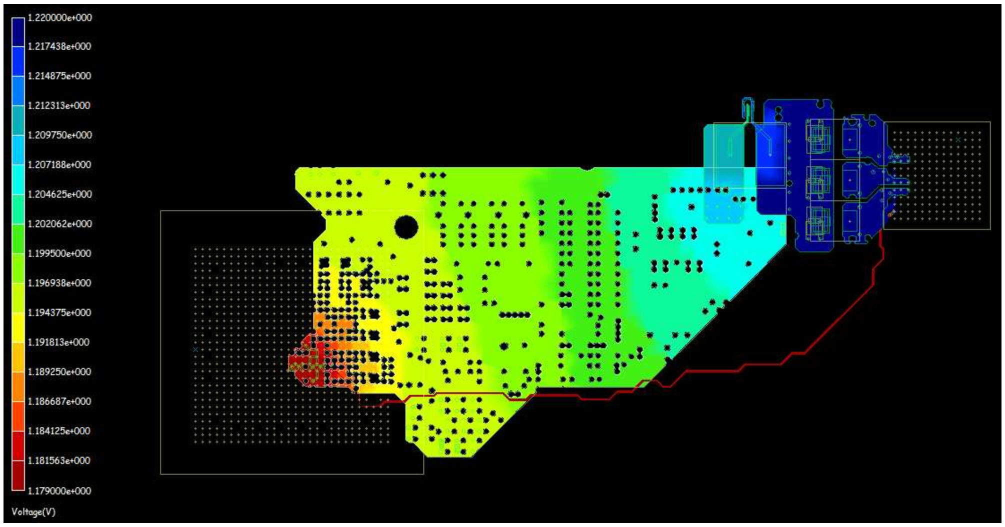
Net[from]	Component [from]:	Net[to]	Component [to]:	Etch Resistance (Ω)	% of Total Etch Resistance
vdd_mpu	R181	vdd_mpu	U52	0,006311	90 %
vdd_mpu	R181	vdd_mpu	U52	0,006311	92 %
vdd_mpu	R181	vdd_mpu	U52	0,006311	92 %
			Total Etch Resistance =	**0,007007**	**100 %**
			Total Etch Resistance =	**0,006852**	**100 %**
			Total Etch Resistance =	**0,006837**	**100 %**
			Max Value =	**0,007007**	

Table 7-8. PDN Effective Resistance - From PMIC Source to Device Load

PDN Elements	PDN Effective Resistance (Ω)	% of Total Etch Resistance
Etch	0,008045	89 %
Inductor	0	0 %
Sense Resistor	0,001	11 %
Max PDN Effectiv Resistance from Source	**0,009045**	**100 %**

IR Drop: vdd_mpu (PCB RevJan14, Sentinel PSI)

- Source Conditions: 1.22 V @ 5,12 A
- Recommended R_{eff} < 10 mΩ
- R_{eff} = Total Trace Resistance + Sence Resistor = 8,0 4mΩ + 1 mΩ = 9,04 mΩ
- Voltage / IR Drop: 1,22 - 1,179 = 52,6 mV



PCB_CPD_5

Figure 7-25. vdd_mpu Voltage/IR Drop [All Layers]

Dynamic analysis of this PCB design for the MPU power domain determined the vdd_mpu decoupling capacitor loop inductance and impedance vs frequency analysis shown below. As you can see, the loop inductance values ranged from 1.0 nH to 1.4 nH and were less than maximum 2.0 nH recommended.

NOTE

Comparing loop inductances for capacitors at different distances from the processor's input power balls shows an 18 % reduction for caps placed closer. This was derived by averaging the inductances for the 3 caps with distances over 800 mils (Avg LL = 1.33 nH) vs the 3 caps with distances less than 600 mils (Avg LL = 1.096 nH).

Table 7-9. Rail - vdd_mpu

Cap Ref Des	Model Port #	Loop Inductacne [nH]	Footprint Types	PCB Side	Distance to Ball-Field [mils]	Value [µF]	Size
C356	1	1,4	4vWSE	Bottom	897	22	0603
C359	2	1,26	4vWSE	Bottom	855	2,2	0402
C360	3	1,33	4vWSE	Bottom	850	4,7	0402
C365	4	1,14	4vWSE	Bottom	817	0,1	0201
C366	5	1,13	4vWSE	Bottom	755	0,1	0201
C367	6	1,07	4vWSE	Bottom	758	1	0201
C368	7	1,12	4vWSE	Bottom	811	0,1	0201
C369	8	1,06	4vWSE	Bottom	690	0,1	0201
C370	9	1,12	4vWSE	Bottom	680	0,1	0201
C384	10	1,04	4vWSE	Bottom	686	0,1	0201
C385	11	1,07	4vWSE	Top	686	0,1	0201
C387	12	1,16	4vWSE	Top	755	0,1	0201
C389	13	1,18	4vWSE	Top	693	0,1	0201
C391	14	1,14	4vWSE	Bottom	693	0,1	0201
C392	15	1,18	4vWSE	Bottom	542	0,1	0201
C396	16	1,11	4vWSE	Bottom	745	0,1	0201
C91	17	1,1	4vWSE	Bottom	515	1	0201
C92	18	1,09	4vWSE	Bottom	622	0,22	0201
C93	19	1,01	4vWSE	Bottom	504	0,47	0201
C94	20	1,13	4vWSE	Bottom	604	0,47	0201
C95	21	1,04	4vWSE	Bottom	612	1	0201
C96	22	1,08	4vWSE	Top	612	0,22	0201

Loop Inductance range: 1,01 - 1,40 nH

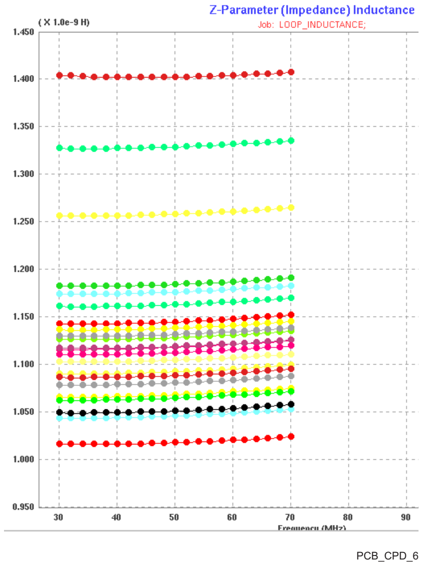


Figure 7-26. vdd_mpu Decoupling Cap Loop Inductances

Figure 7-27 shows vdd_mpu Impedance vs Frequency characteristics.

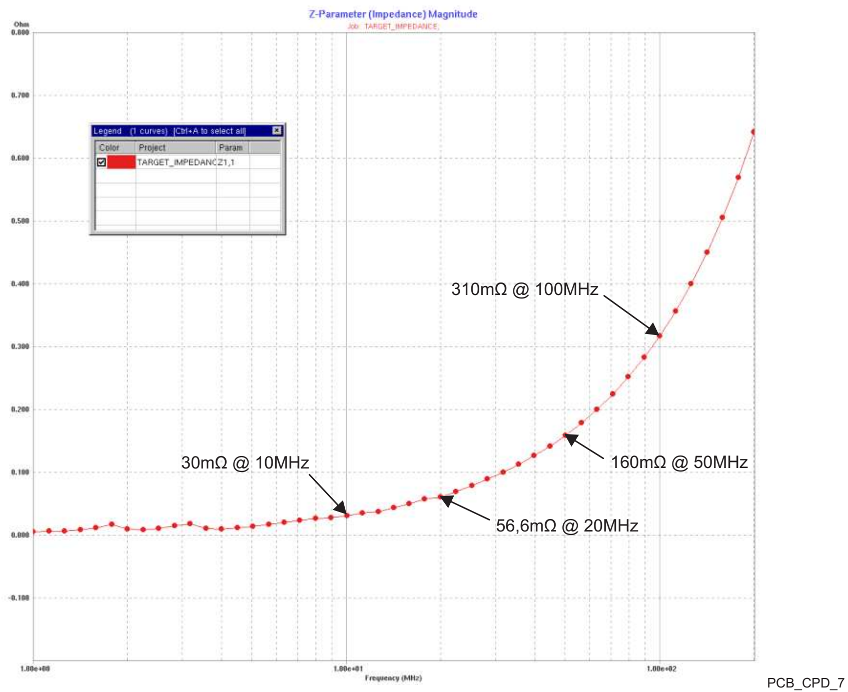


Figure 7-27. vdd_mpu Impedance vs Frequency

7.4 Single-Ended Interfaces

7.4.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces.

- Line spacing:
  – For a line width equal to W, the spacing between two lines must be 2W, at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the device package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see Figure 7-28).

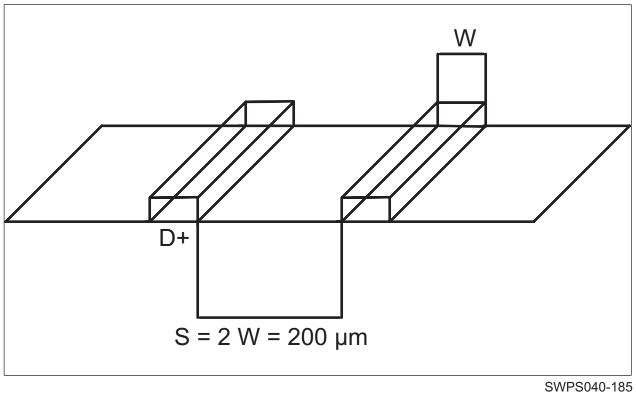


Figure 7-28. Ground Guard Illustration

- Length matching (unless otherwise specified):
  – For bus or traces at frequencies less than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
  – For bus or traces at frequencies greater than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance
  – Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35-Ω and 65-Ω.
- Multiple peripheral support
  – For interfaces where multiple peripherals have to be supported in the star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

7.4.2 QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the QSPI interfaces.

- The qspi1_sclk output signal must be looped back into the qspi1_rtclk input.
- The signal propagation delay from the qspi1_sclk ball to the QSPI device CLK input pin (A to C) must be approximately equal to the signal propagation delay from the QSPI device CLK pin to the qspi1_rtclk ball (C to D).
- The signal propagation delay from the QSPI device CLK pin to the qspi1_rtclk ball (C to D) must be approximately equal to the signal propagation delay of the control and data signals between the QSPI device and the SoC device (E to F, or F to E).
- The signal propagation delay from the qspi1_sclk signal to the series terminators (R2 = 10 Ω) near the QSPI device must be < 450 pS (~7 cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 7-29.

- Propagation delays and matching:
  – A to C = C to D = E to F.
  – Matching skew: < 60 pS
  – A to B < 450 pS
  – B to C = as small as possible (< 60 pS)

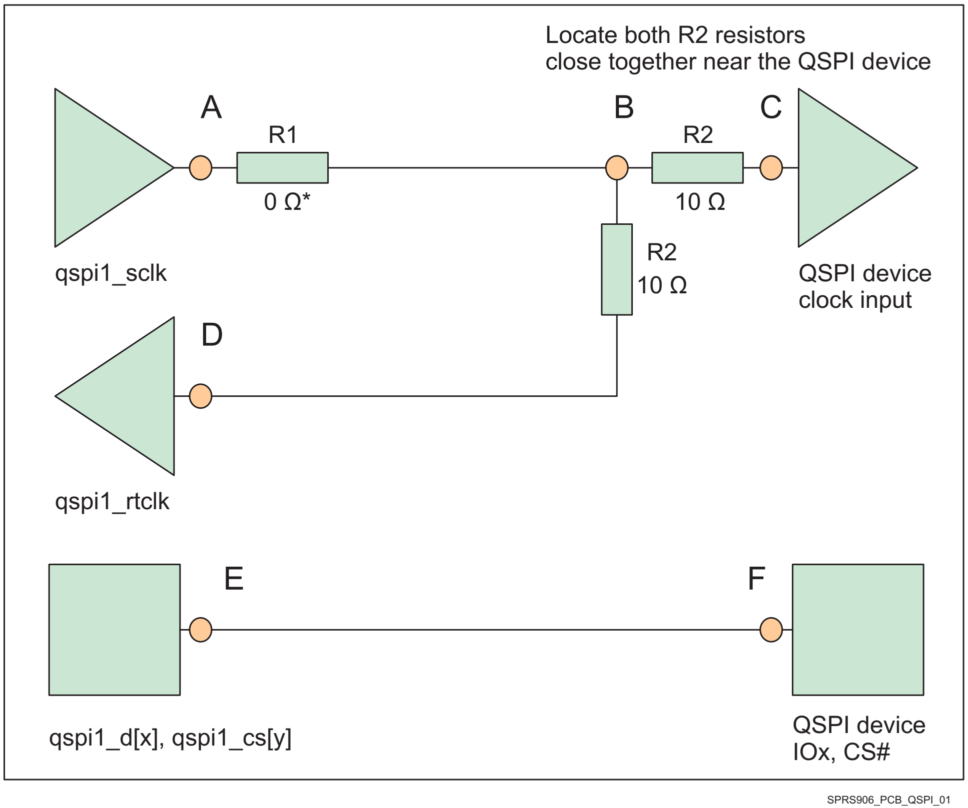


Figure 7-29. QSPI Interface High Level Schematic

NOTE

*0 Ω resistor (R1), located as close as possible to the qspi1_sclk pin, is placeholder for fine-tuning if needed.

7.5 Differential Interfaces

7.5.1 General Routing Guidelines

To maximize signal integrity, proper routing techniques for differential signals are important for high-speed designs. The following general routing guidelines describe the routing guidelines for differential lanes and differential signals.

- As much as possible, no other high-frequency signals must be routed in close proximity to the differential pair.
- Must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the differential impedance value recommended.
- Minimize external components on differential lanes (like external ESD, probe points).
- Through-hole pins are not recommended.
- Differential lanes mustn't cross image planes (ground planes).
- No sharp bend on differential lanes.

- Number of vias on the differential pairs must be minimized, and identical on each line of the differential pair. In case of multiple differential lanes in the same interface, all lines should have the same number of vias.
- Shielded routing is to be promoted as much as possible (for instance, signals must be routed on internal layers that are inside power and/or ground planes).

7.5.2 USB 2.0 Board Design and Layout Guidelines

This section discusses schematic guidelines when designing a universal serial bus (USB) system.

7.5.2.1 Background

Clock frequencies generate the main source of energy in a USB design. The USB differential DP/DM pairs operate in high-speed mode at 480 Mbps. System clocks can operate at 12 MHz, 48 MHz, and 60 MHz. The USB cable can behave as a monopole antenna; take care to prevent RF currents from coupling onto the cable.

When designing a USB board, the signals of most interest are:

- Device interface signals: Clocks and other signal/data lines that run between devices on the PCB.
- Power going into and out of the cable: The USB connector socket pin 1 (VBUS) may be heavily filtered and need only pass low frequency signals of less than ~100 kHz. The USB socket pin 4 (analog ground) must be able to return the current during data transmission, and must be filtered sparingly.
- Differential twisted pair signals going out on cable, DP and DM: Depending upon the data transfer rate, these device terminals can have signals with fundamental frequencies of 240 MHz (high speed), 6 MHz (full speed), and 750 kHz (low speed).
- External crystal circuit (device terminals XI and X0): 12 MHz, 19.2 MHz, 24 MHz, and 48 MHz fundamental. When using an external crystal as a reference clock, a 24 MHz and higher crystal is highly recommended.

7.5.2.2 USB PHY Layout Guide

The following sections describe in detail the specific guidelines for USB PHY Layout.

7.5.2.2.1 General Routing and Placement

Use the following routing and placement guidelines when laying out a new design for the USB physical layer (PHY). These guidelines help minimize signal quality and electromagnetic interference (EMI) problems on a four-or-more layer evaluation module (EVM).

- Place the USB PHY and major components on the un-routed board first. For more details, see Section 7.5.2.2.2.3.
- Route the high-speed clock and high-speed USB differential signals with minimum trace lengths.
- Route the high-speed USB signals on the plane closest to the ground plane, whenever possible.
- Route the high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC’s that use or duplicate clock signals.
- Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mils.
- Route all high-speed USB signal traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

7.5.2.2.2 Specific Guidelines for USB PHY Layout

The following sections describe in detail the specific guidelines for USB PHY Layout.

7.5.2.2.2.1 Analog, PLL, and Digital Power Supply Filtering

To minimize EMI emissions, add decoupling capacitors with a ferrite bead at power supply terminals for the analog, phase-locked loop (PLL), and digital portions of the chip. Place this array as close to the chip as possible to minimize the inductance of the line and noise contributions to the system. An analog and digital supply example is shown in Figure 7-30. In case of multiple power supply pins with the same function, tie them up to a single low-impedance point in the board and then add the decoupling capacitors, in addition to the ferrite bead. This array of caps and ferrite bead improve EMI and jitter performance. Take both EMI and jitter into account before altering the configuration.

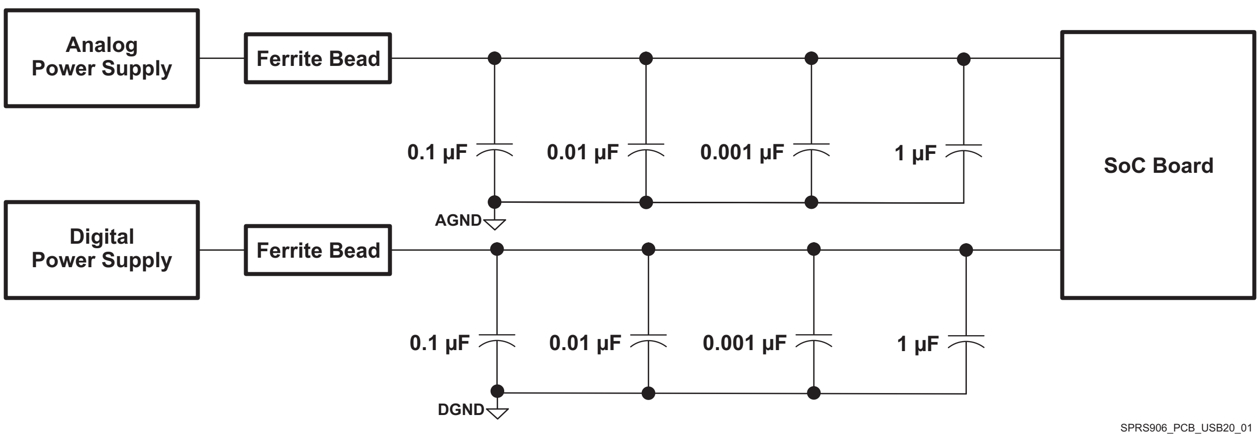


Figure 7-30. Suggested Array Capacitors and a Ferrite Bead to Minimize EMI

Consider the recommendations listed below to achieve proper ESD/EMI performance:

- Use a 0.01 μF cap on each cable power VBUS line to chassis GND close to the USB connector pin.
- Use a 0.01 μF cap on each cable ground line to chassis GND next to the USB connector pin.
- If voltage regulators are used, place a 0.01 μF cap on both input and output. This is to increase the immunity to ESD and reduce EMI. For other requirements, see the device-specific datasheet.

7.5.2.2.2.2 Analog, Digital, and PLL Partitioning

If separate power planes are used, they must be tied together at one point through a low-impedance bridge or preferably through a ferrite bead. Care must be taken to capacitively decouple each power rail close to the device. The analog ground, digital ground, and PLL ground must be tied together to the low-impedance circuit board ground plane.

7.5.2.2.2.3 Board Stackup

Because of the high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 7-31.

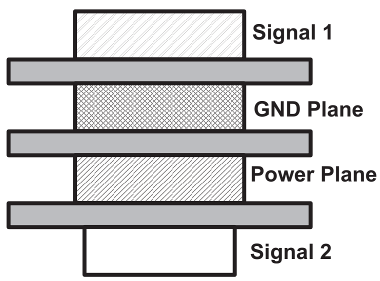


Figure 7-31. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably SIGNAL1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

7.5.2.2.2.4 Cable Connector Socket

Short the cable connector sockets directly to a small chassis ground plane (GND *strap*) that exists immediately underneath the connector sockets. This shorts EMI (and ESD) directly to the chassis ground before it gets onto the USB cable. This etch plane should be as large as possible, but all the conductors coming off connector pins 1 through 6 must have the board signal GND plane run under. If needed, scoop out the chassis GND strap etch to allow for the signal ground to extend under the connector pins. Note that the etches coming from pins 1 and 4 (VBUS power and GND) should be wide and via-ed to their respective planes as soon as possible, respecting the filtering that may be in place between the connector pin and the plane. See Figure 7-32 for a schematic example.

Place a ferrite in series with the cable shield pins near the USB connector socket to keep EMI from getting onto the cable shield. The ferrite bead between the cable shield and ground may be valued between 10 Ω and 50 Ω at 100 MHz; it should be resistive to approximately 1 GHz. To keep EMI from getting onto the cable bus power wire (a very large antenna) a ferrite may be placed in series with cable bus power, VBUS, near the USB connector pin 1. The ferrite bead between connector pin 1 and bus power may be valued between 47 Ω and approximately 1000 Ω at 100 MHz. It should continue being resistive out to approximately 1 GHz, as shown in Figure 7-32.

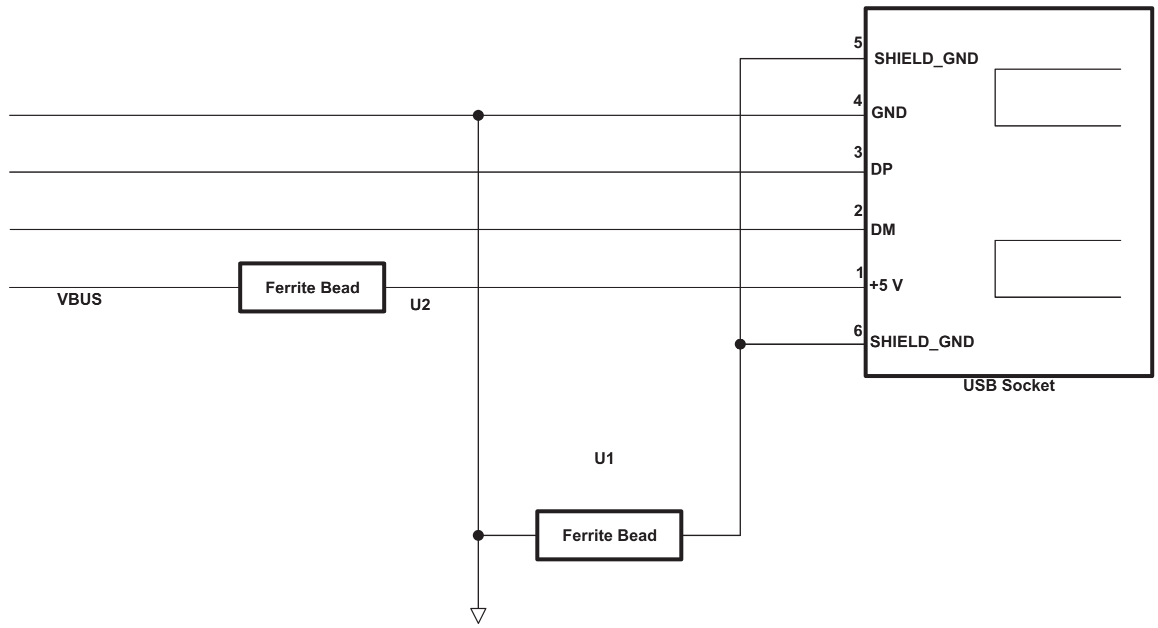


Figure 7-32. USB Connector

7.5.2.2.2.5 Clock Routings

To address the system clock emissions between devices, place a ~10 Ω to 130 Ω resistor in series with the clock signal. Use a trial and error method of looking at the shape of the clock waveform on a high-speed oscilloscope and of tuning the value of the resistance to minimize waveform distortion. The value on this resistor should be as small as possible to get the desired effect. Place the resistor close to the device generating the clock signal. If an external crystal is used, follow the guidelines detailed in the *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (SLLA122).

When routing the clock traces from one device to another, try to use the 3W spacing rule. The distance from the center of the clock trace to the center of any adjacent signal trace should be at least three times the width of the clock trace. Many clocks, including slow frequency clocks, can have fast rise and fall times. Using the 3W rule cuts down on crosstalk between traces. In general, leave space between each of the traces running parallel between the devices. Avoid using right angles when routing traces to minimize the routing distance and impedance discontinuities. For further protection from crosstalk, run guard traces beside the clock signals (GND pin to GND pin), if possible. This lessens clock signal coupling, as shown in Figure 7-33.

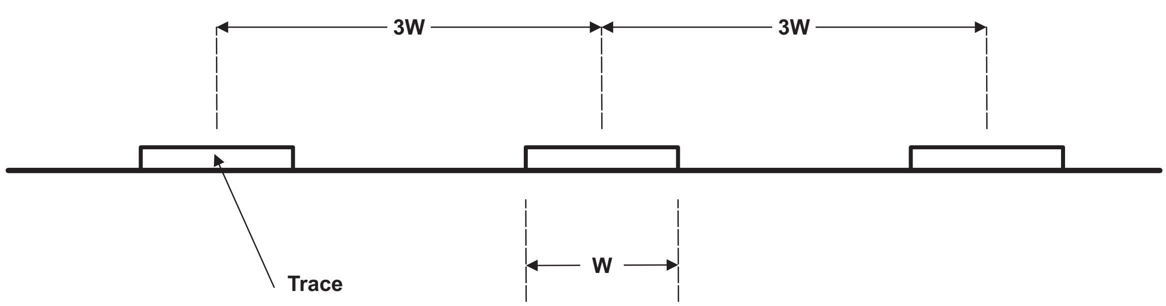


Figure 7-33. 3W Spacing Rule

7.5.2.2.2.6 Crystals/Oscillator

Keep the crystal and its load capacitors close to the USB PHY pins, XI and XO (see Figure 7-34). Note that frequencies from power sources or large capacitors can cause modulations within the clock and should not be placed near the crystal. In these instances, errors such as dropped packets occur. A placeholder for a resistor, in parallel with the crystal, can be incorporated in the design to assist oscillator startup.

Power is proportional to the current squared. The current is *I = C*dv/dt*, because *dv/dt* is a function of the PHY, current is proportional to the capacitive load. Cutting the load to 1/2 decreases the current by 1/2 and the power to 1/4 of the original value. For more details on crystal selection, see the *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (SLLA122).

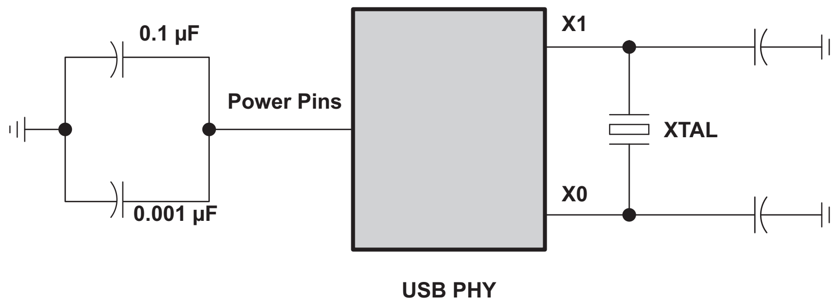


Figure 7-34. Power Supply and Clock Connection to the USB PHY

7.5.2.2.2.7 DP/DM Trace

Place the USB PHY as close as possible to the USB 2.0 connector. The signal swing during high-speed operation on the DP/DM lines is relatively small (400 mV ± 10 %), so any differential noise picked up on the twisted pair can affect the received signal. When the DP/DM traces do not have any shielding, the traces tend to behave like an antenna and picks up noise generated by the surrounding components in the environment. To minimize the effect of this behavior:

- DP/DM traces should always be matched lengths and must be no more than 4 inches in length; otherwise, the eye opening may be degraded (see Figure 7-35).
- Route DP/DM traces close together for noise rejection on differential signals, parallel to each other and within two mils in length of each other. The measurement for trace length must be started from device's balls.
- A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance of 90 Ω ± 15 %. In layout, the impedance of DP and DM should each be 45 Ω ± 10 %.
- DP/DM traces should not have any extra components to maintain signal integrity. For example, traces cannot be routed to two USB connectors.

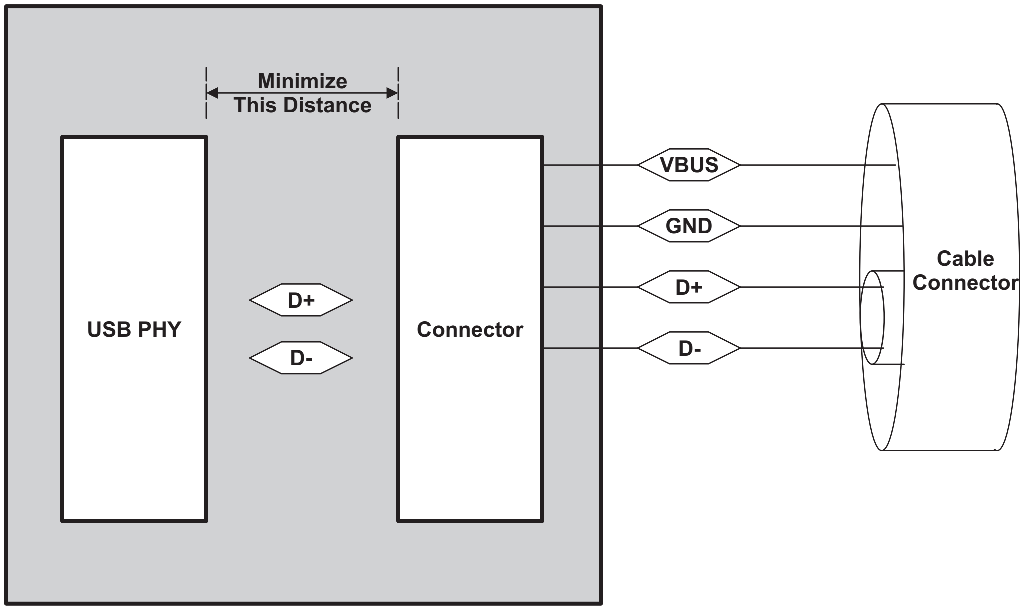


Figure 7-35. USB PHY Connector and Cable Connector

7.5.2.2.2.8 DP/DM Vias

When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

7.5.2.2.2.9 Image Planes

An image plane is a layer of copper (voltage plane or ground plane), physically adjacent to a signal routing plane. Use of image planes provides a low impedance, shortest possible return path for RF currents. For a USB board, the best image plane is the ground plane because it can be used for both analog and digital circuits.

- Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop as shown in Figure 7-36. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.
- Avoid crossing the image power or ground plane boundaries with high-speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals (DP, DM). Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through vias.

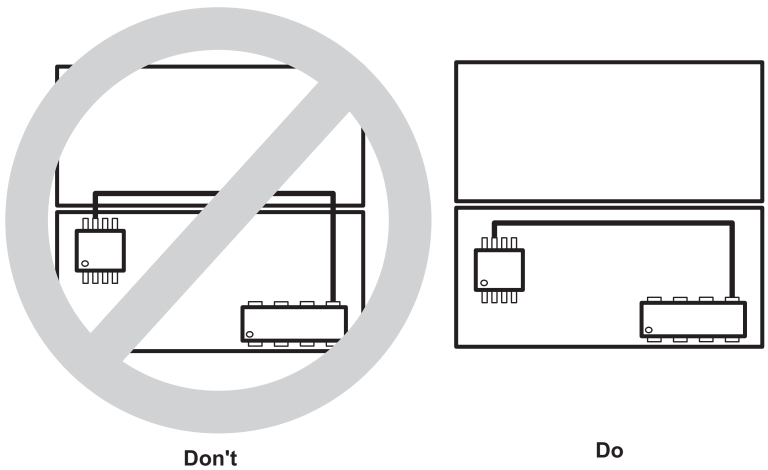


Figure 7-36. Do Not Cross Plane Boundaries

- Do not overlap planes that do not reference each other. For example, do not overlap a digital power plane with an analog power plane as this produces a capacitance between the overlapping areas that could pass RF emissions from one plane to the other, as shown in Figure 7-37.

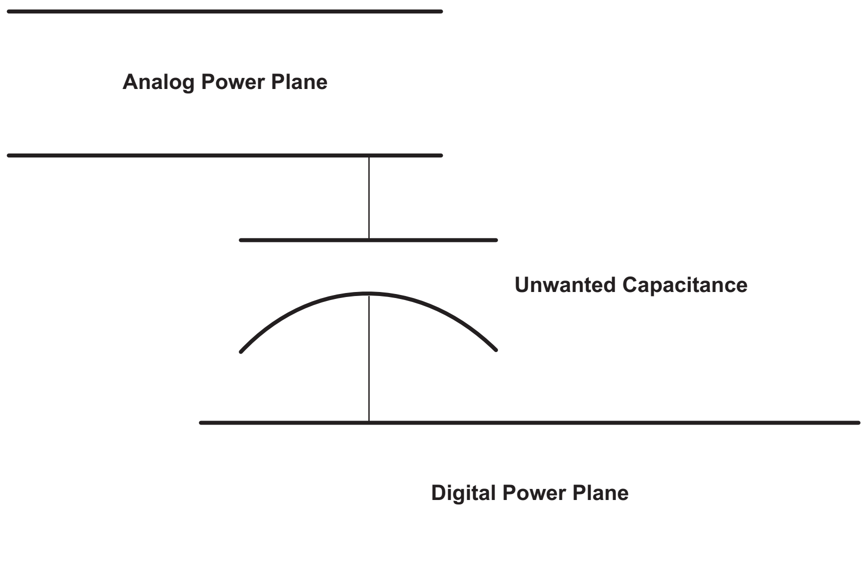


Figure 7-37. Do Not Overlap Planes

- Avoid image plane violations. Traces that route over a slot in an image plane results in a possible RF return loop, as shown in Figure 7-38.

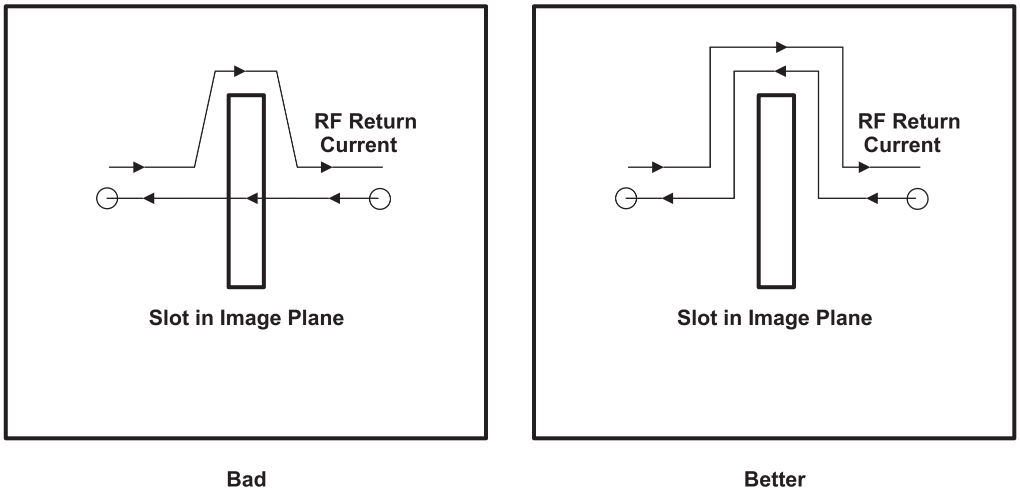


Figure 7-38. Do Not Violate Image Planes

7.5.2.2.2.10 JTAG Interface

For test and debug of the USB PHY only, an IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) and Serial Test and Configuration Interface (STCI) may be available on the System-on-Chip (SoC). If available, keep the USB PHY JTAG interface less than six inches; keeping this distance short reduces noise coupling from other devices and signal loss due to resistance.

7.5.2.2.2.11 Power Regulators

Switching power regulators are a source of noise and can cause noise coupling if placed close to sensitive areas on a circuit board. Therefore, the switching power regulator should be kept away from the DP/DM signals, the external clock crystal (or clock oscillator), and the USB PHY.

7.5.2.3 Electrostatic Discharge (ESD)

International Electronic Commission (IEC) 61000-4-xx is a set of about 25 testing specifications from the IEC. IEC ESD Stressing is done both un-powered and with power applied, and with the device functioning. There must be no physical damage, and the device must keep working normally after the conclusion of the stressing. Typically, equipment has to pass IEC stressing at 8 kV contact and 15 kV air discharge, or higher. To market products/systems in the European community, all products/systems must be CE compliant and have the CE Mark. To obtain the CE Mark, all products/systems need to go through and pass IEC standard requirements; for ESD, it is 61000-4-2. 61000-4-2 requires that the products/systems pass contact discharge at 8 kV and air discharge at 15 kV. When performing an IEC ESD Stressing, only pins accessible to the *outside world* need to pass the test. The system into which the integrated circuit (IC) is placed makes a difference in how well the IC does. For example:

- Cable between the zap point and the IC attenuate the high frequencies in the waveform.
- Series inductance on the PCB board attenuates the high frequencies.
- Unless the capacitor’s ground connection is inductive, capacitance to ground shunts away high frequencies.

7.5.2.3.1 IEC ESD Stressing Test

The following sections describe in detail the IEC ESD Stressing Test modes and test types.

7.5.2.3.1.1 Test Mode

The IEC ESD Stressing test is done through two modes: contact discharge mode and air discharge mode.

For the contact discharge test mode, the preferred way is direct contact applied to the conductive surfaces of the equipment under test (EUT). In the case of the USB system, the conductive surface is the outer casing of the USB connector. The electrode of the ESD generator is held in contact with the EUT or a coupling plane prior to discharge. The arc formation is created under controlled conditions, inside a relay, resulting in repeatable waveforms; however, this arc does not accurately recreate the characteristic unique to the arc of an actual ESD event.

7.5.2.3.1.2 Air Discharge Mode

The air discharge usually applies to a non-conductive surface of the EUT. Instead of a direct contact with the EUT, the charged electrode of the ESD generator is brought close to the EUT, and a spark in the air to the EUT actuates the discharge. Compared to the contact discharge mode, the air discharge is more realistic to the actual ESD occurrence. However, due to the variations of the arc length, it may not be able to produce repeatable waveform.

7.5.2.3.1.3 Test Type

The IEC ESD Stressing test has two test types: direct discharge and indirect discharge. Direct discharge is applies directly to the surface or the structure of the EUT. It includes both contact discharge and air discharge modes. Indirect discharge applies to a coupling plane in the vicinity of the EUT. The indirect discharge is used to simulate personal discharge to objects which are adjacent to the EUT. It includes contact discharge mode only.

7.5.2.3.2 TI Component Level IEC ESD Test

TI Component Level IEC ESD Test tests only the IC terminals that are exposed in system level applications. It can be used to determine the robustness of on-chip protection and the latch-up immunity. The IC can only pass the TI Component Level IEC ESD test when there is no latch-up and IC is fully functional after the test.

7.5.2.3.3 Construction of a Custom USB Connector

A standard USB connector, either type A or type B, provides good ESD protection. However, if a custom USB connector is desired, the following guidelines should be observed to ensure good ESD protection.

- There should be an easily accessible shield plate next to the connector for air-discharge mode purpose.
- Tie the outer shield of the connector to GND. When a cable is inserted into the connector, the shield of the cable should first make contact with the outer shield.
- If the connector includes power and GND, the lead of power and GND need to be longer than the leads of signal.
- The connector needs to have a key to ensure proper insertion of the cable.
- See the standard USB connector for reference.

7.5.2.3.4 ESD Protection System Design Consideration

ESD protection system design consideration is covered in Section 7.5.2.2 of this document. The following are additional considerations for ESD protection in a system.

- Metallic shielding for both ESD and EMI
- Chassis GND isolation from the board GND
- Air gap designed on board to absorb ESD energy
- Clamping diodes to absorb ESD energy
- Capacitors to divert ESD energy
- The use of external ESD components on the DP/DM lines may affect signal quality and are not recommended.

7.5.2.4 References

- *USB 2.0 Specification*, Intel, 2000, http://www.usb.org/developers/docs/
- *High Speed USB Platform Design Guidelines*, Intel, 2000, http://www.intel.com/technology/usb/download/usb2dg_R1_0.pdf
- *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (SLLA122)

7.5.3 USB 3.0 Board Design and Layout Guidelines

This section provides the timing specification for the USB3.0 (USB1 in the device) interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the USB3.0 interface requirements are met. The design rules stated within this document are targeted at DEVICE mode electrical compliance. HOST mode and/or systems that do not include the 3m USB cable and far-end 11-inch PCB trace required by DEVICE mode compliance testing may not need the complete list of optimizations shown in this document; however, applying these optimizations to HOST mode systems will lead to optimal DEVICE mode performance.

7.5.3.1 USB 3.0 interface introduction

The USB 3.0 has two unidirectional differential pairs: TXp/TXn pair and RXp/RXn pair. AC coupling caps are needed on the board for TX traces.

Figure 7-39 present high level schematic diagram for USB 3.0 interface.

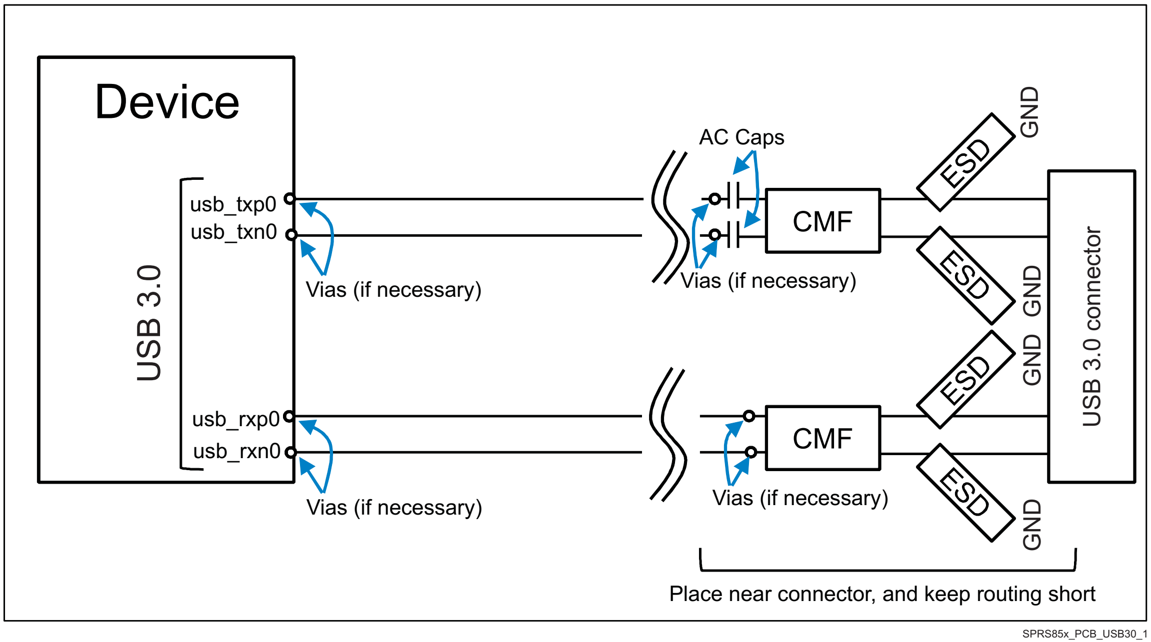


Figure 7-39. USB 3.0 Interface High Level Schematic

NOTE

ESD components should be on a PCB layer next to a system GND plane layer so the inductance of the via to GND will be minimal.

If vias are used, place the vias near the AC Caps or CMFs and under the SoC BGA, if necessary.

Figure 7-40 present placement diagram for USB 3.0 interface.

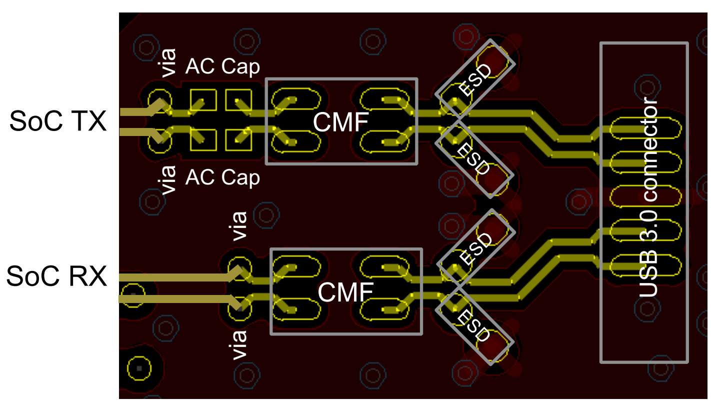


Figure 7-40. USB 3.0 placement diagram

Table 7-10. USB1 Component Reference

INTERFACE	COMPONENT	SUPPLIER	PART NUMBER
USB3 PHY	ESD	TI	TPD1E05U06
	CMF	Murata	DLW21SN900HQ2
	C	-	100 nF (typical size: 0201)

7.5.3.2 USB 3.0 General routing rules

Some general routing guidelines regarding USB 3.0:

- Avoid crossing splits reference plane(s).
- Shorter trace length is preferred.
- Minimize the via usage and layer transition
- Keep large spacing between TX and RX pairs.
- Intra-lane delay mismatch between DP and DM less than 1ps. Same for RXp and RXn.
- Distance between common mode filter (CMF) and ESD protection device should be as short as possible
- Distance between ESD protection device and USB connector should be as short as possible.
- Distance between AC capacitors (TX only) and CMF should be as short as possible.
- USB 3.0 signals should always be routed over an adjacent ground plane.

Table 7-11 and Table 7-12 present routing specification and recommendations for USB1 in the device.

Table 7-11. USB1 Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Device balls to USB 3.0 connector trace length			3500	Mils
Skew within a differential pair		3	6	Mils
Number of stubs allowed on TX/RX traces			0	Stubs
TX/RX pair differential impedance	83	90	97	Ω
Number of vias on each TX/RX trace (1)			2	Vias
Differential pair to any other trace spacing (2) (3) (4)	2xDS	3xDS		
Number of ground plane cuts allowed within USB3 routing region (except for specific ground carving as explained in this document)			0	Cuts
Number of layers between USB3.0 routing region and reference ground plane			0	Layers
PCB trace width		6		Mils
PCB BGA escape via pad size		18		Mils
PCB BGA escape via hole size		10		Mils

(1) Vias must be used in pairs and spaced equally along a signal path.

(2) DS = differential spacing of the traces.

(3) Exceptions may be necessary in the SoC package BGA area.

(4) GND guard-bands on the same layer may be closer, but should not be allowed to affect the impedance of the differential pair routing. GND guard-bands to isolate USB3.0 differential pairs from all other signals are recommended.

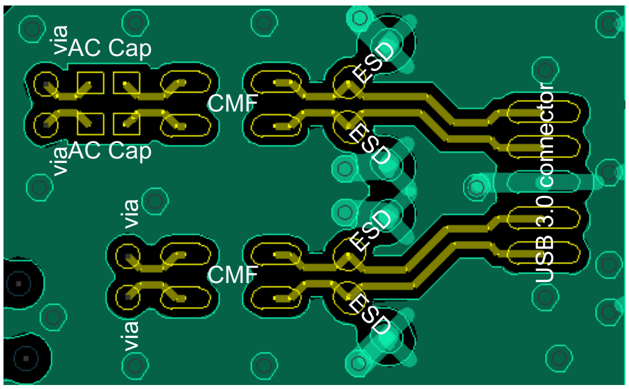
Table 7-12. USB1 Routing Recommendations

Item	Description	Reason
ESD location	Place ESD component on same layer as connector (no via or stub to ESD component)	Eliminate reflection loss from via and stub to ESD
ESD part number	TPD1E05U06	Minimize capacitance (0.42 pF)
CMF part number	DLW21SN900HQ2	Manufacturer's recommended device
Connector	Use USB3.0 connector with supporting s-parameter model	Enable full signal chain simulation
Carve Ground	Carve GND underneath AC Caps, ESD, CMF, and connector	Minimize capacitance under ESD and CMF
Round pads	Minimize pad size and round the corners of the pads for the ESD and CMF components	Minimize capacitance

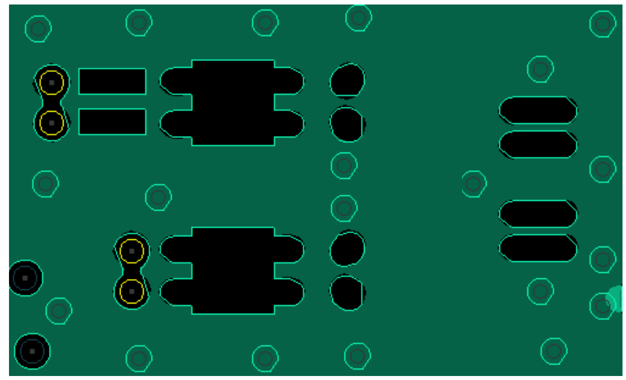
Table 7-12. USB1 Routing Recommendations (continued)

Item	Description	Reason
Vias	Max 2 vias per signal trace. If vias are required, place vias close to the AC Caps and CMFs. Vias under the SoC grid array may be used if necessary to route signals away from BGA pattern.	Vias significantly degrade signal integrity at 2.5 GHz

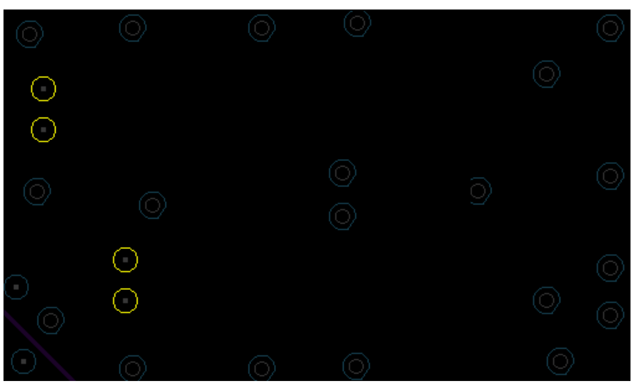
Figure 7-41 presents an example layout, demonstrating the “carve GND” concept.



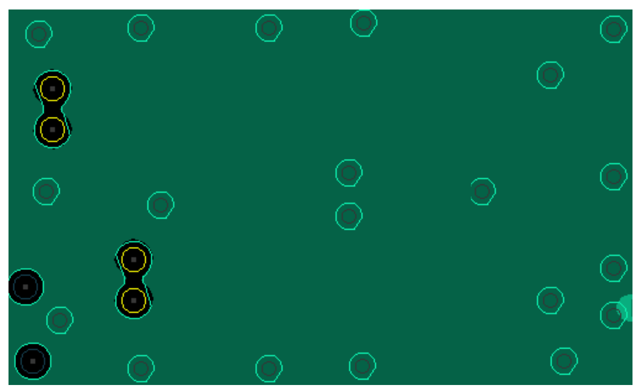
Top Layer: Routing from SoC through AC Caps, CMF, and ESD to connector.



Layer2, GND: Gaps carved in GND underneath AC Caps, CMF, ESD, and connector.



Layer3, Signal: Implement as keep-out zone underneath carved GND areas.



Layer4, GND Plane underneath AC Caps, CMF, ESD, and connector.

SPRS85x_PCB_USB30_3

Figure 7-41. USB 3.0 Example “carve GND” layout

7.5.4 *HDMI Board Design and Layout Guidelines*

This section provides the timing specification for the HDMI interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the HDMI interface requirements are met. The design rules stated within this document are targeted at resolutions less than or equal to 1080p60 with 8-bit color; deep color (10-bit) requires further signal integrity optimization.

7.5.4.1 HDMI Interface Schematic

The HDMI bus is separated into three main sections (HDMI Ethernet and the optional Audio Return Channel are not specifically supported by this Device):

1. Transition Minimized Differential Signaling (TMDS) high speed digital video interface

2. Display Data Channel (I2C bus for configuration and status exchange between two devices)
3. Consumer Electronics Control (optional) for remote control of connected devices.

The DDC and CEC are low speed interfaces, so nothing special is required for PCB layout of these signals.

The TMDS channels are high speed differential pairs and therefore require the most care in layout. Specifications for TMDS layout are below.

Figure 7-42 shows the HDMI interface schematic.

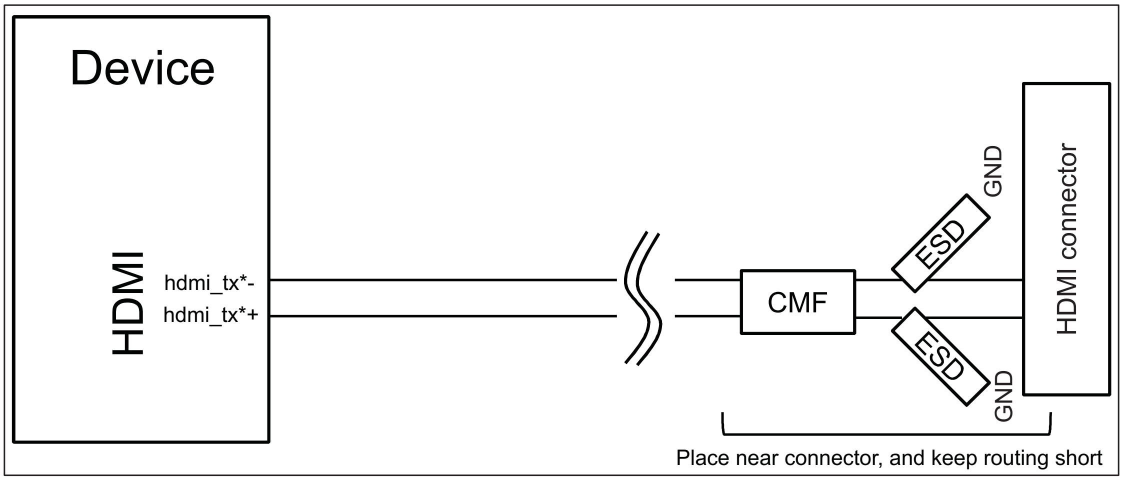


Figure 7-42. HDMI Interface High Level Schematic

Figure 7-43 presents placement diagram for HDMI interface.

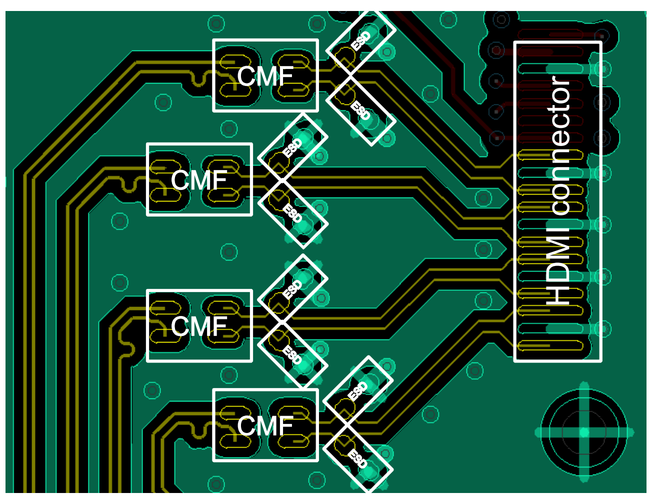


Figure 7-43. HDMI Placement Diagram

Table 7-13. HDMI Component Reference

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
HDMI	ESD	TI	TPD1E05U06
	CMF	Murata	DLW21SN900HQ2

7.5.4.2 TMDS General Routing Guidelines

The TMDS signals are high speed differential pairs. Care must be taken in the PCB layout of these signals to ensure good signal integrity.

The TMDS differential signal traces must be routed to achieve 100 Ω (+/- 10 %) differential impedance and 60 Ω (+/-10 %) single ended impedance. Single ended impedance control is required because differential signals can't be closely coupled on PCBs and therefore single ended impedance becomes important.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 60 Ω impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations don't affect impedance as much, therefore it's easier to maintain accurate impedance over the length of the signal. The wider traces also show reduced skin effect and therefore often result in better signal integrity.

Some general routing guidelines regarding TMDS:

- Avoid crossing splits reference plane(s).
- Shorter trace length is preferred.
- Distance between common mode filter (CMF) and ESD protection device should be as short as possible
- Distance between ESD protection device and HDMI connector should be as short as possible.

Table 7-14 shows the routing specifications for the TMDS signals.

Table 7-14. TMDS Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Device balls to HDMI header trace length			4000	Mils
Skew within a differential pair		3	5	Mils
Number of stubs allowed on TMDS traces			0	stubs
TMDS pair differential impedance	90	100	110	Ω
TMDS single-ended impedance	54	60	66	Ω
Number of vias on each TMDS trace			0	Vias
TMDS differential pair to any other trace spacing (1) (2) (3)	2×DS	3×DS		Mils
Number of ground plane cuts allowed within HDMI routing region (except for specific ground carving as explained in this document)			0	Cuts
Number of layers between HDMI routing region and reference ground plane			0	Layers
PCB trace width		4.4		Mils

(1) DS = differential spacing of the traces.

(2) Exceptions may be necessary in the SoC package BGA area.

(3) GND guard-bands may be closer, but should not be allowed to affect the impedance of the differential pair routing. GND guard-bands to isolate HDMI differential pairs from all other signals is recommended.

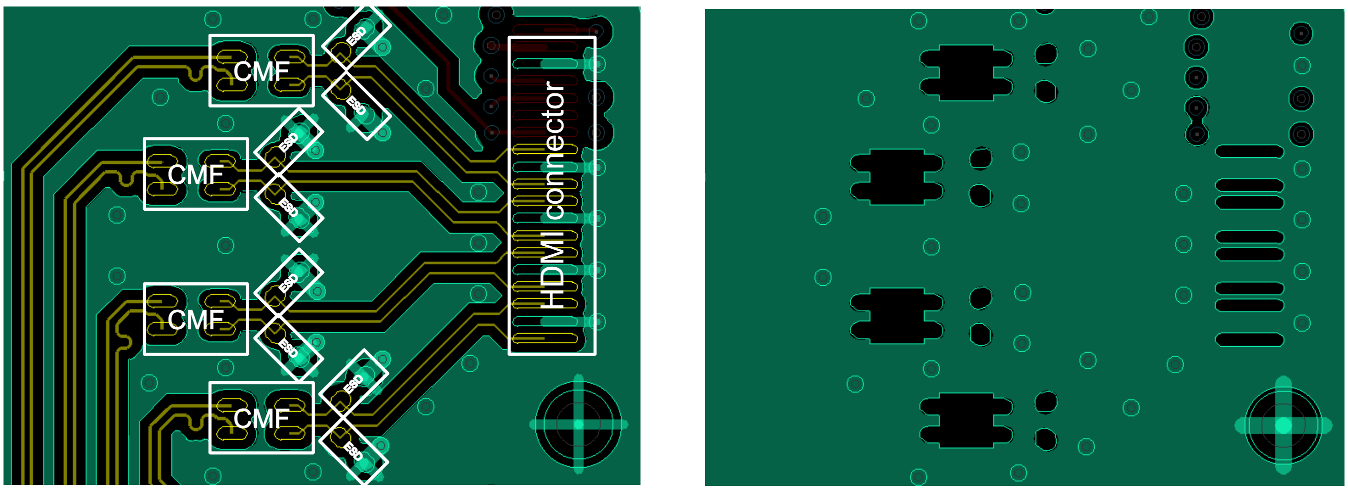
Table 7-15. TDMS Routing Recommendations

Item	Description	Reason
ESD part number	TPD1E05U06	Minimize capacitance (0.42 pF)

Table 7-15. TDMS Routing Recommendations (continued)

Item	Description	Reason
Carve Ground	Carve GND underneath ESD and CMF	Minimize capacitance under ESD and CMF
Round pads	Reduce pad size and round the corners of the pads for the ESD and CMF components	Minimize capacitance
Routing layer	Route all signals only on the same layer as SoC	Minimize reflection loss

Figure 7-44presents an example layout, demonstrating the “carve GND” concept.



Top Layer: Routing from SoC through CMF, and ESD to connector.

Layer2, GND: Gaps carved in GND underneath, CMF, ESD, and connector.

SPRS85x_PCB_HDMI_3

Figure 7-44. HDMI Example “carve GND” layout

7.5.4.3 TPD5S115

The TPD5S115 is an integrated HDMI companion chip solution. The device provides a regulated 5 V output (5VOUT) for sourcing the HDMI power line. The TPD5S115 exceeds the IEC61000-4-2 (Level 4) ESD protection level.

7.5.4.4 HDMI ESD Protection Device (Required)

Interfaces that connect to a cable such as HDMI generally require more ESD protection than can be built into the processor’s outputs. Therefore this HDMI interface requires the use of an ESD protection chip to provide adequate ESD.

When selecting an ESD protection chip, choose the lowest capacitance ESD protection available to minimize signal degradation. In no case should be ESD protection circuit capacitance be more than 5pF.

TI manufactures these devices that provide ESD protection for HDMI signals such as the TPDxE05U06. For more information see the www.ti.com website.

7.5.4.5 PCB Stackup Specifications

Table 7-16 shows the stackup and feature sizes required for HDMI.

Table 7-16. HDMI PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCB Routing/Plane Layers	4	6	-	Layers

Table 7-16. HDMI PCB Stackup Specifications (continued)

PARAMETER	MIN	TYP	MAX	UNIT
Signal Routing Layers	2	3	-	Layers
Number of ground plane cuts allowed within HDMI routing region	-	-	0	Cuts
Number of layers between HDMI routing region and reference ground plane	-	-	0	Layers
PCB Trace width		4		Mils

7.5.4.6 Grounding

Each TMDS channel has its own shield pin and they should be grounded to provide a return current path for the TMDS signal.

7.5.5 SATA Board Design and Layout Guidelines

The device provides one SATA port. This section provides the timing specification for the SATA interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the SATA interface requirements are met.

7.5.5.1 SATA Interface Schematic

Figure 7-45 shows the data portion of the SATA interface schematic.

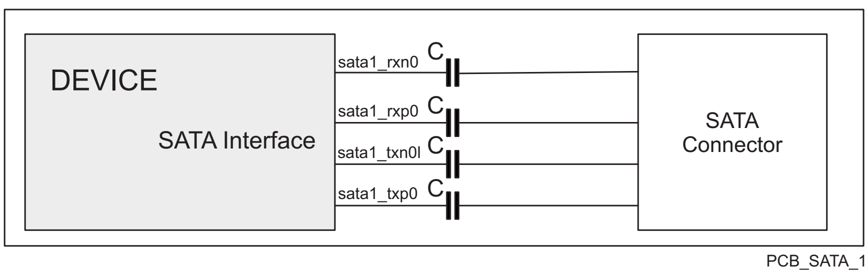


Figure 7-45. SATA Interface High Level Schematic

NOTE

AC coupling capacitors (C) are required on the receive and transmit data pairs. Table 7-17 shows the requirements for these capacitors.

Table 7-17. SATA AC Coupling Capacitors Requirements

PARAMETER	MIN	TYP	MAX	UNIT
SATA AC coupling capacitor value	0.3	10	12	nF
SATA AC coupling capacitor package size		0402	0603	EIA(1)(2)

(1) EIA LxW units, i.e., a 0402 is a 40×20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

7.5.5.2 Compatible SATA Components and Modes

Table 7-18 shows the compatible SATA components and supported modes. Note that the only supported configuration is an internal cable from the processor host to the SATA device.

Table 7-18. Compatible SATA Components and Modes

PARAMETER	MIN	MAX	UNIT	SUPPORTED
Transfer Rates	1.5	3	Gbps	
Internal Cable	-	-	-	YES

7.5.5.3 PCB Stackup Specifications

Table 7-19 shows the stackup and feature sizes required for these types of SATA connections.

Table 7-19. SATA PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Number of ground plane cuts allowed within SATA routing region	-	-	0	Cuts
Number of layers between SATA routing area and reference plane	-	-	0	Layers
PCB Routing clearance		4		Mils
PCB Trace width		4		Mils

7.5.5.4 Routing Specifications

The SATA data signal traces must be routed to achieve 100 Ω (+/-10 %) differential impedance and 60 Ω (+/-10 %) single ended impedance. The signal ended impedance is required because differential signals can’t be closely coupled on PCBs and therefore single ended impedance becomes important. 60 Ω is chosen for the single ended impedance to minimize problems caused by too low an impedance.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 100 Ω differential and 60 Ω single ended impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

Table 7-20 shows the routing specifications for the SATA data signals.

Table 7-20. SATA Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
SATA signal trace length (device balls to SATA connector)			3050(1)	Mils
Differential pair trace skew matching			5	Mils
Number of stubs allowed on SATA traces(2)			0	stubs
TX/RX pair differential impedance	90	100	110	Ω
TX/RX single-ended impedance	54	60	66	Ω
Number of vias on each SATA trace			0	Vias
SATA differential pair to any other trace spacing	2×DS(3)			

(1) Beyond this, signal integrity may suffer.

(2) Inline pads may be used for probing.

(3) DS = differential spacing of the SATA traces.

Table 7-21. SATA Routing Recommendations

Item	Description	Reason
ESD part number	None	ESD suppression generally not used on SATA

7.5.6 *PCIe Board Design and Layout Guidelines*

The PCIe interface on the device provides support for a 5.0 Gbps lane with polarity inversion.

7.5.6.1 PCIe Connections and Interface Compliance

The PCIe interface on the device is compliant with the PCIe revision 3.0 specification. Please refer to the PCIe specifications for all connections that are described in it. Those recommendations are more descriptive and exhaustive than what is possible here.

The use of PCIe compatible bridges and switches is allowed for interfacing with more than one other processor or PCIe device.

7.5.6.1.1 Coupling Capacitors

AC coupling capacitors are required on the transmit data pair. Table 7-22 shows the requirements for these capacitors.

Table 7-22. PCIe AC Coupling Capacitors Requirements

PARAMETER	MIN	TYP	MAX	UNIT
PCIe AC coupling capacitor value	90	100	110	nF
PCIe AC coupling capacitor package size		0402	0603	EIA[1][2]

(1) EIA LxW units, i.e., a 0402 is a 40×20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

7.5.6.1.2 Polarity Inversion

The PCIe specification requires polarity inversion support. This means for layout purposes, polarity is unimportant because each signal can change its polarity on die inside the chip. This means polarity within a lane is unimportant for layout.

7.5.6.2 Non-standard PCIe connections

The following sections contain suggestions for any PCIe connection that is NOT described in the official PCIe specification, such as an on-board Device to Device or Device to other PCIe compliant processor connection.

7.5.6.2.1 PCB Stackup Specifications

Table 7-23 shows the stackup and feature sizes required for these types of PCIe connections.

Table 7-23. PCIe PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Number of ground plane cuts allowed within PCIe routing region	-	-	0	Cuts
Number of layers between PCIe routing area and reference plane [1]	-	-	0	Layers
PCB Routing clearance		4		Mils
PCB Trace width		4		Mils

(1) A reference plane may be a ground plane or the power plane referencing the PCIe signals.

7.5.6.2.2 Routing Specifications

7.5.6.2.2.1 Impedance

The PCIe data signal traces must be routed to achieve 100-Ω (± 10 %) differential impedance and 60-Ω (± 10 %) single-ended impedance. The single-ended impedance is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important. These requirements are the same as those recommended in the PCIe Motherboard Checklist 1.0 document, available from PCI-SIG (www.pcisig.com).

These impedances are impacted by trace width, trace spacing, distance between signals and referencing planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs result in as close to 100-Ω differential impedance and 60-Ω single-ended impedance as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met. See Table 7-24 below.

7.5.6.2.2.2 Differential Coupling

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production. For PCBs with very tight space limitations (which are usually small) this can work, but for most PCBs, the loosely coupled option is probably best.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier (because each trace is not so fixed in position relative to the other), and trace width variations don't affect impedance as much, therefore it's easier to maintain an accurate impedance over the length of the signal. For longer routes, the wider traces also show reduced skin effect and therefore often result in better signal integrity with a larger eye diagram opening.

Table 7-24 shows the routing specifications for the PCIe data signals.

Table 7-24. PCI-E Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCIe signal trace length (device balls to PCIe connector)			4700[(1)]	Mills
Differential pair trace matching			5[(2)]	Mils
Number of stubs allowed on PCIe traces[(3)]			0	stubs
TX/RX pair differential impedance	90	100	110	Ω
TX/RX single-ended impedance	54	60	66	Ω
Pad size of vias on PCIe trace			25[(4)]	Mils
Hole size of vias on PCIe trace			14	Mils
Number of vias on each PCIe trace			0	Vias
PCIe differential pair to any other trace spacing	2×DS[(5)]			

(1) Beyond this, signal integrity may suffer.
(2) For example, RXP0 within 5 Mils of RXN0.
(3) Inline pads may be used for probing.
(4) 35-Mil antipad maximum recommended.
(5) DS = differential spacing of the PCIe traces.

Table 7-25. PCI-E Routing Recommendations

Item	Description	Reason
ESD part number	None	ESD suppression generally not used on PCIe

7.5.6.2.2.3 *Pair Length Matching*

Each signal in the differential pair should be matched to within 5 mils of its matching differential signal. Length matching should be done as close to the mismatch as possible.

7.5.6.3 LJCB_REFN/P Connections

A Common Refclk Rx Architecture is required to be used for the device PCIe interface. Specifically, two modes of Common Refclk Rx Architecture are supported:

- **External REFCLK Mode**: An common external 100 MHz clock source is distributed to both the Device and the link partner
- **Output REFCLK Mode**: A 100 MHz HCSL clock source is output by the device and used by the link partner

In **External REFCLK Mode**, a high-quality, low-jitter, differential HCSL 100 MHz clock source compliant to the PCIe REFCLK AC Specifications should be provided on the Device's ljcb_clkn / ljcb_clkp inputs. Alternatively, an LVDS clock source can be used with the following additional requirements:

- External AC coupling capacitors described in Table 7-26 should be populated at the ljcb_clkn / ljcb_clkp inputs.
- All termination requirements (ex. parallel 100 Ω termination) from the clock source manufacturer should be followed.

In **Output REFCLK Mode**, the 100 MHz clock from the Device's DPLL_PCIE_REF should be output on the Device's ljcb_clkn / ljcb_clkp pins and used as the HCSL REFCLK by the link partner. External near-side termination to ground described in Table 7-27 is required on both of the ljcb_clkn / ljcb_clkp outputs in this mode.

Table 7-26. LJCB_REFN/P Requirements in External LVDS REFCLK Mode

PARAMETER	MIN	TYP	MAX	UNIT
ljcb_clkn / ljcb_clkp AC coupling capacitor value		100		nF
ljcb_clkn / ljcb_clkp AC coupling capacitor package size		0402	0603	EIA(1)(2)

(1) EIA LxW units, i.e., a 0402 is a 40×20 mils surface mount capacitor.

(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side by side.

Table 7-27. LJCB_REFN/P Requirements in Output REFCLK Mode

PARAMETER	MIN	TYP	MAX	UNIT
ljcb_clkn / ljcb_clkp near-side termination to ground value	47.5	50	52.5	Ω

7.6 Clock Routing Guidelines

7.6.1 32-kHz Oscillator Routing

When designing the printed-circuit board:

- Keep the crystal as close as possible to the crystal pins X1 and X2.
- Keep the trace lengths short and small to reduce capacitor loading and prevent unwanted noise pickup.
- Place a guard ring around the crystal and tie the ring to ground to help isolate the crystal from unwanted noise pickup.
- Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling.

- Finally, an additional local ground plane on an adjacent PCB layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane must be isolated from the regular PCB ground plane and tied to the GND pin of the RTC. The plane must not be any larger than the perimeter of the guard ring. Make sure that this ground plane does not contribute to significant capacitance (a few pF) between the signal line and ground on the connections that run from X1 and X2 to the crystal.

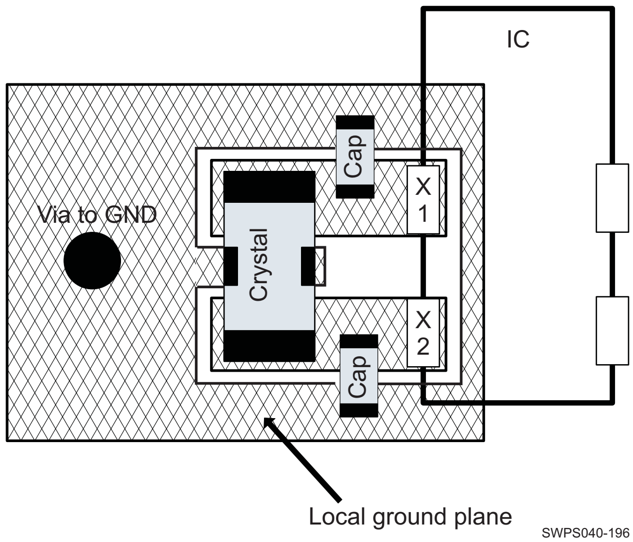


Figure 7-46. Slow Clock PCB Requirements

7.6.2 Oscillator Ground Connection

Although the impedance of a ground plane is low it is, of course, not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. Figure 7-47 shows the grounding scheme for slow (low frequency) clock generated from the internal oscillator.

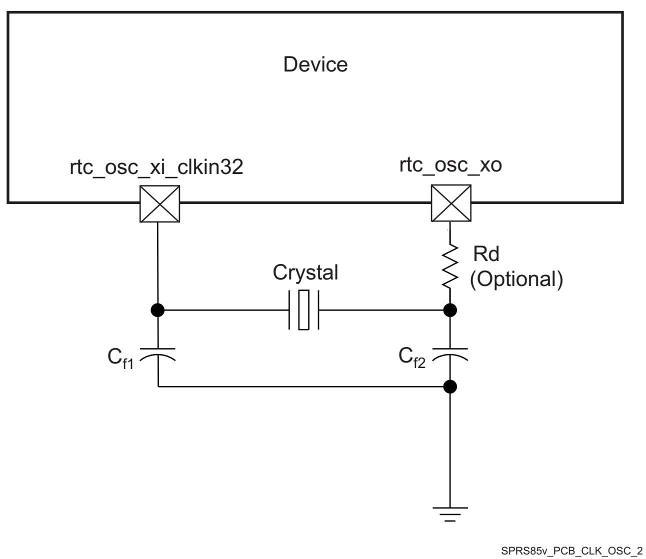
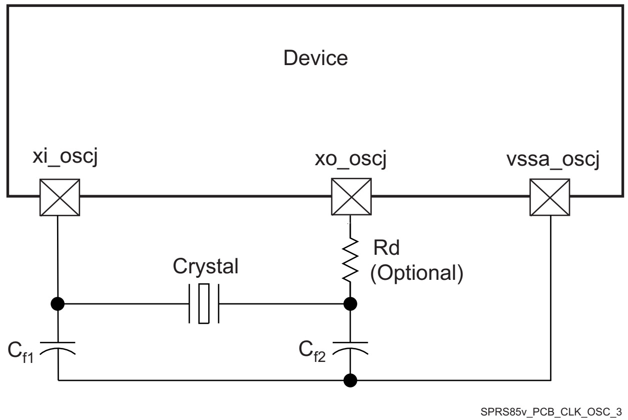


Figure 7-47. Grounding Scheme for Low-Frequency Clock

Figure 7-48 shows the grounding scheme for high-frequency clock.



(1) j in *_osc = 0 or 1

Figure 7-48. Grounding Scheme for High-Frequency Clock

7.7 DDR2/DDR3 Board Design and Layout Guidelines

7.7.1 DDR2/DDR3 General Board Layout Guidelines

To help ensure good signaling performance, consider the following board design guidelines:

- Avoid crossing splits in the power plane.
- Minimize Vref noise.
- Use the widest trace that is practical between decoupling capacitors and memory module.
- Maintain a single reference.
- Minimize ISI by keeping impedances matched.
- Minimize crosstalk by isolating sensitive bits, such as strobes, and avoiding return path discontinuities.
- Use proper low-pass filtering on the Vref pins.
- Keep the stub length as short as possible.
- Add additional spacing for on-clock and strobe nets to eliminate crosstalk.
- Maintain a common ground reference for all bypass and decoupling capacitors.
- Take into account the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.

7.7.2 DDR2 Board Design and Layout Guidelines

7.7.2.1 Board Designs

TI only supports board designs that follow the guidelines outlined in this document. The switching characteristics and the timing diagram for the DDR2 memory controller are shown in Table 7-28 and Figure 7-49.

Table 7-28. Switching Characteristics Over Recommended Operating Conditions for DDR2 Memory Controller

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR21	$t_{c(DDR\_CLK)}$	Cycle time, DDR_CLK	2.5	8	ns

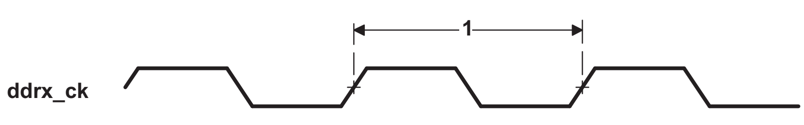


Figure 7-49. DDR2 Memory Controller Clock Timing

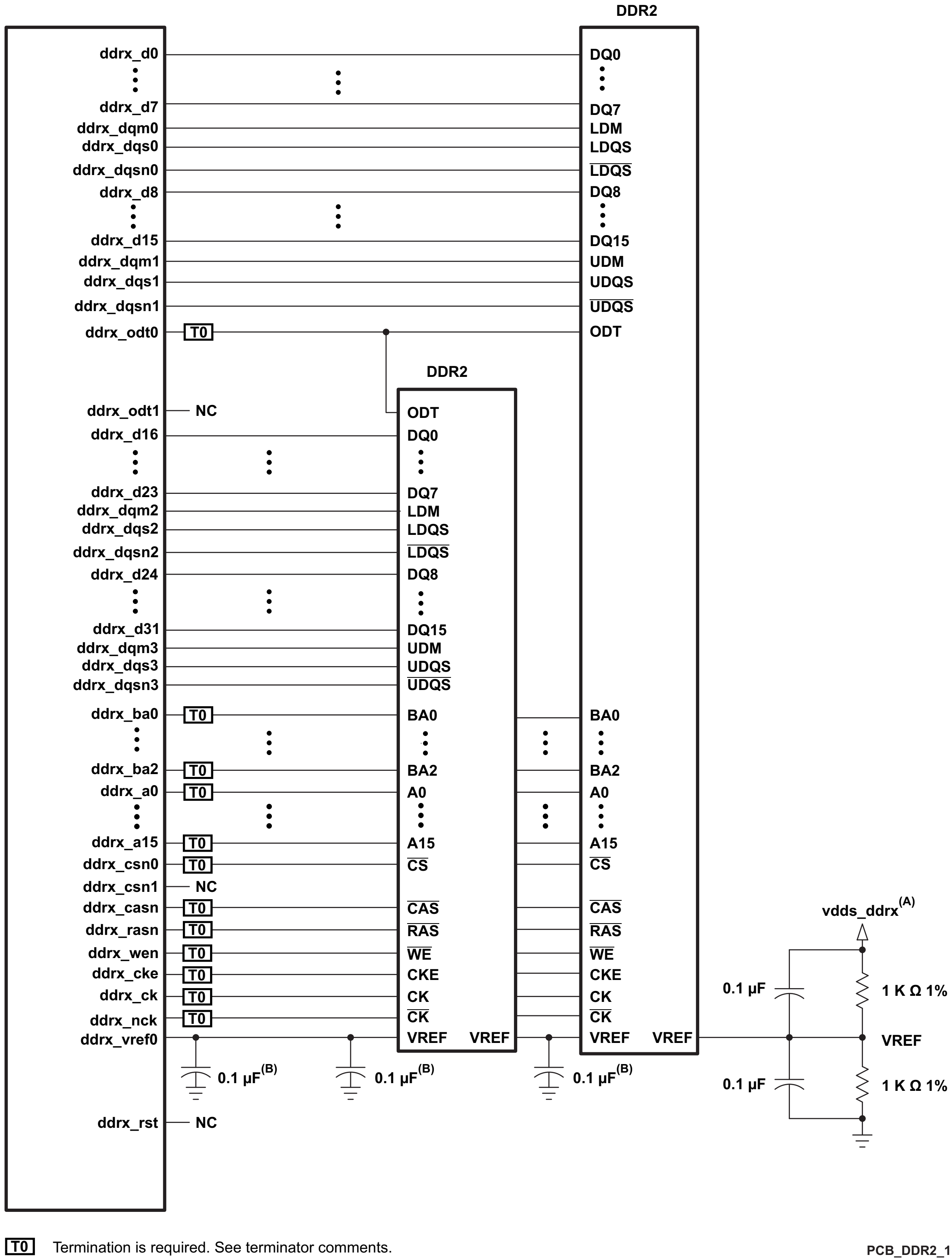
7.7.2.2 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR2 specification, see the *Understanding TI's PCB Routing Rule-Based DDR Timing Specification* Application Report (Literature Number: SPRAAV0).

7.7.2.2.1 DDR2 Interface Schematic

Figure 7-50 shows the DDR2 interface schematic for a x32 DDR2 memory system. In Figure 7-51 the x16 DDR2 system schematic is identical except that the high-word DDR2 device is deleted.

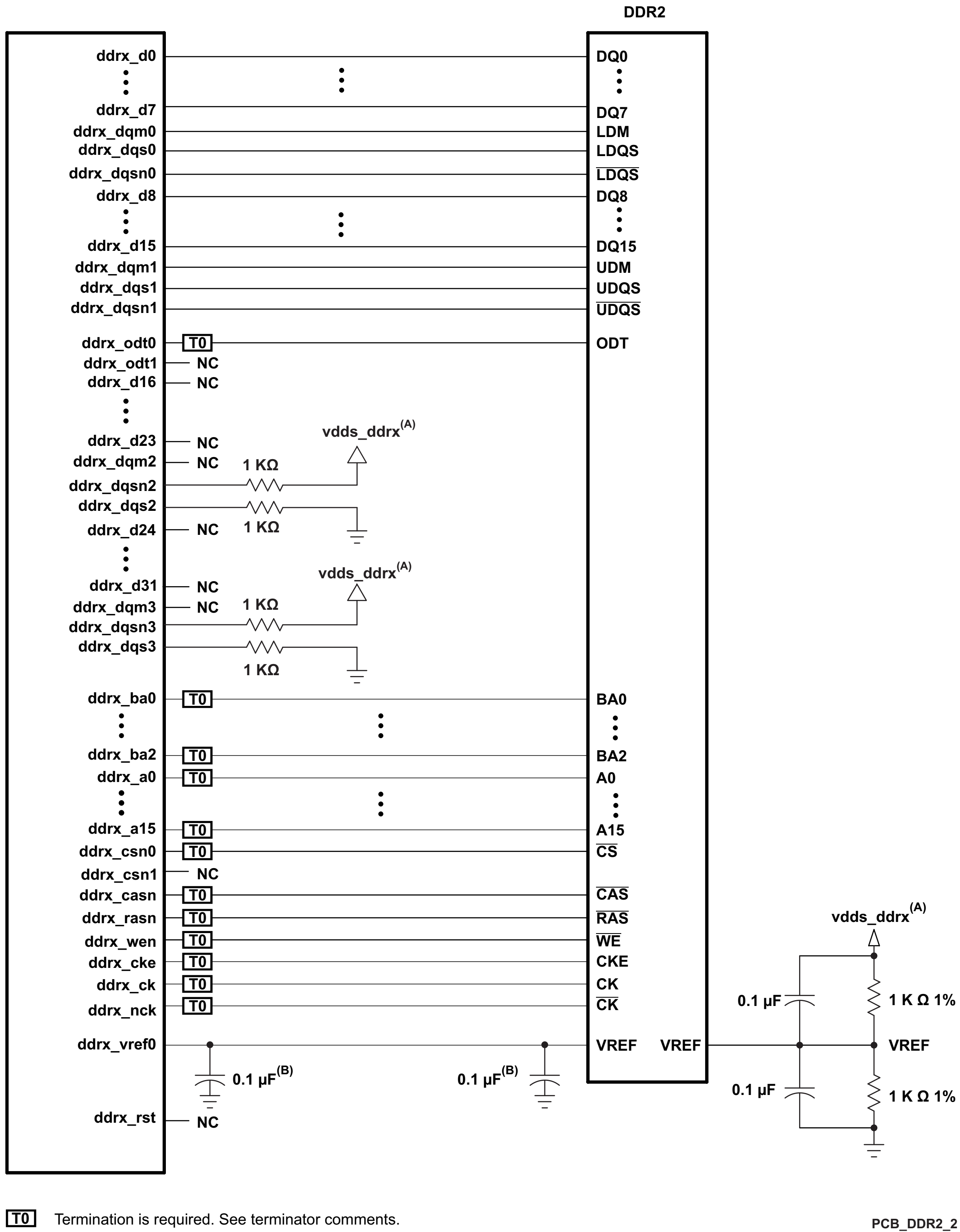
When not using all or part of a DDR2 interface, the proper method of handling the unused pins is to tie off the ddr*x*_dqs*i* pins to ground via a 1k-Ω resistor and to tie off the ddrx_dqsn*i* pins to the corresponding vdds_ddr*x* supply via a 1k-Ω resistor. This needs to be done for each byte not used. The vdds_ddr*x* and ddr*x*_vref0 power supply pins need to be connected to their respective power supplies even if DDR*x* is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.



A. vdds_ddrx is the power supply for the DDR2 memories and the Device DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

Figure 7-50. 32-Bit DDR2 High-Level Schematic



T0 Termination is required. See terminator comments.

A. vdds_ddrx is the power supply for the DDR2 memories and the Device DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

Figure 7-51. 16-Bit DDR2 High-Level Schematic

7.7.2.2.2 Compatible JEDEC DDR2 Devices

Table 7-29 shows the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-800 speed grade DDR2 devices.

Table 7-29. Compatible JEDEC DDR2 Devices (Per Interface)

NO.	PARAMETER	MIN	MAX	UNIT
CJ21	JEDEC DDR2 device speed grade(1)	DDR2-800		
CJ22	JEDEC DDR2 device bit width	x16	x16	Bits
CJ23	JEDEC DDR2 device count(2)	1	2	Devices
CJ24	JEDEC DDR2 device ball count(3)	84	92	Balls

(1) Higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.

(2) One DDR2 device is used for a 16-bit DDR2 memory system. Two DDR2 devices are used for a 32-bit DDR2 memory system.

(3) The 92-ball devices are retained for legacy support. New designs will migrate to 84-ball DDR2 devices. Electrically, the 92- and 84-ball DDR2 devices are the same.

7.7.2.2.3 PCB Stackup

The minimum stackup required for routing the Device is a six-layer stackup as shown in Table 7-30. Additional layers may be added to the PCB stackup to accommodate other circuitry or to reduce the size of the PCB footprint.

Table 7-30. Minimum PCB Stackup

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal routing
5	Plane	Ground
6	Signal	Bottom routing mostly vertical

Complete stackup specifications are provided in Table 7-31.

Table 7-31. PCB Stackup Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT
PS21	PCB routing/plane layers	6			
PS22	Signal routing layers	3			
PS23	Full ground reference layers under DDR2 routing region(1)	1			
PS24	Full vdds_ddr*x* power reference layers under the DDR2 routing region(1)	1			
PS25	Number of reference plane cuts allowed within DDR routing region(2)			0	
PS26	Number of layers between DDR2 routing layer and reference plane(3)			0	
PS27	PCB routing feature size		4		Mils
PS28	PCB trace width, w		4		Mils
PS29	Single-ended impedance, Zo	50		75	Ω
PS210	Impedance control(5)	Z-5	Z	Z+5	Ω

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers. A full ground reference layer should be placed adjacent to each DDR routing layer in PCB stack up.

(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.

(5) Z is the nominal singled-ended impedance selected for the PCB specified by PS29.

7.7.2.2.4 Placement

Figure 7-52 shows the required placement for the Device as well as the DDR2 devices. The dimensions for this figure are defined in Table 7-32. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR2 device is omitted from the placement.

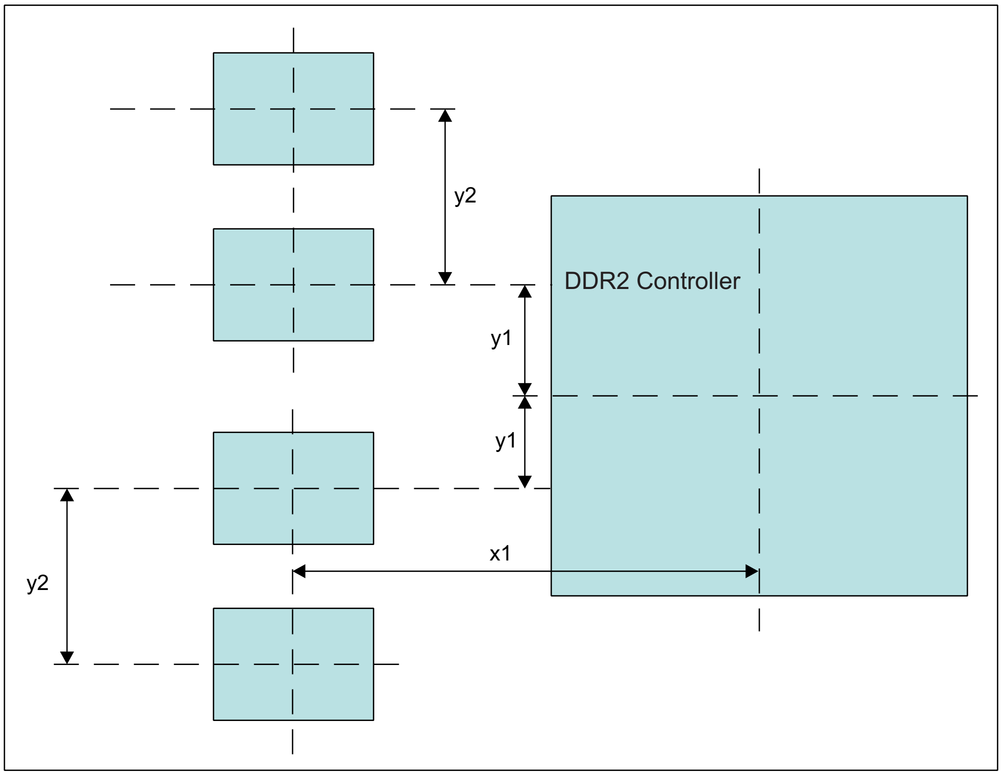


Figure 7-52. Device and DDR2 Device Placement

Table 7-32. Placement Specifications DDR2

NO.	PARAMETER	MIN	MAX	UNIT
KOD21	X1		2000	Mils
KOD22	Y1		500	Mils
KOD23	Y2		1300	Mils
KOD24	DDR2 keepout region (1)			
KOD25	Clearance from non-DDR2 signal to DDR2 keepout region (2) (3)	4		W

(1) DDR2 keepout region to encompass entire DDR2 routing area.

(2) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

(3) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR2 and should be separated by this specification.

7.7.2.2.5 DDR2 Keepout Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keepout region is defined for this purpose and is shown in Figure 7-53. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 7-32.

The region shown in Table 7-32 should encompass all the DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keepout region. Non-DDR2 signals may be routed in the region, provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the vdds_ddr*x* power plane should cover the entire keepout region. Routes for the two DDR interfaces must be separated by at least 4x; the more separation, the better.

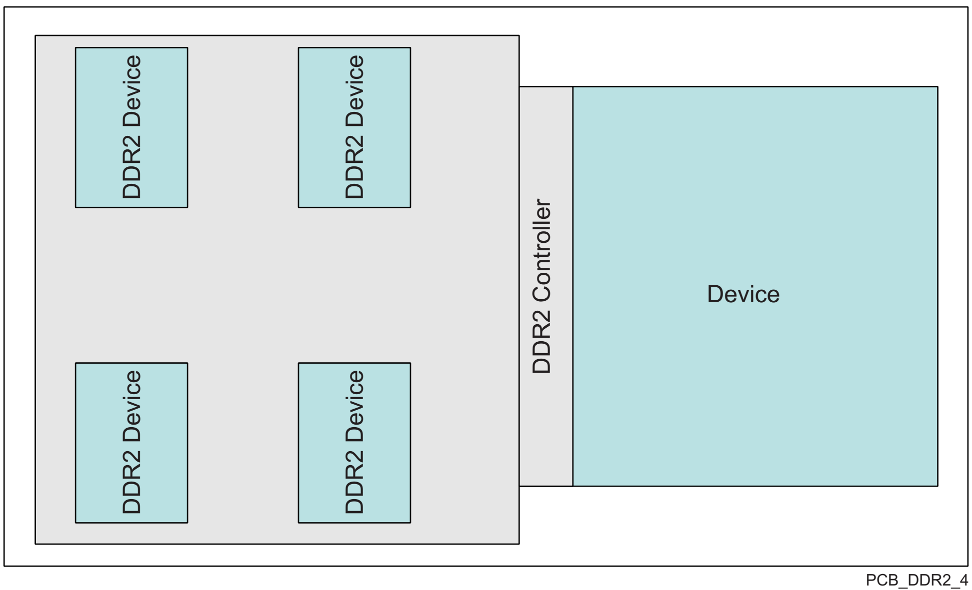


Figure 7-53. DDR2 Keepout Region

7.7.2.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 7-33 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR2 interfaces and DDR2 device. Additional bulk bypass capacitance may be needed for other circuitry.

Table 7-33. Bulk Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
BC21	vdds_ddrx bulk bypass capacitor (≥ 1 µF) count(1)		1		Devices
BC22	vdds_ddrx bulk bypass total capacitance		22		µF

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR2 signal routing.

7.7.2.2.7 High-Speed Bypass Capacitors

TI recommends that a PDN/power integrity analysis is performed to ensure that capacitor selection and placement is optimal for a given implementation. This section provides guidelines that can serve as a good starting point.

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 7-34 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. HS bypass capacitor value is < 1 μF
3. Minimize the distance from the bypass cap to the pins/balls being bypassed.
4. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
5. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
6. Minimize via sharing. Note the limites on via sharing shown in Table 7-34.

Table 7-34. High-Speed Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
HS21	HS bypass capacitor package size(1)		0201	0402	10 Mils
HS22	Distance, HS bypass capacitor to processor being bypassed(2)(3)(4)			400(12)	Mils
HS23	processor HS bypass capacitor count (12)	See Table 7-3 and (11)			Devices
HS24	processor HS bypass capacitor total capacitance per vdds_ddrx rail (12)	See Table 7-3 and (11)			μF
HS25	Number of connection vias for each device power/ground ball per vdds_ddrx rail (5)	1			Vias
HS26	Trace length from device power/ground ball to connection via(2)		35	70	Mils
HS27	Distance, HS bypass capacitor to DDR device being bypassed(6)			150	Mils
HS28	Number of connection vias for each HS capacitor(8)(9)		4 (14)		Vias
HS29	DDR2 device HS bypass capacitor count(7)		12 (13)		Devices
HS210	DDR2 device HS bypass capacitor total capacitance(7)	0.85			μF
HS211	Trace length from bypass capacitor connect to connection via(2)(9)		35	100	Mils
HS212	Number of connection vias for each DDR2 device power/ground ball(10)	1			Vias
HS213	Trace length from DDR2 device power/ground ball to connection via(2)(8)		35	60	Mils

(1) LxW, 10-mil units, that is, a 0402 is a 40×20-mil surface-mount capacitor.
(2) Closer/shorter is better.
(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.
(4) Three of these capacitors should be located underneath the processor, between the cluster of vdds_ddr*x* balls and ground balls, between the DDR interfaces on the package.
(5) See the Via Channel™ escape for the processor package.
(6) Measured from the DDR2 device power/ground ball to the center of the capacitor package.
(7) Per DDR2 device.
(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.
(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.
(10) Up to a total of two pairs of DDR power/ground balls may share a via.
(11) The capacitor recommendations in this data manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.
(12) For more information, see Section 7.3, *Core Power Domains* .
(13) For more information refer to DDR2 specification.
(14) Preferred configuration is 4 vias: 2 to power and 2 to ground.

7.7.2.2.8 Net Classes

Table 7-35 lists the clock net classes for the DDR2 interface. Table 7-36 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

Table 7-35. Clock Net Class Definitions

CLOCK NET CLASS	PIN NAMES
CK	ddr*x*_ck / ddr*x*_nck
DQS0	ddr*x*_dqs0 / ddr*x*_dqsn0
DQS1	ddr*x*_dqs1 / ddr*x*_dqsn1
DQS2(1)	ddr*x*_dqs2 / ddr*x*_dqsn2
DQS3(1)	ddr*x*_dqs3 / ddr*x*_dqsn3

(1) Only used on 32-bit wide DDR2 memory systems.

Table 7-36. Signal Net Class Definitions

SIGNAL NET CLASS	ASSOCIATED CLOCK NET CLASS	PIN NAMES
ADDR_CTRL	CK	ddr*x*_ba[2:0], ddr*x*_a[14:0], ddr*x*_csn*j*, ddr*x*_casn, ddr*x*_rasn, ddr*x*_wen, ddr*x*_cke, ddr*x*_odt*i*
DQ0	DQS0	ddr*x*_d[7:0], ddr*x*_dqm0
DQ1	DQS1	ddr*x*_d[15:8], ddr*x*_dqm1
DQ2(1)	DQS2	ddr*x*_d[23:16], ddr*x*_dqm2
DQ3(1)	DQS3	ddr*x*_d[31:24], ddr*x*_dqm3

(1) Only used on 32-bit wide DDR2 memory systems.

7.7.2.2.9 DDR2 Signal Termination

Signal terminators are required in CK and ADDR_CTRL net classes. Serial terminators may be used on data lines to reduce EMI risk; however, serial terminations are the only type permitted. ODTs are integrated on the data byte net classes. They should be enabled to ensure signal integrity.Table 7-37 shows the specifications for the series terminators.

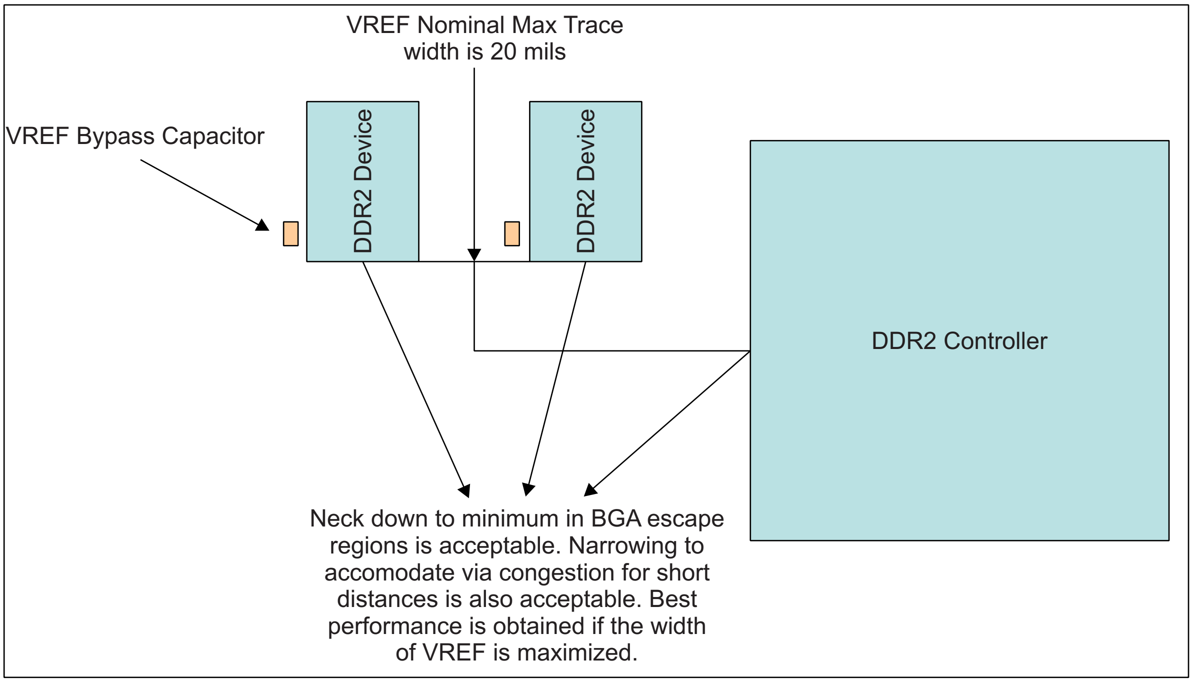
Table 7-37. DDR2 Signal Terminations

NO.	PARAMETER	MIN	TYP	MAX	UNIT
ST21	CK net class(1)(2)	0		10	Ω
ST22	ADDR_CTRL net class(1) (2)(3)(4)	0	22	Zo	Ω
ST23	Data byte net classes (DQS0-DQS3, DQ0-DQ3)(5)	0		Zo	Ω

(1) Only series termination is permitted, parallel or SST specifically disallowed on board.
(2) Only required for EMI reduction.
(3) Terminator values larger than typical only recommended to address EMI issues.
(4) Termination value should be uniform across net class.
(5) No external terminations allowed for data byte net classes. ODT is to be used.

7.7.2.2.10 VREF Routing

VREF (ddr*x*_vref0) is used as a reference by the input buffers of the DDR2 memories as well as the processor. VREF is intended to be half the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 7-51. Other methods of creating VREF are not recommended. Figure 7-54 shows the layout guidelines for VREF.

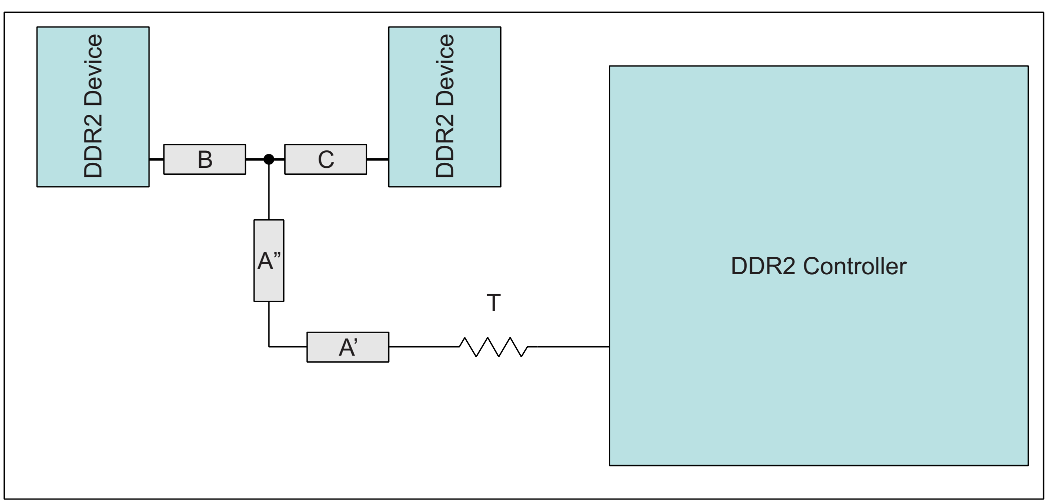


PCB_DDR2_5

Figure 7-54. VREF Routing and Topology

7.7.2.3 DDR2 CK and ADDR_CTRL Routing

Figure 7-55 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A = (A'+A") should be maximized.



PCB_DDR2_6

Figure 7-55. CK and ADDR_CTRL Routing and Topology

Table 7-38. CK and ADDR_CTRL Routing Specification [(1)]

NO.	PARAMETER	MIN	MAX	UNIT
RSC21	Center-to-center ddrx_ck - ddrx_nck spacing		2w	
RSC22	ddrx_ck / ddrx_nck skew[(1)]		5	ps
RSC23	CK A-to-B/A-to-C skew mismatch[(2)]		10	ps

Table 7-38. CK and ADDR_CTRL Routing Specification [(1)] (continued)

NO.	PARAMETER	MIN	MAX	UNIT
RSC24	CK B-to-C skew mismatch		10	ps
RSC25	Center-to-center CK to other DDR2 trace spacing[(3)]	4w		
RSC26	CK/ADDR_CTRL trace length[(4)]		680	ps
RSC27	ADDR_CTRL-to-CK skew mismatch		25	ps
RSC28	ADDR_CTRL-to-ADDR_CTRL skew mismatch		25	ps
RSC29	Center-to-center ADDR_CTRL to other DDR2 trace spacing[(3)]	4w		
RSC210	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing[(3)]	3w		
RSC211	ADDR_CTRL A-to-B/A-to-C skew mismatch[(2)]		25	ps
RSC212	ADDR_CTRL B-to-C skew mismatch		25	ps

(1) The length of segment A = A' + A″ as shown in Figure 7-55.

(2) Series terminator, if used, should be located closest to the Device.

(3) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(4) This is the longest routing length of the CK and ADDR_CTRL net classes.

(5) Length of A should be maximized.

Figure 7-56 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

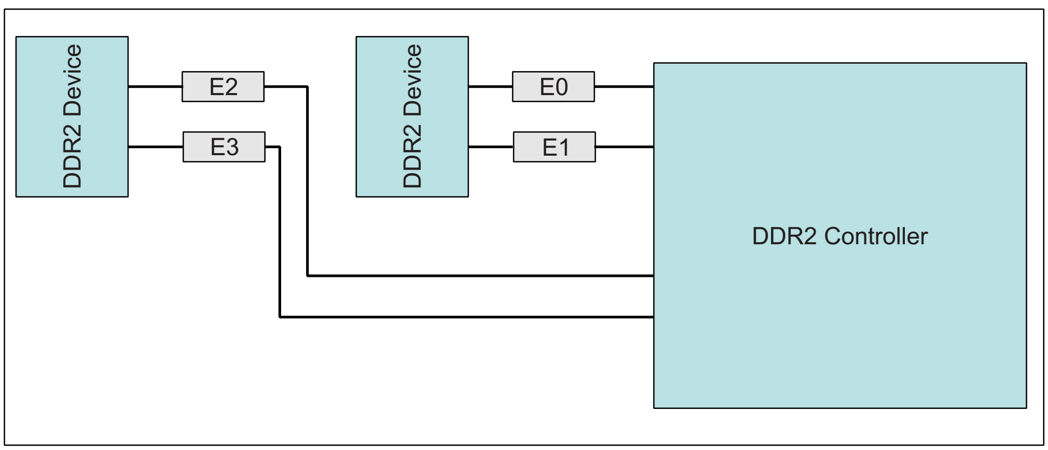


Figure 7-56. DQS and DQ Routing and Topology

Table 7-39. DQS and DQ Routing Specification

NO.	PARAMETER	MIN	MAX	UNIT
RSDQ21	Center-to-center DQS-DQSn spacing in E0|E1|E2|E3	2w		
RSDQ22	DQS-DQSn skew in E0|E1|E2|E3		5	ps
RSDQ23	Center-to-center DQS to other DDR2 trace spacing[(1)]	4w		
RSDQ24	DQS/DQ trace length [(2)(3)(4)]		325	ps
RSDQ25	DQ-to-DQS skew mismatch[(2)(3)(4)]		10	ps
RSDQ26	DQ-to-DQ skew mismatch[(2)(3)(4)]		10	ps
RSDQ27	DQ-to-DQ/DQS via count mismatch[(2)(3)(4)]		1	Vias
RSDQ28	Center-to-center DQ to other DDR2 trace spacing[(1)(5)]	4w		
RSDQ29	Center-to-center DQ to other DQ trace spacing[(1)(6)(7)]	3w		
RSDQ210	DQ/DQS E skew mismatch[(2)(3)(4)]		25	ps

(1) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) A 16-bit DDR memory system has two sets of data net classes; one for data byte 0, and one for data byte 1, each with an associated DQS (2 DQSs) per DDR EMIF used.
(3) A 32-bit DDR memory system has four sets of data net classes; one each for data bytes 0 through 3, and each associated with a DQS (4 DQSs) per DDR EMIF used.
(4) There is no need, and it is not recommended, to skew match across data bytes; that is, from DQS0 and data byte 0 to DQS1 and data byte 1.
(5) DQs from other DQS domains are considered *other DDR2 trace*.
(6) DQs from other data bytes are considered *other DDR2 trace*.
(7) This is the longest routing distance of each of the DQS and DQ net classes.

7.7.3 DDR3 Board Design and Layout Guidelines

7.7.3.1 Board Designs

TI only supports board designs using DDR3 memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3 memory controller are shown in Table 7-40 and Figure 7-57.

Table 7-40. Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(DDR\_CLK)}$	Cycle time, DDR_CLK	1.5	2.5[(1)]	ns

(1) This is the absolute maximum the clock period can be. Actual maximum clock period may be limited by DDR3 speed grade and operating frequency (see the DDR3 memory device data sheet).

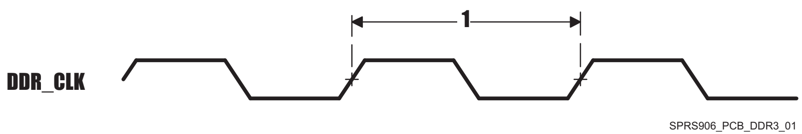


Figure 7-57. DDR3 Memory Controller Clock Timing

7.7.3.2 DDR3 EMIF

The processor contains one DDR3 EMIF.

7.7.3.3 DDR3 Device Combinations

Because there are several possible combinations of device counts and single- or dual-side mounting, Table 7-41 summarizes the supported device configurations.

Table 7-41. Supported DDR3 Device Combinations

NUMBER OF DDR3 DEVICES	DDR3 DEVICE WIDTH (BITS)	MIRRORED?	DDR3 EMIF WIDTH (BITS)
1	16	N	16
2	8	Y[(1)]	16
2	16	N	32
2	16	Y[(1)]	32
3	16	N[(3)]	32
4	8	N	32
4	8	Y[(2)]	32
5	8	N [(3)]	32

(1) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.

(2) This is two mirrored pairs of DDR3 devices.

(3) Three or five DDR3 device combination is not available on this device, but combination types are retained for consistency with the DRA7xx family of devices.

7.7.3.4 DDR3 Interface Schematic

7.7.3.4.1 32-Bit DDR3 Interface

The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. Figure 7-58 and Figure 7-59 show the schematic connections for 32-bit interfaces using ×16 devices.

7.7.3.4.2 16-Bit DDR3 Interface

Note that the 16-bit wide interface schematic is practically identical to the 32-bit interface (see Figure 7-58 and Figure 7-59); only the high-word DDR memories are removed and the unused DQS inputs are tied off.

When not using all or part of a DDR interface, the proper method of handling the unused pins is to tie off the ddrx_dqs*i* pins to ground via a 1-kΩ resistor and to tie off the ddrx_dqsn*i* pins to the corresponding vdds_ddr*x* supply via a 1-kΩ resistor. This needs to be done for each byte not used. Although these signals have internal pullups and pulldowns, external pullups and pulldowns provide additional protection against external electrical noise causing activity on the signals.

The vdds_ddr*x* and ddrx_vref0 power supply pins need to be connected to their respective power supplies even if ddrx is not being used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.

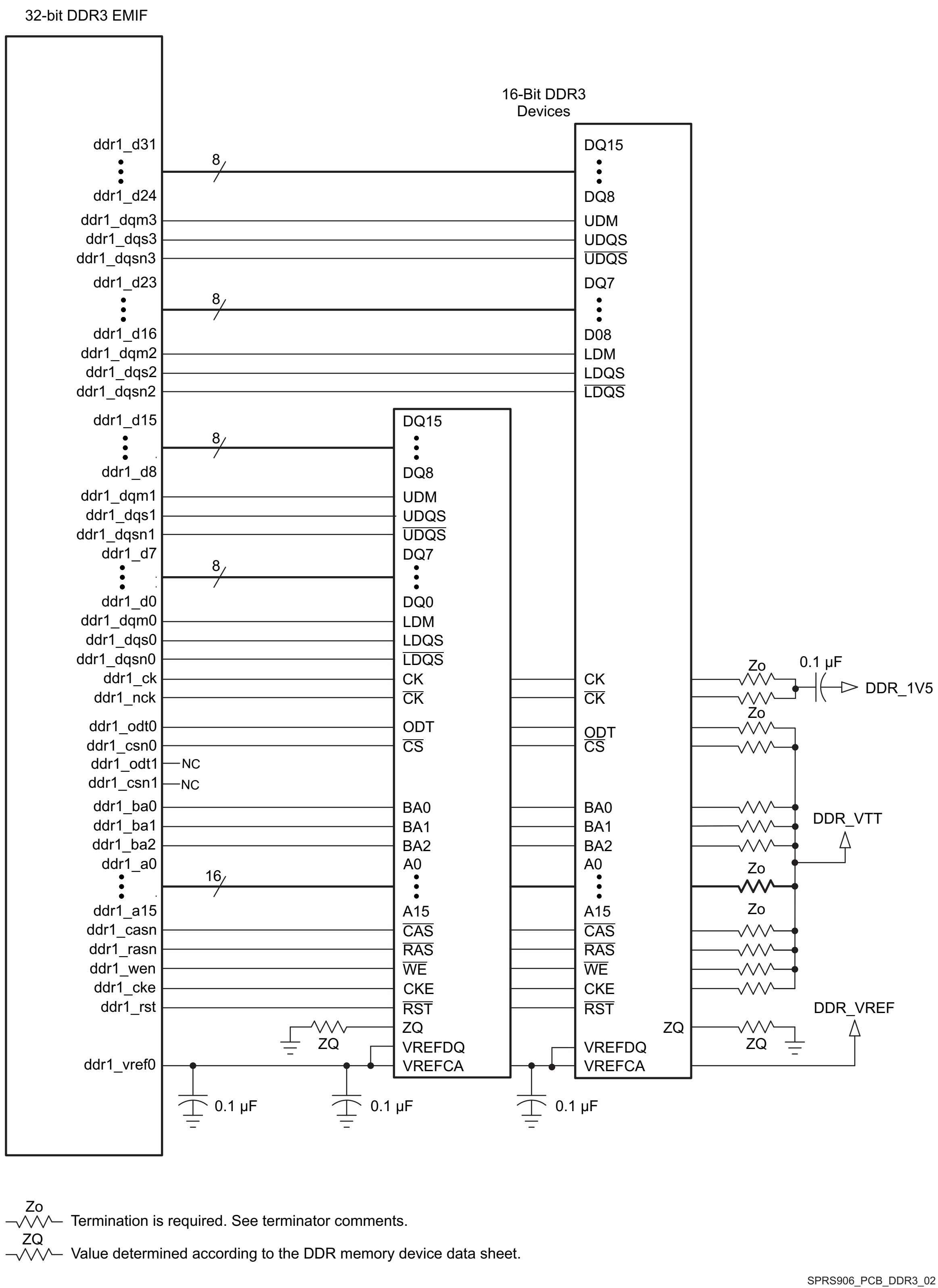


Figure 7-58. 32-Bit, One-Bank DDR3 Interface Schematic Using Two 16-Bit DDR3 Devices

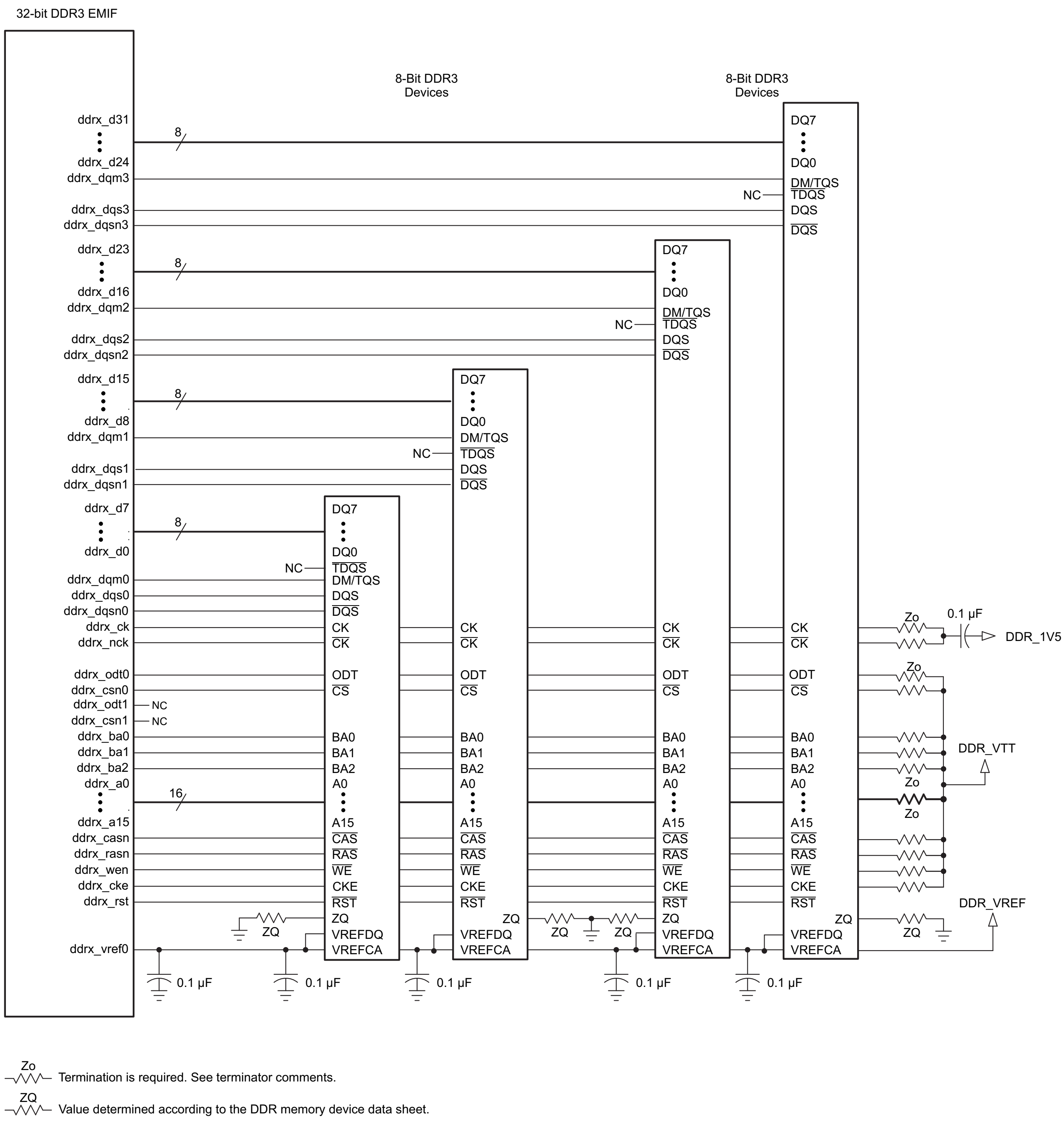


Figure 7-59. 32-Bit, One-Bank DDR3 Interface Schematic Using Four 8-Bit DDR3 Devices

7.7.3.5 Compatible JEDEC DDR3 Devices

Table 7-42 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface. Generally, the DDR3 interface is compatible with DDR3-1333 devices in the x8 or x16 widths.

Table 7-42. Compatible JEDEC DDR3 Devices (Per Interface)

NO.	PARAMETER	CONDITION	MIN	MAX	UNIT
1	JEDEC DDR3 device speed grade[(1)]	DDR clock rate = 400 MHz	DDR3-800	DDR3-1600	
		400 MHz< DDR clock rate ≤ 533 MHz	DDR3-1066	DDR3-1600	
		533 MHz< DDR clock rate ≤ 667 MHz	DDR3-1333	DDR3-1600	
2	JEDEC DDR3 device bit width		x8	x16	Bits
3	JEDEC DDR3 device count[(2)]		2	4	Devices

(1) Refer to Table 7-40, Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller for the range of supported DDR clock rates.

(2) For valid DDR3 device configurations and device counts, see Section 7.7.3.4, Figure 7-58, and Figure 7-59.

7.7.3.6 PCB Stackup

The minimum stackup for routing the DDR3 interface is a six-layer stack up as shown in Table 7-43. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI/EMI performance, or to reduce the size of the PCB footprint. Complete stackup specifications are provided in Table 7-44.

Table 7-43. Six-Layer PCB Stackup Suggestion

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly vertical
2	Plane	Ground
3	Plane	Split power plane
4	Plane	Split power plane or Internal routing
5	Plane	Ground
6	Signal	Bottom routing mostly horizontal

Table 7-44. PCB Stackup Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT
PS1	PCB routing/plane layers	6			
PS2	Signal routing layers	3			
PS3	Full ground reference layers under DDR3 routing region(1)	1			
PS4	Full 1.5-V power reference layers under the DDR3 routing region(1)	1			
PS5	Number of reference plane cuts allowed within DDR routing region(2)			0	
PS6	Number of layers between DDR3 routing layer and reference plane(3)			0	
PS7	PCB routing feature size		4		Mils
PS8	PCB trace width, w		4		Mils
PS9	Single-ended impedance, Zo	50		75	Ω
PS10	Impedance control(5)	Z-5	Z	Z+5	Ω

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.

(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.

(5) Z is the nominal singled-ended impedance selected for the PCB specified by PS9.

7.7.3.7 Placement

Figure 7-60 shows the required placement for the processor as well as the DDR3 devices. The dimensions for this figure are defined in Table 7-45. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3 devices are omitted from the placement.

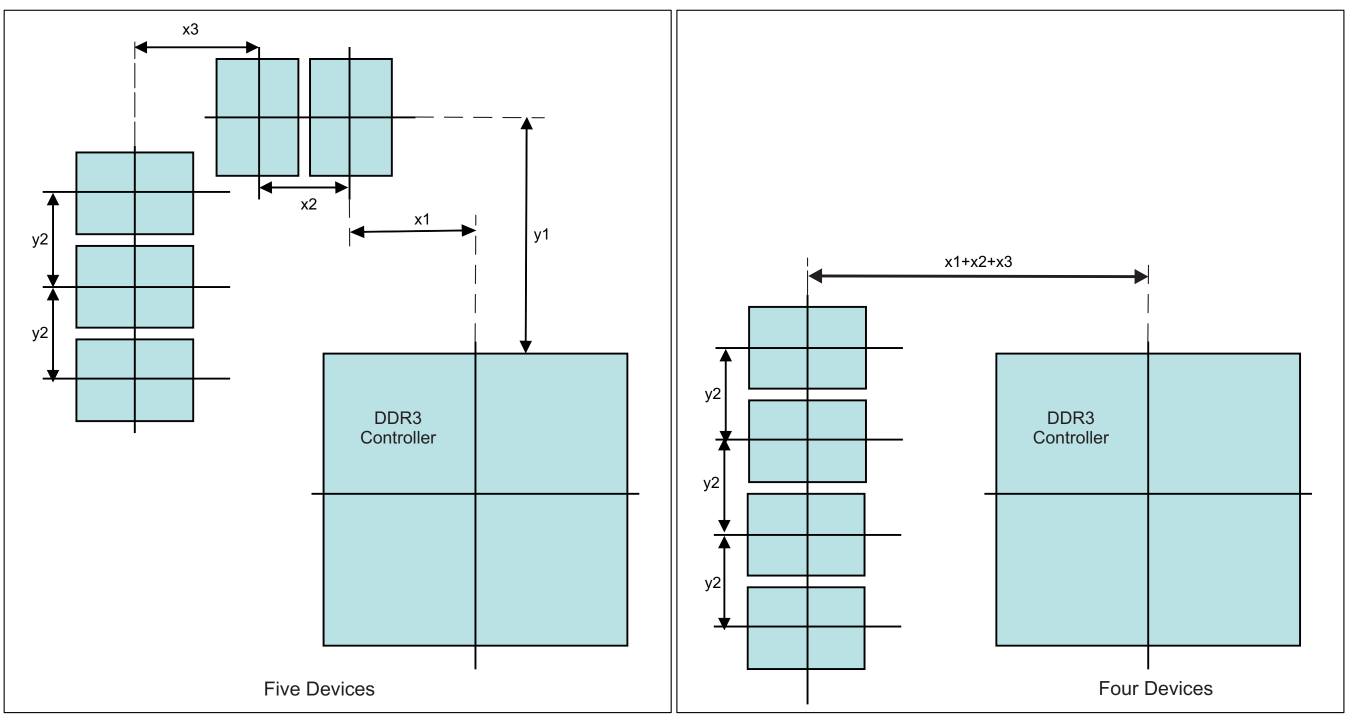


Figure 7-60. Placement Specifications

Table 7-45. Placement Specifications DDR3

NO.	PARAMETER	MIN	MAX	UNIT
KOD31	X1		500	Mils
KOD32	X2		600	Mils
KOD33	X3		600	Mils
KOD34	Y1		1800	Mils
KOD35	Y2		600	Mils
KOD36	DDR3 keepout region (1)			
KOD37	Clearance from non-DDR3 signal to DDR3 keepout region (2) (3)	4		W

(1) DDR3 keepout region to encompass entire DDR3 routing area.
(2) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.
(3) If a device has more than one DDR controller, the signals from the other controller(s) are considered non-DDR3 and should be separated by this specification.

7.7.3.8 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in Figure 7-61. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 7-45. Non-DDR3 signals should not be routed on the DDR signal layers within the DDR3 keepout region. Non-DDR3 signals may be routed in the region, provided they are routed on layers separated from the DDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.5-V DDR3 power plane should cover the entire keepout region. Also note that the two signals from the DDR3 controller should be separated from each other by the specification in Table 7-45 (see KOD37).

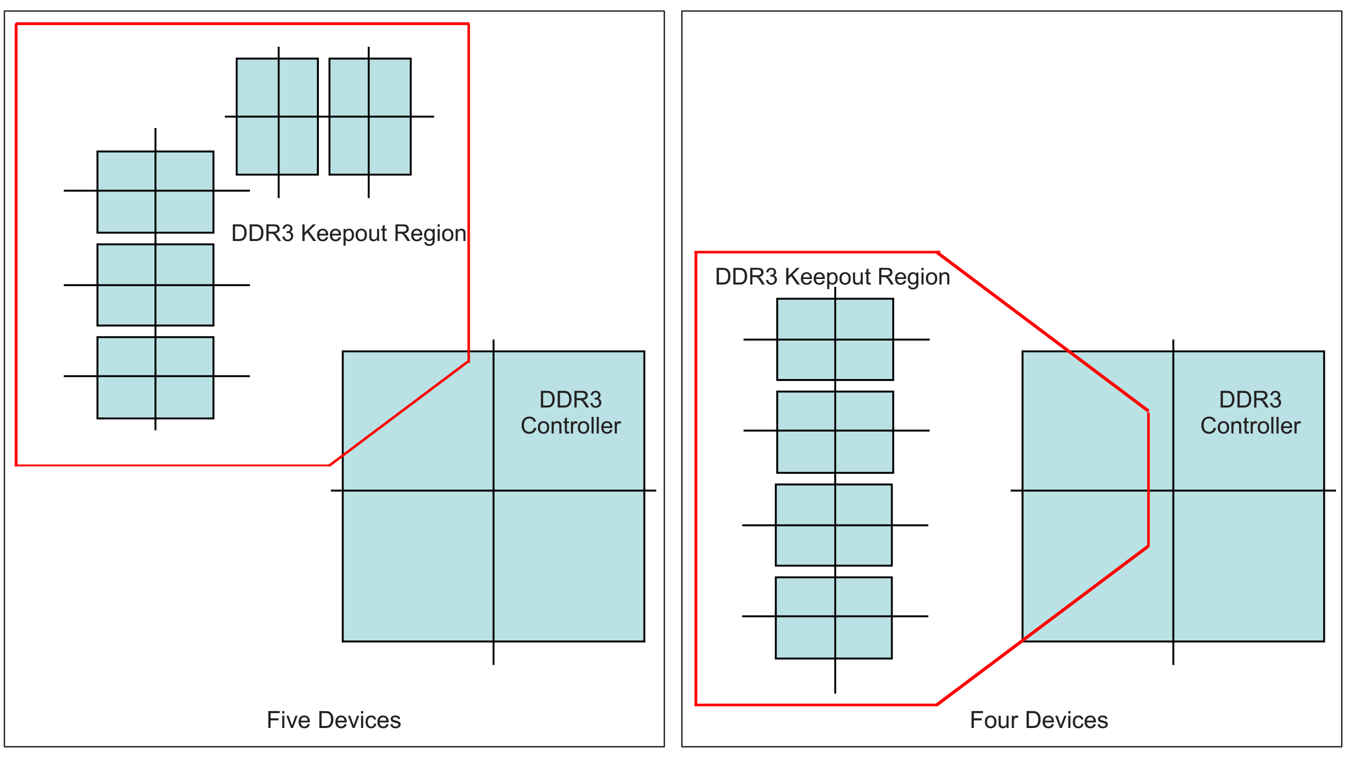


Figure 7-61. DDR3 Keepout Region

7.7.3.9 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. Table 7-46 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 controllers and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry.

Table 7-46. Bulk Bypass Capacitors

NO.	PARAMETER	MIN	MAX	UNIT
1	vdds_ddr*x* bulk bypass capacitor count(1)	1		Devices
2	vdds_ddr*x* bulk bypass total capacitance	22		µF

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

7.7.3.10 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critcal for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 7-47 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the pins/balls being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limites on via sharing shown in Table 7-47.

Table 7-47. High-Speed Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	HS bypass capacitor package size(1)		0201	0402	10 Mils
2	Distance, HS bypass capacitor to processor being bypassed(2)(3)(4)			400	Mils
3	Processor HS bypass capacitor count per vdds_ddrx rail(12)	See Table 7-3 and (11)			Devices
4	Processor HS bypass capacitor total capacitance per vdds_ddrx rail(12)	See Table 7-3 and (11)			µF
5	Number of connection vias for each device power/ground ball(5)				Vias
6	Trace length from device power/ground ball to connection via(2)		35	70	Mils
7	Distance, HS bypass capacitor to DDR device being bypassed(6)			150	Mils
8	DDR3 device HS bypass capacitor count(7)	12			Devices
9	DDR3 device HS bypass capacitor total capacitance(7)	0.85			µF
10	Number of connection vias for each HS capacitor(8)(9)	2			Vias
11	Trace length from bypass capacitor connect to connection via(2)(9)		35	100	Mils
12	Number of connection vias for each DDR3 device power/ground ball(10)	1			Vias
13	Trace length from DDR3 device power/ground ball to connection via(2)(8)		35	60	Mils

(1) LxW, 10-mil units, that is, a 0402 is a 40×20-mil surface-mount capacitor.

(2) Closer/shorter is better.

(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.

(4) Three of these capacitors should be located underneath the processor, between the cluster of DDR_1V5 balls and ground balls, between the DDR interfaces on the package.

(5) See the Via Channel™ escape for the processor package.

(6) Measured from the DDR3 device power/ground ball to the center of the capacitor package.

(7) Per DDR3 device.

(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.

(10) Up to a total of two pairs of DDR power/ground balls may share a via.

(11) The capacitor recommendations in this Data Manual reflect only the needs of this processor. Please see the memory vendor's guidelines for determining the appropriate decoupling capacitor arrangement for the memory device itself.

(12) For more information, see Section 7.3, *Core Power Domains*.

7.7.3.10.1 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Because these are returns for signal current, the signal via size may be used for these capacitors.

7.7.3.11 Net Classes

Table 7-48 lists the clock net classes for the DDR3 interface. Table 7-49 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

Table 7-48. Clock Net Class Definitions

CLOCK NET CLASS	processor PIN NAMES
CK	ddrx_ck/ddrx_nck
DQS0	ddrx_dqs0 / ddrx_dqsn0
DQS1	ddrx_dqs1 / ddrx_dqsn1
DQS2[(1)]	ddrx_dqs2 / ddrx_dqsn2
DQS3[(1)]	ddrx_dqs3 / ddrx_dqsn3

(1) Only used on 32-bit wide DDR3 memory systems.

Table 7-49. Signal Net Class Definitions

SIGNAL NET CLASS	ASSOCIATED CLOCK NET CLASS	processor PIN NAMES
ADDR_CTRL	CK	ddr*x*_ba[2:0], ddr*x*_a[14:0], ddr*x*_csn*j*, ddr*x*_casn, ddr*x*_rasn, ddr*x*_wen, ddr*x*_cke, ddr*x*_odt*i*
DQ0	DQS0	ddr*x*_d[7:0], ddr*x*_dqm0
DQ1	DQS1	ddr*x*_d[15:8], ddr*x*_dqm1
DQ2[(1)]	DQS2	ddr*x*_d[23:16], ddr*x*_dqm2
DQ3[(1)]	DQS3	ddr*x*_d[31:24], ddr*x*_dqm3

(1) Only used on 32-bit wide DDR3 memory systems.

7.7.3.12 DDR3 Signal Termination

Signal terminators are required for the CK and ADDR_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

7.7.3.13 VREF_DDR Routing

ddrx_vref0 (VREF) is used as a reference by the input buffers of the DDR3 memories as well as the processor. VREF is intended to be half the DDR3 power supply voltage and is typically generated with the DDR3 VDDS and VTT power supply. It should be routed as a nominal 20-mil wide trace with 0.1 µF bypass capacitors near each device connection. Narrowing of VREF is allowed to accommodate routing congestion.

7.7.3.14 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

7.7.3.15 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in Table 7-50.

7.7.3.15.1 Four DDR3 Devices

Four DDR3 devices are supported on the DDR EMIF consisting of four x8 DDR3 devices arranged as one bank (CS). These four devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

7.7.3.15.1.1 CK and ADDR_CTRL Topologies, Four DDR3 Devices

Figure 7-62 shows the topology of the CK net classes and Figure 7-63 shows the topology for the corresponding ADDR_CTRL net classes.

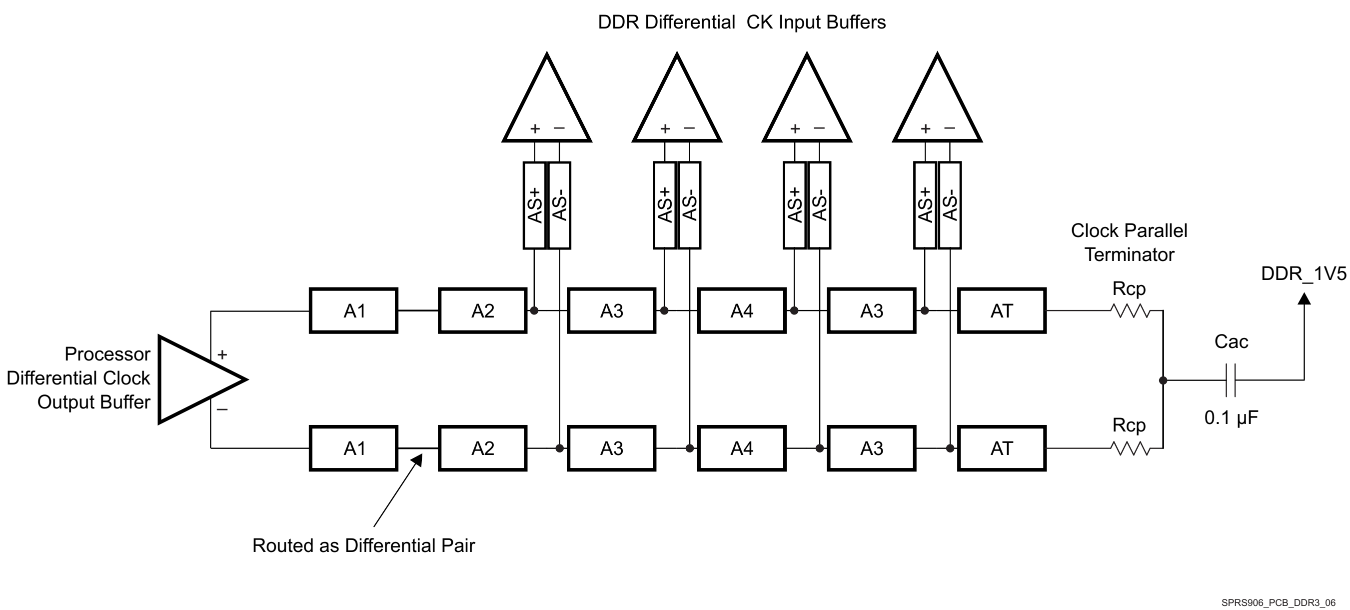


Figure 7-62. CK Topology for Four x8 DDR3 Devices

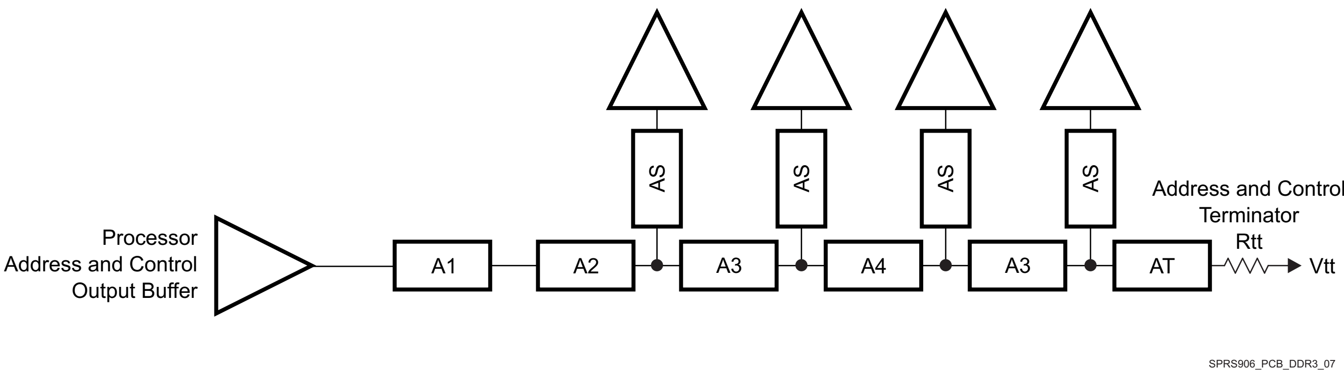


Figure 7-63. ADDR_CTRL Topology for Four x8 DDR3 Devices

7.7.3.15.1.2 CK and ADDR_CTRL Routing, Four DDR3 Devices

Figure 7-64 shows the CK routing for four DDR3 devices placed on the same side of the PCB. Figure 7-65 shows the corresponding ADDR_CTRL routing.

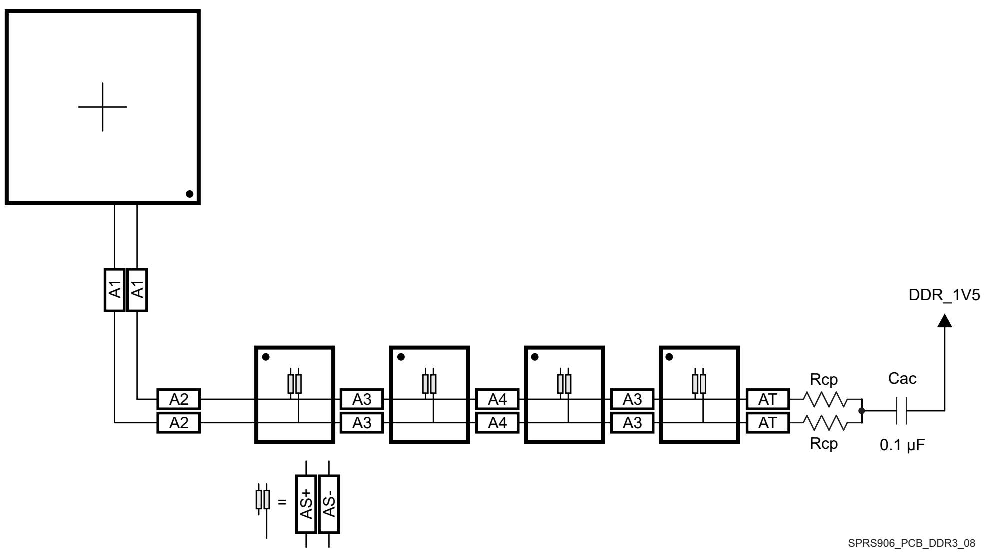


Figure 7-64. CK Routing for Four Single-Side DDR3 Devices

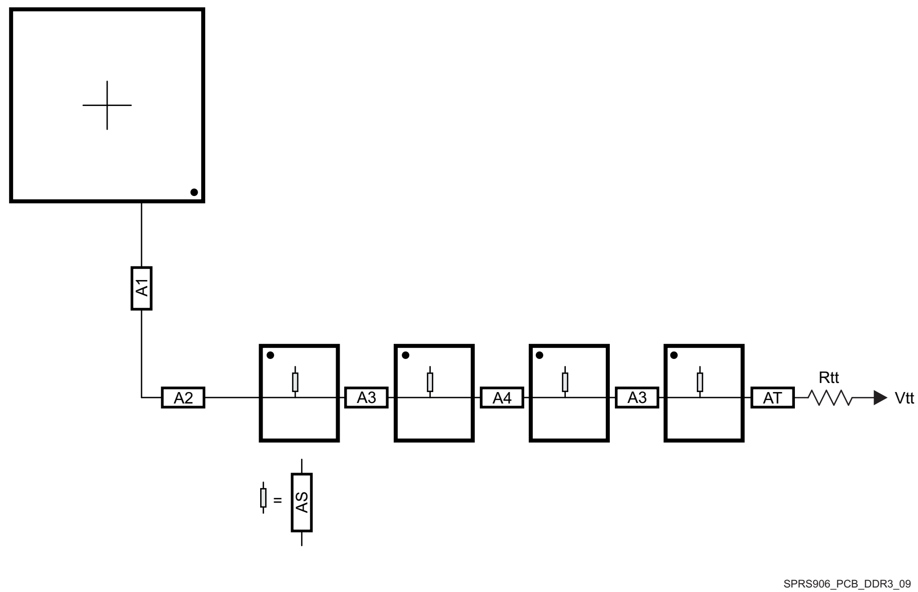


Figure 7-65. ADDR_CTRL Routing for Four Single-Side DDR3 Devices

To save PCB space, the four DDR3 memories may be mounted as two mirrored pairs at a cost of increased routing and assembly complexity. Figure 7-66 and Figure 7-67 show the routing for CK and ADDR_CTRL, respectively, for four DDR3 devices mirrored in a two-pair configuration.

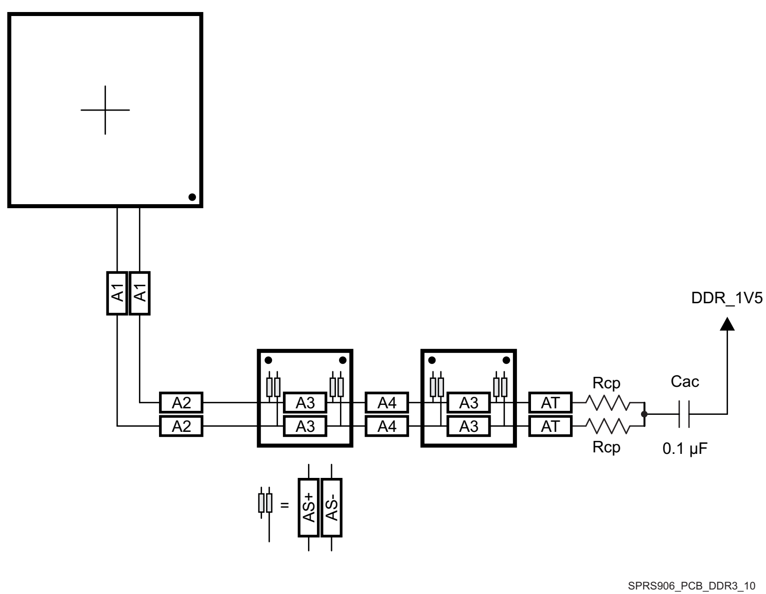


Figure 7-66. CK Routing for Four Mirrored DDR3 Devices

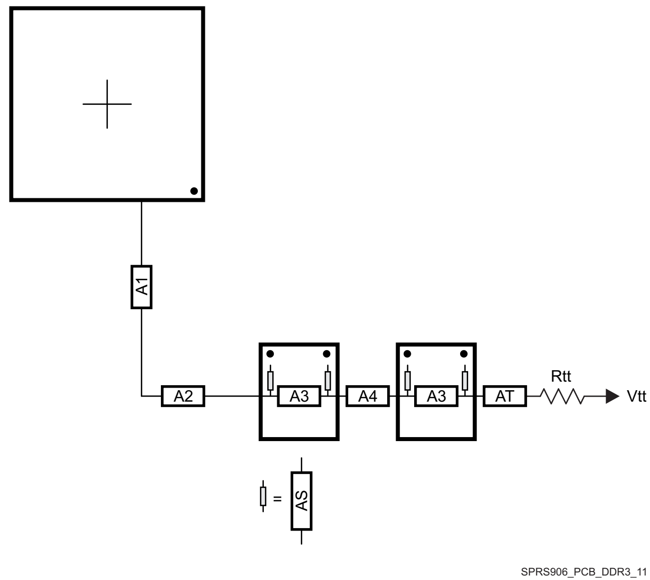


Figure 7-67. ADDR_CTRL Routing for Four Mirrored DDR3 Devices

7.7.3.15.2 Two DDR3 Devices

Two DDR3 devices are supported on the DDR EMIF consisting of two x8 DDR3 devices arranged as one bank (CS), 16 bits wide, or two x16 DDR3 devices arranged as one bank (CS), 32 bits wide. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

7.7.3.15.2.1 CK and ADDR_CTRL Topologies, Two DDR3 Devices

Figure 7-68 shows the topology of the CK net classes and Figure 7-69 shows the topology for the corresponding ADDR_CTRL net classes.

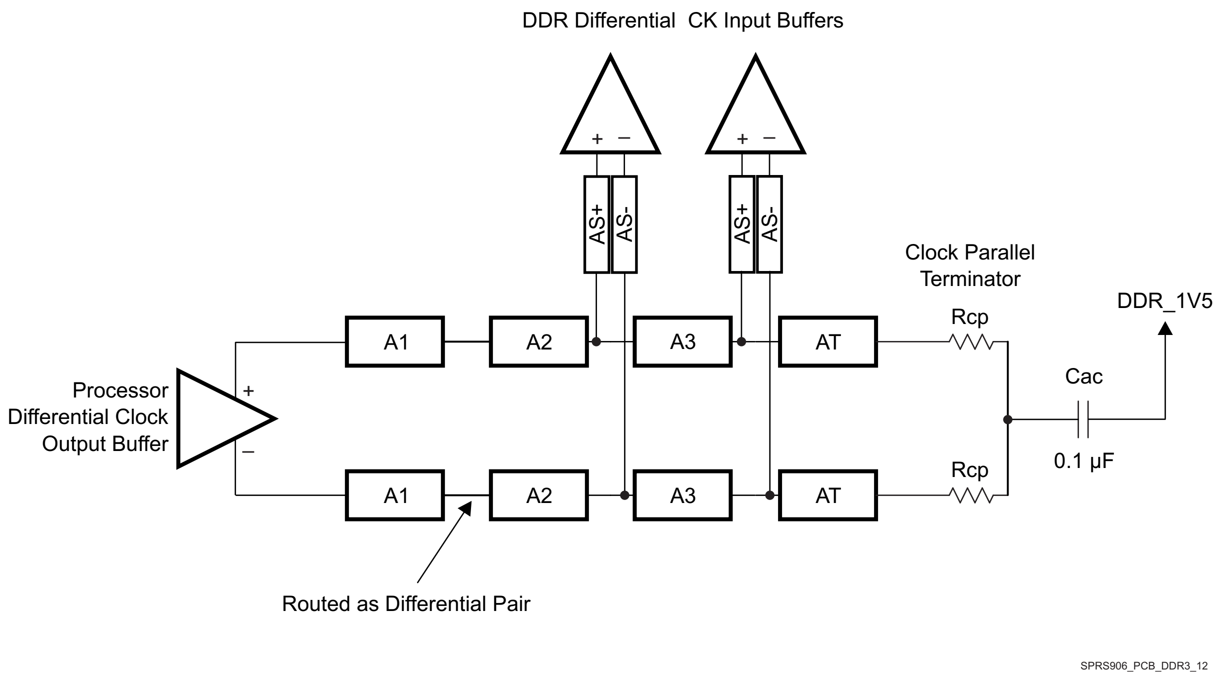


Figure 7-68. CK Topology for Two DDR3 Devices

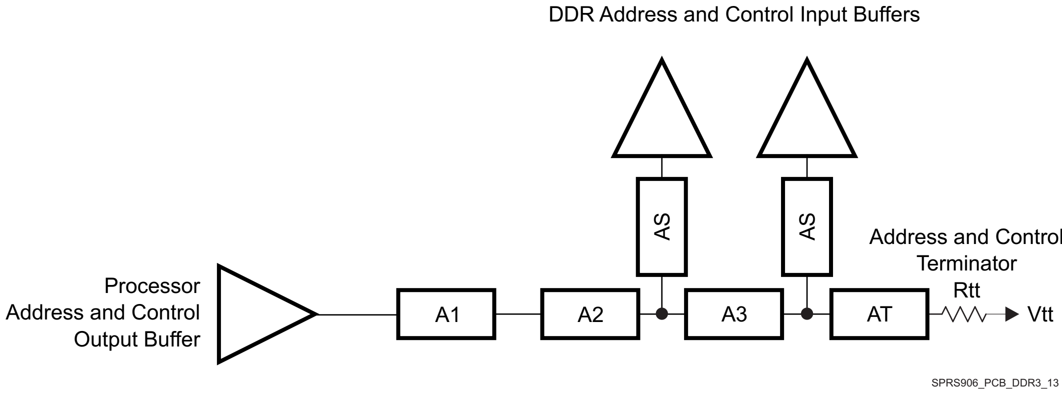


Figure 7-69. ADDR_CTRL Topology for Two DDR3 Devices

7.7.3.15.2.2 CK and ADDR_CTRL Routing, Two DDR3 Devices

Figure 7-70 shows the CK routing for two DDR3 devices placed on the same side of the PCB. Figure 7-71 shows the corresponding ADDR_CTRL routing.

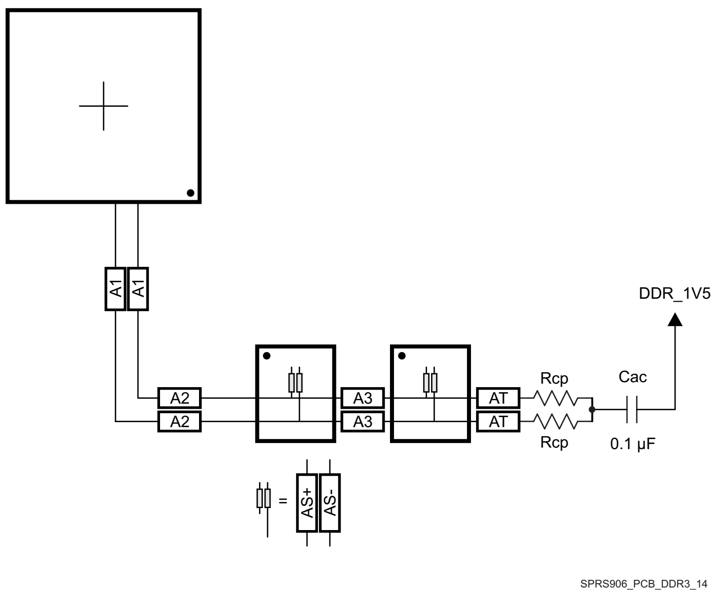


Figure 7-70. CK Routing for Two Single-Side DDR3 Devices

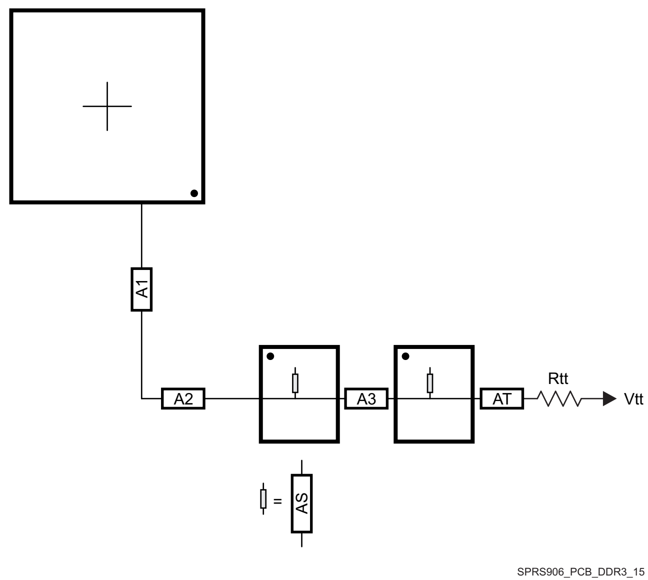


Figure 7-71. ADDR_CTRL Routing for Two Single-Side DDR3 Devices

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. Figure 7-72 and Figure 7-73 show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.

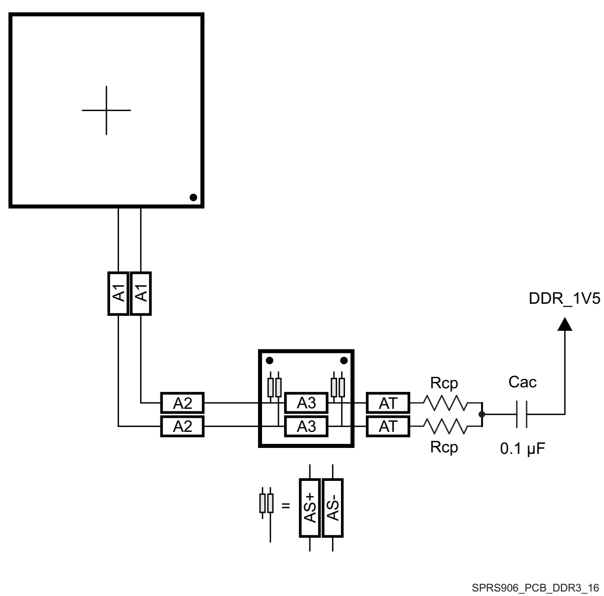


Figure 7-72. CK Routing for Two Mirrored DDR3 Devices

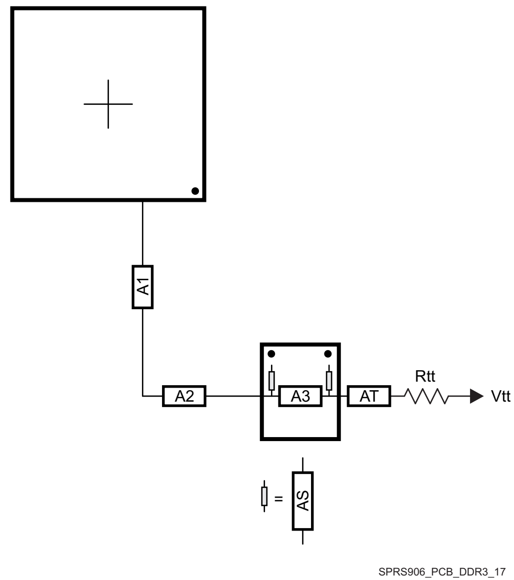


Figure 7-73. ADDR_CTRL Routing for Two Mirrored DDR3 Devices

7.7.3.15.3 One DDR3 Device

A single DDR3 device is supported on the DDR EMIF consisting of one x16 DDR3 device arranged as one bank (CS), 16 bits wide.

7.7.3.15.3.1 CK and ADDR_CTRL Topologies, One DDR3 Device

Figure 7-74 shows the topology of the CK net classes and Figure 7-75 shows the topology for the corresponding ADDR_CTRL net classes.

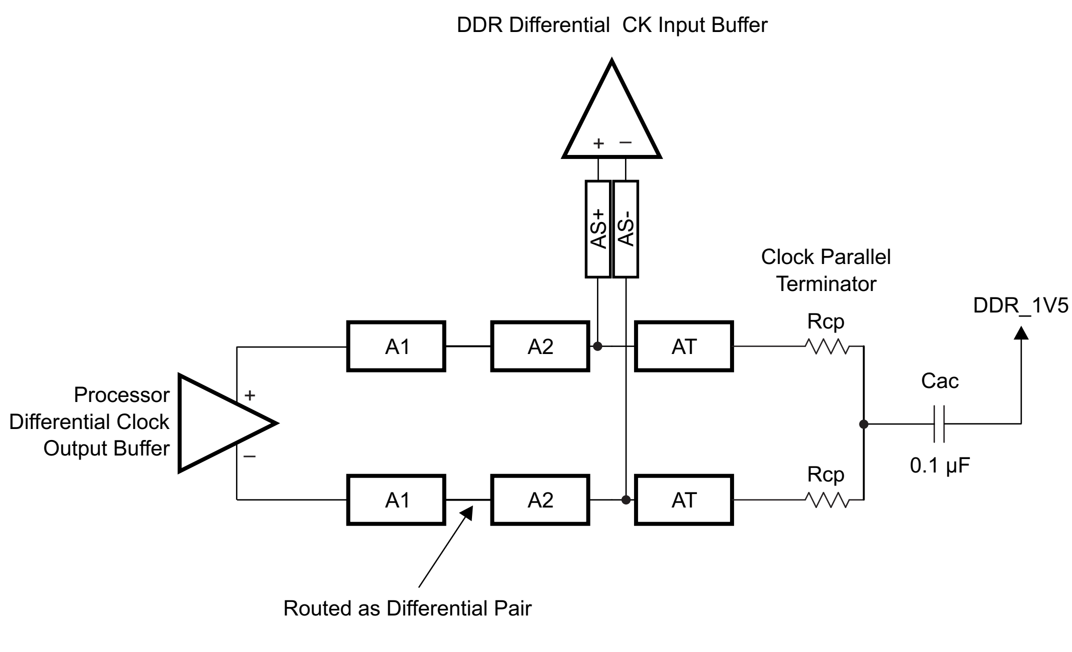


Figure 7-74. CK Topology for One DDR3 Device

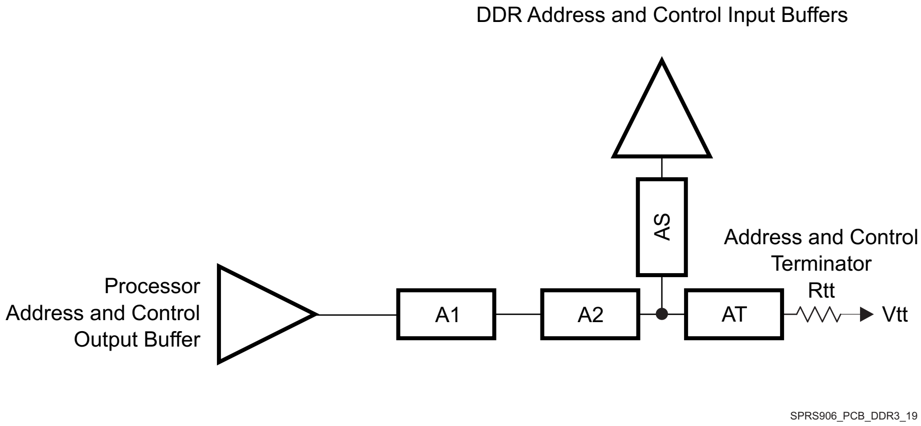


Figure 7-75. ADDR_CTRL Topology for One DDR3 Device

7.7.3.15.3.2 CK and ADDR/CTRL Routing, One DDR3 Device

Figure 7-76 shows the CK routing for one DDR3 device placed on the same side of the PCB. Figure 7-77 shows the corresponding ADDR_CTRL routing.

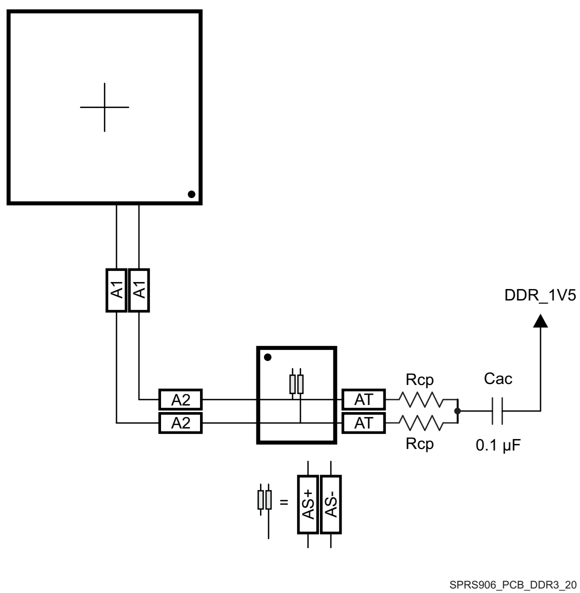


Figure 7-76. CK Routing for One DDR3 Device

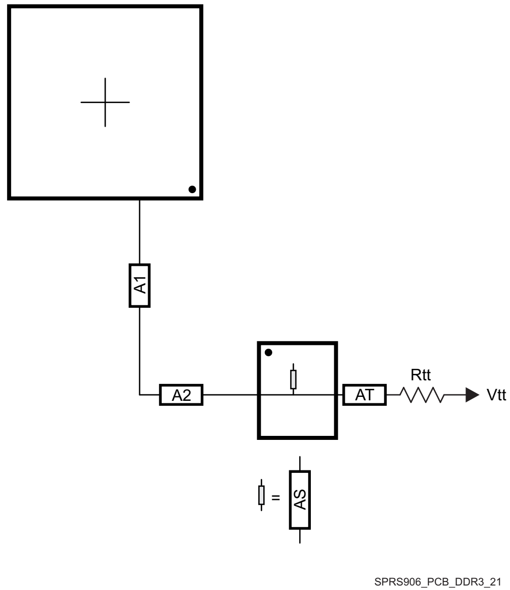


Figure 7-77. ADDR_CTRL Routing for One DDR3 Device

7.7.3.16 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

Care should be taken to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes if both reference planes are ground or vdds_ddr. Ensure there are nearby bypass capacitors to allow the return currents to transition between reference planes if one of the reference planes is ground. The goal is to minimize the size of the return current loops.

7.7.3.16.1 DQS and DQ/DM Topologies, Any Number of Allowed DDR3 Devices

DQS lines are point-to-point differential, and DQ/DM lines are point-to-point singled ended. Figure 7-78 and Figure 7-79 show these topologies.

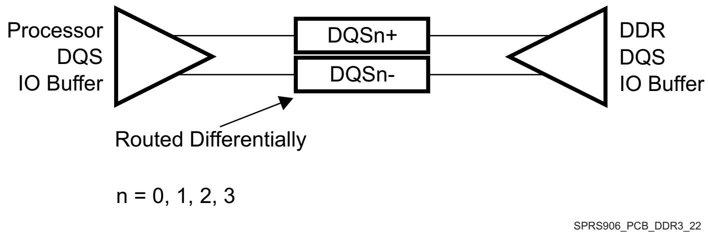


Figure 7-78. DQS Topology

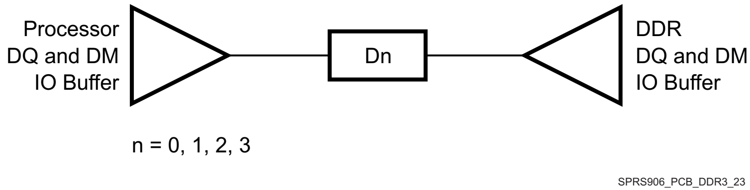


Figure 7-79. DQ/DM Topology

7.7.3.16.2 DQS and DQ/DM Routing, Any Number of Allowed DDR3 Devices

Figure 7-80 and Figure 7-81 show the DQS and DQ/DM routing.

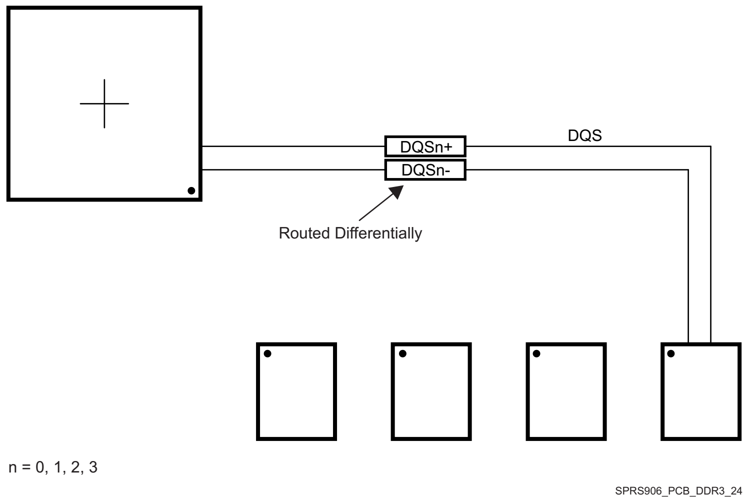


Figure 7-80. DQS Routing With Any Number of Allowed DDR3 Devices

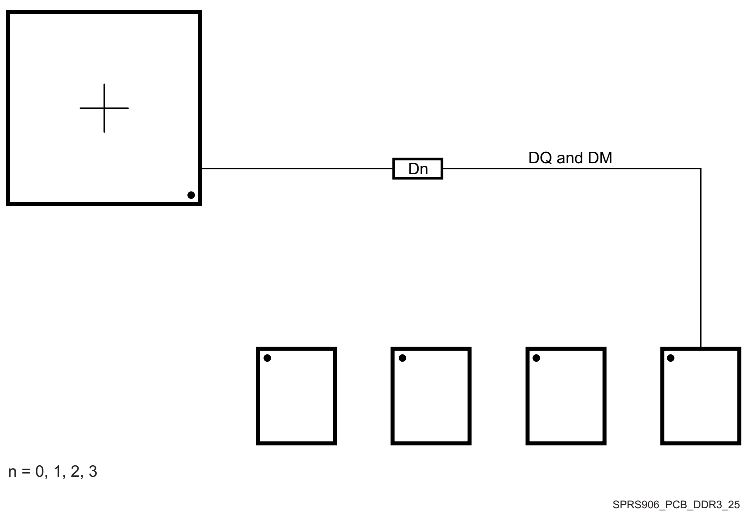


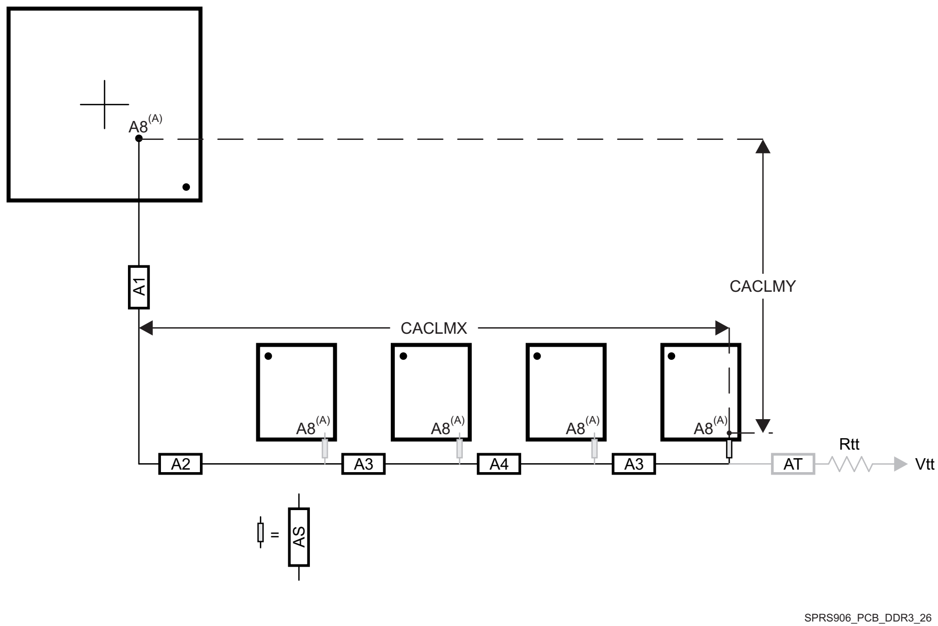
Figure 7-81. DQ/DM Routing With Any Number of Allowed DDR3 Devices

7.7.3.17 Routing Specification

7.7.3.17.1 CK and ADDR_CTRL Routing Specification

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 7-82 and Figure 7-83 show this distance for four loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK/ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 7-50.

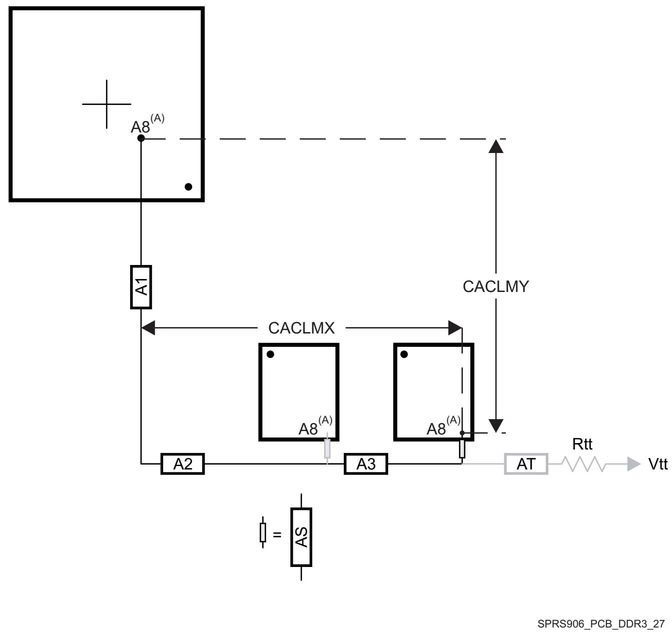


A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 7-82. CACLM for Four Address Loads on One Side of PCB



A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 7-83. CACLM for Two Address Loads on One Side of PCB

Table 7-50. CK and ADDR_CTRL Routing Specification(2)(3)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
CARS31	A1+A2 length			500(1)	ps
CARS32	A1+A2 skew			29	ps
CARS33	A3 length			125	ps
CARS34	A3 skew(4)			6	ps
CARS35	A3 skew(5)			6	ps
CARS36	A4 length			125	ps
CARS37	A4 skew			6	ps
CARS38	AS length		5	17(1)	ps
CARS39	AS skew		1.3	14(1)	ps
CARS310	AS+/AS- length		5	12	ps
CARS311	AS+/AS- skew			1	ps
CARS312	AT length(6)		75		ps
CARS313	AT skew(7)		14		ps
CARS314	AT skew(8)			1	ps
CARS315	CK/ADDR_CTRL trace length			1020	ps
CARS316	Vias per trace			3(1)	vias
CARS317	Via count difference			1(15)	vias
CARS318	Center-to-center CK to other DDR3 trace spacing(9)	4w			
CARS319	Center-to-center ADDR_CTRL to other DDR3 trace spacing(9)(10)	4w			
CARS320	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(9)	3w			

Table 7-50. CK and ADDR_CTRL Routing Specification[(2)(3)] (continued)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
CARS321	CK center-to-center spacing[(11)(12)]				
CARS322	CK spacing to other net[(9)]	4w			
CARS323	Rcp[(13)]	Zo-1	Zo	Zo+1	Ω
CARS324	Rtt[(13)(14)]	Zo-5	Zo	Zo+5	Ω

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.

(2) The use of vias should be minimized.

(3) Additional bypass capacitors are required when using the DDR_1V5 plane as the reference plane to allow the return current to jump between the DDR_1V5 plane and the ground plane when the net class switches layers at a via.

(4) Non-mirrored configuration (all DDR3 memories on same side of PCB).

(5) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).

(6) While this length can be increased for convenience, its length should be minimized.

(7) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.

(8) CK net class only.

(9) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.

(10) The ADDR_CTRL net class of the other DDR EMIF is considered *other DDR3 trace spacing*.

(11) CK spacing set to ensure proper differential impedance.

(12) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.

(13) Source termination (series resistor at driver) is specifically not allowed.

(14) Termination values should be uniform across the net class.

(15) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure all segment skew maximums are not exceeded.

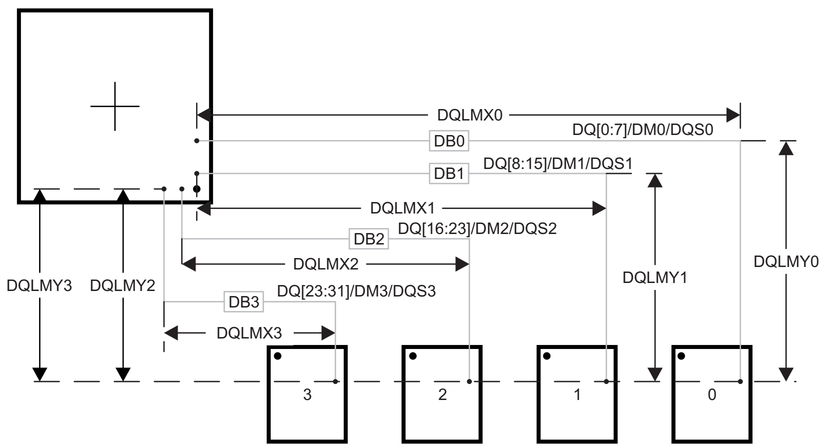
7.7.3.17.2 DQS and DQ Routing Specification

Skew within the DQS and DQ/DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are four DQLMs, DQLM0-DQLM3. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

NOTE

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

Given the DQS and DQ/DM pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 7-84 shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS and DQ/DM routing, these specifications are contained in Table 7-51.



DB0 - DB3 represent data bytes 0 - 3.

SPRS906_PCB_DDR3_28

There are four DQLMs, one for each byte (32-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:
DQLM0 = DQLMX0 + DQLMY0
DQLM1 = DQLMX1 + DQLMY1
DQLM2 = DQLMX2 + DQLMY2
DQLM3 = DQLMX3 + DQLMY3

Figure 7-84. DQLM for Any Number of Allowed DDR3 Devices

Table 7-51. Data Routing Specification(2)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
DRS31	DB0 length			340	ps
DRS32	DB1 length			340	ps
DRS33	DB2 length			340	ps
DRS34	DB3 length			340	ps
DRS35	DBn skew(3)			5	ps
DRS36	DQSn+ to DQSn- skew			1	ps
DRS37	DQSn to DBn skew(3)(4)			5(10)	ps
DRS38	Vias per trace			2(1)	vias
DRS39	Via count difference			0(10)	vias
DRS310	Center-to-center DBn to other DDR3 trace spacing(6)	4			w(5)
DRS311	Center-to-center DBn to other DBn trace spacing(7)	3			w(5)
DRS312	DQSn center-to-center spacing(8)(9)				
DRS313	DQSn center-to-center spacing to other net	4			w(5)

(1) Max value is based upon conservative signal integrity approach. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) External termination disallowed. Data termination should use built-in ODT functionality.
(3) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.
(4) Each DQS pair is length matched to its associated byte.
(5) Center-to-center spacing is allowed to fall to minimum 2w for up to 1250 mils of routed length.
(6) Other DDR3 trace spacing means other DDR3 net classes not within the byte.
(7) This applies to spacing within the net classes of a byte.
(8) DQS pair spacing is set to ensure proper differential impedance.
(9) The most important thing to do is control the impedance so inadvertent impedance mismatches are not created. Generally speaking, center-to-center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the singleended impedance, Zo.
(10) Via count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through vias – has been applied to ensure DBn skew and DQSn to DBn skew maximums are not exceeded.

8 Device and Documentation Support

TI offers an extensive line of development tools, including methods to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules as listed below.

8.1 Device Nomenclature and Orderable Information

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, TDA2Px). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of TDA2Px devices in the ABZ package type, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the Silicon Errata (literature number SPRZ397).

8.1.1 Standard Package Symbolization

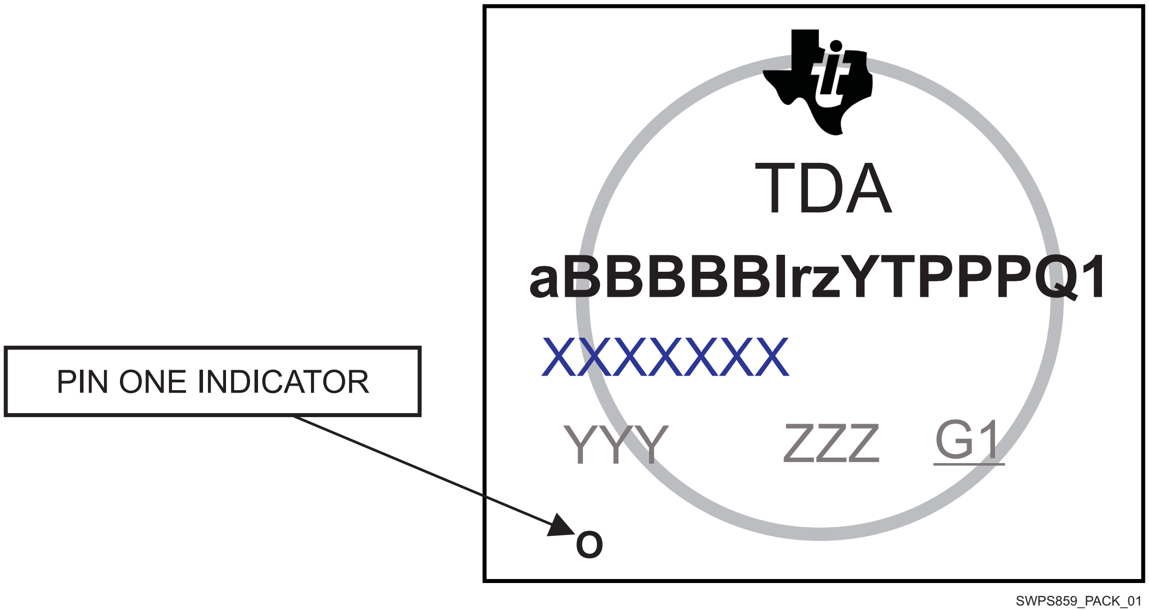


Figure 8-1. Printed Device Reference

NOTE

Some devices have a cosmetic circular marking visible on the top of the device package which results from the production test process. These markings are cosmetic only with no reliability impact.

8.1.2 Device Naming Convention

Table 8-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		MARKING	ORDERABLE	
a	Device evolution stage[(1)]	X	*Contact TI*	Prototype
		P		Preproduction (production test flow, no reliability data)
		BLANK		Production
BBBBB[(3)]	Base production part number	TDA2PS		ADAS 2nd Generation Super Tier
		TDA2PH		ADAS 2nd Generation High Tier
		TDA2PM		ADAS 2nd Generation Mid Tier
		TDA2PL		ADAS 2nd Generation Low Tier
I	Device Identity	A		Scene Analysis
		V		Scene Viewing
		E		Ethernet Decode
		R		Driver Recorder
		F		Fusion
		G		GFX enabled
		X		ADAS Superset
		D		DSP only
r	Device revision	BLANK		SR 1.0

Table 8-1. Nomenclature Description (continued)

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		MARKING	ORDERABLE	
z	Device Speed	A		Indicates the speed grade for each of the cores in the device. For more information see Section 3.1, *Device Comparison Table*.
		B		
		D		
		F		
		N		
		R		
		U		
		T		
Y	Device type	BLANK		General purpose (Prototype and Production)
		E		Emulation (E) devices
		S		High-Security device, Secure Boot Supported
		D		High security devices
T	Temperature(2)	I		Industrial: -40 °C to 85 °C (initial prototypes)
		Q		Full temp range: -40 °C to 125 °C
PPP	Package designator	ABZ		ABZ S-PBGA-N760 (23mm x 23mm) Package
c	Carrier designator	N/A	BLANK	Tray
		N/A	R	Tape & Reel
Q1	Automotive Designator	BLANK		Does not meets automotive qualification
		Q1		Meets Q100 equal requirements, with exceptions as specified in DM.
XXXXXXX		*As marked*	*N/A*	Lot Trace Code
YYY		*As marked*	*N/A*	Production Code, For TI use only
ZZZ		*As marked*	*N/A*	Production Code, For TI use only
O		*As marked*	*N/A*	Pin one designator
G1		*As marked*	*N/A*	ECAT—Green package designator

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) Applies to device max junction temperature.

(3) X577Px is the base part number for the superset device. Software should constrain the features used to match the intended production device.

NOTE

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

8.2 Tools and Software

The following products support development for TDA2x platforms:

TDA2Px Pad Configuration Tool is an interactive pad-configuration tool that allows the user to visualize the device pad configuration state on power-on reset and then customize the configuration of the pads for the specific use-case and identify the device register settings associated to that configuration.

TDA2Px Register Descriptor is an interactive device register configuration tool that allows users to visualize the register state on power-on reset, and then customize the configuration of the device for the specific use-case.

TDA2Px Clock Tree Tool is interactive clock tree configuration software that allows the user to visualize the device clock tree, interact with clock tree elements and view the effect on PRCM registers, interact with the PRCM registers and view the effect on the device clock tree, and view a trace of all the device registers affected by the user interaction with the clock tree.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.3 Documentation Support

The following documents describe the TDA2Px devices.

TRM SPRUIF0 TDA2Px SoC for Advanced Driver Assistance Systems (ADAS) Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the TDA2x family of devices.

Errata **TDA2Px Silicon Errata** Describes known advisories on silicon and provides workarounds.

8.3.1 FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

8.3.2 Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

8.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates — including silicon errata — go to the product folder for your device on www.ti.com. In the upper right-hand corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

8.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.6 Trademarks

ICEPick is a trademark of Texas Instruments.
Neon, CoreSight are trademarks of Arm Limited.
Arm, Cortex are registered trademarks of Arm Limited.
HDMI is a trademark of HDMI Licensing, LLC.
PowerVR is a registered trademark of Imagination Technologies Ltd.
JTAG is a registered trademark of JTAG Technologies, Inc.
MMC is a trademark of MultiMediaCard Association.
PCI Express is a registered trademark of PCI-SIG.
SD is a registered trademark of Toshiba Corporation.
Vivante is a registered trademark of Vivante Corporation.
All other trademarks are the property of their respective owners.

8.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical Packaging Information

The following pages include mechanical packaging information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Mechanical Data

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TDA2PSXTQABZQ1	ACTIVE	FCCSP	ABZ	760	60	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 125	TDA2PSXTQABZQ1 941 941 ABZ	Samples
TDA2PSXTQABZRQ1	ACTIVE	FCCSP	ABZ	760	400	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 125	TDA2PSXTQABZQ1 941 941 ABZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

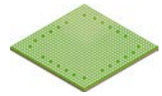
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

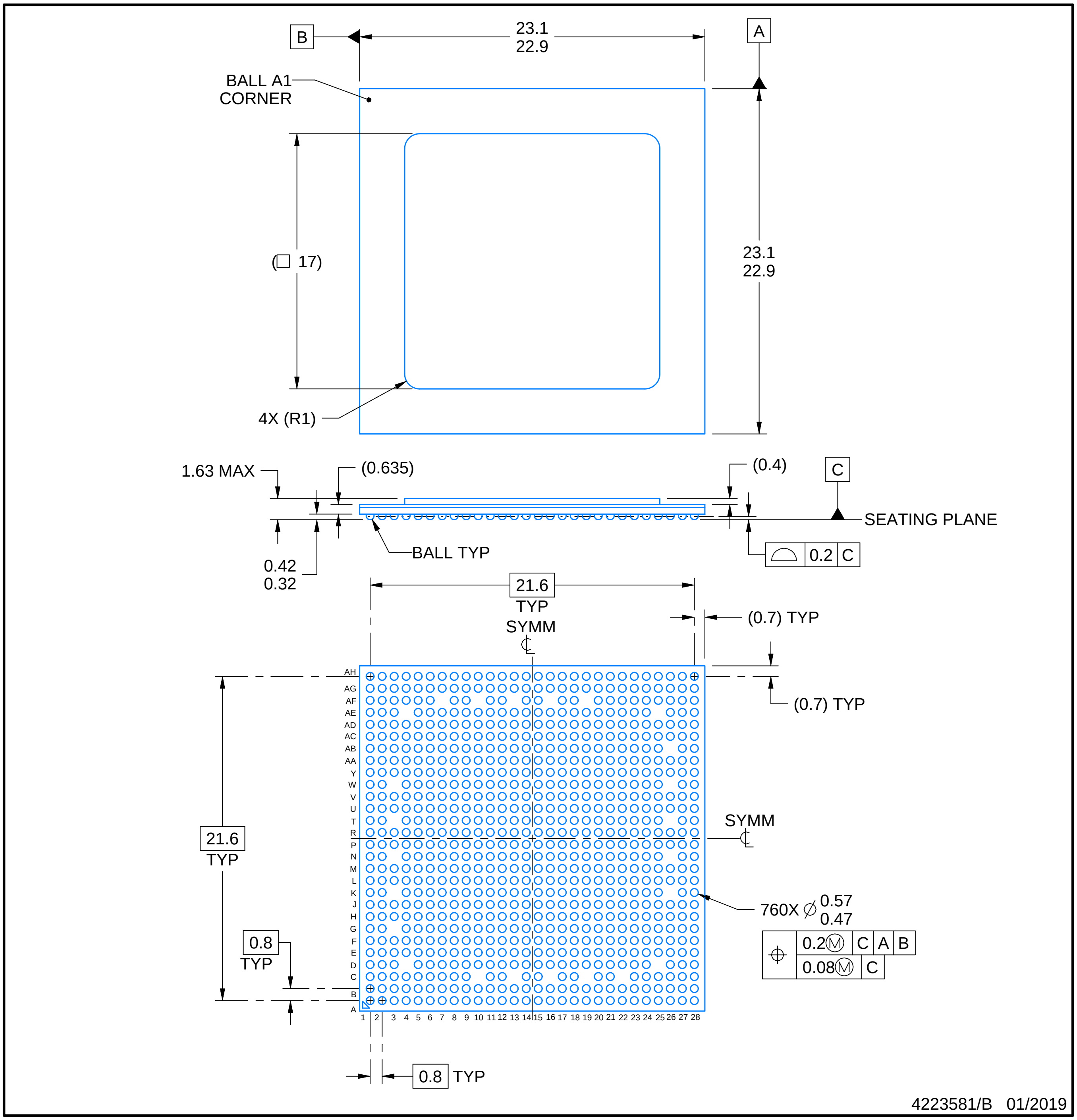


PACKAGE OUTLINE

ABZ0760A

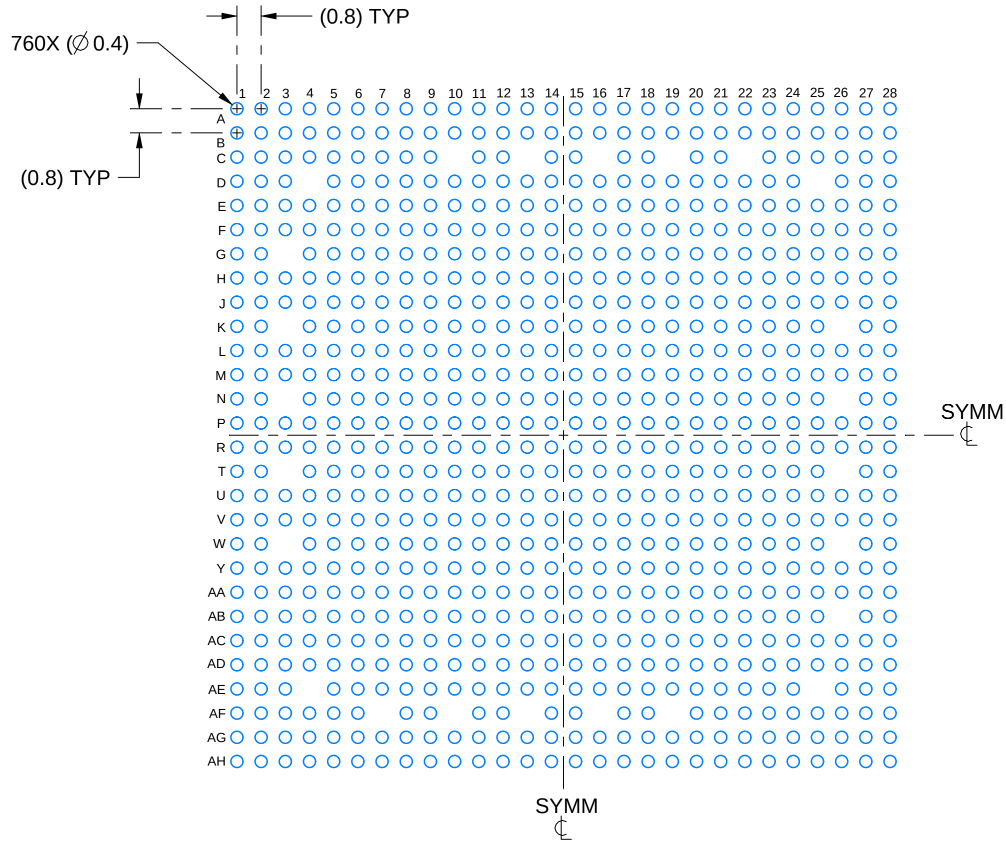
FCBGA - 1.63 mm max height

BALL GRID ARRAY

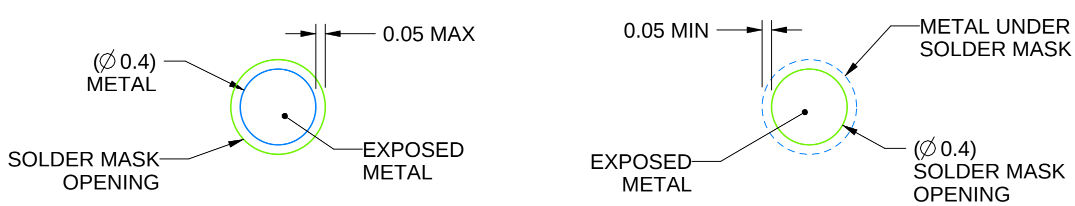


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 4X



NON-SOLDER MASK
DEFINED
(PREFERRED)

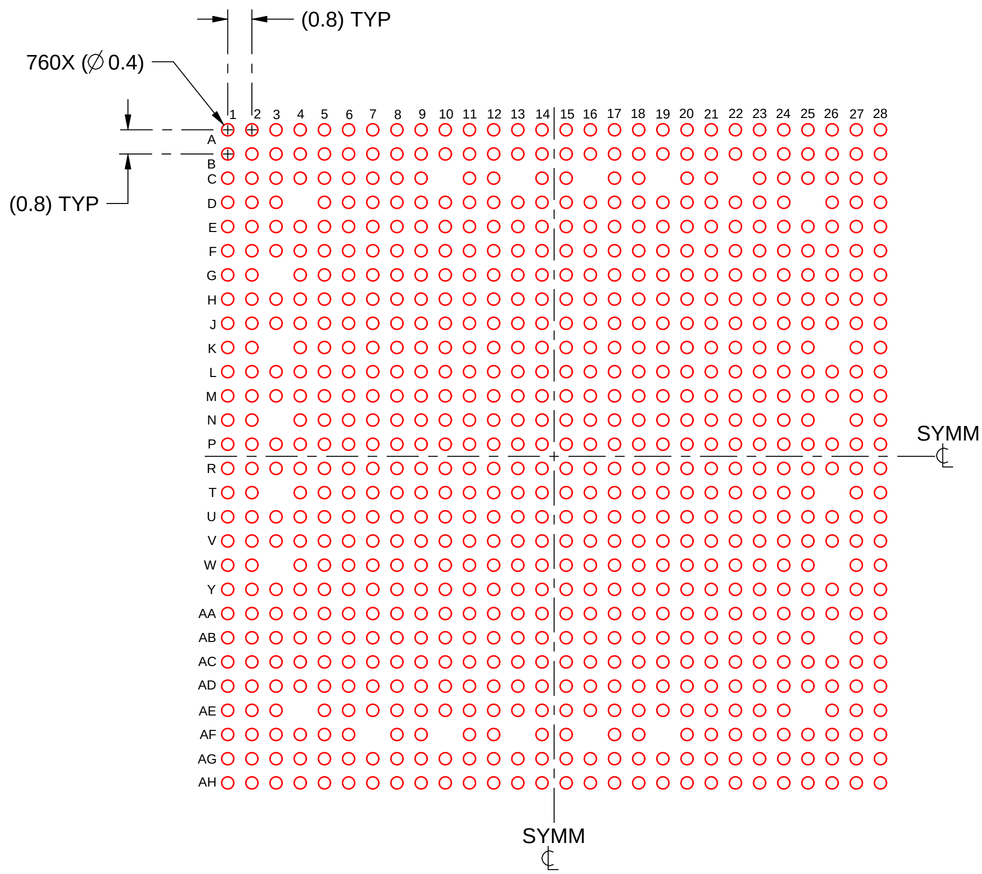
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223581/B 01/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 4X

4223581/B 01/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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