TLV3511 7ns High-Speed Comparator with Rail-to-Rail Input

1 Features

- Propagation delay: 6ns
- High toggle frequency: 180MHz
- Wide supply range: 2.7V to 5.5V
- Input offset voltage: +/- 1mV typ.
- Low supply current: 1.1mA per channel
- Input voltage range extends 300mV beyond either rail
- Internal hysteresis: 2.3mV
- Power-on-reset provides a known startup condition
- Push-pull output
- Temperature range: -40°C to +125°C

2 Applications

- Motor Drive Diagnostics & Monitoring
- Servo Drive Control Module
- Servo drive position sensor
- Medical & Healthcare
- Field Transmitters & Sensors

3 Description

The TLV351x is a family of 5V single and dual channel comparators with push-pull outputs. The family has an excellent speed-to-power combination with a propagation delay of 7ns and a full supply voltage range of 2.7V to 5.5V with a quiescent supply current of only 1mA per channel.

All devices include a Power-On Reset (POR) feature. This makes sure the output is in a known state (output LOW) until the minimum supply voltage has been reached before the output responds to the inputs, thus preventing false outputs during system power-up and power-down.

Likewise, the TLV351x are conveniently available in standard leaded and leadless packages with features such as rail-to-rail inputs, low offset voltage, and large output drive current. These features along with fast response time make the comparators well-suited for current sensing, zero-cross detection, and a variety of other applications where precision and speed is critical.

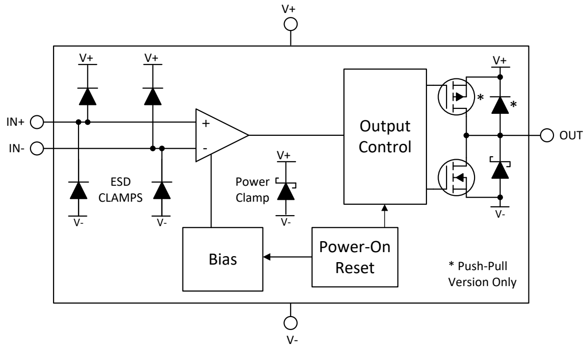
All devices are specified for operation across the expanded temperature range of –40°C to 125°C.

Device Information

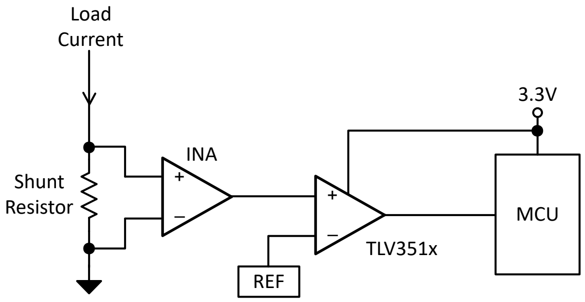
PART NUMBER	PACKAGE [1]	BODY SIZE (NOM) [2]
TLV3511	SC-70 (5)	1.25mm × 2.00mm
	SOT-23 (5) (Preview)	1.60mm × 2.90mm
	SOT (5) (Preview)	1.2mm × 1.5mm
TLV3512	VSSOP (8) (Preview)	3.00mm × 3.00mm
	WSON (8) (Preview)	2.00mm × 2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram



Low-Side Current Sensing

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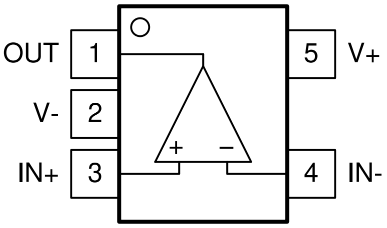
4 Pin Configuration and Functions

Pin Configurations: TLV3511 and TLV3512



DCK, DBV, DRL Packages
SC70, SOT-23-5, SOT
Top View
(Standard "north west" pinout)

Table 4-1. Pin Functions: TLV3511

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output
V-	2	-	Negative supply voltage
IN+	3	I	Non-inverting (+) input
IN-	4	I	Inverting (-) input
V+	5	-	Positive supply voltage

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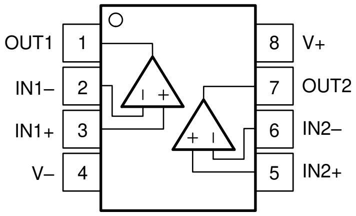

Figure 4-1. DGK Package
8-Pin VSSOP
Top View

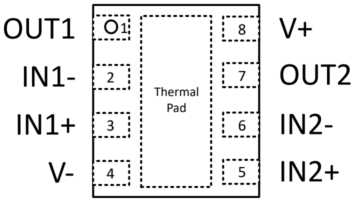

Figure 4-2. DSG Package
8-Pin WSON
Top View

Pin Functions: TLV3512

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2–	3	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	7	O	Output, channel 1
OUT2	6	O	Output, channel 2
V-	5	-	Negative (lowest) supply or ground
V+	8	-	Positive (highest) supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage V_S = (V+) - (V-)		6	V
Differential input voltage, VID	-6	6	V
Input pins (IN+, IN–) from (V-) [2]	– 0.5	(V+) + 0.5	V
Current into input pins (IN+, IN-)	-10	10	mA
Output (OUT) from (V-)	– 0.5	(V+) + 0.5	V
Output short-circuit current	-100	100	mA
Output short-circuit duration		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to (V–) and (V+). Input signals that can swing more than 0.5V beyond the supply rails must be current-limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage V_S = (V+) - (V-)	2.7	5.5	V
Input voltage range	(V-) - 0.3	(V+) + 0.3	V
Ambient temperature, T_A	–40	125	°C

5.4 Thermal Information

THERMAL METRIC [1]		TLV3511 DBV (SOT-23)	TLV3511 DCK (SC70)	UNIT
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	198.1	220.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.6	136.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.7	65.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.1	34.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.3	65.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

V_S = 2.7V to 5V, $V_{CM} = V_S / 2$; at T_A = 25°C (unless otherwise noted).
Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input Offset Voltage	V_S = 5V, $V_{CM} = V_S / 2$		±1	±5	mV
V_{IO}	Input Offset Voltage	V_S = 5V, $V_{CM} = V_S / 2$, T_A = -40 to 125℃			±6	mV
V_{HYS}	Hysteresis	V_S = 5V, $V_{CM} = V_S / 2$		2.3		mV
V_{HYS}	Hysteresis	V_S = 5V, $V_{CM} = V_S / 2$, T_A = -40 to 125℃			3.5	mV
V_{CM}	Common-mode voltage range		(V-) - 0.2		(V+) + 0.2	V
I_B	Input bias current	V_S = 5V, $V_{CM} = V_S / 2$, T_A = -40 to 125℃			1.5	nA
I_{OS}	Input offset current	V_S = 5V, $V_{CM} = V_S / 2$			10	pA
C_{IN}	Input capacitance			4		pF
CMRR	Common-mode rejection ratio	$V_{CM} = V_{EE}$ - 0.2V to V_{CC} + 0.2V		80		dB
DC Output Characteristics						
V_{OH}	Voltage swing from (V+)	V_S = 5V, I_{Source} = 4mA		120	225	mV
V_{OH}	Voltage swing from (V+)	V_S = 5V, I_{Source} = 4mA, -40 to 125C			250	mV
V_{OL}	Voltage swing from (V-)	V_S = 5V, I_{Sink} = 4mA		140	225	mV
V_{OL}	Voltage swing from (V-)	V_S = 5V, I_{Sink} = 4mA, -40 to 125C			250	mV
I_{SC}	Short-circuit current	V_S = 5V, sourcing		75		mA
		V_S = 5V, sinking		85		
Power Supply						
I_Q	Supply current / Channel	V_S = 2.7V and 5V, no load, output low, T_A = -40 to 125℃		1.1	2	mA
$V_{POR\ (postive)}$	Power-On Reset Voltage			2.2		V
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 5.5V, T_A = -40 to 125℃		93		dB

5.6 Switching Characteristics

For V_S = 2.7V to V_S = 5V, $V_{CM} = V_S / 2$; C_L = 15pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low	Midpoint of input to midpoint of output, V_{OD} = 10mV		10		ns
t_{PHL}	Propagation delay time, high to-low	Midpoint of input to midpoint of output, V_{OD} = 50mV		6	7	ns
t_{PLH}	Propagation delay time, low-to high	Midpoint of input to midpoint of output, V_{OD} = 10mV		10		ns
t_{PLH}	Propagation delay time, low-to high	Midpoint of input to midpoint of output, V_{OD} = 50mV		6	7	ns
t_{PD} Skew	Propagation delay skew	Measured as absolute value of the difference between t_{PDLH} and t_{PDHL}		300		ps
PWin	Minimum input pulse width	Voverdrive = Vunderdrive = 50mV PWout = 90% of PWin		3.5		ns
f_{TOGGLE}	Input toggle frequency	$V_{IN} = 200mV_{PP}$ Sine Wave, When output high reaches 90% of $V_{CC} - V_{EE}$ or output low reaches 10% of $V_{CC} - V_{EE}$		180		MHz
t_R	Rise time	Measured from 20% to 80%		1		ns
t_F	Fall time	Measured from 20% to 80%		1		ns
t_{ON}	Power-up time	During power on, (V+) must exceed 2.2V for 2.1µs before the output will reflect the input.		2.1		µs

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5.7 Typical Characteristics

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

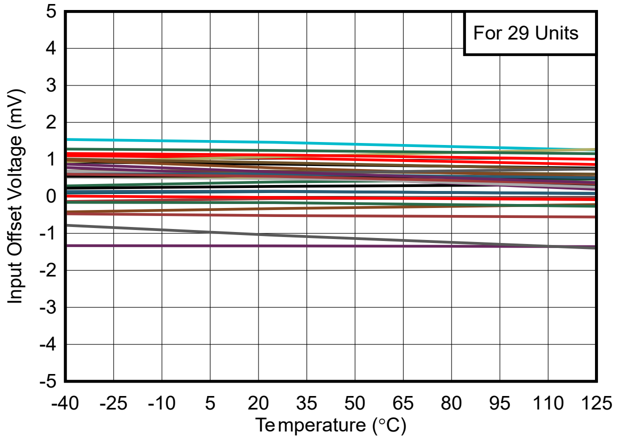

Figure 5-1. Offset vs. Temperature

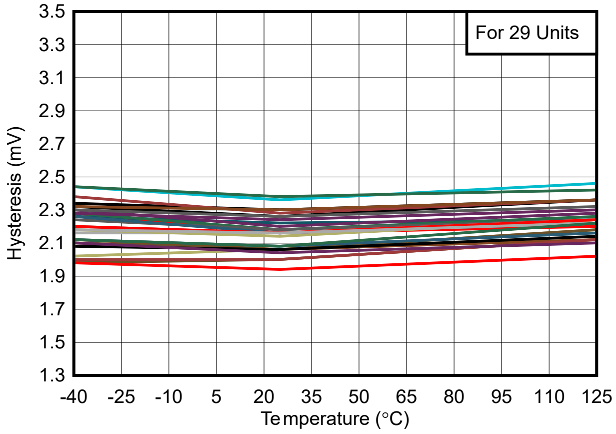

Figure 5-2. Hysteresis vs. Temperature

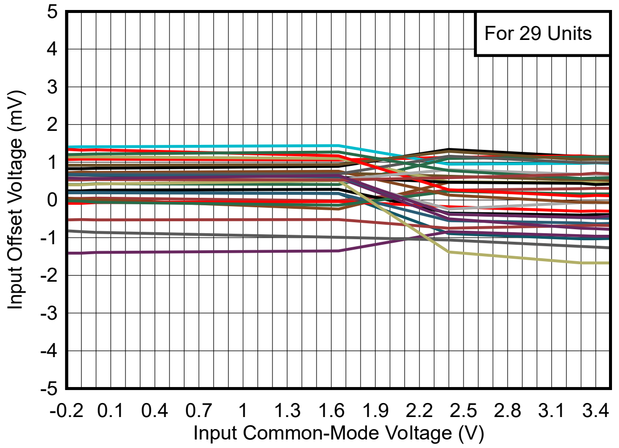

Figure 5-3. Offset vs. Common-Mode, 3.3V

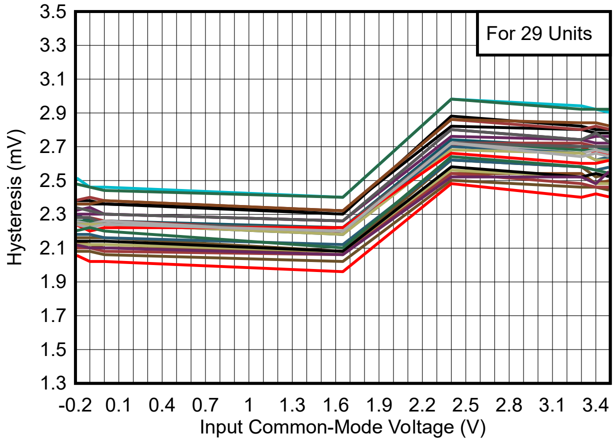

Figure 5-4. Hysteresis vs. Common-Mode, 3.3V

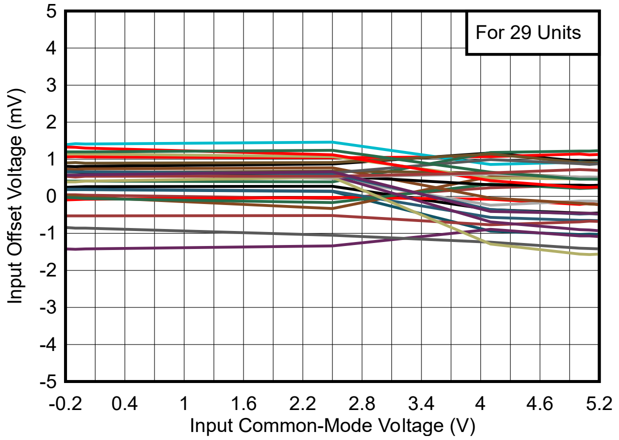

Figure 5-5. Offset vs. Common-Mode, 5V

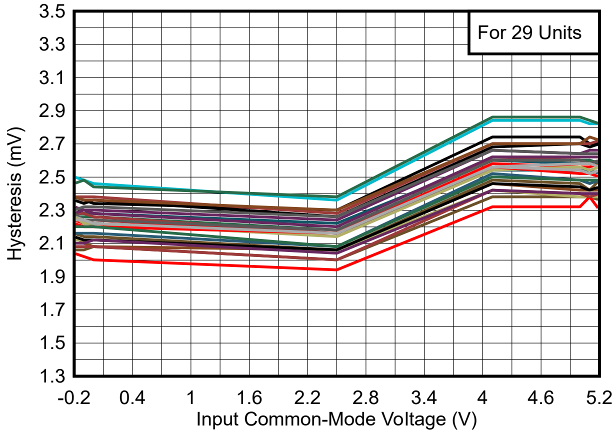

Figure 5-6. Hysteresis vs. Common-Mode, 5V

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5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

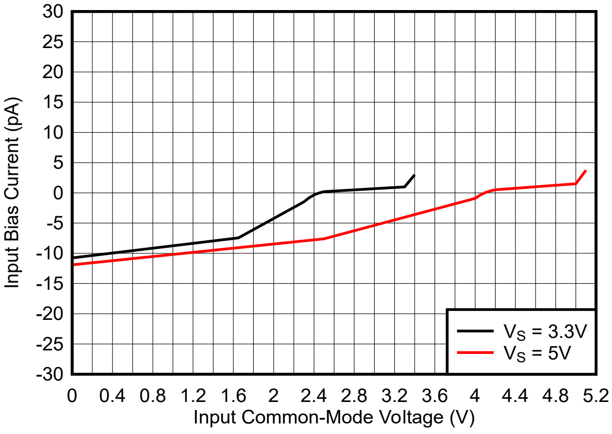

Figure 5-7. Bias Current vs. Common-Mode

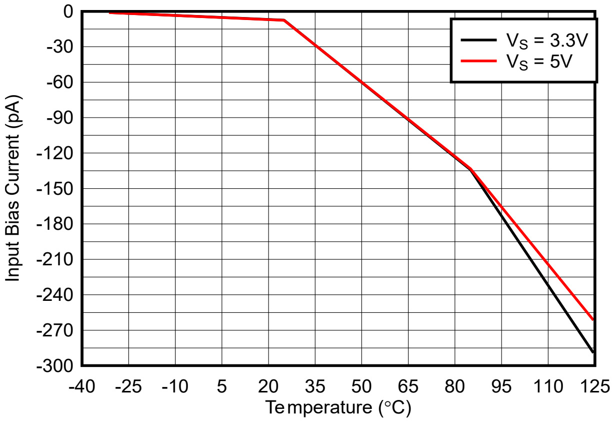

Figure 5-8. Bias Current vs. Temperature

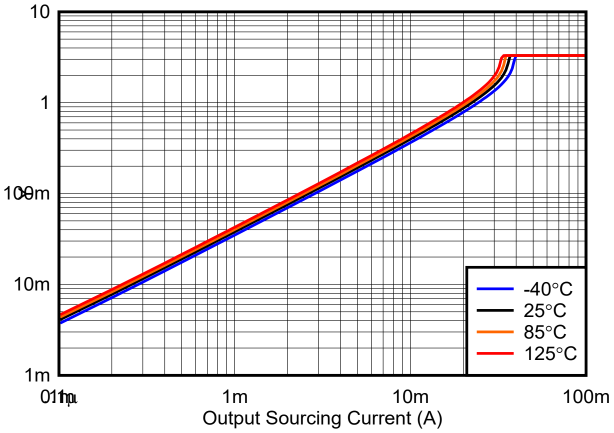

Figure 5-9. Output Voltage vs. Output Sourcing Current, 3.3V

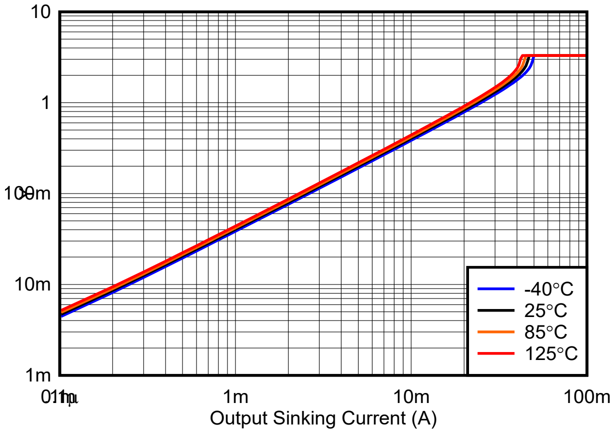

Figure 5-10. Output Voltage vs. Output Sinking Current, 3.3V

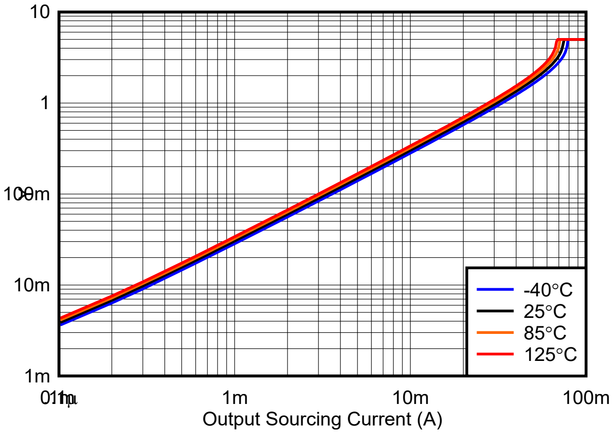

Figure 5-11. Output Voltage vs. Output Sourcing Current, 5V

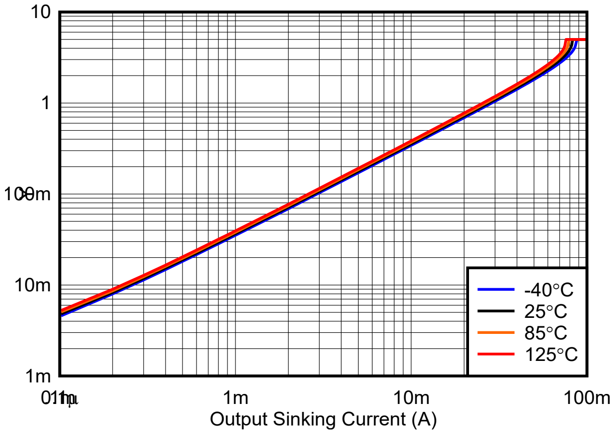

Figure 5-12. Output Voltage vs. Output Sinking Current, 5V

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5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

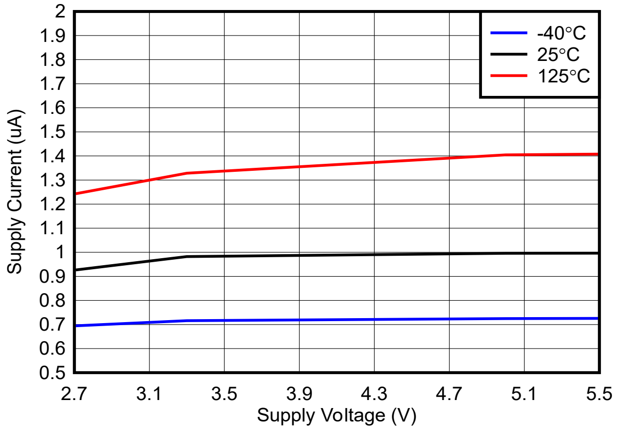

Figure 5-13. Supply Current vs. Supply Voltage (Output Low)

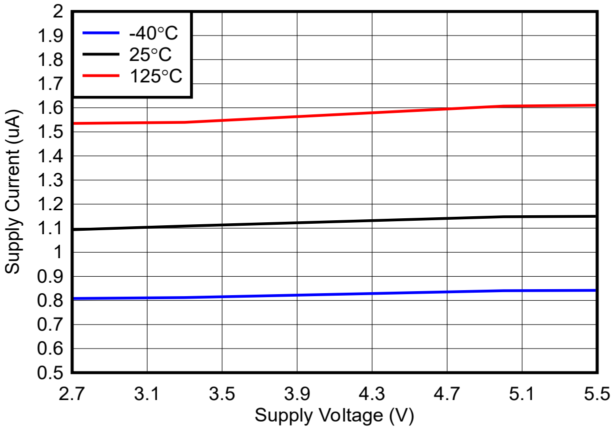

Figure 5-14. Supply Current vs. Supply Voltage (Output High)

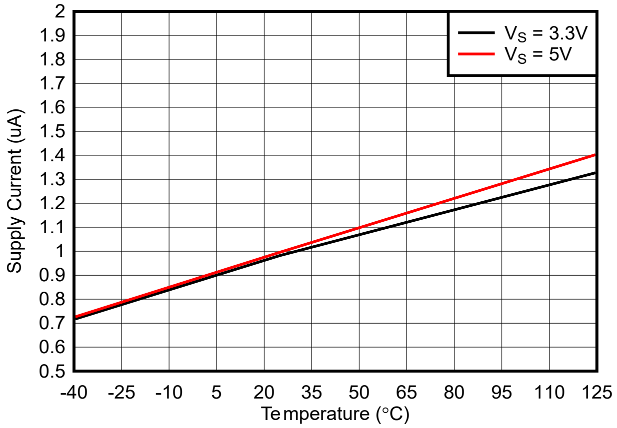

Figure 5-15. Supply Current vs. Temperature (Output Low)

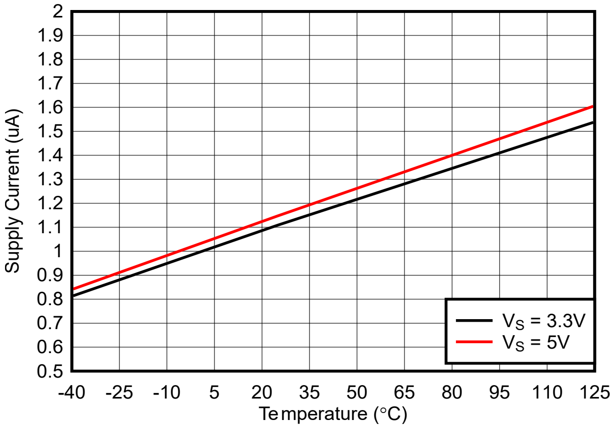

Figure 5-16. Supply Current vs. Temperature (Output High)

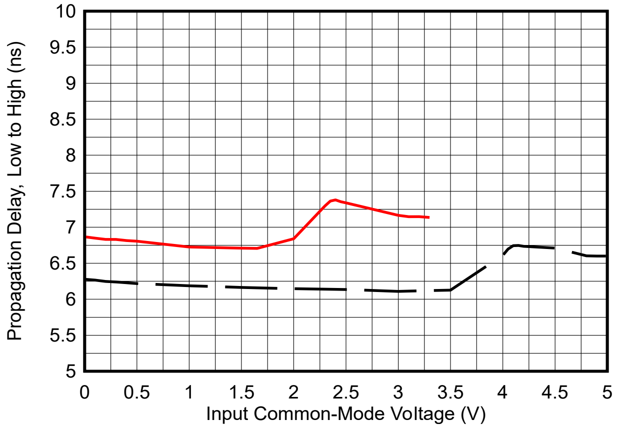

Figure 5-17. Propagation Delay (Low to High) vs. Common-Mode

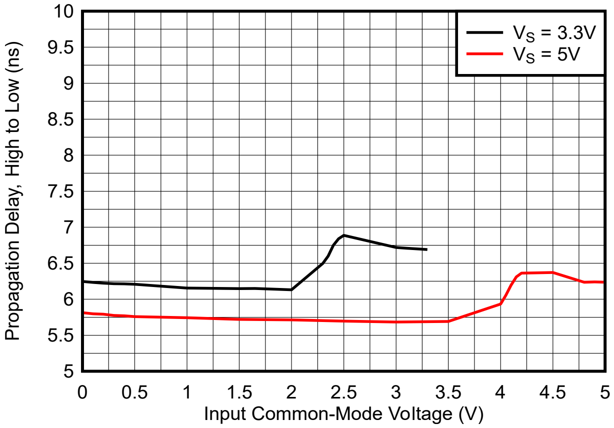

Figure 5-18. Propagation Delay (High to Low) vs. Common-Mode

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5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

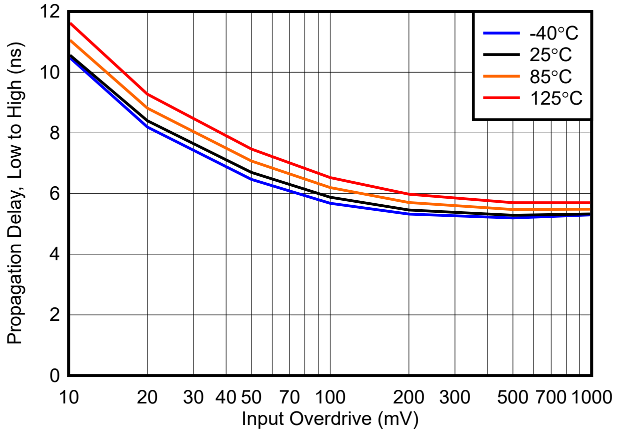

Figure 5-19. Propagation Delay (Low to High) vs. Overdrive (3.3V)

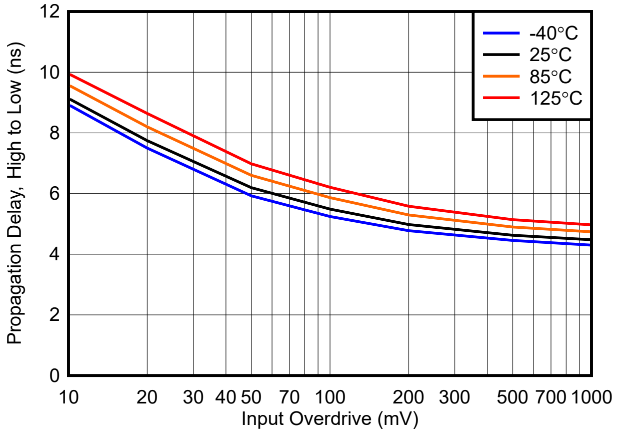

Figure 5-20. Propagation Delay (High to Low) vs. Overdrive (3.3V)

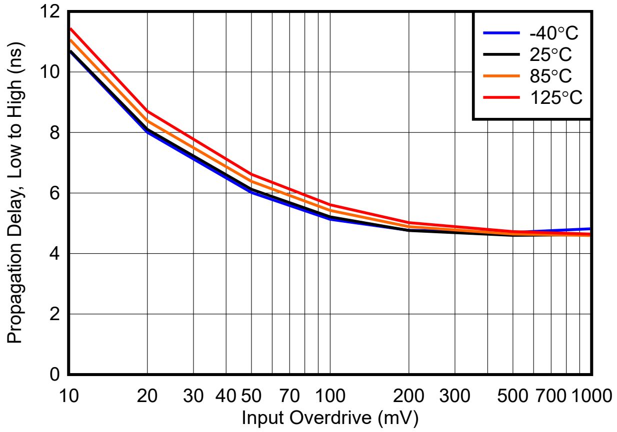

Figure 5-21. Propagation Delay (Low to High) vs. Overdrive (5V)

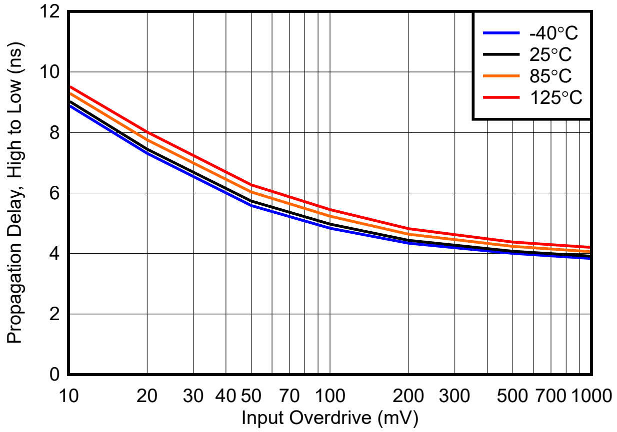

Figure 5-22. Propagation Delay (High to Low) vs. Overdrive (5V)

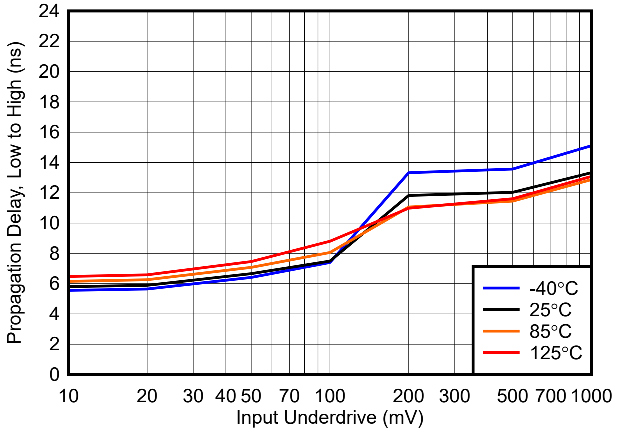

Figure 5-23. Propagation Delay (Low to High) vs. Underdrive (3.3V)

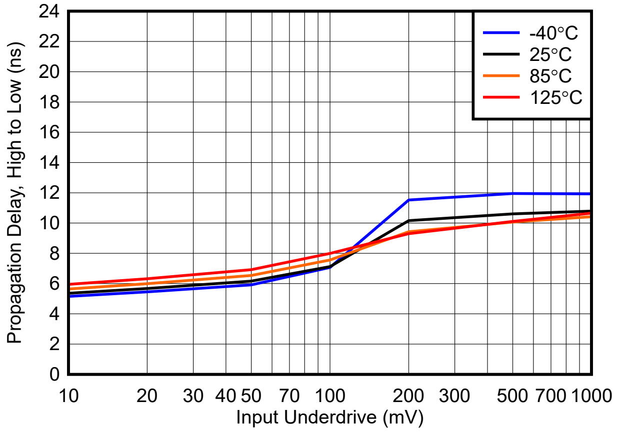

Figure 5-24. Propagation Delay (High to Low) vs. Underdrive (3.3V)

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5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

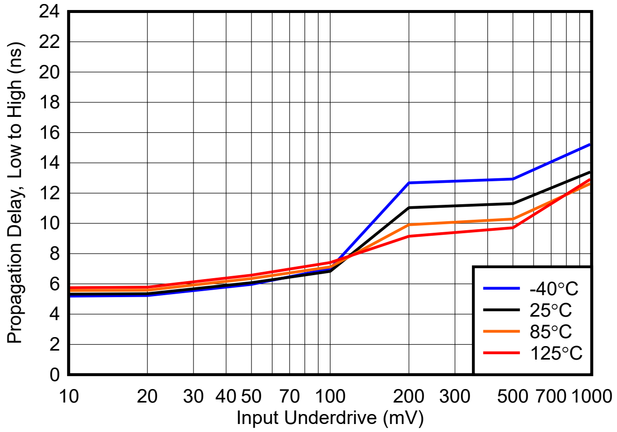

Figure 5-25. Propagation Delay (Low to High) vs. Underdrive (5V)

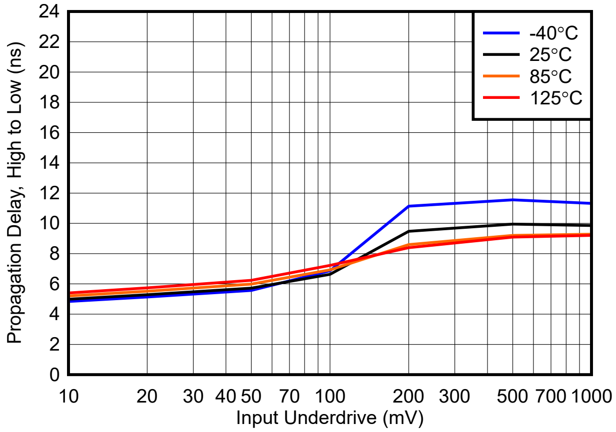

Figure 5-26. Propagation Delay (High to Low) vs. Underdrive (5V)

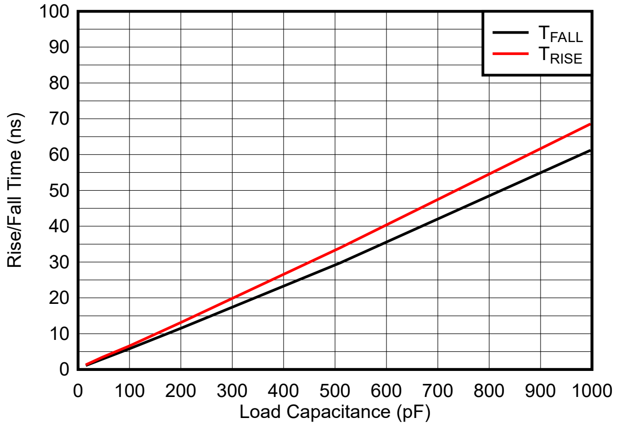

Figure 5-27. Rise and Fall Times vs. Capacitive Loads at 3.3V

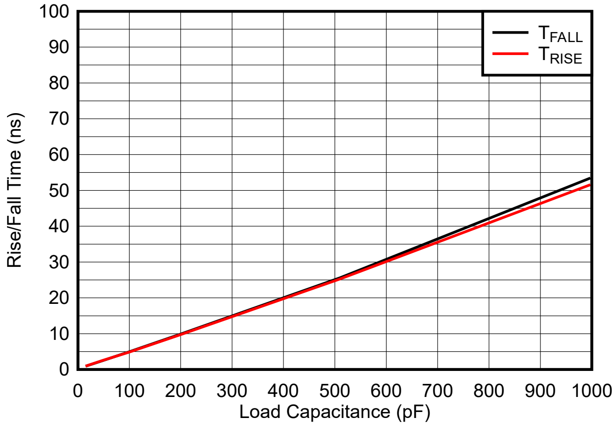

Figure 5-28. Rise and Fall Times vs. Capacitive Loads at 5V

6 Detailed Description

6.1 Overview

The TLV351x devices are high-speed comparators consuming 1mA per channel with 7ns of propagation delay. The TLV351x detects fast voltage and current transients while maintaining low power consumption with single-ended, push-pull outputs

6.2 Functional Block Diagrams

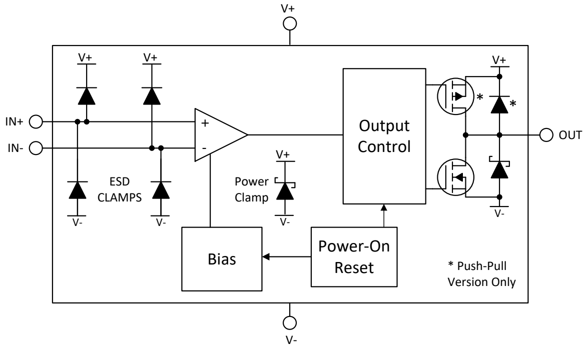

Figure 6-1. Block Diagram

6.3 Feature Description

The TLV351x comparators feature rail-to-rail inputs with integrated hysteresis, single-ended, push-pull outputs, and a Power-ON-Reset function.

6.4 Device Functional Modes

6.4.1 Inputs

The inputs incorporate internal ESD protection circuits to (V+) and (V-). Voltages on the inputs are limited to 0.3V beyond the rails.

When connecting to a low impedance source such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct. Limit the current to 10mA or less. One form of series resistance is any resistive input dividers or networks.

6.4.1.1 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs can be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+).

6.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown below. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

  (typically 2mV for the TLV351x family)

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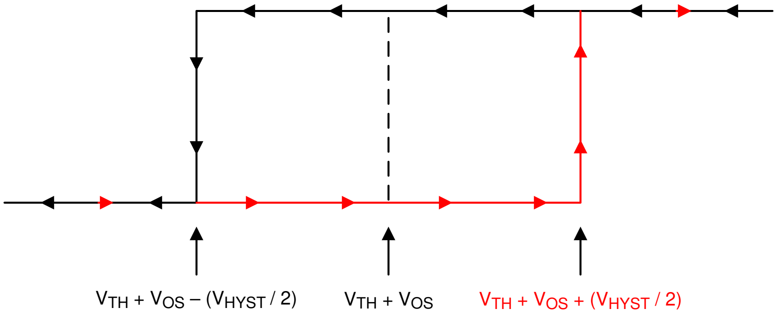

Figure 6-2. Hysteresis Transfer Curve

6.4.3 Outputs

The TLV351x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

6.4.4 ESD Protection

The inputs and outputs incorporate internal ESD protection circuits to (V+) and (V-).

Voltages on the inputs are limited to 0.3V beyond the rails. If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents in case the clamps conduct. Limit the current to 10mA or less.

6.4.5 Power-On Reset (POR)

The TLV351x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is active for up to 2.1us after the V_{POR} of 2.2V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV351x devices, the output is held low during the POR period (t_{on}) as shown below.

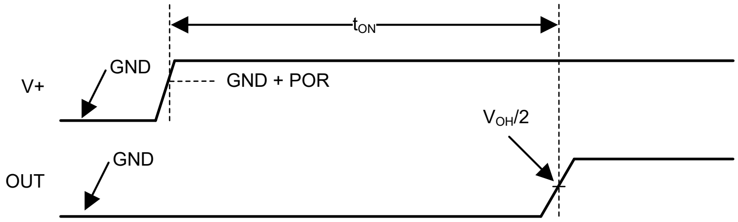

Figure 6-3. Power-On Reset Timing Diagram

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Likewise, the table below summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in the figure below and is measured from the mid-point of the input to the midpoint of the output.

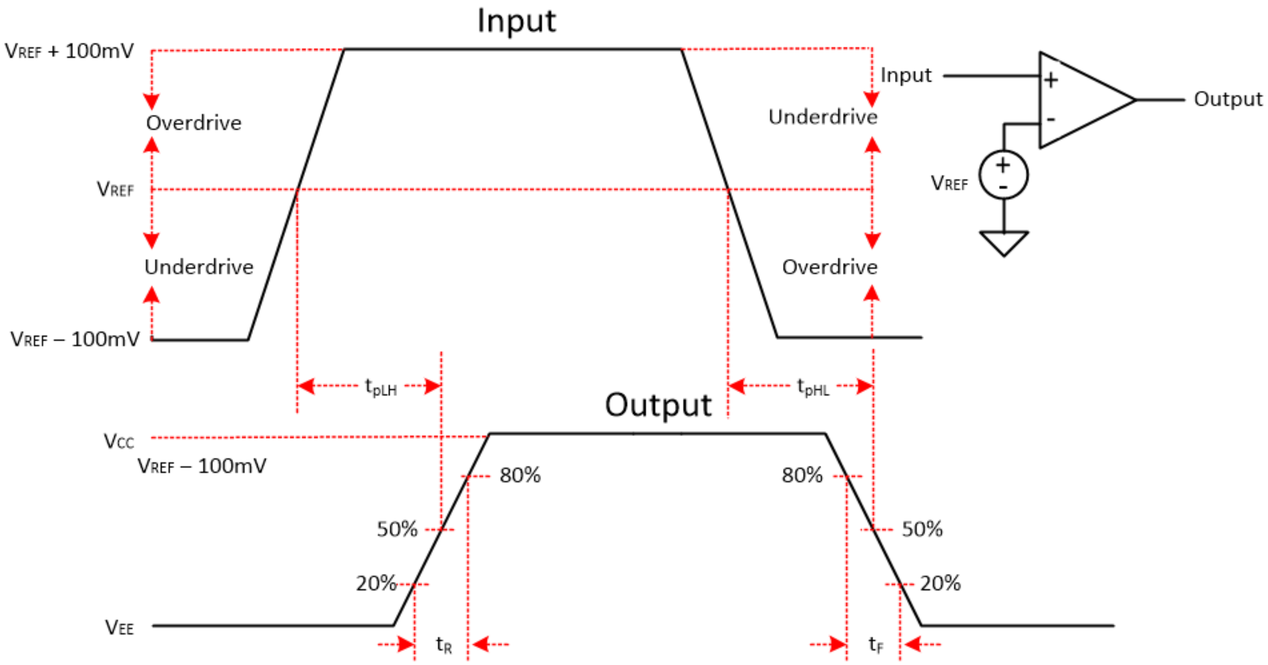

Figure 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the above example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration frequently produces a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV351x only have a minimal amount of internal hysteresis of 2mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on the current output state.

The hysteresis transfer curve is shown below. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

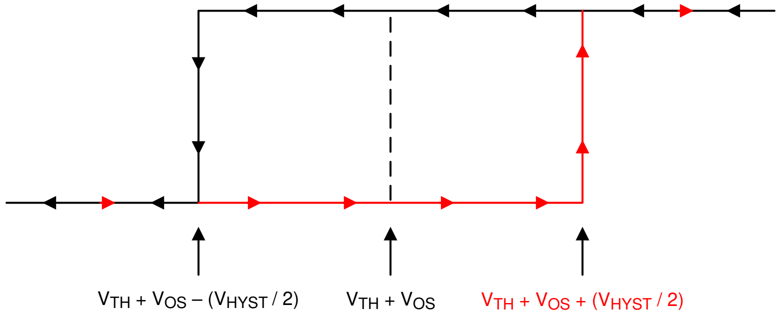

Figure 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown below.

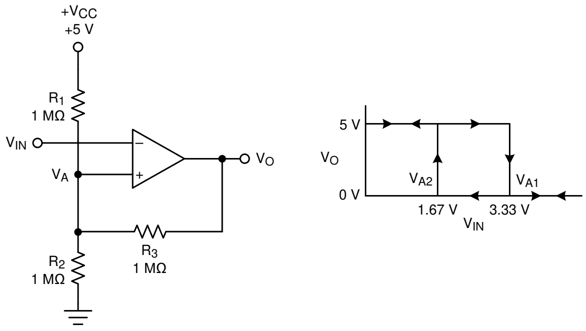

Figure 7-3. TLV351x in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown below.

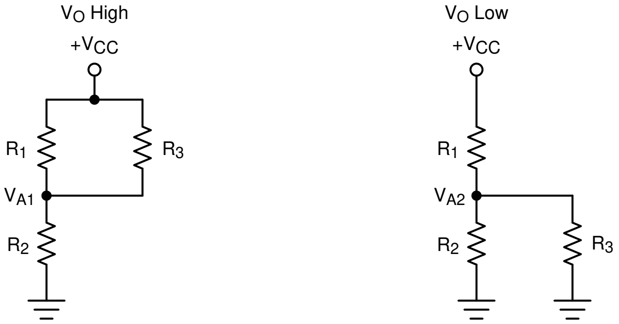

Figure 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown above on the left.

The equation below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown above on the right.

Use equation below to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

The equation below defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown below.

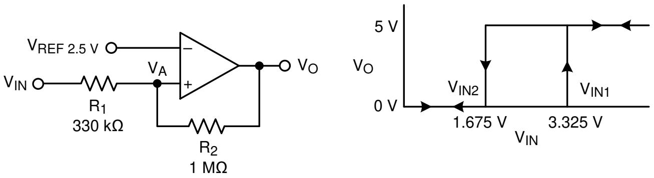

Figure 7-5. TLV351x in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown below.

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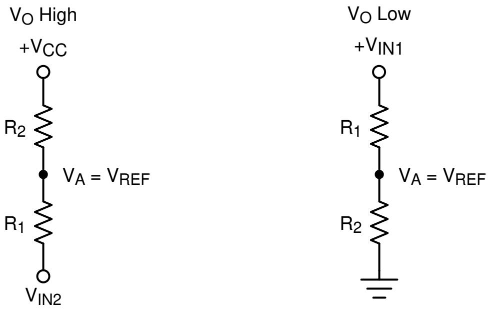

Figure 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use the equation below to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use equation below to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown below.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7.2 Typical Applications

7.2.1 Low-Side Current Sensing

The figure below shows a simple low-side current sensing circuit using a high-speed comparator. Since this design does not utilze an amplifier, the response time is only limited by the propagation delay of the comparator. With faster response time, the design is well-suited for short-circuit detection when speed is more important than accuracy. When the voltage across the shunt resistor reaches the critical over-current threshold created by R1 and R2, the comparator output changes state.

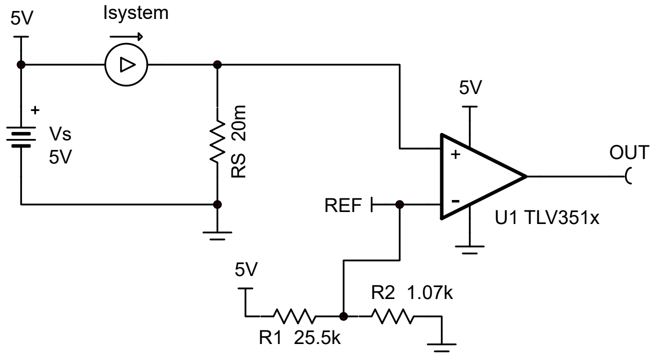

Figure 7-7. Current Sensing

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (overcurrent) event occurs when system current (Isystem) reaches 10A
- Alert signal (OUT) is active high
- Operate from a 5V power supply

7.2.1.2 Detailed Design Procedure

To minimize power dissipation and voltage drop across the shunt resistor (RS), a value of 20mΩ is selected. Since the overcurrent level of 10A creates a 200mV drop across RS, R1 and R2 are calculated to create the voltage divider value of 200mV from the regulated 5V supply voltage. If the system is expected to operate close to the 10A maximum, hysteresis can be added to the design as shown in Non-Inverting Comparator With Hysteresis.

7.2.1.3 Application Curve

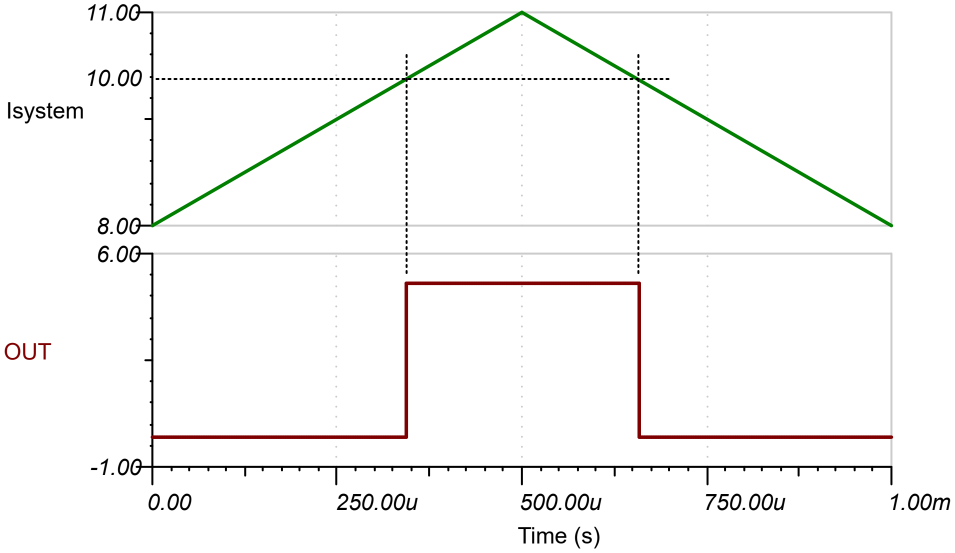

Figure 7-8. Current Sensing Results

7.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that limits the input voltage range and creates an inaccurate comparison or even oscillations.

The device is capable of being powered from both "split" supplies ((V+) &(V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output now swings "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications it is important to maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and need to be treated as high speed logic devices. Place the bypass capacitor as close to the supply pin as possible and connect to a solid ground plane, directly between the (V+) and GND pins.

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Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a (V+) or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor added in series with the output dampens any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, use controlled impedance traces with back-terminations when routing long distances.

7.4.2 Layout Example

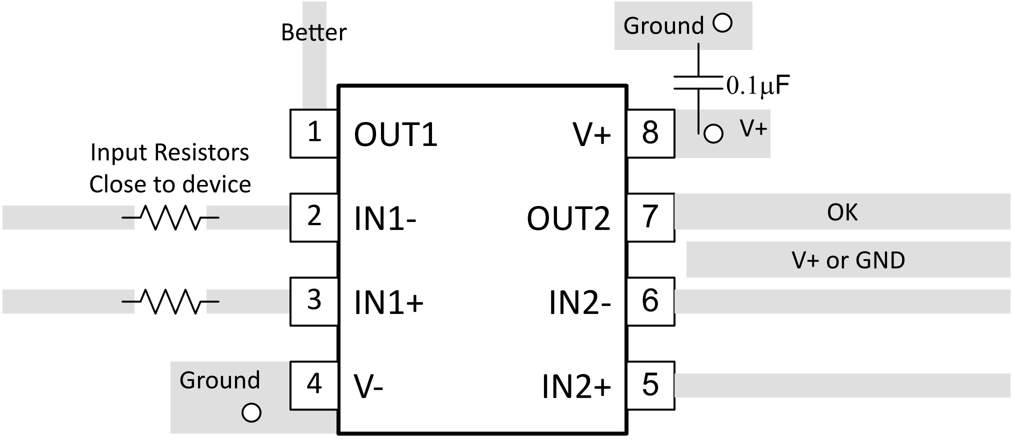

Figure 7-9. Dual Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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