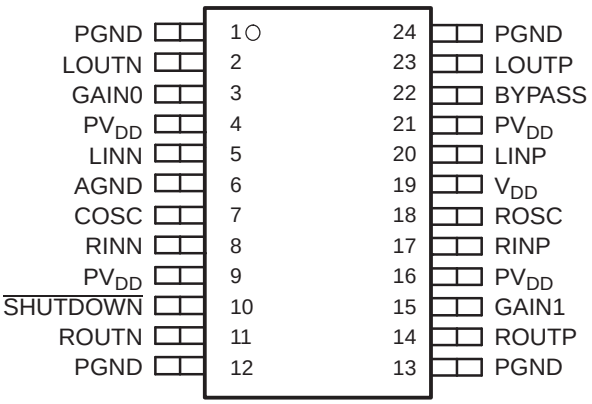
2-W FILTERLESS STEREO CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- **Modulation Scheme Optimized to Operate Without a Filter**
- **2 W Into 3-Ω Speakers (THD+N< 0.4%)**
- **< 0.08% THD+N at 1 W, 1 kHz, Into 4-Ω Load**
- **Extremely Efficient Third Generation 5-V Class-D Technology:**
  - **Low Supply Current (No Filter) . . . 8 mA**
  - **Low Supply Current (Filter) . . . 15 mA**
  - **Low Shutdown Current . . . 1 µA**
  - **Low Noise Floor . . . 56 μV_{RMS}**
  - **Maximum Efficiency Into 3 Ω, 65-70%**
  - **Maximum Efficiency Into 8 Ω, 75-85%**
  - **4 Internal Gain Settings . . . 8-23.5 dB**
  - **PSRR . . . -77 dB**
- **Integrated Depop Circuitry**
- **Short-Circuit Protection (Short to Battery, Ground, and Load)**
- **-40°C to 85°C Operating Temperature Range**

PW OR PWP PACKAGE
(TOP VIEW)



DESCRIPTION

The TPA2000D2 is the third generation 5-V class-D amplifier from Texas Instruments. Improvements to previous generation devices include: lower supply current, lower noise floor, better efficiency, four different gain settings, smaller packaging, and fewer external components. The most significant advancement with this device is its modulation scheme that allows the amplifier to operate without the output filter. Eliminating the output filter saves the user approximately 30% in system cost and 75% in PCB area.

The TPA2000D2 is a monolithic class-D power IC stereo audio amplifier, using the high switching speed of power MOSFET transistors. These transistors reproduce the analog signal through high-frequency switching of the output stage. The TPA2000D2 is configured as a bridge-tied load (BTL) amplifier capable of delivering greater than 2 W of continuous average power into a 3-Ω load at less than 1% THD+N from a 5-V power supply in the high fidelity range (20 Hz to 20 kHz). With 1 W being delivered to a 4-Ω load at 1 kHz, the typical THD+N is less than 0.08%.

A BTL configuration eliminates the need for external coupling capacitors on the output. Low supply current of 8 mA makes the device ideal for battery-powered applications. Protection circuitry increases device reliability: thermal, over-current, and under-voltage shutdown.

Efficient class-D modulation enables the TPA2000D2 to operate at full power into 3-Ω loads at an ambient temperature of 85°C.

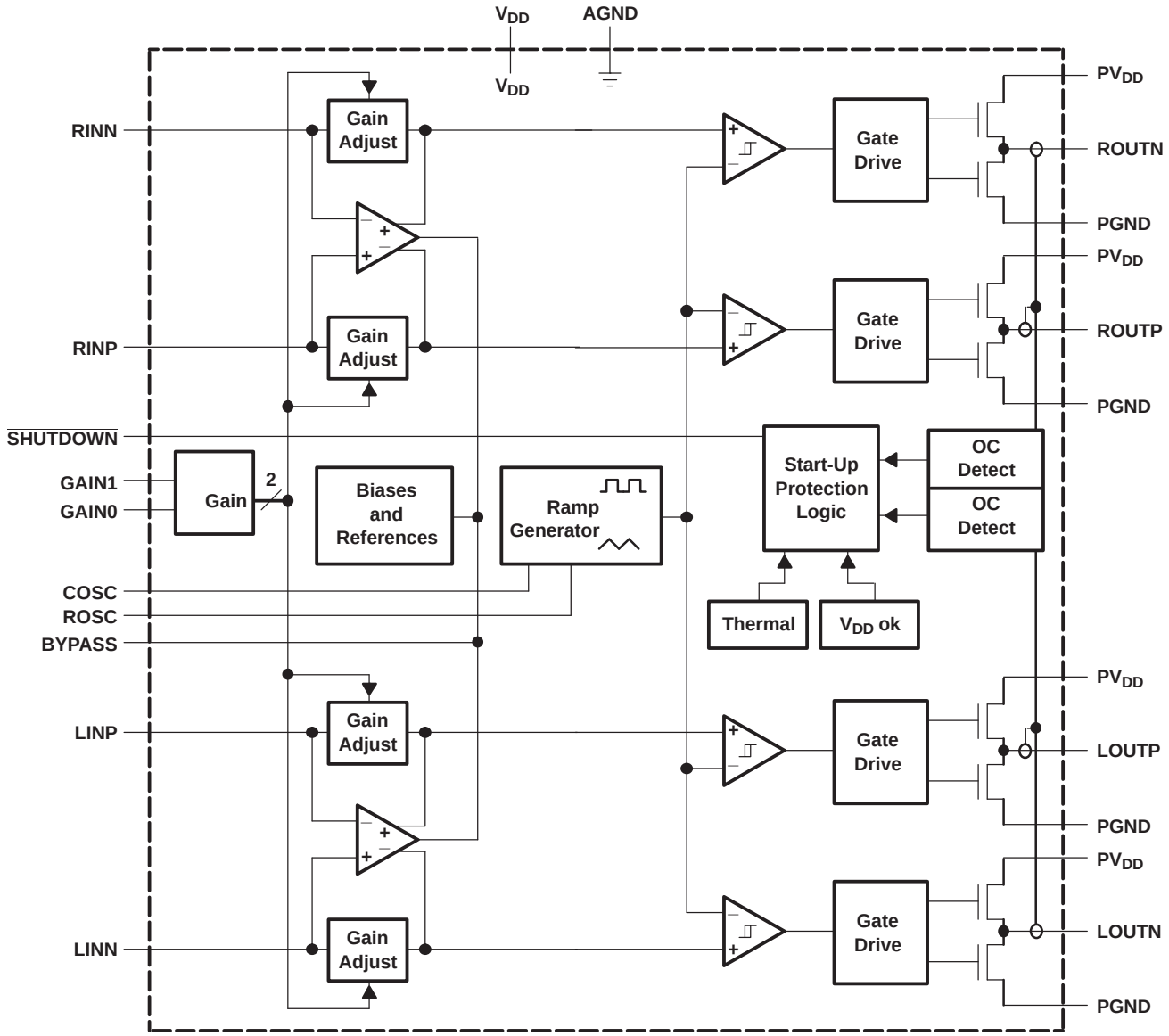
AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICE	
	TSSOP (PW)	TSSOP (PWP)(2)
–40°C to 85°C	TPA2000D2PW	TPA2000D2PWP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA2000D2PWPR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



TERMINAL FUNCTION

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	6	-	Analog ground
BYPASS	22	I	Tap to voltage divider for internal midsupply bias generator used for analog reference.
COSC	7	I	A capacitor connected to this terminal sets the oscillation frequency in conjunction with ROSC. For proper operation, connect a 220 pF capacitor from COSC to ground.
GAIN0	3	I	Bit 0 of gain control (TTL logic level)
GAIN1	15	I	Bit 1 of gain control (TTL logic level)
LINN	5	I	Left channel negative differential audio input
LINP	20	I	Left channel positive differential audio input
LOUTN	2	O	Left channel negative audio output
LOUTP	23	O	Left channel positive audio output
PGND	1, 24	-	Power ground for left channel H-bridge
	12, 13	-	Power ground for right channel H-bridge
PV_{DD}	4, 21	-	Power supply for left channel H-bridge
	9, 16	-	Power supply for right channel H-bridge
RINN	8	I	Right channel negative differential audio input
RINP	17	I	Right channel positive differential audio input
ROSC	18	I	A resistor connected to this terminal sets the oscillation frequency in conjunction with COSC. For proper operation, connect a 120 kΩ resistor from ROSC to ground.
ROUTN	11	O	Right channel negative audio output
ROUTP	14	O	Right channel positive output
$\overline{\text{SHUTDOWN}}$	10	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal; normal operation if a TTL logic high is placed on this terminal.
V_{DD}	19	-	Analog power supply

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{DD}, PV_{DD}	Supply voltage	-0.3 V to 6 V
V_I	Input voltage	-0.3 V to V_{DD}+0.3 V
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature range	-40°C to 85°C
T_J	Operating junction temperature range	-40°C to 150°C
T_{stg}	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW	1.04 W	8.34 mW/°C	0.67 W	0.54 W
PWP	2.7 W	21.8 mW/°C	1.7 W	1.4 W

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{DD}, PV_{DD}	Supply voltage		4.5		5.5	V
V_{IH}	High-level input voltage	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$	2			V
V_{IL}	Low-level input voltage	GAIN0, GAIN1, $\overline{\text{SHUTDOWN}}$			0.8	V
R_{OSC}	Oscillator resistance			120		kΩ
C_{OSC}	Oscillator capacitance			220		pF
f_s	Switching frequency		200		300	kHz
T_A	Operating free-air temperature		-40		85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = PV_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	V_I = 0 V			25	mV
PSRR	Power supply rejection ratio	V_{DD}=PV_{DD} = 4.5 V to 5.5 V		-77		dB
I_{IH}	High-level input current	V_{DD}=PV_{DD} = 5.5 V, V_I = V_{DD} = PV_{DD}			1	µA
I_{IL}	Low-level input current	V_{DD}=PV_{DD} = 5.5 V, V_I = 0 V			1	µA
I_{DD}	Supply current	No filter (with or without speaker load)		8	10	mA
I_{DD}	Supply current	With filter, L = 22 µH, C = 1 µF		15		mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	15	µA

OPERATING CHARACTERISTICS

T_A = 25°C, V_{DD} = PV_{DD} = 5 V, R_L = 4 Ω, Gain = 8 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.1%, f = 1 kHz, R_L = 3 Ω		2		W
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 20 Hz to 20 kHz		<0.5%		
B_{OM}	Maximum output power bandwidth	THD = 5%		20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz, $C_{(BYPASS)}$ = 0.4 µF		-60		dB
SNR	Signal-to-noise ratio			87		dBV
	Integrated noise floor	20 Hz to 20 kHz, No input		56		µV
Z_I	Input impedance			>20		kΩ

Table 1. Gain Settings

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	8	104
0	1	12	74
1	0	17.5	44
1	1	23.5	24

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Output power	2, 3
	FFT at 1.5 W output power	vs Frequency	4
THD+N	Total harmonic distortion plus noise	vs Output power	5-7
		vs Frequency	8, 9
	Crosstalk	vs Frequency	10
	Power supply rejection ratio	vs Frequency	11

TEST SET-UP FOR GRAPHS

The THD+N measurements shown do not use an LC output filter, but use a low pass filter with a cutoff frequency of 20 kHz so the switching frequency does not dominate the measurement. This is done to ensure that the THD+N measured is just the audible THD+N. The THD+N measurements are shown at the highest gain for worst case.

The LC output filter used in the efficiency curves (Figure 2 and Figure 3) is shown in Figure 1.

L1 = L2 = 22 µH (DCR = 110 mΩ,

Part number = SCD0703T-220 M-S,

Manufacturer = GCI)

C1 = C2 = 1 µF

The ferrite filter used in the efficiency curves (Figure 2 and Figure 3) is shown in Figure 1, where L is a ferrite bead.

L1 = L2 = ferrite bead (part number = 2512067007Y3, manufacturer = Fair-Rite)

C1 = C2 = 1 nF

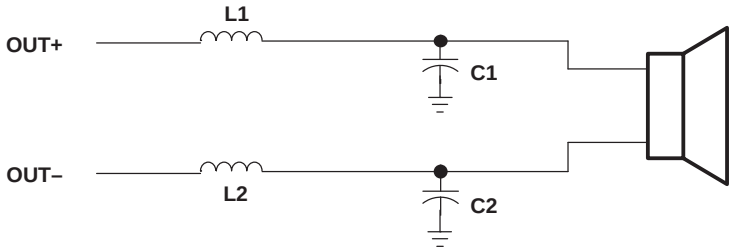


Figure 1. Class-D Output Filter

TYPICAL CHARACTERISTICS

EFFICIENCY
vs
OUTPUT POWER

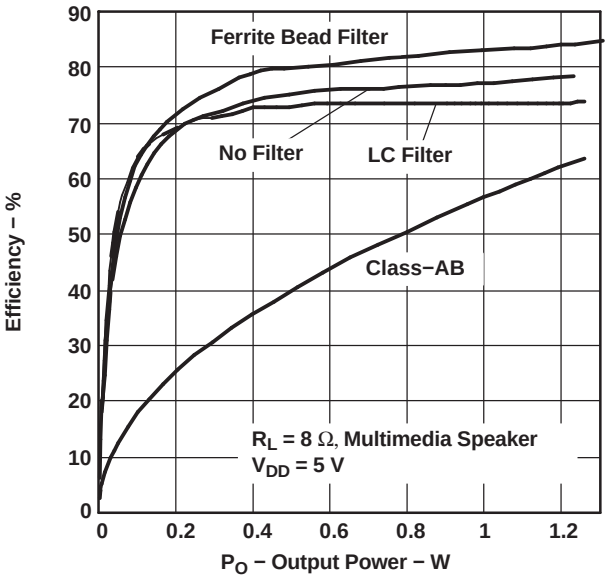


Figure 2.

EFFICIENCY
vs
OUTPUT POWER

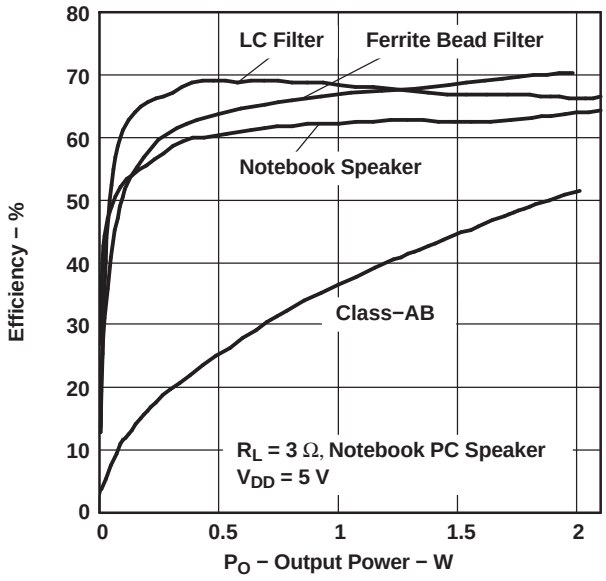


Figure 3.

FFT AT 1.5 W OUTPUT POWER
vs
FREQUENCY

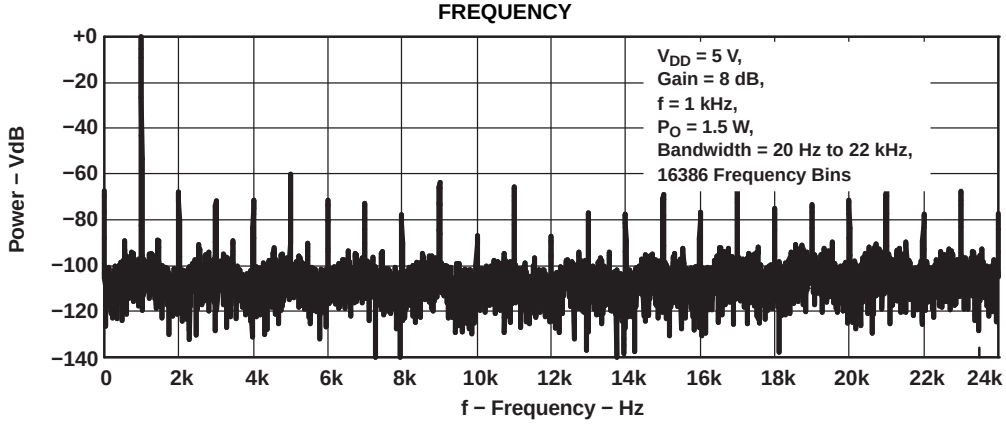


Figure 4.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

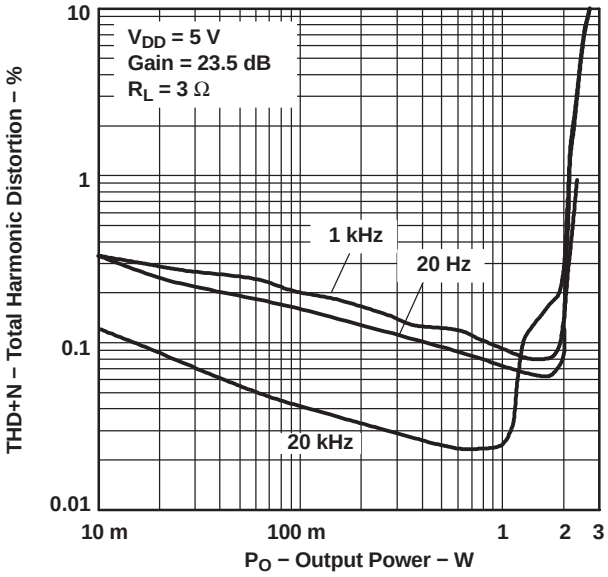


Figure 5.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

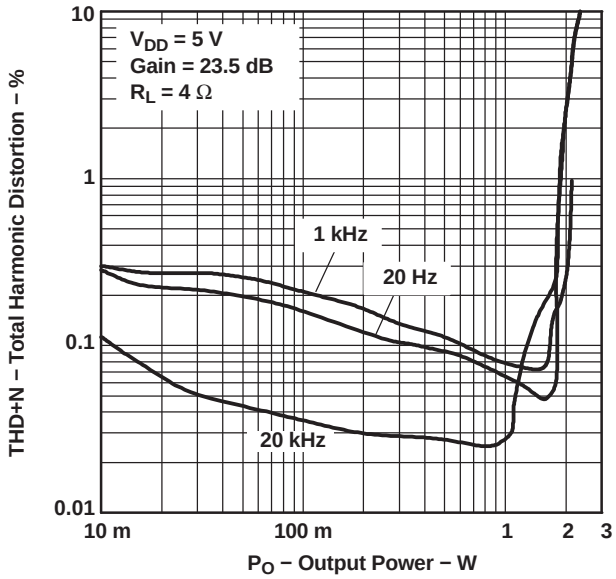


Figure 6.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

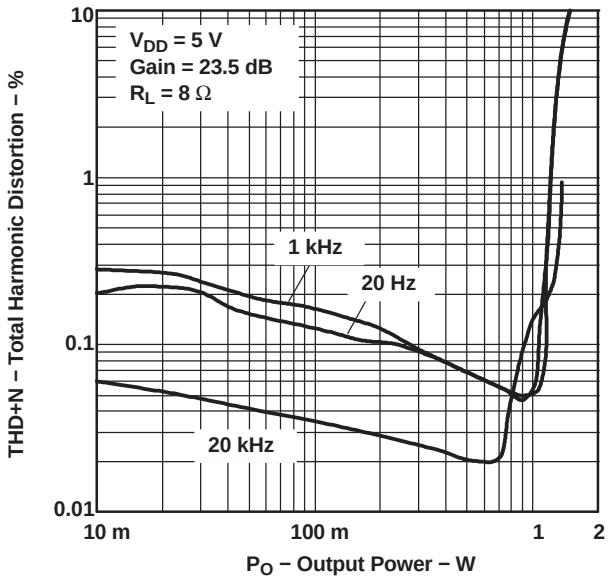


Figure 7.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

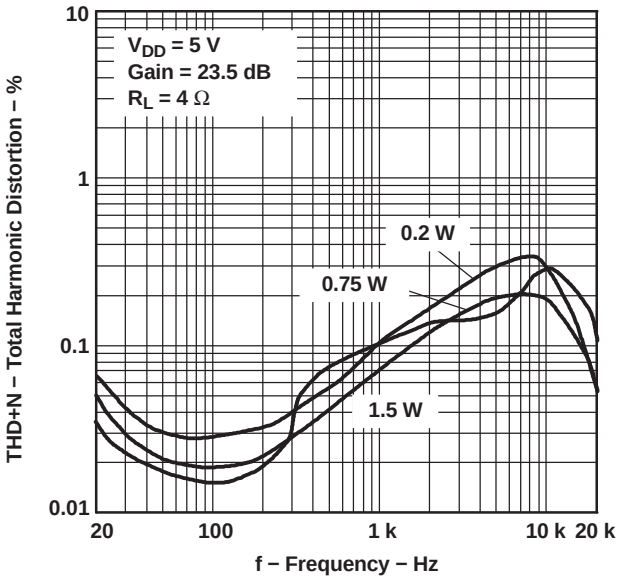


Figure 8.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

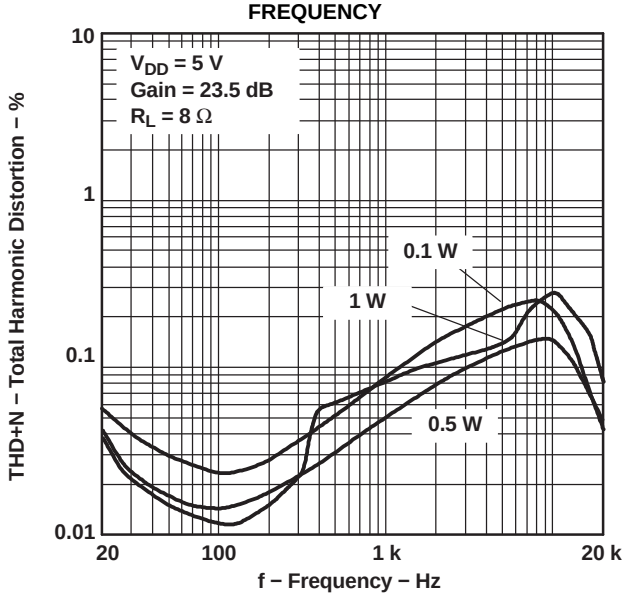


Figure 9.

CROSSTALK
vs
FREQUENCY

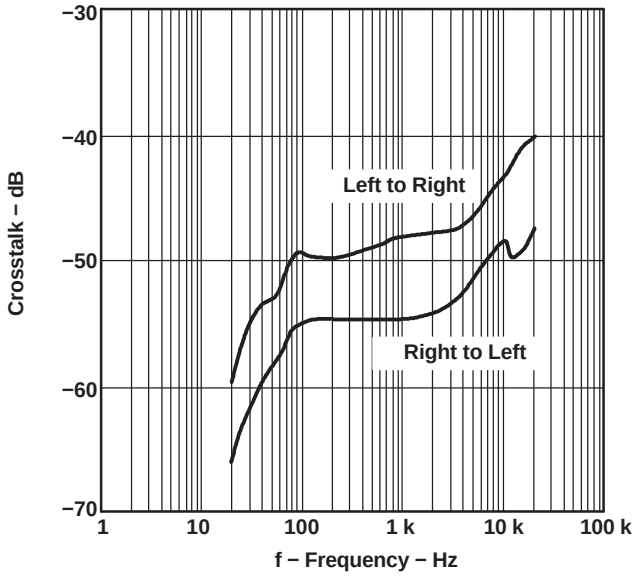


Figure 10.

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

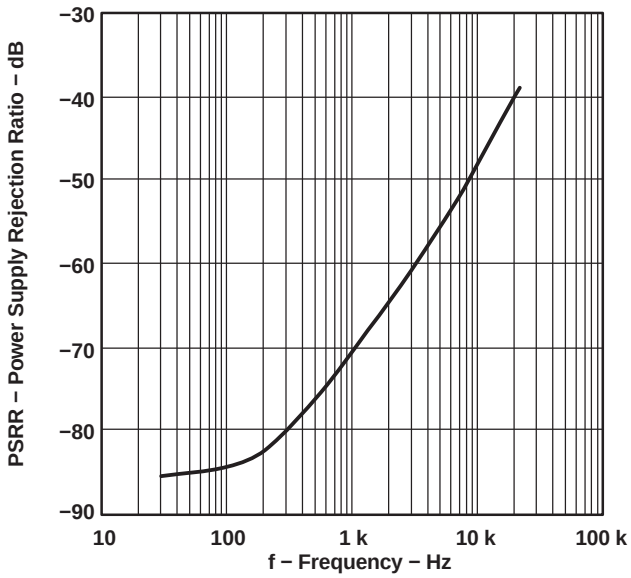


Figure 11.

APPLICATION INFORMATION

ELIMINATING THE OUTPUT FILTER WITH THE TPA2000D2

This section focuses on why the user can eliminate the output filter with the TPA2000D2.

EFFECT ON AUDIO

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

TRADITIONAL CLASS-D MODULATION SCHEME

The traditional class-D modulation scheme, which is used in the TPA005Dxx family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{DD}. Therefore, the differential prefiltered output varies between positive and negative V_{DD}, where filtered 50% duty cycle yields 0 volts across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 12. Note that even at an average of 0 volts across the load (50% duty cycle), the current to the load is high causing high loss, thus causing a high supply current.

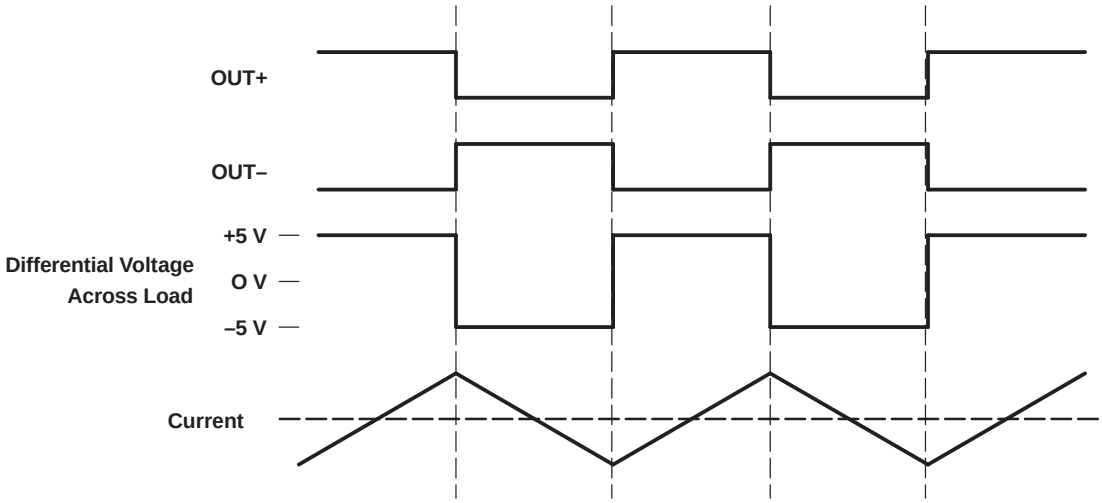


Figure 12. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA2000D2 MODULATION SCHEME

The TPA2000D2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUT+ and OUT- are now in phase with each other with no input. The duty cycle of OUT+ is greater than 50% and OUT- is less than 50% for positive voltages. The duty cycle of OUT+ is less than 50% and OUT- is greater than 50% for negative voltages. The voltage across the load sits at 0 volts throughout most of the switching period greatly reducing the switching current, which reduces any I^2R losses in the load.

APPLICATION INFORMATION (continued)

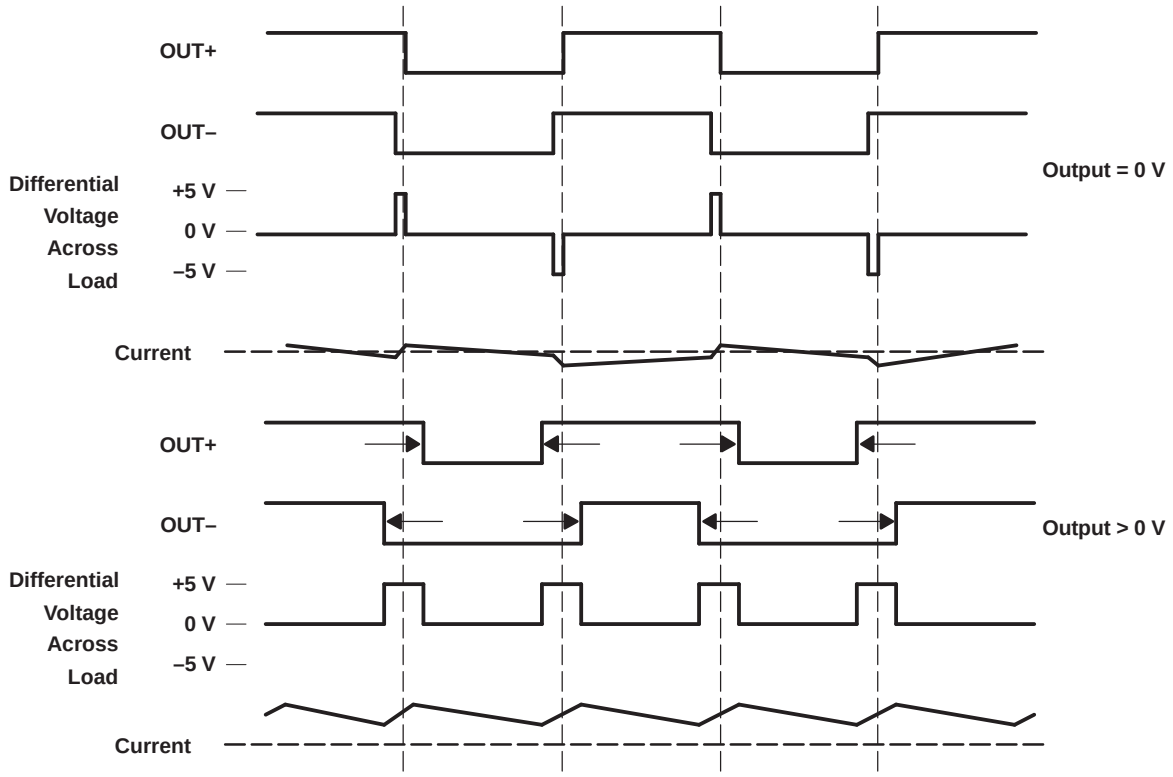


Figure 13. The TPA2000D2 Output Voltage and Current Waveforms Into an Inductive Load

EFFICIENCY: WHY YOU MUST USE A FILTER WITH THE TRADITIONAL CLASS-D MODULATION SCHEME

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{DD}$ and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2000D2 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{DD} instead of $2 \times V_{DD}$. As the output power increases, the pulses widen making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker, which results in less power dissipated and increased efficiency.

EFFECTS OF APPLYING A SQUARE WAVE INTO A SPEAKER

Audio specialists have said for years not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, is not significant because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is very small. However,

APPLICATION INFORMATION (continued)

damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load needs to be calculated by subtracting the theoretical supplied power, $P_{SUP\ THEORETICAL}$, from the actual supply power, P_{SUP}, at maximum output power, P_{OUT}. The switching power dissipated in the speaker is the inverse of the measured efficiency, $\eta_{MEASURED}$, minus the theoretical efficiency, $\eta_{THEORETICAL}$.

$$P_{SPKR} = P_{SUP} - P_{SUP\ THEORETICAL} \text{ (at max output power)} \quad (1)$$

$$P_{SPKR} = P_{SUP} / P_{OUT} - P_{SUP\ THEORETICAL} / P_{OUT} \text{ (at max output power)} \quad (2)$$

$$P_{SPKR} = 1/\eta_{MEASURED} - 1/\eta_{THEORETICAL} \text{ (at max output power)} \quad (3)$$

The maximum efficiency of the TPA2000D2 with an 8-Ω load is 85%. Using Equation 3 with the efficiency at maximum power from Figure 2 (78%), we see that there is an additional 106 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

WHEN TO USE AN OUTPUT FILTER

Design the TPA2000D2 without the filter if the traces from amplifier to speaker are short. The TPA2000D2 passed FCC and CE radiated emissions with no shielding with speaker wires 8 inches (20,32 cm) long or less. Notebook PCs and powered speakers where the speaker is in the same enclosure as the amplifier are good applications for class-D without a filter.

A ferrite bead filter can often be used if the design is failing radiated emissions without a filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

GAIN SETTING VIA GAIN0 AND GAIN1 INPUTS

The gain of the TPA2000D2 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 2 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance may shift by 30% due to shifts in the actual resistance of the input resistors.

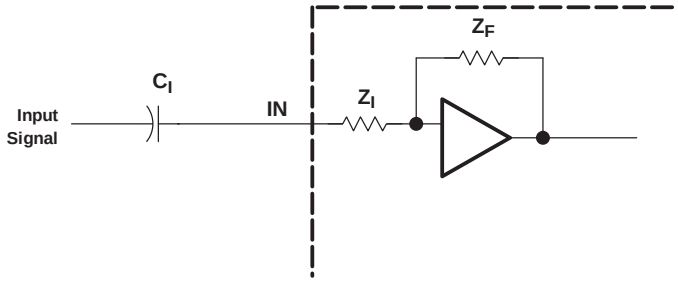
For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 20 kΩ, which is the absolute minimum input impedance of the TPA2000D2. At the lower gain settings, the input impedance could increase to as high as 115 kΩ.

Table 2. Gain Settings

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	8	104
0	1	12	74
1	0	17.5	44
1	1	23.5	24

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value.



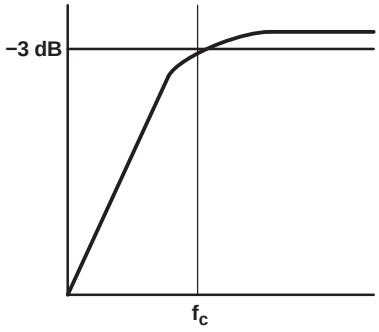
The -3 dB frequency can be calculated using Equation 4:

$$f_{-3\ dB} = \frac{1}{2\pi C_I Z_I} \quad (4)$$

INPUT CAPACITOR, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in Equation 5.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (5)$$



The value of C_I is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 20 kΩ and the specification calls for a flat bass response down to 80 Hz. Equation 5 is reconfigured as Equation 6.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (6)$$

In this example, C_I is 0.1 µF, so one would likely choose a value in the range of 0.1 µF to 1 µF. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

C_I should be 10 times smaller than the bypass capacitor to reduce clicking and popping noise from power on/off and entering and leaving shutdown. After sizing CI for a given cutoff frequency, size the bypass capacitor up to 10 times that of the input capacitor.

$$C_I \le C_{BYP} / 10 \quad (7)$$

SWITCHING FREQUENCY

The switching frequency is determined using the values of the components connected to R_{OSC} (pin 18) and C_{OSC} (pin 7) and is calculated with the following equation:

$$f_S = \frac{6.6}{R_{OSC} C_{OSC}} \quad (8)$$

The switching frequency was chosen to be centered on 250 kHz. This frequency is the optimum audio fidelity of oversampling and of maximizing efficiency by minimizing the switching losses of the amplifier. The recommended values are a resistance of 120 kΩ and a capacitance of 220 pF. Using these component values, the amplifier operates properly by using 5% tolerance resistors and 10% tolerance capacitors. The tolerance of the components can be changed, as long as the switching frequency remains between 200 kHz and 300 kHz. Within this range, the internal circuitry of the device provides stable operation.

POWER SUPPLY DECOUPLING, C_S

The TPA2000D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, C_{BYP}

The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown. To have minimal pop, C_{BYP} should be 10 times larger than C_I.

$$C_{BYP} \geq 10 \times C_I \quad (9)$$

DIFFERENTIAL INPUT

The differential input stage of the amplifier cancels any noise that appears on both input lines of a channel. To use the TPA2000D2 EVM with a differential source, connect the positive lead of the audio source to the RINP (LINP) input and the negative lead from the audio source to the RINN (LINN) input. To use the TPA2000D2 with a single-ended source, ac ground the RINN and LINN inputs through a capacitor and apply the audio single to the RINP and LINP inputs. In a single-ended input application, the RINN and LINN inputs should be ac-grounded at the audio source instead of at the device inputs for best noise performance.

SHUTDOWN MODES

The TPA2000D2 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(SD)}$ = 1 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected, because amplifier operation would be unpredictable.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

EVALUATION CIRCUIT

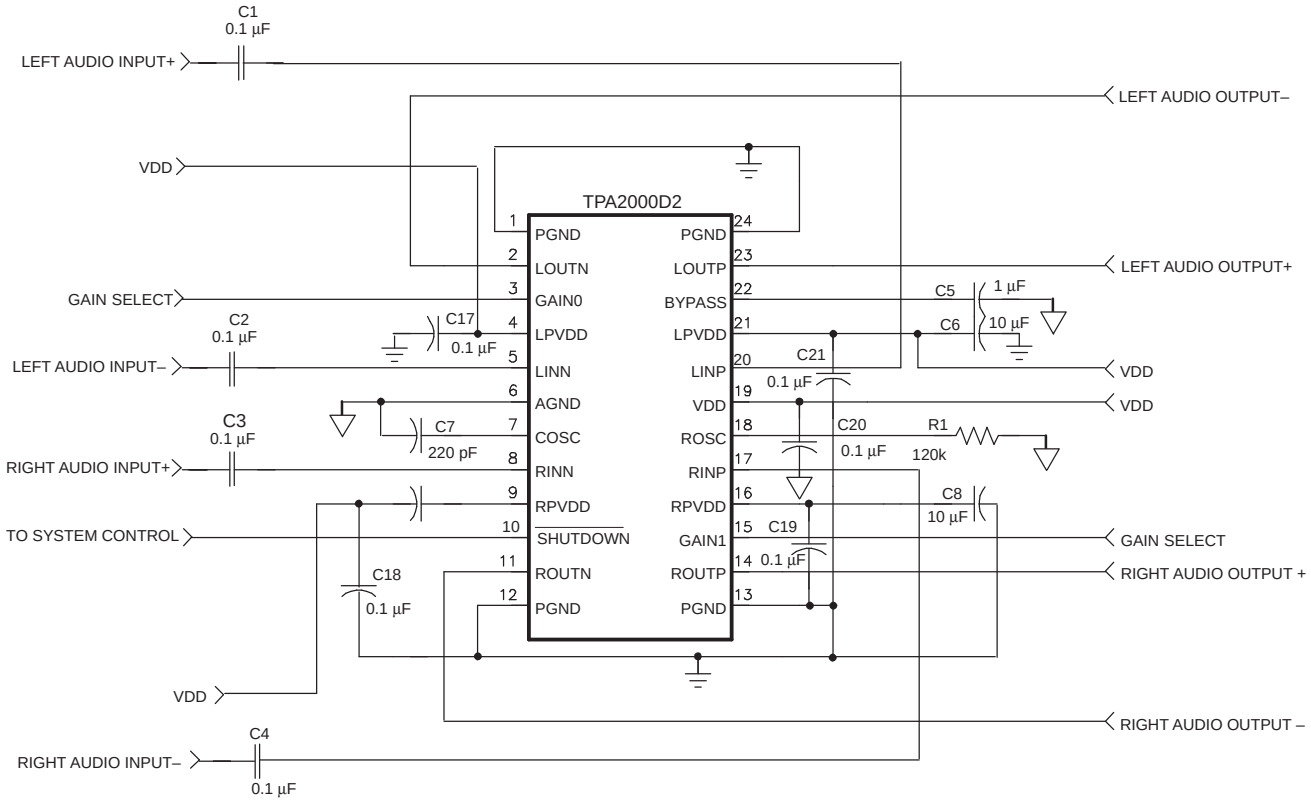


Table 3. TPA2000D2 Application Bill of Materials

REFERENCE	DESCRIPTION	SIZE	QUANTITY	MANUFACTURER	PART NUMBER
C1-4, C17-21	Capacitor, ceramic chip, 0.1 µF, ±10%, X7R, 50 V	0805	9	Kemet	C0805C104K5RAC
C5	Capacitor, ceramic, 1.0 µF, 80%/-20%, Y5V, 16 V	0805	1	Murata	GRM40-Y5V105Z16
C6, C8	Capacitor, ceramic, 10 µF, 80%/-20%, Y5V, 16 V	1210	2	Murata	GRM235-Y5V106Z16
C7	Capacitor, ceramic, 220 pF, ±10%, XICON, 50 V	0805	2	Mouser	140-CC501B221K
R1	Resistor, chip, 120 kΩ, 1/10 W, 5%, XICON	0805	1	Mouser	260-120K
U1	IC, TPA2000D2, audio power amplifier, 2-W, 2-channel, class-D	24 pin TSSOP	1	TI	TPA2000D2PWP

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA2000D2PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA2000D2	Samples
TPA2000D2PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA2000D2	Samples
TPA2000D2PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA2000D2	Samples
TPA2000D2PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA2000D2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

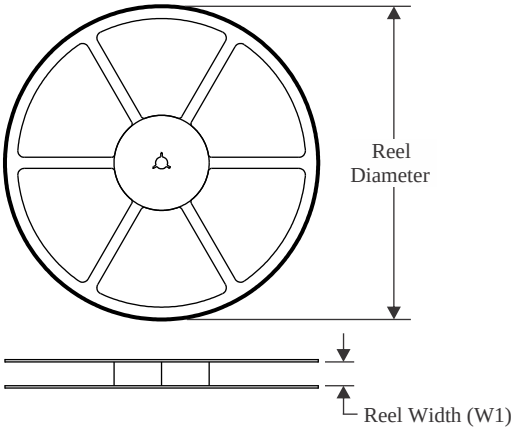
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

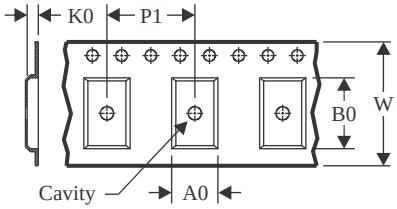
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

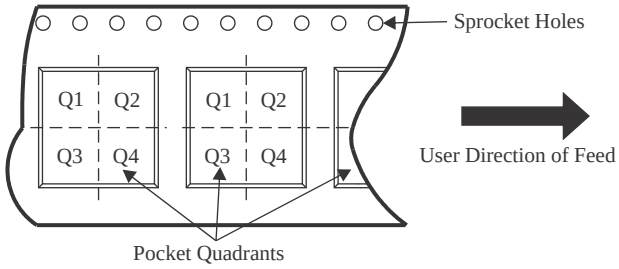


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

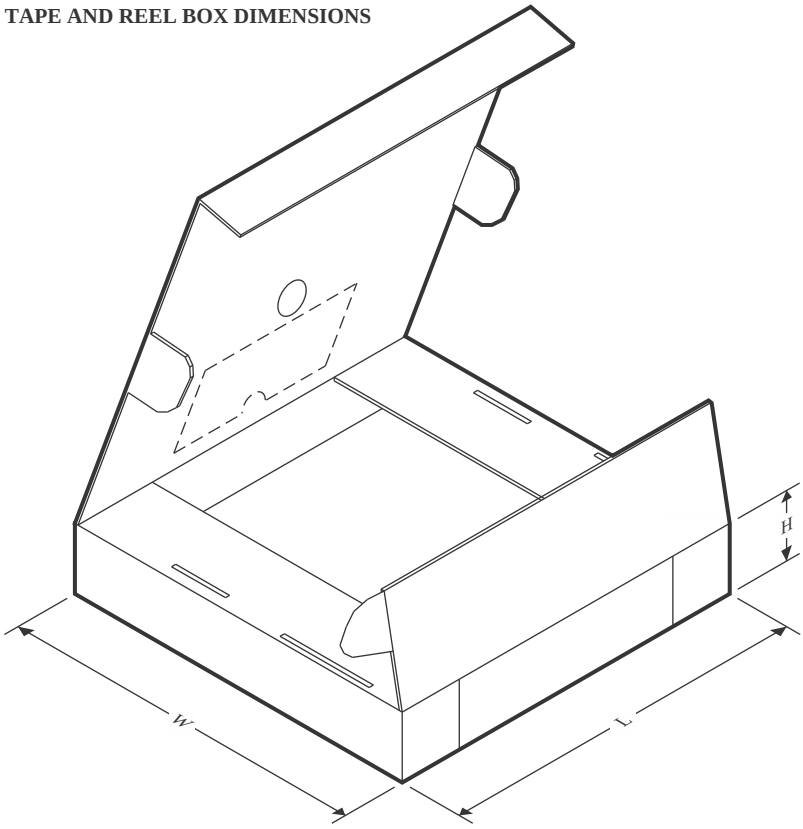
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2000D2PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPA2000D2PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

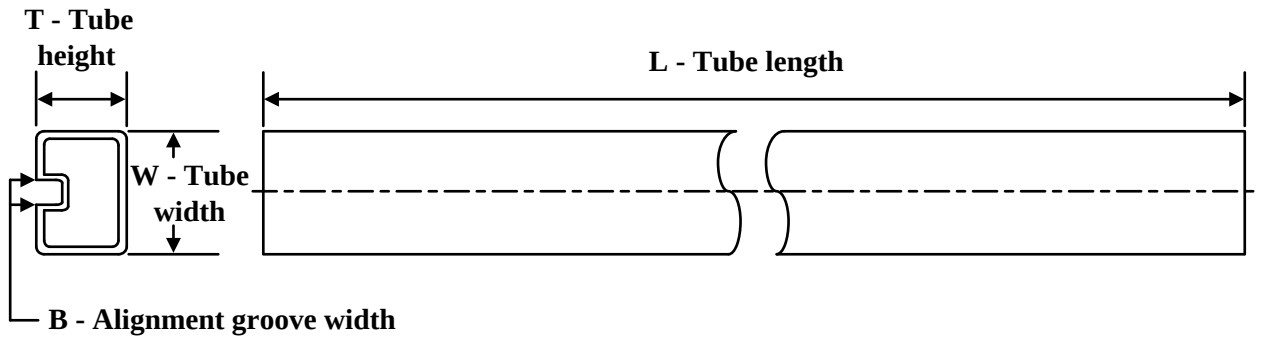
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2000D2PWPR	HTSSOP	PWP	24	2000	356.0	356.0	35.0
TPA2000D2PWR	TSSOP	PW	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

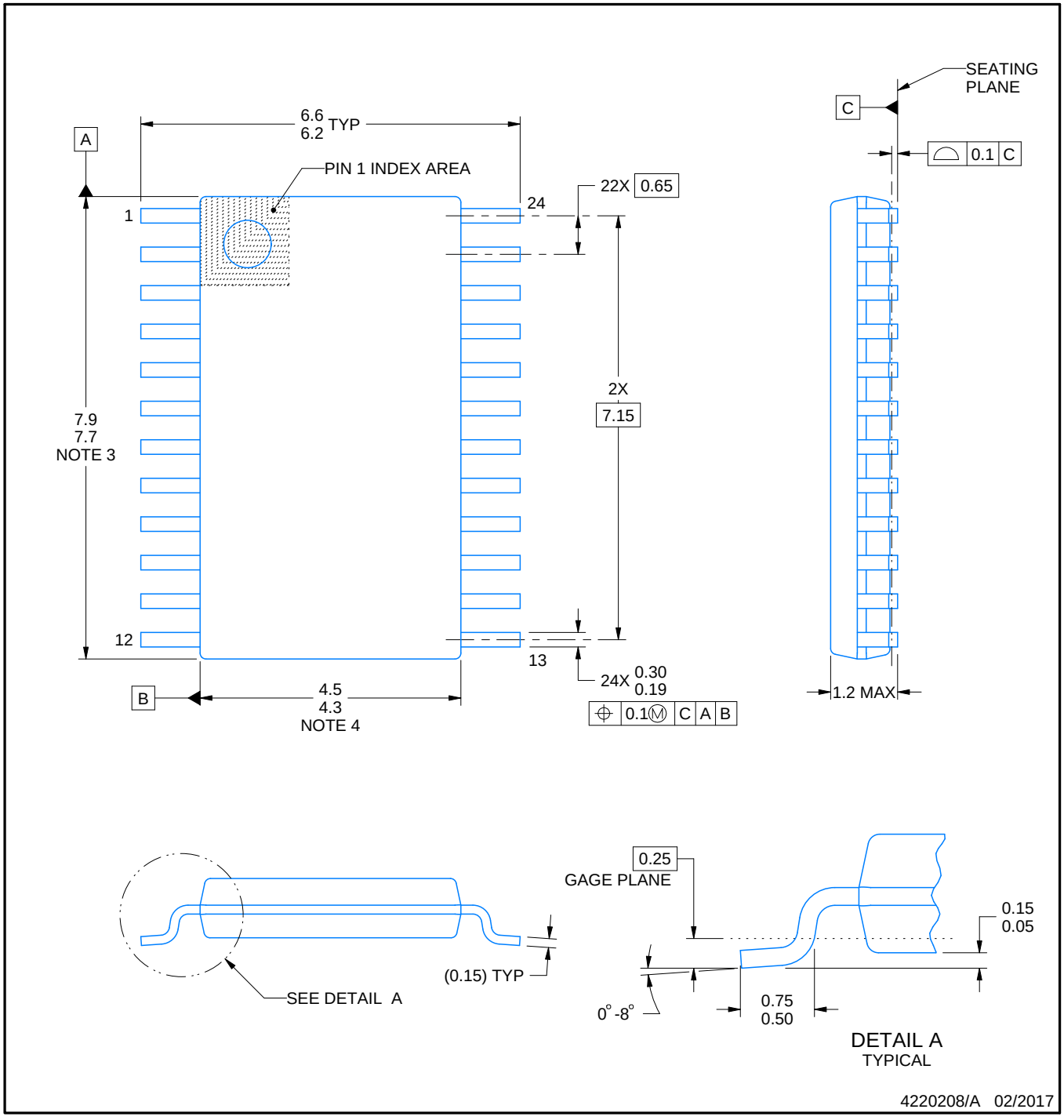
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA2000D2PW	PW	TSSOP	24	60	530	10.2	3600	3.5
TPA2000D2PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPA2000D2PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

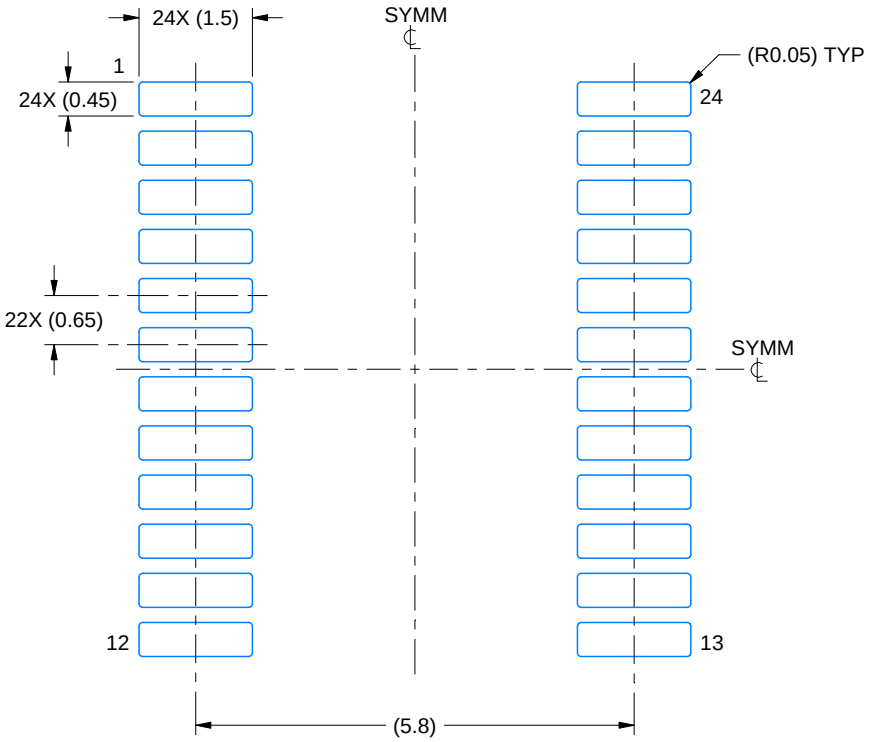
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

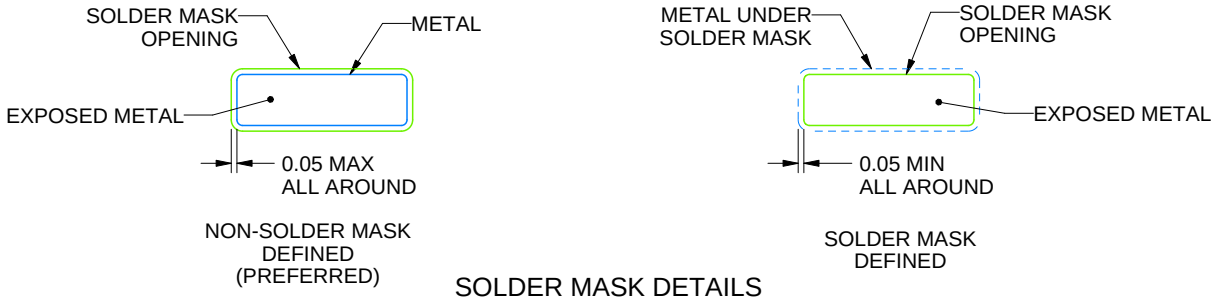


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

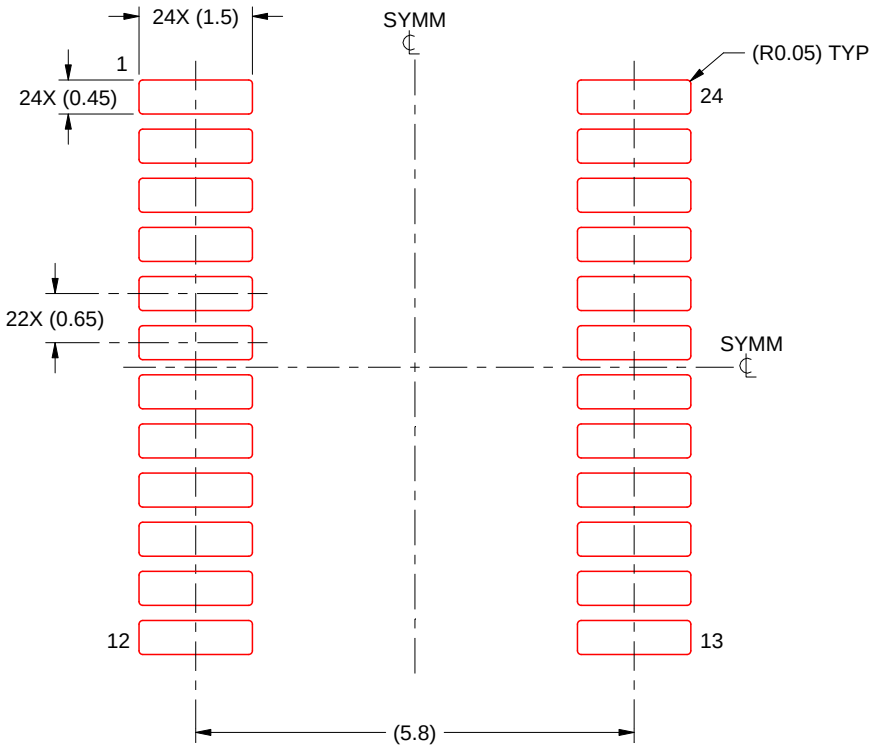


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

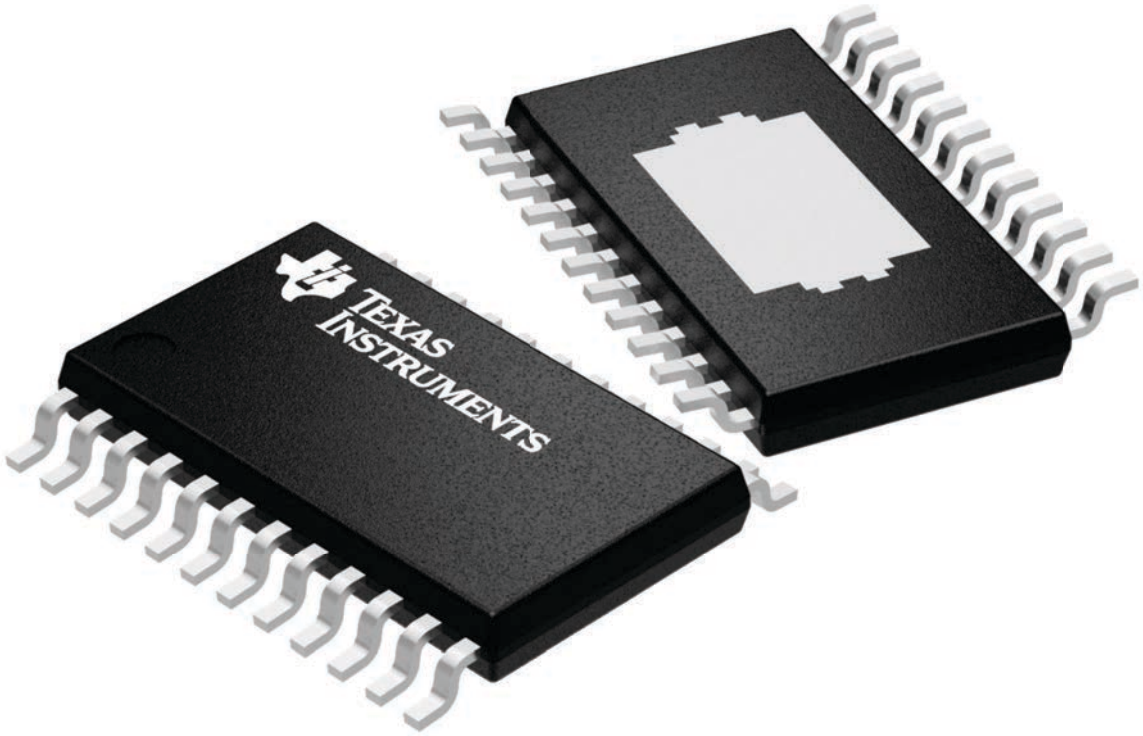
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



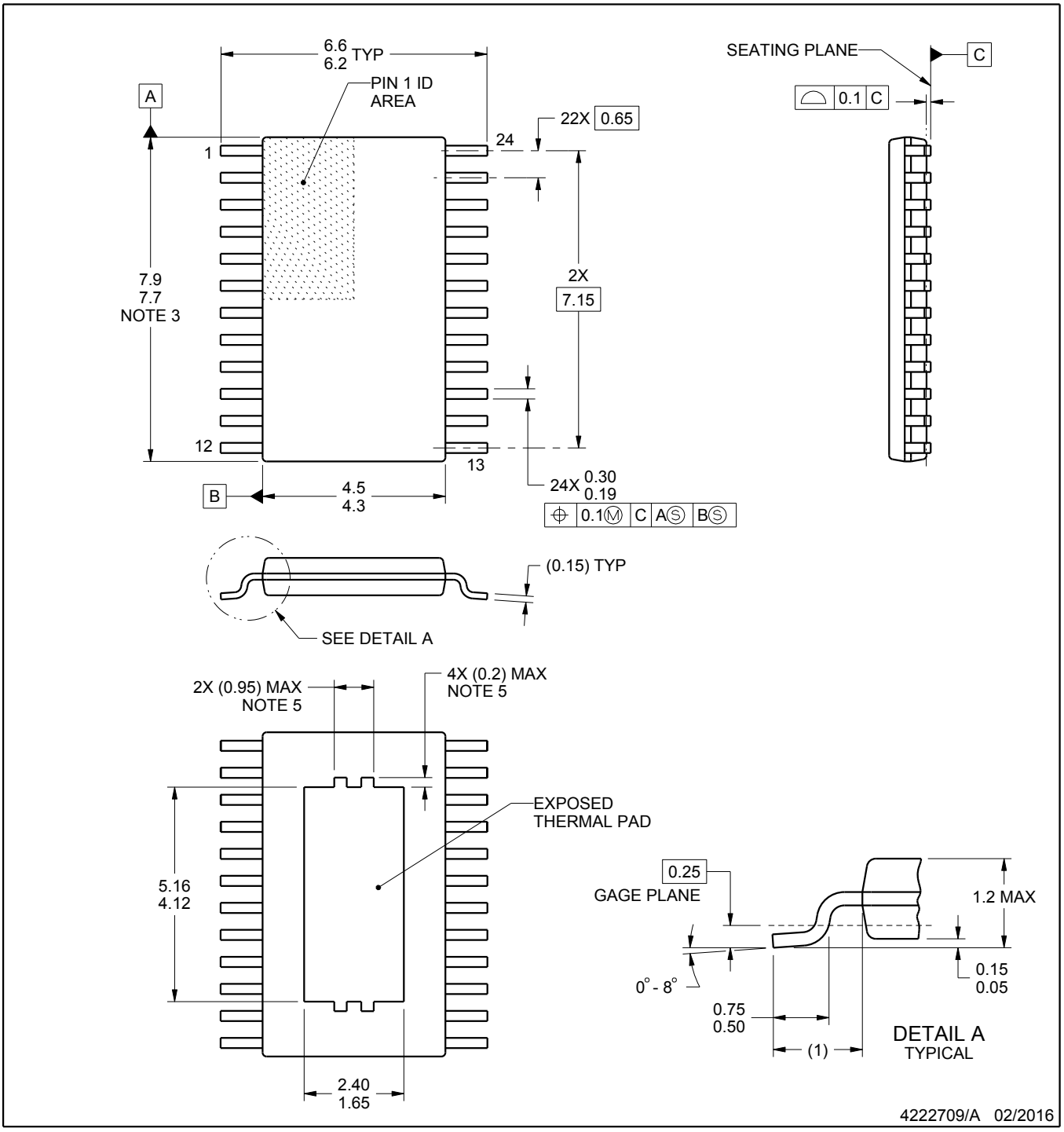
4224742/B

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

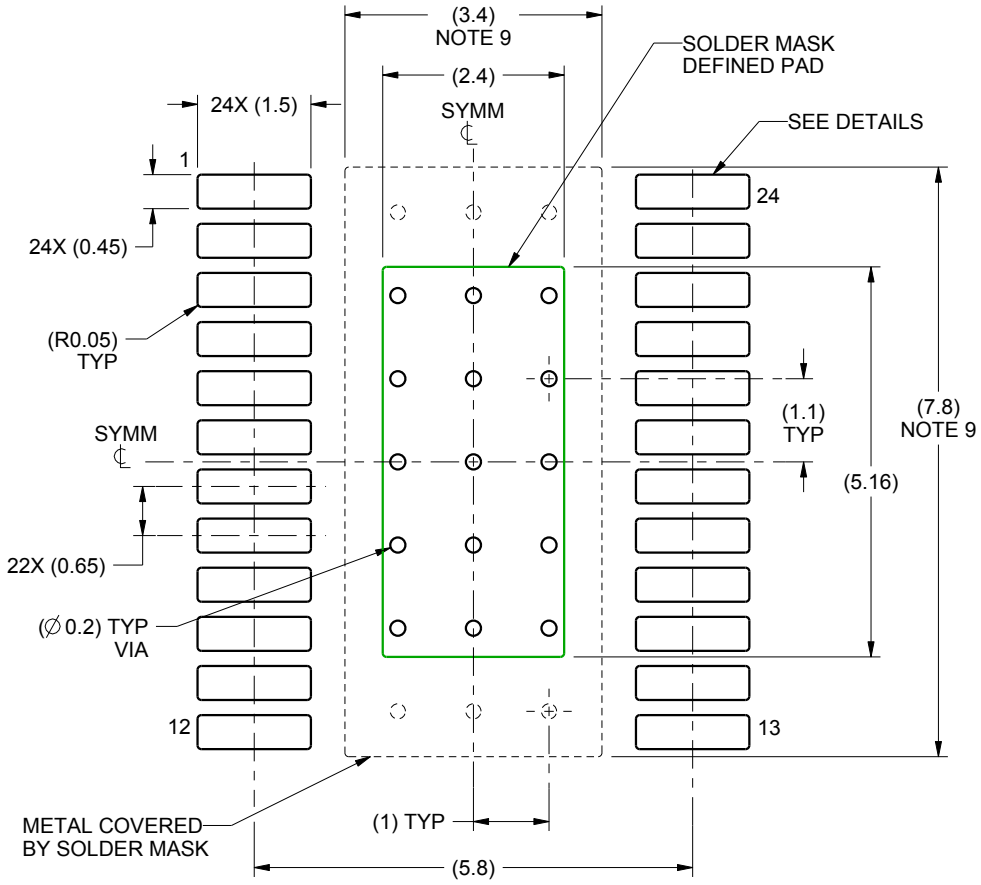
PLASTIC SMALL OUTLINE



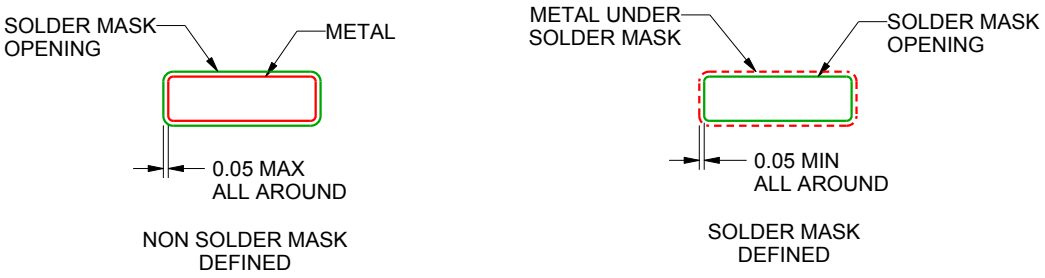
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

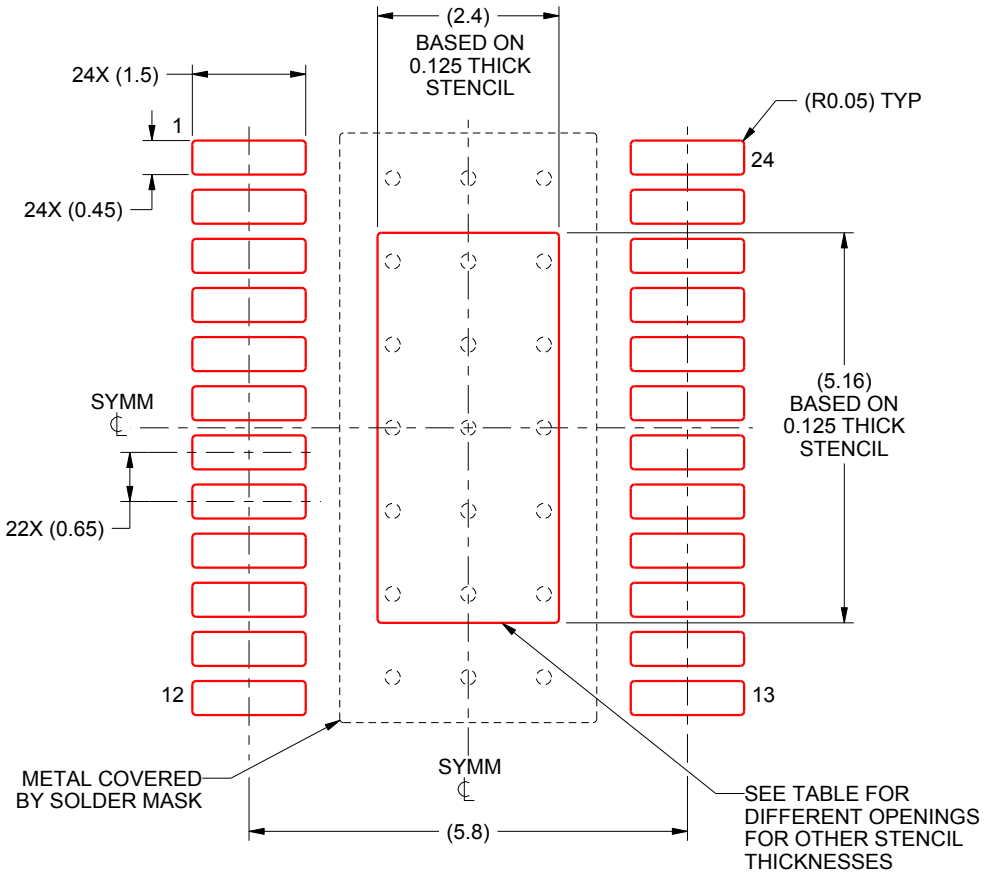


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265