

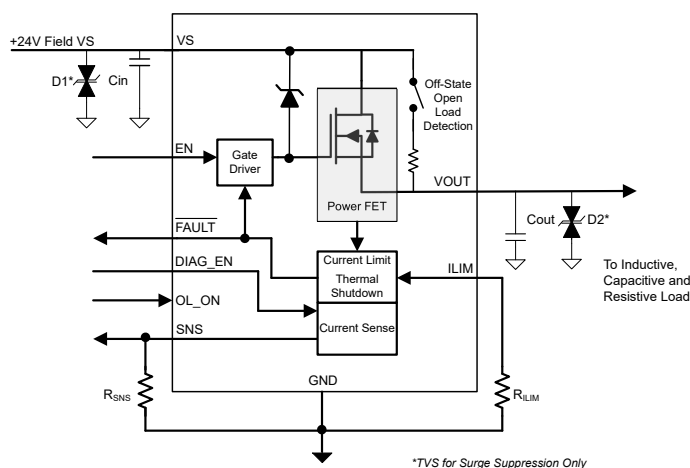
# TPS281C30x 60V Tolerant, 30mΩ, Single-Channel Smart High-Side Switch

## 1 Features

- Wide operating voltage range: 6V to 36V
- 64V DC tolerance when disabled
- Low  $R_{ON}$ : 30mΩ typ, 55mΩ max
- Improve system level reliability through [adjustable current limiting](#)
  - Version A, C: 1A to 5A (fixed 0.5A)
  - Version B, D, E: 2A to 10A (fixed 0.5A)
- Accurate current sensing
  - ±4% at 1A in standard sense mode
  - ±12.5% at 6mA in high accuracy sense mode
- Integrated inductive discharge clamp > 65V
- Low standby current of < 1μA (standby mode only available in version A, B, C, D)
- Low quiescent current ( $I_q$ ) of < 1.5mA
- [Functional safety capable](#)
- Operating junction temperature: –40 to 125°C
- Input control: 1.8V, 3.3V, and 5V logic compatible
- Integrated fault sense voltage scaling for ADC protection
- Open-load detection in off-state
- Thermal shutdown and swing detection
- 14-pin thermally-enhanced TSSOP package
- 20-pin thermally-enhanced QFN package

## 2 Applications

- [Digital output module](#)
- [Safe torque off \(STO\)](#)
- [Holding brake](#)
- [General resistive, inductive, and capacitive loads](#)



**Typical Application Schematic**

## 3 Description

TPS281C30x is a single channel smart high-side switch designed to meet the requirements of industrial control systems. The low  $R_{ON}$  (30mΩ) minimizes device power dissipation, driving a wide range of output load current up to 6A DC and the 64V DC tolerance improves system robustness.

The device integrates protection features such as thermal shut down, output clamp, and current limit. These features improve system robustness during fault events such as short circuit. TPS281C30x implements an adjustable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. In order to drive high inrush current loads such as lamps or fast charging capacitive loads, TPS281C30x implements an inrush current time period with a higher level of allowed current. The device also provides an accurate load current sense that allows for improved load diagnostics such as overload and open-load detection enabling better predictive maintenance.

TPS281C30E provides enhanced Electrical Fast Transient (EFT) immunity, where the device will stay off with up to 2.5kV EFT pulse applied at VS or VOUT, 10nF output capacitor and 100pF coupling capacitor between the pulse generator and the output. The EFT level can be further increased if a larger output capacitor is used. The enhanced EFT immunity improves the system's robustness against undesired coupling in the industrial systems.

TPS281C30x is available in a small 14-pin, 4.4mm × 5mm HTSSOP leaded package (version A, B, C, D) with 0.65mm pin pitch and 20-pin, 5mm × 5mm QFN with 0.65mm pin pitch (all versions) minimizing the PCB footprint.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TPS281C30x	RGW (QFN, 20)	5.00mm × 5.00mm
	PWP (HTSSOP, 14)	5.00mm × 6.40mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet. Version E only available in QFN package.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



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## 4 Device Comparison Table

**Table 4-1. Device Options**

DEVICE VERSION	PART NUMBER	CURRENT LIMIT RANGE	INTEGRATED CLAMP FOR INDUCTIVE LOADS	ENHANCED EFT IMMUNITY	STANDBY MODE DURING OFF STATE	OFF STATE OPEN LOAD DETECTION
A	TPS281C30A <sup>(1)</sup>	1 A to 5 A	Yes	No	Yes	Yes
B	TPS281C30B <sup>(1)</sup>	2 A to 10 A	Yes	No	Yes	Yes
C	TPS281C30C <sup>(1)</sup>	1 A to 5 A	No	No	Yes	Yes
D	TPS281C30D <sup>(1)</sup>	2 A to 10 A	No	No	Yes	Yes
E	TPS281C30E <sup>(2)</sup>	2 A to 10 A	No	Yes	No	No

- (1) Devices available in RGW package now. PWP package in preview. Contact TI for additional information.  
 (2) Device is only available in RGW package.

## 5 Pin Configuration and Functions

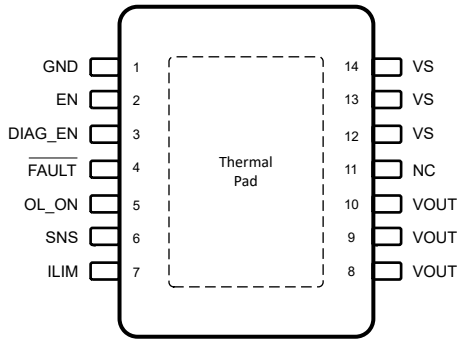


Figure 5-1. PWP Package, 14-Pin HTSSOP (Top View)

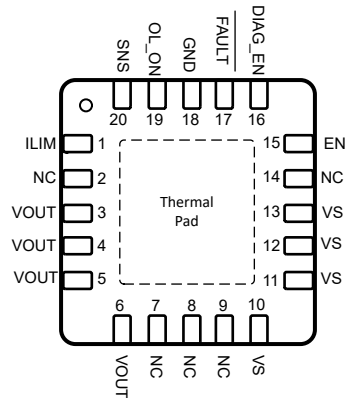


Figure 5-2. RGW Package, 20-Pin QFN (Top View)

Table 5-1. Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	PWP	RGW		
GND	1	18	Power	Ground of device. Connect to resistor- diode ground network to have reverse polarity protection.
EN	2	15	I	Input control for channel activation. Internal pull-down.
DIAG_EN	3	16	I	Enable-disable pin for diagnostics and current sensing. Internal pull-down.
FAULT	4	17	O	Open drain global fault output. Referred to $\overline{FLT}$ , or fault pin.
OL_ON	5	19	I	Enable-disable pin for higher resolution current sense(Only available when $I_{OUT} < I_{K_{SNS2\_EN}}$ ). Internal pull-down.
SNS	6	20	O	Analog current output corresponding to load current. Connect a resistor to GND to convert to voltage.
ILIM	7	1	O	Adjustable current limit. Connect a resistor to set the current limit. Optionally short to ground or leave pin floating to set the current limit to the default internal current limit. See the electrical characteristics for more information.
NC	11	2, 7, 8, 9, 14	N/A	No internal connection.
VOUT	8, 9, 10	3, 4, 5, 6	Power	Output of high side switch, connect to load.
VS	12, 13, 14	10, 11, 12, 13	Power	Power supply input.
Pad	Thermal Pad	Pad	—	Thermal pad, internally shorted to ground.

### Recommended Connection for Unused Pins

TPS281C30x is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins may be considered as optional.

Table 5-2. Connections for Optional Pins

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
SNS	Ground through 10-k $\Omega$ resistor	Analog sense is not available.
ILIM	Float	If the ILIM pin is left floating, the device will be set to the default internal current-limit threshold. This is considered a fault state for the device.
FAULT	Float	If the FAULT pin is unused, the system cannot read faults from the output.
DIAG_EN	Float or ground through R <sub>PROT</sub> resistor	With DIAG_EN unused, the analog sense, open-load, and short-to-supply diagnostics are not available.

**Table 5-2. Connections for Optional Pins (continued)**

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
OL_ON	Ground through R <sub>PROT</sub> resistor	With OL_ON unused, the high accuracy sense mode is not available.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Continuous supply voltage, $V_S$ with respect to IC GND: Version A, B	-0.7	64	V
Continuous supply voltage, $V_{OUT}$ with respect to IC GND: Version A, B	-60	64	V
Transient (< 100 us) voltage at the supply pin, $V_S$ with respect to IC GND: Version A, B	-0.7	81	V
Continuous supply voltage, $V_S$ with respect to IC GND: Version C, D, E	-0.7	83	V
Continuous supply voltage, $V_{OUT}$ with respect to IC GND: Version C, D, E	-60	83	V
Continuous voltage across the VS and VOUT pins ( $V_S - V_{OUT}$ ): Version C, D, E	-0.7	83	V
Enable pin voltage, $V_{EN}$	-1	6	V
OL_ON pin voltage, $V_{OL\_ON}$	-1	6	V
DIAG_EN pin voltage, $V_{DIAG\_EN}$	-1	6	V
Sense pin voltage, $V_{SNS}$	-1	6	V
FAULT pin voltage, $V_{FAULT}$	-1	6	V
Reverse ground current, $I_{GND}$	$V_S < 0\text{ V}$		-50 mA
Maximum junction temperature, $T_J$		150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{ESD}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	All pins except VS and VOUT	±2000 V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	VS and VOUT with respect to GND	±4000 V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	All pins	±750 V
$V_{(ESD4)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2 <sup>(4)</sup>	VS and VOUT	±8000 V
$V_{(EFT)}$	Electrostatic discharge	Electrical fast transient, per IEC 61000-4-4, version E <sup>(3)</sup>	VS and VOUT	±2500 V
$V_{(surge)}$	Electrostatic discharge	Surge protection with 42 $\Omega$ , per IEC 61000-4-5; 1.2/50 $\mu\text{s}$ <sup>(4)</sup>	VS and VOUT	±1000 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.  
(3) Tested with application circuit and supply voltage ( $V_S$ ) of 24-V, ENx pins High (Output Enabled) and and EN pins Low (Outputs Disabled). 2.5kV is rated for 100pF coupling capacitor, 10nF output capacitor at the output. The max EFT voltage level will change with different coupling capacitor and output capacitor used.  
(4) Tested with application circuit and supply voltage ( $V_S$ ) of 24-V, ENx pins High (Output Enabled) and and EN pins Low (Outputs Disabled)

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
$V_{S\_OP\_NOM}$	Nominal supply voltage <sup>(1)</sup>	6.0	36	V
$V_{S\_OP\_MAX}$	Extended operating voltage <sup>(2)</sup>	6.0	48	V
$V_{EN}$	Enable voltage	-1	5.5	V
$V_{OL\_ON}$	OL_ON pin voltage, $V_{OL\_ON}$	-1	5.5	V

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DIAG_EN</sub>	Diagnostic Enable voltage	-1	5.5	V
V <sub>FAULT</sub>	FAULT pin voltage	-1	5.5	V
V <sub>SNS</sub>	Sense voltage	-1	5.5	V
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

- (1) All operating voltage conditions are measured with respect to device GND  
(2) Device will function within extended operating range, however some parametric values might not apply

## 6.4 Thermal Information

THERMAL METRIC <sup>(1) (2)</sup>		TPS281C30x		UNIT
		RGW (QFN)	PWP (HTSSOP)	
		20 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	28.9	31.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	19.7	23.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	7.5	7.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	0.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	7.5	7.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	0.8	1.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [SPRA953](#) application report.  
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

## 6.5 Electrical Characteristics

V<sub>S</sub> = 6 V to 36 V, T<sub>A</sub> = -40°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
<b>VS SUPPLY VOLTAGE AND CURRENT</b>							
I <sub>L,NOM</sub>	Continuous load current	V <sub>EN</sub> = HI	T <sub>AMB</sub> = 85°C		6	A	
I <sub>STBY, VS</sub>	Total device standby current (including MOSFET) with diagnostics disabled (Ver. A, B, C, D)	V <sub>S</sub> ≤ 36 V, V <sub>EN</sub> = V <sub>DIAG_EN</sub> = LO, V <sub>OUT</sub> = 0 V	T <sub>J</sub> = -40°C to 85°C		0.25	0.7	μA
			T <sub>J</sub> = 150°C		0.63	6	μA
I <sub>STBY, VS_DIAG</sub>	V <sub>S</sub> standby current with diagnostics enabled (Ver. A, B, C, D)	V <sub>S</sub> ≤ 36 V, V <sub>EN</sub> = LO, V <sub>DIAG_EN</sub> = HI, V <sub>OUT</sub> = 0 V		1.2	1.5	mA	
I <sub>Q(OFF), VS</sub>	V <sub>S</sub> quiescent during OFF state (Ver. E)	V <sub>S</sub> ≤ 60 V, V <sub>EN</sub> = 0 V, V <sub>OUT</sub> = 24V, V <sub>DIAG</sub> = 0V	T <sub>J</sub> = -40°C to 85°C		0.95		mA
			T <sub>J</sub> = 125°C		0.98		mA
I <sub>Q, VS</sub>	V <sub>S</sub> quiescent current with diagnostics disabled	V <sub>EN</sub> = HI, V <sub>DIAG_EN</sub> = LO	I <sub>OUT</sub> = 0A		0.98	1.3	mA
I <sub>Q, VS_DIAG</sub>	V <sub>S</sub> quiescent current with diagnostics enabled	V <sub>ENx</sub> = HI, V <sub>DIAG_EN</sub> = HI	I <sub>OUT</sub> = 0A		1.0	1.5	mA
t <sub>STBY</sub>	Standby mode delay time (Ver. A, B, C, D)	V <sub>EN</sub> = V <sub>DIAG_EN</sub> = 0 V to standby		20		ms	
I <sub>OUT(OFF)</sub>	Output leakage current (Ver. A, B, C, D)	V <sub>S</sub> ≤ 36 V, V <sub>EN</sub> = V <sub>DIAG_EN</sub> = 0 V, V <sub>OUT</sub> = 0 V	T <sub>J</sub> = 85°C		0.4		μA
			T <sub>J</sub> = 125°C		0.5		6

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 $V_S = 6\text{ V to }36\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{OUT(OFF)}$	Output leakage current (Ver. E)	$V_S \leq 36\text{ V}$ , $V_{EN} = V_{DIAG\_EN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$	$T_J = -40^\circ\text{C to }85^\circ\text{C}$			28	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$			28	$\mu\text{A}$
		$V_S \leq 36\text{ V}$ , $V_{EN} = V_{DIAG\_EN} = 0\text{ V}$ , $V_{OUT} = 10\text{ V}$	$T_J = -40^\circ\text{C to }85^\circ\text{C}$	-6		9	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$	-10		10	$\mu\text{A}$
$t_{EFT\_DELAY}$	Delay for EFT protection after device turnoff (Ver. E)	$V_S \leq 60\text{ V}$ , $V_{EN} = 0\text{ V}$ , $V_{OUT}$ floating, $V_{DIAG} = 0\text{ V}$	$T_J = -40^\circ\text{C to }125^\circ\text{C}$			270	$\mu\text{s}$
<b>VS UNDERVOLTAGE LOCKOUT (UVLO) INPUT</b>							
$V_{S,UVLOR}$	$V_S$ undervoltage lockout rising	Measured with respect to the GND pin of the device		5.0	5.4	5.75	V
$V_{S,UVLOF}$	$V_S$ undervoltage lockout falling	Measured with respect to the GND pin of the device		4.1	4.5	4.85	V
<b>VS OVERVOLTAGE LOCKOUT (OVLO) INPUT</b>							
$V_{S,OVPR}$	$V_S$ overvoltage protection rising (Ver. A, B, C, D)	Measured with respect to the GND pin of the device, $V_{EN} = 5\text{ V}$		51	54	57	V
	$V_S$ overvoltage protection rising (Ver. E)	Measured with respect to the GND pin of the device, $V_{EN} = 5\text{ V}$		50	54	57	V
$V_{S,OVPR}$	$V_S$ overvoltage protection recovery falling	Measured with respect to the GND pin of the device, $V_{EN} = 5\text{ V}$		49	52	56	V
$V_{S,OVPH}$	$V_S$ overvoltage protection threshold hysteresis	Measured with respect to the GND pin of the device, $V_{EN} = 5\text{ V}$			1.5		V
$t_{VS,OVPR}$	$V_S$ overvoltage protection deglitch time	Time from triggering the OVP fault to FET turn-off			110	160	$\mu\text{s}$
<b>VDS CLAMP</b>							
$V_{DS,Clamp}$	$V_{DS}$ clamp voltage	Version A, B FET current = 10 mA	$V_S = 24\text{ V}$	65	72.5	80	V
			$V_S = 6\text{ V}$	48	53	58	V
<b>RON CHARACTERISTICS</b>							
$R_{ON}$	VS to VOUT On-resistance	Version B, D, E = $0.5\text{ A} \leq I_{OUT} \leq 6\text{ A}$ , A, C = $0.5\text{ A} \leq I_{OUT} \leq 3\text{ A}$ $V_S = 24\text{ V}$	$T_J = 25^\circ\text{C}$		29		$\text{m}\Omega$
			$T_J = 125^\circ\text{C}$			55	$\text{m}\Omega$
$R_{ON(REV)}$	On-resistance during reverse polarity	Version B, D, E = $0.5\text{ A} \leq I_{OUT} \leq 6\text{ A}$ , A, C = $0.5\text{ A} \leq I_{OUT} \leq 3\text{ A}$ $V_S = -24\text{ V}$	$T_J = -40^\circ\text{C to }125^\circ\text{C}$		30	60	$\text{m}\Omega$
$R_{ON\_AUXFE T}$	VS to VOUT On-resistance High Accuracy Sense Mode	$V_S = 24\text{ V}$ , $I_{OUT} = 40\text{ mA}$ $OL\_ON=DIAG\_EN=5\text{ V}$	$T_J = -40^\circ\text{C to }125^\circ\text{C}$		5.2	12	$\Omega$
<b>CURRENT LIMIT CHARACTERISTICS</b>							
$K_{CL}$	Current Limit Ratio	Device Version A, C	$R_{ILIM} = 10\text{ k}\Omega$ to $50\text{ k}\Omega$	40	50	60	A * $\text{k}\Omega$
		Device Version B, D, E	$R_{ILIM} = 10\text{ k}\Omega$ to $50\text{ k}\Omega$	80	100	120	A * $\text{k}\Omega$
$I_{LIM\_STARTUP}$	Peak current prior to regulation when switch is enabled	Device Version A, C	$R_{ILIM} = 10\text{ k}\Omega$ to $50\text{ k}\Omega$		$2 \times I_{CL}$	6.5	A
		Device Version B, D, E	$R_{ILIM} = 10\text{ k}\Omega$ to $50\text{ k}\Omega$		$2 \times I_{CL}$	14	A
$t_{LIM\_STARTUP\_DELAY}$	Peak current delay time prior to regulation when switch is enabled			7		12	ms



$V_S = 6\text{ V to }36\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CL}$	Current Limit level	Device Version A, C Short circuit condition	$R_{ILIM} = 50\text{ k}\Omega$	0.8	1	1.2	A
			$R_{ILIM} = 25\text{ k}\Omega$	1.8	2	2.2	A
			$R_{ILIM} = 16.7\text{ k}\Omega$	2.7	3	3.3	A
			$R_{ILIM} = 12.5\text{ k}\Omega$	3.6	4	4.4	A
			$R_{ILIM} = 10\text{ k}\Omega$	4.5	5	5.5	A
			$R_{ILIM} = \text{GND, open, or out of range} (<9\text{ k}\Omega, \text{ and } >100\text{ k}\Omega)$		0.5	0.8	A
$I_{CL}$	Current Limit level	Device Version B, D Short circuit condition	$R_{ILIM} = 50\text{ k}\Omega$	1.85	2	2.5	A
			$R_{ILIM} = 25\text{ k}\Omega$	3.7	4	4.6	A
			$R_{ILIM} = 16.7\text{ k}\Omega$	5.6	6	6.6	A
			$R_{ILIM} = 12.5\text{ k}\Omega$	7.2	8	8.8	A
			$R_{ILIM} = 10\text{ k}\Omega$	9	10	11	A
			$R_{ILIM} = \text{GND, open, or out of range} (<9\text{ k}\Omega, \text{ and } >100\text{ k}\Omega)$	0.2	0.5	1	A
$I_{CL}$	Current Limit level	Device Version E Short circuit condition	$R_{ILIM} = 50\text{ k}\Omega$	1.7	2	2.3	A
			$R_{ILIM} = 25\text{ k}\Omega$	3.6	4	4.4	A
			$R_{ILIM} = 16.7\text{ k}\Omega$	5.4	6	6.6	A
			$R_{ILIM} = 12.5\text{ k}\Omega$	7.1	8	8.9	A
			$R_{ILIM} = 10\text{ k}\Omega$	8.8	10	11.2	A
			$R_{ILIM} = \text{GND, open, or out of range} (<9\text{ k}\Omega, \text{ and } >100\text{ k}\Omega)$	0.3	0.5	0.8	A
$I_{CL\_LINPK}$	Overcurrent Limit Threshold <sup>(1)</sup>	Overload condition	$R_{ILIM} = 10\text{ k}\Omega \text{ to } 50\text{ k}\Omega$			$1.3 \times I_{CL}$	A
$I_{ILIM\_ENPS}$	Peak current enabling into permanent short		$R_{ILIM} = 10\text{ k}\Omega$			$2 \times I_{CL}$	A
$I_{ILIM\_ENPS2}$	Peak current enabling into permanent short		$R_{ILIM} = 10\text{ k}\Omega$ , $t < I_{LIM\_STARTUP\_DELAY}$			$I_{LIM\_STARTUP}$	A
$V_{ILIM\_OVP}$	$I_{LIM}$ Switchover threshold during overvoltage		Rising	37	40	43	V
			Hysteresis		2		V
$I_{ILIM\_OVP}$	$I_{LIM}$ Current Limit threshold during overvoltage	Overload condition	$R_{ILIM} = X$ , $V_{VS} \geq V_{ILIM\_OVP}$	0	0.552	1.5	A
$t_{IOS}$	Short circuit response time	$V_S = 24\text{ V}$			0.5		$\mu\text{s}$
$I_{ILIM\_OVERVOLTAGE}$	$I_{LIM}$ Current Limitation threshold during overvoltage	Overload condition when $V_S > 36\text{ V}$ <sup>(1)</sup>	$R_{ILIM} = X$ , $48\text{ V} \geq V_{VS} \geq 36\text{ V}$			5.25	A
<b>THERMAL SHUTDOWN CHARACTERISTICS</b>							
$T_{ABS}$	Thermal shutdown			175	185	195	$^\circ\text{C}$
$T_{REL}$	Relative thermal shutdown				77		$^\circ\text{C}$
$t_{RETRY}$	Retry time	Time from fault shutdown until switch re-enable (thermal shutdown).		1.4	2.1	3	ms
Fault Response	Fault response to Thermal Shutdown			Auto-retry			
$T_{HYS}$	Absolute Thermal shutdown hysteresis				10		$^\circ\text{C}$
<b>FAULT PIN CHARACTERISTICS</b>							

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 $V_S = 6\text{ V to }36\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CL\_FAULT\_R}$ (2)	$I_{CL}$ Current Limit Fault Assertion Threshold (Ver. A, B, C, D)	$V_{DIAG\_EN} = 5\text{ V}$ , $V_{OL\_ON} = 0\text{ V}$	Rising	$0.90 \times I_{CL}$	$0.95 \times I_{CL}$		A
	$I_{CL}$ Current Limit Fault Assertion Threshold (Ver. E)	$V_{DIAG\_EN} = 5\text{ V}$ , $V_{OL\_ON} = 0\text{ V}$	Rising	$0.77 \times I_{CL}$	$0.92 \times I_{CL}$		A
$I_{CL\_FAULT\_F}$ (2)	$I_{CL}$ Fault De-Assertion Threshold (Ver. A, B, C, D)	$V_{DIAG\_EN} = 5\text{ V}$ , $V_{OL\_ON} = 0\text{ V}$	Falling	$0.85 \times I_{CL}$	$0.90 \times I_{CL}$		A
	$I_{CL}$ Fault De-Assertion Threshold (Ver. E)	$V_{DIAG\_EN} = 5\text{ V}$ , $V_{OL\_ON} = 0\text{ V}$	Falling	$0.72 \times I_{CL}$	$0.86 \times I_{CL}$		A
$V_{FAULT}$	FAULT low output voltage	$I_{FAULT} = 2.5\text{ mA}$				0.5	V
$t_{FAULT\_BLANKING}$	Fault blanking time during startup		$V_{DIAG\_EN} = 5\text{ V}$ , $V_{EN} = 0\text{ to }5\text{ V}$			12	ms
$t_{FAULT\_FLT}$	Fault indication-time	Time between fault and FAULT asserting				75	$\mu\text{s}$
$t_{FAULT\_SNS}$	Fault indication-time (Ver. A, B, C, D)	$V_{DIAG\_EN} = 5\text{ V}$ Time between fault and $I_{SNS}$ settling at $V_{SNSFH}$	$V_{DIAG\_EN} = 5\text{ V}$ Time between fault and $I_{SNS}$ settling at $V_{SNSFH}$			95	$\mu\text{s}$
	Fault indication-time (Ver. E)	$V_{DIAG\_EN} = 5\text{ V}$ Time between fault and $I_{SNS}$ settling at $V_{SNSFH}$	$V_{DIAG\_EN} = 5\text{ V}$ Time between fault and $I_{SNS}$ settling at $V_{SNSFH}$			98	$\mu\text{s}$
<b>CURRENT SENSE CHARACTERISTICS</b>							
$I_{KSNS2\_EN}$	Load current supported to enable KSNS2 when in KSNS1 Mode (Ver. A, B, C, D)	$V_{EN} = V_{DIAG\_EN} = 5\text{ V}$ , $V_{OL\_ON} = \text{GND}$		42	50	70	mA
	Load current supported to enable KSNS2 when in KSNS1 Mode (Ver. E)	$V_{EN} = V_{DIAG\_EN} = 5\text{ V}$ , $V_{OL\_ON} = \text{GND}$		39	50	70	mA
$I_{KSNS2\_DIS}$	Load current to disable KSNS2 when in KSNS2 Mode (Ver. A, B, C, D)	$V_{EN} = V_{DIAG\_EN} = 5\text{ V}$ , $V_{OL\_ON} = \text{GND}$		75	85	105	mA
	Load current to disable KSNS2 when in KSNS2 Mode (Ver. E)	$V_{EN} = V_{DIAG\_EN} = 5\text{ V}$ , $V_{OL\_ON} = \text{GND}$		74	85	96	mA
$K_{SNS}$	Current sense ratio - Standard Sensing $I_{OUT} / I_{SNS}$	$I_{OUT} = 2\text{ A}$ , $V_{OL\_ON} = \text{GND}$			1300		A/A
$K_{SNS2}$	Current sense ratio - High Accuracy Sensing $I_{OUT} / I_{SNS}$	$I_{OUT} = 30\text{ mA}$ , $V_{OL\_ON} = 5\text{ V}$			24.6		A/A

$V_S = 6\text{ V to }36\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$I_{\text{SNS}}$	Current sense current and accuracy	$V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ , $V_{\text{OL\_ON}} = \text{GND}$	$I_{\text{OUT}} = 7\text{ A}$		5.38		mA	
					-6		6	%
			$I_{\text{OUT}} = 6\text{ A}$		4.61		6	mA
					-6		6	%
			$I_{\text{OUT}} = 4\text{ A}$		3.0		4	mA
					-4		4	%
			$I_{\text{OUT}} = 2\text{ A}$		1.533		4	mA
					-4		4	%
			$I_{\text{OUT}} = 1\text{ A}$		0.764		4	mA
					-4		4	%
$I_{\text{SNS2}}$	Current sense current and accuracy for high accuracy sense mode	$V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ , $V_{\text{OL\_ON}} = 5\text{ V}$	$I_{\text{OUT}} = 40\text{ mA}$		1.62		mA	
					-6		6	%
			$I_{\text{OUT}} = 20\text{ mA}$		0.833		6	mA
					-6		6	%
			$I_{\text{OUT}} = 10\text{ mA}$		0.404		10	mA
		-10		10	%			
$I_{\text{SNS2}}$	Current sense current and accuracy for high accuracy sense mode	$V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ , $V_{\text{OL\_ON}} = 5\text{ V}$	$I_{\text{OUT}} = 4\text{ mA}$		0.161		mA	
					-12.5		12.5	%
			$I_{\text{OUT}} = 2\text{ mA}$		0.0800		15	mA
					-15		15	%
$I_{\text{SNS2}}$	Current sense current and accuracy for high accuracy sense mode	$V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ , $V_{\text{OL\_ON}} = 5\text{ V}$	$I_{\text{OUT}} = 1\text{ mA}$		0.0395		mA	
					-20		20	%

**SNS PIN CHARACTERISTICS**

$V_{\text{SNSFH}}$	$V_{\text{SNS}}$ fault high-level	$V_{\text{DIAG\_EN}} = 5\text{ V}$		4.5	5	5.77	V
		$V_{\text{DIAG\_EN}} = 3.3\text{ V}$ , $R_{\text{SNS}} = \text{Open}$		3.5	3.95	4.4	V
		$V_{\text{DIAG\_EN}} = V_{\text{IH}}$		2.8	3.66	3.8	V
$I_{\text{SNSFLT}}$	$I_{\text{SNS}}$ fault high-level	$V_{\text{DIAG\_EN}} > V_{\text{IH,DIAG\_EN}}$		5.8	6.4		mA
$I_{\text{SNSFLT}}$	$I_{\text{SNS}}$ fault high-level (Ver. E)	$V_{\text{DIAG\_EN}} > V_{\text{IH,DIAG\_EN}}$	$V_{\text{DIAG\_EN}} > V_{\text{IH,DIAG\_EN}}$	5.3	6.4		mA
$I_{\text{SNSleak}}$	$I_{\text{SNS}}$ leakage	$V_{\text{DIAG\_EN}} = 5\text{ V}$ , $I_{\text{L}} = 0\text{ mA}$				1.3	$\mu\text{A}$
$V_{\text{S\_SNS}}$	$V_{\text{S}}$ headroom needed for full current sense and fault functionality (Ver. A, B, C, D)	$V_{\text{DIAG\_EN}} = 3.3\text{ V}$		5.8			V
	$V_{\text{S}}$ headroom needed for full current sense and fault functionality	$V_{\text{DIAG\_EN}} = 5\text{ V}$		6.5			V
$V_{\text{S\_SNS}}$	$V_{\text{S}}$ headroom needed for full current sense and fault functionality (Ver. E)	$V_{\text{DIAG\_EN}} = 3.3\text{ V}$		6			V

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 $V_S = 6\text{ V to }36\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OPEN LOAD DETECTION CHARACTERISTICS</b>						
$V_{OL\_OFF}$	OFF state open-load (OL) detection voltage	$V_{EN} = 0\text{ V}$ , $V_{DIAG\_EN} = 5\text{ V}$	1.5	2	2.5	V
$R_{OL\_OFF}$	OFF state open-load (OL) detection internal pull-up resistor	$V_{EN} = 0\text{ V}$ , $V_{DIAG\_EN} = 5\text{ V}$	120	150	180	k $\Omega$
$t_{OL\_OFF}$	OFF state open-load (OL) detection deglitch time	$V_{EN} = 0\text{ V}$ , $V_{DIAG\_EN} = 5\text{ V}$ , When $V_S - V_{OUT} < V_{OL}$ , duration longer than $t_{OL}$ . Open load detected.		480	700	$\mu\text{s}$
$t_{OL\_OFF\_1}$	OL_OFF and STB indication-time from EN falling	$V_{EN} = 5\text{ V to }0\text{ V}$ , $V_{DIAG\_EN} = 5\text{ V}$ $I_{OUT} = 0\text{ mA}$ , $V_{OUT} = V_S - V_{OL}$		310	700	$\mu\text{s}$
$t_{OL\_OFF\_2}$	OL and STB indication-time from DIA_EN rising	$V_{EN} = 0\text{ V}$ , $V_{DIAG\_EN} = 0\text{ V to }5\text{ V}$ $I_{OUT} = 0\text{ mA}$ , $V_{OUT} = V_S - V_{OL}$			700	$\mu\text{s}$
<b>OL_ON PIN CHARACTERISTICS</b>						
$V_{IL\_OL\_ON}$	Input voltage low-level				0.8	V
$V_{IH\_OL\_ON}$	Input voltage high-level		1.5			V
$V_{IHYS\_OL\_ON}$	Input voltage hysteresis			282		mV
$R_{OL\_ON}$	Internal pulldown resistor		0.7	1	1.3	M $\Omega$
$I_{IL\_OL\_ON}$	Input current low-level	$V_{OL\_ON} = -1\text{ V}$	-25		0	$\mu\text{A}$
$I_{IL\_OL\_ON}$	Input current low-level	$V_{OL\_ON} = 0.8\text{ V}$	0.6	0.8	1.2	$\mu\text{A}$
$I_{IH\_OL\_ON}$	Input current high-level	$V_{OL\_ON} = 5\text{ V}$	3	5	7	$\mu\text{A}$
<b>DIAG_EN PIN CHARACTERISTICS</b>						
$V_{IL\_DIAG\_EN}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH\_DIAG\_EN}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS\_DIAG\_EN}$	Input voltage hysteresis			270		mV
$R_{DIAG\_EN}$	Internal pulldown resistor		200	350	500	k $\Omega$
$I_{IL\_DIAG\_EN}$	Input current low-level (A, B, C, D version)	$V_{DIAG\_EN} = 0.8\text{ V}$ , $V_{EN}=0\text{V}$		0.8		$\mu\text{A}$
	Input current low-level (E version)	$V_{DIAG\_EN} = 0.8\text{ V}$ , $V_{EN}=0\text{V}$		2.9	3.8	$\mu\text{A}$
$I_{IH\_DIAG\_EN}$	Input current high-level	$V_{DIAG\_EN} = 5\text{ V}$		14		$\mu\text{A}$
<b>EN PIN CHARACTERISTICS</b>						
$V_{IL\_EN}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH\_EN}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS\_EN}$	Input voltage hysteresis			280		mV
$R_{EN}$	Internal pulldown resistor		200	350	500	k $\Omega$
$I_{IL\_EN}$	Input current low-level	$V_{EN} = 0.8\text{ V}$		2.2		$\mu\text{A}$
$I_{IH\_EN}$	Input current high-level	$V_{EN} = 5\text{ V}$		14		$\mu\text{A}$

- The maximum current output under overload condition before current limit regulation
- Not tested in production.

## 6.6 SNS Timing Characteristics

 $V_S = 6\text{ V to }36\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted). Parameters not tested in production.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SNS TIMING - CURRENT SENSE</b>					

$V_S = 6\text{ V to }36\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted). Parameters not tested in production.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{SNSION1}}$	Settling time from rising edge of DIAG_EN 50% of $V_{\text{DIAG\_EN}}$ to 90% of settled ISNS	$V_{\text{EN}} = 5\text{ V}$ , $V_{\text{DIAG\_EN}} = 0\text{ V to }5\text{ V}$ , $V_{\text{OL\_ON}} = 0\text{ V}$ , $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_L = 1\text{ A}$			15	$\mu\text{s}$
		$V_{\text{EN}} = 5\text{ V}$ , $V_{\text{DIAG\_EN}} = 0\text{ V to }5\text{ V}$ , $V_{\text{OL\_ON}} = 0\text{ V}$ , $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_L = 50\text{ mA}$			80	$\mu\text{s}$
$t_{\text{SNSION2}}$	Settling time from rising edge of EN and DIAG_EN 50% of $V_{\text{DIAG\_EN}}$ $V_{\text{EN}}$ to 90% of settled ISNS	$V_{\text{EN}} = V_{\text{DIAG\_EN}} = 0\text{ V to }5\text{ V}$ $V_S = 24\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_L = 1\text{ A}$			150	$\mu\text{s}$
$t_{\text{SNSION3}}$	Settling time from rising edge of EN 50% of $V_{\text{EN}}$ to 90% of settled ISNS	$V_{\text{EN}} = 0\text{ V to }5\text{ V}$ , $V_{\text{DIAG\_EN}} = 5\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_L = 1\text{ A}$			150	$\mu\text{s}$
$t_{\text{SNSION4}}$	Settling time from rising edge of OL_ON 50% of $V_{\text{OL\_ON}}$ to 90% of settled ISNS	$V_{\text{OL\_ON}} = 0\text{ to }5\text{ V}$ , $V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_L = 6\text{ mA}$			60	$\mu\text{s}$
$t_{\text{SNSION5}}$	Settling time from falling edge of $I_L <$ $I_{\text{KSNS2\_EN}}$ to 90% of settled ISNS	$V_{\text{OL\_ON}} = V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_L = 100\text{ mA to }10\text{ mA}$			60	$\mu\text{s}$
$t_{\text{SNSION6}}$	Settling time from Rising edge of $I_L >$ $I_{\text{KSNS2\_DIS}}$ to 90% of settled ISNS	$V_{\text{OL\_ON}} = V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_L = 10\text{ mA to }100\text{ mA}$			60	$\mu\text{s}$
$t_{\text{KSNS2\_DIS\_DGL}}$	Deglitch time for transition of $I_L >$ $I_{\text{KSNS2\_DIS}}$ .	$V_{\text{OL\_ON}} = V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_L = 10\text{ mA to }100\text{ mA}$			30	$\mu\text{s}$
$t_{\text{SNSIOFF}}$	Settling time from falling edge of DIAG_EN	$V_{\text{EN}} = 5\text{ V}$ , $V_{\text{DIAG\_EN}} = 5\text{ V to }0\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $R_L = 48\ \Omega$			20	$\mu\text{s}$
$t_{\text{SETTLEH}}$	Settling time from rising edge of load step to 90% of settled value of current sense output	$V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_{\text{OUT}} = 0.5\text{ A to }3\text{ A}$			20	$\mu\text{s}$
$t_{\text{SETTLEL}}$	Settling time from output edge of load step to 10% of settled value of current sense output	$V_{\text{EN}} = V_{\text{DIAG\_EN}} = 5\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_{\text{OUT}} = 3\text{ A to }0.5\text{ A}$			20	$\mu\text{s}$
$t_{\text{TIMEOUT}}$	Time to indicate VSNSFH due to VS- VOUT>2V. From rising edge of EN, DIAG_EN and OL_ON 50% of $V_{\text{DIA\_EN}}$ $V_{\text{EN}}$ $V_{\text{OL\_ON}}$ to 50% of rising edge of VSNSFH	$V_{\text{DIAG\_EN}} = V_{\text{EN}} = V_{\text{OL\_ON}} = 0\text{ V to }5\text{ V}$ $R_{\text{SNS}} = 1\text{ k}\Omega$ , $I_{\text{OUT}} = 5\text{ mA}$ $C_{\text{OUT}} = 50\mu\text{F}$		245		$\mu\text{s}$

## 6.7 Switching Characteristics

$V_S = 24\text{ V}$ ,  $T_J = -40^\circ\text{C to }+125^\circ\text{C}$  (unless otherwise noted),  $C_{\text{OUT}} = 22\text{ nF}$

Parameter		Test Conditions	Min	Typ	Max	Unit
$t_{\text{DR}}$	Turnon delay time (from standby, Ver. A, B, C, D)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 20% of VOUT		35	55	$\mu\text{s}$
	Turnon delay time (from delay or diagnostic, Ver. A, B, C, D)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 20% of VOUT		25	45	$\mu\text{s}$
	Turnon delay time (from delay or diagnostic, Ver. E)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 20% of VOUT		49	60	$\mu\text{s}$
$t_{\text{DF}}$	Turnoff delay time (Ver. A, B, C, D)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 80% of VOUT		35	50	$\mu\text{s}$
	Turnoff delay time (Ver. E)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 80% of VOUT		40	55	$\mu\text{s}$
$\text{SR}_R$	VOUT rising slew rate	$V_S = 24\text{ V}$ , 20% to 80% of $V_{\text{OUT}}$ , $R_L = 48\ \Omega$	0.4	0.7	0.95	$\text{V}/\mu\text{s}$
$\text{SR}_F$	VOUT falling slew rate	$V_S = 24\text{ V}$ , 80% to 20% of $V_{\text{OUT}}$ , $R_L = 48\ \Omega$	0.4	0.8	1.2	$\text{V}/\mu\text{s}$
$f_{\text{max}}$	Maximum PWM frequency				1	$\text{kHz}$

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 $V_S = 24\text{ V}$ ,  $T_J = -40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$  (unless otherwise noted),  $C_{OUT} = 22\text{ nF}$ 

Parameter		Test Conditions	Min	Typ	Max	Unit
$t_{ON}$	Turnon time (Ver. A, B, C, D)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 80% of VOUT		55	75	$\mu\text{s}$
	Turnon time (Ver. E)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 80% of VOUT		69	96	$\mu\text{s}$
$t_{OFF}$	Turnoff time (Ver. A, B, C, D)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 20% of VOUT		60	70	$\mu\text{s}$
	Turnoff time (Ver. E)	$V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ 50% of EN to 20% of VOUT		60	80	$\mu\text{s}$
$t_{ON} - t_{OFF}$	Turnon and off matching (Ver. A, B, C, D)	1ms ON time switch enable pulse $V_S = 24\text{ V}$ , $R_L = 48\ \Omega$	-25		45	$\mu\text{s}$
	Turnon and off matching (Ver. E)	100- $\mu\text{s}$ ON time switch enable pulse, $V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ , $F = f_{max}$	5		68	$\mu\text{s}$
$\Delta_{PWM}$	PWM accuracy - average load current	200- $\mu\text{s}$ enable pulse, $V_S = 24\text{ V}$ , $R_L = 48\ \Omega$ $F = f_{max}$	-15		15	%
$E_{ON}$	Switching energy losses during turnon	$V_S = 24\text{ V}$ , $R_L = 8\ \Omega$ , 1 ms pulse, VOUT from 20% to 80% of VS voltage		0.5		mJ
$E_{OFF}$	Switching energy losses during turnoff	$V_S = 24\text{ V}$ , $R_L = 8\ \Omega$ , 1 ms pulse, VOUT from 80% to 20% of VS voltage		0.25		mJ

## 6.8 Typical Characteristics

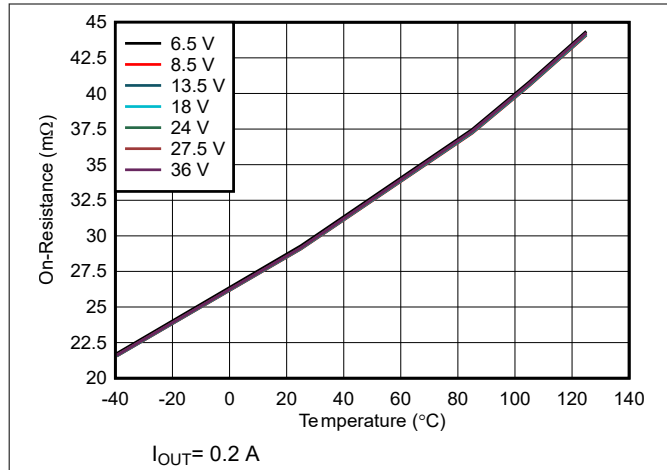


Figure 6-1. On-Resistance ( $R_{ON}$ ) vs Temperature vs VS Supply Voltage

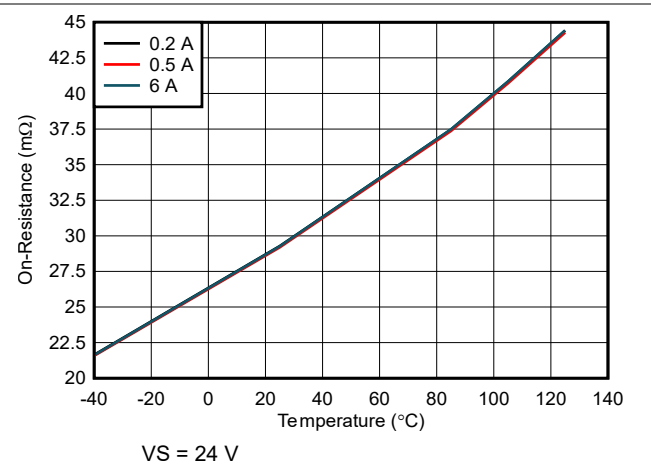


Figure 6-2. On-Resistance ( $R_{ON}$ ) vs Temperature vs Load Current

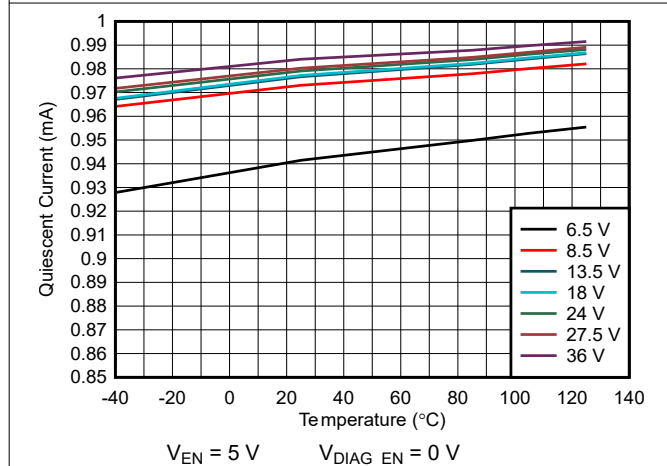


Figure 6-3. Quiescent Current ( $I_{Q, VS}$ ) From VS Input Supply vs Temperature vs VS Voltage

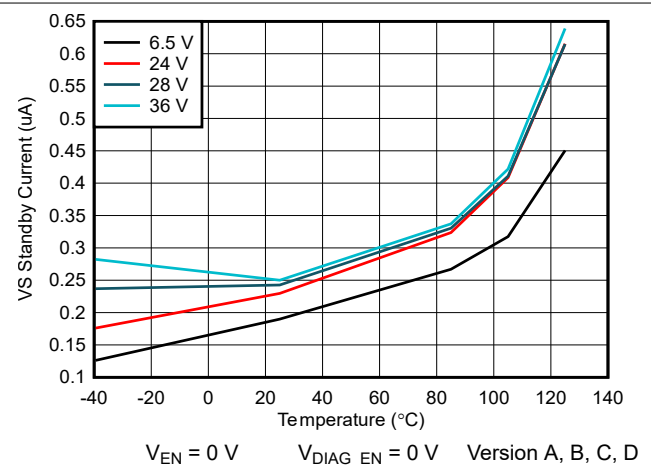


Figure 6-4. Standby Current ( $I_{STBY, VS}$ ) From VS Input Supply vs Temperature vs VS Voltage

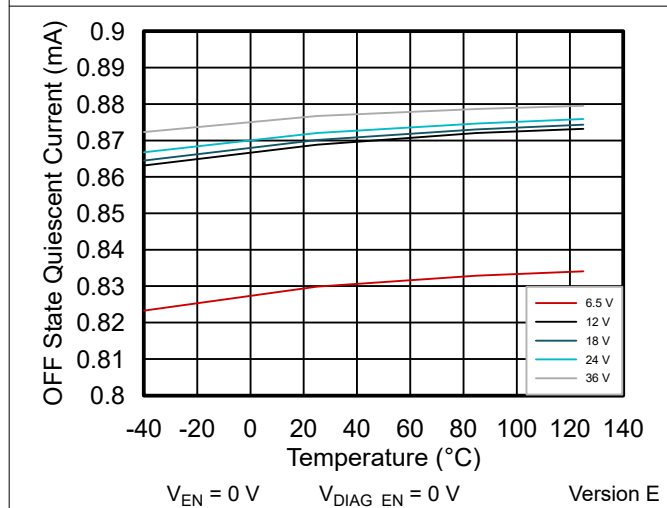


Figure 6-5. OFF State Quiescent Current ( $I_{Q(OFF)}$ ) From VS Input Supply vs Temperature vs VS Voltage

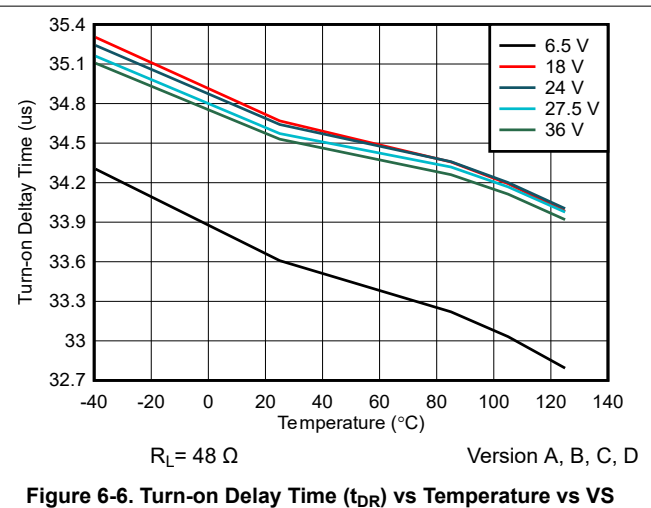


Figure 6-6. Turn-on Delay Time ( $t_{DR}$ ) vs Temperature vs VS Voltage

### 6.8 Typical Characteristics (continued)

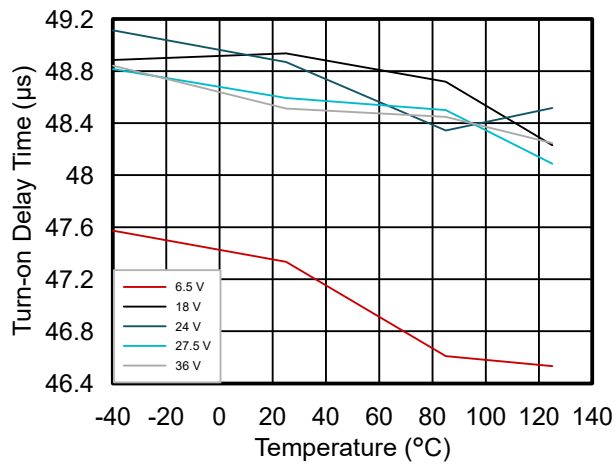


Figure 6-7. Turn-on Delay Time ( $t_{DR}$ ) vs Temperature vs VS Voltage

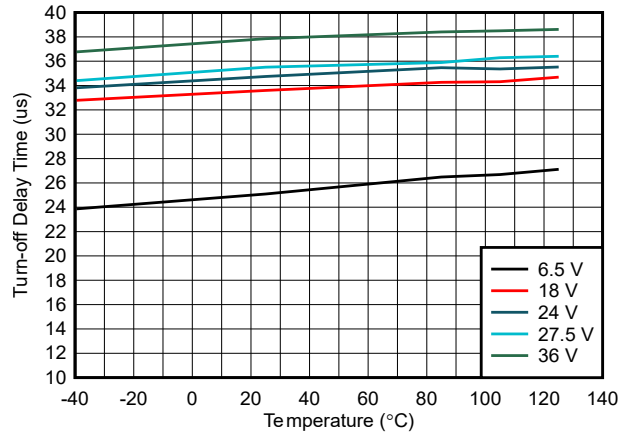


Figure 6-8. Turn-off Delay Time ( $t_{DF}$ ) vs Temperature vs VS Voltage

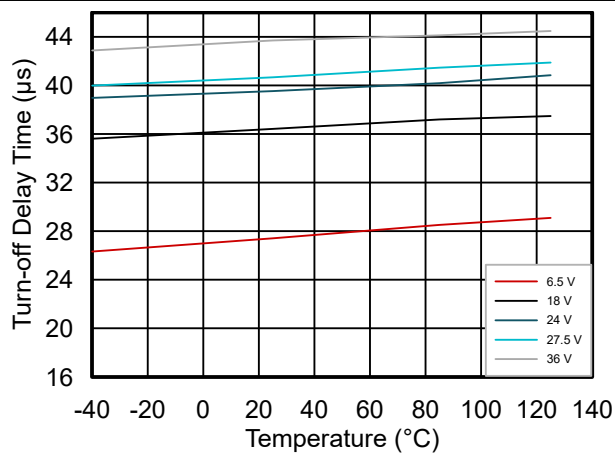


Figure 6-9. Turn-off Delay Time ( $t_{DF}$ ) vs Temperature vs VS Voltage

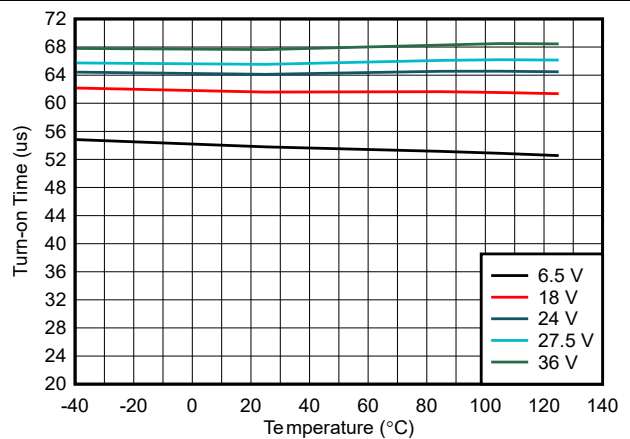


Figure 6-10. Turn-on Time ( $t_{ON}$ ) vs Temperature vs VS Voltage

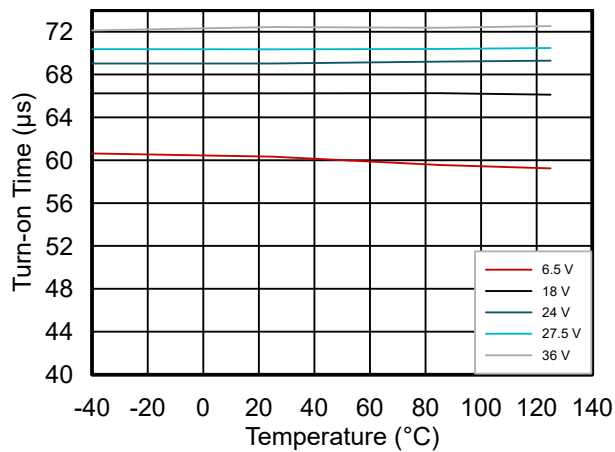


Figure 6-11. Turn-on Time ( $t_{ON}$ ) vs Temperature vs VS Voltage

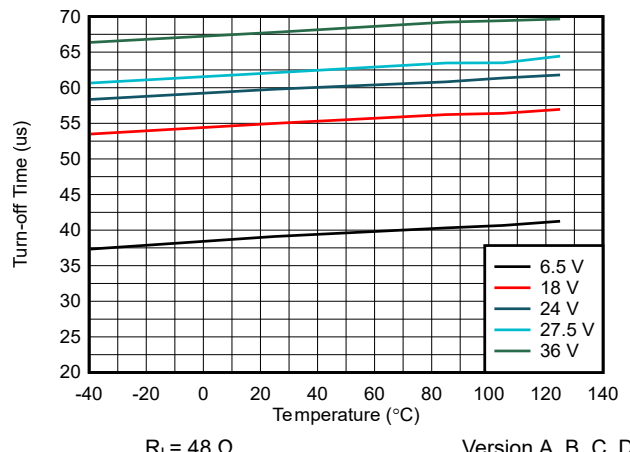


Figure 6-12. Turn-off Time ( $t_{OFF}$ ) vs Temperature vs VS Voltage



### 6.8 Typical Characteristics (continued)

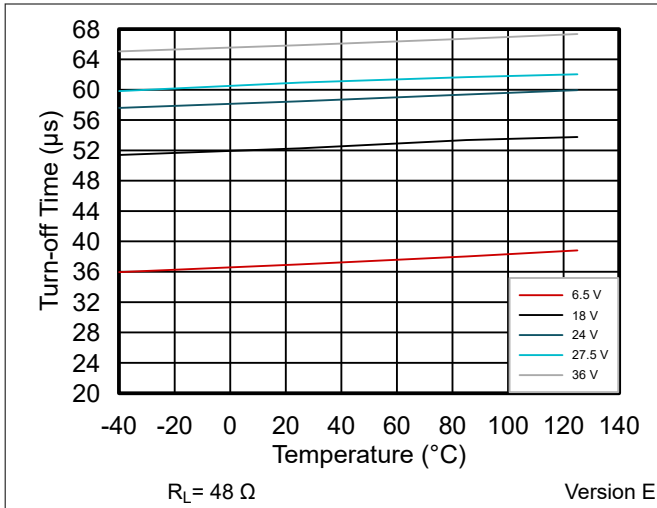


Figure 6-13. Turn-off Time ( $t_{OFF}$ ) vs Temperature vs VS Voltage

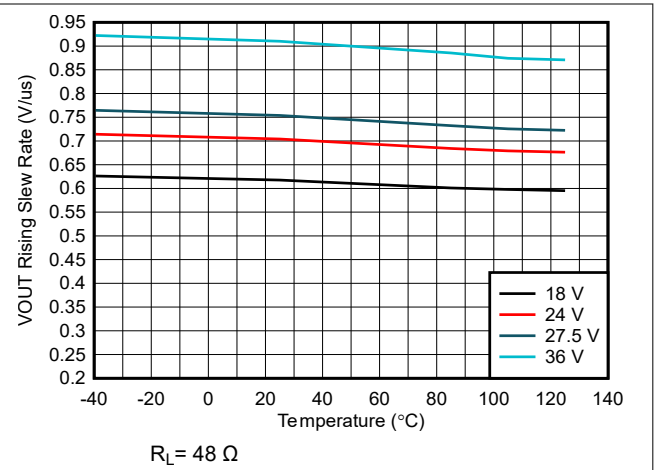


Figure 6-14. VOUT Rising Slew Rate ( $SR_R$ ) vs Temperature vs VS Voltage

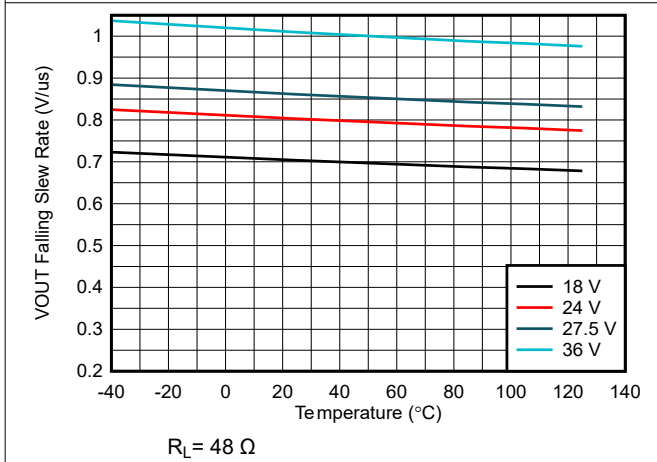


Figure 6-15. VOUT Falling Slew Rate ( $SR_F$ ) vs Temperature vs VS Voltage

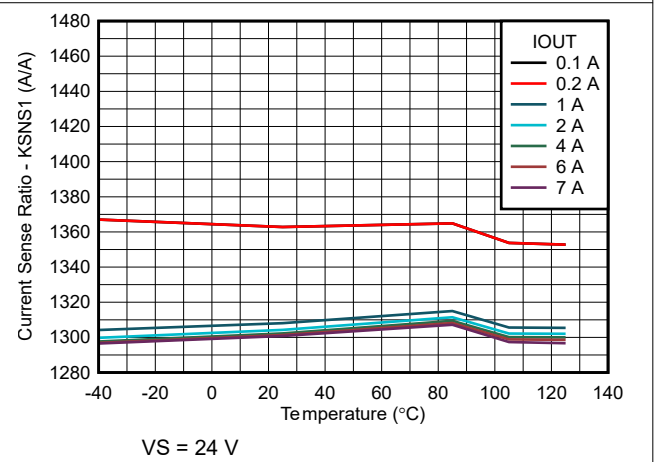


Figure 6-16. Current Sense Ratio ( $KSNS_1$ ) vs Temperature vs Load Current

### 6.8 Typical Characteristics (continued)

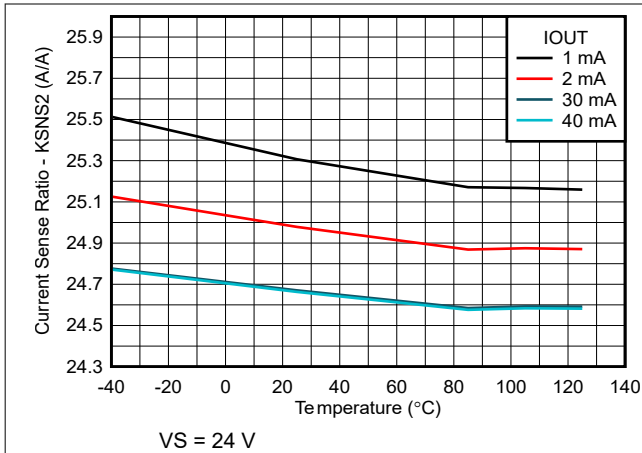


Figure 6-17. Current Sense Ratio ( $KSNS_2$ ) vs Temperature vs Load Current

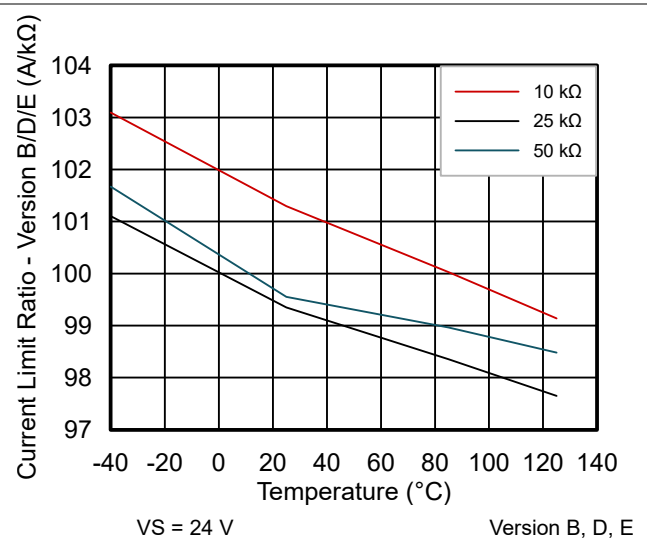
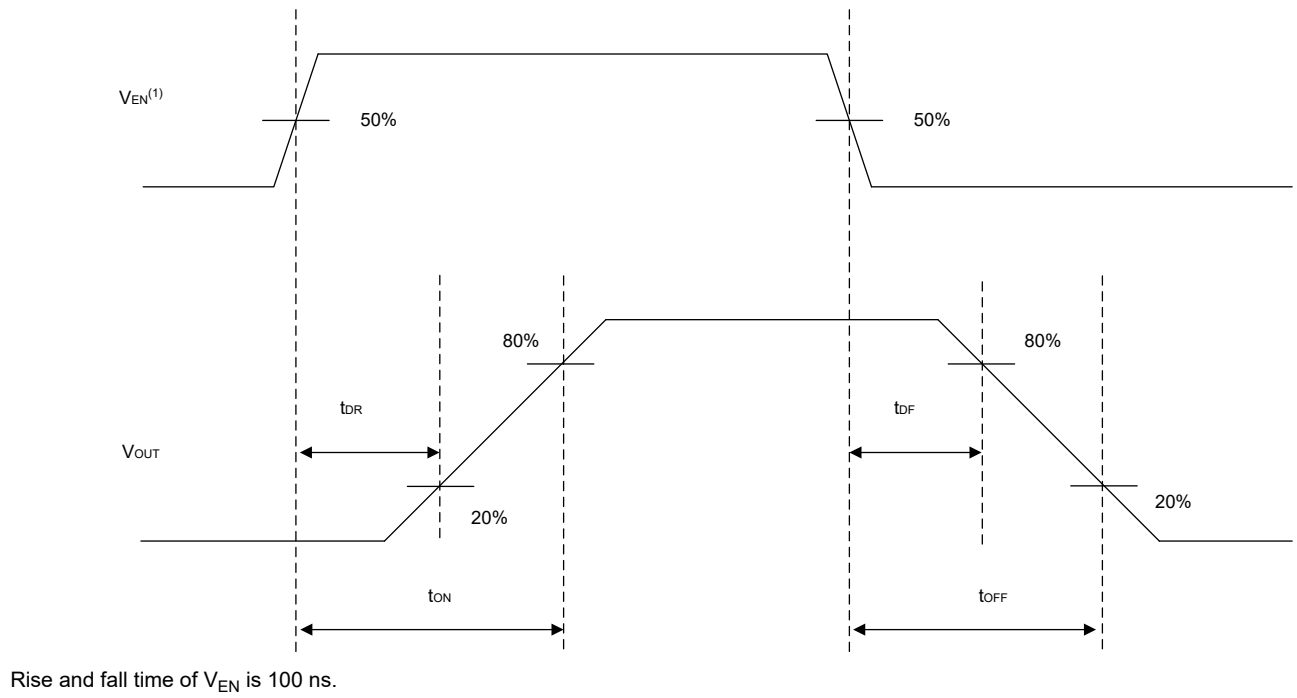
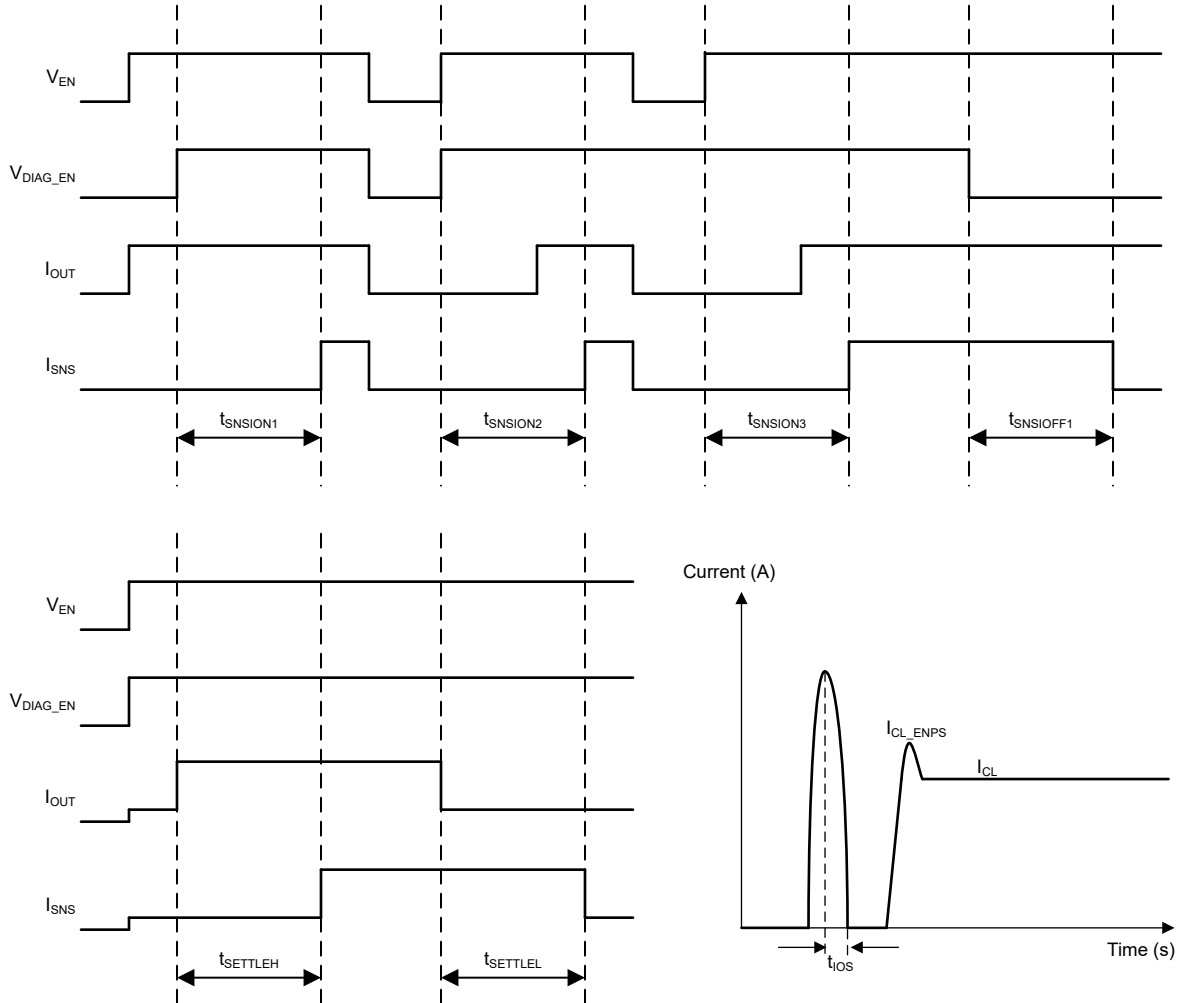


Figure 6-18. Current Limit Ratio ( $K_{CL}$ ) vs Temperature vs  $R_{ILIM}$

## 7 Parameter Measurement Information



**Figure 7-1. Switching Characteristics Definitions**



Rise and fall times of control signals are 100 ns. Control signals include: EN, DIAG\_EN.

**Figure 7-2. SNS Timing Characteristics Definitions**

## 8 Detailed Description

### 8.1 Overview

The TPS281C30 is a single-channel, fully-protected, high-side power switch with an integrated NMOS power FET and charge pump rated to 60V DC tolerance. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. Low logic high threshold,  $V_{IH}$ , of 1.5V on the input pins allow use of MCU's down to 1.8V. A programmable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two pins to support both digital status and analog current-sense output.

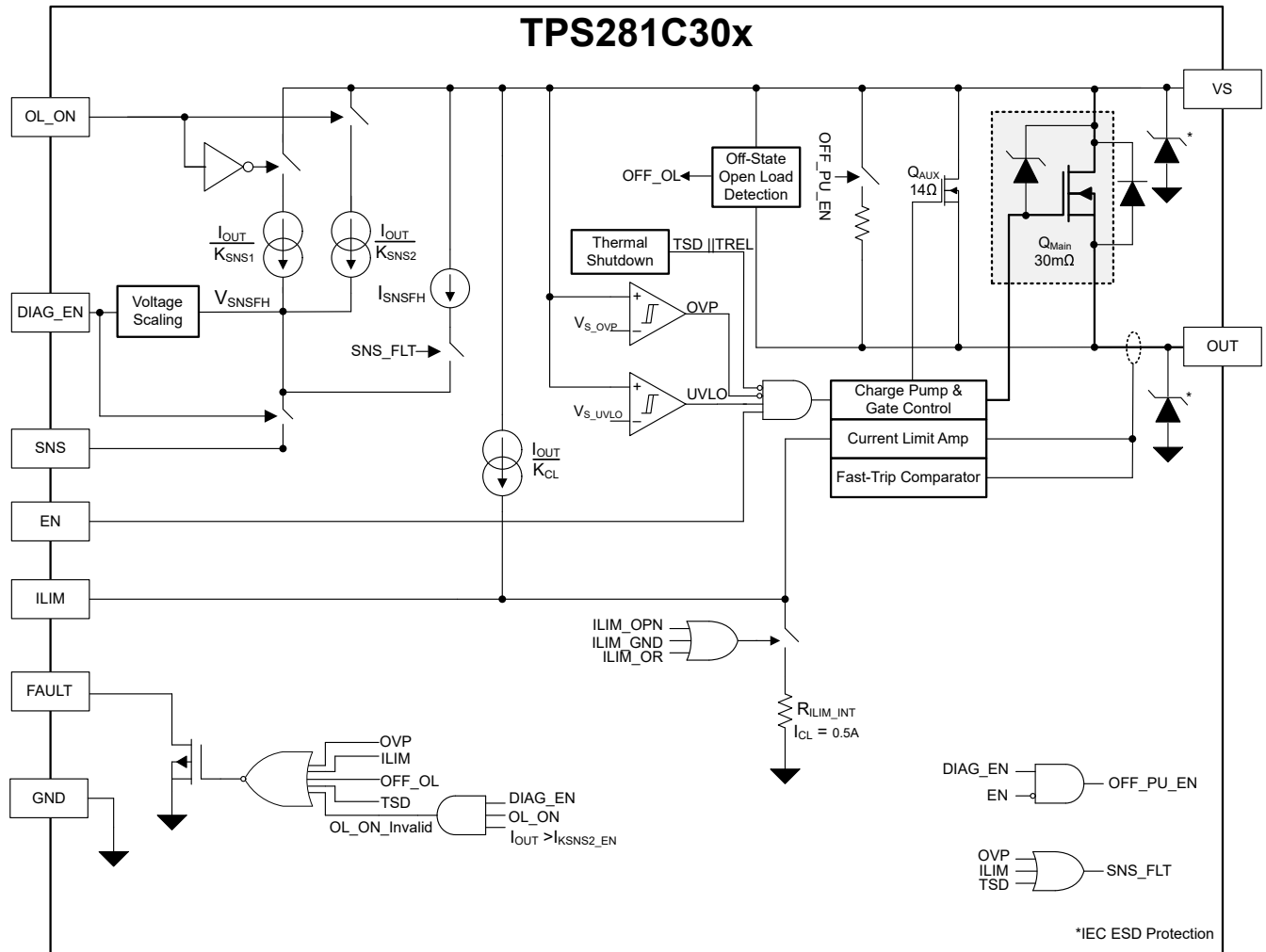
The digital status report is implemented with an open-drain structure on the fault pin. When a fault condition occurs, the pin is pulled down to GND. An external pullup is required to match the microcontroller supply level. High-accuracy current sensing allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source  $1 / K_{SNS}$  of the load current, which is reflected as voltage on the SNS pin.  $K_{SNS}$  is a constant value across temperature and supply voltage. The SNS pin can also report a fault by forcing a voltage of  $V_{SNSFH}$  that scales with the diagnostic enable voltage so that the max voltage seen by the system's ADC is within an acceptable value. This removes the need for an external zener diode or resistor divider on the SNS pin.

The external high-accuracy current limit allows setting the current limit value by application. It highly improves the reliability of the system by clamping the inrush current effectively under start-up or short-circuit conditions. Also, it can save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. An internal current limit can also be implemented in this device. The lower value of the external or internal current-limit value is applied.

An active drain to source voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. During the inductive switching-off cycle, both the energy of the power supply ( $E_{BAT}$ ) and the load ( $E_{LOAD}$ ) are dissipated on the high-side power switch itself. With the benefits of process technology and excellent IC layout, the TPS281C30x device can achieve excellent energy dissipation capacity, which can help save the external free-wheeling circuitry in most cases.

The TPS281C30x device can be used as a high-side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters. Please note that for driving inductive loads, versions without internal VDS clamp (Ver. C, D, E) would require an external clamp to dissipate the inductive energy at turn-off.

## 8.2 Functional Block Diagram

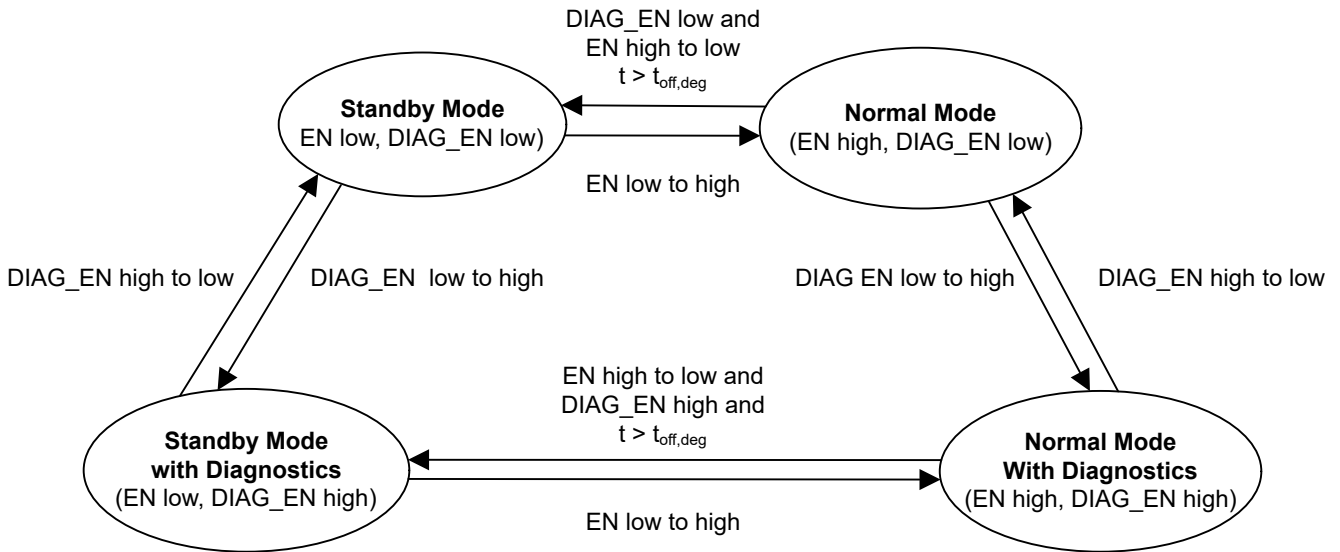


### 8.3 Device Functional Modes

#### 8.3.1 Working Mode

The four working modes in the device are normal mode, normal mode with diagnostics, standby mode, and standby mode with diagnostics. The standby mode and the standby mode with diagnostics are only available in version A, B, C, D. If an off-state power saving is required in the system, the standby current is less than 500 nA with EN and DIAG\_EN low. If an off-state diagnostic is required in the system, the typical standby current is around 0.5 mA with DIAG\_EN high. Note that to enter standby mode requires IN low and  $t > t_{STBY}$ .  $t_{STBY}$  is the standby-mode deglitch time, which is used to avoid false triggering or interfere with PWM switching.

For E version, there is no standby mode when the device is OFF, and the current consumption will be  $I_{Q(OFF)}$  when EN is low.



**Figure 8-1. Work-Mode State Machine**

## 8.4 Feature Description

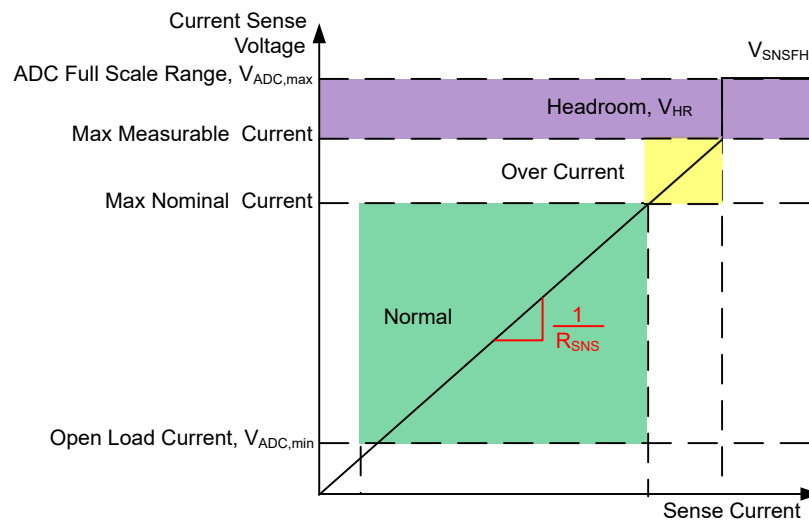
### 8.4.1 Accurate Current Sense

The current-sense function is internally implemented, which allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source  $1 / K_{\text{SNS}}$  of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

$K_{\text{SNS}}$  is the ratio of the output current and the sense current. The accuracy values of  $K_{\text{SNS}}$  quoted in the electrical characteristics do take into consideration temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases.

The maximum voltage out on the SNS pin is clamped to  $V_{\text{SNSFH}}$  which is the fault voltage level. In order to make sure that this voltage is not higher than the system can tolerate, TI has correlated the voltage coming in on the DIAG\_EN pin with the maximum voltage out on the SNS pin. If DIAG\_EN is between  $V_{\text{IH}}$  and 3.3 V, the maximum output on the SNS pin will be  $\sim 3.3$  V. However, if the voltage at DIAG\_EN is above 3.3 V, then the fault SNS voltage,  $V_{\text{SNSFH}}$ , will track that voltage up to 5 V. This is done because the GPIO voltage output that is powering the diagnostics through DIAG\_EN, will be close to the maximum acceptable ADC voltage within the same microcontroller. Therefore, the sense resistor value,  $R_{\text{SNS}}$ , can be chosen to maximize the range of currents needed to be measured by the system. The  $R_{\text{SNS}}$  value should be chosen based on application need. The maximum usable  $R_{\text{SNS}}$  value is bounded by the ADC minimum acceptable voltage,  $V_{\text{ADC,min}}$ , for the smallest load current needed to be measured by the system,  $I_{\text{LOAD,min}}$ . The minimum acceptable  $R_{\text{SNS}}$  value has to ensure the  $V_{\text{SNS}}$  voltage is below the  $V_{\text{SNSFH}}$  value so that the system can determine faults. This difference between the maximum readable current through the SNS pin,  $I_{\text{LOAD,max}} \times R_{\text{SNS}}$ , and the  $V_{\text{SNSFH}}$  is called the headroom voltage,  $V_{\text{HR}}$ . The headroom voltage is determined by the system but is important so that there is a difference between the maximum readable current and a fault condition. Therefore, the minimum  $R_{\text{SNS}}$  value has to be the  $V_{\text{SNSFH}}$  minus the  $V_{\text{HR}}$  times the sense current ratio,  $K_{\text{SNS}}$  divided by the maximum load current the system needs to measure,  $I_{\text{LOAD,max}}$ . This boundary equation can be seen in [Equation 1](#).

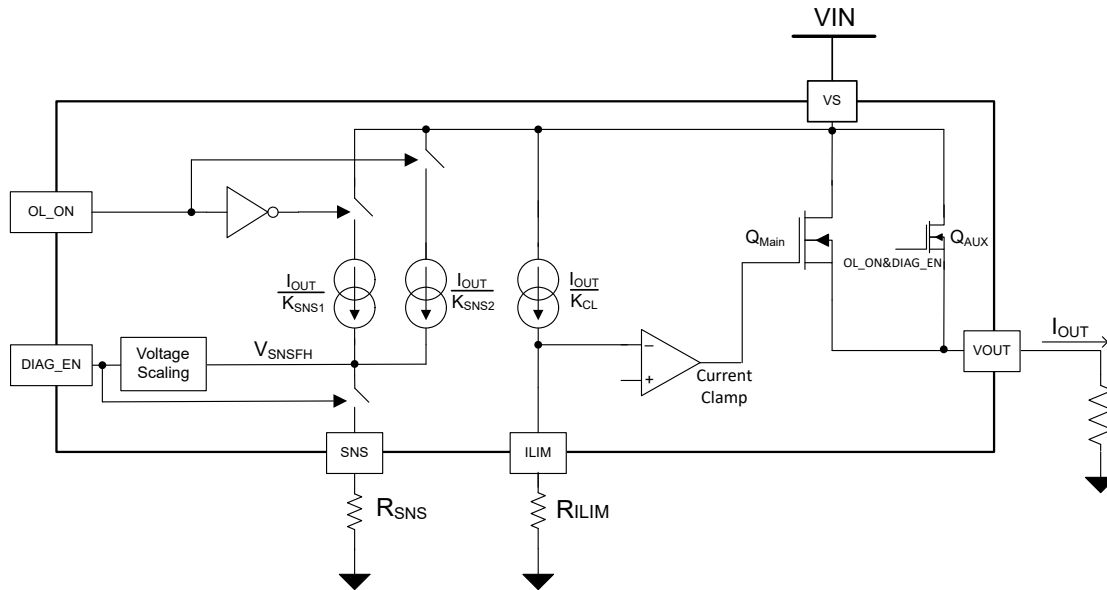
$$V_{\text{ADC,min}} \times K_{\text{SNS}} / I_{\text{LOAD,min}} \leq R_{\text{SNS}} \leq (V_{\text{SNSFH}} - V_{\text{HR}}) \times K_{\text{SNS}} / I_{\text{LOAD,max}} \quad (1)$$



**Figure 8-2. Voltage Indication on the Current-Sense Pin**

The maximum current the system wants to read,  $I_{\text{LOAD,max}}$ , needs to be below the current limit threshold because once the current limit threshold is tripped the  $V_{\text{SNS}}$  value will go to  $V_{\text{SNSFH}}$ . Additionally, currents being measured should be below 7 A to ensure that the current sense output is not saturated.





**Figure 8-3. Current-Sense and Current-Limit Block Diagram**

Since this scheme adapts based on the voltage coming in from the MCU. There is no need to have a zener diode on the SNS pin to protect from high voltages.

### 8.4.1.1 High Accuracy Sense Mode

In some applications, having accurate current sensing at lower load currents can be critical to distinguish between a real load and a fault scenario such as an open load condition(Wire-Break). To address this challenge, TPS281C30x implements a high accuracy sense mode that enables customers to achieve  $\pm 30\%$  @6mA load. This mode will be activated when diagnostics are enabled(DIAG\_EN=HI), OL\_ON = HI and  $I_{Load} < I_{Ksns2\_EN}$ . To achieve this high accuracy, the device increases its main path resistance to improve its sense accuracy while high accuracy sensing is active. TI recommends users to disable this accuracy sense mode by setting OL\_ON=LO if the load starts to increase beyond 40mA. This will proactively prevent any higher power dissipation states.

In other scenarios such as a sudden load step where the system might not be fast enough to react to the change in SNS output current. For this case, in order to prevent a high-power dissipation state given by the increased resistance. TPS281C30x senses the load flowing through the VS-VOUT path to remain  $< I_{Ksns2\_DIS}$ . If the load increases beyond  $I_{Ksns2\_DIS}$  the FET resistance will revert back to its lowest resistance and high accuracy sense mode will be disabled. This will result in nFAULT being asserted to signal that high accuracy sense mode has been disabled. This will ensure the lowest power dissipation when higher loads are being driven. In addition to this, the user can PWM the OL\_ON pin to disable the high resistance mode and minimize power losses further.

However, even if accuracy is achieved by the device; Depending on the current sense ratio, system ADCs can struggle to measure lower load currents accurately due to the low voltages that would need to be read by the ADC. As an example, a 6mA  $I_{Load}$  will be represented as ~5mV using  $RSNS=1k\Omega$  with a current sense ratio of 1200. For a 10-bit 5V-ADC the 5mV output is just over 1LSB(4.88mV). This does not provide enough margin to accurately measure this current for the ADC and likely a higher resolution would need to be used.

Therefore, in order to enable lower ADC resolution requirements and to accurately sense low load currents when operating in high accuracy sense mode, TPS281C30x decreases its current sense ratio to 24. With a sense ratio of 24, the 6mA  $I_{Load}$  will be represented as 250mV using  $RSNS=1k\Omega$  when operating in high accuracy sense mode. This equals to 51LSBs of margin for the same 10-bit ADC or even for an 8-bit ADC the output would still provide >12LSBs of headroom.

[Full Protection and Diagnostics](#) for full device states.

**Table 8-1. Current Sensing Operation Modes**

Conditions	EN	VOUT	OL_ON	KSNS	SNS	FAULT	Behavior	Recovery
Normal Standard Sensing	L	L	L	1200	0	Hi-Z	Normal	
	H	H	L	1200	$I_{Load} / K_{sns1}$	Hi-Z	Normal	
High Accuracy Sense Normal Operation	H	H	H	24	$I_{Load} / K_{sns2}$	Hi-Z	Enables x50 sense ratio for high accuracy sensing and FAULT stays Hi-Z since valid condition is met $I_{Load} < I_{Ksns2\_EN}$ .	
High Accuracy Sense Invalid Range	H	H	H	1200	$I_{Load} / K_{sns1}$	L	FAULT is asserted signaling that high accuracy sensing is not enabled since $I_{Load} > I_{Ksns2\_DIS}$	Clears when load falls below $I_{Ksns2\_EN}$ or OL_ON is reset to LO.

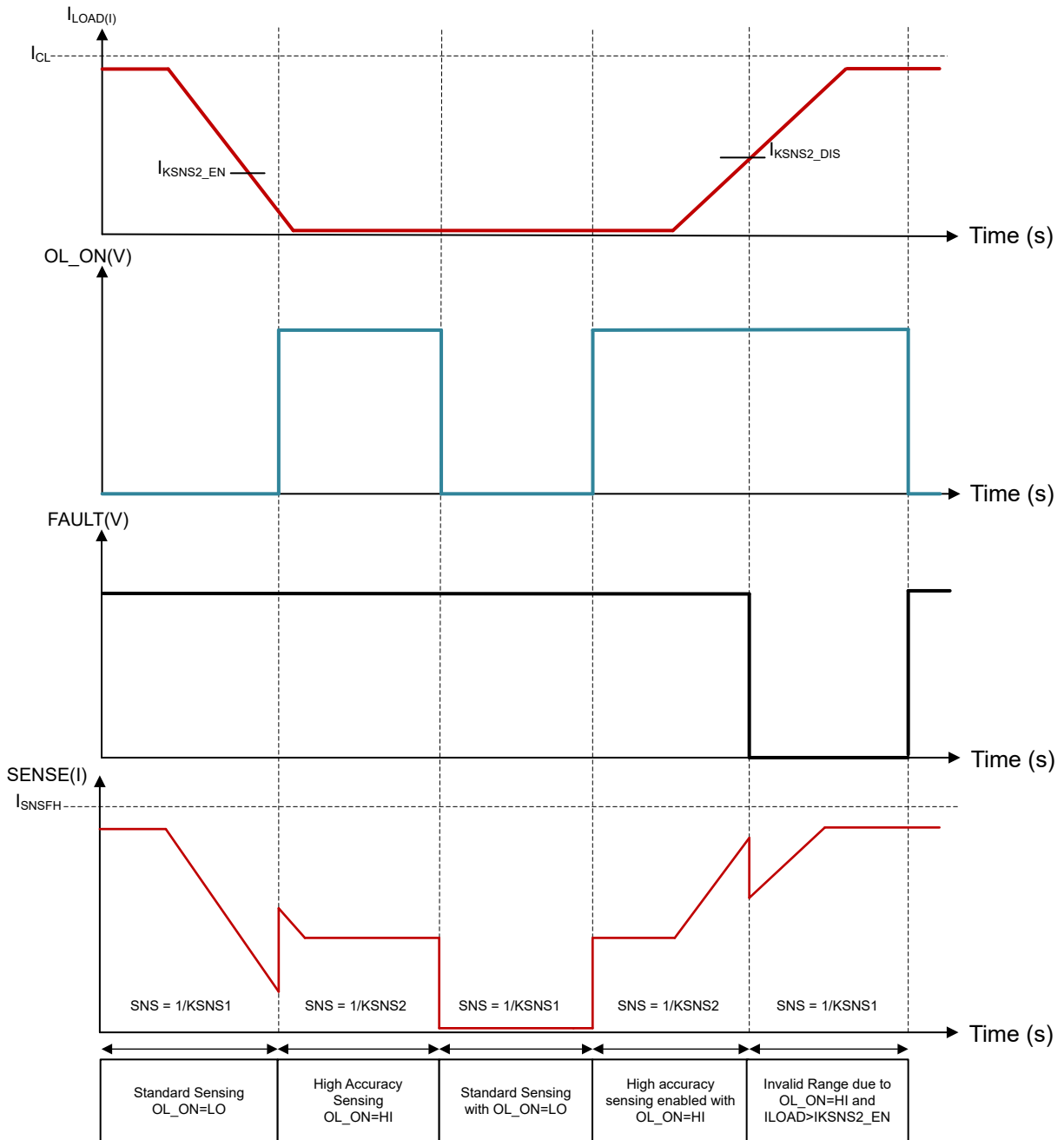


Figure 8-4. High Accuracy Sensing FAULT Indication

### 8.4.2 Programmable Current Limit

A high-accuracy current limit allows higher reliability, which protects the power supply during short circuit or power up. Also, it can save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage.

Current limit offers protection from overstressing to the load and integrated power FET. Current limit holds the current at the set value, and pulls up the SNS pin to  $V_{SNSFH}$  and asserts the  $\overline{FAULT}$  pin as diagnostic reports. The two current-limit thresholds are:

- External programmable current limit -- An external resistor,  $R_{ILIM}$  is used to set the channel current limit. When the current through the device exceeds  $I_{CL}$  (current limit threshold), a closed loop steps in immediately.  $V_{GS}$  voltage regulates accordingly, leading to the  $V_{DS}$  voltage regulation. When the closed loop is set up, the current is clamped at the set value. The external programmable current limit provides the capability to set the current-limit value by application.

Additionally this value can be dynamically changed by changing the resistance on the ILIM pin. This can be seen in the [Applications Section](#)

- Internal current limit:  $I_{LIM}$  pin open or pin shorted to ground -- If the external current limit is out of range on the lower end or the  $I_{LIM}$  pin is shorted to ground, the internal current limit is fixed and typically 0.5A. This works as a safety power limiting mechanism during failures with shorts or open connections with PCB

Overstress.

Both the internal current limit ( $I_{lim,nom}$ ) and external programmable current limit are always active when  $V_S$  is powered and EN is high. The lower value one (of  $I_{LIM}$  and the external programmable current limit) is applied as the actual current limit. The typical deglitch time for the current limit to assert is 2.5 $\mu$ s.

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the ILIM pin must be connected with device GND. Calculate  $R_{LIM}$  with [Equation 2](#).

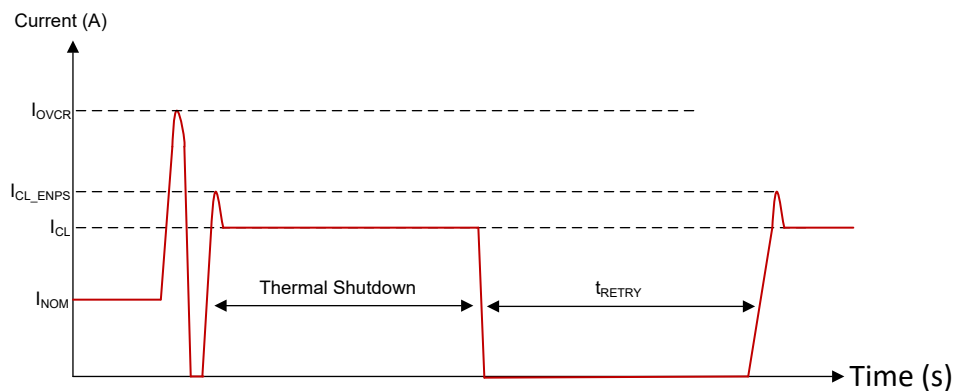
$$R_{LIM} = K_{CL} / I_{CL} \quad (2)$$

For better protection from a hard short-to-GND condition (when  $V_S$  and input are high and a short to GND happens suddenly), an open-loop fast-response behavior is set to turn off the channel, before the current-limit closed loop is set up. With this fast response, the device can achieve better inrush-suppression performance.

#### 8.4.2.1 Short-Circuit and Overload Protection

TPS281C30 provides output short-circuit protection to ensure that the device will prevent current flow in the event of a low impedance path to GND, removing the risk of damage or significant supply droop. The device is guaranteed to protect against short-circuit events regardless of the state of the ILIM pins and with up to 36-V supply at 125°C.

[On-State Short-Circuit Behavior](#) shows the behavior of TPS281C30x when a short-circuit occurs and the device is in the on-state and already outputting current. When the internal pass FET is fully enabled, the current clamping settling time is slower so to ensure overshoot is limited, the device implements a fast trip level at a level  $I_{OVCR}$ . When this fast trip threshold is hit, the device immediately shuts off for a short period of time before quickly re-enabling and clamping the current to  $I_{CL}$  level after a brief transient overshoot to the higher peak current ( $I_{CL\_ENPS}$ ) level. The device will then keep the current clamped at the regulation current limit until the thermal shutdown temperature is hit and the device will safely shut-off.



**Figure 8-5. On-State Short-Circuit Behavior**

Overload Behavior shows the behavior of the TPS281C30x when there is a small change in impedance that sends the load current above the  $I_{CL}$  threshold. The current rises to  $I_{CL\_LINPK}$  above the regulation level. Then the current limit regulation loop kicks in and the current drops to the  $I_{CL}$  value.

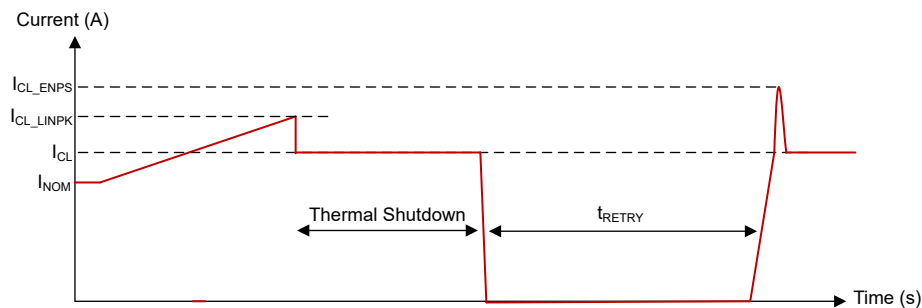


Figure 8-6. Overload Behavior

In all of these cases, the internal thermal shutdown is safe to hit repetitively. There is no device risk or lifetime reliability concerns from repeatedly hitting this thermal shutdown level.

#### 8.4.2.2 Capacitive Charging

**Capacitive Charging Circuit** shows the typical set up for a capacitive load application and the internal blocks that function when the device is used. Note that all capacitive loads will have an associated "load" in parallel with the capacitor that is described as a resistive load but in reality it can be inductive or resistive.

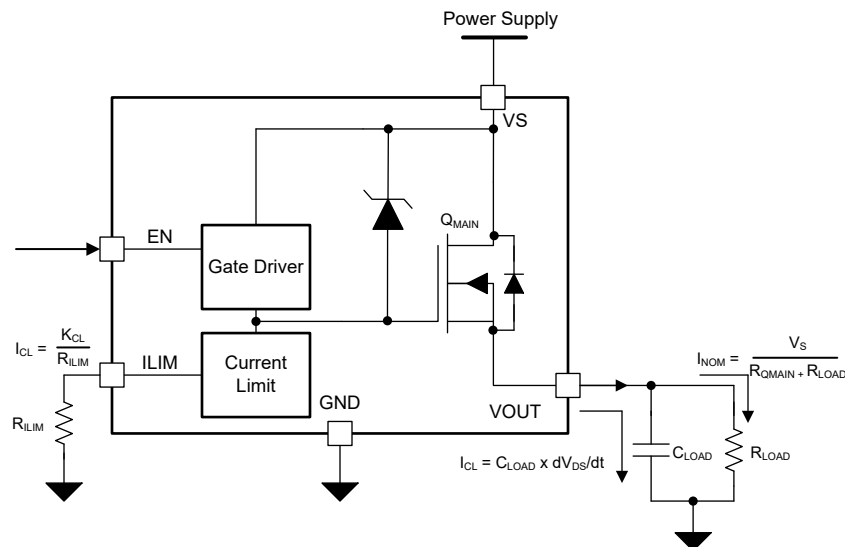
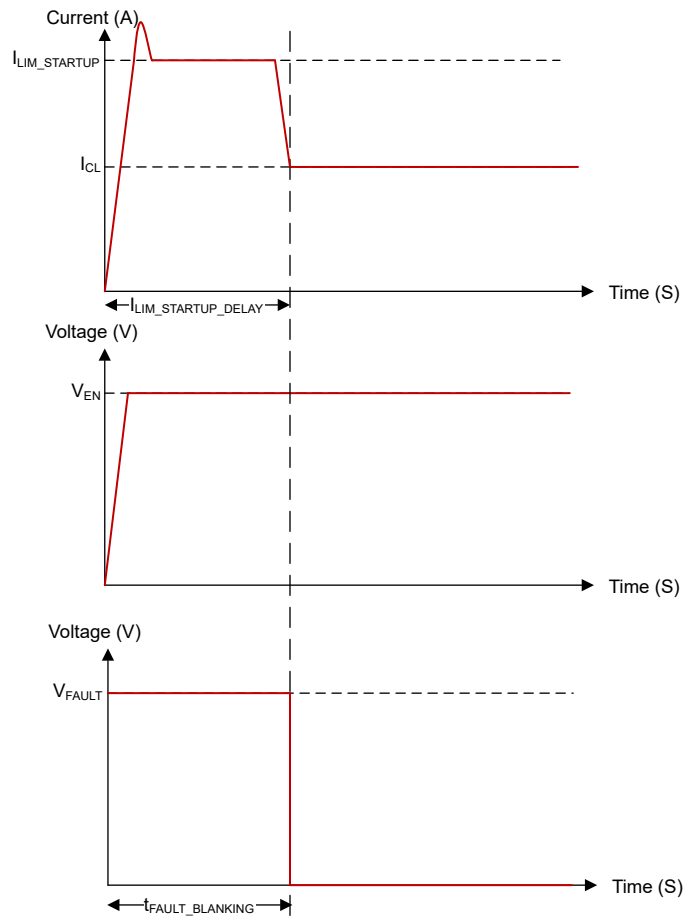


Figure 8-7. Capacitive Charging Circuit

The first thing to check is that the nominal DC current,  $I_{NOM}$ , is acceptable for the TPS281C30 device. This can easily be done by taking the  $R_{\theta JA}$  from the [Thermal Section](#) and multiplying the  $R_{ON}$  of the TPS281C30 and the  $I_{NOM}$  with it, add the ambient temperature and if that value is below the thermal shutdown value the device can operate with that load current. For an example of this calculation see the [Applications Section](#).

The second key care about for this application is to make sure that the capacitive load can be charged up completely without the device hitting thermal shutdown. This is because if the device hits thermal shutdown during the charging, the resistive nature of the load in parallel with the capacitor will start to discharge the capacitor over the duration the TPS281C30x is off. Note that there are some application with high enough load impedance that the TPS281C30 hitting thermal shutdown and trying again is acceptable; however, for the majority of applications the system should be designed so that the TPS281C30x does not hit thermal shutdown while charging the capacitor.

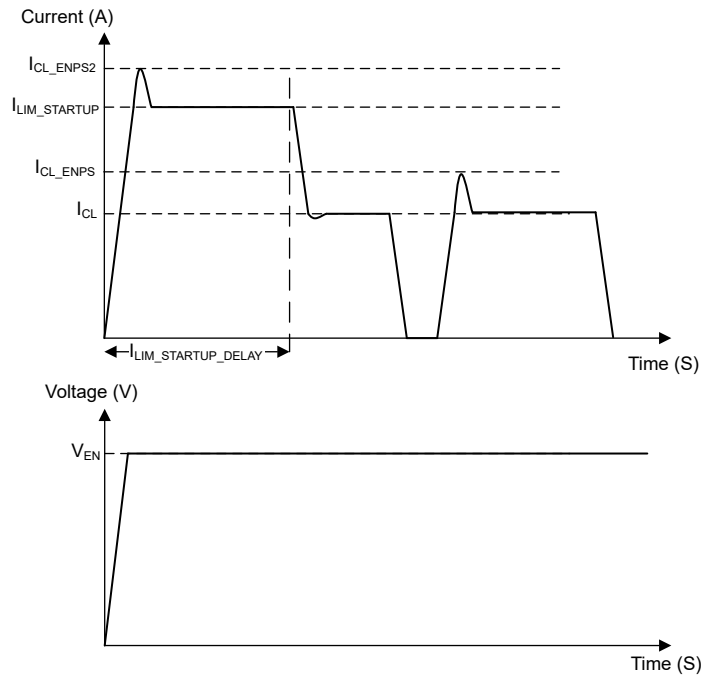
With the current clamping feature of the TPS281C30x, capacitors can be charged up at a lower inrush current than other high current limit switches. This lower inrush current means that the capacitor will take a little longer to charge all the way up. However, to minimize this longer charge time during startup, TPS281C30 implements an inrush current handling feature described in [On-State Short Circuit Behavior](#). When the EN pin goes high to turn on the high side switch, the device will default its current limit threshold to  $I_{LIM\_STARTUP}$  for a duration of  $I_{LIM\_STARTUP\_DELAY}$ . During this delay period, a capacitive load can be charged at a higher rate than what typical  $I_{CL}$  would allow and FAULT will be masked to prevent unwanted Fault triggers. After  $I_{LIM\_STARTUP\_DELAY}$ , the current limit will default back to  $I_{CL}$  and Fault will work normally.



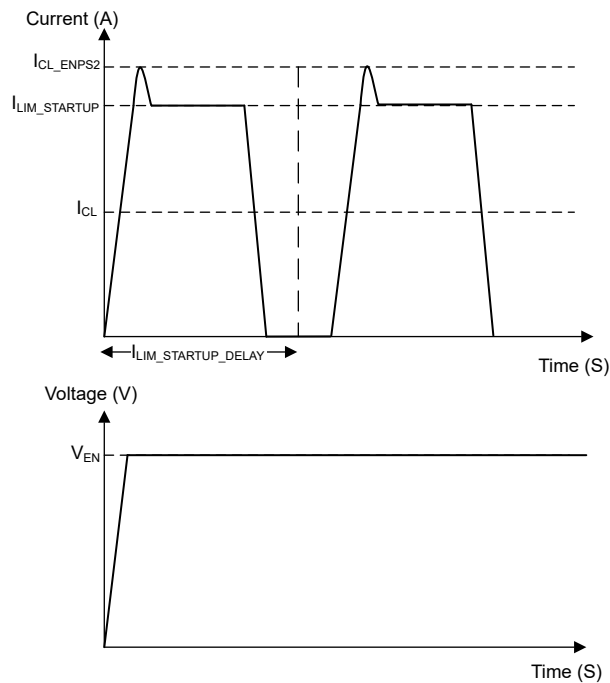
**Figure 8-8. Inrush Current Handling**

The initial inrush current period when the current limit is higher enables two different system advantages when driving loads:

- Enables higher load current to be supported for a period of time of the order of milliseconds to drive high inrush current loads like incandescent bulb loads.
- Enables fast capacitive load charging. In some situations, it is ideal to charge capacitive loads at a higher current than the DC current to ensure quick supply bring up. This architecture allows a module to quickly charge a capacitive load using the initial higher inrush current limit and then use a lower current limit to reliably protect the module under overload or short circuit conditions.



**Figure 8-9. Auto-retry Behavior After  $I_{LIM\_STARTUP\_DELAY}$  Period Expires**



**Figure 8-10. Auto-retry Behavior Before  $I_{LIM\_STARTUP\_DELAY}$  Period Expires**

While in current limiting mode, at any level, the device will have a high power dissipation. If the FET temperature exceeds the over-temperature shutdown threshold, the device will turn off just the channel that is overloaded. After cooling down, the device will re-try. If the device is turning off prematurely on start-up, it is recommended to improve the PCB thermal layout, lower the current limit to lower power dissipation, or decrease the inrush current (capacitive loading).

For more information about capacitive charging with high side switches see the [How to Drive Capacitive Loads](#) application note. This application note has information about the thermal modeling available along with quick ways to estimate if a high side switch will be able to charge a capacitor to a given voltage.

### 8.4.3 Inductive-Load Switching-Off Clamp

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET may break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely  $V_{DS,clamp}$ , the clamp diode between the drain and gate. Please note that the internal  $V_{DS,clamp}$  will only be available in version A, B. For version C, D, E, an external clamp across VDS or at VOUT is required to dissipate the inductive energy properly.

$$V_{DS,Clamp} = V_S - V_{OUT} \quad (3)$$

During the current-decay period ( $T_{DECAY}$ ), the power FET is turned on for inductance-energy dissipation. Both the energy of the power supply ( $E_S$ ) and the load ( $E_{LOAD}$ ) are dissipated on the high-side power switch itself, which is called  $E_{HSD}$ . If resistance is in series with inductance, some of the load energy is dissipated in the resistance.

$$E_{HSD} = E_S + E_{LOAD} = E_S + E_L - E_R \quad (4)$$

From the high-side power switch's view,  $E_{HSD}$  equals the integration value during the current-decay period.

$$E_{HSD} = \int_0^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t) dt \quad (5)$$

$$T_{DECAY} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \quad (6)$$

$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[ R \times I_{OUT(MAX)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \right] \quad (7)$$

When R approximately equals 0,  $E_{HSD}$  can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I_{OUT(MAX)}^2 \frac{V_{BAT} + |V_{OUT}|}{R^2} \quad (8)$$



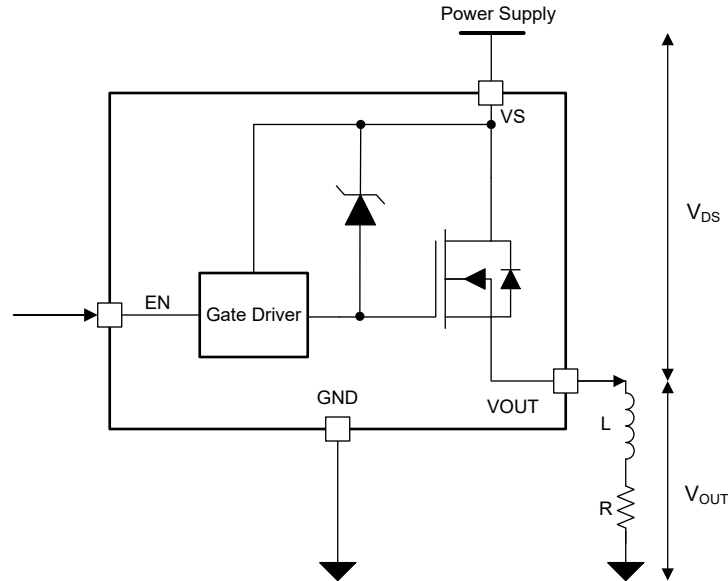


Figure 8-11. Driving Inductive Load

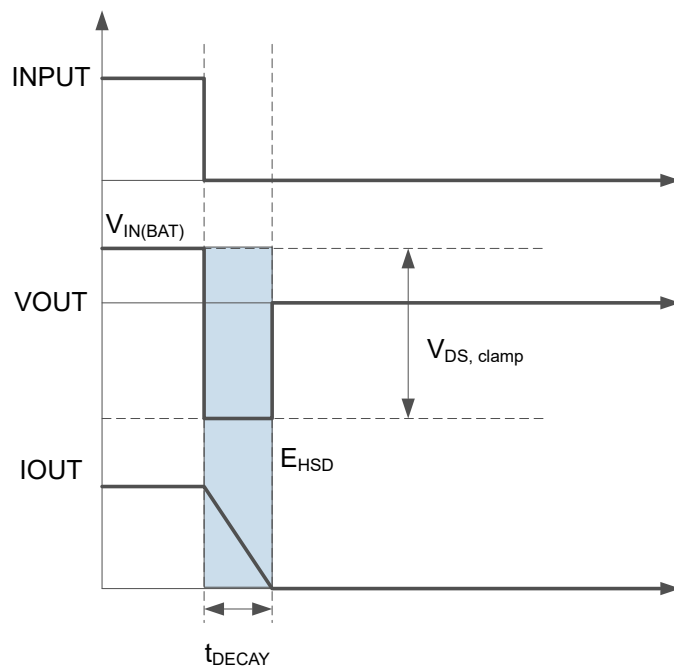


Figure 8-12. Inductive-Load Switching-Off Diagram

As discussed previously, when switching off, battery energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation. For each high-side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition. TI provides the upper limit of single-pulse energy that devices can tolerate under the test condition:  $V_S = 24\text{ V}$ , inductance from 0.1 mH to 400 mH,  $R = 0\ \Omega$ , FR4 2s2p board,  $2 \times 70\text{-}\mu\text{m}$  copper,  $2 \times 35\text{-}\mu\text{m}$  copper, thermal pad copper area 600 mm<sup>2</sup>.

#### 8.4.4 Inductive Load Demagnetization

When switching off an inductive load, the inductor can impose a negative voltage on the output of the switch. The TPS281C30 includes voltage clamps between VS and VOUT to limit the voltage across the FETs and

demagnetize load inductance if there is any. The negative voltage applied at the OUT pin drives the discharge of inductor current. Figure 8-13 shows the device discharging a 400-mH load.

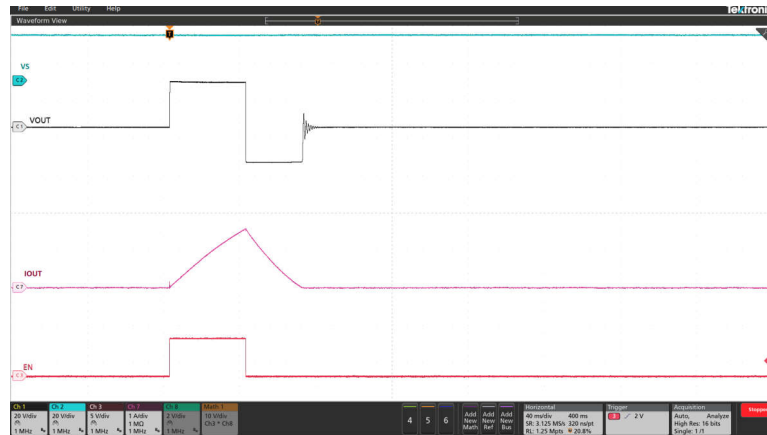


Figure 8-13. TPS281C30 Inductive Discharge (400 mH)

The maximum acceptable load inductance is a function of the energy dissipated in the device and therefore the load current and the inductive load. The maximum energy and the load inductance the device can withstand for one pulse inductive dissipation at 125°C is shown in Figure 8-14. The device (version A, B) can withstand 40% of this energy for one million inductive repetitive pulses with a >4-Hz repetitive pulse. If the application parameters exceed this device limit, use a protection device like a freewheeling diode to dissipate the energy stored in the inductor.

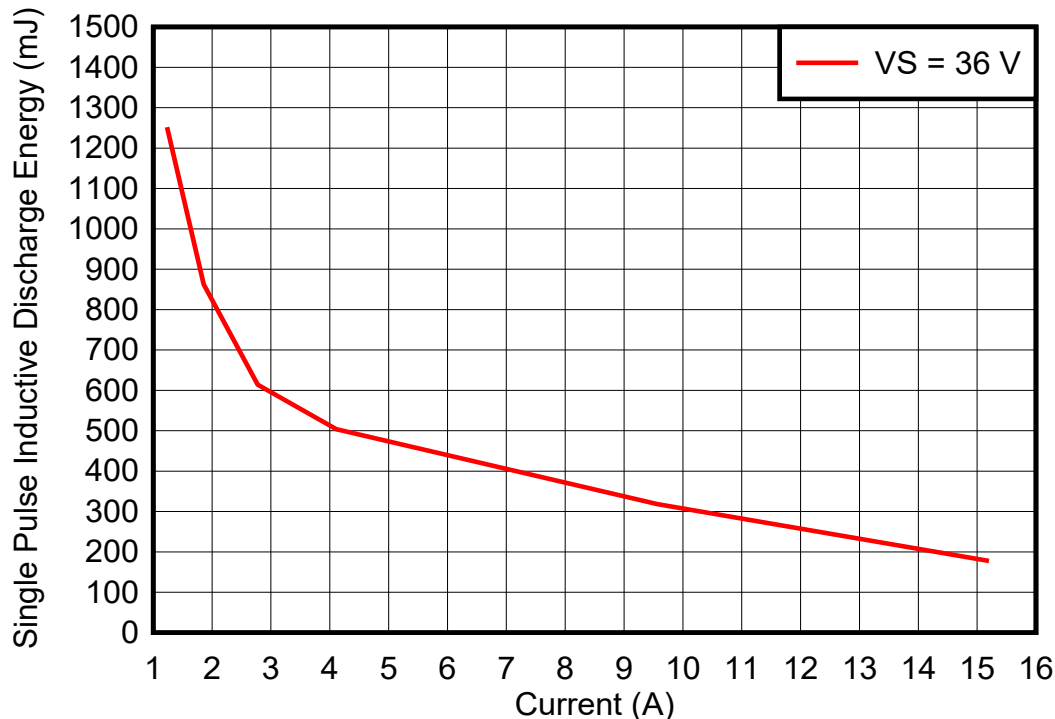


Figure 8-14. TPS281C30 Inductive Load Discharge Energy Capability at 125°C

### 8.4.5 Full Protections and Diagnostics

**Current Sensing** is active when DIAG\_EN enabled. When DIAG\_EN is low, current sense is disabled. The SNS output is internally clamped to around 1V if there is an external voltage appear at SNS pin.

**Table 8-2. DIAG\_EN Logic Table**

DIAG_EN	EN Condition	Protections and Diagnostics
HIGH	HIGH	See Fault Table
	LOW	
LOW	HIGH	Diagnostics disabled and SNS output is clamped internally to around 1V. Protection is normal and $\overline{\text{FAULT}}$ continues to indicate TSD or ILIM.
	LOW	

**Table 8-3. Status Table (DIAG\_EN=HIGH )**

Conditions	EN	VOUT	OL_ON	FAULT	SNS	Behavior	Recovery
Normal Standard Sensing	L	L	L	Hi-Z	0	Normal	
	H	H	L	Hi-Z	$I_{Load} / K_{sns1}$	Normal	
High Accuracy Sense Invalid Range	H	H	H	L	$I_{Load} / K_{sns1}$	FAULT is asserted signaling that high accuracy sensing is not enabled since $I_{Load} > I_{Ksns2\_EN}$	Clears when load falls below $I_{Ksns2\_EN}$ or OL_ON is reset to LO.
High Accuracy Sense Normal Operation	H	H	H	Hi-Z	$I_{Load} / K_{sns2}$	Enables x50 sense ratio for high accuracy sensing and FAULT stays Hi-Z since valid condition is met $I_{Load} < I_{Ksns2\_EN}$ .	
Overcurrent	H	$V_S - I_{LIM} * R_{LOAD}$	x	L	$V_{SNSFH}$	Holds the current at the current limit until thermal shutdown	
STG, Relative Thermal Shutdown, Absolute Thermal Shutdown	H	H/L	x	L	$V_{SNSFH}$	Shuts down when devices hits relative or absolute thermal shutdown	Auto retries when $T_{HYSIS}$ met and it has been longer than $t_{RETRY}$ amount of time
Open Load (not available in Ver. E)	H	H	L	Hi-Z	$I_{Load} / K_{sns1} = \sim 0$	Normal behavior, user can judge if it is an open load or not	
	H	H	H	Hi-Z	$I_{Load} / K_{sns2} = \sim 0$	Normal behavior, user can judge if it is an open load or not	
	L	H	L	L	$V_{SNSFH}$	Internal pullup resistor is active. If $V_S - V_{OUT} < V_{OL}$ then fault active	Clears when fault goes away
Reverse Polarity	x	x	x	x	x	Channel turns on to lower power dissipation. Current into ground pin is limited by external ground network	

#### 8.4.5.1 Open-Load Detection

##### On-State Open Load Detection

When the main channel is enabled faults are diagnosed by reading the voltage on the SNS or  $\overline{FLT}$  pin and judged by the user. A benefit of high-accuracy current sense is that this device can achieve a very low open-load detection threshold, which correspondingly expands the normal operation region. As explained in section [high accuracy sense mode](#), this mode can be used to sense 6mA currents accurately.

##### Off-State Open Load Detection (available in ver. A, B, C, D)

In the off state, if a load is connected, the output voltage is pulled to 0V. In the case of an open load, the output voltage is close to the supply voltage,  $V_S - V_{OUT} < V_{ol,off}$ . The FLT pin goes low to indicate the fault to the MCU, and the SNS pin is pulled up to  $I_{SNSFH}$ . There is always a leakage current  $I_{ol,off}$  present on the output, due to the internal logic control path or external humidity, corrosion, and so forth. Thus, TI implemented an internal pullup resistor to offset the leakage current. This pullup current should be less than the output load current to avoid false detection in the normal operation mode. To reduce the standby current, TI implemented a switch in series with the pullup resistor controlled by the DIAG\_EN pin. The pull up resistor value is 150 kΩ.

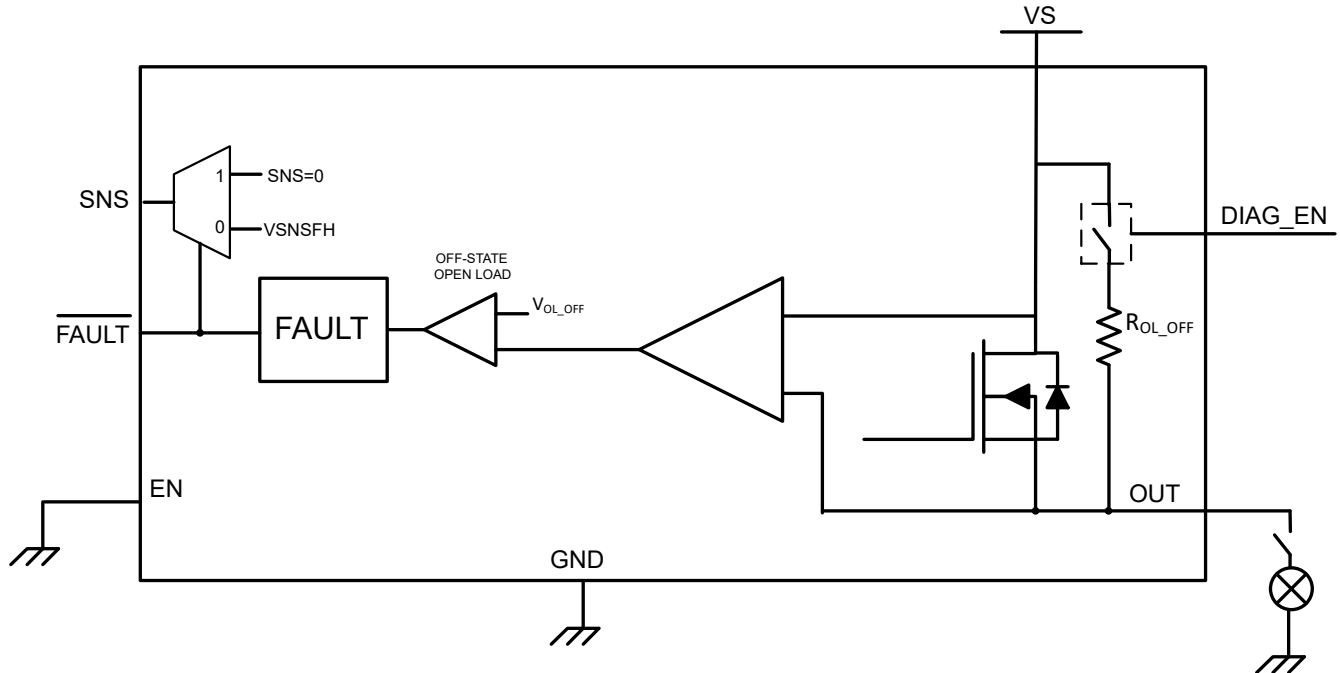
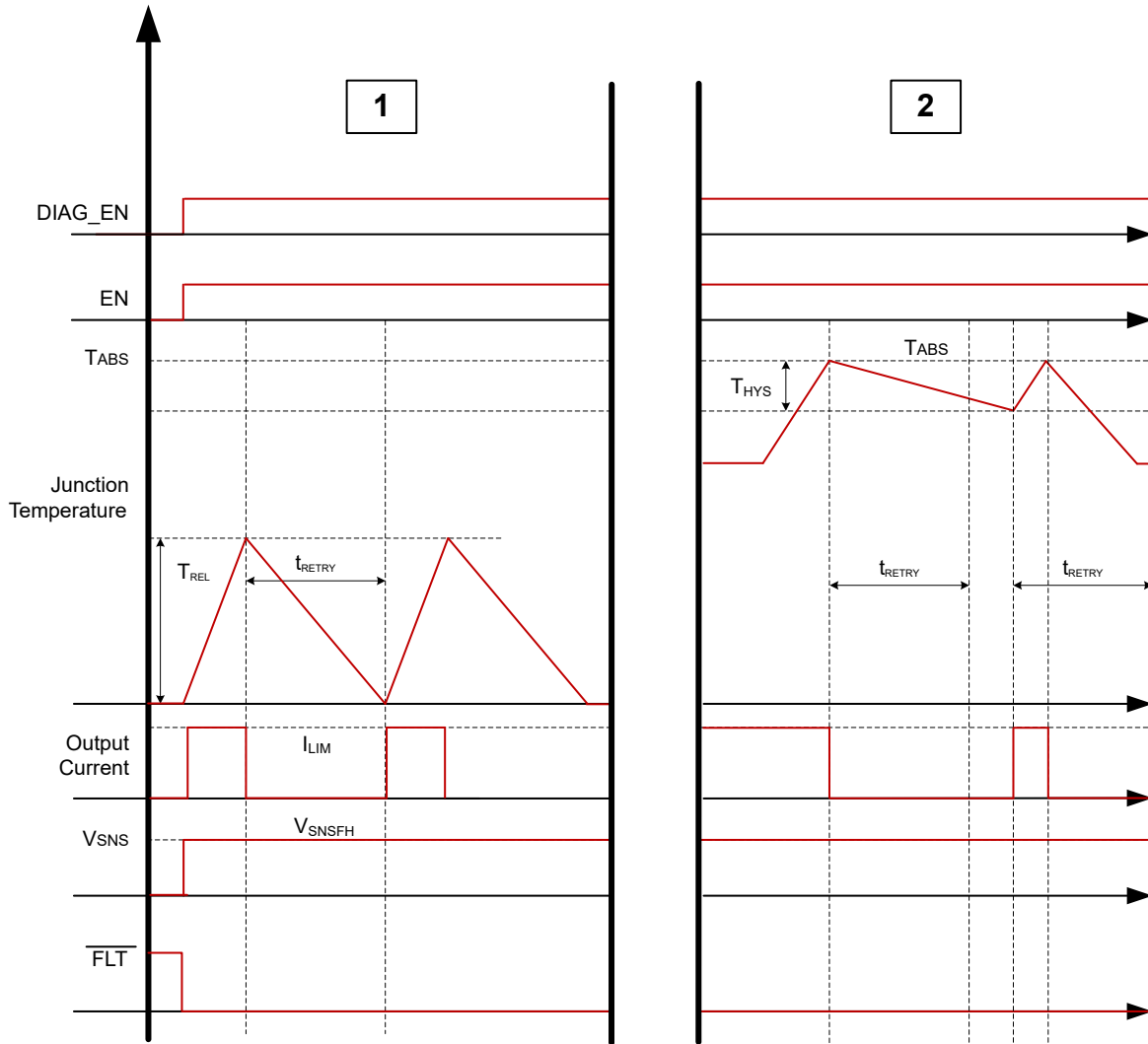


Figure 8-15. Off-State Open-Load Detection Circuit

#### 8.4.5.2 Thermal Protection Behavior

The thermal protection behavior can be split up into 2 categories of events that can happen. [Thermal behavior](#) shows each of these categories.

1. **Relative thermal shutdown:** The device is enabled into an over current event. The DIAG\_EN pin is high so that diagnostics can be monitored on SNS and FLT. The output current rises up to the  $I_{LIM}$  level and the FLT goes low while the SNS goes to  $V_{SNSFH}$ . With this large amount of current going through the junction temperature of the FET increases rapidly with respect to the controller temperature. When the power FET temperature rises  $T_{REL}$  amount above the controller junction temperature  $\Delta T = T_{FET} - T_{CON} > T_{REL}$ , the device shuts down. The faults are continually shown on SNS and FLT and the part waits for the  $t_{RETRY}$  timer to expire. When  $t_{RETRY}$  timer expires, since EN is still high, the device will come back on into this  $I_{LIM}$  condition.
2. **Absolute thermal shutdown:** In this case, the ambient temperature is now much higher than previous. The device is still enabled in an over current event with DIAG\_EN high. However, in this case the junction temperature rises up and hits an absolute reference temperature,  $T_{ABS}$ , and then shuts down. The device will not recover until both  $T_J < T_{ABS} - T_{hys}$  and the  $t_{RETRY}$  timer has expired.



**Figure 8-16. Thermal Behavior**

#### 8.4.5.3 Undervoltage Lockout (UVLO) Protection

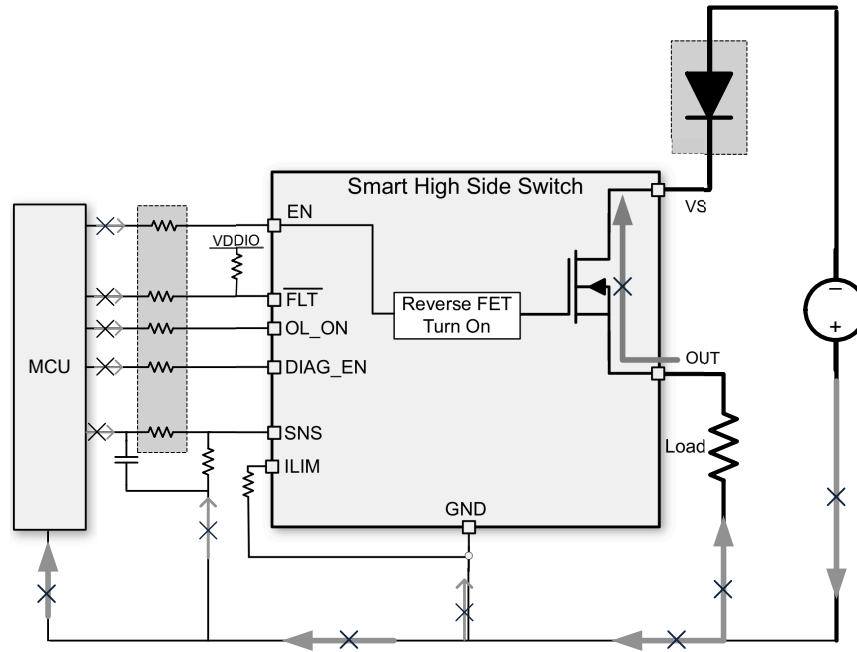
The device monitors the supply voltage  $V_S$  to prevent unpredictable behaviors in the event that the supply voltage is too low. When the supply voltage falls down to  $V_{UVLOF}$ , the output stage is shut down automatically. When the supply rises up to  $V_{UVLOR}$ , the device turns on. If an overcurrent event trips the UVLO threshold, the device will shut off and come back on into a current limit safely.

#### 8.4.5.4 Overvoltage (OVP) Protection

The device monitors the supply voltage  $V_S$  to prevent unpredictable behaviors in the event that the supply voltage is too high. When the supply increases beyond  $V_{S,OVP}$ , the output stage is shut down automatically. When the supply falls below  $V_{S,OVPF}$ , the device turns on. If an overcurrent event trips the OVP threshold due to inductive load oscillations, the device integrates a deglitcher to avoid immediate output shutoff due to short transients.

### 8.4.5.5 Reverse Polarity Protection

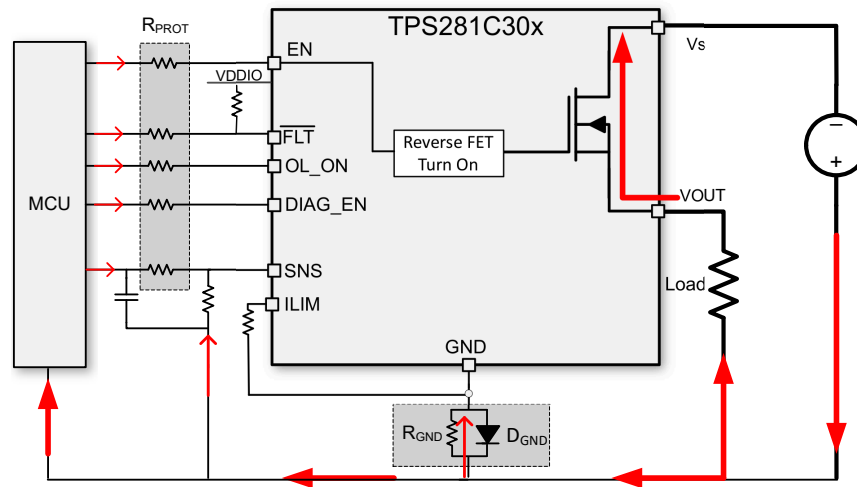
**Method 1:** Blocking diode connected with VBB. Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.



**Figure 8-17. Reverse Protection With Blocking Diode**

**Method 2 (GND network protection):** Only the high-side device is protected under this connection. The load reverse loop is limited by the load itself. Note when reverse polarity happens, the continuous reverse current through the power FET should be less than  $I_{rev}$ . Of the three types of ground pin networks, TI strongly recommends type 3 (the resistor and diode in parallel). No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Leave the NC pin floating or connect to the device GND. TI recommends to leave floating.
- Connect the current limit programmable resistor to the device GND.



**Figure 8-18. Reverse Protection With GND Network**

- **Type 1 (resistor):** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses. However, this leads to higher GND shift during normal operation mode. Also, consider the resistor power dissipation.

$$R_{GND} \leq \frac{V_{GNDshift}}{I_{nom}} \tag{9}$$

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \tag{10}$$

where

- $V_{GNDshift}$  is the maximum value for the GND shift, determined by the HSS and microcontroller. TI suggests a value  $\leq 0.6V$ .
- $I_{nom}$  is the nominal operating current.
- $-V_{CC}$  is the maximum reverse voltage seen on the battery line.
- $-I_{GND}$  is the maximum reverse current the ground pin can withstand, which is available in [Section 6.1](#).

If multiple high-side power switches are used, the resistor can be shared among devices.

- **Type 2 (diode):** A diode is needed to block the reverse voltage, which also brings a ground shift ( $\approx 600mV$ ). However, an inductive load is not acceptable to avoid an abnormal status when switching off.
- **Type 3 (resistor and diode in parallel (recommended)):** A peak negative spike may occur when the inductive load is switching off, which may damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are  $1.5k\Omega$  resistor in parallel with an  $I_F > 100mA$  diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.



#### 8.4.5.6 Protection for MCU I/Os

In many conditions, such as the negative surge pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin may damage the MCU I/O pins [more likely, the internal circuitry connected to the pins]. Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 10 kΩ resistance for the RPROT resistors.

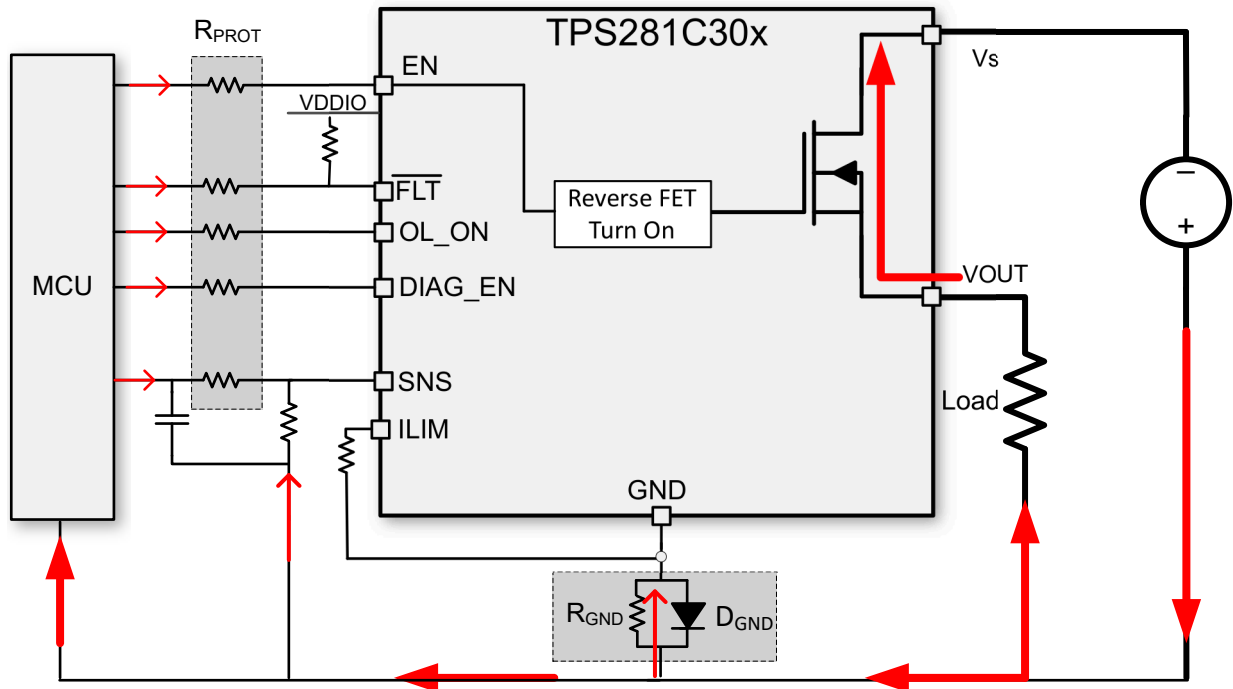


Figure 8-19. MCU IO Protections

#### 8.4.5.7 Diagnostic Enable Function

The diagnostic enable pin, DIAG\_EN, offers multiplexing of the microcontroller diagnostic input for current sense or digital status, by sharing the same sense resistor and ADC line or I/O port among multiple devices.

In addition, this pin can be used to manage power dissipation by the device. During the output-on period, if no continuous sense output diagnostics are required, the diagnostic disable feature will lower the operating current. On the other hand, the output-off period, the diagnostic disable function lowers the current consumption for the standby condition.

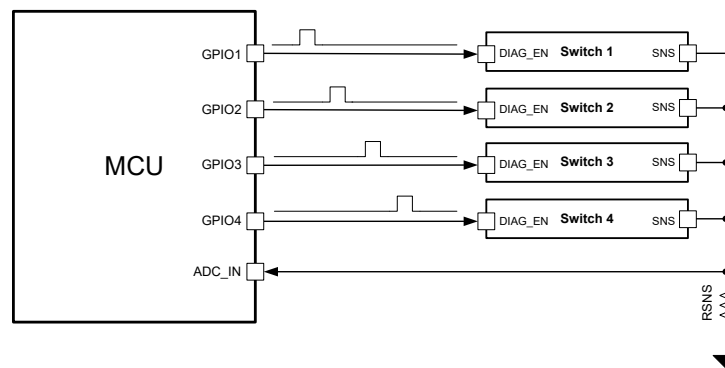


Figure 8-20. Resistor sharing

#### 8.4.5.8 Loss of Ground

The ground connection may be lost either on the device level or on the module level. If the ground connection is lost, the channel output will be disabled irrespective of the EN input level. If the switch was already disabled when the ground connection was lost, the outputs will remain disabled even when the channels are enabled. The steady state current from the output to the load that remains connected to the system ground is below the level specified in the [Specifications](#) section of this document. When the ground is reconnected, normal operation will resume.

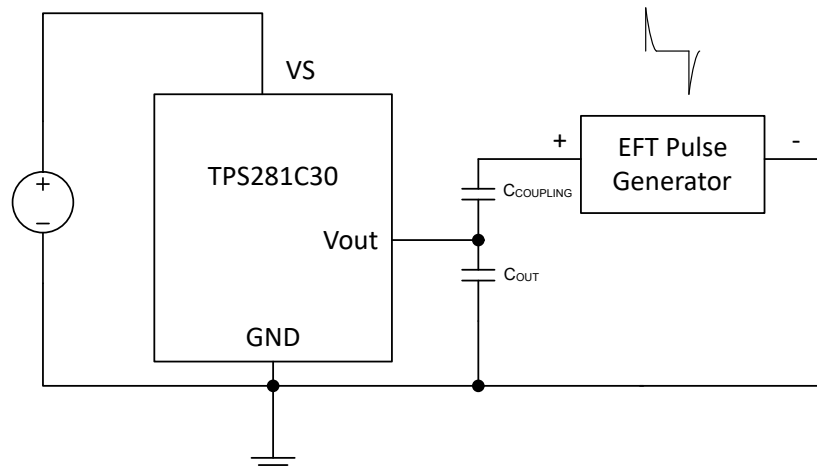
#### 8.4.5.9 Enhanced EFT Immunity

TPS281C30E has an enhanced EFT immunity compared to the other variants. The E variant implemented a stronger gate pulldown circuit which helps the device in the OFF state to stay OFF when an EFT pulses comes in. Due to the active circuit in the OFF state, the E variant will draw a higher current from the supply during the OFF state  $I_{Q(OFF)}$  compared to the other variants. E version device will have Hi-Z on the output while OFF, with leakage current  $I_{OUT(OFF)}$ .

The max EFT voltage level  $V_{(EFT)}$  will largely depending on the components used in the test circuit. The larger the output capacitor, and the smaller the coupling capacitor, the higher the EFT voltage level can be tolerated. As the coupling capacitor value is fixed in most EFT standards, increasing the output capacitor value can be an effective way to increase the maximum EFT voltage level.

[Figure 8-21](#) shows the setup for EFT testing. TPS281C30E is tested to pass +/- 2.5 kV EFT at VS and VOUT with 10nF output capacitor and 100pF coupling capacitor as shown in the diagram. The output capacitor can be increased if passing higher level of EFT is desired. The A, B, C, D variants are tested to pass +/- 2 kV EFT at VS and VOUT with 22nF output capacitor and 100pF coupling capacitor. The DIAG\_EN has to be high for A, B, C, D version in the OFF state in order to not enter the sleep state and have the EFT immunity stated above, while the DIAG\_EN can be either high or low for E version as the EFT protection circuit is always active. The test conditions are outlined in [EFT Test Conditions](#).

There is a strong pulldown circuitry to keep the power FET OFF during OFF state EFT transient. The circuitry is activated after  $EFT_{DELAY}$  period to not affect the normal turn-off slew rate. However, the part is not protected during the  $EFT_{DELAY}$  period as illustrated in [Figure 8-22](#).



**Figure 8-21. EFT Test Setup**

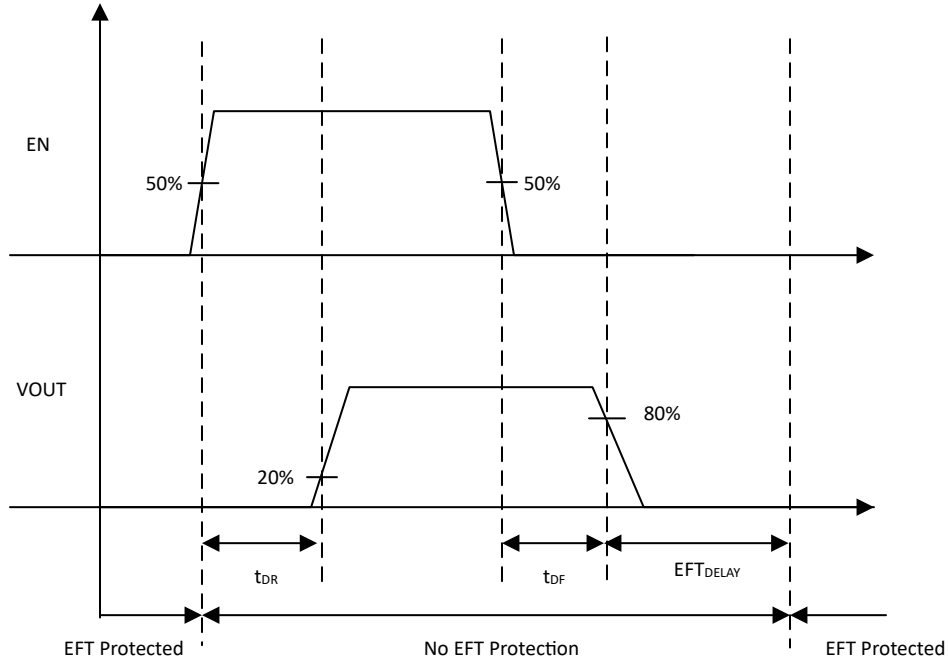


Figure 8-22. EFT Timing Diagram

Table 8-4. EFT Test Conditions

Device Version	EFT Level	C <sub>OUT</sub>	C <sub>COUPLING</sub>	DIAG_EN
A, B, C, D	+/- 2 kV	22nF	100pF	High
E	+/- 2.5 kV	10nF	100pF	High/Low

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

### 9.2 Typical Application

The [Typical Application Circuit](#) shows an example of how to design the external circuitry parameters.

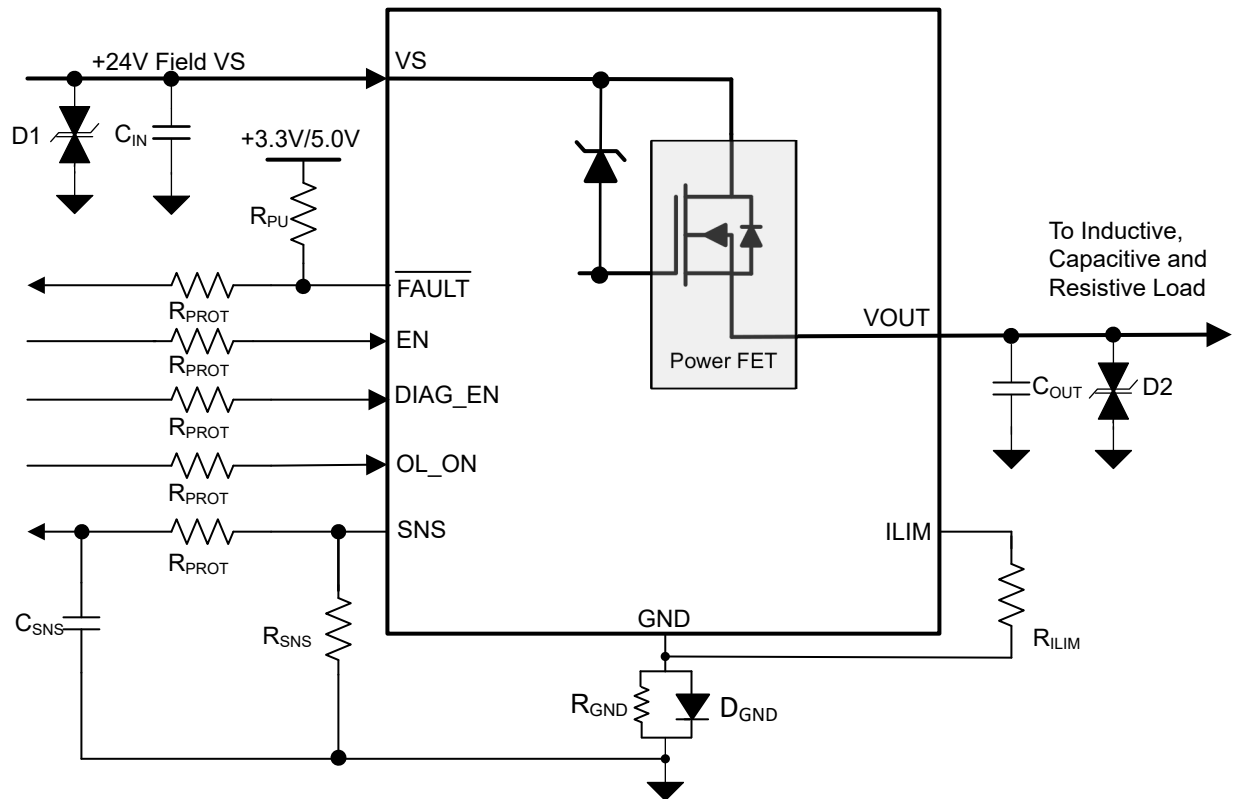


Figure 9-1. Typical Application Circuit

### 9.2.1 Design Requirements

Component	Typical Value	Purpose
D1	SMBJ60CA	Clamp surge voltages at the supply input
D2	SMBJ36CA (Optional for version A, B)	Dissipate the inductive energy at turn-off. A clamp is required for version C, D, E for driving inductive loads.
CIN1	100nF	Stabilize the input supply and filter out low frequency noise.
CIN2	4.7nF	Filtering of voltage transients (for example, ESD, IEC 61000-4-5) and improved emissions.
RPROT	10kΩ	Protection resistor for microcontroller and device I/O pins - Optional for reverse polarity protection
RILIM	7.5kΩ – 50kΩ	Set current limit threshold
RSNS	1kΩ	Translate the sense current into sense voltage.
CSNS	100pF	Coupled with RPROT on the SNS line creates a low pass filter to filter out noise going into the ADC of the MCU.
CVOUT	22nF	Improves EMI performance, filtering of voltage transients
RGND	1kΩ	Stabilize GND potential during turn-off of inductive load - Optional for reverse polarity protection
DGND	BAS21 Diode	Keeps GND close to system ground during normal operation - Optional for reverse polarity protection

#### 9.2.1.1 IEC 61000-4-5 Surge

The TPS281C30 is designed to survive against IEC 61000-4-5 surge using external TVS clamps. The device is rated to 64 V ensuring that external TVS diodes can clamp below the rated maximum voltage of the TPS281C30x. Above 64 V, the device includes VDS clamps to help shunt current and ensure that the device survives the transient pulses. Depending on the class of the output, TI recommends that the system has a SMBJ36A or SMCJ36A between VS and module GND.

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Selecting RILIM

In this application, the TPS281C30A must allow for the maximum DC current with margin but minimize the energy in the switch and the load on the input supply during a fault condition by minimizing the current limit.

The nominal current limit should be set such that the worst case (lowest) current limit will be higher than the maximum load current (4 A). Since the lower limit is 10% below the typical value, for this application, the best  $I_{LIM}$  set point is approximately 5.5A. The below equation allows you to calculate the  $R_{ILIM}$  value that is placed from the  $I_{LIMx}$  pins to GND pin of the device.  $R_{ILIM}$  is calculated in kΩ.

$$R_{ILIM} = K_{CL} / I_{CL} \tag{11}$$

The  $K_{CL}$  value in the [Specifications](#) section is 50A/kΩ. So the calculated value of  $R_{ILIM}$  is 9.09 kΩ which can be found as a standard 1% resistor.

#### 9.2.2.2 Selecting RSNS

[Table 9-1](#) shows the requirements for the load current sense in this application. The  $K_{SNS}$  value is specified for the device and can be found in the [Specifications](#) section.

**Table 9-1.  $R_{SNS}$  Calculation Parameters**

PARAMETER	EXAMPLE VALUE
Current Sense Ratio ( $K_{SNS1}$ )	1300

**Table 9-1. R<sub>SNS</sub> Calculation Parameters (continued)**

PARAMETER	EXAMPLE VALUE
Current Sense Ratio (K <sub>SNS2</sub> )	24
Largest diagnosable load current	4.8 A
Smallest diagnosable load current	4 mA
Full-scale ADC voltage	5.0 V
ADC resolution	10 bit

The load current measurement up to 4.8 A ensures that even in the event of an overload but below the set current limit, the MCU can register and react by turning off the FET while the low level of 4 mA allows for accurate measurement of low load currents and enable the distinction open load faults from supported nominal load currents. For load currents < 50 mA, the customer can enable high accuracy sensing to change the sense ratio from K<sub>SNS1</sub> to K<sub>SNS2</sub>. This prevents the requirement of a higher resolution ADC and it also increases sense accuracy. Go to [high accuracy sensing](#) for more information.

The R<sub>SNS</sub> resistor value should be selected such that the largest diagnosable load current puts the SNS pin voltage (V<sub>SNS</sub>) at about 90% of the ADC full-scale. With this design, any ADC value above 80% of full scale (FS) can be considered a fault. Additionally, the R<sub>SNS</sub> resistor value should ensure that the smallest diagnosable load current does not cause V<sub>SNS</sub> to fall below at a least a few LSB of the ADC.

With the given example values, a 1.0-kΩ sense resistor satisfies both requirements.

**Table 9-2. V<sub>SNS</sub> Calculation**

Sense Mode	OL_ON	LOAD (A)	SENSE RATIO	I <sub>SNS</sub> (mA)	R <sub>SNS</sub> (Ω)	V <sub>SNS</sub> (V)	% of 5-V ADC
Standard Sensing	LO	4.8A	1200	3.69	1000	3.69	73.8%
High Accuracy Sensing	HI	0.004	24	0.166	1000	0.166	3.3% (~34 LSBs)

## 9.3 Power Supply Recommendations

The TPS281C30 device is designed to operate in a 24V industrial system. The allowed supply voltage range (V<sub>S</sub> pin) is 6V to 36V as measured at the V<sub>S</sub> pin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in [Section 6.5](#). The device is also designed to withstand voltage transients beyond this range such as SELV supply failures.

It is recommended to place a 0.1μF capacitor at the V<sub>S</sub> supply input to stabilize the input supply and filter out low frequency noise. The power supply must be able to withstand all transient load current steps. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

V <sub>S</sub> INPUT SUPPLY VOLTAGE RANGE	DESCRIPTION
6V to 36V	Nominal supply voltage, all parametric specifications apply. The device is completely short-circuit protected.
36V > V <sub>S</sub> > V <sub>S, OVPR</sub>	Device is fully functional and protected but timing parametrics can deviate from specifications.
V <sub>S</sub> > V <sub>S, OVPR</sub>	SELV supply voltage. Device disables and tolerates up to 64V at the input for extended period of time.

## 9.4 Layout

### 9.4.1 Layout Guidelines

To prevent thermal shutdown, T<sub>J</sub> must be less than 125°C. If the output current is very high, the power dissipation may be large. The HTSSOP and QFN packages have good thermal impedance. However, the PCB

layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

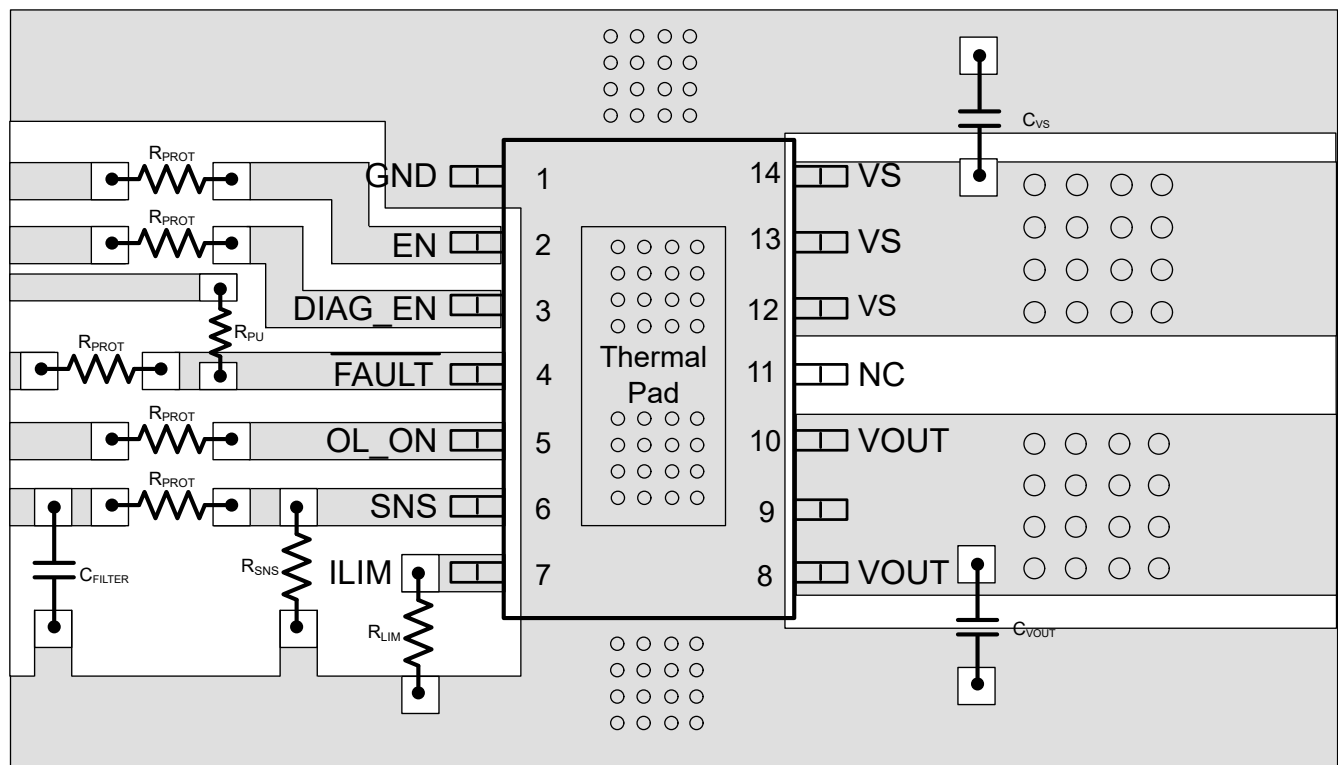
- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

**9.4.1.1 EMC Considerations**

**9.4.2 Layout Example**

**9.4.2.1 PWP Layout without a GND Network**

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.



**Figure 9-2. PWP Layout Without a GND Network**

### 9.4.2.2 PWP Layout with a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.

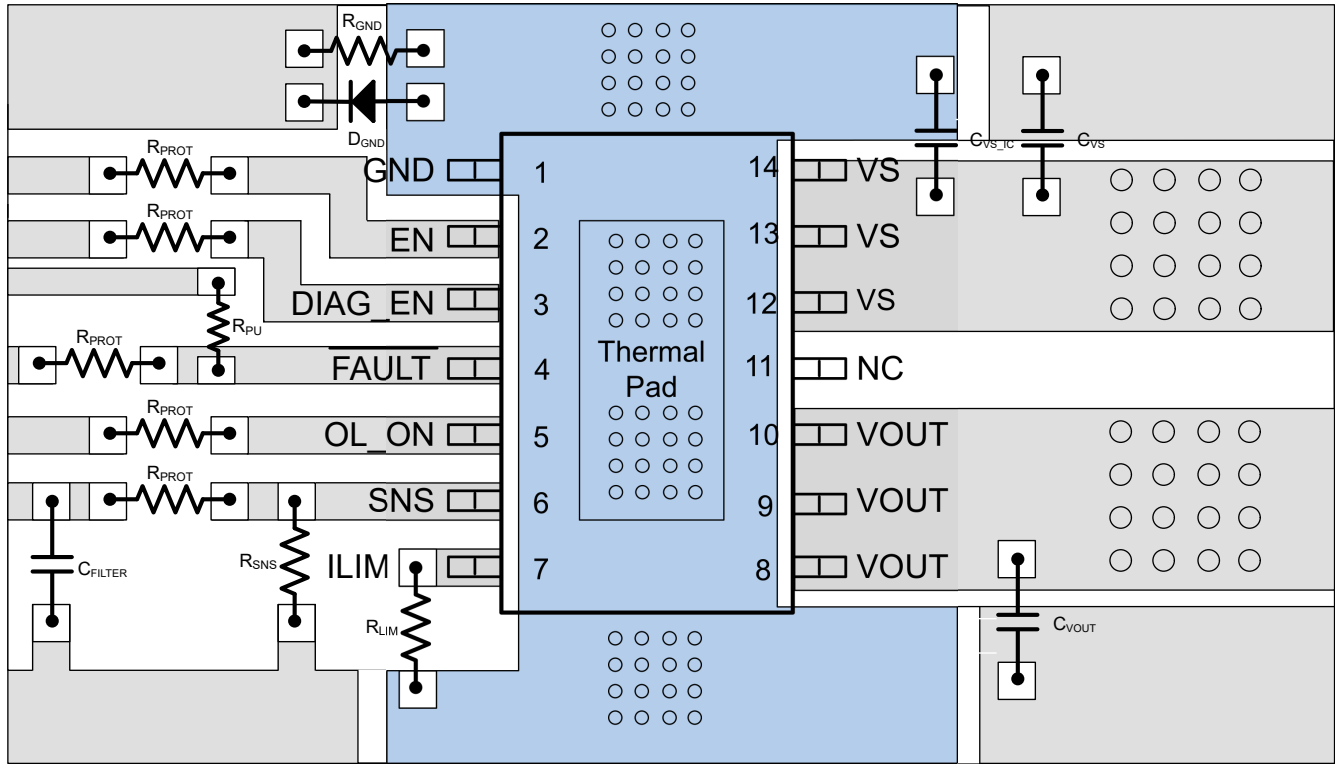


Figure 9-3. PWP Layout With a GND Network

### 9.4.2.3 RGW Layout with a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.



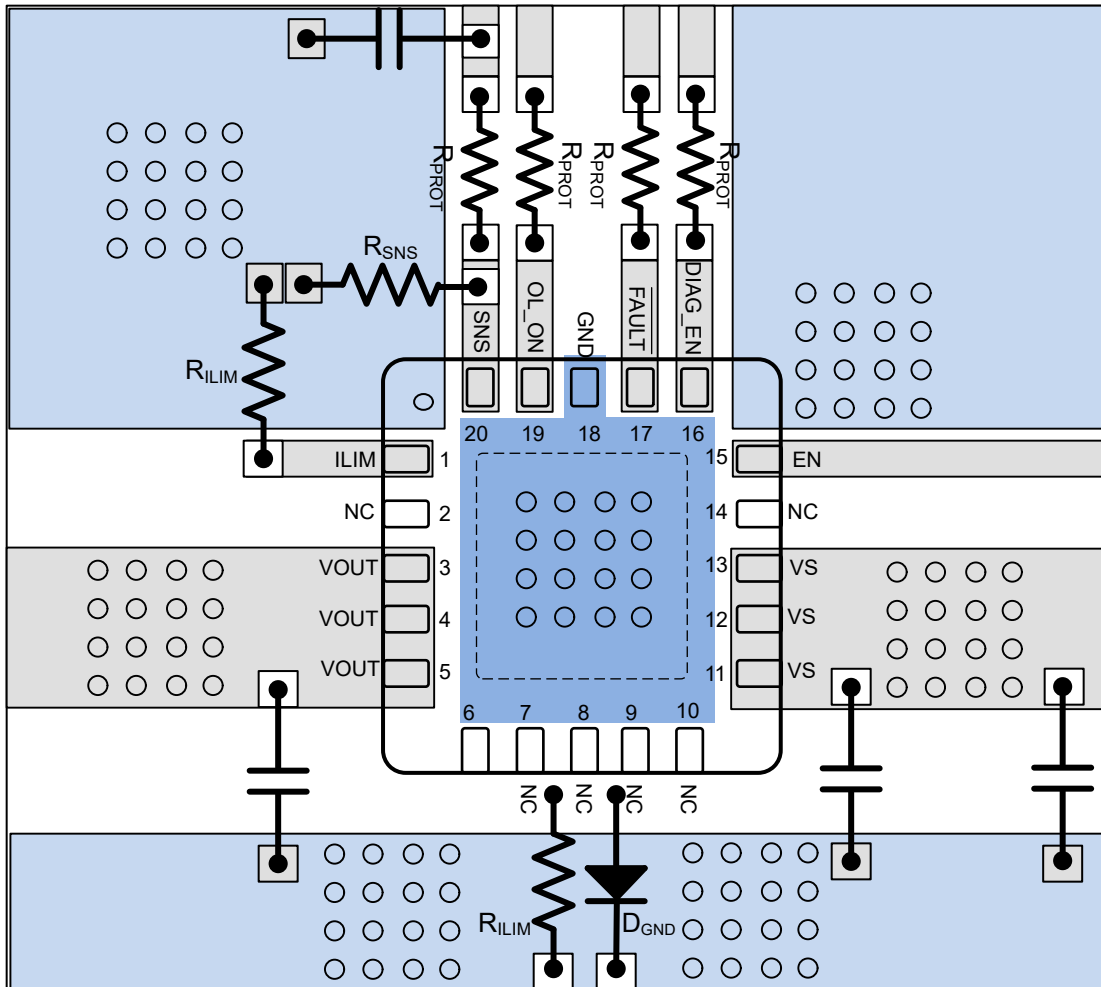


Figure 9-4. RGW Layout With a GND Network

### 9.4.3 Thermal Considerations

This device possesses thermal shutdown (TABS) circuitry as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal-shutdown trip point, the output turns on again.

Calculate the power dissipated by the device according to [Equation 13](#).

$$P_T = I_{OUT}^2 \times R_{DS(on)} + V_S \times I_{NOM} \quad (12)$$

where

- $P_T$  = Total power dissipation of the device

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (13)$$

For more information please see [How to Drive Resistive, Inductive, Capacitive, and Lighting Loads](#).

## 10 Device and Documentation Support

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision A (June 2023) to Revision B (August 2024) Page

- Added variant TPS281C30E to the data sheet..... 1

### Changes from Revision \* (December 2022) to Revision A (June 2023) Page

- Updated device status from preview to production data ..... 1

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS281C30ARGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28C30A	<a href="#">Samples</a>
TPS281C30BRGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28C30B	<a href="#">Samples</a>
TPS281C30CRGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28C30C	<a href="#">Samples</a>
TPS281C30DRGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28C30D	<a href="#">Samples</a>
TPS281C30ERGWR	ACTIVE	VQFN	RGW	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	28C30E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS281C30ARGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS281C30BRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS281C30CRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS281C30DRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS281C30ERGWR	VQFN	RGW	20	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS281C30ARGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS281C30BRGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS281C30CRGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS281C30DRGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS281C30ERGWR	VQFN	RGW	20	5000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

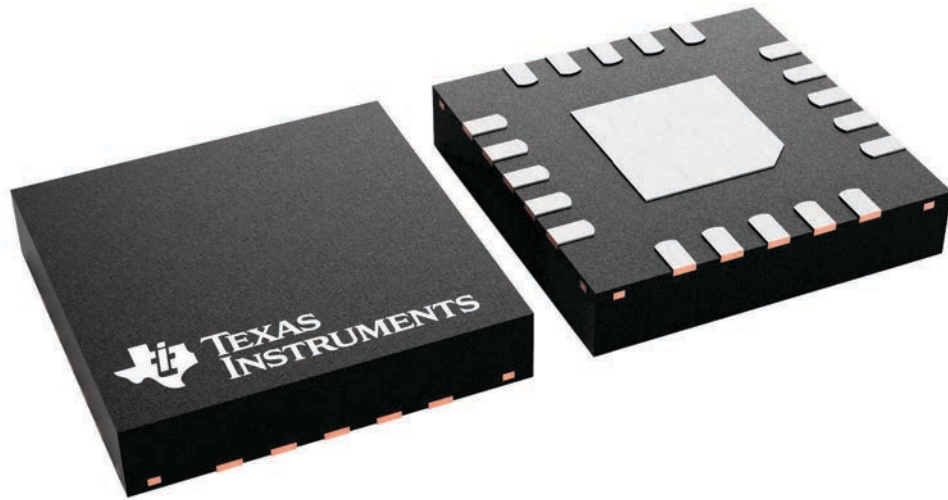
**RGW 20**

**VQFN - 1 mm max height**

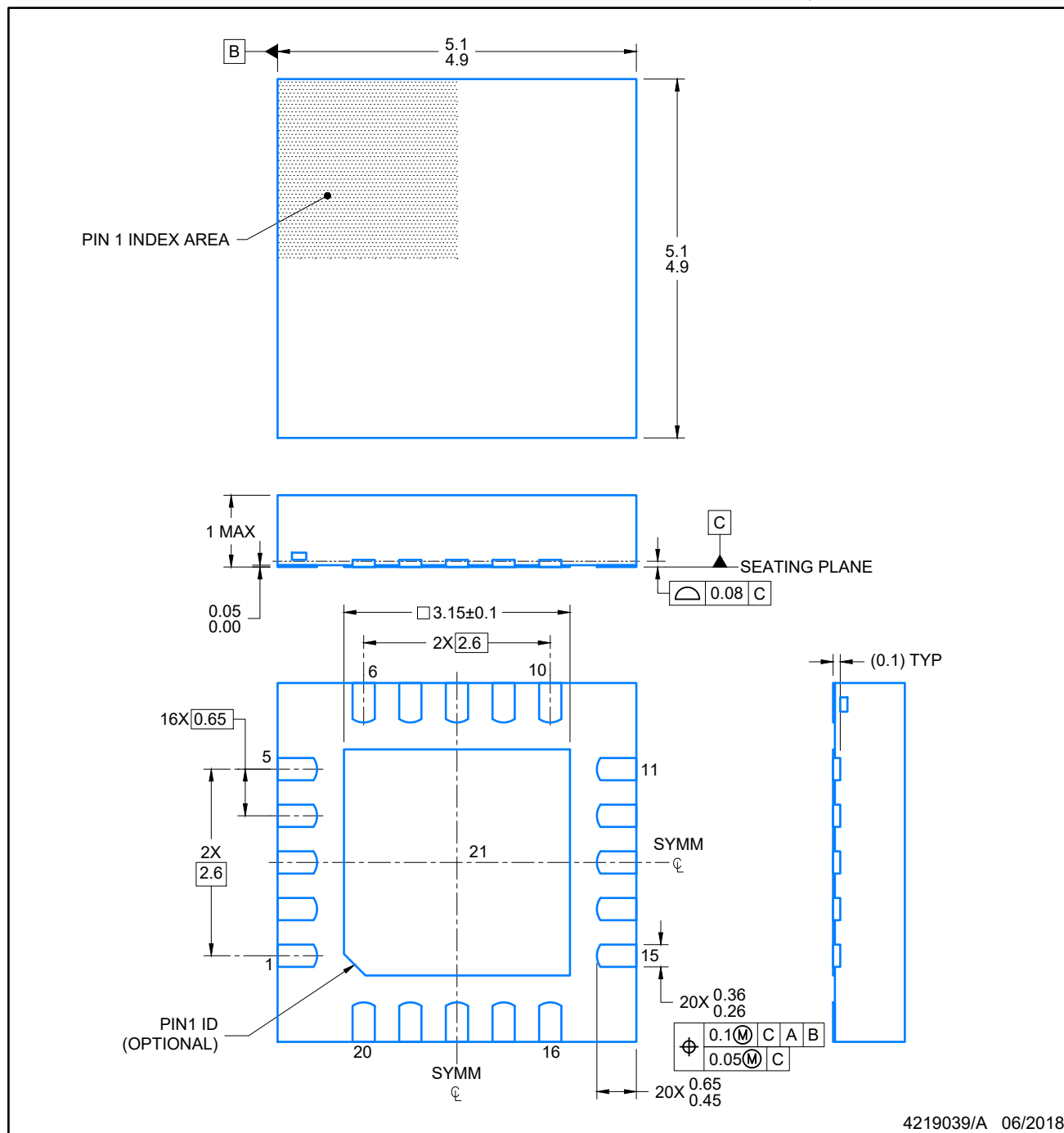
5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



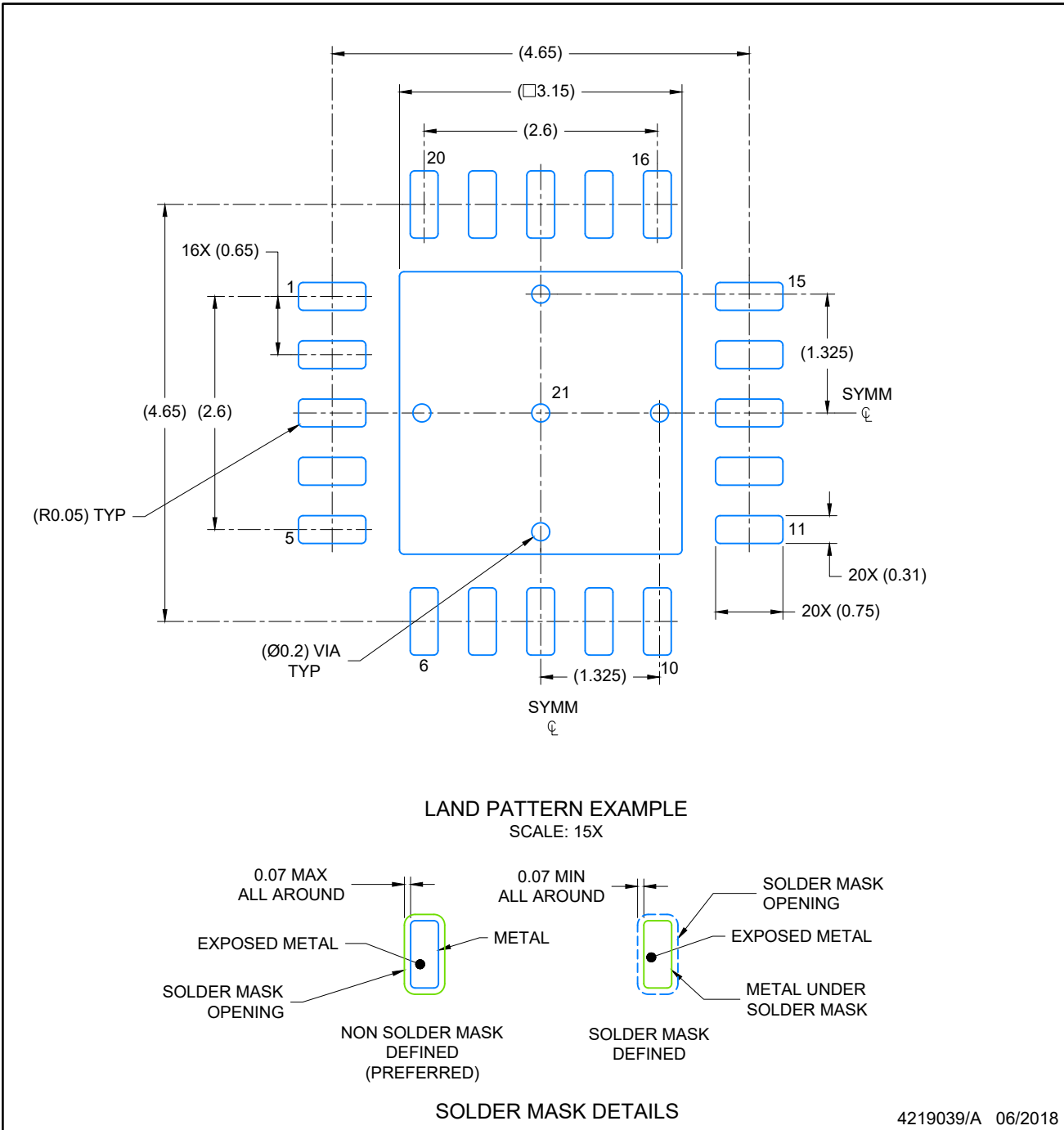
4227157/A



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.





4219039/A 06/2018

NOTES: (continued)

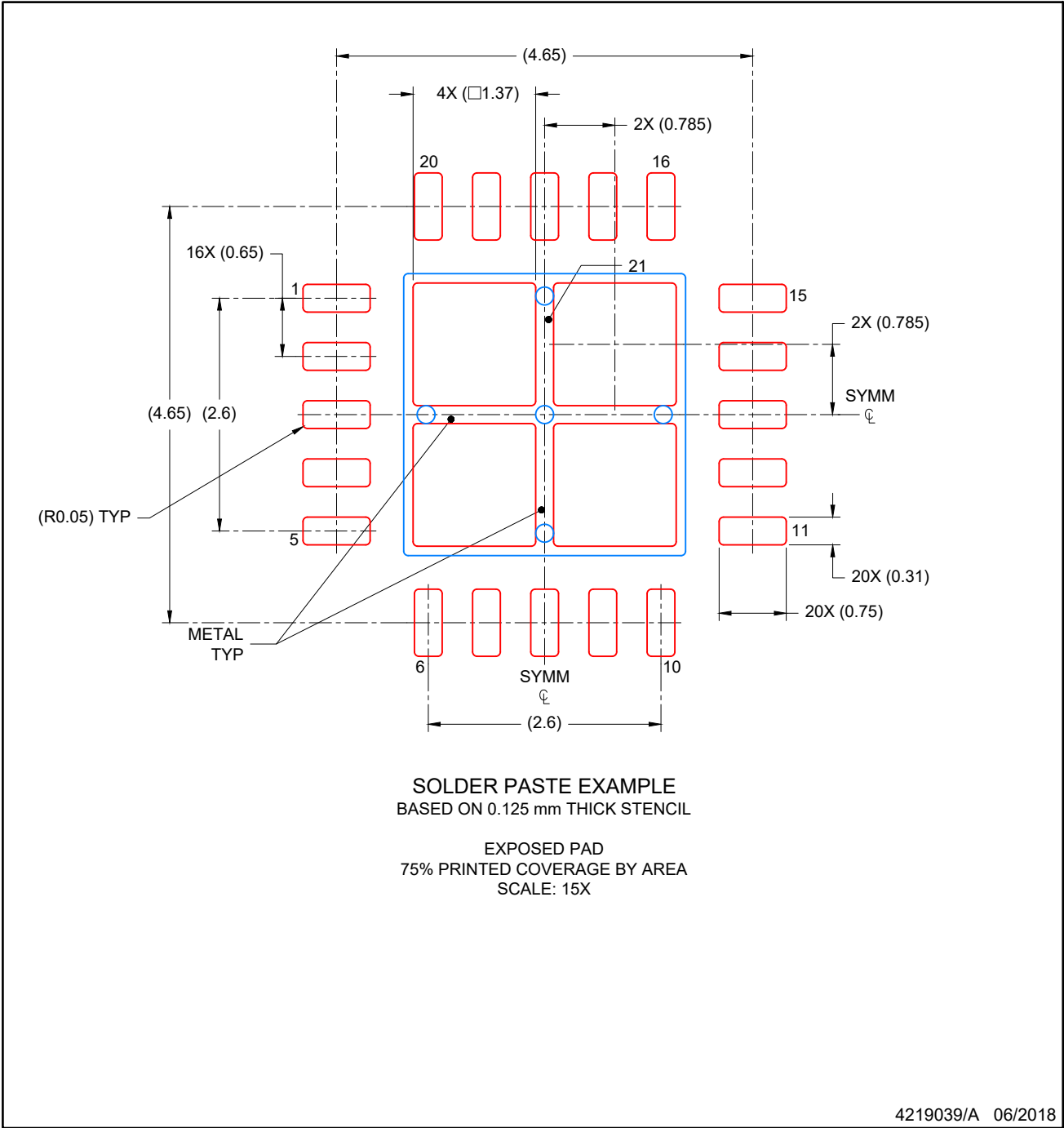
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGW0020A

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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