TPS3847 18-V, 380-nA Voltage Monitor

1 Features

- Ultralow Supply Current: 380 nA
- Wide Supply Voltage Range: 4.5 V to 18 V
- High Threshold Accuracy: ±2.5%
- Internal Hysteresis
- Push-Pull Output
- 20-ms (max) Delay Timing
- Factory-Trimmed, Fixed-Voltage Thresholds
- Specified Operating Temperature Range: –40°C to +85°C
- Operational from –40°C to +105°C
- Package: 5-Pin SOT

2 Applications

- Portable and Battery-Powered Equipment
- Desktops, Notebooks, and Ultrabooks
- Industrial Systems
- Servers
- Security Systems

3 Description

The TPS3847 family consists of wide operating voltage, ultralow-current devices that monitor the voltage at the supply pin. The device asserts an active-low reset signal whenever the VCC supply voltage drops below the factory-trimmed reset threshold voltage. The reset output remains asserted for 20 ms (max) after the VCC voltage rises above the threshold voltage.

The ultralow current consumption of 380 nA combined with 18-V capability makes the TPS3847 ideal for use in low-power and portable applications.

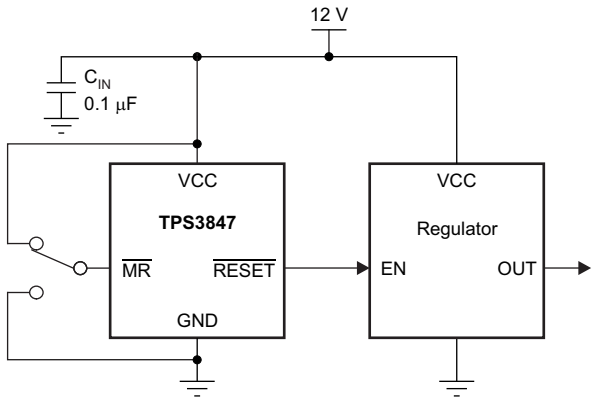
The TPS3847 features precision, factory-trimmed threshold voltages and extremely low-power operation. The TPS3847 is available in an industry-standard, 5-pin, SOT package.

Device Information(1)

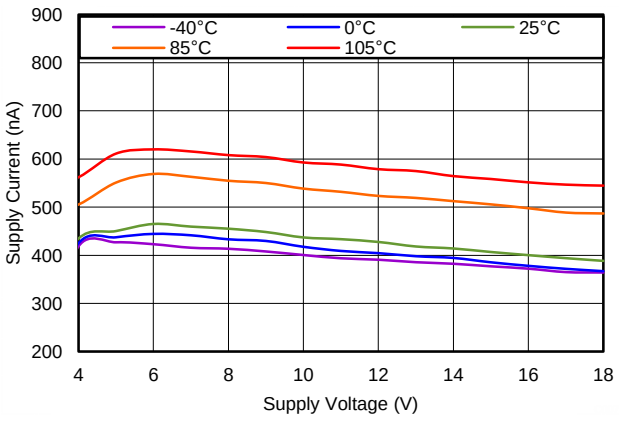
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3847	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Typical Application



Supply Current vs Supply Voltage



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2014) to Revision A **Page**

- Changed device name to reflect entire family of devices ... 1
- Changed all SOT-23 to SOT ... 1
- Changed $\overline{MR}$ maximum specification in *Absolute Maximum Ratings* table ... 4
- Changed $V_{(\overline{MR})}$ maximum specification in *Recommended Operating Conditions* table ... 4
- Deleted maximum value for C_{IN} in *Recommended Operating Conditions* ... 4
- Changed conditions of *Electrical Characteristics* table: added condition for typical values ... 5
- Added new row to V_{IT-} for TPS3847108 in *Electrical Characteristics* ... 5
- Added new row to V_{HYS} for TPS3847108 in *Electrical Characteristics* ... 5
- Added maximum specification to second row of V_{OL} parameter in *Electrical Characteristics* table ... 5
- Changed V_{OH} test conditions to I_{OH} = *2 mA* in *Electrical Characteristics* table ... 5
- Added conditions to *Timing Requirements* table ... 6
- Changed $t_{d(START)}$ maximum specification in *Timing Requirements* table ... 6
- Added condition to Figure 2 ... 7
- Changed Y-axis in Figure 12 ... 10
- Changed title of *Typical Application* section ... 12

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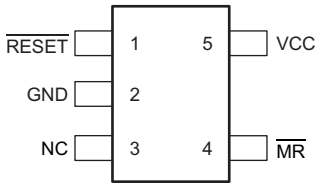
5 Pin Configuration and Functions

DBV Package
5-Pin SOT
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
$\overline{MR}$	4	I	Manual reset. Pull this pin to a logic low to force the $\overline{RESET}$ output low regardless of the voltage on VCC. After the $\overline{MR}$ pin is pulled to a logic high, the $\overline{RESET}$ output goes high after the $\overline{RESET}$ delay time (t_d) if the voltage on VCC is higher than the positive-going threshold voltage.
NC	3	—	No internal connection.
$\overline{RESET}$	1	O	Active low reset output. $\overline{RESET}$ stays low as long as the voltage on VCC is below the factory trimmed threshold voltage. $\overline{RESET}$ transitions from low to high once the VCC voltage is above the positive-going threshold voltage for a specified time (t_d). $\overline{RESET}$ is a push-pull output.
VCC	5	I	Power supply and monitored voltage. TI recommends adding a small 0.1-µF bypass capacitor near the VCC pin.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	VCC	–0.3	+20	V
	$\overline{MR}$	–0.3	VCC + 0.3	V
	$\overline{RESET}$	–0.3	+5.5	V
Current	$\overline{RESET}$		10	mA
Temperature(2)	Operating junction, T_J	–40	+105	°C
	Storage, T_{stg}	–65	+150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that the junction temperature is equal to the ambient temperature.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(VCC)}$	Power supply voltage	4.5		18	V
$V_{(\overline{MR})}$	$\overline{MR}$ pin voltage	0	1.2	VCC	V
$V_{(\overline{RESET})}$	$\overline{RESET}$ pin voltage	0		5	V
$I_{(\overline{RESET})}$	$\overline{RESET}$ pin current	0		2	mA
C_{IN}	Input capacitor	0	0.1		µF
T_J	Junction temperature	–40	+25	+85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS3847 DBV (SOT) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	208.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	
ψ_{JT}	Junction-to-top characterization parameter	14.6	
ψ_{JB}	Junction-to-board characterization parameter	36.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

At T_J = –40°C to +85°C, 4.5 V < V_{CC} < 18 V, and C_{IN} = 0.1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
$V_{(VCC)}$	Input supply voltage range			4.5		18	V
V_{VO}	Minimum $V_{(VCC)}$ voltage for valid output(1)	I_{OL} = 1 µA, V_{OL} = 400 mV				0.8	V
$I_{(VCC)}$	Supply current (into VCC pin)	Output not connected	T_J = 25°C, $V_{(VCC)}$ = 18 V		380		nA
			T_J = 25°C			750	nA
			–40°C ≤ T_J ≤ +85°C			900	nA
MONITORED THRESHOLD							
$V_{IT–}$	Negative going input threshold accuracy	T_J = 25°C			±0.5%		
				–2.5%		+2.5%	
	Negative-going threshold voltage	TPS3847085		8.2875	8.5	8.7125	V
		TPS3847108		10.53	10.8	11.07	V
V_{HYS}	Hysteresis voltage	TPS3847085			0.11 × $V_{IT–}$		V
		TPS3847108			0.035 × $V_{IT–}$		V
OUTPUT							
V_{OL}	Push-pull low-level output voltage ($\overline{RESET}$)	0.9 V < $V_{(VCC)}$ < 2.4 V, I_{OL}= 10 µA			0.009	0.4	V
		2.4 V ≤ $V_{(VCC)}$ < 4.5 V, I_{OL}= 250 µA			0.015	0.4	V
		4.5 V ≤ $V_{(VCC)}$ ≤ 18 V, I_{OL}= 2 mA			0.09	0.4	V
V_{OH}	Push-pull high-level output voltage ($\overline{RESET}$)	I_{OH} = –2 mA		1.6		3.1	V
			$V_{(VCC)}$ = 18 V		2.45		V
		I_{OH} = –10 µA		3		4	V
			$V_{(VCC)}$ = 18 V		3.55		V
$\overline{MR}$ PIN							
V_{IL}	Low-level input voltage					0.4	V
V_{IH}	High-level input voltage			1.2			V
$I_{lkg(MR)}$	$\overline{MR}$ leakage current	$\overline{MR}$ High, $V_{(VCC)}$ = 18 V			–23		nA

(1) The lowest supply voltage ($V_{(VCC)}$) at which $\overline{RESET}$ is valid. $t_{RISE(VCC)}$ ≥ 15 µs/V, where t_{RISE} is the rise time.

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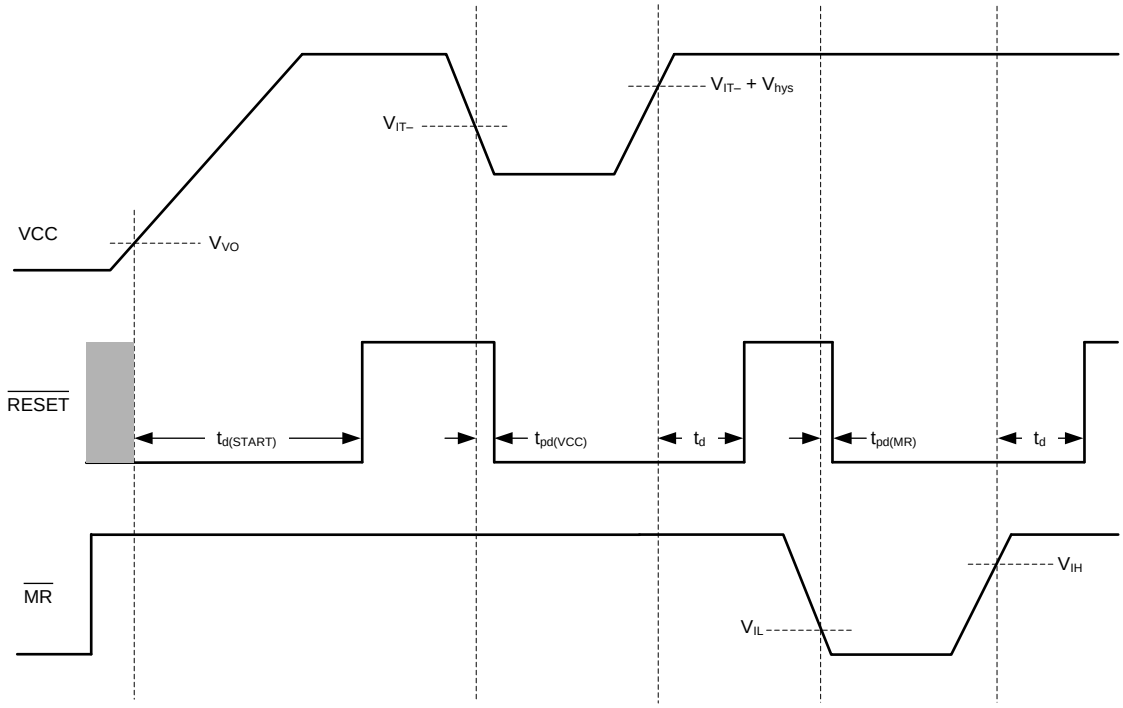
6.6 Timing Requirements

At T_J = –40°C to +85°C, 4.5 V < VCC < 18 V, and C_{IN} = 0.1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		MIN	TYP	MAX	UNIT
t_d	$\overline{\text{RESET}}$ delay time(1)		4.5	20	ms
$t_{d(START)}$	Startup delay time(2)		6.5	40	ms
$t_{pd(VCC)}$	Propagation delay for VCC falling(3)		55		µs
$t_{pd(MR)}$	Propagation delay $\overline{\text{MR}}$ falling(4)		50		µs
$t_{P(MR)}$	$\overline{\text{MR}}$ minimum high to low pulse duration for $\overline{\text{RESET}}$ low		50		µs

(1) Delay from when $V_{(VCC)} \geq V_{IT-}$ or $V_{MR} \geq V_{IH}$ until $\overline{\text{RESET}}$ goes high when $V_{(VCC)}$ starts from above the specified minimum $V_{(VCC)}$. Measured with 5% overdrive.
(2) When $V_{(VCC)}$ starts from less than the specified minimum $V_{(VCC)}$ and then exceeds V_{th}, $\overline{\text{RESET}}$ goes high after the startup delay ($t_{d(START)}$) instead of the $\overline{\text{RESET}}$ delay time (t_d). Measured with 5% overdrive.
(3) Delay from $V_{(VCC)} < V_{th}$ until $\overline{\text{RESET}}$ goes low. Measured with 8% overdrive.
(4) Delay from $V_{MR} < V_{IL}$ until $\overline{\text{RESET}}$ goes low. Measured with 8% overdrive.



Timing Diagram

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6.7 Typical Characteristics

At $V_{(VCC)}$ = 18 V, $\overline{MR}$ = 1.2 V, $\overline{RESET}$ = open, and C_{IN} = 0.1 µF (unless otherwise noted).

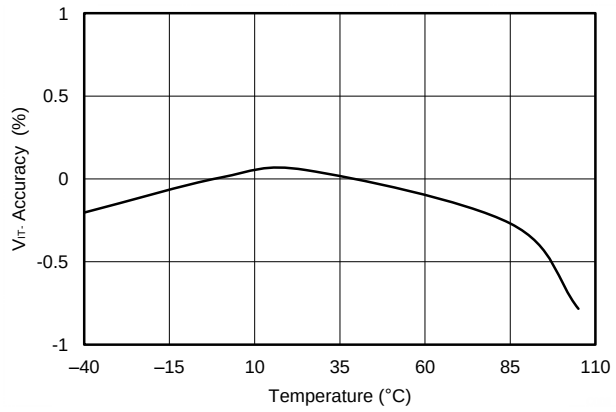

Figure 1. Negative-Going Threshold Accuracy vs Temperature

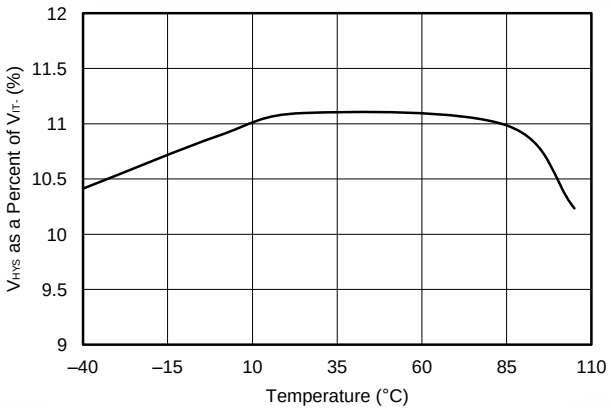

Figure 2. Hysteresis vs Temperature

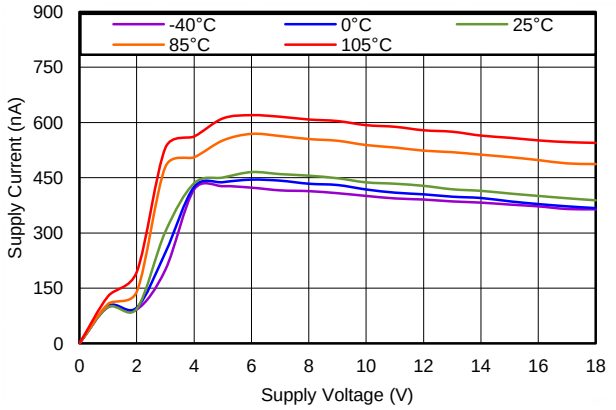

Figure 3. Supply Current vs $V_{(VCC)}$ and Temperature

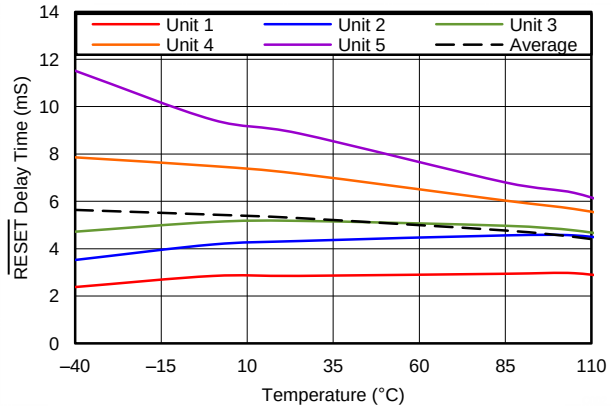

Figure 4. $\overline{RESET}$ Delay Time vs Temperature Distribution

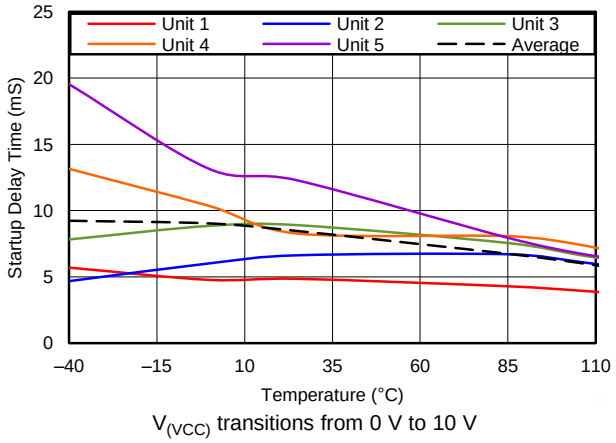

Figure 5. Startup Delay Time vs Temperature Distribution

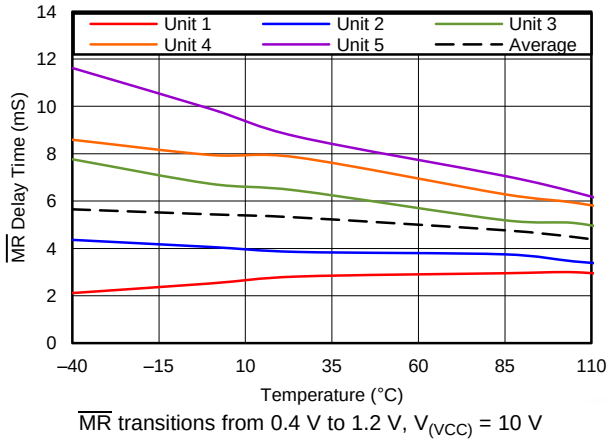

Figure 6. $\overline{MR}$ Delay Time vs Temperature Distribution

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Typical Characteristics (continued)

At $V_{(VCC)}$ = 18 V, $\overline{MR}$ = 1.2 V, $\overline{RESET}$ = open, and C_{IN} = 0.1 µF (unless otherwise noted).

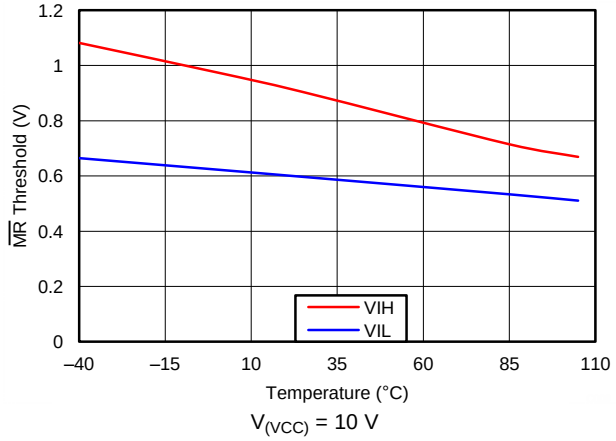

Figure 7. $\overline{MR}$ Threshold vs Temperature

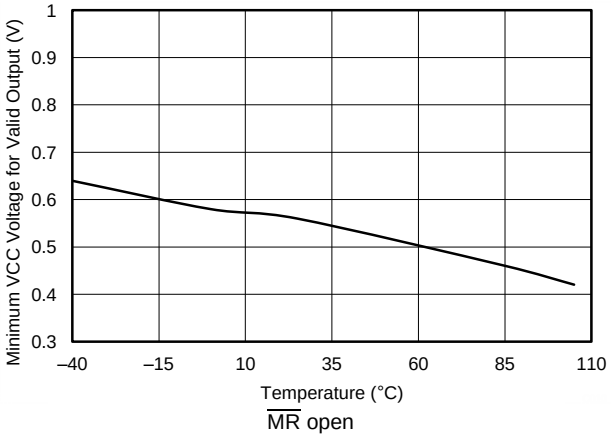

Figure 8. Minimum $V_{(VCC)}$ for Valid Output vs Temperature

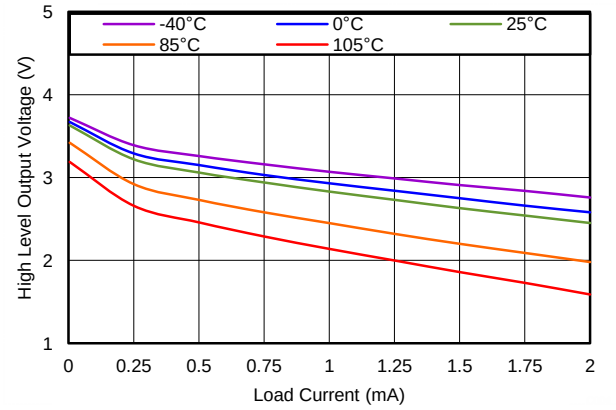

Figure 9. High-Level Output Voltage vs Load Current

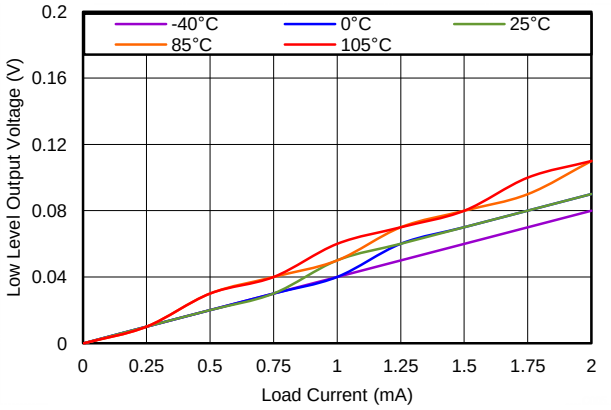

Figure 10. Low-Level Output Voltage vs Load Current

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7 Detailed Description

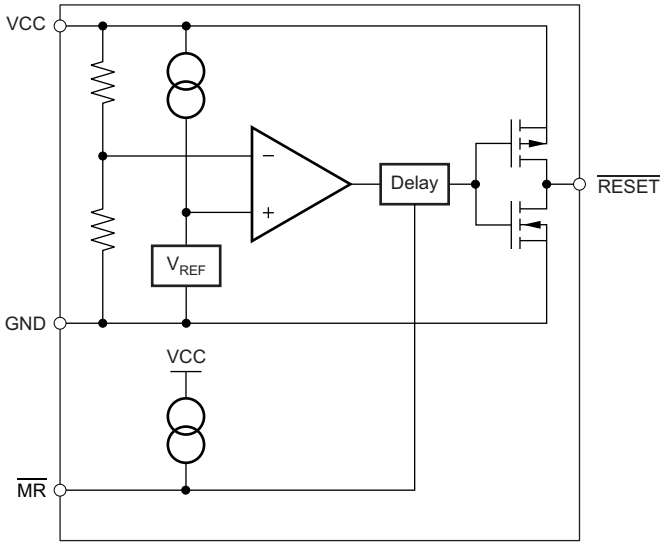
7.1 Overview

The TPS3847 is a family of ultralow-current supervisors for high-voltage applications that are specified from –40°C to +85°C and operational up to 105°C (see the *Typical Characteristics* section for typical –40°C to +105°C performance).

The $\overline{\text{RESET}}$ output goes low after the power-supply voltage ($V_{(VCC)}$) drops below the negative-going input threshold voltage ($V_{IT–}$), and after the VCC falling propagation delay ($t_{pd(VCC)}$) elapses. When $V_{(VCC)}$ rises above the positive-going reset threshold (V_{IT+}), which is the negative-going threshold voltage plus the hysteresis ($V_{IT–}$ + V_{hys}), $\overline{\text{RESET}}$ outputs a high signal after the reset delay time (t_d) elapses.

The TPS3847 also features a manual reset pin ($\overline{\text{MR}}$) that allows a processor, or other logic devices, to initiate a reset, even when $V_{(VCC)}$ exceeds $V_{IT–}$. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to transition to logic low after the $\overline{\text{MR}}$ propagation delay ($t_{pd(MR)}$) elapses. When $\overline{\text{MR}}$ returns to a logic high and $V_{(VCC)}$ exceeds V_{IT+}, $\overline{\text{RESET}}$ transitions to logic high after t_d elapses.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Ultralow Supply Current

The TPS3847 uses a unique sampling scheme to maintain an extremely-low average quiescent current of 380 nA. This low quiescent current is ideal for applications that require extremely-low power consumption.

7.3.2 Wide Supply Range

This device has an operational input supply range of 4.5 V to 18 V, allowing for a wide range of applications. This wide supply range is ideal for applications that have either large transients or high dc voltage supplies.

7.3.3 High-Accuracy Negative Threshold

The TPS3847 has a negative threshold accuracy of ±2.5% and uses well-controlled and matched internal resistors to set the threshold voltage in order to eliminate the inaccuracies because of the external resistors. Unlike The TPS3847, voltage supervisors that require external resistors to set the threshold voltage always add inaccuracy to the specified performance.

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Feature Description (continued)

7.3.4 Push-Pull Output

The TPS3847 has a push-pull output stage that covers many of the common digital logic levels. Push-pull outputs simplify many designs compared to open-drain output devices because push-pull outputs do not require a pull-up resistor or an additional low-voltage rail. Compared to open-drain output devices, push-pull devices reduce power consumption when the output is low because open-drain devices sink current through the pull-up resistor to ground in order to create the logic-low signal.

7.3.5 Manual Reset ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a processor, or other logic devices, to initiate a reset even when the voltage on VCC is greater than V_{IT-}. A logic low on $\overline{MR}$ causes $\overline{RESET}$ to output a logic low. After $\overline{MR}$ returns to a logic high and the power-supply voltage is greater than V_{IT+}, $\overline{RESET}$ transitions to logic high after the reset delay time (t_d) elapses.

7.3.6 VCC Transient Rejection

The TPS3847 has built-in rejection of fast transients on the VCC pin. Transient rejection depends on both the duration and overdrive, or amplitude, of the transient. Overdrive of the transient is measured from the bottom of the transient to the negative threshold voltage (V_{IT-}) of the device, as shown in Figure 11.

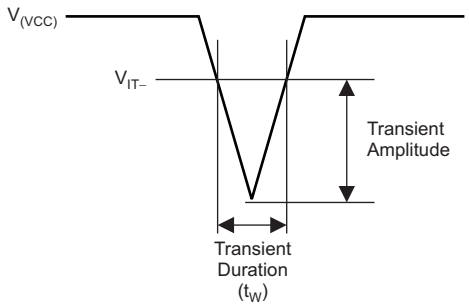

Figure 11. Voltage Transient Measurement

Figure 12 shows the relationship between the overdrive and the duration required to trigger a reset. Any combination of duration and amplitude greater than that shown in Figure 12 generates a reset signal.

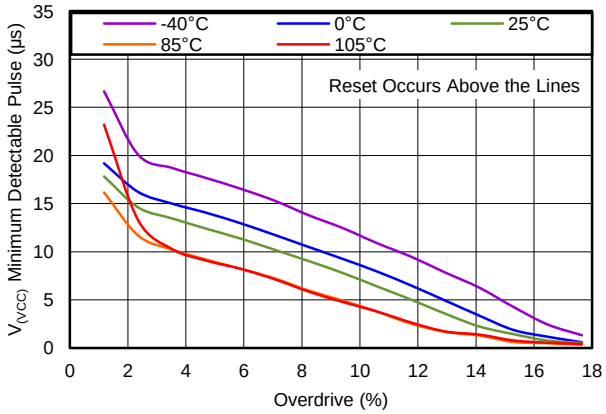

Figure 12. Minimum Detectable Pulse on VCC vs Overdrive

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Feature Description (continued)

7.3.7 Controlled Startup Current

The input supply current of the TPS3847 is very well controlled, including during startup. Some low-current devices exhibit spikes in the supply current before reaching the minimum supply voltage; this type of startup behavior can cause problems in some applications. Figure 13 shows that there are no spikes in supply current, and the device is well controlled all the way from 0 V to minimum $V_{(VCC)}$.

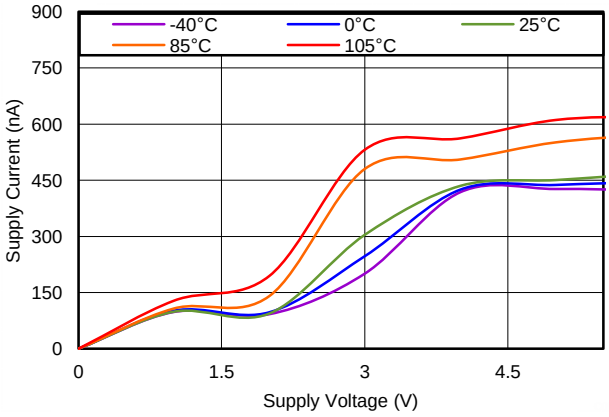

Figure 13. Supply Current During Startup

7.3.8 Low Minimum Supply Voltage for Valid Output

The TPS3847 is designed to have a valid $\overline{\text{RESET}}$ signal, even with a low input supply voltage. Figure 14 shows that even at –40°C, the TPS3847 typically has a valid output with only 0.65 V on the input supply; at 105°C, that input supply voltage goes down to less than 0.45 V.

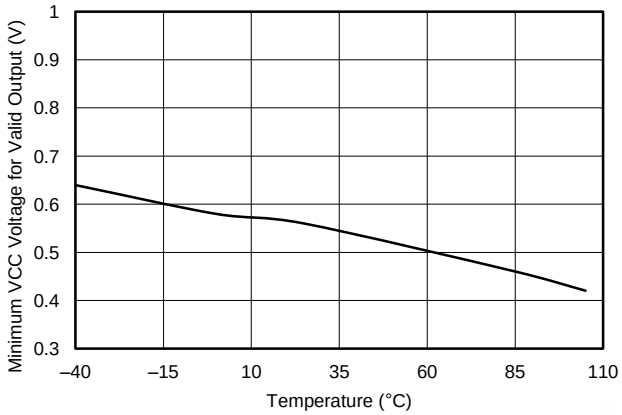

Figure 14. Minimum Supply Voltage for Valid Output vs Temperature

7.4 Device Functional Modes

The TPS3847 has two functional modes:

1. $\overline{\text{MR}}$ high: in this mode, $\overline{\text{RESET}}$ is high or low depending on the value of $V_{(VCC)}$ relative to $V_{IT–}$.
2. $\overline{\text{MR}}$ low: in this mode, $\overline{\text{RESET}}$ is held low regardless of the value of $V_{(VCC)}$.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS3847 family consists of wide-operating voltage, ultralow-current devices that monitor the power-supply voltage. The device asserts an active-low reset signal whenever the supply voltage drops below the factory-trimmed reset. The ultralow current consumption of 380 nA combined with 18-V capability makes the TPS3847 ideal for use in low-power and portable applications.

8.2 Typical Application

Wide operating voltage and threshold options make the TPS3847 well suited for monitoring dual- and triple-cell, lithium-ion battery applications. Figure 15 shows the TPS3847 used to disable a buck converter when the cell voltage discharges below the threshold voltage. When the cell voltage reaches V_{IT-}, the enable pin of the TPS62120 is driven low, placing the buck converter in a low-current, shutdown state.

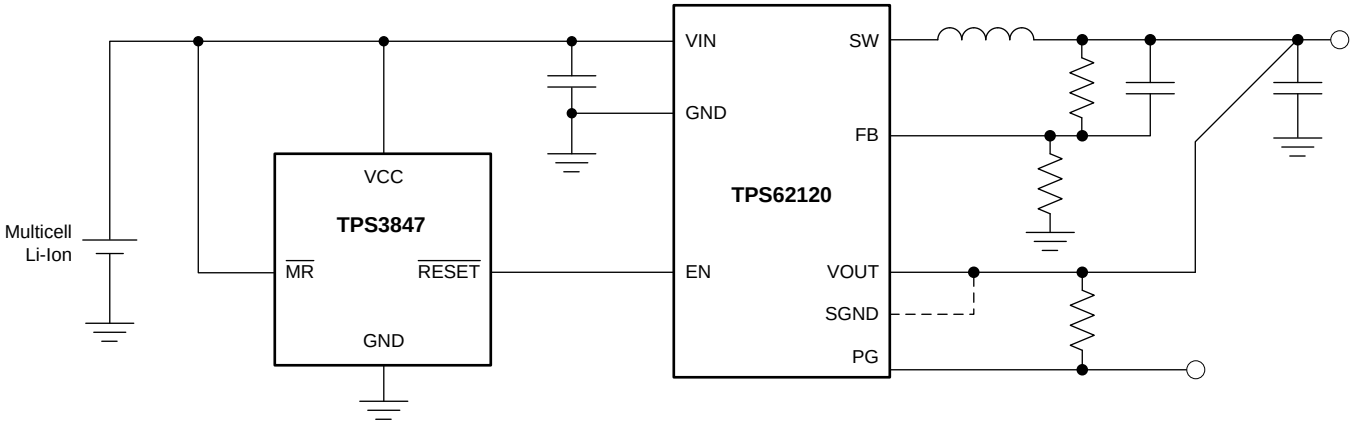

Figure 15. Disabled Buck Converter

8.2.1 Design Requirements

8.2.1.1 Input Capacitor

The TPS3847 uses a unique sampling scheme to maintain an extremely low average quiescent current of 380 nA. However, this current rises to approximately 12 µA for approximately 500 µs while the TPS3847 refreshes the reference voltage. This refresh pulse typically occurs every 200 ms. If the source impedance to the supply voltage is high, then the additional current during sampling may trigger a false reset as a result of the voltage drop from the supply to the VCC pin. For sources with a high impedance, or applications with long or thin VCC traces, add a 0.1-µF or larger bypass capacitor near the VCC pin. Adding this bypass capacitor effectively keeps the average current supplied from the input source close to 380 nA, reducing the voltage droop caused by the refresh pulse, and is good analog design practice.

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Typical Application (continued)

8.2.1.2 Driving Bidirectional Reset Pins

Some microcontrollers have bidirectional reset pins that act as both an input and an output. When using bidirectional reset pins, place a series resistor between the TPS3847 $\overline{\text{RESET}}$ pin and the microcontroller in order to protect against excessive current flow in case both the TPS3847 and the microcontroller attempt to drive the reset line simultaneously. Figure 16 illustrates the connection of the TPS3847 to a microcontroller using a series resistor to drive a bidirectional reset line. Assuming the maximum voltage that the microprocessor outputs is the same as the TPS3847 (4 V), use a resistor value greater than 20 kΩ in order to limit the output current to 2 mA or less when one pin is driven high and the other is driven low. In order to cover the majority of applications, use a resistor value of 47 kΩ.

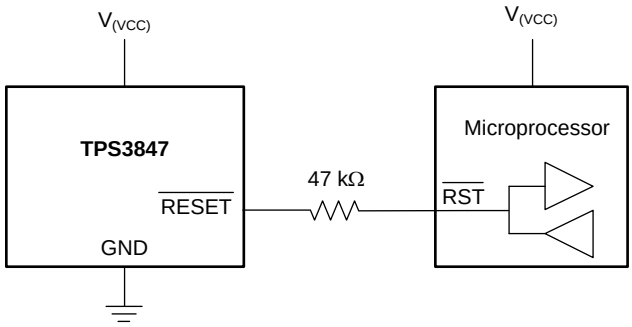

Figure 16. Connection to Bidirectional Reset Pin

8.2.1.3 Manual Reset ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor, or other logic devices, to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to transition to logic low. After $\overline{\text{MR}}$ returns to a logic high and $V_{(VCC)}$ is greater than V_{IT+}, $\overline{\text{RESET}}$ transitions to a logic high after the reset delay time, t_d, elapses.

Note that internal to the device $\overline{\text{MR}}$ is connected to a very small current source that goes from the internal sub-regulated voltage to the $\overline{\text{MR}}$ node. If the logic signal driving $\overline{\text{MR}}$ does not exceed 3 V, there is 25 nA of additional current drawn from the input supply because of this current source. Do not leave this pin floating; either drive this pin above or below the $\overline{\text{MR}}$ high and low input levels. Tie $\overline{\text{MR}}$ directly to VCC if not used.

8.2.1.4 Threshold Overdrive

Threshold overdrive is how much $V_{(VCC)}$ exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the $\overline{\text{RESET}}$ response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1:

$$\text{Overdrive} = |(V_{(VCC)} / V_{IT} - 1) \times 100\%| \quad (1)$$

where:

- V_{IT} is either V_{IT-} or V_{IT+}, depending on whether calculating the overdrive for the negative-going threshold or the positive-going threshold, respectively.

Figure 12 illustrates the VCC minimum detectable pulse versus overdrive, and is used to visualize the relationship overdrive has on $t_{pd(VCC)}$ for negative-going events.

For positive-going events, after the overdrive is greater than 5%, the changes to t_d are negligible because of the significantly longer delay time. When overdrive is less than 5%, t_d can increase to 200 ms while the device waits for the next voltage reference refresh pulse.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

- Select desired device based on the threshold voltage.
- Ensure that the trace from the input supply to the VCC pin is low impedance in order to avoid false reset signals during the refresh cycle. If the impedance is too high, add an input capacitor of 0.1-µF or larger close to the VCC pin (see the *Input Capacitor* section).
- If the $\overline{\text{RESET}}$ of the TPS3847 is driving a bidirectional pin, place a resistor between the output of the TPS3847 and the bidirectional pin (see the *Driving Bidirectional Reset Pins* section).

8.2.3 Application Curves

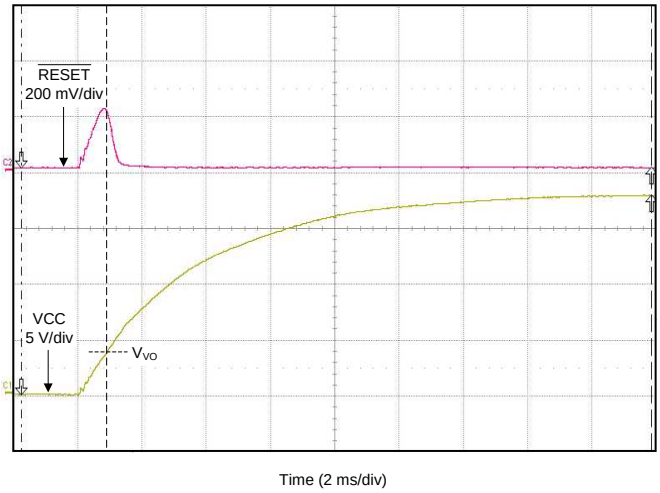

Figure 17. Startup Showing Minimum $V_{(VCC)}$ for Valid Output

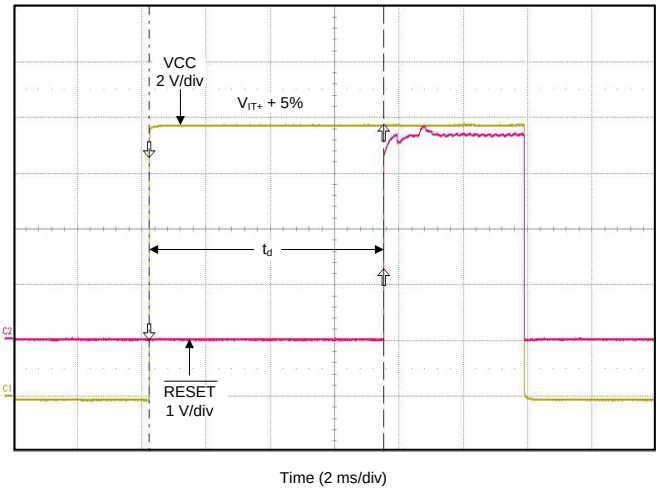

Figure 18. Startup Delay Time

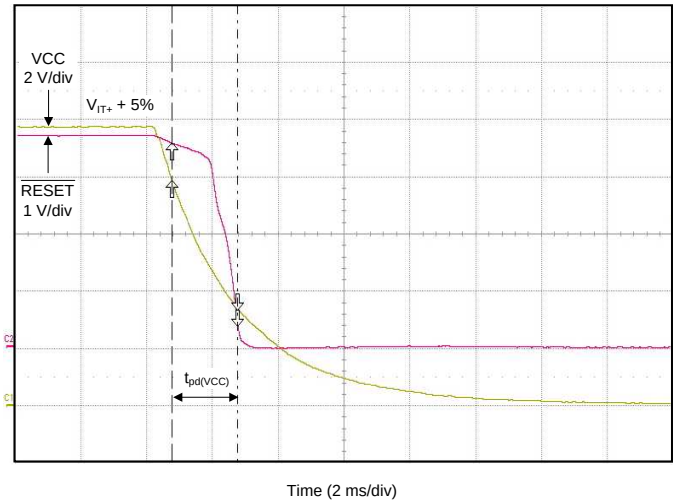

Figure 19. Propagation Delay Time

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8.3 Do's and Don'ts

Connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor between the VCC pin and the GND pin.

Connect the $\overline{MR}$ pin to a voltage higher than 1.2 V in order for $\overline{RESET}$ to go high or low, depending on the value of $V_{(VCC)}$ relative to V_{IT-}.

Connect the $\overline{MR}$ pin to a voltage lower than 0.4 V in order to hold $\overline{RESET}$ low, regardless of the value of $V_{(VCC)}$.

Connect the $\overline{MR}$ pin to the VCC pin if $\overline{MR}$ functionality is not used.

Do not connect the VCC pin to a high-impedance supply without a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) bypass capacitor.

Do not use a thin, long trace to connect the VCC pin to the input supply without a 0.1-µF to 1.0-µF low ESR bypass capacitor.

Do not leave the $\overline{MR}$ pin floating.

9 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 4.5 V and 18 V. Use a low-impedance power supply to eliminate inaccuracies caused by the current during the voltage-reference refresh.

10 Layout

10.1 Layout Guidelines

Make sure the connection to the VCC pin is low impedance and able to carry 12 µA without a significant voltage drop. Place a 0.1-µF bypass capacitor near the VCC pin if the 12-µA current causes too much voltage droop.

10.2 Layout Example

The layout example in Figure 20 shows how the TPS3847 is laid out on a printed circuit board (PCB). Although not required, use C_{IN} for best device performance.

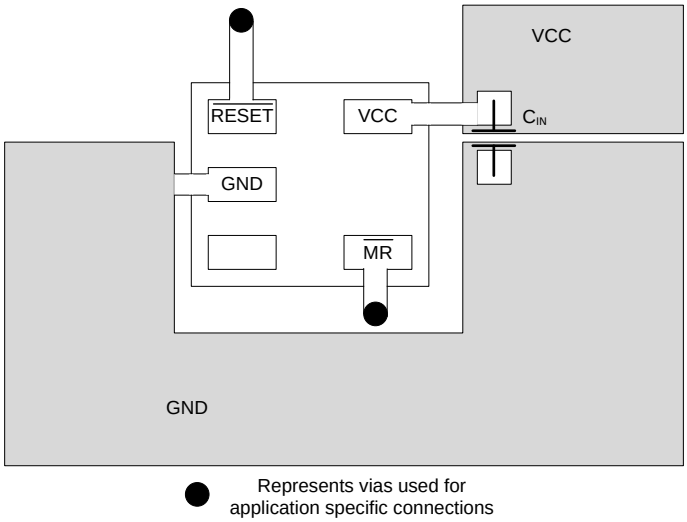

Figure 20. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

TPS3847*xxxyyy* is the generic naming convention for this device. TPS3847 represents the family of these devices, *xxx* is used to display the negative going threshold voltage and a decimal should be placed after the second number while *yyy* is reserved for the package designator.

Example: TPS3847085DBV
Family: TPS3847
Negative-Going Threshold Voltage: 8.5 V
DBV Package: 5-pin SOT

11.2 Documentation Support

11.2.1 Related Documentation

TPS3847085EVM-577 Evaluation Module User's Guide, SBVU023

TPS62120 Data Sheet, SLVSAD5

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3847085DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	PC7I	Samples
TPS3847085DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	PC7I	Samples
TPS3847108DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZBYD	Samples
TPS3847108DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZBYD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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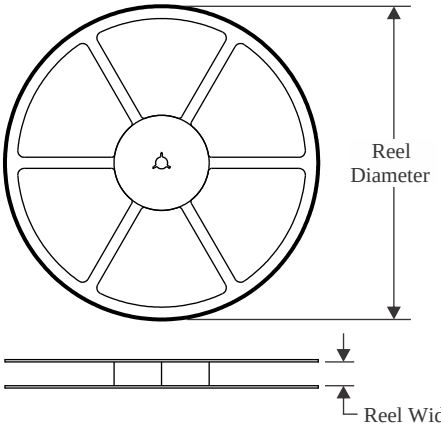
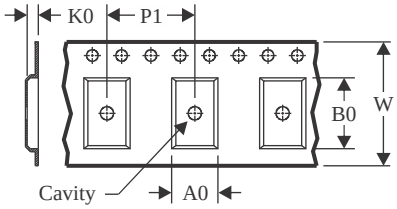
TAPE AND REEL INFORMATION

REEL DIMENSIONS

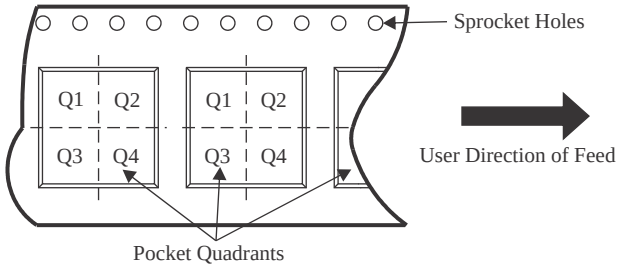


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

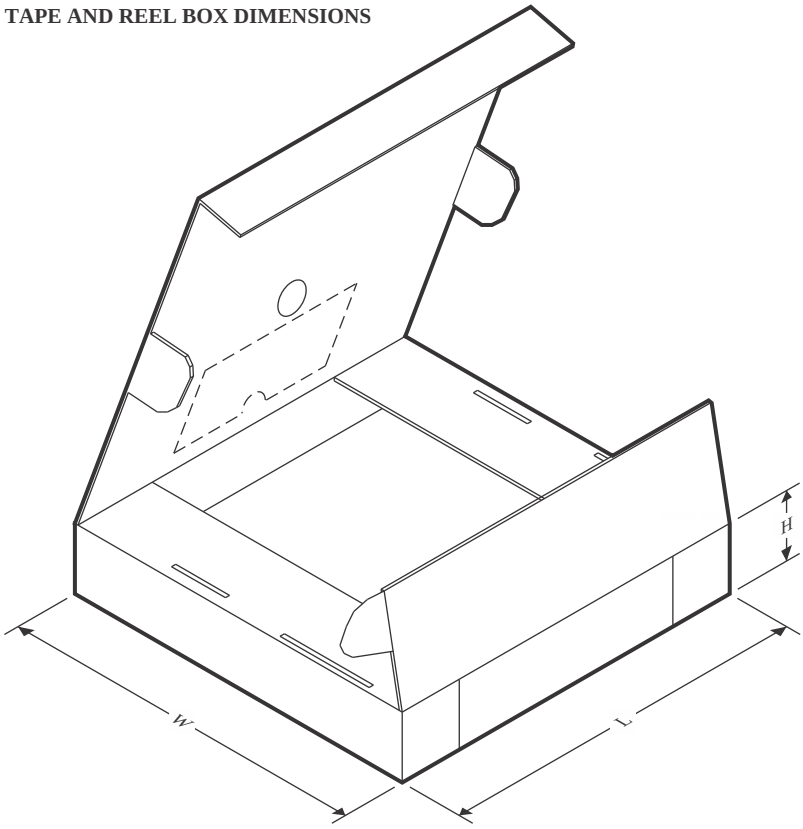
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3847085DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3847085DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS3847085DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3847108DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3847108DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3847108DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

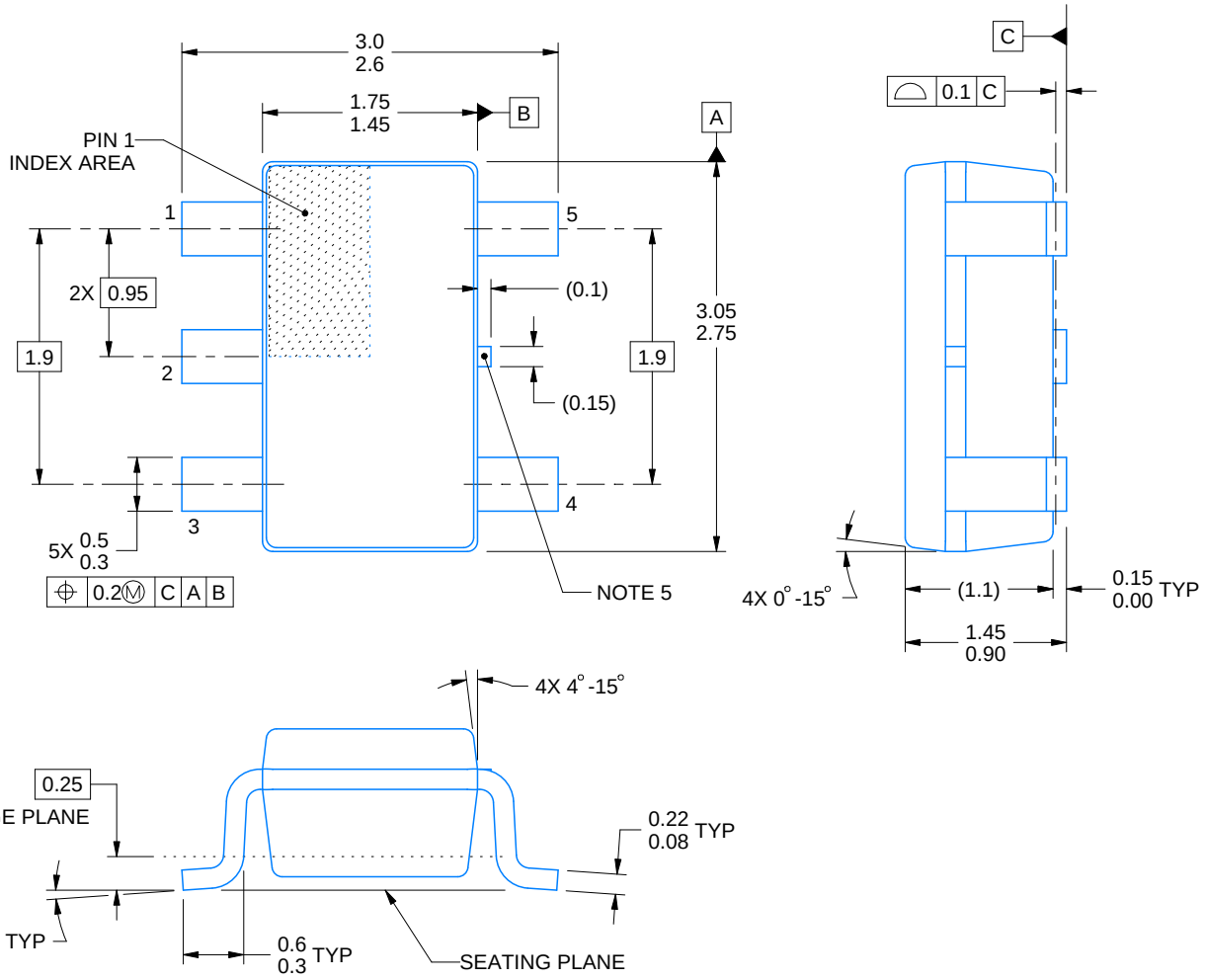
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3847085DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3847085DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3847085DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS3847108DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3847108DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS3847108DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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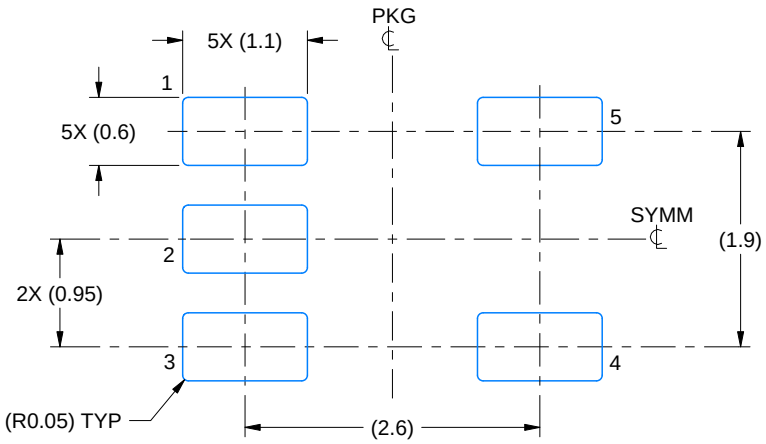
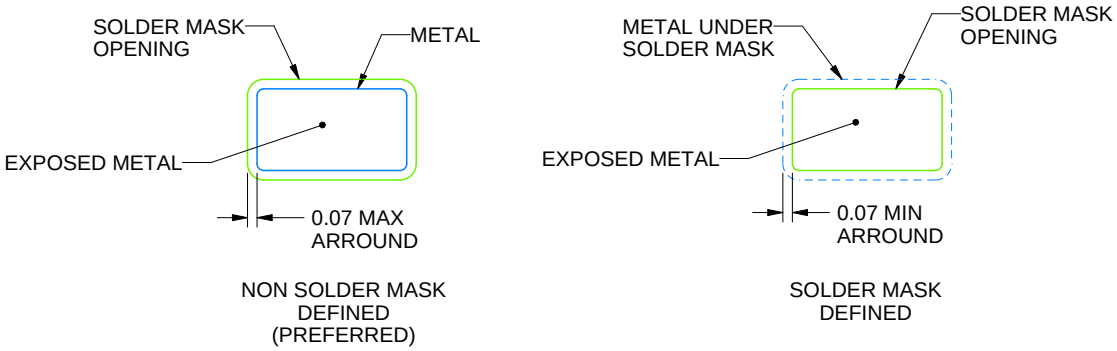
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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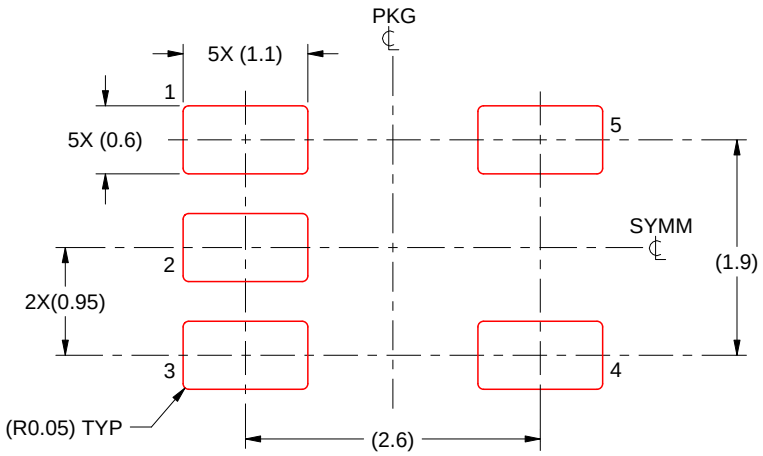
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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