TPS536C7B1 Dual-Channel D-CAP+™, Dual-Channel (N+M ≤ 12 Phases) Step-Down, Multiphase Controller with PMBus™ Interface

1 Features

- Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.25 V to 5.5 V
- Per-phase switching frequency range: 300 kHz to 2000 kHz
- Dual Output Supporting N+M Phase Configurations (N+M ≤ 12, M ≤ 6)
- PMBus v1.3.1 system interface for configuration, control and telemetry of voltage, current, power, temperature, and fault status
- Adaptive voltage scaling (AVS) through VOUT_COMMAND
- Enhanced D-CAP+ control to provide super transient performance with excellent dynamic current sharing
- Programmable loop compensation
- Flexible phase-firing order
- External pinstrap for Ch. A boot voltage settings
- Individual phase current calibrations and reporting
- Phase thermal balance management (TBM)
- Full support for dynamic phase shedding (DPS)
- Fast phase-adding for undershoot reduction (USR)
- Body-diode braking for overshoot reduction (OSR)
- Driverless Configuration for efficient high-frequency switching
- Fully Compatible with TI NexFET™ power stage for high-density solutions
- Accurate, Programmable Adaptive Voltage Positioning (AVP)
- Patented AutoBalance™ Phase Balancing
- 6 mm × 6 mm, 48-Pin, QFN Package

2 Applications

- Data center network switches
- Campus and branch switches
- Core and edge routers
- Hardware accelerator cards
- High performance CPU/ASIC/FPGA power

3 Description

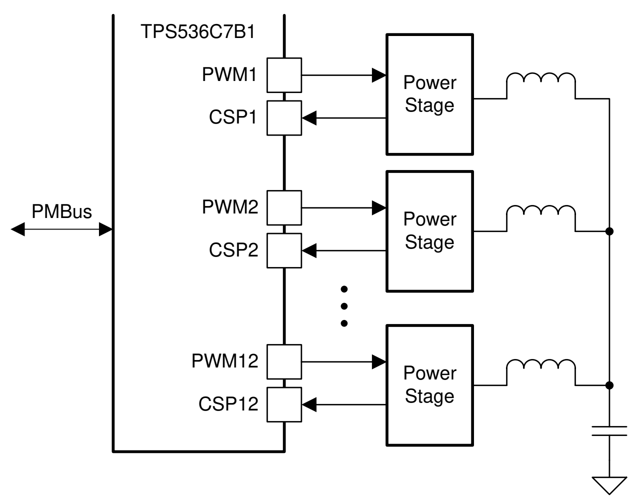
The TPS536C7B1 is a step-down controller with dual channels, built-in non-volatile memory (NVM), and PMBus interface, and is fully compatible with TI NexFET™ smart power stages. Advanced control features such as the D-CAP+ architecture provide fast transient response, low output capacitance, and good current sharing. The device also provides a novel phase interleaving strategy and flexible firing order. Adjustable control of output voltage slew rate and adaptive voltage positioning are also supported. In addition, the device supports the PMBus communication interface for reporting telemetry of voltage, current, power, temperature, and fault conditions to the system host. All programmable parameters can be configured by the PMBus interface, and can be stored in NVM as the new default values to minimize the external component count.

The TPS536C7B1 device if offered in a thermally enhanced 48-pin QFN packaged and is rated to operate from –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS536C7B1	QFN (48)	6 mm × 6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2020	*	Initial Release

5 Pin Configuration and Functions

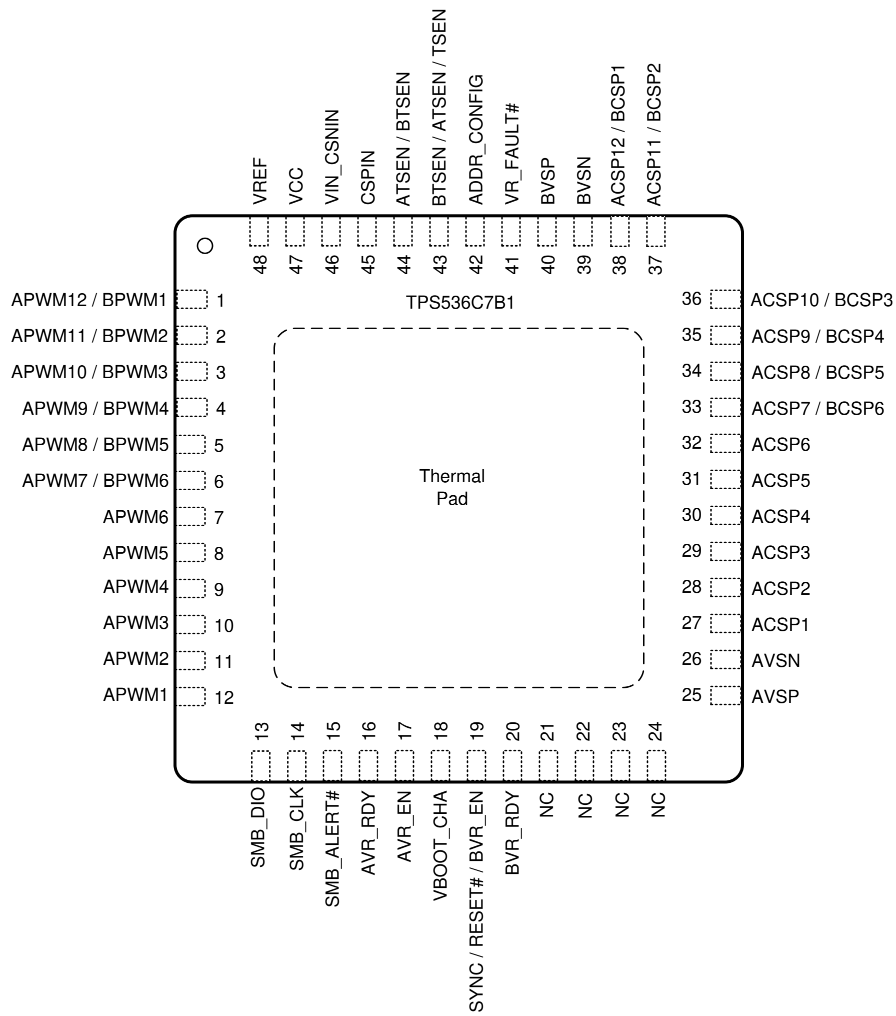


Figure 5-1. RSL Package 48-Pin QFN Top View

Table 5-1. Default functionality of multifunction pins

PIN	DEFAULT
1, 2, 3, 4, 5, 6, 33, 34, 35, 36, 37, 38	Based on ADDR_CONFIG pinstrap resistors
19	BVR_EN
43	BTSEN
44	ATSEN

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ACSP1	27	I	Current sense input for channel A. Connect to the IOUT pin of TI smart power stages. Float unused CSP pins.
ACSP2	28	I	
ACSP3	29	I	
ACSP4	30	I	
ACSP5	31	I	
ACSP6	32	I	
ACSP7 / BCSP6	33	I	Current sense input for phase 7 of channel A or phase 6 of channel B. Float unused CSP pins.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
ACSP8 / BCSP5	34	I	Current sense input for phase 8 of channel A or phase 5 of channel B. Float unused CSP pins.
ACSP9 / BCSP4	35	I	Current sense input for phase 9 of channel A or phase 4 of channel B. Float unused CSP pins.
ACSP10 / BCSP3	36	I	Current sense input for phase 10 of channel A or phase 3 of channel B. Float unused CSP pins.
ACSP11 / BCSP2	37	I	Current sense input for phase 11 of channel A or phase 2 of channel B. Float unused CSP pins.
ACSP12 / BCSP1	38	I	Current sense input for phase 12 of channel A or phase 1 of channel B. Float unused CSP pins.
ADDR_CONFIG	42	I	Connect a voltage divider from VREF to ADDR_CONFIG to GND. The value of the resistor between this pin and ground selects the phase configuration, and the pin voltage selects the PMBus address. Both are latched at VCC power-up. See Pinstrapping for more information. Use the PIN_DETECT_OVERRIDE command to select options which are not available by pinstrapping.
APWM1	12	O	PWM signal for phase 1 of channel A. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM2	11	O	PWM signal for phase 2 of channel A. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM3	10	O	PWM signal for phase 3 of channel A. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM4	9	O	PWM signal for phase 4 of channel A. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM5	8	O	PWM signal for phase 5 of channel A. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM6	7	O	PWM signal for phase 6 of channel A. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM7 / BPWM6	6	O	PWM signal for phase 7 of channel A, or phase 6 of channel B. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM8 / BPWM5	5	O	PWM signal for phase 8 of channel A, or phase 5 of channel B. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM9 / BPWM4	4	O	PWM signal for phase 9 of channel A, or phase 4 of channel B. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM10 / BPWM3	3	O	PWM signal for phase 10 of channel A, or phase 3 of channel B. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM11 / BPWM2	2	O	PWM signal for phase 11 of channel A, or phase 2 of channel B. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
APWM12 / BPWM1	1	O	PWM signal for phase 12 of channel A, or phase 1 of channel B. Connect to the PWM pin of the TI smart power stage. Float unused PWM pins.
ATSEN / BTSEN	44	I	Multi-function pin. Configure through PMBus. **ATSEN (default):** Connect to the TAO pin of the TI smart power stages of channel A to sense the highest temperature of the power stages and to sense the built-in fault signal from the power stages. **BTSEN:** Connect to the TAO pin of the TI smart power stages of channel B to sense the highest temperature of the power stages and to sense the built-in fault signal from the power stages. Float unused TSEN pins.
AVR_EN	17	I	Active high enable input for channel A. By default, asserting the AVR_EN pin activates channel A. Polarity and enable conditions are programmable through ON_OFF_CONFIG.
AVR_RDY	16	O	VRD "Ready" output signal of channel A. This open drain output requires an external pull-up resistor. The AVR_RDY pin is pulled low when a shutdown event occurs.
AVSN	26	I	Negative input of the remote voltage sense of channel A.
AVSP	25	I	Positive input of the remote voltage sense of channel A.
BTSEN . / ATSEN / TSEN	43	I	Multi-function pin. Configure through PMBus. **BTSEN (default):** Connect to the TAO pin of the TI smart power stages of channel B to sense the highest temperature of the power stages and to sense the built-in fault signal from the power stages. **BTSEN:** Connect to the TAO pin of the TI smart power stages of channel A to sense the highest temperature of the power stages and to sense the built-in fault signal from the power stages. **TSEN:** Connect to the TAO pin of the TI smart power stages of channels A and B to sense the highest temperature of the power stages and to sense the built-in fault signal from the power stages. Float unused TSEN pins.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	**NO.**		
BVR_EN / RESET# / SYNC	19	I	Multi-function pin. Configure through PMBus. **BVR_EN (Default)** : Active high enable input for channel B. Asserting the BVR_EN pin activates channel B. Polarity and enable conditions are programmable through ON_OFF_CONFIG. **RESET#**: Active low signal which causes both channels output voltage target to revert to their respective VBOOT values when asserted. Pull-up to 3.3 V. **SYNC**: If assigned as an output, this pin provides a free-running clock for other TPS536C7B1 devices to synchronize to. If assigned as an input, an internal phase locked-loop can synchronize switching of one or both channels to a clock supplied to this pin. Phase shift and data direction are programmable through NVM.
BVR_RDY	20	O	VRD "Ready" output signal of channel B. This open drain output requires an external pull-up resistor. The BVR_RDY pin is pulled low when a shutdown event occurs.
BVSN	39	I	Negative input of the remote voltage sense of channel B. If channel B is not used, connect BVSN to GND.
BVSP	40	I	Positive input of the remote voltage sense of channel B. If channel B is not used, connect BVSP to GND.
CSPIN	45	I	Positive terminal of the integrated high-side current sensing amplifier. Connect to the supply side of the input current sense element. Tie to VIN_CSNIN, and to the input voltage, if measured input current sensing is not used.
NC	21	-	Do not connect.
	22	-	
	23	-	
	24	-	
SMB_ALERT#	15	O	SMBus or I^{2}C bi-directional alert pin interface. (Open drain)
SMB_CLK	14	I	SMBus or I^{2}C serial clock interface. (Open drain)
SMB_DIO	13	I/O	SMBus or I^{2}C bi-directional serial data interface. (Open drain)
VBOOT_CHA	18	I	Connect a resistor divider from VREF to VBOOT_CHA to GND. Pinstrap for Channel A boot voltage. The value is latched at VCC power-up. See Pinstrapping for more information. Use the PIN_DETECT_OVERRIDE command to select options which are not available by pinstrapping.
VCC	47	P	3.3-V power input. Bypass to GND with a ceramic capacitor with a value greater than or equal to 1 µF effective capacitance.
VIN_CSNIN	46	I	Negative terminal of the integrated high-side current sense amplifier. Connect to the power-stage side of the current sense element. The VIN_CSNIN voltage is also used to determine the correct on-time for the converter. Tie to CSPIN, and to the input voltage, if measured input current sensing is not used.
VREF	48	O	1.5-V LDO reference voltage. Bypass to GND with a minimum effective 1-µF ceramic capacitor. Connect the VREF pin to the REFIN pin of the TI smart power stages as the current sense common-mode voltage.
VR_FAULT#	41	O	VR fault indicator. (Open-drain). This alert pulls low to indicate the converter has experienced a potentially catastrophic fault. The failures include the high-side FETs short, over-voltage, over-temperature, and the input over-current conditions. Use the fault signal on the platform to remove the power source by turning off the AC power supply. When the failure occurs, the VR_FAULT# pin is LOW, and put the controller into latch-off mode.
Thermal Pad		G	Analog ground pad. Connect to GND plan with vias.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage (1) (2)	CSPIN, VIN_CSNIN	–0.3	19	V
	Pin voltage, duration less than 100 ns ACSP1, ACSP2, ACSP3, ACSP4, ACSP5, ACSP6, ACSP7 / BCSP6, ACSP8 / BCSP5, ACSP9 / BCSP4, ACSP10 / BCSP3, ACSP11 / BSPC2, ACSP12 / BCSP1, ADDR_CONFIG, ATSEN / BTSEN, AVR_EN, AVSP, VBOOT_CHA, BTSEN / ATSEN / TSEN, BVSP, BVR_EN, SMB_CLK, SMB_DIO, SYNC, RESET#, VCC	-0.3	5.0	
	Pin voltage, duration greater than or equal to 100 ns ACSP1, ACSP2, ACSP3, ACSP4, ACSP5, ACSP6, ACSP7 / BCSP6, ACSP8 / BCSP5, ACSP9 / BCSP4, ACSP10 / BCSP3, ACSP11 / BSPC2, ACSP12 / BCSP1, ADDR_CONFIG, ATSEN / BTSEN, AVR_EN, AVSP, VBOOT_CHA, BTSEN / ATSEN / TSEN, BVSP, BVR_EN, SMB_CLK, SMB_DIO, SYNC, RESET#, VCC	–0.3	3.6	
	AGND, AVSN, BVSN	–0.3	0.3	
Output voltage (1) (2)	Pin voltage, duration less than 100 ns APWM1, APWM2, APWM3, APWM4, APWM5, APWM6, APWM7 / BPWM6, APWM8 / BPWM5, APWM9 / BPWM4, APWM10 / BPWM3, APWM11 / BPWM2, APWM12 / BPWM1, AVR_RDY, BVR_RDY, SMB_ALERT#, SYNC, VR_FAULT#	–0.3	5.0	V
	Pin voltage, duration greater than or equal to 100 ns APWM1, APWM2, APWM3, APWM4, APWM5, APWM6, APWM7 / BPWM6, APWM8 / BPWM5, APWM9 / BPWM4, APWM10 / BPWM3, APWM11 / BPWM2, APWM12 / BPWM1, AVR_RDY, BVR_RDY, SMB_ALERT#, SYNC, VR_FAULT#	–0.3	3.6	
	VREF	–0.3	1.8	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal GND unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Input voltage	CSPIN, VIN_CSNIN	4.5	12	18	V
	VCC	2.97	3.3	3.6	
	ACSP1, ACSP2, ACSP3, ACSP4, ACSP5, ACSP6, ACSP7 / BCSP6, ACSP8 / BCSP5, ACSP9 / BCSP4, ACSP10 / BCSP3, ACSP11 / BSPC2, ACSP12 / BCSP1, ADDR_CONFIG, ATSEN / BTSEN, AVR_EN, AVSP, VBOOT_CHA, BTSEN / ATSEN / TSEN, BVSP, BVR_EN, SMB_CLK, SMB_DIO, SYNC, RESET#	–0.1		3.6	
	AGND, AVSN, BVSN	–0.1		0.1	

		MIN	NOM	MAX	UNIT
Output voltage	VREF	–0.1		1.52	V
	APWM1, APWM2, APWM3, APWM4, APWM5, APWM6, APWM7 / BPWM6, APWM8 / BPWM5, APWM9 / BPWM4, APWM10 / BPWM3, APWM11 / BPWM2, APWM12 / BPWM1, AVR_RDY, BVR_RDY, SMB_ALERT#, SYNC, VR_FAULT#	–0.1		3.6	
Ambient temperature, T_A		–40		125	°C

6.4 Electrical Specifications

6.4.1 Thermal Information

THERMAL METRIC(1)		TPS536C7B1	UNIT
		RSL (VQFN)	
		48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4.2 Supply

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply: Currents, UVLO, and Power-On Reset						
I_{VCC}	VCC supply current with all phases active	Enable = 'HI '			100	mA
$V_{CCNORMAL}$	VCC Normal Range	Normal operation	2.97		3.6	V
$V_{CCUVLOH}$	VCC UVLO 'OK ' Threshold	Ramp up	2.92		2.97	V
$V_{CCUVLOL}$	VCC UVLO Fault Threshold	Ramp down	2.68		2.82	V
$V_{CCUVLOH}$	VCC UVLO Hysteresis	Hyseteresis	138		600	mV

6.4.3 DAC and Voltage Feedback

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
References: DAC and VREF						
V_{MODE}	Supported VOUT_MODE	VOUT_MODE = 16h	ULINEAR16, Absolute, N = -10 exponent			-
V_{DACRNG}	VDAC range	No external divider. VOUT_MAX ≤ 1.87 V	0.25		1.87	V
		No external divider VOUT_MAX > 1.87 V	0.50		3.74	V
R_{DIV}	External resistor for output voltage scaling with Vout > 3.74 V	VOUT to VSP resistor		500		Ω
		VSP to VSN resistor		500		Ω
V_{DAC}	VSP accuracy	0.25 ≤ VSP ≤ 1 V, I_{CORE} = 0A	-5		5	mV
		1 V < VSP ≤ 1.87 V; I_{CORE} = 0A	-0.5		0.5	%
		1.87 V < VSP ≤ 5 V; I_{CORE} = 0A	-1		1	%
V_{VREF}	VREF output accuracy	VCC = 2.97 V to 3.6 V, I_{VREF} = 0	1.493	1.5	1.507	V
$V_{VREF(REG)}$	VREF load regulation (sourcing)	I_{VREF} = 0A to 10 mA	-8			mV

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VREF load regulaiton (sinking)	I_{VREF} = -10 mA to 0A			8	mV
$V_{TRIM(RES)}$	Vout offset NVM resolution (1)	MFR_SPECIFIC_ED[13:12] = 00b		0.9765		mV
		MFR_SPECIFIC_ED[13:12] = 01b		1.9531		mV
		MFR_SPECIFIC_ED[13:12] = 10b		3.9063		mV
		MFR_SPECIFIC_ED[13:12] = 11b		7.8125		mV
$V_{TRIM(RNG)}$	Vout offset NVM range (1)	VOUT_TRIM in SLINEAR16 format	-128		127	LSB
Voltage Sense: AVSP/BVSP and AVSN/BVSN						
I_{AVSP}	AVSP Input Bias Current	Not in Fault, Disable or UVLO; AVSP = VDAC = 1.8 V AVSN = 0 V			50	µA
I_{AVSN}	AVSN Input Bias Current	Not in Fault, Disable or UVLO; AVSP = VDAC = 1.8 V, AVSN = 0 V	-55			µA
I_{BVSP}	BVSP Input Bias Current	Not in Fault, Disable or UVLO; BVSP = VDAC = 1.8 V, BVSN = 0 V			50	µA
I_{BVSN}	BVSN Input Bias Current	Not in Fault, Disable or UVLO; BVSP = VDAC = 1.8 V, BVSN = 0 V	-55			µA

(1) Guaranteed by Design.

6.4.4 Control Loop Parameters

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Loadline and Loop Compensation						
$R_{DCLL(RES)}$	DC load line resolution	VOUT_DROOP = 0 to 1 mΩ		7.8125		µΩ
		VOUT_DROOP = 1 to 2 mΩ		15.625		µΩ
		VOUT_DROOP = 2 to 4 mΩ		31.25		µΩ
		VOUT_DROOP = 4 to 8 mΩ		62.5		µΩ
$R_{DCLL(ACC)}$	DC load line accuracy	VOUT_DROOP > 0.3 mΩ	-2.5		2.5	%
$R_{ACLL(RES)}$	AC loadline resolution (1)	USER_DATA_01[47:32] = 0 to 1.0 mΩ (program in SLINEAR11 format)		15.625		µΩ
		USER_DATA_01[47:32] = 1 to 2 mΩ (program in SLINEAR11 format)		31.25		µΩ
		USER_DATA_01[47:32] = 2 to 4 mΩ (program in SLINEAR11 format)		62.5		µΩ
		USER_DATA_01[47:32] = 4 to 8 mΩ (program in SLINEAR11 format)		125		µΩ
$R_{ACLL(RES)}$	AC loadline accuracy (1)	AC loadline > 0.3 mΩ	-5		5	%
t_{INT}	Static integration-time constant (1)	USER_DATA_01[23:20] = 0000b	0.9	1	1.1	µs
		USER_DATA_01[23:20] = 0001b	1.8	2	2.2	µs
		USER_DATA_01[23:20] = 0010b	2.7	3	3.3	µs
		USER_DATA_01[23:20] = 0011b	3.6	4	4.4	µs
		USER_DATA_01[23:20] = 0100b	4.5	5	5.5	µs
		USER_DATA_01[23:20] = 0101b	5.4	6	6.6	µs
		USER_DATA_01[23:20] = 0110b	6.3	7	7.7	µs
		USER_DATA_01[23:20] = 0111b	7.2	8	8.8	µs
		USER_DATA_01[23:20] = 1000b	8.1	9	9.9	µs
		USER_DATA_01[23:20] = 1001b	9	10	11	µs
		USER_DATA_01[23:20] = 1010b	9.9	11	12.1	µs

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USER_DATA_01[23:20] = 1011b	10.8	12	13.2	µs
		USER_DATA_01[23:20] = 1100b	11.7	13	14.3	µs
		USER_DATA_01[23:20] = 1101b	12.6	14	15.4	µs
		USER_DATA_01[23:20] = 1110b	13.5	15	16.5	µs
		USER_DATA_01[23:20] = 1111b	14.4	16	17.6	µs
t_{DINT}	Dynamic integration-time constant (1)	USER_DATA_01[27:24] = 0000b	0.8	1	1.2	µs
		USER_DATA_01[27:24] = 0001b	1.9	2	2.1	µs
		USER_DATA_01[27:24] = 0010b	2.85	3	3.15	µs
		USER_DATA_01[27:24] = 0011b	3.8	4	4.2	µs
		USER_DATA_01[27:24] = 0100b	4.75	5	5.25	µs
		USER_DATA_01[27:24] = 0101b	5.7	6	6.3	µs
		USER_DATA_01[27:24] = 0110b	6.65	7	7.35	µs
		USER_DATA_01[27:24] = 0111b	7.6	8	8.4	µs
		USER_DATA_01[27:24] = 1000b	8.55	9	9.45	µs
		USER_DATA_01[27:24] = 1001b	9.5	10	10.5	µs
		USER_DATA_01[27:24] = 1010b	10.45	11	11.55	µs
		USER_DATA_01[27:24] = 1011b	11.4	12	12.6	µs
		USER_DATA_01[27:24] = 1100b	12.35	13	13.65	µs
		USER_DATA_01[27:24] = 1101b	13.3	14	14.7	µs
		USER_DATA_01[27:24] = 1110b	14.25	15	15.75	µs
		USER_DATA_01[27:24] = 1111b	15.2	16	16.8	µs
G_{INTTC}	Scaling factor for integration time constants (1)	USER_DATA_01[4] = 0b		1		x
		USER_DATA_01[4] = 1b		6		x
K_{AC}	AC gain settings (1)	USER_DATA_01[13:12] = 00b	0.45	0.5	0.55	x
		USER_DATA_01[13:12] = 01b	0.9	1	1.1	x
		USER_DATA_01[13:12] = 10b	1.35	1.5	1.65	x
		USER_DATA_01[13:12] = 11b	1.8	2	2.2	x
K_{INT}	Integration gain settings (1)	USER_DATA_01[15:14] = 00b	0.45	0.5	0.55	x
		USER_DATA_01[15:14] = 01b	0.9	1	1.1	x
		USER_DATA_01[15:14] = 10b	1.35	1.5	1.65	x
		USER_DATA_01[15:14] = 11b	1.8	2	2.2	x
V_{DINT}	Dynamic Integration Voltage Setting. Based on V_{ERR} (1)	USER_DATA_01[11:8] = 000b	48	60	72	mV
		USER_DATA_01[11:8] = 001b	68	80	92	mV
		USER_DATA_01[11:8] = 010b	88	100	112	mV
		USER_DATA_01[11:8] = 011b	108	120	132	mV
		USER_DATA_01[11:8] = 100b	128	140	152	mV
		USER_DATA_01[11:8] = 101b	148	160	172	mV
		USER_DATA_01[11:8] = 110b	168	180	192	mV
		USER_DATA_01[11:8] = 111b		Disabled		
Ramp Selections						
V_{RAMP}	Ramp Setting (1)	USER_DATA_01[19:17] = 000b	70	80	90	mV
		USER_DATA_01[19:17] = 001b	110	120	130	mV
		USER_DATA_01[19:17] = 010b	150	160	170	mV
		USER_DATA_01[19:17] = 011b	190	200	210	mV

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USER_DATA_01[19:17] = 100b	230	240	250	mV
		USER_DATA_01[19:17] = 101b	270	280	290	mV
		USER_DATA_01[19:17] = 110b	310	320	330	mV
		USER_DATA_01[19:17] = 111b	350	360	370	mV

(1) Guaranteed by Design.

6.4.5 Dynamic VID (DVID) Tuning

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Voltage Transitions						
$V_{OFS(WAKE)}$	V_{DAC} offset during soft-start (1)	USER_DATA_04[1:0] = 00b		0		mV
	(independently programmable for each channel)	USER_DATA_04[1:0] = 01b		30		mV
		USER_DATA_04[1:0] = 10b		60		mV
		USER_DATA_04[1:0] = 11b		90		mV
$V_{OFS(UP)}$	V_{DAC} offset during upward transitions (1)	USER_DATA_04[11:10] = 00b		0		mV
	(independently programmable for each channel)	USER_DATA_04[11:10] = 01b		10		mV
		USER_DATA_04[11:10] = 10b		20		mV
		USER_DATA_04[11:10] = 11b		30		mV
$V_{OFS(DOWN)}$	V_{DAC} offset during downward transitions (1)	USER_DATA_04[9:8] = 00b		0		mV
	(independently programmable for each channel)	USER_DATA_04[9:8] = 01b		10		mV
		USER_DATA_04[9:8] = 10b		20		mV
		USER_DATA_04[9:8] = 11b		30		mV
$R_{DCLL(UP)}$	Dynamic DC load line during up transitions (1)	VOUT_DROOP = 0.0 to 1.0 mΩ USER_DATA_04[36:32] = 00h to 1Fh Resolution = 0.03125 mΩ	0		0.96875	mΩ
	(independently programmable for each channel)	VOUT_DROOP = 1.0 to 2.0 mΩ USER_DATA_04[36:32] = 00h to 1Fh Resolution = 0.0625 mΩ	0		1.9375	mΩ
		VOUT_DROOP = 2.0 to 4.0 mΩ USER_DATA_04[36:32] = 00h to 1Fh Resolution = 0.125 mΩ	0		3.8750	mΩ
		VOUT_DROOP = 4.0 to 8.0 mΩ USER_DATA_04[36:32] = 00h to 1Fh Resolution = 0.250 mΩ	0		7.75	mΩ
$R_{ACLL(UP)}$	Dynamic AC load line during up transitions (1)	R_{ACLL} = 0.0 to 1.0 mΩ USER_DATA_04[19:16] = 0h to Fh Resolution = 0.0625 mΩ	0		0.9375	mΩ
	(independently programmable for each channel)	R_{ACLL} = 1.0 to 2.0 mΩ USER_DATA_04[19:16] = 0h to Fh Resolution = 0.125 mΩ	0		1.875	mΩ
		R_{ACLL} = 2.0 to 4.0 mΩ USER_DATA_04[19:16] = 0h to Fh Resolution = 0.250 mΩ	0		3.75	mΩ
		R_{ACLL} = 4.0 to 8.0 mΩ USER_DATA_04[19:16] = 0h to Fh Resolution = 0.500 mΩ	0		7.5	mΩ

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DCLL(DOWN)}$	Dynamic DC load line during down transitions (1)	VOUT_DROOP = 0.0 to 1.0 mΩ USER_DATA_04[44:40] = 00h to 1Fh Resolution = 0.03125 mΩ	0		0.96875	mΩ
	(independently programmable for each channel)	VOUT_DROOP = 1.0 to 2.0 mΩ USER_DATA_04[44:40] = 00h to 1Fh Resolution = 0.0625 mΩ	0		1.9375	mΩ
		VOUT_DROOP = 2.0 to 4.0 mΩ USER_DATA_04[44:40] = 00h to 1Fh Resolution = 0.125 mΩ	0		3.8750	mΩ
		VOUT_DROOP = 4.0 to 8.0 mΩ USER_DATA_04[44:40] = 00h to 1Fh Resolution = 0.250 mΩ	0		7.75	mΩ
$R_{ACLL(DOWN)}$	Dynamic AC load line during down transitions (1)	R_{ACLL} = 0.0 to 1.0 mΩ USER_DATA_04[27:24] = 0h to Fh Resolution = 0.0625 mΩ	0		1	mΩ
	(independently programmable for each channel)	R_{ACLL} = 1.0 to 2.0 mΩ USER_DATA_04[27:24] = 0h to Fh Resolution = 0.125 mΩ	1		2	mΩ
		R_{ACLL} = 2.0 to 4.0 mΩ USER_DATA_04[27:24] = 0h to Fh Resolution = 0.250 mΩ	2		4	mΩ
		R_{ACLL} = 4.0 to 8.0 mΩ USER_DATA_04[27:24] = 0h to Fh Resolution = 0.500 mΩ	4		8	mΩ
$t_{LLR(UP)}$	Dynamic load line up recovery delay (PWM cycles) (1)	USER_DATA_04[23:22] = 00b		1		clks
	(independently programmable for each channel)	USER_DATA_04[23:22] = 01b		2		clks
		USER_DATA_04[23:22] = 10b		4		clks
		USER_DATA_04[23:22] = 11b		8		clks
$t_{LLR(DOWN)}$	Dynamic load line down recovery delay (PWM cycles) (1)	USER_DATA_04[31:30] = 00b		1		clks
	(independently programmable for each channel)	USER_DATA_04[31:30] = 01b		2		clks
		USER_DATA_04[31:30] = 10b		4		clks
		USER_DATA_04[31:30] = 11b		8		clks
SR_{VOUT}	Slew Rate Setting	VOUT_TRANSITION_RATE = E050h	5		5.875	mV/µs
		VOUT_TRANSITION_RATE = E0A0h	10		11.75	mV/µs
		VOUT_TRANSITION_RATE = E0F0h	15		17.625	mV/µs
		VOUT_TRANSITION_RATE = E140h	20		23.5	mV/µs
		VOUT_TRANSITION_RATE = E190h	25		29.375	mV/µs
		VOUT_TRANSITION_RATE = E1E0h	30		35.25	mV/µs
		VOUT_TRANSITION_RATE = E230h	35		41.125	mV/µs
		VOUT_TRANSITION_RATE = E280h	39		47	mV/µs
		VOUT_TRANSITION_RATE = E005h	0.3125		0.367188	mV/µs
		VOUT_TRANSITION_RATE = E00Ah	0.625		0.734375	mV/µs
		VOUT_TRANSITION_RATE = E00Fh	0.9375		1.101563	mV/µs
		VOUT_TRANSITION_RATE = E014h	1.25		1.46875	mV/µs
		VOUT_TRANSITION_RATE = E019h	1.5625		1.835938	mV/µs

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		VOUT_TRANSITION_RATE = E01Eh	1.875		2.203125	mV/µs
		VOUT_TRANSITION_RATE = E023h	2.1875		2.570313	mV/µs
		VOUT_TRANSITION_RATE = E028h	2.5		2.9375	mV/µs

(1) Guaranteed by Design.

6.4.6 Undershoot Reduction (USR) and Overshoot Reduciton (OSR)

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multi-Level OSR and USR						
V_{USR1}	USR Level 1 Voltage Setting (V_{DAC}-V_{DROOP})	USER_DATA_02[12:8] = 00010b	5	15	25	mV
		USER_DATA_02[12:8] = 00011b	7.5	17.5	27.5	mV
		USER_DATA_02[12:8] = 00100b	10	20	30	mV
		USER_DATA_02[12:8] = 00101b	12.5	22.5	32.5	mV
		USER_DATA_02[12:8] = 00110b	15	25	35	mV
		USER_DATA_02[12:8] = 00111b	17.5	27.5	37.5	mV
		USER_DATA_02[12:8] = 01000b	20	30	40	mV
		USER_DATA_02[12:8] = 01001b	22.5	32.5	42.5	mV
		USER_DATA_02[12:8] = 01010b	25	35	45	mV
		USER_DATA_02[12:8] = 01011b	27.5	37.5	47.5	mV
		USER_DATA_02[12:8] = 01100b	30	40	50	mV
		USER_DATA_02[12:8] = 01101b	32.5	42.5	52.5	mV
		USER_DATA_02[12:8] = 01110b	35	45	55	mV
		USER_DATA_02[12:8] = 01111b	37.5	47.5	57.5	mV
		USER_DATA_02[12:8] = 10000b	40	50	60	mV
		USER_DATA_02[12:8] = 10001b	42.5	52.5	62.5	mV
		USER_DATA_02[12:8] = 10010b	45	55	65	mV
		USER_DATA_02[12:8] = 10011b	47.5	57.5	67.5	mV
		USER_DATA_02[12:8] = 10100b	50	60	70	mV
		USER_DATA_02[12:8] = 10101b	52.5	62.5	72.5	mV
		USER_DATA_02[12:8] = 10110b	55	65	75	mV
		USER_DATA_02[12:8] = 10111b	57.5	67.5	77.5	mV
		USER_DATA_02[12:8] = 11000b	60	70	80	mV
		USER_DATA_02[12:8] = 11001b (1)	62.5	72.5	82.5	mV
		USER_DATA_02[12:8] = other (1)		Disabled		
V_{USR2}	USR Level 2 Voltage Setting (V_{DAC}-V_{DROOP})	USER_DATA_02[36:32] = 00000b	5	15	25	mV
		USER_DATA_02[36:32] = 00001b	7.5	17.5	27.5	mV
		USER_DATA_02[36:32] = 00010b	10	20	30	mV
		USER_DATA_02[36:32] = 00011b	12.5	22.5	32.5	mV
		USER_DATA_02[36:32] = 00100b	15	25	35	mV
		USER_DATA_02[36:32] = 00101b	17.5	27.5	37.5	mV
		USER_DATA_02[36:32] = 00110b	20	30	40	mV
		USER_DATA_02[36:32] = 00111b	22.5	32.5	42.5	mV
		USER_DATA_02[36:32] = 01000b	25	35	45	mV

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USER_DATA_02[36:32] = 01001b	27.5	37.5	47.5	mV
		USER_DATA_02[36:32] = 01010b	30	40	50	mV
		USER_DATA_02[36:32] = 01011b	32.5	42.5	52.5	mV
		USER_DATA_02[36:32] = 01100b	35	45	55	mV
		USER_DATA_02[36:32] = 01101b	37.5	47.5	57.5	mV
		USER_DATA_02[36:32] = 01110b	40	50	60	mV
		USER_DATA_02[36:32] = 01111b	42.5	52.5	62.5	mV
		USER_DATA_02[36:32] = 10000b	45	55	65	mV
		USER_DATA_02[36:32] = 10001b	47.5	57.5	67.5	mV
		USER_DATA_02[36:32] = 10010b	50	60	70	mV
		USER_DATA_02[36:32] = 10011b	52.5	62.5	72.5	mV
		USER_DATA_02[36:32] = 10100b	55	65	75	mV
		USER_DATA_02[36:32] = 10101b	57.5	67.5	77.5	mV
		USER_DATA_02[36:32] = 10110b	60	70	80	mV
		USER_DATA_02[36:32] = 10111b	62.5	72.5	82.5	mV
		USER_DATA_02[36:32] = 11000b	65	75	85	mV
		USER_DATA_02[36:32] = 11001b (1)	67.5	77.5	87.5	mV
		USER_DATA_02[36:32] = others (1)		Disabled		mV
PH_{USR1}	Maximum phase added in USR level 1 (1)	USER_DATA_02[1:0] = 00b		3		phases
		USER_DATA_02[1:0] = 01b		4		phases
		USER_DATA_02[1:0] = 10b		5		phases
		USER_DATA_02[1:0] = 11b		All available		phases
V_{OSR}	OSR Voltage Setting	USER_DATA_02[19:16] = 0000b	8	20	32	mV
		USER_DATA_02[19:16] = 0001b	18	30	42	mV
		USER_DATA_02[19:16] = 0010b	28	40	52	mV
		USER_DATA_02[19:16] = 0011b	38	50	62	mV
		USER_DATA_02[19:16] = 0100b	48	60	72	mV
		USER_DATA_02[19:16] = 0101b	58	70	82	mV
		USER_DATA_02[19:16] = 0110b	68	80	92	mV
		USER_DATA_02[19:16] = 0111b	78	90	102	mV
		USER_DATA_02[19:16] = 1000b	88	100	112	mV
		USER_DATA_02[19:16] = 1001b	98	110	122	mV
		USER_DATA_02[19:16] = 1010b	108	120	132	mV
		USER_DATA_02[19:16] = 1011b	118	130	142	mV
		USER_DATA_02[19:16] = 1100b	128	140	152	mV
		USER_DATA_02[19:16] = 1101b	138	150	162	mV
		USER_DATA_02[19:16] = 1110b	148	160	172	mV
		USER_DATA_02[19:16] = 1111b (1)		Disabled		
BB_{OSR}	OSR pulse truncation for 1ph (1)	USER_DATA_02[7] = 0b		Disable		
		USER_DATA_02[7] = 1b		Enable		
BB_{OSR}	OSR body braking for normal phases (1)	USER_DATA_02[5] = 0b and USER_DATA_02[7] = 0b		Disable		
		USER_DATA_02[5] = 1b or USER_DATA_02[7] = 1b		Enable		
TB_{OSR}	OSR body braking time durations (1)	USER_DATA_02[4:2] = 000b	0.3	0.4	0.5	μs

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USER_DATA_02[4:2] = 001b	0.4	0.5	0.6	µs
		USER_DATA_02[4:2] = 010b	0.5	0.6	0.7	µs
		USER_DATA_02[4:2] = 011b	0.8	0.9	1	µs
		USER_DATA_02[4:2] = 100b	0.9	1	1.1	µs
		USER_DATA_02[4:2] = 101b	1	1.1	1.2	µs
		USER_DATA_02[4:2] = 110b	1.8	1.9	2	µs
		USER_DATA_02[4:2] = 111b	1.9	2	2.1	µs

(1) Specified by Design

6.4.7 Dynamic Phase Shedding (DPS)

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Phase Shedding						
PH_{DPS}	Minimum operating phase numbers with DPS enabled (1)	USER_DATA_07[3:2] = 00b		1		Phase
		USER_DATA_07[3:2] = 01b		2		Phase
		USER_DATA_07[3:2] = 10b		4		Phase
		USER_DATA_07[3:2] = 11b		8		Phase
t_{DPAFIL}	Filter time constant for phase adding (1)	USER_DATA_07[7:6] = 00b		0.5		µs
		USER_DATA_07[7:6] = 01b		1		µs
		USER_DATA_07[7:6] = 10b		1.5		µs
		USER_DATA_07[7:6] = 11b		2		µs
I_{DPA2}	Dynamic phase adding thresholds (1-2ph)	USER_DATA_07[11:8] = 0h	8.2	12	15.4	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[11:8] = 1h	8.8	13	17.3	A
		USER_DATA_07[11:8] = 2h	12.2	14	15.7	A
		USER_DATA_07[11:8] = 3h	13.3	15	16.7	A
		USER_DATA_07[11:8] = 4h	14.3	16	17.7	A
		USER_DATA_07[11:8] = 5h	15.1	17	18.7	A
		USER_DATA_07[11:8] = 6h	16.2	18	19.7	A
		USER_DATA_07[11:8] = 7h	17.3	19	20.7	A
		USER_DATA_07[11:8] = 8h	17.9	20	21.7	A
		USER_DATA_07[11:8] = 9h	19.2	21	22.7	A
		USER_DATA_07[11:8] = Ah	20.2	22	23.7	A
		USER_DATA_07[11:8] = Bh	21.3	23	24.8	A
		USER_DATA_07[11:8] = Ch	22.3	24	25.8	A
		USER_DATA_07[11:8] = Dh	23.2	25	26.8	A
		USER_DATA_07[11:8] = Eh	24	26	27.8	A
		USER_DATA_07[11:8] = Fh	24.9	27	28.8	A
I_{DPA3}	Dynamic phase adding thresholds (2-3ph)	USER_DATA_07[23:20] = 0h	25.2	30	35.8	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[23:20] = 1h	27.5	32	37.4	A

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USER_DATA_07[23:20] = 2h	29.1	34	40	A
		USER_DATA_07[23:20] = 3h	31.9	36	41.2	A
		USER_DATA_07[23:20] = 4h	33.5	38	43.5	A
		USER_DATA_07[23:20] = 5h	35.6	40	45.4	A
		USER_DATA_07[23:20] = 6h	37.8	42	47	A
		USER_DATA_07[23:20] = 7h	39.7	44	49.3	A
		USER_DATA_07[23:20] = 8h	45.6	50	55.2	A
		USER_DATA_07[23:20] = 9h	55.6	60	65.3	A
		USER_DATA_07[23:20] = Ah	65.8	70	75.2	A
		USER_DATA_07[23:20] = Bh	75.3	80	85.5	A
		USER_DATA_07[23:20] = Ch	85.8	90	95	A
		USER_DATA_07[23:20] = Dh	95.8	100	105	A
		USER_DATA_07[23:20] = Eh	105.7	110	114.9	A
		USER_DATA_07[23:20] = Fh	114.3	120	125.9	A
I_{DPA4}	Dynamic phase adding thresholds (3-4ph)	USER_DATA_07[19:16] = 0h	40.6	46	52.2	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[19:16] = 1h	43.5	48	53.6	A
		USER_DATA_07[19:16] = 2h	43.2	50	57.4	A
		USER_DATA_07[19:16] = 3h	47.5	52	57.6	A
		USER_DATA_07[19:16] = 4h	48.2	54	60.2	A
		USER_DATA_07[19:16] = 5h	51.5	56	61.4	A
		USER_DATA_07[19:16] = 6h	52.8	58	64.4	A
		USER_DATA_07[19:16] = 7h	54.7	60	66.3	A
		USER_DATA_07[19:16] = 8h	74.7	80	86	A
		USER_DATA_07[19:16] = 9h	94.6	100	106.1	A
		USER_DATA_07[19:16] = Ah	114.9	120	125.4	A
		USER_DATA_07[19:16] = Bh	135.2	140	145.4	A
		USER_DATA_07[19:16] = Ch	154.6	160	166.1	A
		USER_DATA_07[19:16] = Dh	175.1	180	185.5	A
		USER_DATA_07[19:16] = Eh	194.5	200	205.6	A
		USER_DATA_07[19:16] = Fh	213.4	220	226.7	A
I_{DPA5}	Dynamic phase adding thresholds (4-5ph)	USER_DATA_07[31:28] = 0h	55.9	62	69	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[31:28] = 1h	59.5	64	69.6	A
		USER_DATA_07[31:28] = 2h	59.6	66	73.2	A
		USER_DATA_07[31:28] = 3h	63.4	68	73.3	A
		USER_DATA_07[31:28] = 4h	65.1	70	76	A
		USER_DATA_07[31:28] = 5h	67.3	72	77.3	A
		USER_DATA_07[31:28] = 6h	69	74	79.6	A
		USER_DATA_07[31:28] = 7h	71.1	76	81.4	A
		USER_DATA_07[31:28] = 8h	85.1	90	95.4	A
		USER_DATA_07[31:28] = 9h	94.9	100	105.8	A

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USER_DATA_07[31:28] = Ah	104.9	110	115.8	A
		USER_DATA_07[31:28] = Bh	115.2	120	125.4	A
		USER_DATA_07[31:28] = Ch	135.2	140	145.4	A
		USER_DATA_07[31:28] = Dh	154.5	160	165.6	A
		USER_DATA_07[31:28] = Eh	175.2	180	185.2	A
		USER_DATA_07[31:28] = Fh	193.4	200	206.7	A
I_{DPA6}	Dynamic phase adding thresholds (5-6ph)	USER_DATA_07[27:24] = 0h	71.7	78	84.8	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[27:24] = 1h	74.8	81	87.1	A
		USER_DATA_07[27:24] = 2h	77.9	84	90.6	A
		USER_DATA_07[27:24] = 3h	81.6	87	92.8	A
		USER_DATA_07[27:24] = 4h	84.5	90	95.7	A
		USER_DATA_07[27:24] = 5h	87.2	93	99.5	A
		USER_DATA_07[27:24] = 6h	89.9	96	102.7	A
		USER_DATA_07[27:24] = 7h	93	99	105.5	A
		USER_DATA_07[27:24] = 8h	103.4	110	117	A
		USER_DATA_07[27:24] = 9h	114.5	120	126.5	A
		USER_DATA_07[27:24] = Ah	124	130	137.1	A
		USER_DATA_07[27:24] = Bh	134.7	140	145.1	A
		USER_DATA_07[27:24] = Ch	154.1	160	166.6	A
		USER_DATA_07[27:24] = Dh	174.8	180	185.5	A
		USER_DATA_07[27:24] = Eh	194.2	200	205.8	A
		USER_DATA_07[27:24] = Fh	213.2	220	227.3	A
I_{DPA7}	Dynamic phase adding thresholds (6-7ph)	USER_DATA_07[39:36] = 0h	100.1	105	110.5	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[39:36] = 1h	105.6	110	114.7	A
		USER_DATA_07[39:36] = 2h	109.8	115	120.8	A
		USER_DATA_07[39:36] = 3h	115.5	120	125	A
		USER_DATA_07[39:36] = 4h	120.2	125	130.2	A
		USER_DATA_07[39:36] = 5h	125.2	130	135.4	A
		USER_DATA_07[39:36] = 6h	130.6	135	140.1	A
		USER_DATA_07[39:36] = 7h	135.3	140	144.8	A
		USER_DATA_07[39:36] = 8h	155.1	160	165.2	A
		USER_DATA_07[39:36] = 9h	175.2	180	185.1	A
		USER_DATA_07[39:36] = Ah	195.2	200	205	A
		USER_DATA_07[39:36] = Bh	215	220	225.3	A
		USER_DATA_07[39:36] = Ch	235	240	245.2	A
		USER_DATA_07[39:36] = Dh	274.7	280	285.7	A
		USER_DATA_07[39:36] = Eh	314.3	320	325.7	A
		USER_DATA_07[39:36] = Fh	353.9	360	366.1	A
I_{DPA8}	Dynamic phase adding thresholds (7-8ph)	USER_DATA_07[35:32] = 0h	139.5	145	150.8	A

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[35:32] = 1h	145.4	150	155.3	A
		USER_DATA_07[35:32] = 2h	149.7	155	160.4	A
		USER_DATA_07[35:32] = 3h	154.9	160	165.5	A
		USER_DATA_07[35:32] = 4h	160.4	165	170.1	A
		USER_DATA_07[35:32] = 5h	165.1	170	174.9	A
		USER_DATA_07[35:32] = 6h	169.9	175	180.3	A
		USER_DATA_07[35:32] = 7h	175.5	180	185.1	A
		USER_DATA_07[35:32] = 8h	214.9	220	225.3	A
		USER_DATA_07[35:32] = 9h	234.7	240	245.4	A
		USER_DATA_07[35:32] = Ah	254.9	260	265.1	A
		USER_DATA_07[35:32] = Bh	274.6	280	285.8	A
		USER_DATA_07[35:32] = Ch	334.1	340	345.9	A
		USER_DATA_07[35:32] = Dh	373.7	380	386.3	A
		USER_DATA_07[35:32] = Eh	413.3	420	426.7	A
		USER_DATA_07[35:32] = Fh	452.9	460	467.1	A
I_{DPA9}	Dynamic phase adding thresholds (8-9ph)	USER_DATA_07[47:44] = 0h	180.2	188	194.8	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[47:44] = 1h	186.9	194	200.6	A
		USER_DATA_07[47:44] = 2h	192.8	200	206.6	A
		USER_DATA_07[47:44] = 3h	198.8	206	212.6	A
		USER_DATA_07[47:44] = 4h	205.4	212	217.9	A
		USER_DATA_07[47:44] = 5h	211.2	218	224.1	A
		USER_DATA_07[47:44] = 6h	216.9	224	230.3	A
		USER_DATA_07[47:44] = 7h	223.6	230	235.8	A
		USER_DATA_07[47:44] = 8h	243	250	256.2	A
		USER_DATA_07[47:44] = 9h	262.9	270	276.4	A
		USER_DATA_07[47:44] = Ah	283.3	290	295.7	A
		USER_DATA_07[47:44] = Bh	323	330	336.4	A
		USER_DATA_07[47:44] = Ch	362.9	370	376.6	A
		USER_DATA_07[47:44] = Dh	402.9	410	417.1	A
		USER_DATA_07[47:44] = Eh	442.5	450	457.5	A
		USER_DATA_07[47:44] = Fh	482	490	498	A
I_{DPA10}	Dynamic phase adding thresholds (9-10ph)	USER_DATA_07[43:40] = 0h	217.5	225	231.7	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[43:40] = 1h	224	230	235.6	A
		USER_DATA_07[43:40] = 2h	227.4	235	241.1	A
		USER_DATA_07[43:40] = 3h	232.8	240	246.6	A
		USER_DATA_07[43:40] = 4h	238.7	245	250.7	A
		USER_DATA_07[43:40] = 5h	243.3	250	256.1	A
		USER_DATA_07[43:40] = 6h	247.7	255	261.6	A

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VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USER_DATA_07[43:40] = 7h	253.3	260	266.1	A
		USER_DATA_07[43:40] = 8h	273.1	280	286.2	A
		USER_DATA_07[43:40] = 9h	292.7	300	306.1	A
		USER_DATA_07[43:40] = Ah	332.8	340	346.4	A
		USER_DATA_07[43:40] = Bh	373	380	386.6	A
		USER_DATA_07[43:40] = Ch	412.6	420	427.4	A
		USER_DATA_07[43:40] = Dh	452.1	460	467.9	A
		USER_DATA_07[43:40] = Eh	491.6	500	508.4	A
		USER_DATA_07[43:40] = Fh	531.1	540	548.9	A
I_{DPA11}	Dynamic phase adding thresholds (10-11ph)	USER_DATA_07[55:52] = 0h	257.4	265	271.7	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[55:52] = 1h	262.7	270	276.6	A
		USER_DATA_07[55:52] = 2h	267.8	275	281.2	A
		USER_DATA_07[55:52] = 3h	273.1	280	285.6	A
		USER_DATA_07[55:52] = 4h	278	285	291.4	A
		USER_DATA_07[55:52] = 5h	283.4	290	296	A
		USER_DATA_07[55:52] = 6h	288.2	295	300.9	A
		USER_DATA_07[55:52] = 7h	292.7	300	306.7	A
		USER_DATA_07[55:52] = 8h	312.9	320	326.5	A
		USER_DATA_07[55:52] = 9h	332.7	340	346.7	A
		USER_DATA_07[55:52] = Ah	352.7	360	367	A
		USER_DATA_07[55:52] = Bh	392.3	400	407.3	A
		USER_DATA_07[55:52] = Ch	431.9	440	448.1	A
		USER_DATA_07[55:52] = Dh	471.3	480	488.7	A
		USER_DATA_07[55:52] = Eh	510.8	520	529.2	A
		USER_DATA_07[55:52] = Fh	550.2	560	569.8	A
I_{DPA12}	Dynamic phase adding thresholds (11-12ph)	USER_DATA_07[51:48] = 0h	297.9	305	311.3	A
	Average current, assuming DPA Hysteresis is set equal to 1/2 I_{SUM} ripple for active phase number, accounting for ripple cancellation	USER_DATA_07[51:48] = 1h	302.7	310	316	A
		USER_DATA_07[51:48] = 2h	306.8	315	321.8	A
		USER_DATA_07[51:48] = 3h	313	320	326.2	A
		USER_DATA_07[51:48] = 4h	317.7	325	331.3	A
		USER_DATA_07[51:48] = 5h	322.7	330	336.3	A
		USER_DATA_07[51:48] = 6h	328.1	335	341.5	A
		USER_DATA_07[51:48] = 7h	332.1	340	346.5	A
		USER_DATA_07[51:48] = 8h	352.8	360	367.1	A
		USER_DATA_07[51:48] = 9h	372.7	380	387.4	A
		USER_DATA_07[51:48] = Ah	412.4	420	427.7	A
		USER_DATA_07[51:48] = Bh	432.1	440	448	A
		USER_DATA_07[51:48] = Ch	471.2	480	488.9	A
		USER_DATA_07[51:48] = Dh	510.6	520	529.5	A
		USER_DATA_07[51:48] = Eh	550	560	570.1	A

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		USER_DATA_07[51:48] = Fh	589.4	600	610.7	A
I_{HYST2}	DPA Hysteresis (1-2ph) Set equal to 1/2 I_{SUM} ripple with 1 phase operational	USER_DATA_07[59:56] = 0h to Fh	0		15	A
I_{HYST3}	DPA Hysteresis (2-3ph) Set equal to 1/2 I_{SUM} ripple with 2 phases operational	USER_DATA_07[71:68] = 0h to Fh	0		15	A
I_{HYST4}	DPA Hysteresis (3-4ph) Set equal to 1/2 I_{SUM} ripple with 3 phases operational	USER_DATA_07[67:64] = 0h to Fh	0		15	A
I_{HYST5}	DPA Hysteresis (4-5ph) Set equal to 1/2 I_{SUM} ripple with 4 phases operational	USER_DATA_07[79:76] = 0h to Fh	0		15	A
I_{HYST6}	DPA Hysteresis (5-6ph) Set equal to 1/2 I_{SUM} ripple with 5 phases operational	USER_DATA_07[75:72] = 0h to Fh	0		15	A
I_{HYST7}	DPA Hysteresis (6-7ph) Set equal to 1/2 I_{SUM} ripple with 6 phases operational	USER_DATA_07[87:84] = 0h to Fh	0		15	A
I_{HYST8}	DPA Hysteresis (7-8ph) Set equal to 1/2 I_{SUM} ripple with 7 phases operational	USER_DATA_07[83:80] = 0h to Fh	0		15	A
I_{HYST9}	DPA Hysteresis (8-9ph) Set equal to 1/2 ISUM ripple with 8 phases operational	USER_DATA_07[95:92] = 0h to Fh	0		15	A
I_{HYST10}	DPA Hysteresis (9-10ph) Set equal to 1/2 ISUM ripple with 9 phases operational	USER_DATA_07[91:88] = 0h to Fh	0		15	A
I_{HYST11}	DPA Hysteresis (10-11ph) Set equal to 1/2 ISUM ripple with 10 phases operational	USER_DATA_07[103:100] = 0h to Fh	0		15	A
I_{HYST12}	DPA Hysteresis (11-12ph) Set equal to 1/2 ISUM ripple with 11 phases operational	USER_DATA_07[99:96] = 0h to Fh	0		15	A
$I_{HYST-DPS}$	Dynamic phase shedding hysteresis	USER_DATA_07[15:14] = 00b		0		A
		USER_DATA_07[15:14] = 01b		1		A
		USER_DATA_07[15:14] = 10b		2		A
		USER_DATA_07[15:14] = 11b		3		A
I_{DPS2}	Phase shed threshold (2-1ph)	Avg. current, calculated		$I_{DPA2} - 1 \times I_{HYST-DPS}$		A
I_{DPS3}	Phase shed threshold (3-2ph)	Avg. current, calculated		$I_{DPA3} - 2 \times I_{HYST-DPS}$		A
I_{DPS4}	Phase shed threshold (4-3ph)	Avg. current, calculated		$I_{DPA4} - 3 \times I_{HYST-DPS}$		A
I_{DPS5}	Phase shed threshold (5-4ph)	Avg. current, calculated		$I_{DPA5} - 4 \times I_{HYST-DPS}$		A
I_{DPS6}	Phase shed threshold (6-5ph)	Avg. current, calculated		$I_{DPA6} - 5 \times I_{HYST-DPS}$		A
I_{DPS7}	Phase shed threshold (7-6ph)	Avg. current, calculated		$I_{DPA7} - 6 \times I_{HYST-DPS}$		A
I_{DPS8}	Phase shed threshold (8-7ph)	Avg. current, calculated		$I_{DPA8} - 7 \times I_{HYST-DPS}$		A
I_{DPS9}	Phase shed threshold (9-8ph)	Avg. current, calculated		$I_{DPA9} - 8 \times I_{HYST-DPS}$		A
I_{DPS10}	Phase shed threshold (10-9ph)	Avg. current, calculated		$I_{DPA10} - 9 \times I_{HYST-DPS}$		A
I_{DPS11}	Phase shed threshold (11-10ph)	Avg. current, calculated		$I_{DPA11} - 10 \times I_{HYST-DPS}$		A
I_{DPS12}	Phase shed threshold (12-11ph)	Avg. current, calculated		$I_{DPA12} - 11 \times I_{HYST-DPS}$		A
T_{DPS_DELAY}	Dynamic phase shedding delay (N+1 ph to N ph) (1)		115	120	125	µs

(1) Guaranteed by Design.

6.4.8 Turbo Mode and Thermal Balance Management (TBM)

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, TJ = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Turbo Mode and Thermal Management						
N_{turbo}	Number of turbo phases		0		4	
G_{TURBO}	Current share gain for Turbo Phases (1)	USER_DATA_10[6:5] = 00b		100		%
		USER_DATA_10[6:5] = 01b		150		%
		USER_DATA_10[6:5] = 10b		180		%
		USER_DATA_10[6:5] = 11b		220		%
K_T	Thermal balance gain (1)	USER_DATA_10[3:0] = 0000b		0.8		%
		USER_DATA_10[3:0] = 0001b		0.85		%
		USER_DATA_10[3:0] = 0010b		0.9		%
		USER_DATA_10[3:0] = 0011b		0.95		%
		USER_DATA_10[3:0] = 0100b		1		%
		USER_DATA_10[3:0] = 0101b		1.05		%
		USER_DATA_10[3:0] = 0110b		1.1		%
		USER_DATA_10[3:0] = 0111b		1.15		%
		USER_DATA_10[3:0] = 1000b		1.2		%

(1) Guaranteed by Design.

6.4.9 Overcurrent Limit (OCL)

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overcurrent Limit Thresholds						
I_{OCL}	Phase Valley OCL Thresholds	Programmable Range	17		130	A
	(Program through IOUT_OC_FAULT_LIMIT)	Programmable Resolution 17 A ≤ I_{OCL} ≤ 80 A		3		A
		Programmable Resolution 85 A ≤ I_{OCL} ≤ 130 A		5		A
		Threshold Accuracy 17 A ≤ I_{OCL} ≤ 80 A	-3.05		3.05	A
		Threshold Accuracy 85 A ≤ I_{OCL} ≤ 130 A	-5.55		5.55	A

6.4.10 Telemetry

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Telemetry						
t_{CS_FIL}	Per-phase current filter time constant (1)			300		µs
t_{CS_UPDATE}	Per-phase current update time (1)			20		µs
I_{CS_RNG}	Per-phase current reporting range		-10		120	A
t_{IMON_FIL}	IMON average time (1)			290		µs
t_{IMON_UPDATE}	IMON update time (1)			24		µs
I_{MON_RNG}	IMON reporting range		-10		70 x Nph	A
I_{MON_ERROR}	Per-phase and total current error (1)	Summed of the per-phase currents and the total current			1.0	A/ph
$I_{MON\_CAL\_OF\_LSB}$	IMON Calibration Offset LSB (1)	IOUT_CAL_OFFSET resolution		0.125		A

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{MON\_CAL\_OF\_RNG}$	IMON Calibration Offset Range [(1)]	IOUT_CAL_OFFSET range	-4		3.75	A
$I_{MON\_CAL\_GA\_LSB}$	IMON Calibration Gain LSB [(1)]	IOUT_CAL_GAIN resolution		0.2		%
$I_{MON\_CAL\_GA\_RNG}$	IMON Calibration Gain Range [(1)]	IOUT_CAL_GAIN range	-10		10	%
I_{MON_LSB}	IMON LSB via PMBus [(1)]				0.125	A
I_{MON_ACC}	Digital IMON Accuracy	12-phase, I_{OUT} = 0 A	-3.5		3.5	A
		12-phase, I_{OUT} = 60 A	-9		9	%
		12-phase, I_{OUT} = 120 A	-4.5		4.5	%
		12-phase, I_{OUT} = 240 A	-3		3	%
		12-phase, I_{OUT} = 360 A	-2.25		2.25	%
		12-phase, I_{OUT} = 600 A	-0.9		0.9	%
		12-phase, I_{OUT} = 840 A	-0.64		0.64	%
		10-phase, I_{OUT} = 0 A	-4		4	A
		10-phase, I_{OUT} = 50 A	-8		8	%
		10-phase, I_{OUT} = 100 A	-4		4	%
		10-phase, I_{OUT} = 200 A	-2		2	%
		10-phase, I_{OUT} = 300 A	-1.33		1.33	%
		10-phase, I_{OUT} = 500 A	-0.8		0.8	%
		8-phase, I_{OUT} = 0 A	-2.5		2.5	A
		8-phase, I_{OUT} = 45 A	-8		8	%
		8-phase, I_{OUT} = 90 A	-4		4	%
		8-phase, I_{OUT} = 135 A	-2.67		2.67	%
		8-phase, I_{OUT} = 180 A	-2		2	%
		8-phase, I_{OUT} = 225 A	-1.6		1.6	%
		8-phase, I_{OUT} = 270 A	-1.33		1.33	%
		8-phase, I_{OUT} = 450 A	-0.8		0.8	%
		6-phase, I_{OUT} = 0 A	-2.4		2.4	A
		6-phase, I_{OUT} = 25.5 A	-9.41		9.41	%
		6-phase, I_{OUT} = 51 A	-4.71		4.71	%
		6-phase, I_{OUT} = 76.5 A	-3.14		3.14	%
		6-phase, I_{OUT} = 102 A	-2.35		2.35	%
		6-phase, I_{OUT} = 127.5 A	-1.88		1.88	%
		6-phase, I_{OUT} = 153 A	-1.57		1.57	%
		6-phase, I_{OUT} = 255 A	-0.94		0.94	%
		2-phase, I_{OUT} = 0 A	-0.8		0.8	A
		2-phase, I_{OUT} = 8.2 A	-9.76		9.76	%
		2-phase, I_{OUT} = 16.4 A	-4.88		4.88	%
		2-phase, I_{OUT} = 24.6 A	-3.25		3.25	%
		2-phase, I_{OUT} = 32.8 A	-2.44		2.44	%
		2-phase, I_{OUT} = 41 A	-1.95		1.95	%
		2-phase, I_{OUT} = 49.2 A	-1.63		1.63	%
		2-phase, I_{OUT} = 82 A	-0.98		0.98	%
		1-phase, I_{OUT} = 0 A	-0.35		0.35	A
		1-phase, I_{OUT} = 3 A	-11.67		11.67	%

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		1-phase, I_{OUT} = 6 A	-5.83		5.83	%
		1-phase, I_{OUT} = 9 A	-3.89		3.89	%
		1-phase, I_{OUT} = 12 A	-2.92		2.92	%
		1-phase, I_{OUT} = 15 A	-2.33		2.33	%
		1-phase, I_{OUT} = 18 A	-1.94		1.94	%
		1-phase, I_{OUT} = 30 A	-1.17		1.17	%
V_{READ_VOUT}	READ_VOUT accuracy	V_{VSP} = 0.25 V to 0.75 V	-5		5	mV
		V_{VSP} = 0.75 V to 1.5 V	-10		10	mV
		V_{VSP} > 1.5 V	-15.0		15.0	mV
$V_{READ\_VOUT\_UPDATE}$	READ_VOUT update rate (1)				200	µs
V_{READ_VIN}	READ_VIN accuracy	V_{IN} = 4.5 V to 17 V	-2		2	%
$V_{READ\_VIN\_UPDATE}$	READ_VIN update rate (1)			150		µs
Temp	READ_TEMPERATURE_1 accuracy	0.28 V to 1.8 V on TSEN pin (-40C to 150C)	-2.5		2.5	C
$Temp_{UPDATE}$	READ_TEMPERATURE_1 update rate (1)			150		µs
$V_{TSENUVR}$	TSEN low voltage (rising edge)	Low voltage detection on TSEN pin before soft-start and during operations	220	245	270	mV
$V_{TSENUVF}$	TSEN low voltage (falling edge)	Low voltage detection on TSEN pin before soft-start and during operations	135	160	185	mV
$V_{TSENUVH}$	TSEN low voltage (hysteresis) (1)	Low voltage detection on TSEN pin before soft-start and during operations	50			mV
t_{TSEN}	TSEN filter time constant (1)			5		MHz
C_{TSEN}	Maximum capacitance on TSEN pin (1)	To get < 0.5us response time			220	pF
$R_{INSHUNT}$	Input current shunt range		0.1		10	mΩ
$G_{INSHUNT}$	Input amplifer gain options for different shunts (analog gain setting)	GINSHUNT = 0h		20		V/V
		GINSHUNT = 1h		30		V/V
		GINSHUNT = 2h		40		V/V
		GINSHUNT = 3h		50		V/V
		GINSHUNT = 4h		60		V/V
		GINSHUNT = 5h		70		V/V
		GINSHUNT = 6h		80		V/V
		GINSHUNT = 7h		100		V/V
V_{CSIN_MAX}	Maximum CSPIN-CSNIN voltage can be sensed (1)	IIN x Shunt (mohm) x Analog Gain			800	mV
t_{IIN_FIL}	IIN average time (1)			440		µs
t_{IIN_UPDATE}	IIN update time (1)			24		µs
I_{IIN_RNG}	IIN reporting range (1)		-5		100	A
I_{IN}	READ_IIN accuracy	IIN = 5.0 A (1 mV), RSHUNT = 0.2 mΩ, GINSHUNT = 20 and 100 V/V	-1		1	A
		IIN = 10.0 A (2 mV), RSHUNT = 0.2 mΩ, GINSHUNT = 20 and 100 V/V	-1		1	A
		IIN = 20.0 A (4 mV), RSHUNT = 0.2 mΩ, GINSHUNT = 20 and 100 V/V	-3.25		3.25	%

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		IIN = 40.0 A (8 mV), RSHUNT = 0.2 mΩ, GINSHUNT = 20 and 100 V/V	-3.25		3.25	%
		IIN = 70.0 A (14 mV), RSHUNT = 0.2 mΩ, GINSHUNT = 20 and 100 V/V	-2		2	%
I_{IN_CAL}	Calculated input current accuracy (1)	I_{IN} = 5A; 12Vin to 1.8Vout	-10		10	%
		I_{IN} = 10A	-5		5	%
		I_{IN} = 40A	-3.5		3.5	%
		IIN = 70A	-3		3	%
V_{READ_PIN}	READ_PIN accuracy	V_{IN} = 12 V; VCSPIN-VCSNIN = 14 mV; (70A @ 0.2 mohm shunt); Exclude ripple;	-2.5		2.5	%
P_{OUT_ACC}	READ_POUT Accuracy		Per IOUT and VOUT			%

(1) Guaranteed by Design.

6.4.11 Phase-Locked Loop and Closed-Loop Frequency Control

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching Frequency						
$f_{SW(RNG)}$	Switching Frequency Range	V_{IN} = 12 V, V_{VSP} = 1.0 V $f_{SW} \times N_{\Phi} \le 8$ MHz	300		2000	kHz
$f_{SW(TOL)}$	Switching Frequency Tolerance	V_{IN} = 12 V, V_{VSP} = 1.0 V $f_{SW} \times N_{\Phi} \le 8$ MHz	–10		10	%
Phase-Lock Loop and Synchronization						
$V_{IL(SYNC)}$	SYNC input logic low (1)				0.8	V
$V_{IH(SYNC)}$	SYNC input logic high (1)		1.35			V
$V_{OL(SYNC)}$	SYNC output logic low (1)	I_{PIN} = ± 0.5 mA			0.4	V
$V_{OH(SYNC)}$	SYNC output logic high (1)	I_{PIN} = ± 0.5 mA	1.7			V
$t_{PW(SYNC)}$	SYNC input minimum pulse width (1)		100			ns
$D_{SYNCOUT}$	SYNC output duty cycle (1)		40	50	60	%
f_{SYNC}	Synchronization frequency (1)		200		2000	kHz
Df_{SYNC}	SYNC allowable frequency difference from free-running frequency (1)	FREQUENCY_SWITCH from 300 kHz to 2 MHz	–50		50	kHz
M_{SYNCA}	Channel A Sync mode (1)	MFR_SPECIFIC_E4[5] = X MFR_SPECIFIC_E4[8] = 0b MFR_SPECIFIC_E4[14] = 0b	Disabled			
		MFR_SPECIFIC_E4[5] = 0b MFR_SPECIFIC_E4[8] = 1b MFR_SPECIFIC_E4[14] = 0b	Internal Clock, CLF Mode			
		MFR_SPECIFIC_E4[5] = 1b MFR_SPECIFIC_E4[8] = 0b MFR_SPECIFIC_E4[14] = 1b	External Clock, PLL Mode			
M_{SYNCB}	Channel B Sync mode (1)	MFR_SPECIFIC_E4[6] = X MFR_SPECIFIC_E4[9] = 0b MFR_SPECIFIC_E4[15] = 0b	Disabled			
		MFR_SPECIFIC_E4[6] = 0b MFR_SPECIFIC_E4[9] = 1b MFR_SPECIFIC_E4[15] = 0b	Internal Clock, CLF Mode			
		MFR_SPECIFIC_E4[6] = 1b MFR_SPECIFIC_E4[9] = 0b MFR_SPECIFIC_E4[15] = 1b	External Clock, PLL Mode			
PH_{SYNCA}	Channel A SYNC Phase Offset (1)	MFR_SPECIFIC_E4[23:20] = 0h		0		deg

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		MFR_SPECIFIC_E4[23:20] = 1h		30		deg
		MFR_SPECIFIC_E4[23:20] = 2h		60		deg
		MFR_SPECIFIC_E4[23:20] = 3h		90		deg
		MFR_SPECIFIC_E4[23:20] = 4h		120		deg
		MFR_SPECIFIC_E4[23:20] = 5h		150		deg
		MFR_SPECIFIC_E4[23:20] = 6h		180		deg
		MFR_SPECIFIC_E4[23:20] = 7h		210		deg
		MFR_SPECIFIC_E4[23:20] = 8h		240		deg
		MFR_SPECIFIC_E4[23:20] = 9h		270		deg
		MFR_SPECIFIC_E4[23:20] = Ah		300		deg
		MFR_SPECIFIC_E4[23:20] = Bh		330		deg
PH_{SYNCB}	Channel B SYNC Phase Offset (1)	MFR_SPECIFIC_E4[31:28] = 0h		0		deg
		MFR_SPECIFIC_E4[31:28] = 1h		30		deg
		MFR_SPECIFIC_E4[31:28] = 2h		60		deg
		MFR_SPECIFIC_E4[31:28] = 3h		90		deg
		MFR_SPECIFIC_E4[31:28] = 4h		120		deg
		MFR_SPECIFIC_E4[31:28] = 5h		150		deg
		MFR_SPECIFIC_E4[31:28] = 6h		180		deg
		MFR_SPECIFIC_E4[31:28] = 7h		210		deg
		MFR_SPECIFIC_E4[31:28] = 8h		240		deg
		MFR_SPECIFIC_E4[31:28] = 9h		270		deg
		MFR_SPECIFIC_E4[31:28] = Ah		300		deg
		MFR_SPECIFIC_E4[31:28] = Bh		330		deg

(1) Guaranteed by Design.

6.4.12 Logic Interface

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic Interface Pins						
V_{AENL}	Channel A ENABLE Logic Low				0.975	V
V_{AENH}	Channel A ENABLE Logic High		1.525			V
V_{AENHYS}	Channel A ENABLE Hysteresis (1)		0.4		0.6	V
t_{AENDIG}	Channel A ENABLE Deglitch (1)		0.275			µs
$t_{AENVRRDYF}$	Channel A ENABLE Low to VRRDY Low	No soft-stop; Only valid when using AVR_EN pin.			1.5	µs
I_{AENH}	Channel A I/O Leakage	Leakage current , V_{AVR_EN} = 1.1 V			25	µA
V_{BENL}	Channel B ENABLE Logic Low				0.925	V
V_{BENH}	Channel B ENABLE Logic High		1.225			V
V_{BENHYS}	Channel B ENABLE Hysteresis (1)		0.2		0.3	V
t_{BENDIG}	Channel B ENABLE Deglitch (1)		0.275			µs
$t_{BENVRRDYF}$	Channel B ENABLE Low to VRRDY Low (1)	No soft-stop; Only valid when using BVR_EN pin.			1.5	µs
I_{BENH}	Channel B I/O Leakage	Leakage current , V_{BVR_EN} = 1.1 V			25	µA
V_{PWML}	PWMx Output Low-level	I_{LOAD} = ± 0.5 mA			0.11	V
V_{PWMH}	PWMx Output High-level	I_{LOAD} = ± 0.5 mA; VCC = 2.97 V	2.85			V
V_{PWM_Tri}	PWMx Tri-State	I_{LOAD} = ± 100 µA	1.440	1.5	1.560	V

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{P\text{-}S\_H\text{-}L}$	PWMx H-L Transition-time (1)	C_{LOAD} = 10 pF; I_{LOAD} = ± 100 µA; 10% to 90% both edges			10	ns
$t_{P\text{-}S\_TRI}$	PWMx Tri-State Transition (1)	C_{LOAD} = 10 pF; I_{LOAD} = ± 100 µA; 10% or 90% to tri-state; both edges			20	ns

(1) Guaranteed by Design.

6.4.13 Current Sensing and Current Sharing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense and Current Sharing						
I_{ACSPx}	ACSPx leakage current	V_{ACSPx} = 2.1 V			75	µA
I_{BAL_TOL}	Internal current share tolerance (1)	At 20.5A/ph operations	-4.5		4.5	%
$I_{SHARE\_WRN\_TH}$	Current Share Warning Threshold	Based on the filtered CSPx average current USER_DATA_11[47:46] = 00b	2.8	5	7.2	A
	(independently programmable for each channel)	USER_DATA_11[47:46] = 01b	7.5	10	12.5	A
		USER_DATA_11[47:46] = 10b	12.5	15	17.5	A

(1) Guaranteed by Design.

6.4.14 Pin Detection Thresholds

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DECODE}	Low-Side Pinstrap Resistor Decode (3 LSB bits) (1)	R_{LOWER} = 154 kΩ with 1% tolerance		111		Bin
		R_{LOWER} = 115 kΩ with 1% tolerance		110		Bin
		R_{LOWER} = 86.6 kΩ with 1% tolerance		101		Bin
		R_{LOWER} = 64.9 kΩ with 1% tolerance		100		Bin
		R_{LOWER} = 49.9 kΩ with 1% tolerance		011		Bin
		R_{LOWER} = 37.4 kΩ with 1% tolerance		010		Bin
		R_{LOWER} = 27.4 kΩ with 1% tolerance		001		Bin
		R_{LOWER} = 20.0 kΩ with 1% tolerance		000		Bin
V_{DECODE}	Pin Voltage Decode (5 MSB bits) (1)	V_{PIN} = 22.5 mV		00000		Bin
		V_{PIN} = 67.5 mV		00001		Bin
		V_{PIN} = 112.5 mV		00010		Bin
		V_{PIN} = 157.5 mV		00011		Bin
		V_{PIN} = 202.5 mV		00100		Bin
		V_{PIN} = 247.5 mV		00101		Bin
		V_{PIN} = 292.5 mV		00110		Bin
		V_{PIN} = 337.5 mV		00111		Bin
		V_{PIN} = 382.5 mV		01000		Bin
		V_{PIN} = 427.5 mV		01001		Bin
		V_{PIN} = 472.5 mV		01010		Bin
		V_{PIN} = 517.5 mV		01011		Bin
		V_{PIN} = 562.5 mV		01100		Bin
		V_{PIN} = 607.5 mV		01101		Bin
		V_{PIN} = 652.5 mV		01110		Bin
		V_{PIN} = 697.5 mV		01111		Bin

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		V_{PIN} = 742.5 mV		10000		Bin
		V_{PIN} = 787.5 mV		10001		Bin
		V_{PIN} = 832.5 mV		10010		Bin
		V_{PIN} = 877.5 mV		10011		Bin
		V_{PIN} = 922.5 mV		10100		Bin
		V_{PIN} = 967.5 mV		10101		Bin
		V_{PIN} = 1012.5 mV		10110		Bin
		V_{PIN} = 1057.5 mV		10111		Bin
		V_{PIN} = 1102.5 mV		11000		Bin
		V_{PIN} = 1147.5 mV		11001		Bin
		V_{PIN} = 1192.5 mV		11010		Bin
		V_{PIN} = 1237.5 mV		11011		Bin
		V_{PIN} = 1282.5 mV		11100		Bin
		V_{PIN} = 1327.5 mV		11101		Bin
		V_{PIN} = 1372.5 mV		11110		Bin
		V_{PIN} = 1417.5 mV		11111		Bin

(1) The same decoding scheme and thresholds apply to both the ADDR_CONFIG and VBOOT_CHA pins.

6.4.15 ADDR_CONFIG Pinstrap Decoding

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PH_{CFG}	Phase Configuration (Channel A + Channel B)	Pinstrap Mode Decode 3 LSB = 000b		12+0		Phases
		Pinstrap Mode Decode 3 LSB = 001b		11+0		Phases
		Pinstrap Mode Decode 3 LSB = 010b		10+2		Phases
		Pinstrap Mode Decode 3 LSB = 011b		9+2		Phases
		Pinstrap Mode Decode 3 LSB = 100b		8+2		Phases
		Pinstrap Mode Decode 3 LSB = 101b		7+2		Phases
		Pinstrap Mode Decode 3 LSB = 110b		6+2		Phases
		Pinstrap Mode Decode 3 LSB = 111b		5+2		Phases
		NVM Mode (PIN_DETECT_OVERRIDE)		PHASE_CONFIG		Phases
PMB_{ADDR}	PMBus Address (7 bit I^2C Address)	Pinstrap Mode		88d + 5 MSB of decode		Bin
		NVM Mode (PIN_DETECT_OVERRIDE)		SLAVE_ADDRESS		Bin

6.4.16 VBOOT_CHA Pinstrap Decoding

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BOOTA}	Boot voltage for Channel A	Pinstrap Mode Decode = 0d		0		V
		Pinstrap Mode Decode = 1d to 253d		0.24 + (Decode × 0.01)		V

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		Pinstrap Mode Decode = 254d		3.3		V
		Pinstrap Mode Decode = 255d[1]		5		V
		NVM Mode (PIN_DETECT_OVERRIDE)		VOUT_COMMAND		V

(1) Requires an external divider on the VSP and VSN pins. VOUT_SCALE_LOOP is automatically programmed to 0.5

6.4.17 Timing Specifications

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing Specifications						
t_{ENABLE}	Enable delay time options [1]	TON_DELAY range = 0.5 ms to 127.5 ms with	0.5		127.5	ms
	(independently programmable for each channel)	TON_DELAY resolution		0.5		ms
		TON_DELAY accuracy	-10		10	%
$t_{DISABLE}$	Disable delay time options [1]	TOFF_DELAY range = 0.5 ms to 127.5 ms	0.5		127.5	ms
	(independently programmable for each channel)	TOFF_DELAY resolution		0.5		ms
		TOFF_DELAY accuracy	-10		10	%
PH_{START}	Operating Phases during Soft-Start [1]	USER_DATA_07[5:4] = 00b		MIN(4, N_{TOTAL})		ph
	(independently programmable for each channel)	USER_DATA_07[5:4] = 01b		MIN(6, N_{TOTAL})		ph
		USER_DATA_07[5:4] = 10b		MIN(8, N_{TOTAL})		ph
		USER_DATA_07[5:4] = 11b		N_{TOTAL}		ph
t_{OFF_MIN}	Controller minimum OFF time range	Programmable Range USER_DATA_02[23:20] = 0 to Fh	40		135	ns
	(independently programmable for each channel)	Resolution		15		ns
		Accuracy (all settings)	-25		25	ns
t_{ON_MIN}	Controller minimum ON time [1]	USER_DATA_02[39:38] = 0 to 3h	30		60	ns
	(independently programmable each channel)	Resolution		10		ns
		Accuracy	-12		12	ns
t_{ON_BLANK}	Rising-edge blanking time range [1]	Programmable Range USER_DATA_02[31:24]	20		155	ns
	(independently programmable for each channel)	Resolution		5		ns
		Accuracy	-25		25	ns

(1) Guaranteed by Design.

6.4.18 Faults and Converter Protection

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION						
V_{OVTRKA}	Channel A Tracking OV Fault Threshold (Offset with respect to output voltage target including VDROOP)	Programmable Range [2]	32		448	mV
		Resolution		32		mV
		Accuracy (all settings)	-16		16	mV

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVTRKB}	Channel B Tracking OV Fault Threshold (Offset with respect to output voltage target including VDROOP)	Programmable Range (2)	32		448	mV
		Resolution		32		mV
		Accuracy (all settings)	-20		20	mV
V_{OVFIXA}	Channel A Fixed OV Fault Threshold	Programmable Range (2)	0.6		3.7	V
		Resolution		0.1		V
		Accuracy (V_{OVFIX} < 3.6 V)	-50		50	mV
		Accuracy (V_{OVFIX} ≥ 3.6 V)	-65		65	mV
V_{OVFIXB}	Channel B Fixed OV Fault Threshold	Programmable Range (2)	0.6		3.7	V
		Resolution		0.1		V
		Accuracy (V_{OVFIX} < 3.6 V)	-50		50	mV
		Accuracy (V_{OVFIX} ≥ 3.6 V)	-65		65	mV
V_{OVPB-A}	Pre-biased OVP Channel A threshold (1)			3.7		V
V_{OVPB-B}	Pre-biased OVP Channel B threshold (1)			3.7		V
V_{OVW-A}	Channel A Tracking OV Warning Threshold (Offset with respect to output voltage target including VDROOP)	Programmable Range (2)	16		448	mV
		Resolution		8		mV
		Accuracy (all settings)	-12		12	mV
V_{OVW-B}	Channel B Tracking OV Warning Threshold (Offset with respect to output voltage target including VDROOP)	Programmable Range (2)	24		448	mV
		Resolution		8		mV
		Accuracy (all settings)	-23		23	mV
V_{UVW-A}	Channel A UV Warning Threshold (Offset with respect to output voltage target including VDROOP)	Programmable Range (2)	-16		-448	mV
		Resolution		8		mV
		Accuracy (all settings)	-11		11	mV
V_{UVW-B}	Channel B UV Warning Threshold (Offset with respect to output voltage target including VDROOP)	Programmable Range (2)	-8		-448	mV
		Resolution		8		mV
		Accuracy (all settings)	-22		22	mV
V_{UVF-A}	Channel A Tracking UV Fault Threshold (Offset with respect to output voltage target including VDROOP)	Programmable Range (2)	32		448	mV
		Resolution		32		mV
		Accuracy (all settings)	-16		16	mV
V_{UVF-B}	Channel B Tracking UV Fault Threshold (Offset with respect to output voltage target including VDROOP)	Programmable Range (2)	32		448	mV
		Resolution		32		mV
		Accuracy (all settings)	-21		21	mV
$t_{DLY(UVF)}$	Deglitch Time for Triggering UV Fault (1)	VOUT_UV_FAULT_RESPONSE[2:0] = x00b		4		µs
		VOUT_UV_FAULT_RESPONSE[2:0] = x01b		8		µs
		VOUT_UV_FAULT_RESPONSE[2:0] = x10b		12		µs
		VOUT_UV_FAULT_RESPONSE[2:0] = x11b		16		µs
I_{OCP-A}	Channel A Overcurrent Protection Threshold	Programmable Range (2)	1		1023	A
		Resolution		1		A
		Accuracy (11 phase, I_{OCP} ≤ 135 A)	-7		7	A
		Accuracy (11 phase, I_{OCP} > 135 A)	-4		4	%
I_{OCP-B}	Channel B Overcurrent Protection Threshold	Programmable Range (2)	1		1023	A
		Resolution		1		A
		Accuracy (4 phase, I_{OCP} ≤ 75 A)	-3		3	A
		Accuracy (4 phase, I_{OCP} > 75 A)	-3		3	%

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCW-A}	Channel A Overcurrent Warning Threshold	Programmable Range [(2)]	1		1023	A
		Resolution		1		A
		Accuracy (11 phase, I_{OCW} ≤ 135 A)	-7		7	A
		Accuracy (11 phase, I_{OCW} > 135 A)	-4		4	%
I_{OCW-B}	Channel B Overcurrent Warning Threshold	Programmable Range [(2)]	1		1023	A
		Resolution		1		A
		Accuracy (4 phase, I_{OCW} ≤ 75 A)	-3		3	A
		Accuracy (4 phase, I_{OCW} > 75 A)	-3		3	%
T_{OTF}	Over-temperature Fault threshold	Programmable Range	90		160	°C
		Resolution		1		°C
		Accuracy (all settings)	-3		3	°C
T_{OTW}	Over-temperature Warning threshold[(1)]	Programmable Range	90		160	°C
		Resolution		10		°C
		Accuracy (all settings)	-3		3	°C
V_{IOVF}	Input over-voltage fault threshold	Programmable Range	4		18	V
		Resolution		1		V
		Accuracy	-2		2	%
V_{IOVW}	Input over-voltage warning threshold	Programmable Range	4		18	V
		Resolution		1		V
		Accuracy	-2		2	%
V_{IUVW}	Input under-voltage warning threshold	Programmable Range	4.25		11.5	V
		Resolution		0.25		V
		Accuracy (all settings)	-0.25		0.25	V
V_{IUVF}	Input under-voltage fault threshold	Programmable Range	4.0		11.25	
		Resolution		0.25		
		Accuracy (all settings)	-0.25		0.25	V
t_{IUVF}	Input Under-Voltage Fault Response Time [(1)] Time from VIN < V_{IUVF} to converter shutdown	VIN_UV_FAULT_RESPONSE = 80h Shutdown immediately, do not restart			300	µs
I_{IOCF}	Input over-current fault threshold	Programmable Range	4		128	A
		Resolution		4		A
		Accuracy (all settings)	-3.5		3.5	A
I_{IOCW}	Input over-current warning threshold	Programmable Range	4		128	A
		Resolution		4		A
		Accuracy (all settings)	-4		4	A
t_{HICCUP}	Hiccup Wait Time [(1)] Applies only to HICCUP fault responses	USER_DATA_11[15:14] = 00b		5		ms
		USER_DATA_11[15:14] = 01b		10		ms
		USER_DATA_11[15:14] = 10b		25		ms
		USER_DATA_11[15:14] = 11b		50		ms
V_{PSFLT}	ATSEN/BTSEN pin voltage causing Power stage fault (TAO HIGH)			2.6		V
	ATSEN/BTSEN pin voltage clearing Power stage fault (TAO HIGH)			2.4		V
	ATSEN/BTSEN pin voltage hysteresis for Power stage fault (TAO HIGH)			0.2		V

(1) Guaranteed by Design.

(2) Settings are programmed through PMBus commands as described in the *Programming* section of this document. The device internally maps programmed settings to hardware supported values.

6.4.19 PMBus Interface

VCC = 3.3 V, CSPIN = VIN_CSNIN = 12 V, T_J = -40 to 125 ℃ unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PMBus Interface and Timing						
$t_{PMB-BUF}$	PMBus Free time between STOP and START conditions (1)		0.5			µs
$t_{PMB-HD-STA}$	Hold time after Repeated Start Condition (1)		0.26			µs
$t_{PMB-SU-STO}$	Stop condition Setup time (1)		0.26			µs
$t_{PMB-HD-DAT}$	SMB_DIO Hold Time (1) (2)		0			µs
$t_{PMB-SU-DAT}$	SMB_DIO Setup Time (1)		50			ns
$t_{PMB-TIMEOUT}$	SMB_CLK low timeout (1) (3)		25		35	ms
$t_{PMB-LOW}$	SMB_CLK low time (1)		0.5			µs
$t_{PMB-HIGH}$	SMB_CLK high time (1) (4)		0.26		50	µs
$t_{PMB-LOW-SEXT}$	Maximum clock stretching time (slave) (1) (5)				25	ms
$t_{PMB-LOW-MEXT}$	Maximum clock stretching time (master) (1) (6)				10	ms
t_{R-PMB}	SMB_DIO/SMB_CLK rise time, ($V_{IL(MAX)}$-150 mV to $V_{IH(MIN)}$+150 mV) (1)	100 kHz Class			1000	ns
		400 kHz Class			300	ns
		1000 kHz Class			120	ns
t_{F-PMB}	SMB_DIO/SMB_CLK fall time, ($V_{IH(MIN)}$ +150 mV to $V_{IL(MAX)}$ + 150 mV) (1)	100 kHz Class			1000	ns
		400 kHz Class			300	ns
		1000 kHz Class			120	ns
$t_{PMB-REJ}$	Noise spike suppression-time (1) (7)				50	ns
$I_{LK-PMB-BUS}$	Input leakage per PMBus segment (1)		-200		200	µA
$I_{LK-PMB-PIN}$	Input leakage for PMBus pins		-10		10	µA
$C_{PMB-BUS}$	PMBus Bus Capacitance (1)				400	pF
$C_{PMB-PIN}$	PMBus Pin Capacitance (1)				10	pF
V_{PULLUP_PMBus}	PMBus interface pull ups (1)		1.62		3.6	V
V_{IL_PMBus}	SMB_DIO, SMB_CLK Input logic low				0.8	V
V_{IH_PMBus}	SMB_DIO, SMB_CLK Input logic high		1.35			V
V_{HYST_PMBus}	Hysteresis voltage (1)		150	250	350	mV
PMB_{CLKR}	PMBus clock frequency range (1)	PMBus clock (8)	0.05		2	MHz

(1) Guaranteed by Design.
(2) A device must internally provide sufficient hold time for the SMBDAT signal (with respect to the $V_{IH, MIN}$ of the SMBCLK signal) to bridge the undefined region of the falling edge of SMBCLK.
(3) Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT, MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT, MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind

of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT, MAX}$ or longer

(4) $t_{PMB-HIGH, MAX}$ provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH, MAX}$.

(5) $t_{PMB-LOW-SEXT}$ is the cumulative time a given slave device is allowed to extend the clock cycles in one message from the initial START to the STOP. It is possible that another slave device or the master extends the clock causing the combined clock low extend time to be greater than tLOW:SEXT. Therefore, this parameter is measured with the slave device as the sole target of a full-speed master

(6) $t_{PMB-LOW-MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a slave device or another master extends the clock causing the combined clock low time to be greater

(7) Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

(8) I2C High-Speed mode is not supported

6.5 Typical Characteristics

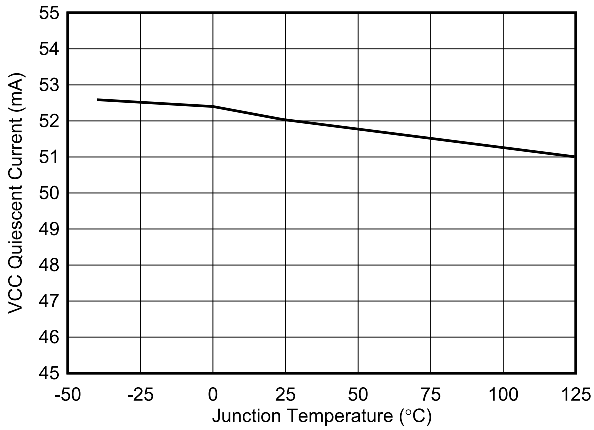


Figure 6-1. Quiescent current vs. junction temperature

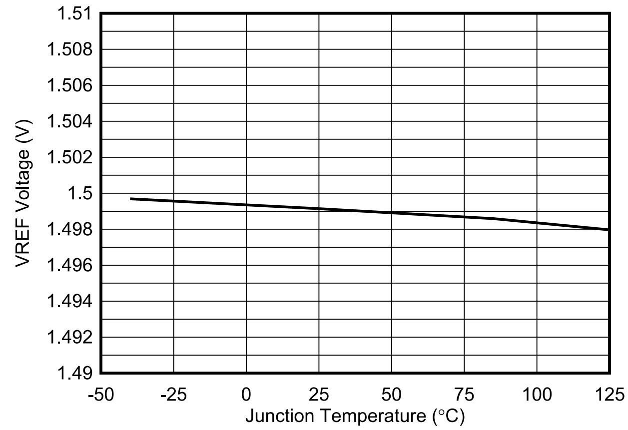


Figure 6-2. VREF voltage vs. junction temperature

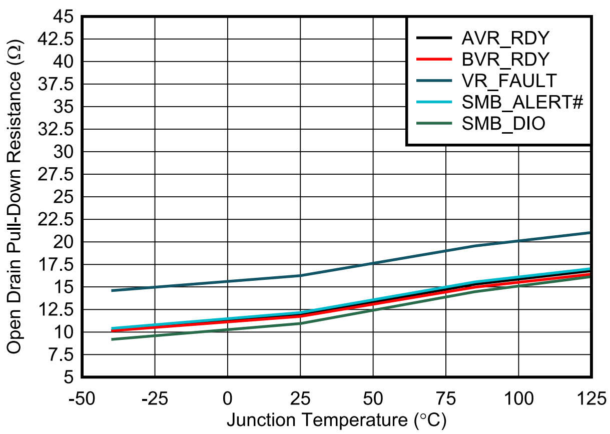


Figure 6-3. Pull-down resistance vs. junction temperature

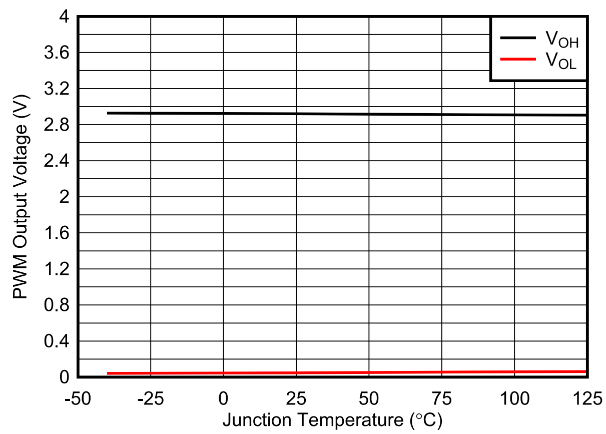


Figure 6-4. PWM output voltage vs. junction temperature (0.5 mA bias)

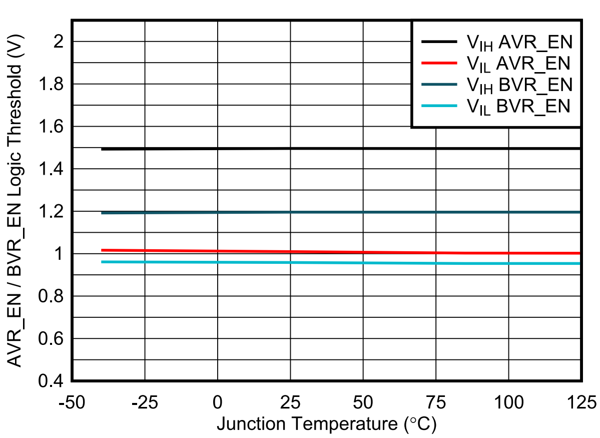


Figure 6-5. AVR_EN / BVR_EN logic threshold vs. junction temperature

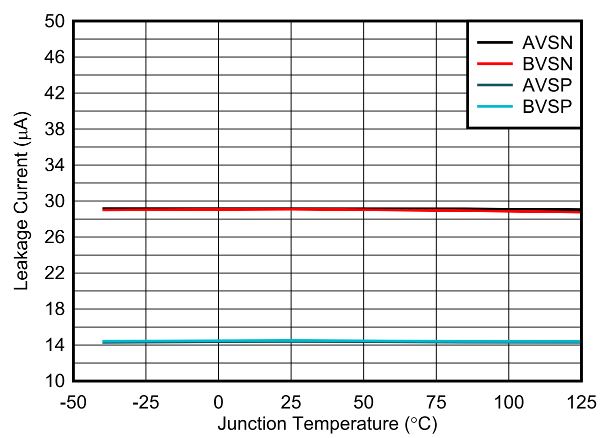


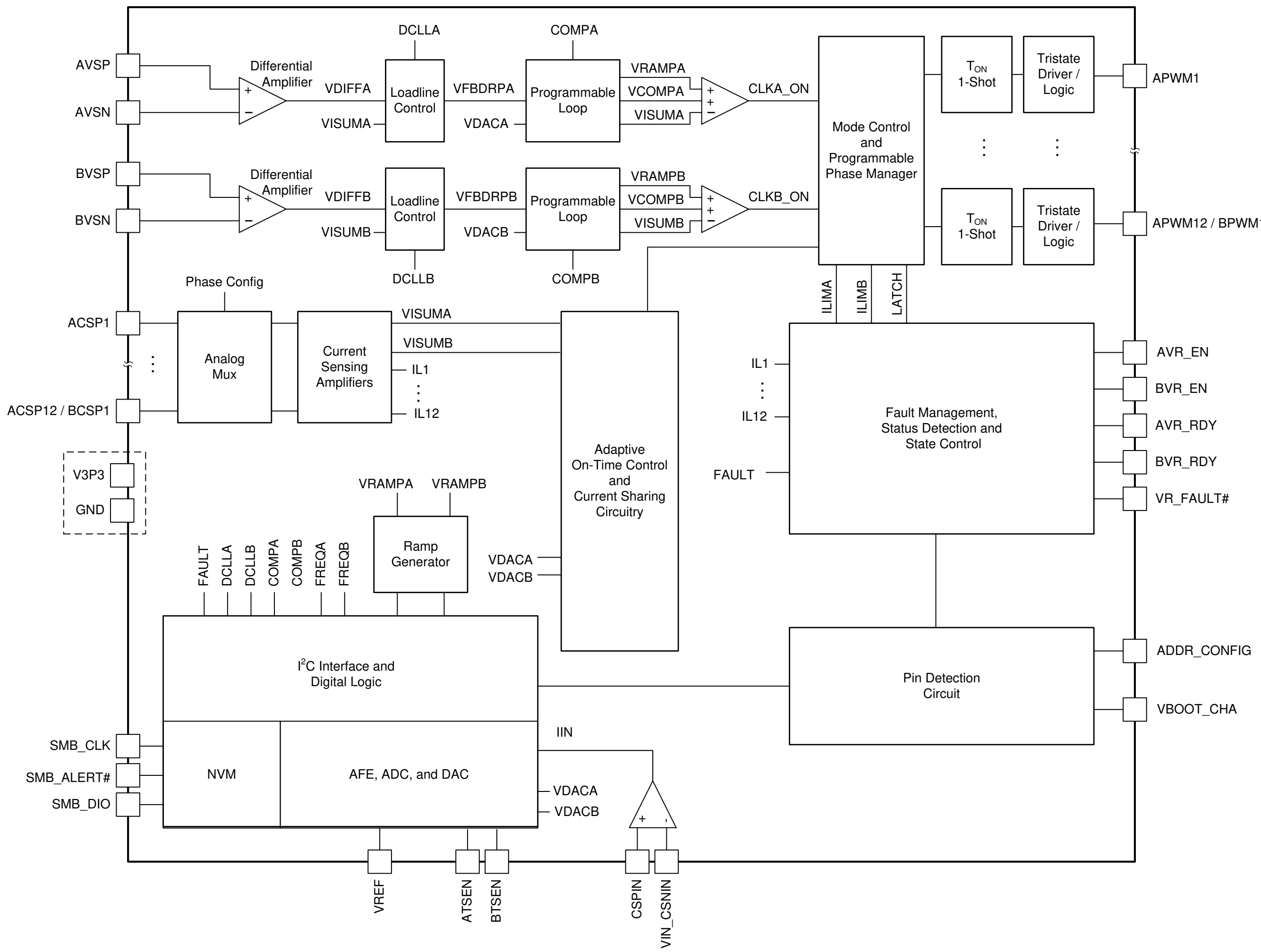
Figure 6-6. AVSP, BVSP, AVSN, BVSN leakage vs. junction temperature (1.0 V bias)

7 Detailed Description

7.1 Overview

The TPS536C7B1 is a 12-phase step-down controller with two channels, built-in non-volatile memory (NVM), a PMBus v1.3.1 interface, and is fully compatible with TI NexFET power stages.

7.2 Functional Block Diagram



7.3 Power-up and initialization

7.3.1 First power-up

When power is applied to TPS536C7B1, an initialization procedure performs self-checks of internal memories, performs pin detection, and loads the values stored in non-volatile memory to operating memory. This procedure can take up to 20 ms to complete, during which time the device may not respond to PMBus commands. Initialization takes place the first time power is applied to the VCC pin and does not repeat unless the device is power cycled. Pin configuration is loaded during this time. Until initialization is complete, all pins remain high impedance, except for the AVR_RDY and BVR_RDY pins which are pulled low by default.

Once initialization is complete, the device waits for an enable condition specified by the ON_OFF_CONFIG command to begin power conversion. By default the device is configured to wait for the AVR_EN pin to be set high to enable channel A, and the BVR_EN pin to be set high to enable channel B. Once an enable condition is received, TPS536C7B1 checks that the powerstage input supply (VIN_CSNIN pin) is above the VIN_ON value, and the powerstage driver is fully powered (e.g. that no TAO_LOW condition exists). This takes approximately 750 µs (up to 1.0 ms) to complete before the first PWM pulses are output by the controller. This process repeats each time power conversion is enabled for any reason, including enable cycling or fault shutdown.

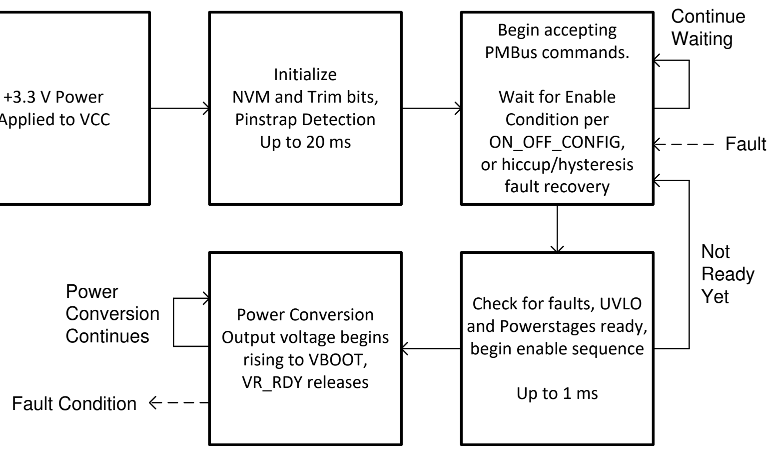


Figure 7-1. Initialization process

7.3.2 Boot voltage configuration (VBOOT)

By default, the boot voltage for channel A is given by pin-detection on the VBOOT_CHA pin. Alternatively, configure the device to use a value stored in non-volatile memory (NVM) for VOUT_COMMAND using the PIN_DETECT_OVERRIDE command. See Pin-strap Detection and PIN_DETECT_OVERRIDE for more information. The boot voltage for Channel B is given by the value stored in non-volatile memory for VOUT_COMMAND always. Whenever power conversion is enabled, each channel boots to its VBOOT value, regardless of whether the output voltage was changed after the last boot-up.

Use the VOUT_COMMAND PMBus command to change the output voltage on-the-fly. This is one implementation of adaptive voltage scaling (AVS) or dynamic VID (DVID). Output voltage transitions occur at the value slew rate specified by the VOUT_TRANSITION_RATE command.

7.3.3 Power Sequencing

There are no strict supply sequencing requirements for TPS536C7B1. VIN_CSNIN and CSP, the powerstage 5-V supply, and the controller VCC (3.3-V) may be safely powered up independently of each other. TI recommends that power conversion be commanded on only after all supplies are established and have had time to settle. Refer to Power Supply Recommendations for more detailed information.

7.4 Pin connections and bevahior

7.4.1 Supplies: VCC and VREF

The VCC pin supplies all analog and digital circuits internal to the device. Connect a 3.3-V supply voltage, and local ceramic bypass capacitor with a minimum effective capacitance of 1.0 µF.

The VREF pin is the output of an internal LDO with a nominal voltage of 1.5 V. The VREF voltage provides a common-mode voltage for the power stage IOUT pins, as well as internal analog circuits. Bypass the VREF pin local to the controller, with a ceramic bypass capacitor with a minimum effective capacitance of 1.0 µF. Connect VREF to the REFIN pins of the power stages.

7.4.2 Differential remote sensing and output voltage scaling: AVSP/AVSN, BVSP/BVSN

A differential remote sense amplifier enables the controller to compensate for I×R drop due to PCB copper, in high current applications. Connect the AVSP/BVSP and AVSN/BVSN pins respectively to the output voltage at the load point, through the network described in Figure 7-2. A connection to the output voltage, local to the power stages, shown by R_{LCL_P} and R_{LCL_N}, maintains closed loop operation even if the load is uninstalled, or the remote sense connection is opened. Route the differential remote sense lines as a tightly-coupled differential pair, and maintain a wide clearance to any fast switching nets, such as power stage switch nodes or power input voltage. Optionally, use a small filtering capacitor, shown as C_{FILT}, at the controller side to improve noise immunity.

The output voltage set-point is generated by an internal precision reference DAC. The reference DAC is capable of producing reference voltages up to 1.87 V. For output voltage set-points below 1.87 V, no scaling (internal or external) is required, and the sensed output voltage is compared directly to the reference voltage.

For output voltage set-points between 1.87 V and 3.74 V, the controller applies internal scaling of the remote sense amplifier, and no external sense divider is needed. Set the VOUT_MAX command greater than 1.87 V to enable this internal scaling. For output voltage set-points greater than 3.74 V, apply an external sense divider with R_{RMT_P} = R_{DIV} = 500 Ω, and set the VOUT_SCALE_LOOP command to 0.5 V/V. This enables output voltage set-points up to 5.5 V. The overvoltage/undervoltage thresholds are referenced to the VSP/VSN pins only and need to be scaled appropriately for applications with an external resistor divider. Refer to Table 7-1 for more information.

TPS536C7B1 performs an open/short detection on the AVSP/AVSN and BVSP/BVSN pins at initialization to determine if the voltage sense lines are open. The controller flags a fault condition and does not attempt to boot if an open sense line is detected. Ground the VSP/VSN lines for unused channels to prevent false-triggering, in applications which do not make use of both channels. As such, the local sense resistor connection may be omitted, but is still recommended for debug and system bode plot measurement.

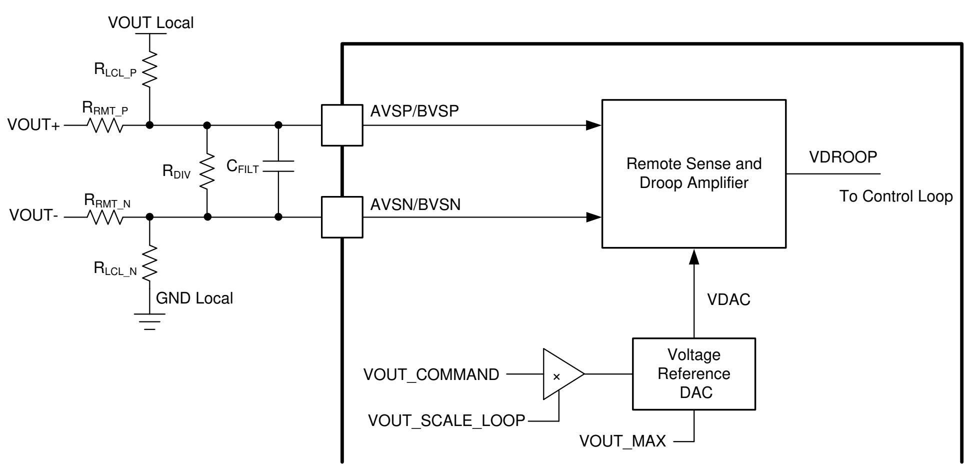


Figure 7-2. Differential remote sensing

Table 7-1. Component and command values

Component / Command	Value (Vout ≤ 1.87 V)	Value (1.87 V < Vout ≤ 3.74 V)	Value (3.74 V < Vout ≤ 5.5 V)
R_{LCL_P}	DNP	DNP	DNP
R_{RMT_P}	0 Ω	0 Ω	500 Ω
R_{RMT_N}	0 Ω	0 Ω	0 Ω
R_{LCL_N}	DNP	DNP	DNP
R_{DIV}	DNP	DNP	500 Ω
C_{FILT}	100 pF (optional)	100 pF (optional)	100 pF (optional)
VOUT_SCALE_LOOP	1.0	1.0	0.5
VOUT_MAX	VOUT_MAX ≤ 1.87 V	1.87 V < VOUT_MAX ≤ 3.74 V	3.74 V < VOUT_MAX ≤ 5.5 V
VOUT_COMMAND	VOUT_COMMAND ≤ 1.87 V	VOUT_COMMAND ≤ 3.74 V	VOUT_COMMAND ≤ 5.5 V

7.4.3 Input current sensing: VIN_CSNIN and CSPIN

The VIN_CSNIN and CSP pins are internally connected to a high-side current sense amplifier. Kelvin connect these pins to the external sense element R_{SENSE} as shown in Figure 7-3, and route back to the controller as a tightly coupled differential pair. R_{SENSE} may be a precision current sense shunt resistor or an input inductor DCR, with an associated temperature compensation network. TI recommends adding common-mode filtering capacitors, shown as C_{CMFILT}, and a differential-mode filtering capacitor C_{DMFILT} to reduce measurement noise. A typical value for these capacitors is 1.0 µF.

For designs that do not use input current sensing, connect VIN_CSNIN and CSPIN together, and to the input voltage supply. The controller requires input voltage sense for proper on-time generation. Ensure the VIN_CSNIN and CSPIN pins remain within ± 300 mV due to internal ESD protection structures on these pins.

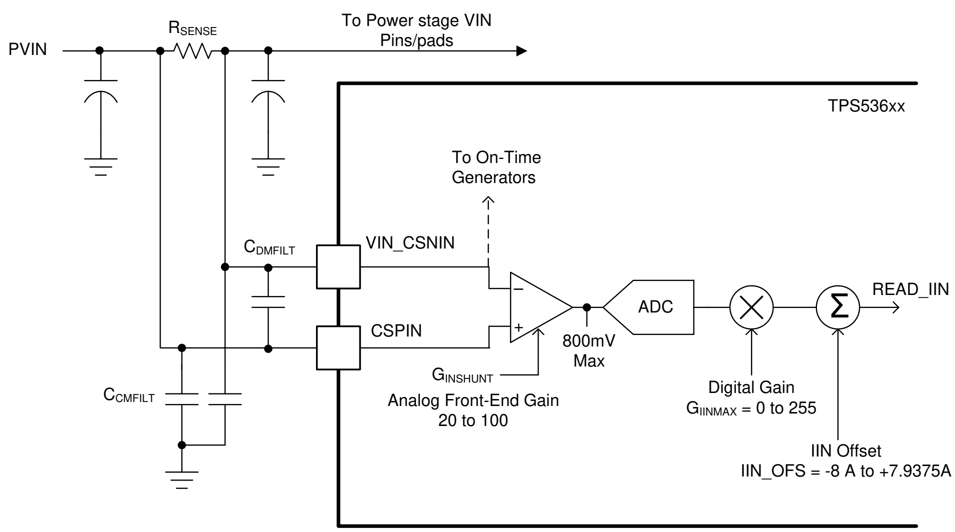


Figure 7-3. Input current sensing

Once properly calibrated, the READ_IIN command returns measured input current data in real time. Power supply telemetry and calibration describes the process and equations for input current calibration.

7.4.4 Pin-strap detection and PIN_DETECT_OVERRIDE

The ADDR_CONFIG pin provides limited resistor pin detection for the PMBus slave address, and phase configuration. Connect a resistor divider to ADDR_CONFIG as shown in Figure 7-4. Refer to Table 7-2 to select resistor values. The table shows series E96 value equivalents. Use 1% tolerance resistors for all values. After pin detection completes, the decoded results are loaded into the SLAVE_ADDRESS and PHASE_CONFIG commands. Phase firing order is automatically selected by pin detection. Disable phase number detection on the ADDR_CONFIG pin detection using PIN_DETECT_OVERRIDE, to use a non-default firing order.

The VBOOT_CHA pin provides resistor pin detection for the channel A boot voltage. The channel B boot voltage does not have pin detection and must be programmed in non-volatile memory. Connect a resistor divider to VBOOT_CHA as shown in Figure 7-4. The table shows series E96 value equivalents. Use 1% tolerance resistors for all values. After pin detection completes, the decoded result is loaded into the VOUT_COMMAND command for PAGE 0.

For each each pin detection, during boot-up the device performs two measurements to determine an 8 bit binary number, referred to as the *pinstrap decode*. The 3 LSB bits are determined by shorting the high-side resistor and measuring the low-side resistor value. The 5 MSB bits are determined by measuring the pin voltage. The decoded value is then mapped to the configuration values shown in the tables below.

Values not given by ADDR_CONFIG pinstrap decoding and VBOOT_CHA pinstrap decoding can still be achieved using the PIN_DETECT_OVERRIDE command. This command instructs the device at power-up, whether to follow the values given by pin detection, or use values stored in non-volatile memory to populate the SLAVE_ADDRESS, PHASE_CONFIG and VOUT_COMMAND commands. Each parameter has a separate control, so it is possible, for example, to pin detect PMBus address, while taking phase configuration from NVM.

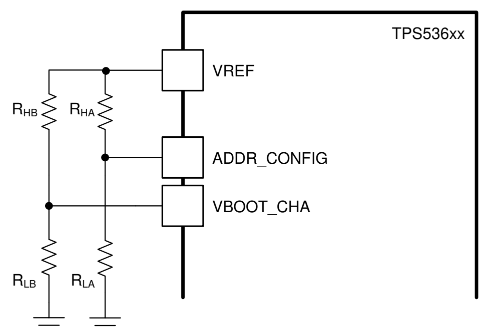


Figure 7-4. Pin-strap pin connections

Example: Selecting a PMBus address not available by pin-strapping

1. Select the ADDR_CONFIG resistors R_{HA} and R_{LA} to ensure each device on the bus still has a unique adddress at the first power-up. Each device still must be addressed uniquely, in order to configure the PIN_DETECT_OVERRIDE command.
2. Write bit 2 in PIN_DETECT_OVERRIDE command to 0b, to disable pin detection for the PMBus Address on the ADDR_CONFIG pin.
3. Write the SLAVE_ADDRESS command, to configure the new slave address, in 7-bit right-justified binary format (e.g. 96d = 1100000b).
4. Issue a STORE_USER_ALL command to commit the configuration to non-volatile memory
5. At the next power cycle, the values stored in non-volatile memory are used, instead of those selected by the ADDR_CONFIG resistors selected.

Table 7-2. ADDR_CONFIG pinstrap decoding

Phase Configuration (Ch. A + Ch. B)		12 + 0 LSB = 000b		11 + 0 LSB = 001b		10 + 2 LSB = 010b		9 + 2 LSB = 011b		8 + 2 LSB = 100b		7 + 2 LSB = 101b		6 + 2 LSB = 110b		5 + 2 LSB = 111b	
MSB	PMBus Address	R_{HA} (kΩ)	R_{LA} (kΩ)	R_{HA} (kΩ)	R_{LA} (kΩ)	R_{HA} (kΩ)	R_{LA} (kΩ)	R_{HA} (kΩ)	R_{LA} (kΩ)	R_{HA} (kΩ)	R_{LA} (kΩ)	R_{HA} (kΩ)	R_{LA} (kΩ)	R_{HA} (kΩ)	R_{LA} (kΩ)	R_{HA} (kΩ)	R_{LA} (kΩ)
00000b	88d / B0h	1300	20	1780	27.4	2430	37.4	3240	49.9	4220	64.9	5620	86.6	7500	115	9760	154
00001b	89d / B2h	422	20	576	27.4	787	37.4	1050	49.9	1370	64.9	1820	86.6	2430	115	3240	154
00010b	90d / B4h	249	20	340	27.4	464	37.4	619	49.9	806	64.9	1070	86.6	1430	115	1910	154
00011b	91d / B6h	169	20	232	27.4	316	37.4	422	49.9	549	64.9	732	86.6	976	115	1300	154
00100b	92d / B8h	127	20	174	27.4	237	37.4	316	49.9	412	64.9	549	86.6	732	115	976	154
00101b	93d / BAh	102	20	140	27.4	191	37.4	255	49.9	332	64.9	442	86.6	576	115	787	154
00110b	94d / BCh	82.5	20	113	27.4	154	37.4	205	49.9	267	64.9	357	86.6	475	115	634	154
00111b	95d / BEh	68.1	20	95.3	27.4	130	37.4	174	49.9	226	64.9	301	86.6	392	115	536	154
01000b	96d / C0h	59	20	80.6	27.4	110	37.4	147	49.9	191	64.9	255	86.6	332	115	453	154
01001b	97d / C2h	Not recommended - reserved SMBus address															
01010b	98d / C4h	43.2	20	59	27.4	80.6	37.4	110	49.9	140	64.9	187	86.6	249	115	332	154
01011b	99d / C6h	38.3	20	52.3	27.4	71.5	37.4	95.3	49.9	124	64.9	165	86.6	221	115	294	154
01100b	100d / C8h	33.2	20	45.3	27.4	61.9	37.4	82.5	49.9	107	64.9	143	86.6	191	115	255	154
01101b	101d / CAh	29.4	20	40.2	27.4	54.9	37.4	73.2	49.9	95.3	64.9	127	86.6	169	115	226	154
01110b	102d / CCh	26.1	20	35.7	27.4	48.7	37.4	64.9	49.9	84.5	64.9	113	86.6	150	115	200	154
01111b	103d / CEh	23.2	20	31.6	27.4	43.2	37.4	57.6	49.9	73.2	64.9	97.6	86.6	133	115	178	154
10000b	104d / D0h	20.5	20	28.0	27.4	38.3	37.4	51.1	49.9	66.5	64.9	88.7	86.6	118	115	158	154
10001b	105d / D2h	18.2	20	24.9	27.4	34.0	37.4	45.3	49.9	57.6	64.9	78.7	86.6	105	115	140	154
10010b	106d / D4h	16.2	20	22.1	27.4	30.1	37.4	40.2	49.9	51.1	64.9	69.8	86.6	93.1	115	124	154
10011b	107d / D6h	14.3	20	19.6	27.4	26.7	37.4	35.7	49.9	45.3	64.9	61.9	86.6	82.5	115	110	154
10100b	108d / D8h	12.4	20	17.4	27.4	23.2	37.4	30.9	49.9	40.2	64.9	53.6	86.6	71.5	115	95.3	154
10101b	109d / DAh	11.0	20	15.0	27.4	20.5	37.4	27.4	49.9	35.7	64.9	47.5	86.6	63.4	115	84.5	154
10110b	110d / DCh	9.5	20	13.3	27.4	18.2	37.4	24.3	49.9	30.9	64.9	41.2	86.6	54.9	115	75.0	154
10111b	111d / DEh	8.5	20	11.5	27.4	15.8	37.4	21.0	49.9	26.7	64.9	36.5	86.6	48.7	115	64.9	154
11000b	112d / E0h	7.2	20	9.8	27.4	13.3	37.4	17.8	49.9	23.2	64.9	30.9	86.6	41.2	115	54.9	154
11001b	113d / E2h	6.2	20	8.5	27.4	11.5	37.4	15.4	49.9	19.6	64.9	26.7	86.6	35.7	115	47.5	154
11010b	114d / E4h	5.1	20	7.2	27.4	9.5	37.4	13.0	49.9	16.5	64.9	22.1	86.6	29.4	115	40.2	154
11011b	115d / E6h	4.2	20	5.8	27.4	7.9	37.4	10.5	49.9	13.7	64.9	18.2	86.6	24.3	115	32.4	154
11100b	116d / E8h	3.4	20	4.6	27.4	6.3	37.4	8.5	49.9	11.0	64.9	14.7	86.6	19.6	115	26.1	154
11101b	117d / EAh	2.6	20	3.6	27.4	4.9	37.4	6.5	49.9	8.5	64.9	11.3	86.6	15.0	115	20.0	154
11110b	118d / ECh	1.9	20	2.6	27.4	3.5	37.4	4.6	49.9	6.0	64.9	8.1	86.6	10.7	115	14.3	154
11111b	119d / EEh	1.2	20	1.6	27.4	2.2	37.4	2.9	49.9	3.7	64.9	5.0	86.6	6.7	115	8.9	154

Table 7-3. VBOOT_CHA Pinstrap Decoding

	R_{LB} = 20.0 kΩ LSB = 000b		R_{LB} = 27.4 kΩ LSB = 001b		R_{LB} = 37.4 kΩ LSB = 010b		R_{LB} = 49.9 kΩ LSB = 011b		R_{LB} = 64.9 kΩ LSB = 100b		R_{LB} = 86.6 kΩ LSB = 101b		R_{LB} = 115.0 kΩ LSB = 110b		R_{LB} = 154.0 kΩ LSB = 111b	
MSB	V_{BOOTA} (V)	R_{HB} (kΩ)	V_{BOOTA} (V)	R_{HB} (kΩ)	V_{BOOTA} (V)	R_{HB} (kΩ)	V_{BOOTA} (V)	R_{HB} (kΩ)	V_{BOOTA} (V)	R_{HB} (kΩ)	V_{BOOTA} (V)	R_{HB} (kΩ)	V_{BOOTA} (V)	R_{HB} (kΩ)	V_{BOOTA} (V)	R_{HB} (kΩ)
00000b	Do Not Use		0.25	1780	0.26	2430	0.27	3240	0.28	4220	0.29	5620	0.3	7500	0.31	9760
00001b	0.32	422	0.33	576	0.34	787	0.35	1050	0.36	1370	0.37	1820	0.38	2430	0.39	3240
00010b	0.4	249	0.41	340	0.42	464	0.43	619	0.44	806	0.45	1070	0.46	1430	0.47	1910
00011b	0.48	169	0.49	232	0.5	316	0.51	422	0.52	549	0.53	732	0.54	976	0.55	1300
00100b	0.56	127	0.57	174	0.58	237	0.59	316	0.6	412	0.61	549	0.62	732	0.63	976
00101b	0.64	102	0.65	140	0.66	191	0.67	255	0.68	332	0.69	442	0.7	576	0.71	787
00110b	0.72	82.5	0.73	113	0.74	154	0.75	205	0.76	267	0.77	357	0.78	475	0.79	634
00111b	0.8	68.1	0.81	95.3	0.82	130	0.83	174	0.84	226	0.85	301	0.86	392	0.87	536
01000b	0.88	59	0.89	80.6	0.90	110	0.91	147	0.92	191	0.93	255	0.94	332	0.95	453
01001b	0.96	49.9	0.97	68.1	0.98	93.1	0.99	124	1	162	1.01	215	1.02	287	1.03	383
01010b	1.04	43.2	1.05	59	1.06	80.6	1.07	110	1.08	140	1.09	187	1.1	249	1.11	332
01011b	1.12	38.3	1.13	52.3	1.14	71.5	1.15	95.3	1.16	124	1.17	165	1.18	221	1.19	294
01100b	1.2	33.2	1.21	45.3	1.22	61.9	1.23	82.5	1.24	107	1.25	143	1.26	191	1.27	255
01101b	1.28	29.4	1.29	40.2	1.3	54.9	1.31	73.2	1.32	95.3	1.33	127	1.34	169	1.35	226
01110b	1.36	26.1	1.37	35.7	1.38	48.7	1.39	64.9	1.4	84.5	1.41	113	1.42	150	1.43	200
01111b	1.44	23.2	1.45	31.6	1.46	43.2	1.47	57.6	1.48	75	1.49	97.6	1.5	133	1.51	178
10000b	1.52	20.5	1.53	28	1.54	38.3	1.55	51.1	1.56	66.5	1.57	88.7	1.58	118	1.59	158
10001b	1.6	18.2	1.61	24.9	1.62	34	1.63	45.3	1.64	59	1.65	78.7	1.66	105	1.67	140
10010b	1.68	16.2	1.69	22.1	1.7	30.1	1.71	40.2	1.72	52.3	1.73	69.8	1.74	93.1	1.75	124
10011b	1.76	14.3	1.77	19.6	1.78	26.7	1.79	35.7	1.8	46.4	1.81	61.9	1.82	82.5	1.83	110
10100b	1.84	12.4	1.85	17.4	1.86	23.2	1.87	30.9	1.88	40.2	1.89	53.6	1.9	71.5	1.91	95.3
10101b	1.92	11	1.93	15	1.94	20.5	1.95	27.4	1.96	35.7	1.97	47.5	1.98	63.4	1.99	84.5
10110b	2	9.53	2.01	13.3	2.02	18.2	2.03	24.3	2.04	30.9	2.05	41.2	2.06	54.9	2.07	75
10111b	2.08	8.45	2.09	11.5	2.1	15.8	2.11	21	2.12	27.4	2.13	36.5	2.14	48.7	2.15	64.9
11000b	2.16	7.15	2.17	9.76	2.18	13.3	2.19	17.8	2.2	23.2	2.21	30.9	2.22	41.2	2.23	54.9
11001b	2.24	6.19	2.25	8.45	2.26	11.5	2.27	15.4	2.28	20	2.29	26.7	2.30	35.7	2.31	47.5
11010b	2.32	5.11	2.33	7.15	2.34	9.53	2.35	13	2.36	16.9	2.37	22.1	2.38	29.4	2.39	40.2
11011b	2.4	4.22	2.41	5.76	2.42	7.87	2.43	10.5	2.44	13.7	2.45	18.2	2.46	24.3	2.47	32.4
11100b	2.48	3.4	2.49	4.64	2.50	6.34	2.51	8.45	2.52	11	2.53	14.7	2.54	19.6	2.55	26.1
11101b	2.56	2.61	2.57	3.57	2.58	4.87	2.59	6.49	2.60	8.45	2.61	11.3	2.62	15	2.63	20
11110b	2.64	1.87	2.65	2.55	2.66	3.48	2.67	4.64	2.68	6.04	2.69	8.06	2.70	10.7	2.71	14.3
11111b	2.72	1.15	2.73	1.58	2.74	2.15	2.75	2.87	2.76	3.74	2.77	4.99	3.3 [(1)]	6.65	5 [(1)]	8.87

(1) Requires the use of an external output voltage divider.

7.4.5 Enable and disable: AVR_EN and BVR_EN

The ON_OFF_CONFIG command controls the conditions which TPS536C7B1 requires to enable power conversion. By default only the AVR_EN (active high) pin enables channel A, and only the BVR_EN pin (active high) enables channel B. This command can program the controller ignore the VR_EN pins and require the OPERATION command to be sent to enable power conversion, or even require a combination of the two.

When enabled, first the controller waits for a delay time given by TON_DELAY, then ramps the output voltage at a controlled slew rate SR_{BOOT}. The device requires 750 µs typically (up to 1.0 ms), to begin ramping the output voltage, after being enabled. Turn-on delay added by the TON_DELAY is in addition to this delay.

The ON_OFF_CONFIG command also controls the turn-off behavior. When configured for *immediate-off*, the controller immediately tri-states all PWM pins assigned to that channel and stops transferring power immediately. When configured for *soft-off* the controller first waits for the TOFF_DELAY time, then actively ramps down the output voltage at a controlled slew rate.

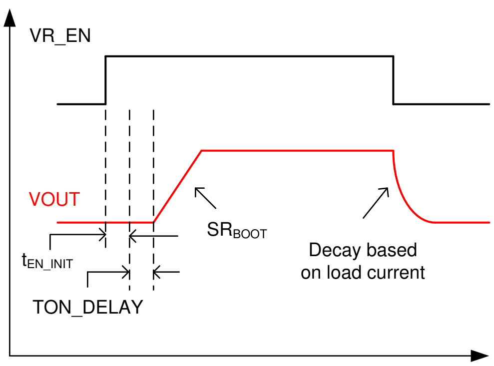


Figure 7-5. Soft-start and immediate-off (decay)

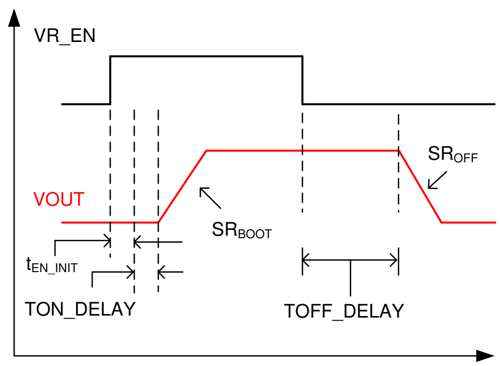


Figure 7-6. Soft-start and soft-off

The TON_RISE and TOFF_FALL commands are used to calculate the turn-on and turn-off (in the case of soft-off) slew rates. While these commands are numerically programmable from 0 to 31.75 ms, only a limited set of slew rates are supported. During enable, the device calculates the target rising and falling slew rates according to Equation 1 and Table 7-4, then selects the nearest available value from Table 7-4.

$$SR_{BOOT} = LOOKUP\left(\frac{VOUT\_COMMAND}{TON\_RISE}\right) \quad (1)$$

$$SR_{OFF} = LOOKUP\left(\frac{VOUT\_COMMAND}{TOFF\_FALL}\right) \quad (2)$$

Table 7-4. Supported SR_{BOOT} and SR_{OFF} slew rates

Supported slew rates (mV/µs)	
0.093	0.313
0.097	0.625
0.101	0.938
0.105	1.250
0.111	1.563
0.117	1.875
0.124	2.188
0.131	2.50
0.140	5.00
0.151	10.00
1.163	15.00
0.175	20.00
0.192	25.00

Table 7-4. Supported SR_{BOOT} and SR_{OFF} slew rates (continued)

Supported slew rates (mV/µs)	
0.213	30.00
0.238	35.00
0.265	40.00

Example: VOUT_COMMAND = 0.88 V, TON_RISE = 1.0 ms

The target slew rate is calculated as SR_{BOOT} = LOOKUP(880 mV/1000 µs) = 0.88 mV/µs. The nearest supported value of 0.9375 mV/µs is selected.

The expected rise time is approximately (880 mV / 0.9375 mV/µs) ≈ 940 µs.

7.4.6 System feedback: AVR_RDY and BVR_RDY

The AVR_RDY and BVR_RDY pins are used to signal to the system, when each channel is in regulation. These pins are open drain structures, and require external pull-up resistors. During boot-up, the VR_RDY pins are released when the internal reference DAC reaches the boot voltage. Any condition which causes the channel to stop converting power, causes its VR_RDY pin to pull low. This includes any fault protection-related shutdown, or the channel simply being disabled. The VR_RDY pins do not assert to alert the host to any warning conditions or faults configured to be ignored.

7.4.7 Catastrophic fault alert: VR_FAULT#

The VR_FAULT# pin is an open drain output which alerts the system to potentially catastrophic power supply faults. The VR_FAULT# pin is an open drain structure. Connect an external pull-up resistor to this pin.

Only the most critical fault conditions assert the VR_FAULT# pin. Fault responses configured to be ignored do not assert the VR_FAULT# pin. The VR_FAULT_CONFIG PMBus command provides some options to control which fault conditions cause this pin to assert.

Fault conditions which assert the VR_FAULT# pin include:

- Over-voltage fault (including pre-bias OVP, fixed OVP, and tracking OVP)
- Powerstage fault (TAO_HIGH)
- Input overcurrent fault
- Output overcurrent fault (configurable)
- Over-temperature fault (configurable)
- Faults from channel A only, or channel A+B (configurable)

7.4.8 Output voltage reset: RESET#

By default, pin 19 functions as the channel B enable pin, BVR_EN. Use the command to assign pin 19 as a hardware voltage reset signal, RESET#, as needed. When pin 19 is not assigned as BVR_EN, the AVR_EN pin becomes a shared enable pin for both channels. RESET# is an active-low signal. Connect an external pull-up to this pin to make its default state high (e.g. not in reset).

Asserting the RESET# pin low during regulation causes the output voltage of both channels to slew back to their respective V_{BOOT} values, at the slew rate defined by . While RESET# is asserted low, new output voltage targets from PMBus are ignored. Figure 7-7 describes the behavior of the RESET# pin.

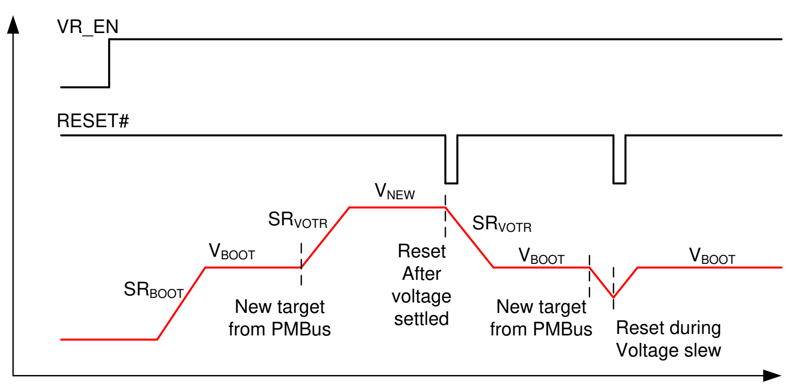


Figure 7-7. RESET# behavior

The RESET# pin is not a global reset pin for the device. Asserting RESET# changes only the output voltage target of both channels. RESET# does not cause any operating state change or re-initialization.

7.4.9 Synchronization: SYNC

By default, pin 19 functions as the channel B enable pin, BVR_EN. Use the MULTIFUNCTION_PIN_CONFIG command to assign pin 19 as a synchronization pin as needed. When pin 19 is not assigned as BVR_EN, the AVR_EN pin becomes a shared enable pin for both channels. When there is no SYNC pin assigned, configure the SYNC_CONFIG to operate based on internal timing, in order to maintain an accurate switching frequency over the full range of operation. Any external clock applied to must have a 50% duty cycle, and the FREQUENCY_SWITCH command must still be programmed as close as possible to the desired switching frequency after any scaling. The input on the SYNC pin must be ±50 kHz from the configured FREQUENCY_SWITCH value.

An internal phase-locked loop (PLL) adjusting the on-time of each phase enables edge synchronization. During steady-state operation, when synchronization is used, the PWM pin assigned to order 0 is synchronized to a clock on the SYNC pin. The DCAP+ control topology is inherently a variable frequency scheme. During load transients, the pulse frequency of each channel modulates to maintain voltage regulation. Load transients cause the PLL to lose phase lock, and slowly return to phase lock based on the PLL loop bandwidth. The PLL bandwidth is much slower than the voltage regulation loop, and it can take many cycles for the PLL to re-lock following a transient event. Figure 7-8 illustrates the DCAP+ response to a load transient using edge synchronization.

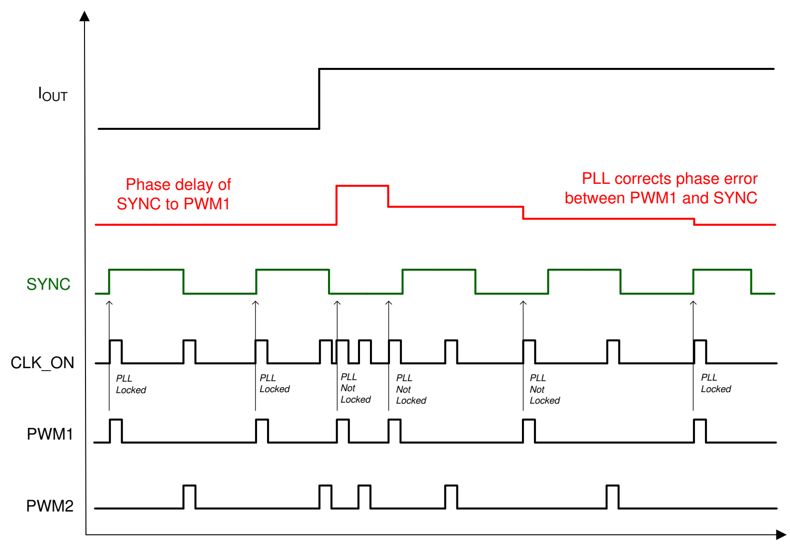


Figure 7-8. Synchronization behavior (2 phase example, no phase shift)

The SYNC_CONFIG command configures various options related to synchronization. These include: enable/disable of the PLL, sync direction (clock master or clock slave), input clock division ratio, phase shift, and gain/scalar terms to increase/decrease the PLL loop bandwidth. Refer to the *Technical Reference Manual* for a complete register map.

Figure 7-9 and Figure 7-10 illustrate two common methods of synchronizing multiple converters based on TPS536C7B1. Use the programmable phase shift parameters to phase spread multiple converters, to improve ripple cancellation and reduce beat frequencies on input supplies.

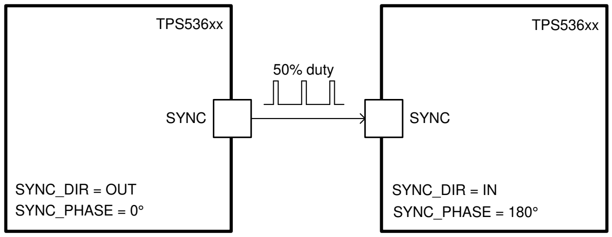


Figure 7-9. Clock master driving a clock slave

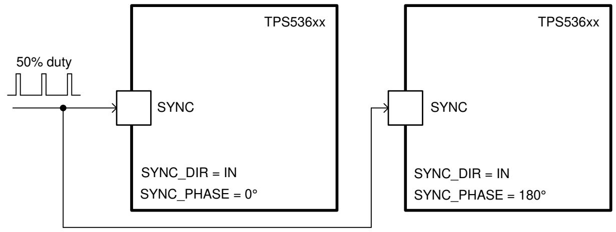


Figure 7-10. Two clock slaves driven externally

7.4.10 Smart power stage connections: PWM, CSP and TSEN

Interface the controller to TI smart power stage devices, as shown in Figure 7-11.

Connect the PWM pins of the controller to the PWM pins of the power stage devices. The PWM pins are three-state logic outputs of the controller. A PWM pin being logic-high commands the power stage device to turn its high-side FET on, and its low-side FET off. A PWM pin being logic-low commands the power stage device to turn its low-side FET on and its high-side FET off. TI power stage devices provide a weak drive on their PWM pins, causing them to float to a mid-level value when the controller stops driving them. During enable, or dynamic phase addition, the controller starts phases switching with a transition from tri-state to high. Similarly, during disable or dynamic phase shedding, the controller disables phases with a transition from low-to-tri-state. Float unused PWM pins on the controller.

Connect the IOUT pins of the powerstage devices to the CSP pins of the controller. Connect the VREF pin of the controller to the REFIN pins of the powerstage devices. A local bypass capacitor C_{VREF}, is required for the controller VREF pin. Optionally, add a local VREF bypass capacitor at the powerstage devices. VREF provides common-mode voltage for the IOUT signal, which is a voltage representing the output current of each powerstage with a nominal gain of 5 mV/A. Float unused CSP pins on the controller.

Connect the TAO/FAULT pins of all powerstages within a channel to each other, and to the corresponding TSEN pin of the controller. For example, tie all TAO/FAULT pins of powerstages used on channel A together and to the controller ATSEN pin. TI recommends adding a 2200 pF capacitor to the TSEN pins at the controller to reduce temperature measurement noise. TI recommends keeping a place holder for a 1000 pF capacitor at the powerstage side. Refer to the individual powerstage datasheet for more detailed recommendations. During normal operation, the TSEN pins provide a voltage signal proportional to the temperature of the warmest powerstage device according to Equation 3 . During a UVLO condition, the powerstages pull the shared TAO line low to inform the controller they are not able to accept PWM input. When powerstages detect a fault condition internally, they pull the shared TAO pin high to inform the controller a fault condition has occurred. If channel B is not used, float the BTSEN pin.

$$\text{READ\_TEMPERATURE\_1} = \left(\frac{V_{TSEN} - 600\text{mV}}{8\text{mV}}\right)°\text{C} \tag{3}$$

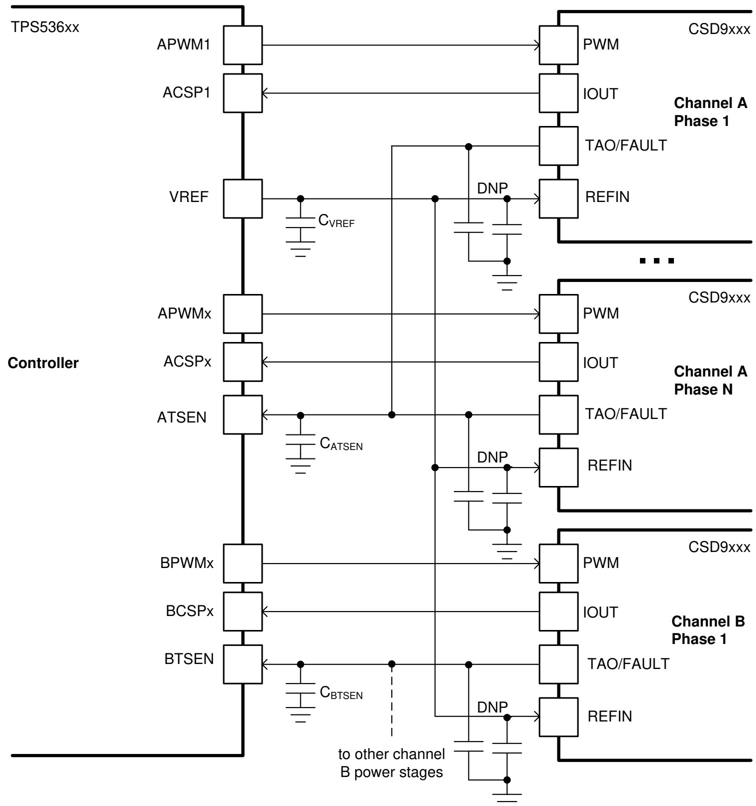


Figure 7-11. Power stage pin connections

7.4.11 PMBus pins: SMB_DIO, SMB_CLK, and SMB_ALERT#

The SMB_CLK, SMB_DIO, and SMB_ALERT# pins are used for PMBus communication, an open-drain interface. TPS536C7B1 is compatible with both 1.8-V and 3.3-V logic levels as shown in to Part I of the PMBus specification, revision v1.3.1. At least one external pull-up resistor is required for these pins. The 100 kHz, 400 kHz and 1 MHz modes of operation are supported. PMBus is a shared bus, where devices are assigned a communication address. Select the PMBus slave address as described in Section 7.4.4. The controller device stretches clock pulses during operation when more processing time is required. Clock stretching support in the PMBus master is mandatory. See the Section 7.9 section for more information about PMBus functionality.

7.5 Advanced power management functions

7.5.1 Adaptive voltage scaling or dynamic VID (DVID) through VOUT_COMMAND

Figure 7-12 shows a conceptual view of the TPS536C7B1 output voltage control, and dynamic behavior.

Update the VOUT_COMMAND value through PMBus to change the output voltage of each channel on-the-fly. Optionally, use the OPERATION command to toggle the output voltage bewteen the VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW and VOUT_COMMAND values. This is described in more detail in Output voltage margining.

The VOUT_MAX and VOUT_MIN commands define the maximum and minimum allowed voltage, through any combination of offsets and voltage target commands. If commanded higher or lower than these limits, the output voltage transitions to these limits and stops.

The soft-start and soft-off slew rates are calculated using the current output voltage target and TON_RISE and TOFF_FALL command values. All output voltage transitions which occur during normal power conversion follow the slew rate defined by VOUT_TRANSITION_RATE.

The VOUT_SCALE_LOOP parameter must be set properly when an external output voltage divider is being used. This value is used internally to provide scaling for all output voltage related parameters.

Update the VOUT_TRIM value to apply a static offset to the output voltage target. This may be used to fine-tune the output voltage in production, or null any board related offsets.

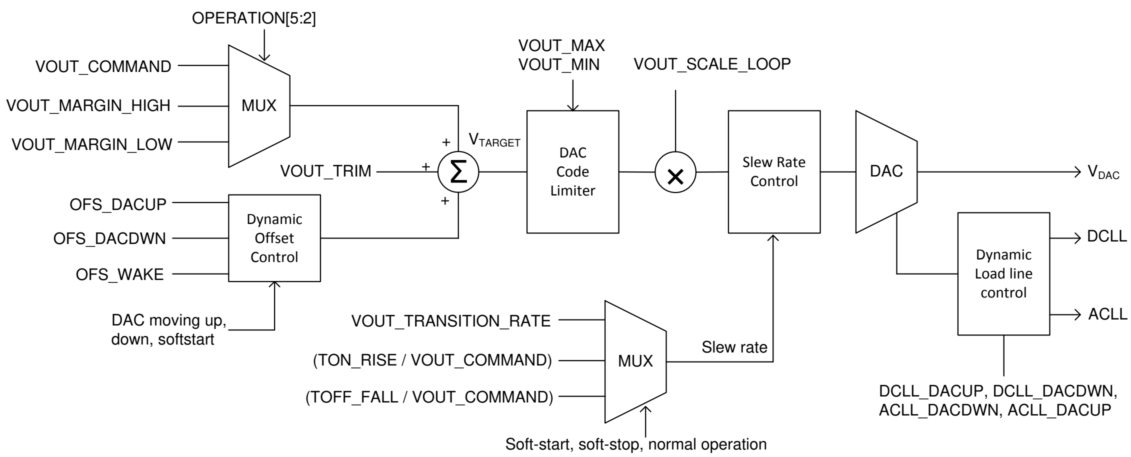


Figure 7-12. Output voltage control conceptual view

TPS536C7B1 provides several options to fine-tune the controller response to high speed output voltage transitions. For example, large output voltage steps upward cause an inrush current, required to charge the output capacitors for that channel. This inrush current combined with the DC load line setting make the output voltage appear to move more slowly than the commanded slew rate. Use the DVID_CONFIG command to configure *dynamic* loadlines and offsets which apply only during output voltage transitions. Typically, set the DC and AC load lines for upward moving transitions to a value equal or lower than the nominal. Similarly, typically, set the DC and AC loadlines to a value larger than the nominal value for downward moving transitions. Refer to the *Technical Reference Manual* for a register map of this command.

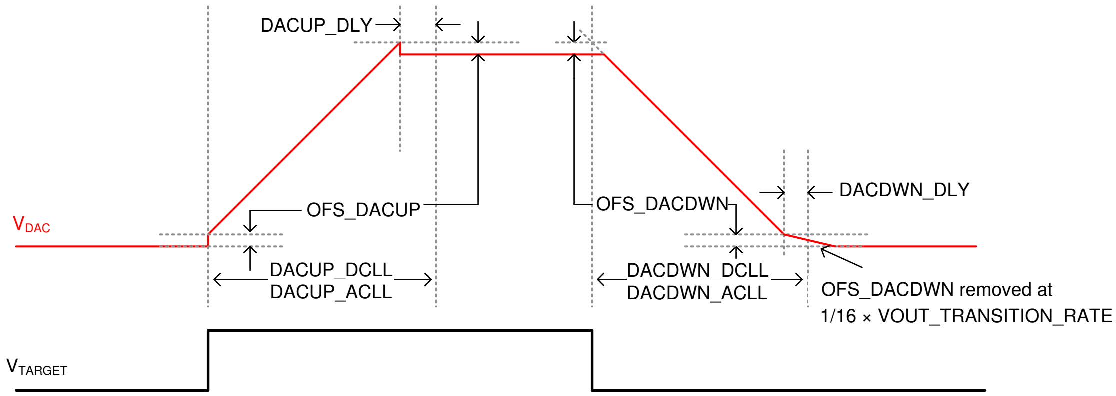


Figure 7-13. Dynamic load line and offset control

The DVID_CONFIG command also allows the user to configure dynamic offsets which are only applied during output voltage transitions. The configured *recovery delays* determine when the load line and offset values return to nominal settings, in terms of PWM (order 0) cycle counts. Figure 7-13 illustrates the dynamic load line, offset and recovery delay behavior of the controller.

7.5.2 Output voltage margining

Output voltage margin testing allows power designers to test the response of their system to across output voltage tolerance corners.

The MARGIN bits in the OPERATION command can be used to toggle the active channel between several states:

Table 7-5. Supported MARGIN settings

MARGIN bits	Description	Output voltage target	Voltage fault detection
0000b	Margin none	VOUT_COMMAND	Enabled
0101b	Margin low (act on faults)	VOUT_MARGIN_LOW	Enabled
0110b	Margin low (ignore on faults)	VOUT_MARGIN_LOW	Disabled
1001b	Margin high (act on faults)	VOUT_MARGIN_HIGH	Enabled
1010b	Margin high (ignore on faults)	VOUT_MARGIN_HIGH	Disabled
Other	Not supported/invalid data		

Example procedure: voltage margin (ignore fault) testing

1. Write to the PAGE command to select the desired channel (E.g. 00h for channel A).
2. Write VOUT_COMMAND to the desired value during margin none operation.
3. Write VOUT_MARGIN_LOW to the desired value during margin low operation.
4. Write VOUT_MARGIN_HIGH to the desired value during margin high operation.
5. Write the ON_OFF_CONFIG command to ensure the device is configured to respect the OPERATION command.
6. Toggle to margin none operation. Write OPERATION to 80h.
7. Toggle to margin low (ignore fault) operation. Write OPERATION to 94h.
8. Toggle to margin high (ignore fault) operation. Write OPERATION to A4h.

7.5.3 Power supply telemetry and calibration

Table 7-6 summarizes the available telemetry functions through PMBus.

Table 7-6. Summary of telemetry functions

Parameter	Sensed Signal(s)	Shared/ Paged/ Phased	PMBus Command(s)	Range	Update Rate and filter time constant
Output voltage	VSP-VSN	Paged	READ_VOUT	0 to 3.74 V (VOUT_SCALE_LOOP=1.0) 0 to 5.5 V (VOUT_SCALE_LOOP=0.5)	24 µs update + 330 µs time const.
Output current	CSP1 to CSP12	Paged	READ_IOUT (PHASE=FFh) IOUT_CAL_GAIN IOUT_CAL_OFFSET	(-10.0 to 70.0 A) × N_ϕ + Offset	24 µs update + 290 µs time const.
Per-phase current	CSP1 to CSP12	Paged, Phased	READ_IOUT (PHASE=00h, 01h, ...) IOUT_CAL_OFFSET	-10.0 to 70.0 A per phase	20 µs update + 300 µs time const.
Output power	Calculated (V_{OUT} × I_{OUT})	Paged	READ_POUT	Per READ_VOUT and READ_IOUT	
Power stage temperature	ATSEN, BTSEN	Paged	READ_TEMPERATURE_1	-40 to 165 °C	150 µs update + 650 µs time const.
Input voltage	VIN_CSNIN	Shared	READ_VIN	0.0 to 18.7 V	150 µs update + 660 µs time const.
Input current	CSPIN, VIN_CSNIN	Shared	READ_IIN MFR_CALIBRATION_ CONFIG	-5.0 to 100.0 A	24 µs update + 440 µs time const.
Input power	Calculated (V_{IN} × I_{IN})	Shared	READ_PIN	Per READ_VIN and READ_IIN	

No sensor gain or offset calibration is required for output voltage, temperature or input voltage telemetry.

7.5.3.1 Output current calibration

Use the IOUT_CAL_GAIN to adjust the gain of the output current telemetry. One gain setting is provided which applies to all phases in the channel. Use the IOUT_CAL_OFFSET to adjust the current measurement offset for each phase. The offset for the total channel is calculated as a sum of the configured offsets for all phases. During power supply characterization use the PHASE_CONFIG command to configure the controller for 1-phase mode, to enable measurement of a single phase measurement offset. Refer to the example below.

The READ_IOUT command value is calculated according to Equation 4 and Equation 5.

$$\mathrm{READ\_IOUT_{TOTAL}} = \frac{1}{\mathrm{IOUT\_CAL\_GAIN}} \times \sum_{\mathrm{phases}}^{\mathrm{active}} (\mathrm{CSP_i} - \mathrm{VREF}) + \sum_{\mathrm{phases}}^{\mathrm{active}} \mathrm{IOUT\_CAL\_OFFSET_i} \quad (4)$$

where

- $\mathrm{READ\_IOUT_{TOTAL}}$ is the total output current telemetry value, accessible with PHASE=FFh
- IOUT_CAL_GAIN is the output current gain setting (one per channel)
- CSP_i is the voltage of the current sense signal from each power stage
- VREF is the digitized value of the internal 1.5-V LDO

- $IOUT\_CAL\_OFFSET_i$ is the output current offset setting for each phase

$$READ\_IOUT_{PHASE\ i} = \frac{1}{IOUT\_CAL\_GAIN} \times \left(CSP_i - VREF\right) + IOUT\_CAL\_OFFSET_i \quad (5)$$

where

- $READ\_IOUT_{PHASE\ i}$ is the per-phase current telemetry value, accessible with PHASE=00h for phase 1, 01h for phase 2, etc ...
- IOUT_CAL_GAIN is the output current gain setting (one per channel)
- CSP_i is the voltage of the current sense signal for that phase
- VREF is the digitized value of the internal 1.5-V LDO
- $IOUT\_CAL\_OFFSET_i$ is the output current offset setting for that phase

Example procedure: Per-Phase calibration of READ_IOUT

First select the correct IOUT_CAL_GAIN for the whole channel:

1. With all phases active, apply the first load current, I_{OUT1}, to the converter and wait for the READ_IOUT value to stabilize. Read-back and record the value of READ_IOUT as I_{MON1}.
2. With all phases active, apply the second load current, I_{OUT2}, to the converter and wait for the READ_IOUT value to stabilize. Read-back and record the value of READ_IOUT as I_{MON2}.
3. Calculate the new gain setting according to Equation 6.
4. Write the PAGE to the current channel, and the PHASE to FFh.
5. Write the newly calculated value to IOUT_CAL_GAIN.
6. Perform an NVM Store operation and power cycle.

$$IOUT\_CAL\_GAIN_{new} = \frac{I_{OUT2} - I_{OUT1}}{I_{MON2} - I_{MON1}} \times IOUT\_CAL\_GAIN_{current} \quad (6)$$

Next, select the IOUT_CAL_OFFSET for each phase according to the procedure below:

1. Record the current values of PHASE_CONFIG and IOUT_CAL_OFFSET for each phase.
2. Adjust the TON_RISE temporarily to accomodate enabling power conversion with one phase only active, if needed.
3. With power conversion disabled for both channels, update the PHASE_CONFIG command so that only the first phase is active, and its assigned ORDER is 0.
4. Enable power conversion through the VR_EN pins or OPERATION as configured through ON_OFF_CONFIG.
5. Apply a known load current, I_{OUT1}. Wait for the READ_IOUT to stabilize and record the value as I_{MON1}.
6. Calculate the new IOUT_CAL_OFFSET per Equation 7, where *i* is the currently configured phase.
7. Store the newly calculated offset for the first phase value in memory temporarily.
8. Repeat steps 3-7 for each phase in the converter.
9. Disable power conversion.
10. Set the PHASE_CONFIG back to the original value.
11. Write the PAGE to the current channel, and the PHASE to 00h for the first phase.
12. Write the newly calculated IOUT_CAL_OFFSET value.
13. Repeat steps 11-12 for each phase. PHASE value 01h refers to the 2nd phase, 02h refers to the 3rd phase and so on.
14. Re-set the TON_RISE to the desired value during normal operation, if needed.
15. Perform an NVM Store operation and power cycle.

$$IOUT\_CAL\_OFFSET_{new} = I_{OUT\ i} - \left(I_{MON\ i} + IOUT\_CAL\_OFFSET_{current}\right) \quad (7)$$

7.5.3.2 Input current calibration (measured)

Use MFR_CALIBRATION_CONFIG command to adjust the gain and offset of the input current sensor. First, set analog front-end gain such to keep the signal at the ADC to be less than 800 mV. Then set the digital gain to fine-tune the total gain based on the selected input current shunt. Finally adjust the input current offset based on lab measurements. A detailed example of input current sensor calibration is shown in Input current sensing: VIN_CSNIN and CSPIN.

The equation for input current sense measurements is shown in Equation 8.

$$READ\_IIN = I_{IN} \times R_{SENSE} \times G_{INSHUNT} \times \left(\frac{G_{IINMAX}}{800\ mV}\right) + IIN\_OFS \quad (8)$$

where

- I_{IN} is the true input current in amperes
- R_{SENSE} is the effective sense element gain in ohms
- $G_{INSHUNT}$ is the analog front-end gain
- G_{IINMAX} is a digital-domain gain factor used for fine tuning
- IIN_OFS is an offset factor applied to the resulting value in amperes

Estimate the maximum input current for the design using Equation 9.

$$I_{IN(MAX)} = \left(\frac{V_{OUT(A)} \times I_{PEAK(A)}}{V_{IN} \times \eta_{IPEAK(A)}} + \frac{V_{OUT(B)} \times I_{PEAK(B)}}{V_{IN} \times \eta_{IPEAK(B)}}\right) \times K_{MARGIN} \quad (9)$$

where

- $V_{OUT(A)}$ and $V_{OUT(B)}$ are the output voltage for channels A and B respectively
- $I_{PEAK(A)}$ and $I_{PEAK(B)}$ are the peak design currents for channels A and B respectively
- V_{IN} is the input voltage for the design
- $\eta_{IPEAK(A)}$ and $\eta_{IPEAK(B)}$ are the full-load conversion efficiency for channels A and B respectively
- K_{MARGIN} is a factor of safety used for design margin

Select the analog front-end gain, $G_{IINSHUNT}$, to maximize the signal level at the ADC whie remaining within its full scale range of 800 mV. Select the closest available value less than the result of Equation 10.

$$G_{IINSHUNT} \le \frac{800\ mV}{I_{IN(MAX)} \times R_{SENSE}} \quad (10)$$

Finally select the digital gain factor, G_{IINMAX}, with a resolution of 0.5 per LSB, to fine-tune the current sense gain using Equation 11.

$$G_{IINMAX} = \frac{800\ mV}{G_{IINSHUNT} \times R_{SENSE}} \quad (11)$$

Example: 12V to 0.88 V 12+0 design at 400 A / 25 A, R_{SENSE} = 0.3 mΩ

Channel B is not used in this design. Estimate the maximum input current, according to the calculation below.

$$I_{IN(MAX)} = \left(\frac{1.8V \times 400A}{12V \times 95\%} + \frac{1.0V \times 25A}{12V \times 90\%}\right) \times 1.25 = 82A$$

Select the analog front-end gain, and digital gain factors as shown below. Set the IIN_OFS should to 0.0 A, and tune the value based on design characterization measurements.

$$G_{IINSHUNT} \le \frac{800mV}{82A \times 0.2m\Omega} \rightarrow G_{IINSHUNT} = 40$$

$$G_{IINMAX} = \frac{800mV}{40 \times 0.2m\Omega} \approx 100$$

Finally, the calibrated input current measurement is verified to be calibrated properly.

$$READ\_IIN = I_{IN} \times 0.2m\Omega \times 40 \times \left(\frac{100}{800mV}\right) \approx 1.0 \times I_{IN}$$

7.5.3.3 Input current calibration (calculated)

Applications which do not use measured current sensing can still report calculated input current based on the output voltage, output current and input voltage of each channel. To use calculated input current reporting, connect the VIN_CSNIN and CSPIN pins together, and to the input voltage. A connection to the input voltage is still required for the control loop to set the correct on-time. Use the CALCIIN_RD setting in MISC_OPTIONS to enable calculated input current reporting. The controller estimates the converter power efficiency for each channel by comparing the actual on-time of the PWM pins, which get wider as the conversion loss increases to maintain voltage and frequency regulation, to the idealized on-time assuming no power loss. Fine-tune the gain of the calculated input current measurement through PMBus, using the MFR_CALIBRATION_CONFIG command.

$$I_{IN(CALC)} = \frac{V_{OUT(A)} \times I_{OUT(A)}}{V_{IN} \times \eta_{est(A)} \times \mathrm{CALCIIN\_EFF\_A}} + \frac{V_{OUT(B)} \times I_{OUT(B)}}{V_{IN} \times \eta_{est(B)} \times \mathrm{CALCIIN\_EFF\_B}} \qquad (16)$$

where

- $V_{OUT(A)}$ is the output voltage telemetry value for channel A
- $IOUT_{(A)}$ is the output current telemetry value for channel A
- V_{IN} is the input current telemetry value (shared)
- $\eta_{est(A)}$ is the controller's estimated conversion efficiency on channel A
- CALCIIN_EFF_A is the PMBus programmable gain factor to fine-tune the current gain for channel A
- $V_{OUT(B)}$ is the output voltage telemetry value for channel B
- $IOUT_{(B)}$ is the output current telemetry value for channel B
- $\eta_{est(B)}$ is the controller's estimated conversion efficiency on channel B
- CALCIIN_EFF_B is the PMBus programmable gain factor to fine-tune the current gain for channel B

7.5.4 Flexible phase assignment

Use the PHASE_CONFIG command to assign each PWM pin to a logical phase number. By default, phase configuration settings are derived from pinstrapping and not from non-volatile memory. Refer to Section 7.4.4, for more information about enabling NVM phase configuration settings. Refer to the *Technical Reference Manual* for a register map of the PHASE_CONFIG command. Each PWM pin has 4 available settings:

- **ENABLE:** Controls whether the phase is active or remains at tristate always.
- **PAGE:** Assigns each phase to channel A or channel B. This setting also determines which CSP pins are incorporated in the I_{SUM} control signals for each channel.
- **PHASE:** Assigns each phase within a channel a PHASE setting at which it can be addressed. The PHASE assignment is not backed by non-volatile memory, and each phase is assigned a derived PHASE setting at power-on.
- **ORDER:** Controls the order in which phases are fired with respect to each other. Figure 7-14 and Figure 7-15 illustrate the effect of different ordering assignments. Reconfigure the phase ordering to ensure adjacent phases do not interfere with each other due to layout related coupling issues. If dynamic phase shedding is used, phases add or drop according to their assigned ORDER value.

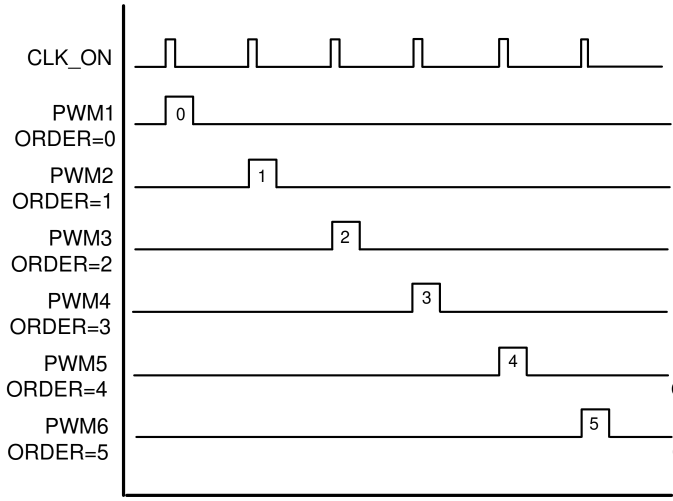


Figure 7-14. 0-1-2-3-4-5 fire order (6 phase example)

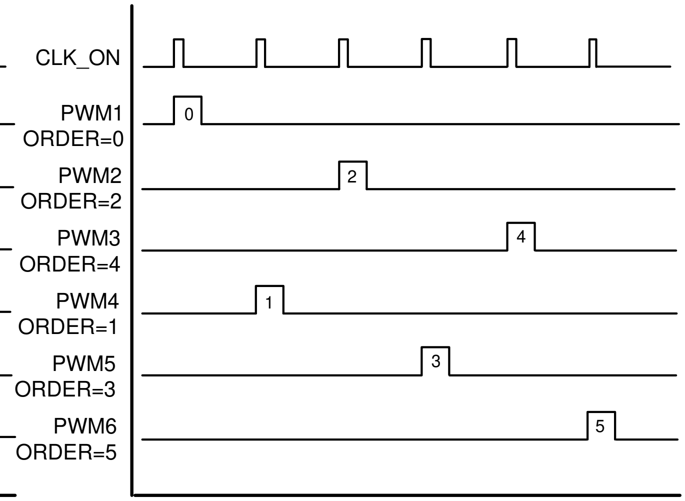


Figure 7-15. 0-2-4-1-3-5 fire order (6 phase example)

Observe the following rules when updating the phase configuration settings. The *Fusion Digital Power Designer* GUI enforces these rules, but the controller itself does not:

- Channel A may be assigned up to 12 phases. Channel B may be assigned up to 6 phases.
- The ORDER assignments within a channel must be continuous, and start at 0. Do not skip phase order assignments.
- The PHASE assignments within a channel must be continuous, start at 0 counting upward from APWM1 for channel A and downward from APWM12/BPWM1 for channel B.

Example: 8+2 phase configuration with non-standard fire order

1. Write the PIN_DETECT_OVERRIDE command to ensure the controller takes its phase configuration from non-volatile memory at the next power-up.
2. Write the PHASE_CONFIG command as shown below.
3. Issue STORE_USER_ALL. At the next power-on, the phase configuration is restored from NVM.

Table 7-7. Example settings: 8+2, 0-2-4-6-1-3-5-7 ordering

Pin Name	Bit Numbers	Phase Enable	PAGE	PHASE	ORDER
APWM12/BPWM1	191:176	1	1	0	0
APWM11/BPWM2	175:160	1	1	1	1
APWM10/BPWM3	159:144	0	X	X	X
APWM9/BPWM4	143:128	0	X	X	X
APWM8/BPWM5	127:112	1	0	7	7
APWM7/BPWM6	111:96	1	0	6	5
APWM6	95:80	1	0	5	3
APWM5	79:64	1	0	4	1
APWM4	63:48	1	0	3	6
APWM3	47:32	1	0	2	4
APWM2	31:16	1	0	1	2
APWM1	15:0	1	0	0	0

7.5.5 Thermal balance management (TBM)

In any practical multiphase printed circuit board design, some power stages are physically located near to, or between other phases. Power stages physically located between two other power stages experience mutual heating as a result of power dissipation from adjacent power stages. Hence, even though the controller device regulates the DC current sharing of each phase, the temperature of each power stage may be different.

Optionally, adjust the per-phase current sharing ratio K_T for each phase using the ISHARE_CONFIG command. This open-loop adjustment allows the designer to balance the temperature of each phase to compensate for mutual heating and non-uniform ground copper for heat spreading. The per-phase current limit of each phase is not affected by this setting. Refer to the *Technical Reference Manual* for a register map of ISHARE_CONFIG.

Thermal balancing is accomplished by scaling the gain of each phase current, as provided to the current sharing amplifier, in the on-time generator circuit for each phase. Refer to Figure 7-23 for more information. Each phase has an independently programmable gain K_T. Current share gain is assigned according to the logical phase number (PHASE setting) for each phase. The current carried by each phase when thermal balancing is active, can be calculated according to Equation 13.

First, calculate the effective thermal phase number, N_T as shown in Equation 13. This value changes with different numbers of operational phases, when phase shedding is enabled.

$$N_T = \frac{1}{K_{T1}} + \frac{1}{K_{T2}} + \ldots + \frac{1}{K_{Tn}} \tag{17}$$

where

- N_T is the effective thermal phase number.
- K_{T1}, K_{T2}, K_{Tn} are the individual thermal balance gains for phase 1, phase 2, ... phase n.

Then each phase carries a proportion of the total current, I_{SUM}, as shown in Equation 14.

$$I_{PHASE\ i} = \frac{I_{SUM}}{N_T \times K_{Ti}} \tag{18}$$

where

- I_i is the phase current for the i-th phase in amperes
- I_{SUM} is the total current carried by all phases in amperes
- K_{Ti} is thermal balance gain assigned to the i-th phase
- N_T is the effective thermal phase number, calculated above

Then, the current sharing ratio, comparing one phase to another is given by Equation 15.

$$\frac{I_{PHASE\ i}}{I_{PHASE\ j}} = \frac{K_{Tj}}{K_{Ti}} \tag{19}$$

where

- I_i and I_j are the phase current of the i-th and j-th phases in amperes
- K_{Ti} and K_{Tj} are the thermal balance gains of the i-th and j-th phases

Example: Balancing phase temperature for 7-phase converter

Consider a 7-phase converter with the following thermal balance gains assigned:

PHASE	Thermal Balance Gain K_i	VALUE	PHASE	Thermal Balance Gain K_i	VALUE
Phase 1	K_1	0.8	Phase 5	K_5	1.0
Phase 2	K_2	0.9	Phase 6	K_6	0.9
Phase 3	K_3	1.0	Phase 7	K_7	0.8
Phase 4	K_4	1.0			

Calculate N_T according to Equation 16.

$$N_T = \frac{1}{0.8} + \frac{1}{0.9} + \frac{1}{1.0} + \frac{1}{1.0} + \frac{1}{1.0} + \frac{1}{0.9} + \frac{1}{0.8} \approx 7.722 \tag{20}$$

Phases 1 and 7 have the same thermal balance gain, and carry the same proportion of the total current. Phases 2 and 6 have the same thermal balance gain and carry the same proportion of total current. Similarly, phases 3, 4, and 5 carry the same proportion of total current. Equation 17, Equation 18, and Equation 19 show the expected phase currents as a fraction of the total current I_{SUM}.

$$I_1 = I_7 = \frac{I_{SUM}}{N_T \times K_1} = \frac{I_{SUM}}{7.722 \times 0.8} \approx I_{SUM} \times 0.162 \tag{21}$$

$$I_2 = I_6 = \frac{I_{SUM}}{N_T \times K_2} = \frac{I_{SUM}}{7.722 \times 0.9} \approx I_{SUM} \times 0.144 \tag{22}$$

$$I_3 = I_4 = I_5 = \frac{I_{SUM}}{N_T \times K_3} = \frac{I_{SUM}}{7.772 \times 1.0} \approx I_{SUM} \times 0.129 \tag{23}$$

The ratios of two phase currents can be easily calculated as shown in Equation 20 and Equation 21.

$$\frac{I_2}{I_1} = \frac{K_{T1}}{K_{T2}} = \frac{0.9}{0.8} \approx 1.125 \tag{24}$$

$$\frac{I_4}{I_6} = \frac{K_{T6}}{K_{T4}} = \frac{0.9}{1.0} \approx 0.9 \tag{25}$$

7.5.6 Dynamic phase adding/shedding (DPA/DPS)

The dynamic phase shedding (DPS) feature allows the controller to dynamically select the number of operational phases for each channel, based on the total output current. This increases the total converter efficiency by reducing unnecessary switching losses when the output current is low enough to be supported by a fewer number of phases, than are available in hardware. Use the PHASE_SHED_CONFIG command to configure the phase adding/shedding thresholds. Refer to the *Technical Reference Manual* for a full listing of available thresholds.

Set the DPS_EN bit to 0b to disable phase shedding operation. The MIN_PH setting determines the minimum number of phases which are active during light-load operation.

Phase adding is detected based on the summed peak current of all phases in the analog domain. Phase shedding is detected based on average current telemetry, with a forced delay of 120 µs. The phase add thresholds are not affected by current measurement calibration, but the phase shed thresholds are.

Each phase has 3 settings available:

- **Phase add threshold (PH_ADDx)** selects the nominal phase adding threshold. Set this value approximately equal to the peak efficiency point per phase to optimize overall converter efficiency.
- **Phase add hysteresis (DPA_HYSTx)** selects the phase add threshold hsyteresis. Nominally set this value to one-half the value of the ripple current on the I_{SUM} current for that number of phases.
- **Phase drop hysteresis (DPS_HYST)** selects the phase drop hysteresis (per-phase average current). There is one setting per channel.

The phase add/drop thresholds can be calculated according to the equations below. First determine the ripple cancellation effect for each combination of phase numbers, for the chosen duty cycle using Equation 22. This value affects the true add thresholds.

$$K_i = \frac{\Delta I_{RIPPLE(ISUM)}}{\Delta I_{RIPPLE(PHASE)}} \approx \frac{N_i \times \left(D - \frac{m}{N_i}\right) \times \left(\frac{m+1}{N_i} - D\right)}{D \times (1 - D)} \tag{26}$$

where

- K_i is the ripple cancellation ratio before the phase transition

- $\Delta I_{ripple(ISUM)}$ is the ripple in the summed current after cancellation
- $\Delta I_{ripple(IPHASE)}$ is the ripple each individual phase
- N_i is the number of phases currently active
- D is the converter duty cycle, nominally Vout / Vin
- m is the maximum integer which does not exceed $N_i \times D$ (can be zero)

Calculate the DC phase adding thresholds based on the chosen configuration using Equation 23. Phases are added based on peak I_{SUM} current, after being passed through a 1 µs filter. Typically, choose the DPA_HYST settings to cancel out the current ripple term. Then the DC current adding threshold is equal to the PH_ADDx value selected.

$$I_{DPA(i\ to\ i+1)} \approx PH\_ADD_{i+1} + DPA\_HYST_{i+1} - K_i \times \frac{\Delta I_{RIPPLE(PHASE)}}{2} \quad (27)$$

where

- $I_{DPA(i\ to\ i+1)}$ is the DC current at which the controller transitions from i to i+1 phases
- PH_ADD_i is the selected phase add threshold for phase number i
- DPA_HYST_i is the selected phase add hysteresis for phase number i
- $\Delta I_{RIPPLE(PHASE)}$ is the ripple each individual phase

Calculate the DC phase drop thresholds based on the chosen configuration using Equation 24 phases are added based on the output current telemetry value, with a deglitch filter of 120 µs.

$$I_{DPS(i+1\ to\ i)} \approx PH\_ADD_{i+1} - i \times DPS\_HYST \quad (28)$$

where

- $I_{DPS(i+1\ to\ i)}$ is the DC current at which the controller transitions from i+1 to i phases
- PH_ADD_{i+1} is the selected phase add threshold for phase number i+1
- N_i is the number of phases currently active before the phase shed event
- DPA_HYST_i is the selected phase shed hysteresis

Phase add/shed example: 600-kHz, 8-phase, 12-V to 0.8-V converter, with 120 nH inductor

Assume V_{IN} = 12 V, V_{OUT} = 0.88, f_{SW} = 600 kHz, L = 120 nH.

The example below explains how to calculate the phase adding and shedding thresholds for 2 to 3 phases. First calculate the inductor ripple current in one phase. Set the DPA_HYST3 setting to approximately 1/2 the inductor current ripple in one phase. Assuming the phase adding threshold for phase 3, PH_ADD3, parameter is set to 40.0 A, and the phase shed hysteresis, DPS_HYST is set to 2.0 A, the phase adding and shedding thresholds are calculated as shown below.

$$I_{RIPPLE(PHASE)} = \frac{V_{OUT} \times (V_{OUT} - V_{IN})}{V_{IN} \times L \times f_{SW}} = \frac{0.88V \times (12V - 0.88V)}{12V \times 120nH \times 600kHz} = 11.3A$$

$$m = FLOOR\left(2 \times \frac{0.88V}{12V}\right) = 0$$

$$K_2 \approx \frac{N_i \times \left(D - \frac{m}{N_i}\right) \times \left(\frac{m+1}{N_i} - D\right)}{D \times (1 - D)} \approx \frac{2phases \times \left(\frac{0.88V}{12V} - \frac{0}{12phases}\right) \times \left(\frac{0+1}{12phases} - \frac{0.88V}{12V}\right)}{\frac{0.88V}{12V} \times \left(1 - \frac{0.88V}{12V}\right)} \approx 0.92$$

$$I_{DPA(2\ to\ 3)} \approx PH\_ADD_3 + DPA\_HYST_3 - K_i \times \frac{\Delta I_{RIPPLE(PHASE)}}{2} \approx 40A + 6A - 0.92 \times \frac{11.3A}{2} = 40.8A$$

$$I_{DPS(3\ to\ 2)} \approx PH\_ADD_3 - 2 \times DPS\_HYST = 40A - 2 \times 2A = 36A$$

7.5.7 Turbo Mode

The turbo mode feature enables multiphase systems to boost their efficiency by separating phases which carry the thermal steady state current of the load (normal phases) from those which only need to turn on to support fast load transient events (turbo phases).

- **Normal phases** carry the steady state current, and are operational all or most of the time. Normal phases can use larger inductance values to enable converter operation at lower switching frequency, as well as reduce inductor core loss.
- **Turbo phases** carry the AC load transient current and are not intended to remain operational always. Uselower inductance values for turbo phases to enable them to ramp up their phase current quickly as they turn on during transient events. Assign a higher current sharing ratio to turbo phases using the ISHARE_CONFIG command. Turbo phases are activated whenever USR2 is triggered, or whenever the converter output current exceeds their respective phase adding threshold. Turbo phases are always added last, and multiple turbo phases are added at the same time, regardless of their ordering assignment.

Turbo mode is only applicable to systems which use dynamic phase shedding. This feature is optional, and only recommended in cases where the system provides enough margin for the turbo phase power stages to operate within their safe operating area. The per-phase current report is not correct in turbo mode.

Use the PHASE_CONFIG command to assign phases as being either normal phases or turbo phases.

Example: 7 phases with 2 turbo phases

- Use the PHASE_CONFIG command to assign phase order 3 and 6 as turbo phases. Assign turbo phases out-of-phase with each other to avoid increasing the converter output ripple by a large amount due to loss of interleaving benefits.
- Use the ISHARE_CONFIG command to assign the "turbo gain" ratio as 2.0. This means the turbo phases will carry 2.0x the current of normal phases when turned on. Ensure that the turbo phase power stages are still operated within their safe operating area at worst case.
- Nominally, assign the turbo phases an inductance value proportionally lower compared to normal phases. In this case, normal phases use 150 nH inductance, and turbo phases use 75 nH. Without turbo phase, all normal phases would require 120nH.
- Use the PHASE_CONFIG command to set the dynamic phase adding thresholds for 5-6 phases and 6-7 phases high enough that they do not add during steady state current operation.
- Use the FREQUENCY_SWITCH command to reduce the switching frequency, to reduce switching loss.
- As shown in Figure 7-16 and Figure 7-17, the design still meets the transient requirement. The efficiency improvement is approximately 0.3-0.5%.

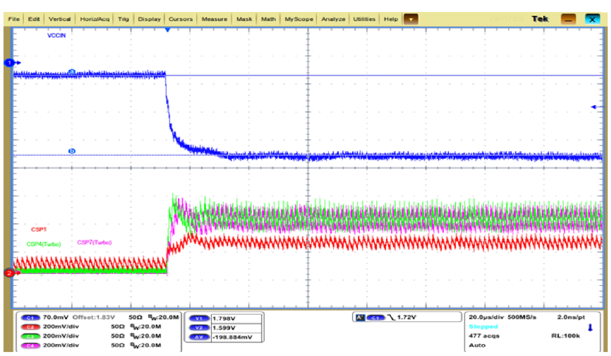


Figure 7-16. Load step with Turbo Mode

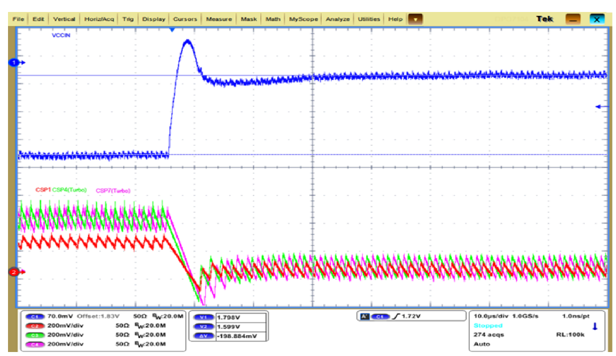


Figure 7-17. Load removal with Turbo Mode

7.6 Control Loop Theory of Operation

7.6.1 Adaptive voltage positioning and DC load line (droop)

TPS536C7B1 supports adaptive voltage positioning (AVP) through the VOUT_DROOP PMBus command. This feature is also referred to as the DC load line (DCLL) for the control loop. Use a non-zero DC load line to reduce output voltage set-point as a function of the load current, with a controlled slope. This feature is optional. Set the DC load line to 0.0 mΩ in applications which do not use a load line.

The DC load line provides two main benefits:

- Reducing the output voltage set-point, reduces the power consumption of the system, when the load current is high.
- Adaptive voltage positioning increases the allowable undershoot and overshoot during load transient events. Figure 7-18 and Figure 7-19 compare example output voltage specifications for systems with zero load line and non-zero load line. The nominal setting for the output voltage is chosen to be higher, to allow the entire transient window as margin for transient overshoot and undershoot.

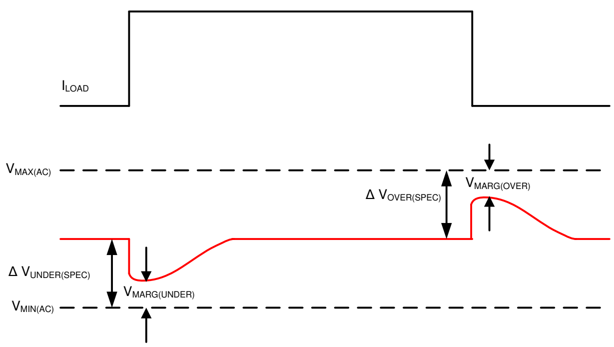


Figure 7-18. Load transient specification (zero load line)

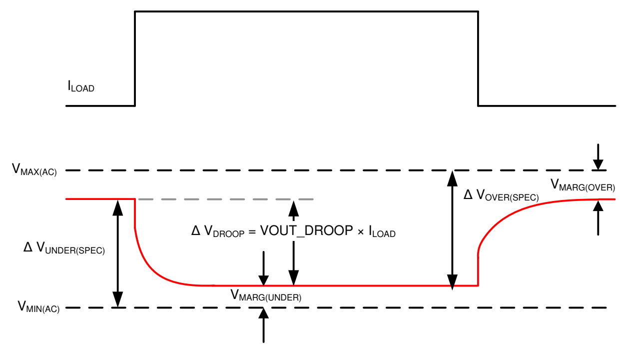


Figure 7-19. Load transient specification (non-zero load line)

7.6.2 DCAP+ conceptual overview

Figure 7-20 below describes the theory of operation for multiphase DCAP+ control, in continuous conduction mode (CCM).

The summed inductor currents, I_{SUM}, and output voltage deviation information, along with appropriate gain and integration, are processed to form a control signal V_{COMP}. Neglecting the output voltage information and integration, the V_{COMP} signal is a scaled version of I_{SUM}. A compensating ramp signal, V_{RAMP}, has a slope proportional to the number of phases, and switching frequency setting. When the V_{RAMP} and V_{COMP} signals intersect, the controller fires a new pulse.

Phase management logic distributes new pulses to the next phase in the firing order sequence. Each phase is assigned a firing order, at which pulses are passed to that phase. A separate, slower loop adjusts the on-times for each phase based on the output voltage setpoint, switching frequency setting, and current balance error.

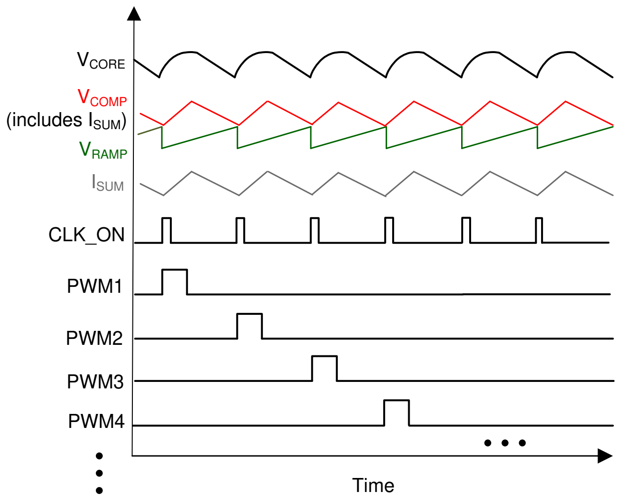


Figure 7-20. DCAP+ conceptual diagram (FCCM)

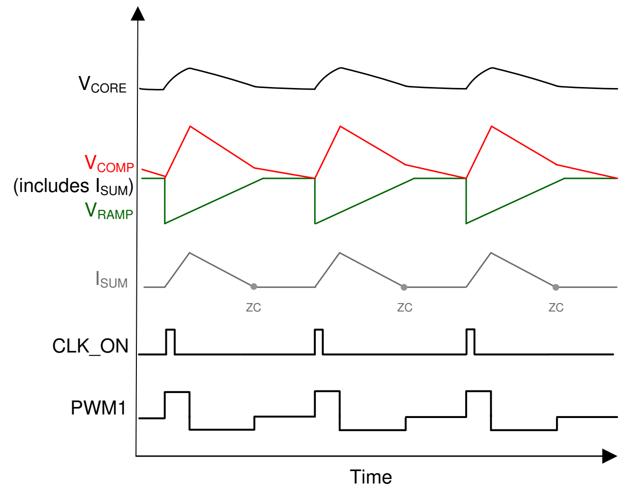


Figure 7-21. DCAP+ conceptual diagram (DCM)

7.6.3 Off-time control: loop compensation and transient tuning

Figure 7-22 shows a conceptual block diagram of the DCAP+ off-time control loop. Transient response tuning is accomplished by changing the parameters which generate the V_{COMP} signal. These parameters are accessible using the COMPENSATION_CONFIG command. Refer to the *Technical Reference Manual* for a register map of this command.

The V_{COMP} signal is generated by the sum of three signal paths. Finally the V_{COMP} signal is scaled by the AC gain parameter, K_{AC}.

- **Proportional path:** An error amplifier subtracts the sensed output voltage from the output voltage target, set by V_{DAC}. The gain of the proportional path is set by the AC load line (ACLL). Reducing the value of the AC load line increases the proportional path gain, which gives faster transient response. Setting the AC load line to a very low value can lead to low phase margin. The minimum recommended ACLL value is 0.125 m ohm.
- **Integral path:** The difference between the sensed output voltage and the output voltage target, V_{DAC}, is compared to the ideal droop (I_{SUM} × DCLL) value to create an error voltage, V_{ERR}. An integrator adjusts the setpoint of V_{COMP}, to drive the output voltage error to zero. Integration provides high DC gain, giving the power supply excellent output regulation and DC load line performance. The programmable integration time constant, τ_{INT} changes the settling time of of the output voltage folliowing a transient. Increasing the integration time constant improves phase margin. The programmable integration path gain, K_{INT}, sets the gain of the integral path.
- **Current feedback:** The summed phase current, I_{SUM}, with a nominal gain of 5 mV/A, is used directly to generate V_{COMP}, as well as in the integral path to set the DC load line. The gain of this path is not affected by the IOUT_CAL_GAIN or IOUT_CAL_OFFSET calibration commands.

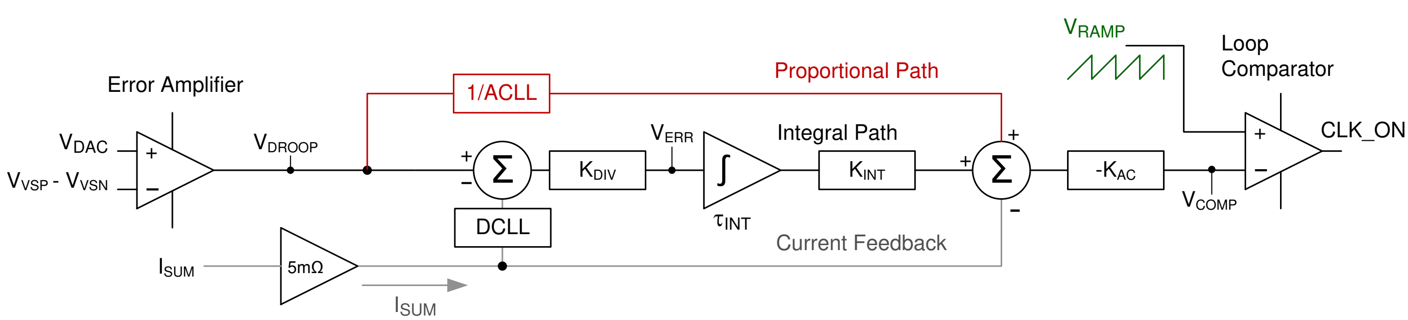


Figure 7-22. Loop compensation conceptual block diagram

7.6.4 On-time control: adaptive t_{on} and autobalance current sharing

The nominal on-time for each phase is determined by an adaptive one-shot circuit, which generates on-times according to Equation 25. PWM on-times are adjusted very slowly compared to off-times, so the DCAP+ modulator behaves similar to a constant-on-time architecture.

Use the FREQUENCY_SWITCH command to set the nominal per-phase switching frequency.

$$t_{ON} = \frac{V_{DAC} + K_{ISHARE} \times (I_L - I_{AVG})}{V_{IN} \times FREQUENCY\_SWITCH} + \Delta PLL\_CLF \tag{34}$$

where

- t_{ON} is the on-time for the phase in seconds
- V_{DAC} is the output voltage set-point in volts
- FREQUENCY_SWITCH is the commanded switching frequency in Hz
- V_{IN} is the sensed input voltage from the VIN_CSNIN pin
- K_{ISHARE} is the gain of the current share loop
- I_L is the current carried by the phase
- I_{AVG} is the average phase current for all phases
- ΔPLL_CLF is the on-time adjustment from the closed loop frequency correction circuit

Current sharing is implemented by adapting the on-time for each phase, according to the difference between its own phase current I_L, and the average of all phase currents I_{AVG}. When the phase current for any one phase is greater than the average of all phase currents, the on-time of that phase is reduced accordingly. Similarly, if the phase current of any one phase is less than the average of all phase currents, the on-time of that phase is increased.

The on-time is also proportional to the sensed input voltage, which provides the controller with inherent input voltage feed-forward.

Furthermore, a frequency control loop adjusts the on-times for each phase to drive the actual switching frequency equal to the FREQUENCY_SWITCH setting. An internal clock counts the number of observed pulses over a set interval, and compares the result to the calculated ideal number. If too many pulses are fired in the sampling period, the switching frequency is too high, and the on-times are increased to reduce the steady-state switching frequency. If too few pulses are fired during the sampling period, the switching frequency is too low and the on-times are reduced to increase the steady-state frequency. The PWM pin assigned to ORDER=0 is used for counting purposes, as it does not drop due to phase shedding.

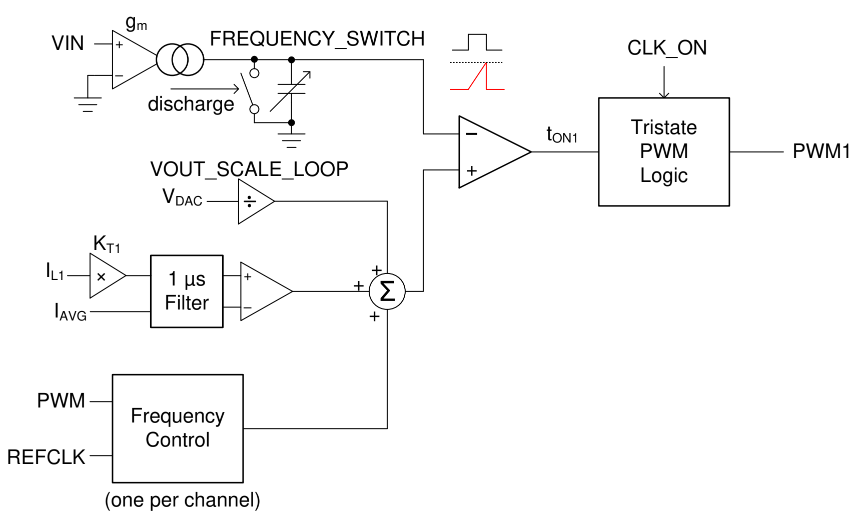


Figure 7-23. On-time generation and auto-balance current sharing

7.6.5 Load transient response

TPS536C7B1 achieves fast load transient performance using the inherently variable switching frequency characteristics of DCAP+ control. Figure 7-24 illustrates the load insertion behavior, in which PWM pulses are generated with faster frequency than the steady-state frequency, to provide more energy to the output voltage, improving undershoot performance. Figure 7-25 illustrates the load release behavior, in which PWM pulses can be delayed to avoid charging extra energy to the load until the output voltage reaches the peak overshoot.

When there is a sudden load increase, the output voltage immediately drops. The controller device reacts to this drop by lowering the voltage on internal V_{COMP} signal. This forces PWM pulses to fire more frequently, which causes the inductor current to rapidly increase. As the converter output current reaches the new load current, the device reaches a steady-state operating condition and the PWM switching resumes the steady-state frequency.

When there is a sudden load release, the output voltage immediately overshoots. The control loop reacts to this rise by increasing the voltage of the internal V_{COMP} signal. This rise forces the PWM pulses to be delayed until the converter output current reaches the new load current. At that point, the switching resumes and steady-state switching continues. In Figure 7-24 and Figure 7-25, the ripples on V_{OUT} , and V_{COMP} voltages are not shown for simplicity.

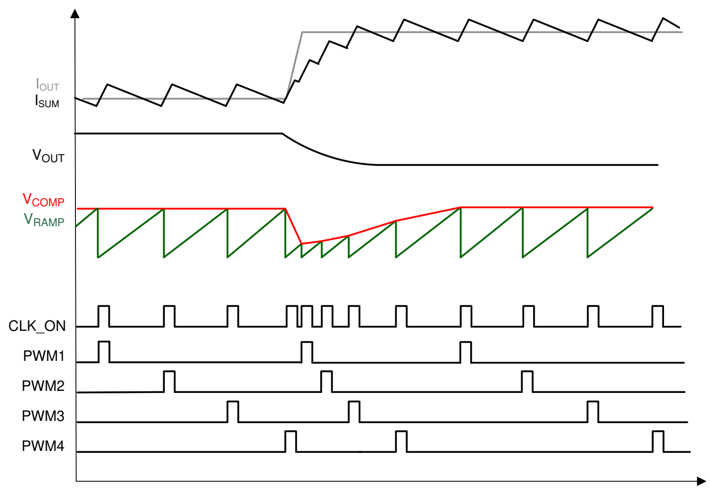


Figure 7-24. Load insertion response (4-phase example, 0-1-2-3 ordering)

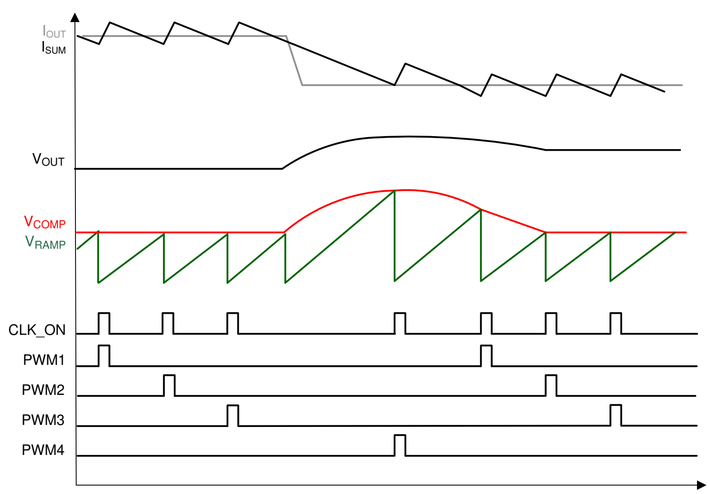


Figure 7-25. Load release response (4-phase Example, 0-1-2-3 ordering)

7.6.6 Forced minimum on-time, minimum off-time and leading-edge blanking time

Under normal linear operation, the PWM on- and off-times are generated by the control loop. To improve noise immunity, the controller forces a minimum on-time whenever the PWM pins pulse high. The off-time for any phase is limited by a forced minimum off-time. Although TI smart power stage devices have built-in protection from glitches on the PWM pins also, this feature provides redundant protection against cross-conduction issues.

The controller also limits the time between sending pulses to any two adjacent phases. This is referred to as the leading-edge blanking time, t_{BLANK}. Increase the leading edge blanking time to prevent over-compensation (or "ring-back") by the controller during heavy load transient events. The minimum on-time, minimum off-time, and leading edge blanking time are programmable by the NONLINEAR_CONFIG PMBus command. Refer to the *Technical Reference Manual* for a register map of this command.

For multiphase designs, the maximum per-phase switching frequency during transients, is limited by the leading edge blanking time parameters as shown in Equation 26. The controller also forces a minimum-off-time per phase. The greater of the two limits the maximum frequency.

$$f_{PHASE(max)} = \frac{1}{N_{\Phi} \times t_{BLANK}} \tag{35}$$

where

- N_{Φ} is the number of active phases
- t_{BLANK} is the leading edge blanking time in seconds

7.6.7 Nonlinear: undershoot reduction (USR), overshoot reduction (OSR) and dynamic integration

Nonlinear features improve the controller response to severe repetitive load transient conditions.

When the controller is subjected to load transients at very high frequency, the output voltage may not be able to completely settle before the next transient event occurs. As a result, particularly during overshoot events, when the controller is firing pulses infrequently, the controller integration path can see error which does not completely settle. Accumulation of large overshoot error can cause the controller response to following undershoot events to be slower. To prevent excess accumulation of error during repetitive load transient events, the controller implements *dynamic integration*. When the output voltage overshoots its target by a certain voltage, V_{DINT}, the controller integration time constant can be changed to an alternate value, the dynamic integration time constant. Use the COMPENSATION_CONFIG command to configure the dynamic integration time constant and threshold voltage. Typically, set the dynamic integration constant to a longer time than the static integration time constant.

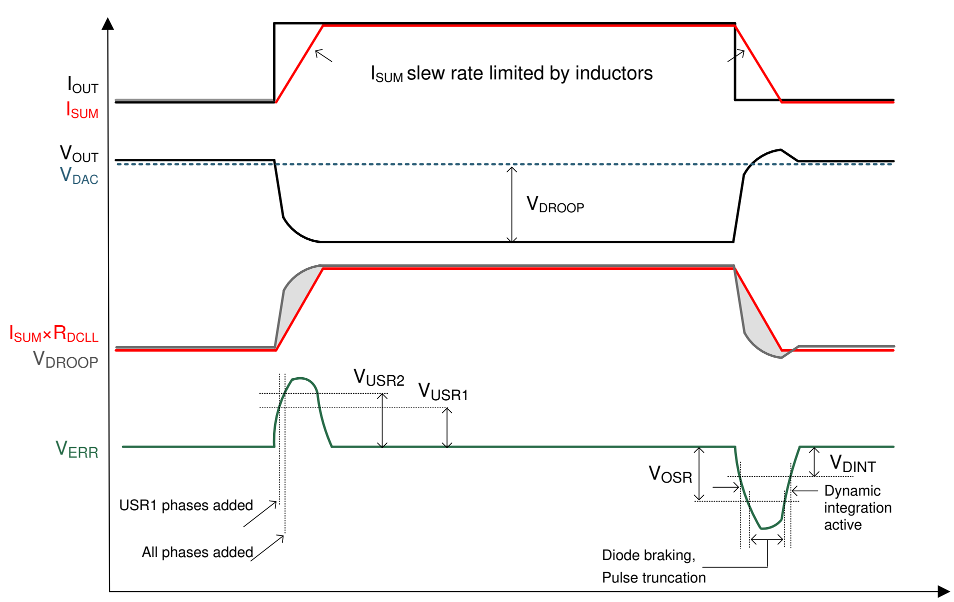


Figure 7-26. Dynamic integration, OSR, USR detection

Systems which use the dynamic phase shedding feature, may still have sudden and severe load transient events occur. The undershoot reduction (USR) feature allows the controller to add phases even before the output current reaches the dynamic phase adding thresholds. This ensures the transient undershoot event is stopped as quickly as possible. TPS536C7B1 has two levels of USR. The USR1 threshold is used to quickly enable a configurable number of phases, USR1_PH. The USR2 threshold adds all enabled phases, assigned to that channel. Use the NONLINEAR_CONFIG command to configure the USR1 and USR2 features.

The overshoot reduction (OSR) feature reduces output voltage overshoot during severe load transient events, by turning off the low-side FETs of the powerstage devices (e.g. tri-stating the controller PWM pins), when an overshoot event occurs. The inductor current of each phase must remain continuous, forcing the output current through the body diode of each low-side FET. This dissipates excess energy more quickly than keeping the powerstage low-side FET fully conducting, due to the forward voltage drop characteristics of the body diodes. As a result, the transient overshoot is smaller when this technique is used, compared to simply turning on the low-side FET of each powerstage. However, this results in excess heat which must be properly managed in systems with highly repetitive transient conditions. Additionally, TPS536C7B1 can be configured to truncate PWM pulses, to reduce the worst-case response time to overshoot events. The NONLINEAR_CONFIG command provides four controls for overshoot reduction: an enable bit for diode braking, an enable bit for pulse truncation, the OSR threshold, V_{OSR}, and the diode braking timeout, which limits the maximum amount of time during which diode braking takes place, to manage excess heating. Refer to the *Technical Reference Manual* for a register map of this command.

7.7 Power supply fault protection

7.7.1 Host notification and status reporting

The supported status bits and registers are detailed in Figure 7-27. All of the fault conditions listed in Section 7.7.3 have associated status bits. Status bits and SMB_ALERT# may be cleared using the CLEAR_FAULTS command, commanding the offending channel to disable (as specified in ON_OFF_CONFIG), or by power cycling. Most commonly, issue CLEAR_FAULTS with the PAGE set to FFh, to clear faults for both channels.

(79h) STATUS_WORD [paged] | (78h) STATUS_BYTE [paged] (and LSB of STATUS_WORD)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

MSB
Bit 15: More info in STATUS_VOUT
Bit 14: More info in STATUS_IOUT
Bit 13: More info in STATUS_INPUT
Bit 12: More info in STATUS_MFR
Bit 11: VR_RDY pin is low
Bit 9: More info in STATUS_OTHER

LSB
Bit 7: Device was busy and could not respond
Bit 6: Power conversion is disabled for any reason
Bit 5: Vout OV Fault
Bit 4: Iout OC Fault
Bit 3: Vin UV Fault
Bit 2: More info in STATUS_TEMPERATURE
Bit 1: More info in STATUS_CML
Bit 0: More info in MSB

(7Ah) STATUS_VOUT [paged]

7	6	5	4	3	2	1	0

Bit 7: Vout OV Fault (Fixed or Tracking). More info in STATUS_EXTENDED
Bit 6: Vout OV Warn
Bit 5: Vout UV Warn
Bit 4: Vout UV Fault (Tracking)
Bit 3: Vout commanded outside VOUT_MIN/VOUT_MAX window
Bit 2: TON_MAX Fault

(7Bh) STATUS_IOUT [paged]

7	6	5	4	3	2	1	0

Bit 7: Iout (Isum) OC Fault
Bit 5: Iout (Isum) OC Warn
Bit 3: Ishare Warn. More info in STATUS_PHASES

(7Ch) STATUS_INPUT [shared]

7	6	5	4	3	2	1	0

Bit 7: Vin OV Fault
Bit 6: Vin OV Warn
Bit 5: Vin UV Warn
Bit 4: Vin UV Fault
Bit 3: Unit off due to low input voltage
Bit 2: Iin OC Fault
Bit 1: Iin OC Warn
Bit 0: Pin OP Warn

(7Dh) STATUS_TEMPERATURE [paged]

7	6	5	4	3	2	1	0

Bit 7: Power stage OT Fault
Bit 6: Power stage OT Warn

(7Eh) STATUS_CML [shared]

7	6	5	4	3	2	1	0

Bit 7: Invalid command
Bit 6: Invalid data
Bit 5: Packet error check failed
Bit 4: Memory failure
Bit 1: Communication error
Bit 0: Other communication error occurred

(7Fh) STATUS_OTHER [shared]

7	6	5	4	3	2	1	0

Bit 0: Device was first to assert SMB_ALERT#

(DCh) STATUS_PHASES [paged][phased]

15	14	13	12	...	2	1	0

If PHASE=FFh (address all phases)
Bit 0: Warn info available about Phase 1
Bit 1: Warn info available about Phase 2
⋮
If PHASE=00h, 01h, … (individual phase)
Bit 7: Ishare (higher than avg) warning
Bit 6: Ishare (lower than avg) warning
Bit 1: Per-phase OCL warning

(DDh) STATUS_EXTENDED [shared]

55	54	53	52	...	2	1	0

Bit 55: CML Access error
Bit 54: Bad group command
Bit 53: Attempted group read
Bit 52: Unknown CML error
Bit 51: Transaction aborted
Bit 50: Lost arbitration
Bit 49: Block size was NACK
Bit 45: Too few bytes rx'd
Bit 44: Too many bytes rx'd
Bit 43: Block size too small
Bit 42: Block size too large
Bit 41: Write to protected cmd
Bit 39: VSP open Ch. B
Bit 38: VSP open Ch. A
Bit 37: VSN open Ch. B
Bit 36: VSN open Ch. A
Bit 28: SYNC/CLF fault
Bit 26: Update not allowed
Bit 25: BOOT pin detect failed
Bit 24: ADDR pin detect failed
Bit 19: Invalid phase config
Bit 18: Invalid config file
Bit 15: TAO low Ch. B
Bit 14: TAO low Ch. A
Bit 5: Pre-bias OVP Ch. B
Bit 4: Pre-bias OVP Ch. A
Bit 3: Tracking OVP Ch. B
Bit 2: Tracking OVP Ch. A
Bit 1: Fixed OVP Ch. B
Bit 0: Fixed OVP Ch. A

(80h) STATUS_MFR_SPECIFIC [paged]

7	6	5	4	3	2	1	0

Bit 7: Power-on self-check failed
Bit 6: More info in STATUS_EXTENDED
Bit 4: More info in STATUS_PHASES
Bit 3: RESET# Vout occurred
Bit 0: Power stage fault (TAO High)

Figure 7-27. Status register support and decoding

TPS536C7B1 supports a full set of PMBus status registers and the SMB_ALERT# notification protocol. Any condition which causes a status bit to assert, also causes TPS536C7B1 to assert the SMB_ALERT# signal (unless that bit is masked via SMBALERT_MASK). Use the alert response address (ARA) protocol to determine the address of the device experiencing a fault condition in multi-slave systems. The SMB_ALERT# protocol is optional, and the system designer may choose to implement fault management through other means. Figure 7-28 shows a flow diagram of using the ARA protocol.

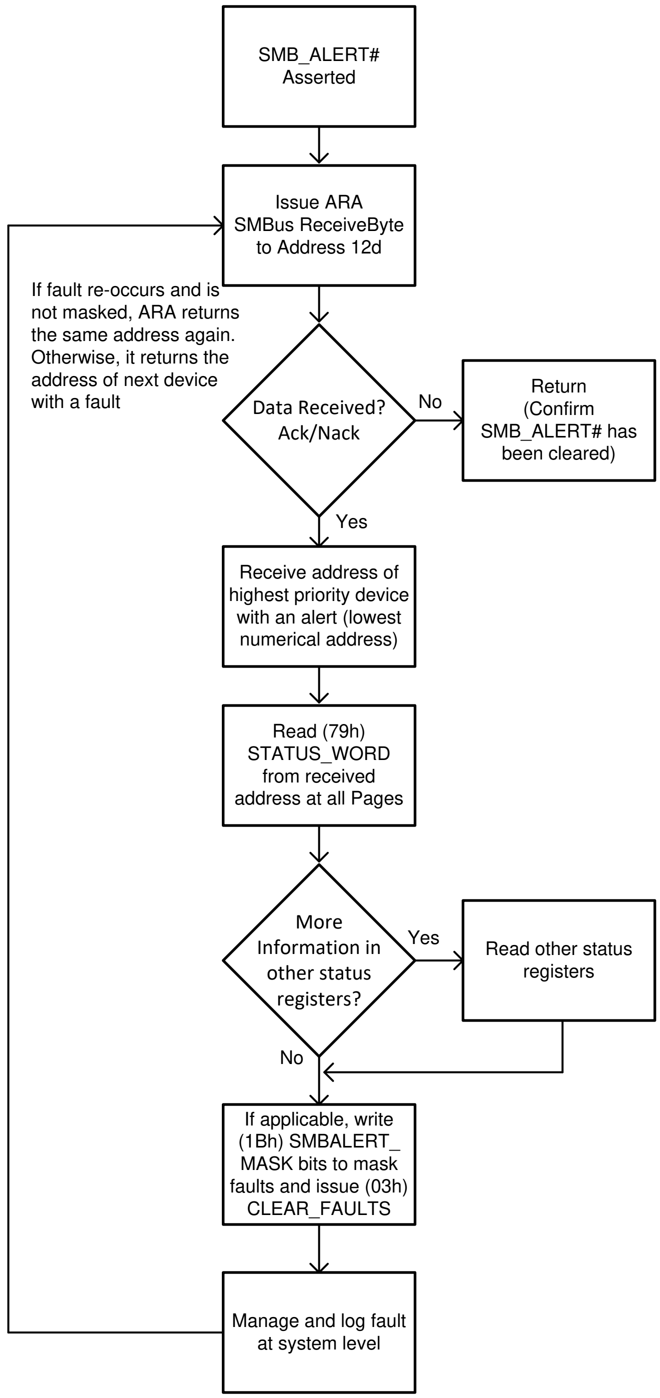


Figure 7-28. Flow diagram of SMB_ALERT# response protocol

7.7.2 Fault type and response definitions

Paged fault conditions apply only to a single channel and are duplicated for channel A and channel B. Paged fault conditions only cause one channel to shut down when triggered. For latch-off faults, the enable for that channel must be toggled to re-enable power conversion. For example, if channel B experiences an overvoltage fault, only channel B stops power conversion, and channel B must be commanded to disable power conversion, and re-enable power conversion to continue normal operation.

Shared fault conditions apply to channels A and B simultaneously. Shared fault conditions cause both channels A and B to shut down when triggered.

Warning conditions do not cause any interruption to power conversion. They are meant to inform the system host of changing conditions so that it can react prior to a fault being triggered. Warnings do conditions set associated PMBus status bits and trigger the SMB_ALERT# signal when not masked.

Fault conditions set to the *ignore response* are treated as warnings. Faults set to the ignore response do not cause any interruption of power conversion but do still cause status bits and SMB_ALERT# to trigger.

Fault conditions set to the *latch-off response* cause power conversion to stop immediately. The channel must be commanded to stop power conversion then restart to continue operation. Start-up from a latch-off fault is identical to a normal power-up and the configured TON_DELAY is still observed. The RSTOSD option in MISC_OPTIONS controls whether the boot voltage returns to its last programmed value, or boots to its VBOOT value.

Fault conditions set to the *hysteretic response* cause power conversion to stop immediately. When the fault condition no longer exists, the TPS536C7B1 attempts to restart immediately. The configured TON_DELAY is still observed.

Fault conditions set to the *hiccup response* cause power condition to stop immediately. After a hiccup wait time, 25 ms by default, TPS536C7B1 attempts to re-enable power conversion. The configured TON_DELAY is still observed. If the fault condition has disappeared, the start-up attempt succeeds and power conversion continues. Otherwise, the process repeats indefinitely. The RSTOSD option in MISC_OPTIONS controls whether the boot voltage returns to its last programmed value, or boots to its VBOOT value.

The TOFF_DELAY is not respected during any fault shutdown response.

7.7.3 Fault behavior summary

Table 7-8. Fault detection and behavior

Fault Name	Shared / Paged / Phased	Condition	Latency	Enabled	Programmable Range	Response	Alerts (1)	Clearing (2)
Output Voltage / Current / Power								
Pre-Bias OV Fault	Shared	VSP voltage exceeded threshold	Max 350 µs after 3.3V OK	Until initialization complete, then disabled	3.7 V fixed by design	All PWM Low, Latch-Off	VR_FAULT#	3.3 V Power Cycle
Fixed OV Fault	Paged	VSP voltage exceeded fixed threshold	1.0 µs	After initialization complete	0.6 V to 3.7 V	Ignore, Latch-Off, Hiccup PWM Pulled Low	VR_FAULT# if not ignore response	3.3 V power cycle if triggered while power conversion is disabled. Otherwise, clearable through Enable cycle, or CLEAR_FAULTS
Tracking OV Fault	Paged	VSP-VSN voltage exceeded VID + Droop + OV Offset	1.0 µs	During power conversion	Offset from current VID+Droop, +32 to +448 mV Offset	Ignore, Latch-Off, Hiccup PWM pulled low	VR_FAULT# if not ignore response	Enable cycle, or CLEAR_FAULTS
Tracking OV Warn	Paged	VSP-VSN voltage exceeded VID + Droop + OV Offset	2.0 µs	During power conversion	Offset from current VID + Droop +24 to +448 mV Offset	Warning only	n/a	Enable cycle, or CLEAR_FAULTS
Tracking UV Warn	Paged	VSP-VSN voltage below VID + Droop - UV Offset	2.0 µs	During power conversion	Offset from current VID + Droop -24 to -448 mV Offset	Warning only	n/a	Enable cycle, or CLEAR_FAULTS
Tracking UV Fault	Paged	VSP-VSN voltage below VID + Droop- UV Offset	1.0 µs	During power conversion	Offset from current VID + Droop -32 to -448 mV Offset	Ignore, Latch-Off, Hiccup PWM Tri-State	n/a	Enable cycle, or CLEAR_FAULTS
Max Turn-on time (TON_MAX)	Paged	VSP-VSN did not rise to threshold quickly enough during soft-start	500 µs	During soft-start only	0 ms to 31.75 ms	Ignore, Latch-Off, Hiccup PWM Tri-State	n/a	Enable cycle, or CLEAR_FAULTS
Vout Min/Max Warning	Paged	Vout commanded above VOUT_MAX or below VOUT_MIN	N/A	During power conversion	VOUT_MAX and VOUT_MIN	DAC Voltage clamped to limit Warning only	n/a	Enable cycle, or CLEAR_FAULTS
Over-current Fault	Paged	Total current exceeded threshold	175 µs	During power conversion	0 to 1023 A(3)	Ignore, Latch-Off, Hiccup PWM Tri-State	VR_FAULT# configurable	Enable cycle, or CLEAR_FAULTS
Per-Phase Over-current Limit	Paged, Phased	Phase current exceeded threshold	Cycle-by-cycle	During power conversion	17 to 130 A(3)	Warning only, PWM pulses skipped to limit phase current	n/a	Enable cycle, or CLEAR_FAULTS
Current Share Warning	Paged, Phased	Phase current above or below average current for all phases by threshold	175 µs	During power conversion	5 to 20 A per phase	Warning only	n/a	Enable cycle, or CLEAR_FAULTS

(1) Any fault response which causes a shutdown event de-asserts VR_RDY. All faults have associated PMBus status bits and SMB_ALERT# response (unless masked by SMBALERT_MASK commands)
(2) Fault condition must have disappeared, otherwise fault re-triggers immediately
(3) IOUT_OC_FAULT_LIMIT[PAGE=x][PHASE=FFh] sets the per-page OC fault threshold, IOUT_OC_FAULT_LIMIT[PAGE=x][PHASE=Other] sets the per-phase OCL threshold

Table 7-9. Fault detection and behavior (continued)

Fault Name	Shared / Paged / Phased	Condition	Latency	Enabled	Programmable Range	Response	Alerts (1)	Clearing (2)
Power Stage Feedback								
Over-Temperature Fault	Paged	Power Stage Temperature exceeded threshold	950 µs	After initialization complete	+90 to +160 °C	Ignore, Latch-Off, Hiccup PWM Tri-State	VR_FAULT# configurable	Enable cycle, or CLEAR_FAULTS
Over-Temperature Warning	Paged	Power Stage Temperature exceeded threshold	950 µs	After initialization complete	+90 to +160 °C	Warning only	n/a	Enable cycle, or CLEAR_FAULTS
Power Stage Fault	Paged	TAO pulled high by power stage	1.0 µs	After initialization complete	TAO > 2.5 V	Ignore, Latch-Off, Hiccup PWM Tri-State	VR_FAULT# if not ignore response	Enable cycle, or CLEAR_FAULTS
Power Stage Not Ready (TAO LOW)	Paged	TAO pulled low by power stage	1.0 µs	After initialization complete	TAO < 230 mV Falling (50mV hysteresis)	Hysteresis Start-up is blocked if not yet enabled, or rail is shutdown. PWM tristated	n/a	Enable cycle, or CLEAR_FAULTS
Input Voltage / Current / Power								
Input Over-Voltage Fault	Shared	VIN_CSNIN voltage exceeded threshold	950 µs	After initialization complete	0 to 19 V	Ignore, Latch-Off, Hiccup PWM Tri-State	n/a	Enable cycle, or CLEAR_FAULTS
Input Over-Voltage Warning	Shared	VIN_CSNIN voltage exceeded threshold	950 µs	After initialization complete	0 to 19 V	Warning only	n/a	Enable cycle, or CLEAR_FAULTS
Input Under-Voltage Warning	Shared	VIN_CSNIN voltage below threshold	950 µs	VIN > VIN_ON first time and either channel enabled	4.0 to 11.25 V	Warning only	n/a	Enable cycle, or CLEAR_FAULTS
Input Under-Voltage Fault	Shared	VIN_CSNIN voltage below threshold	950 µs	VIN > VIN_ON first time and either channel enabled	4.0 to 11.25 V	Ignore, Latch-Off, Hiccup PWM Tri-State	n/a	Enable cycle, or CLEAR_FAULTS
Input Over-Current Fault	Shared	CSPIN-VIN_CSNIN current below threshold	525 µs	During power conversion	4 to 128 A	Ignore, Latch-Off, Hiccup PWM Tri-State	VR_FAULT# if not ignore response	Enable cycle, or CLEAR_FAULTS
Input Over-Current Warning	Shared	CSPIN-VIN_CSNIN current below threshold	525 µs	During power conversion	4 to 128 A	Warning only	n/a	Enable cycle, or CLEAR_FAULTS
Input Over-Power Warning	Shared	Computed input power above threshold	525 µs	During power conversion	8 to 2044 W	Warning only	n/a	Enable cycle, or CLEAR_FAULTS
Self-Checking								
Invalid ADDR Pinstrap	Shared	ADDR pin open, low, high, or non-convergent detection	Checked once at initialization	Checked during power-on and enable	Per detection thresholds	Latch-Off, PWM tristate	n/a	3.3 V Power Cycle
Invalid BOOT Pinstrap	Shared	BOOT pin open, low, high, or non-convergent detection	Checked once at initialization	Checked during power-on and enable	Per detection thresholds	Latch-Off, PWM tristate	n/a	3.3 V Power Cycle
PMBus Interface								
PMBus Communication Error	Shared	PMBus Communication Error (See STATUS_CML)	Per PMBus communication frequency	After initialization complete	See PMBus Specification	Warning only	n/a	Enable cycle, or CLEAR_FAULTS

(1) Any fault response which causes a shutdown event de-asserts VR_RDY. All faults have associated PMBus status bits and SMB_ALERT# response (unless masked by SMBALERT_MASK commands)
(2) Fault condition must have disappeared, otherwise fault re-triggers immediately

7.7.4 Detailed fault descriptions

7.7.4.1 Overvoltage fault (OVF) and warning (OVW)

TPS536C7B1 supports several forms of overvoltage protection. Figure 7-29 describes the overvoltage protection scheme in more detail.

- **Pre-Bias OVF** protects the converter while initialization runs. This protection is active $t_{INIT\text{-}PBOV}$, 350 µs maximum after the VCC pin voltage is established, until initialization is complete. The threshold is hard-coded to 3.7 V. In response to this condition, all PWM pins (regardless of channel assignment) pull low, regardless of the overvoltage response setting. This fault cannot be cleared without a power cycle of the VCC pin. The fixed overvoltage protection becomes active after $t_{INIT\text{-}LOGIC}$, up to 20 ms after the VCC pin voltage is established. This fault detection cannot be disabled.
- **Fixed OVF** is a programmable limit based on the VSP pin voltage, above which it is not safe to operate the load device. Program the threshold through MFR_PROTECTION_CONFIG. This fault detection is active regardless of power conversion. If triggered while power conversion is disabled, this fault is treated as potentially catastrophic, and cannot be cleared without a power cycle of the VCC pin.
- **Tracking OVF** is a fault limit, programmable as an offset from the current VOUT_COMMAND value. Program this threshold through VOUT_OV_FAULT_LIMIT. When the VSP-VSN pin differential voltage exceeds this limit during power conversion, the tracking overvoltage fault condition is detected. This fault detection is disabled whenever power conversion is disabled.
- **Tracking OVW** is a warning limit, programmable as an offset from the current VOUT_COMMAND value. Program this threshold through VOUT_OV_WARN_LIMIT. When the VSP-VSN pin differential voltage exceeds this limit during power conversion, the tracking overvoltage warning condition is detected. This is a warning condition only, and does not cause any interruption to power conversion. The overvoltage warning provides early feedback to they system host allowing it to make adjustments prior a fault triggering.

In response to the overvoltage warning condition, TPS536C7B1 sets the appropriate status bits in STATUS_WORD and STATUS_VOUT and asserts the SMB_ALERT# line if these bits are not masked.

In response to the overvoltage fault condition TPS536C7B1 responds according to the programmed VOUT_OV_FAULT_RESPONSE. When not set to the ignore response, this causes the PWM pins of the rail which experienced a fault to pull low immediately. Additionally, TPS536C7B1 sets the appropriate status bits in STATUS_WORD and STATUS_VOUT and asserts the SMB_ALERT# line if these bits are not masked.

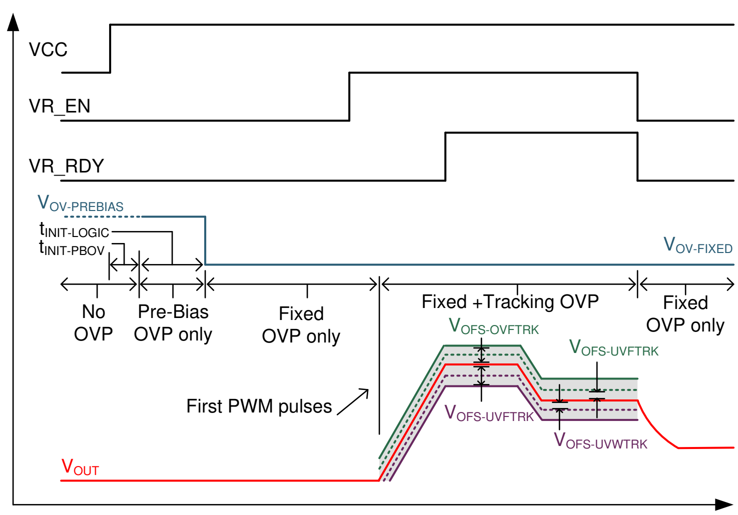


Figure 7-29. Overvoltage Protection

Program the tracking overvoltage fault threshold through the VOUT_OV_FAULT_LIMIT command as an absolute voltage. When a new VOUT_OV_FAULT_LIMIT command is received the device calculates the tracking overvoltage offset value internally according to Equation 27. The threshold voltages get scaled with the use of an external voltage sensing divider and VOUT_SCALE_LOOP. TPS536C7B1 supports tracking overvoltage fault offsets from +32 mV to +448 mV in 32 mV steps.

Program the tracking overvoltage warning through the VOUT_OV_WARN_LIMIT command as an absolute voltage. Similarly, when a new VOUT_OV_WARN_LIMIT command is received, the device calculates the tracking overvoltage warning offset according to Equation 28. The threshold voltages get scaled with the use of an external voltage sensing divider and VOUT_SCALE_LOOP. TPS536C7B1 supports tracking overvoltage warning offsets from +24 mV to +448 mV in 8 mV steps.

Program the fixed overvoltage fault threshold through MFR_PROTECTION_CONFIG. TPS536C7B1 supports values from 0.6 V to 3.7 V, in 100 mV steps.

$$V_{OFS(OVF\ TRK)} = \frac{VOUT\_OV\_FAULT\_LIMIT - VOUT\_COMMAND}{VOUT\_SCALE\_LOOP} \tag{36}$$

$$V_{OFS(OVW\ TRK)} = \frac{VOUT\_OV\_WARN\_LIMIT - VOUT\_COMMAND}{VOUT\_SCALE\_LOOP} \tag{37}$$

The over-voltage warning and fault trip thresholds include the load-line setting as shown in Equation 29 and Equation 30.

$$V_{OVW(trip)} = VOUT\_COMMAND + V_{OFS(OVW\ TRK)} - VOUT\_DROOP \times I_{OUT} \tag{38}$$

$$V_{OVF(trip)} = Min\left(V_{OVFIX}\ ,\ VOUT\_COMMAND + V_{OFS(OVF\ TRK)} - VOUT\_DROOP \times I_{OUT}\right) \tag{39}$$

Updates to VOUT_COMMAND do not cause these the overvoltage offsets to be recalculated. After the output voltage target has been changed, TPS536C7B1 reports the fault and warning thresholds by adding the previously select offset value to the current VOUT_COMMAND.

Example: Programming the OVF and OVW offsets

Assume the current VOUT_COMMAND is 1.000 V, the VOUT_DROOP setting is equal to 0.5 mΩ, and the load current is equal to 100 A.

- Program the VOUT_OV_WARN_LIMIT to 1.128 V (1.0 V + 128 mV), to select the +128 mV tracking overvoltage warning offset. The VOUT_DROOP is assumed to be zero for calculation purposes. However, the over-voltage warning trip threshold does account for the load-line setting and is equal to 1.128 V - 0.5 mΩ × I_{OUT}.
- Program the VOUT_OV_FAULT_LIMIT to 1.256 V (1.0 V + 256 mV) , to select the +256 mV tracking overvoltage fault offset. The VOUT_DROOP is assumed to be zero for calculation purposes. However, the over-voltage fault trip threshold does account for the load-line setting and is equal to 1.256 V - 0.5 mΩ × I_{OUT}.

If the VOUT_COMMAND value is changed to is 1.100 V, the TPS536C7B1 reports VOUT_OV_WARN_LIMIT as 1.228 V (1.1 V + 128 mV), and VOUT_OV_FAULT_LIMIT as 1.356 V (1.1 V + 256 mV). The offset values are not changed.

7.7.4.2 Undervoltage fault (UVF) and warning (UVW)

Two undervoltage threshold limits are provided:

- **Tracking UVF** is a fault limit, programmable as an offset from the current VOUT_COMMAND value. Program this threshold through VOUT_UV_FAULT_LIMIT. When the VSP-VSN pin differential voltage falls below this limit during power conversion, the tracking undervoltage fault condition is detected. This fault detection is disabled whenever power conversion is disabled.
- **Tracking UVW** is a warning limit, programmable as an offset from the current VOUT_COMMAND value. Program this threshold through VOUT_UV_WARN_LIMIT. When the VSP-VSN pin differential voltage exceeds this limit during power conversion, the tracking undervoltage warning condition is detected. This is a warning condition only, and does not cause any interruption to power conversion. The undervoltage warning provides early feedback to they system host allowing it to make adjustments prior a fault triggering.

In response to the undervoltage warning condition, TPS536C7B1 sets the appropriate status bits in STATUS_WORD and STATUS_VOUT and asserts the SMB_ALERT# line if these bits are not masked.

In response to the undervoltage fault condition TPS536C7B1 responds according to the programmed VOUT_UV_FAULT_RESPONSE. When not set to the ignore response, this causes the PWM pins of the rail which experienced a fault to tristate immediately. TPS536C7B1 then sets the appropriate status bits in STATUS_WORD and STATUS_VOUT and asserts the SMB_ALERT# line if these bits are not masked.

Program the tracking undervoltage fault threshold through the VOUT_UV_FAULT_LIMIT command as an absolute voltage. When a new VOUT_UV_FAULT_LIMIT command is received, the device calculates the tracking undervoltage offset value internally according to Equation 38. Threshold voltages get scaled with the use of an external voltage sensing divider, and VOUT_SCALE_LOOP. TPS536C7B1 supports tracking undervoltage fault offsets from -32 mV to -448 mV in 32 mV steps.

Program the tracking undervoltage warning through the VOUT_UV_WARN_LIMIT command as an absolute voltage. When a new VOUT_UV_WARN_LIMIT command is received, the device calculates the tracking undervoltage warning offset according to Equation 39. Threshold voltages get scaled with the use of an external voltage sensing divider, and VOUT_SCALE_LOOP. TPS536C7B1 supports tracking undervoltage warning offsets from -24 mV to -448 mV in 8 mV steps.

$$V_{OFS(UVW\ TRK)} = \frac{VOUT\_COMMAND - VOUT\_UV\_WARN\_LIMIT}{VOUT\_SCALE\_LOOP} \quad (40)$$

$$V_{OFS(UVF\ TRK)} = \frac{VOUT\_COMMAND - VOUT\_UV\_FAULT\_LIMIT}{VOUT\_SCALE\_LOOP} \quad (41)$$

The undervoltage warning and fault trip thresholds include the load-line setting as shown in Equation 33 and Equation 34.

$$V_{UVW(trip)} = VOUT\_COMMAND - V_{OFS(UVW\ TRK)} - VOUT\_DROOP \times I_{OUT} \quad (42)$$

$$V_{UVF(trip)} = VOUT\_COMMAND - V_{OFS(UVF\ TRK)} - VOUT\_DROOP \times I_{OUT} \quad (43)$$

Example: Programming the UVF and UVW thresholds

Assume the current VOUT_COMMAND is 1.000 V, the VOUT_DROOP setting is equal to 0.5 mΩ, and the load current is equal to 100 A.

- Program the VOUT_UV_WARN_LIMIT to 0.872 V (1.0 V - 128 mV), to select the -128 mV tracking undervoltage warning offset. The VOUT_DROOP is assumed to be zero for calculation purposes. However, the undervoltage warning trip threshold does account for the load-line setting and is equal to 0.872 V - 0.5 mΩ × I_{OUT}.
- Program the VOUT_UV_FAULT_LIMIT to 0.744 V (1.0 V - 256 mV), to select the -256 mV tracking undervoltage fault offset. The VOUT_DROOP is assumed to be zero for calculation purposes. However,

the undervoltage fault trip threshold does account for the load-line setting and is equal to 0.744 V - 0.5 mΩ × I_{OUT}.

If the VOUT_COMMAND value is changed to is 1.100 V, the TPS536C7B1 reports VOUT_UV_WARN_LIMIT as 0.972 V (1.1 V - 128 mV), and VOUT_UV_FAULT_LIMIT as 0.844 V (1.1 V - 256 mV). The offset values are not changed.

7.7.4.3 Maximum turn-on time exceeded (TON_MAX)

The TON_MAX_FAULT_LIMIT command sets a maximum allowable time during which the output voltage must reach the regulation window during turn-on. The TON_MAX time is defined as the time between the first switching pulses, and the sensed output voltage exceeding the the minimum allowed regulation point, defined as V_{TONMAX}, in Equation 35. Program the TON_MAX_FAULT_LIMIT greater than the TON_RISE.

$$V_{TONMAX} = \text{VOUT\_UV\_FAULT\_LIMIT} - (\text{VOUT\_DROOP} \times \text{IOUT\_OC\_FAULT\_LIMIT}) \quad (44)$$

Figure 7-30 illustrates the TON_MAX fault. TPS536C7B1 enables its undervoltage fault protection at the first PWM pulses, during the output voltage rise time. Consequently, whenever the VOUT_UV_FAULT_RESPONSE is not set to the ignore response, it triggers first and disables power conversion prior to the TON_MAX time.

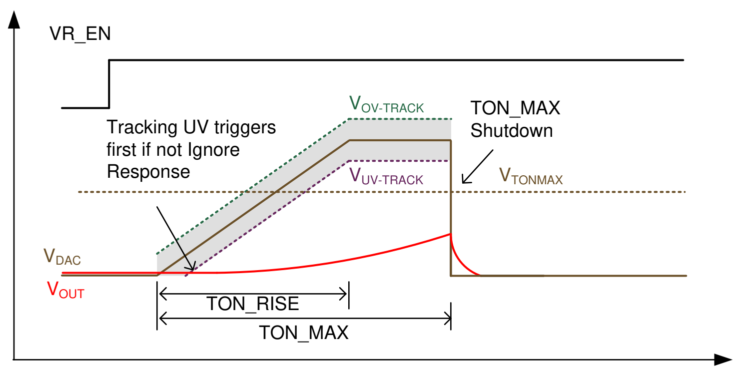


Figure 7-30. TON_MAX fault

In response to the TON_MAX fault condition, TPS536C7B1 responds according to the programmed TON_MAX_FAULT_RESPONSE. When not set to the ignore response, this causes the PWM pins of the rail which experienced the fault to tristate immediately. The TPS536C7B1 then sets the appropriate status bits in STATUS_WORD and STATUS_VOUT and asserts the SMB_ALERT# line if these bits are not masked.

7.7.4.4 Output commanded out-of-bounds (VOUT_MIN_MAX)

The VOUT_MIN and VOUT_MAX commands set the minimum and maximum allowed output voltage targets. TPS536C7B1 does not ramp the output voltage target for either channel outside these limits for any reason. This includes being commanded to do so by VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW or VOUT_TRIM.

Whenever the output voltage target is commanded outside the limits set by VOUT_MIN and VOUT_MAX, TPS536C7B1 detects the VOUT_MIN_MAX warning condition. In response, TPS536C7B1 begins ramping the output voltage target of that channel to the new target, and "clamps" to the VOUT_MIN or VOUT_MAX value. An example is shown in Figure 7-31.

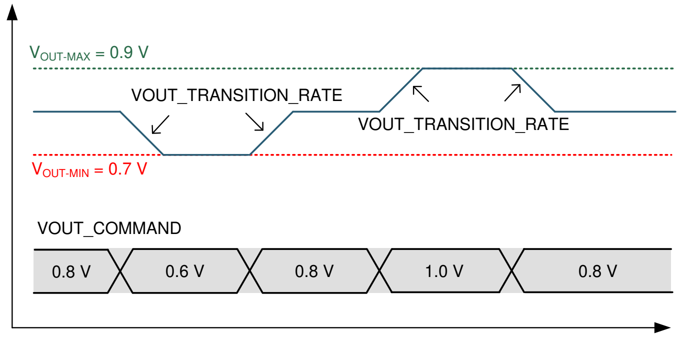


Figure 7-31. VOUT_MIN_MAX example

7.7.4.5 Overcurrent fault (OCF), warning (OCW), and per-phase overcurrent limit (OCL)

TPS536C7B1 provides three layers of overcurrent protection:

- **Overcurrent fault (OCF)** is a programmable threshold which sets the maximum allowed *total current* (sum of all phases) for a channel. Detection is based on output current telemetry. When the sensed output current for a channel exceeds this limit, the output overcurrent fault is detected. Program this threshold using the IOUT_OC_FAULT_LIMIT command with the PHASE set to FFh. TPS536C7B1 supports values of 0 to 1023 A per channel.
- **Per-phase overcurrent limit (OCL)** is a programmable cycle-by-cycle *valley current* limit for each individual phase current, to protect against inductor saturation. TPS536C7B1 does not pass PWM pulses to phases when their current is above the configured OCL threshold. Other than cycle-by-cycle current limit, no action is taken when the per-phase OCL is engaged. Typically, in the case of a severe overload event, power conversion is disabled when the output voltage reaches the VOUT_UV_FAULT_LIMIT. This is illustrated in Figure 7-32. Program the OCL threshold using the IOUT_OC_FAULT_LIMIT command with the PHASE set to 00h. TPS536C7B1 supports values of 17 A to 130 A per phase.
- **Overcurrent warning (OCW)** is a programmable warning threshold based on the *total current* (sum of all phases) for a channel. Detection is based on output current telemetry. When the sensed output current for a channel exceeds this limit, the output overcurrent warning is detected. Program this threshold using the IOUT_OC_WARN_LIMIT. TPS536C7B1 supports values of 0 to 1023 A per channel.

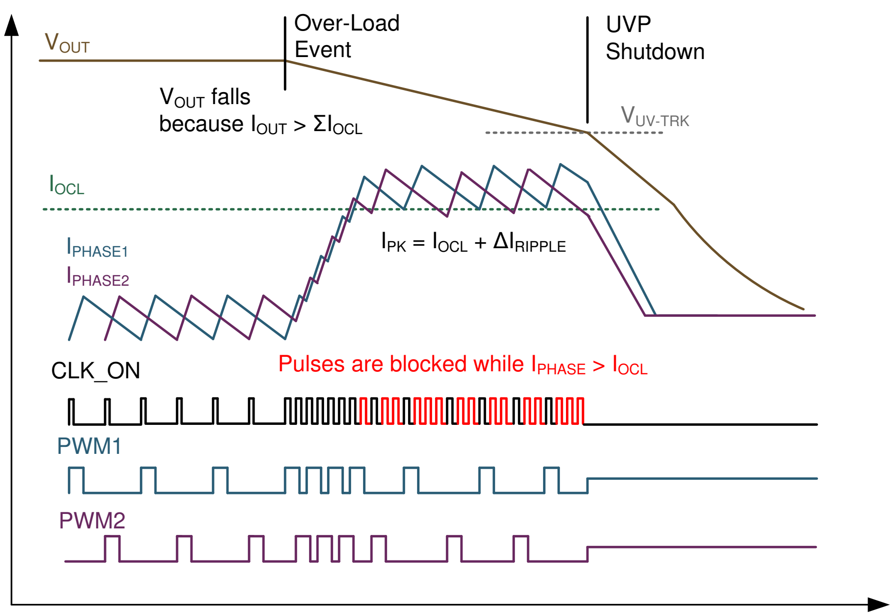


Figure 7-32. Per-phase OCL (2 phase example)

Typically, set the per-phase OCL threshold greater than total peak design current $I_{PK\text{-}CHANNEL}$ to allow margin for transient events, as shown in Equation 36. TI recommends 30-50% design margin. Then peak current allowed in any individual phase is given by Equation 37. Select output inductor components such that current saturation levels are above this limit, including margin for threshold and current sensing accuracy.

$$I_{OCL(min)} = K_{MARGIN} \times \frac{I_{OUT(peak)}}{N_{\Phi}} - \frac{1}{2}\Delta I_{RIPPLE} \quad (45)$$

where

- $I_{OCL(min)}$ is the per-phase overcurrent limit in amperes
- $I_{OUT(PEAK)}$ is the peak design current in amperes
- N_{ϕ} is the number of phases assigned to the channel
- K_{MARGIN} is a factor of safety for design margin

$$I_{PEAK(phase)} = I_{OCL} + \Delta I_{RIPPLE} \quad (46)$$

where

- $I_{PEAK(phase)}$ is the peak current observed in any individual phase
- I_{OCL} is the per-phase overcurrent limit in amperes
- ΔI_{RIPPLE} is the peak-to-peak inductor current ripple

In response to the overcurrent warning condition, TPS536C7B1 sets the appropriate status bits in STATUS_WORD and STATUS_IOUT and asserts the SMB_ALERT# line if these bits are not masked.

In response to the overcurrent fault condition, TPS536C7B1 responds according to the programmed IOUT_OC_FAULT_RESPONSE. When not set to the ignore response, this causes the PWM pins of the rail which experienced a fault to tristate immediately. TPS536C7B1 then sets the appropriate status bits in STATUS_WORD and STATUS_IOUT and asserts the SMB_ALERT# line if these bits are not masked.

7.7.4.6 Current share warning (ISHARE)

The TPS536C7B1 telemetry system continually monitors the average current in each phase, and compares it to the average current of all phases assigned the channel. For each phase, whenever the condition described by Equation 38 is satisfied, the current share warning condition is detected. Configure the current share warning threshold through the MFR_PROTECTION_CONFIG command.

$$\left(\frac{I_{SUM}}{N_{\Phi}} - I_{PHASE}\right) \le -I_{SHAREW} \quad \text{or} \quad \left(I_{PHASE} - \frac{I_{SUM}}{N_{\Phi}}\right) \ge +I_{SHAREW} \quad (47)$$

where

- I_{PHASE} is the current in each individual phase of a channel
- I_{SUM} is the total current in that channel
- N_{ϕ} is the total number of phases assigned to that channel
- I_{SHAREW} is the programmed ISHARE warning in amperes

In response to the current share warning condition, TPS536C7B1 sets the appropriate status bits in STATUS_WORD and STATUS_IOUT and asserts the SMB_ALERT# line if these bits are not masked.

7.7.4.7 Overtemperature fault protection (OTF) and warning (OTW)

TI smart power stages sense their internal die temperature and output temperature information as a voltage signal through their TAO pins. The temperature sense output of the powerstage device includes an OR'ing function such that the voltage signal present at the TSEN pin of the TPS536C7B1 represents that of the hottest powerstage in the channel. The TPS536C7B1 digitizes its TSEN pins to provide temperature telemetry.

- **Overtemperature fault (OTF)** is a programmable threshold which sets the maximum allowed temperature of the powerstage devices attached to a channel. Detection is based on output temperature telemetry. When the sensed temperature for a channel exceeds this limit, the overtemperature fault condition is detected. Program this threshold using the OT_FAULT_LIMIT command. TPS536C7B1 supports values of 90 to 160 °C.
- **Overtemperature warning (OTW)** is a programmable threshold which sets a warning based on the temperature sense telemetry for a channel. Detection is based on temperature sense telemetry. When the sensed temperature for a channel exceeds this limit, the overtemperature warning is detected. Program this threshold using the OT_WARN_LIMIT. TPS536C7B1 supports values of 90 to 160 °C.

In response to the overtemperature warning condition, TPS536C7B1 sets the appropriate status bits in STATUS_WORD and STATUS_TEMPERATURE and asserts the SMB_ALERT# line if these bits are not masked.

In response to the overtemperature fault condition, TPS536C7B1 responds according to the programmed OT_FAULT_RESPONSE. When not set to the ignore response, this causes the PWM pins of the rail which experienced a fault to tristate immediately. TPS536C7B1 then sets the appropriate status bits in STATUS_WORD and STATUS_TEMPERATURE and asserts the SMB_ALERT# line if these bits are not masked.

7.7.4.8 Powerstage fault (TAO_HIGH) and powerstage not ready (TAO_LOW)

In addition to temperature sense information, the TPS536C7B1 and TI smart power stage devices use the TAO lines to communicate fault information:

- **Powerstage fault (TAO_HIGH)** is a fault condition detected when any of the connected powerstage devices pulls its TAO line high (> 2.5 V). This occurs for any fault conditions detected inside the smart powerstage itself. Refer to the individual powerstage datasheets for a complete list of conditions which cause the powerstage fault. Program the controller response to a powerstage fault with MFR_PROTECTION_CONFIG.
- **Powerstage not ready (TAO_LOW)** is a fault condition detected when the TAO line is low (160 mV falling, 245 mV rising) for any reason. At power-on, the TI smart power stages hold their TSEN/TAO lines low, until their internal logic is valid, and their state is known (TAO_LOW condition). Once each device is in a valid state, it's pull-down of the shared TSEN/TAO line is released, and the TAO/TSEN lines are driven by the power-stage devices, based on temperature sense telemetry. The start-up of TPS536C7B1 is blocked while the TAO_LOW condition exists, such that the controller does not attempt to begin conversion, until the TAO/TSEN line is released by all power stages. During the initial power-on, no status bit or alerts are set if the controller is commanded to enable with one of its TSEN/TAO pins low. This is done to accomodate power sequences which have the power stage 5V rail being enabled after the controller 3.3V. The TAO_LOW fault is a hysteretic-type response. When the TSEN/TAO pin is released, if the VR enable condition is still active, power conversion starts immediately.

In response to the powerstage fault, the TPS536C7B1 responds according to the configured fault response in MFR_PROTECTION_CONFIG. When not set to the ignore response, this causes the PWM pins for that channel to tristate immediately. TPS536C7B1 then sets the appropriate status bits in STATUS_WORD and STATUS_MFR_SPECIFIC and asserts the SMB_ALERT# line if these bits are not masked.

In response to the TAO_LOW condition, TPS536C7B1 tristates the PWM pins for that channel. TPS536C7B1 then sets the appropriate status bits in STATUS_WORD and STATUS_MFR_SPECIFIC and asserts the SMB_ALERT# line if these bits are not masked. TAO_LOW is a hysteretic fault and cannot be configured otherwise.

7.7.4.9 Input overvoltage fault (VIN_OVF) and warning (VIN_OVW)

TPS536C7B1 supports two layers of input overvoltage protection:

- **Input overvoltage fault (VIN_OVF)** is a programmable threshold which sets the maximum allowed input voltage, above which it is not safe to convert power. Detection is based on input voltage telemetry. When the sensed input voltage exceeds this limit, the input overvoltage fault condition is detected. Program this threshold using the VIN_OV_FAULT_LIMIT command. TPS536C7B1 supports values of 0 to 19 V.
- **Input overvoltage warning (VIN_OVW)** is a programmable threshold which sets a warning based on the input voltage sense telemetry. Detection is based on input voltage sense telemetry. When the sensed input voltage for a channel exceeds this limit, the input overvoltage warning is detected. Program this threshold using the VIN_OV_WARN_LIMIT command. TPS536C7B1 supports values of 0 to 19 V.

In response to the input overvoltage fault, the TPS536C7B1 responds according to the configured fault response in VIN_OV_FAULT_RESPONSE. When not set to the ignore response, this causes the PWM pins for both channels to tristate immediately. TPS536C7B1 then sets the appropriate status bits in STATUS_WORD and STATUS_INPUT and asserts the SMB_ALERT# line if these bits are not masked.

7.7.4.10 Input undervoltage fault (VIN_UVF), warning (VIN_UVW) and turn-on voltage (VIN_ON)

Three programmable parameters control the TPS536C7B1 input undervoltage protection. More detail is shown in Figure 7-33.

- **Turn-on voltage (VIN_ON)** is the input voltage at which TPS536C7B1 allows power conversion to be enabled. Program this threshold through the VIN_ON command. The input undervoltage fault and warning are masked until the turn-on voltage is exceeded the first time during power-up. TPS536C7B1 does not act on commands to enable power conversion while the input voltage is below this limit. No action is taken when the input voltage falls below this threshold during power conversion. Detection is based on input voltage telemetry. TPS536C7B1 supports values from 4.25 V to 11.5 V.

- **Input undervoltage fault (VIN_UVF)** is the input voltage at which power conversion stops. Program this threshold through the VIN_UV_FAULT_LIMIT command. This command is also forced equal to the turn-off voltage (VIN_OFF). Detection is based on input voltage telemetry. When the sensed input voltage falls below this limit, the input undervoltage fault condition is detected. This fault is masked until the sensed input voltage exceeds the turn-on voltage VIN_ON for the first time. TPS536C7B1 supports values from 4.00 V to 11.25 V.
- **Input undervoltage warning (VIN_UVW)** is a programmable threshold which sets a warning based on the input voltage sense telemetry for a channel. Detection is based on input voltage sense telemetry. When the sensed input voltage below this limit, the input undervoltage warning is detected. Program this threshold using the VIN_UV_WARN_LIMIT. TPS536C7B1 supports values of 4.0 V to 11.25 V.

The input undervoltage fault is triggered when the sensed input voltage falls below the VIN_UV_FAULT_LIMIT threshold, and considered to be cleared when the sensed input voltage exceeds the VIN_ON limit. The input undervoltage fault is enabled only when either of the channels is enabled. Toggling the enable for both channels at the same time with the input voltage above the VIN_UV_FAULT_LIMIT threshold clears the fault, and enables power conversion to begin automatically after the input voltage exceeds the VIN_ON limit. In the case where the enable for each channel is independent, commanding one channel to enable conversion does not clear the input undervoltage condition and power conversion may not start automatically when the input voltage exceeds the VIN_ON thresholds. TI recommends to enable power conversion only after the input voltage exceeds the VIN_ON as shown in Figure 7-33.

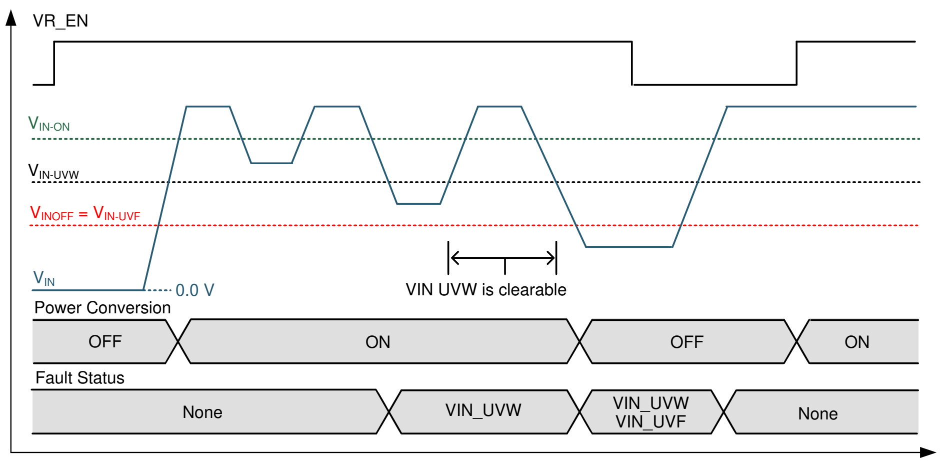


Figure 7-33. Input undervoltage protection (VR_EN active high control)

7.7.4.11 Input overcurrent fault (IIN_OCF) and warning (IIN_OCW)

- **Input overcurrent fault (IIN_OCF)** is a programmable threshold which sets the maximum allowed input current for the converter. Detection is based on input current telemetry. When the sensed input current exceeds this limit, the input overcurrent fault condition is detected. Program this threshold using the IIN_OC_FAULT_LIMIT command. TPS536C7B1 supports values of 4 to 128A.
- **Input overcurrent warning (IIN_OCW)** is a programmable threshold which sets a warning threshold for the input current for the converter. Detection is based on input current telemetry. When the sensed input current exceeds this limit, the input overcurrent warning condition is detected. Program this threshold using the IIN_OC_WARN_LIMIT command. TPS536C7B1 supports values of 4 to 128A.

In response to the input overcurrent fault, the TPS536C7B1 responds according to the configured fault response in IIN_OC_FAULT_RESPONSE. When not set to the ignore response, this causes the PWM pins for both channels to tristate immediately. TPS536C7B1 then sets the appropriate status bits in STATUS_WORD and STATUS_INPUT and asserts the SMB_ALERT# line if these bits are not masked.

7.7.4.12 Input overpower warning (PIN_OPW)

The PIN_OP_WARN_LIMIT command sets an input overpower warning limit for the converter. Detection is based on the input power telemetry, which is derived by multiplying the input voltage and input current measurement values. When the input current telemetry measurements exceeds this limit, TPS536C7B1 detects the input overpower warning condition. TPS536C7B1 supports values from 8 to 2044 W.

The input overpower warning does not interrupt power conversion. In response, TPS536C7B1 sets the appropriate status bits in STATUS_WORD and STATUS_INPUT and asserts the SMB_ALERT# line if these bits are not masked.

7.7.4.13 PMBus command, memory and logic errors (CML)

The STATUS_CML command provides information about communication errors which have occurred. Communication errors are warnings and do not cause any interruption to power conversion.

- **Invalid command (IVC)** occurs when the host attempts to access TPS536C7B1 at a command which it does not support.
- **Invalid data (IVD)** occurs when the host sends data to a supported command which is out of range or unsupported.
- **Packet error check (PEC) error** occurs when TPS536C7B1 receives a transaction with an invalid or incorrect PEC byte.
- **Communication error (COMM)** occurs when the SMBus timeout condition is detected.
- **Other (CML_OTHER)** can occur due to multiple conditions (may not be an exhaustive list):
  - Wrong transaction prototype - e.g. accessing a read word command as a read block
  - Block command send with the incorrect number of bytes, or block count was not acknowledged
  - Bus arbitration was lost
  - Transaction aborted

7.8 Device Functional Modes

Power-on Reset (POR)

When the VCC in voltage is below approximately 2.5 V, the TPS536C7B1 enters power-on reset, and all internal blocks return to their unpowered state. Raise the VCC voltage above the input UVLO threshold to exit the POR state. Exiting POR requires up to 20 ms before power conversion can be enabled, during which the device re-loads all NVM values and performs pinstrap detection.

Disabled state

The ON_OFF_CONFIG PMBus command specifies the combination of VR_EN pins and OPERATION command input required to start power conversion. When the specified combination is not met (e.g. VR_EN is low, for VR_EN only, active high configuration), power conversion is disabled. The PWM pins assigned to the channel remain at tri-state, and the VR_RDY pin for the channel is pulled low. Once the enable conditions are met (e.g. VR_EN pulled high for VR_EN only, active high configuration), the controller begins power conversion, after a period of approximately 750 µs plus any added turn-on delay. The TPS536C7B1 device returns to the disabled state after being disabled by the same means.

Turn-on and turn-off delay

The TON_DELAY and TOFF_DELAY commands allow the user to add additional turn-on or turn-off delay between the time that enable/disable conditions are satisfied, and the TPS536C7B1 begins ramping the output voltage. To ensure consistent behavior, TI recommends not to interrupt the turn-on or turn-off delays with additional enable/disable requests.

Soft-start and soft-off shutdown

The soft-start period begins when the first PWM pulses are fired after a channel is enabled, and ends when the internal loop DAC reaches the boot voltage. During this time, the controller is raising the output voltage at a slew rate derived from to track the loop DAC, and tracking over/undervoltage protections are active.

TPS536C7B1 may be configured to actively ramp the output voltage down to zero after being disabled through the ON_OFF_CONFIG command. During this time, the controller ramps down the loop DAC to zero at the slew rate derived from TOFF_FALL. This behavior is optional, and the default configuration is to have the channel enter directly into the disabled state (immediate off).

Normal operation

The TPS536C7B1 is in the normal state when converting power. During this time, the device responds to new output voltage target (DVID) commands through PMBus as configured through the OPERATION command.

Power conversion continues in Auto-DCM, FCCM dynamic phase shedding, or all phases FCCM, as configured through the PMBus interface.

Fault shutdown (Latch-off)

Any time a fault which is configured with the latch-off response is triggered, the device stops power conversion on the affected channel (or both if caused by a shared fault). The PWM pins remain at tri-state for all faults, excepting over-voltage faults which cause the PWM pins to remain low. The VR_RDY pin remains low as long as the converter is disabled. It remains in this state until commanded to re-enable as specified in ON_OFF_CONFIG.

Fault shutdown (Hiccup)

Any time a fault which is configured with the hiccup response is triggered, the device stops power conversion on the affected channel (or both if caused by a shared fault). The PWM pins remain at tri-state for all faults, excepting over-voltage faults which cause the PWM pins to remain low. It remains in this state until a timer expires, then attempt to re-enable itself, while respecting the configured TON_DELAY and TOFF_DELAY times. The VR_RDY pin remains low as long as the converter is disabled, and re-asserts after a successful start-up attempt.

POR Fault shutdown

Some fault conditions are considered catastrophic and cause the TPS536C7B1 to refuse any further enable attempts. These include: memory errors, internal logic errors, invalid pinstrap, pre-bias overvoltage protection conditions. The only way to recover from a POR fault is to re-cycle the VCC pin voltage below the POR threshold.

7.9 Programming

7.9.1 PMBus overview

TPS536C7B1 is designed to be compatible with the timing and physical layer electrical characteristics of the Power Management Bus (PMBus) Specification, part I, revision 1.3.1 available at http://pmbus.org. The 100-kHz, 400-kHz, and 1000-kHz classes are supported. Input logic levels are designed to be compaitible with 1.8-V and 3.3-V logic. PMBus revision 1.3 is derived from the System Managmenet Bus (SMBus) revision 3.0, available at http://smbus.org/. The communication mechanism is based on the inter-integrated circuit I^2C protocol.

A master with clock stretching support is mandatory for communication with TPS536C7B1 through the PMBus interface. TPS536C7B1 does support the packet error check (PEC) protocol. If the system host supplies clock pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used. TPS536C7B1 can be configured to require PEC for each transaction in systems which require high reliability of communication.

TPS536C7B1 supports the SMB_ALERT# response protocol. The SMB_ALERT# response protocol is a mechanism by which a slave device can alert the master device that it is available for communication. The master device processes this event and simultaneously accesses all slave devices on the bus (that support the protocol) through the alert response address (ARA). Only the slave device that caused the alert acknowledges this request. The host device performs a modified receive byte operation to ascertain the slave devices address. At this point, the master device can use the PMBus status commands to query the slave device that caused the alert. By default, these devices implement the auto alert response, a manufacturer specific improvement to the SMB_ALERT# response protocol, intended to mitigate the issue of bus hogging. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

7.9.2 PMBus transaction types

Support for the following SMBus transaction types is mandatory. The use of PEC is optional. Refer to the SMBus specification and *Technical Reference Manual* for more detailed transaction diagrams.

SMBus Write Block and Read Block transaction types contain a repeated start condition, which may not be compatible with all I^2C master device IP.

- Write Byte / Read Byte
- Write Word / Read Word
- Write Block / Read Block
- Send Byte / Receive Byte
- Block-Write-Block-Read Process Call (for SMBALERT_MASK commands)

7.9.3 PMBus data formats

TPS536C7B1 supports 3 data formats according to the PMBus specification. The data format for each command is listed along with its address and supported values.

- **ULINEAR16 format** uses a 16-bit unsigned integer. The default LSB size is 2^{-10} = 0.97656 mV
- **SLINEAR16 format** uses a 16-bit number representing a decimal. This number has two fields: the 5 MSB bits form an two's complement *exponent*, referred to as N, and the 11 LSB bits form a two's complement *mantissa*, referred to as M. The decimal number is represented as $D = M \times 2^N$
- **Unsigned binary format** uses direct bit maps with each command being subdivided into multiple fields that can have different meaning. Refer to the register maps in the *Technical Reference Manual* for these commands.

TPS536C7B1 accepts writes to SLINEAR11 format commands with any desired exponent value. TI recommends using the default exponent listed for each command for writes to ensure consistent NVM store and restore behavior.

Telemetry commands in the SLINEAR11 format return data with variable exponent values according to the absolute value of the retured value. As a rule TPS536C7B1 returns data in the SLINEAR11 format with the smallest possible exponent, to provide the highest possible command resolution. As a result the host must be able to support decoding of the SLINEAR11 format with any exponent value.

7.9.3.1 Example PMBus number format conversions

Example: Decode SLINEAR11 number E804h

E804h = 11101 00000000100b

Exponent = 11101b. N = -3 (5-bit two's complement)

Mantissa = 00000000100b. M = 4 (11-bit two's complement)

The decimal number D = M × 2^N = 4 × 2^{-3} = 0.5

Example: Encode 5.25 to SLINEAR11 with exponent -4

Exponent = -4 = 11100b (5-bit two's complement)

Mantissa = 5.25 / 2^N = 5.25 / 2^{-4} = 84d = 00001010100b (11-bit two's complement)

SLINEAR11 representation = 11100 00001010100b = E054h

Example: Encode 1.00 V to ULINEAR16 with VOUT_MODE = 16h

VOUT_MODE = 16h (Linear Absolute). Exponent (PARAMETER) = 10110b = -10 (5-bit two's complement)

1.00 V = 1.00 / 2^{-10} = 1024d = 0400h

Example: Decode 03E6h in ULINEAR16 with VOUT_MODE = 16h

VOUT_MODE = 16h (Linear Absolute). Exponent (PARAMETER) = 10110b = -10 (5-bit two's complement)

2^{-10} × 03D6h = 0.9746 V

7.9.3.2 Example system code for PMBus format conversion

Example code for handling the SLINEAR11 and ULINEAR16 formats at the system level is given below. Example code in a syntax similar to the C programming language is provided for reference only. Error checking code is not included. It is the responsibility of the system designer to verify and test all system code.

```
//Maps 5 bit linear exponent to LSB value (2^(twos complement of index))
const float LUT_linear_exponents[32] = {
    1.0,2.0,4.0,8.0,16.0,32.0,64.0,128.0,256.0,512.0,1024.0,2048.0,4096.0,8192.0,
    16384.0,32768.0,0.0000152587890625,0.000030517578125,0.00006103515625,
    0.0001220703125,0.000244140625,0.00048828125,0.0009765625,0.001953125,0.00390625,
    0.0078125,0.015625,0.03125,0.0625,0.125,0.25,0.5
};
```

Figure 7-34. Linear exponent to LSB converstion (look-up table approach)

```
unsigned int float_to_slinear11(float number, signed int exponent)
{
    signed int mantissa;
    float lsb;

    //Decode the exponent and generate twos complement form
    if(exponent < 0) {
        lsb = LUT_linear_exponents[(exponent+32)];
    } else {
        lsb = LUT_linear_exponents[exponent];
    }

    //Decode mantissa based on exponent and generate twos complement form
    mantissa = (signed int)(number / lsb);

    //If numbers are negative, de-sign-extend to 5/11 bit numbers
    mantissa &= 0x07FF;
    exponent &= 0x1F;
    return (mantissa | (exponent << 11));
}
```

Figure 7-35. Floating point to SLINEAR11 conversion

```
float slinear11_to_float(unsigned int number)
{
    unsigned int exponent;
    int mantissa;
    float lsb;

    exponent = number >> 11;
    mantissa = number & 0x07FF;

    //Sign extend Mantissa to 32 bits (use your int size here)
    if (mantissa > 0x03FF) {
        mantissa |= 0xFFFFF800;
    }

    lsb = LUT_linear_exponents[exponent];

    return ((float)mantissa)*lsb;
}
```

Figure 7-36. SLINEAR11 to floating point conversion

```
unsigned int float_to_ulinear16(float number, unsigned char vout_mode)
{
    float lsb;
    lsb = LUT_linear_exponents[(vout_mode & 0x1F)];
    return (unsigned int)(number/lsb);
}
```

Figure 7-37. Floating point to ULINEAR16 conversion

```
float ulinear16_to_float(unsigned int number, unsigned char vout_mode)
{
    float lsb;
    lsb = LUT_linear_exponents[(vout_mode & 0x1F)];
    return ((float)number)*lsb;
}
```

Figure 7-38. ULINEAR16 to floating point conversion

7.9.4 Raw non-volatile memory programming

TPS536C7B1 has 256 bytes of internal EEPROM non-volatile memory (NVM). Each PMBus command with NVM backup is mapped into the NVM array. For example, if a command supports 16 possible values, there are 4 corresponding bits for that field. The NVM array is designed withstand being overwritten greater than 1,000 times over the lifetime of the device.

The USER_NVM_INDEX and USER_NVM_EXECUTE commands provide access to read and write the raw data bytes. These commands allow the entire configuration data for the device to be read/written with a minimum number of transactions, to save programming time. The USER_NVM_EXECUTE command is a 32 byte block which accesses blocks of raw NVM data. The USER_NVM_INDEX command is an auto-incrementing byte command which which selects which 32 bytes of memory are being accessed via the USER_NVM_EXECUTE command.

The *Fusion Digital Power Designer* software provided for this device is capable of exporting raw configuration data, as well as XML configuration files containing the value of each PMBus command.

Configuration validation

The first 9 bytes of data returned by USER_NVM_EXECUTE with index zero, are identifying information for the configuration. Bytes 0 to 6 represent the IC_DEVICE_ID. Bytes 7-8 represent the IC_DEVICE_REV. Byte 9 represents the currently configured PMBus slave address.

During the NVM import process, the controller checks these 9 bytes versus its current configuration, and NACKs theUSER_NVM_EXECUTE (index = 0) command if the data does not match.

Example: Configuration validation

- Reading the USER_NVM_EXECUTE (index 0) from a configured device returns value 0x54 49 53 6C 70 00 00 04 60 … [NVM bytes 0 to 22]. This indicates the configuration data was generated from a device with IC_DEVICE_ID 0x54 49 53 6C 70 00, IC_DEVICE_REV 00 04 and PMBus address 0x60.
- Writing the USER_NVM_EXECUTE (index 0) with the value 0x54 49 53 6C 70 00 00 04 60 … [NVM bytes 0 to 22] to a new device causes it to check its IC_DEVICE_ID is equal to 0x54 49 53 6C 70 00, check its IC_DEVICE_REV is equal to 00 04 and check its PMBus address 0x60. If any of these checks fail, the write operation is rejected.
- Writing the USER_NVM_EXECUTE (index 0) with the value 0xFF FF FF FF FF FF 00 04 60 … [NVM bytes 0 to 22] to a new device causes it skip the IC_DEVICE_ID check, but still check its IC_DEVICE_REV is equal to 00 04 and check its PMBus address 0x60. If any of these checks fail, the write operation is rejected.
- Writing the USER_NVM_EXECUTE (index 0) with the value 0xFF FF FF FF FF FF FF FF 60 … [NVM bytes 0 to 22] to a new device causes it skip the IC_DEVICE_ID check, skip its IC_DEVICE_REV check, but still check its PMBus address 0x60. If any of these checks fail, the write operation is rejected.
- Writing the USER_NVM_EXECUTE (index 0) with the value 0xFF FF FF FF FF FF FF FF FF … [NVM bytes 0 to 22] to a new device causes it skip the IC_DEVICE_ID check, skip its IC_DEVICE_REV check, and skip its PMBus address check. No checks were performed, so the data is accepted.

Procedure: Read all configuration data

Follow the procedures below to read-back NVM data for TPS536C7B1 devices.

1. Configure the device as desired through PMBus commands, then issue STORE_USER_ALL. Power cycle the device or issue RESTORE_USER_ALL with power conversion disabled to ensure operating memory and non-volatile memory bytes are matching.
2. Write the USER_NVM_INDEX command to 00h.
3. Read back and record the USER_NVM_EXECUTE command (index = 0).
4. Read back and record the USER_NVM_EXECUTE command (index = 1).
5. Read back and record the USER_NVM_EXECUTE command (index = 2).
6. Read back and record the USER_NVM_EXECUTE command (index = 3).
7. Read back and record the USER_NVM_EXECUTE command (index = 4).
8. Read back and record the USER_NVM_EXECUTE command (index = 5).
9. Read back and record the USER_NVM_EXECUTE command (index = 6).
10. Read back and record the USER_NVM_EXECUTE command (index = 7).
11. Read back and record the USER_NVM_EXECUTE command (index = 8). The last 23 bytes of this command are not used by the device. TI recommends replacing these bytes with 00h for consistency across different configurations.

Procedure: Write all configuration data

Follow the procedures below to write NVM data for TPS536C7B1 devices.

1. Apply +3.3V to the VCC pin of TPS536C7B1

2. Ensure power conversion is disabled for both channels.
3. Write the USER_NVM_INDEX command to 00h.
4. Write the previously recorded USER_NVM_EXECUTE (index = 0). In this example, disable the self-validation checks by replacing the first 9 bytes with FFh.
5. Write the previously recorded USER_NVM_EXECUTE (index = 1).
6. Write the previously recorded USER_NVM_EXECUTE (index = 2).
7. Write the previously recorded USER_NVM_EXECUTE (index = 3).
8. Write the previously recorded USER_NVM_EXECUTE (index = 4).
9. Write the previously recorded USER_NVM_EXECUTE (index = 5).
10. Write the previously recorded USER_NVM_EXECUTE (index = 6).
11. Write the previously recorded USER_NVM_EXECUTE (index = 7).
12. Write the previously recorded USER_NVM_EXECUTE (index = 8). Replace the last 23 bytes with 00h. An NVM store operation is automatically performed once the last block is successfully received.
13. Wait 100 ms for non-volatile memory programming to complete successfully. Ensure that the +3.3V power supply to the device is not interrupted during this time to guarantee proper memory storage and retention.
14. **Do not** issue an NVM store operation at this point. This overwrites the NVM array with the data values in operating memory.
15. Power cycle the device or issue RESTORE_USER_ALL to continue operation with the newly programmed values. Multifunction pin configurations require a power cycle to take effect.

Table 7-10. Supported Commands and NVM Defaults

CMD Code	Command Name	Default Behavior Ch. A (PAGE = 0)	Default Behavior Ch. B (PAGE = 1)	Default Hex(2) Ch. A	Default Hex(2) Ch. B	R/W Access, NVM
00h	PAGE	Commands address both Channel A and Channel B		FFh		R/W
01h	OPERATION	OPERATION Off, Margin None	OPERATION Off, Margin None	00h	00h	R/W
02h	ON_OFF_CONFIG	AVR_EN pin only, Active High	BVR_EN pin only, Active High	17h	17h	R/W, NVM
03h	CLEAR_FAULTS	Clears all faults related to channel A	Clears all faults related to channel B	N/A	N/A	W
04h	PHASE	Commands address all phases in channel A	Commands address all phases in channel B	FFh	FFh	R/W
05h	PAGE_PLUS_WRITE	Utility to send PAGE along with a PMBus write transaciton		Per command		W
06h	PAGE_PLUS_READ	Utility to send PAGE along with a PMBus read transaciton		Per command		R
10h	WRITE_PROTECT	All commands are writeable		00h		R/W, NVM
15h	STORE_USER_ALL	Stores all current storable register settings into NVM as new defaults		N/A		W
16h	RESTORE_USER_ALL	Restores all storable register settings from NVM		N/A		W
19h	CAPABILITY	1 MHz, PEC, SMB_ALERT Supported		D0h		R
1Bh	SMBALERT_MASK_WORD	No SMB_ALERT sources masked	No SMB_ALERT sources masked	00h	00h	R/W
1Bh	SMBALERT_MASK_VOUT	No SMB_ALERT sources masked	No SMB_ALERT sources masked	00h	00h	R/W, NVM
1Bh	SMBALERT_MASK_IOUT	No SMB_ALERT sources masked	No SMB_ALERT sources masked	00h	00h	R/W, NVM
1Bh	SMBALERT_MASK_INPUT	LOW VIN bit is masked		08h		R/W, NVM
1Bh	SMBALERT_MASK_ TEMPERATURE	No SMB_ALERT sources masked	No SMB_ALERT sources masked	00h	00h	R/W, NVM
1Bh	SMBALERT_MASK_CML	No SMB_ALERT sources masked	No SMB_ALERT sources masked	00h	00h	R/W, NVM
1Bh	SMBALERT_MASK_MFR	VR SETTLED is masked	No SMB_ALERT sources masked	26h	06h	R/W, NVM
1Bh		FIRST_TO_ALERT does not assert SMB_ALERT#		00h		R
20h	VOUT_MODE	ULINEAR16 Mode, Absolute, Exponent = -10	ULINEAR16 Mode, Absolute, Exponent = -10	16h	16h	R
21h	VOUT_COMMAND	0.880 V From pin-detection by default	1.000 V	03 85h	04 00h	R/W, NVM/ Pin Detect (Ch A)
22h	VOUT_TRIM	+0.000 V	+0.000 V	00 00h	00 00h	R/W, NVM
24h	VOUT_MAX	1.869 V (VBOOT_CHA pinstrp active by default) NVM stored value is 1.200 V	1.400 V	07 7Ah / 04 CDh	05 9Ah	R/W, NVM
25h	VOUT_MARGIN_HIGH	0.000 V	0.000 V	00 00h	00 00h	R/W
26h	VOUT_MARGIN_LOW	0.000 V	0.000 V	00 00h	00 00h	R/W
27h	VOUT_TRANSITION_RATE	5.0 mV/µs	5.0 mV/µs	E0 50h	E0 50h	R/W, NVM
28h	VOUT_DROOP	0.000 mΩ	0.000 mΩ	C8 00h	C80 0h	R/W, NVM
29h	VOUT_SCALE_LOOP	1.000	1.000	E8 08h	E8 08h	R/W, NVM
2Bh	VOUT_MIN	0.000 V	0.000 V	00 00h	00 00h	R/W, NVM
33h	FREQUENCY_SWITCH	500 kHz	500 kHz	01 F4h	01 F4h	R/W, NVM
34h	POWER_MODE	DPS disabled, all phases FCCM	DPS disabled, all phases FCCM	03h	03h	R/W
35h	VIN_ON	9.250 V		F0 25h		R/W, NVM

Table 7-10. Supported Commands and NVM Defaults (continued)

CMD Code	Command Name	Default Behavior Ch. A (PAGE = 0)	Default Behavior Ch. B (PAGE = 1)	Default Hex[(2)] Ch. A	Default Hex[(2)] Ch. B	R/W Access, NVM
38h	IOUT_CAL_GAIN	5.000 mΩ	5.000 mΩ	CA 80h	CA 80h	R/W, NVM
39h	IOUT_CAL_OFFSET	+0.125 A (phase 10) 0.000 A (other phases)	0.000 A (all phases)	E8 01h / E8 00h	E8 00h	R/W, NVM
40h	VOUT_OV_FAULT_LIMIT	1.072 V (VOUT_COMMAND + 192 mV)	1.192 V (VOUT_COMMAND + 192 mV)	04 4Ah[(1)]	04 C5h[(1)]	R/W, NVM
41h	VOUT_OV_FAULT_RESPONSE	Latch-off and do not restart	Latch-off and do not restart	80h	80h	R/W, NVM
42h	VOUT_OV_WARN_LIMIT	1.040 V (VOUT_COMMAND + 160 mV)	1.160 V (VOUT_COMMAND + 160 mV)	04 29h[(1)]	04 A4h[(1)]	R/W, NVM
43h	VOUT_UV_WARN_LIMIT	0.704 V (VOUT_COMMAND - 176 mV)	0.824 V (VOUT_COMMAND - 176 mV)	02 D1h[(1)]	03 4Ch[(1)]	R/W, NVM
44h	VOUT_UV_FAULT_LIMIT	0.688 V (VOUT_COMMAND - 192 mV)	0.808 V (VOUT_COMMAND - 192 mV)	02 C0h[(1)]	03 3Bh[(1)]	R/W, NVM
45h	VOUT_UV_FAULT_RESPONSE	Latch-off after 5.0 µs and do not restart	Latch-off after 5.0 µs and do not restart	40h	40h	R/W, NVM
46h	IOUT_OC_FAULT_LIMIT	480 A total current 53 A phase current	80 A total current 53 A phase current	10 E0h 00 35h	00 50h 00 35h	R/W, NVM
47h	IOUT_OC_FAULT_RESPONSE	Latch-off and do not restart	Latch-off and do not restart	C0h	C0h	R/W, NVM
4Ah	IOUT_OC_WARN_LIMIT	440 A total current	60 A total current	01 B8h	00 3Ch	R/W, NVM
4Fh	OT_FAULT_LIMIT	120°C	120°C	00 78h	00 78h	R/W, NVM
50h	OT_FAULT_RESPONSE	Latch-off and do not restart	Latch-off and do not restart	80h	80h	R/W, NVM
51h	OT_WARN_LIMIT	110°C	110°C	00 6Eh	00 6Eh	R/W, NVM
55h	VIN_OV_FAULT_LIMIT	15.0 V		00 0Fh		R/W, NVM
56h	VIN_OV_FAULT_RESPONSE	Latch-off and do not restart		80h		R/W, NVM
57h	VIN_OV_WARN_LIMIT	14.0 V		00 0Eh		R/W, NVM
58h	VIN_UV_WARN_LIMIT	8.50 V		F0 22h		R/W, NVM
59h	VIN_UV_FAULT_LIMIT	8.00 V		F0 20h		R/W, NVM
5Ah	VIN_UV_FAULT_RESPONSE	Latch-off and do not restart		80h		R/W, NVM
5Bh	IIN_OC_FAULT_LIMIT	52.0 A		00 34h		R/W, NVM
5Ch	IIN_OC_FAULT_RESPONSE	Latch-off and do not restart		C0h		R/W, NVM
5Dh	IIN_OC_WARN_LIMIT	44.0 A		00 2Ch		R/W, NVM
60h	TON_DELAY	0.00 ms	0.00 ms	F8 00h	F8 00h	R/W, NVM
61h	TON_RISE	1.5 ms (SR_{BOOT} = 0.625 mV/µs)	1.5 ms (SR_{BOOT} = 0.625 mV/µs)	F0 06h	F0 06h	R/W, NVM
62h	TON_MAX_FAULT_LIMIT	2.0 ms	2.0 ms	F0 08h	F0 08h	R/W, NVM
63h	TON_MAX_FAULT_RESPONSE	Latch-off and do not restart	Latch-off and do not restart	80h	80h	R/W, NVM
64h	TOFF_DELAY	0.00 ms	0.00 ms	F8 00h	F8 00h	R/W, NVM
65h	TOFF_FALL	1.5 ms (SR_{OFF} = 0.625 mV/µs)	1.5 ms (SR_{OFF} = 0.625 mV/µs)	F0 06h	F0 06h	R/W, NVM
6Bh	PIN_OP_WARN_LIMIT	592.0 W		09 28h		R/W, NVM
78h	STATUS_BYTE	Current status channel A	Current status channel B	Current Status	Current Status	R
79h	STATUS_WORD	Current status channel A	Current status channel B	Current Status	Current Status	R/W
7Ah	STATUS_VOUT	Current status channel A	Current status channel B	Current Status	Current Status	R/W

Table 7-10. Supported Commands and NVM Defaults (continued)

CMD Code	Command Name	Default Behavior Ch. A (PAGE = 0)	Default Behavior Ch. B (PAGE = 1)	Default Hex(2) Ch. A	Default Hex(2) Ch. B	R/W Access, NVM
7Bh	STATUS_IOUT	Current status channel A	Current status channel B	Current Status	Current Status	R/W
7Ch	STATUS_INPUT	Current status		Current Status		R/W
7Dh	STATUS_TEMPERATURE	Current status channel A	Current status channel B	Current Status	Current Status	R/W
7Eh	STATUS_CML	Current status		Current Status	Current Status	R/W
7Fh	STATUS_OTHER	Current status		Current status	Current status	R/W
80h	STATUS_MFR_SPECIFIC	Current status channel A	Current status channel B	Current Status	Current Status	R/W
88h	READ_VIN	Measured input voltage		Current Status		R
89h	READ_IIN	Measured input current		Current Status		R
8Bh	READ_VOUT	Measured output voltage channel A	Measured output voltage channel B	Current Status	Current Status	R
8Ch	READ_IOUT	Measured output current channel A	Measured output current channel B	Current Status	Current Status	R
8Dh	READ_TEMPERATURE_1	Measured power stage temperature channel A	Measured power stage temperature channel B	Current Status	Current Status	R
96h	READ_POUT	Calculated output power channel A	Calculated output power channel B	Current Status	Current Status	R
97h	READ_PIN	Calculated input power		Current Status		R
98h	PMBUS_REVISION	Revision 1.3, Part I and Part II compatible		33h		R
99h	MFR_ID	Manufacturer company identification		02 00 00h		R/W, NVM
9Ah	MFR_MODEL	Manufacturer model identification		00 00 00h		R/W, NVM
9Bh	MFR_REVISION	Manufacturer revision identification		00 00 00h		R/W, NVM
9Dh	MFR_DATE	Manufacturer date identification		00 00 00h		R/W, NVM
ADh	IC_DEVICE_ID	TPS536C7B1		54 49 53 6C 70 00h		R
AEh	IC_DEVICE_REV	Revision 2		00 04h		R
B1h	USER_DATA_01 (COMPENSATION_CONFIG)	DC load line: 0.00 mΩ AC load line: 0.20 mΩ Integration time contsant: 1.0 µs Dynamic integration contsant: 4.0 µs Dynamic integration threshold: 60 mV AC gain: 1.0 Integration gain: 1.0 Ramp amplitude: 360 mV	DC load line: 0.00 mΩ AC load line: 0.4375 mΩ Integration time contsant: 7.0 µs Dynamic integration contsant: 3.0 µs Dynamic integration threshold: 120 mV AC gain: 1.0 Integration gain: 1.0 Ramp amplitude: 200 mV	00 D0 0E 73 0D D0 00 C8h	00 53 66 72 1C D0 00 C8h	R/W, NVM
B2h	USER_DATA_02 (NONLINEAR_CONFIG)	USR1 threshold: 120 mV USR2 threshold: 50 mV Min off time: 30 ns Blanking time: 30 ns OSR: Disabled USR1 phases: 4 phases	USR1 threshold: 120 mV USR2 threshold: 50 mV Min off time: 30 ns Blanking time: 35 ns OSR: Disabled USR1 phases: 4 phases	31 1A 0F 06 DAh	31 1A 0F 07 DAh	R/W, NVM

Table 7-10. Supported Commands and NVM Defaults (continued)

CMD Code	Command Name	Default Behavior Ch. A (PAGE = 0)	Default Behavior Ch. B (PAGE = 1)	Default Hex(2) Ch. A	Default Hex(2) Ch. B	R/W Access, NVM
B3h	USER_DATA_03 (PHASE_CONFIG)	12+0 configuration, 0-2-4-6-8-10-1-3-5-7-9-11 From pin-detection by default		00 80 02 81 04 82 06 83 08 84 0A 85 01 86 03 87 05 88 07 89 09 8A 0B 8Bh		R/W, NVM Pin Detect
B4h	USER_DATA_04 (DVID_CONFIG)	DCLL up: 0.00 mΩ DCLL down: 0.00 mΩ ACLL up: 0.50 mΩ ACLL down: 0.50 mΩ Boot offset: 90mV Dynamic offsets: 0 mV	DCLL up: 0.00 mΩ DCLL down: 0.00 mΩ ACLL up: 0.75 mΩ ACLL down: 0.50 mΩ Boot offset: 40mV Dynamic offsets: 0 mV	03 60 08 08 00 00h	03 20 0C 08 00 00h	R/W, NVM
B7h	USER_DATA_07 (PHASE_SHED_CONFIG)	Phase shedding disabled	Phase shedding disabled	30 08 44 44 44 44 44 2F FF FF FF FF FFh	30 08 44 44 44 44 48 2F FF FF FF FF FFh	R/W, NVM
BAh	USER_DATA_10 (ISHARE_CONFIG)	All phases = 1.0 K_T	All phases = 1.0 K_T	04h all phases	04h all phases	RW, NVM
BBh	USER_DATA_11 (MFR_PROTECTION_CONFIG)	ISHARE warning: 50 mV Fixed OVP channel A: 1.2 V Fixed OVP channel B: 1.6 V Powerstage fault response: Ignore Hiccup wait time: 25 ms		8C 99 00 00 00 55 00 00 00 00h		RW, NVM
BDh	USER_DATA_13 (MFR_CALIBRATION_CONFIG)	IIN shunt: 0.5 mΩ (analog gain: 20, digital gain = 80)		88 00 00 00 50 00 00 00 00 00 00 00 00 00 00h		RW, NVM
CDh	MFR_SPECIFIC_CD (MULTIFUNCTION_PIN_CONFIG_1)	Pin 43: BTSEN Pin 19: BVR_EN		Default Settings		RW, NVM
CEh	MFR_SPECIFIC_CE (MULTIFUNCTION_PIN_CONFIG 2)	Pin 44: ATSEN		Default Settings		RW, NVM
CFh	MFR_SPECIFIC_CF (SMBALERT_MASK_EXTENDED)	On-the-fly SMB_ALERT# Mask bits for bits in STATUS_EXTENDED		00 00 00 00 00 00 00h		RW
D1h	MFR_SPECIFIC_D1 (READ_VOUT_MIN_MAX)	Peak logging function for output voltage telemetry		Current status	Current status	RW
D2h	MFR_SPECIFIC_D2 (READ_IOUT_MIN_MAX)	Peak logging function for output current telemetry		Current status	Current status	RW
D3h	MFR_SPECIFIC_D3 (READ_TEMPERATURE_MIN_MAX)	Peak logging function for temperature telemetry		Current status	Current status	RW
D4h	MFR_SPECIFIC_D4 (READ_MFR_VOUT)	Ouptut voltage telemetry in SLINEAR11 format		Current status	Current status	R
D5h	MFR_SPECIFIC_D5 (READ_VIN_MIN_MAX)	Peak logging function for input voltage telemetry		Current status		RW
D6h	MFR_SPECIFIC_D6 READ_IIN_MIN_MAX	Peak logging function for input current telemetry		Current status		RW
D7h	MFR_SPECIFIC_D7 (READ_PIN_MIN_MAX)	Peak logging function for input power telemetry		Current status		RW

Table 7-10. Supported Commands and NVM Defaults (continued)

CMD Code	Command Name	Default Behavior Ch. A (PAGE = 0)	Default Behavior Ch. B (PAGE = 1)	Default Hex[(2)] Ch. A	Default Hex[(2)] Ch. B	R/W Access, NVM
D8h	MFR_SPECIFIC_D8 (READ_POUT_MIN_MAX)	Peak logging function for ouptut power telemetry		Current status	Current status	RW
DAh	MFR_SPECIFIC_DA (READ_ALL)	Returns all telemetry data for the current channel		Current status	Current status	R
DBh	MFR_SPECIFIC_DB (STATUS_ALL)	Returns all status information for the current channel		Current status	Current status	R
DCh	MFR_SPECIFIC_DC (STATUS_PHASES)	Returns status information for phase-wise faults OCL and ISHARE		Current status		R
DDh	MFR_SPECIFIC_DD (STATUS_EXTENDED)	Returns status information for Manufacturer specific bits		Current status		R
E3h	MFR_SPECIFIC_E3 (VR_FAULT_CONFIG)	VR_FAULT# asserts only due to faults on channel A. OC and OT fault assert VR_FAULT#		00 0Eh		RW, NVM
E4h	MFR_SPECIFIC_E4 (SYNC_CONFIG)	Closed loop frequency enabled for both channels		00 12 0A 0A 00 00h		
EDh	MFR_SPECIFIC_ED (MISC_OPTIONS)	FCCM mode, both channels, PEC not required.		10 00 00 60 00h		RW, NVM
EEh	MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE)	Pin detect enabled for ADDR_CONFIG and VBOOT_CHA		13h		RW, NVM
EFh	MFR_SPECIFIC_EF (SLAVE_ADDRESS)	00h Given by pin-detection by default		00h		RW, NVM
F0h	MFR_SPECIFIC_F0 (NVM_CHECKSUM)	CRC of NVM data bytes		Curren status		R
F5h	MFR_SPECIFIC_F5 (USER_NVM_INDEX)	Index = 0 (auto-incrementing)		Default Settings		RW
F6h	MFR_SPECIFIC_F6 (USER_NVM_EXECUTE)	Raw NVM data bytes		Default Settings		RW, NVM
FAh	MFR_SPECIFIC_FA (NVM_LOCK)	NVM unlocked		00 00h		RW, NVM
FBh	MFR_SPECIFIC_FB (MFR_WRITE_PROTECT)	No command groups write protected		00 00h		RW, NVM

(1) Tracking OV, UV offset value only is stored in NVM. Hex value is calculated based on VOUT_COMMAND in the ULINEAR16 format. By default VOUT_COMMAND is restored based on pin detection, so the hex value of these commands differ from this table based on the VBOOT_CHA pinstrap detection results.
(2) Block commands are documented LSB ... MSB, as displayed in *Fusion Digital Power Designer*.

7.9.5 PMBus Command Descriptions

7.9.5.1 (00h) PAGE

Address:	00h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	FFh
Updates Allowed:	On-the-fly
Supported Values:	00h: Channel A 01h: Channel B FFh: Both channels
Description:	Selects which channel future PMBus commands address, in multi-channel devices.

7.9.5.2 (01h) OPERATION

Address:	01h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	00h
Updates Allowed:	On-the-fly
Supported Values:	00h: Immediate Off, Margin None 40h: Soft-Off, Margin None 80h: On, Margin None 98h: On, Margin Low, Act on Faults A8h: On, Margin High, Act on Faults 94h: On, Margin Low, Ignore Faults A4h: On, Margin High, Ignore Faults Other possible values not shown. See the *Technical Reference Manual*
Description:	The OPERATION command is used to enable or disable power conversion, in conjunction input from the enable pins, according to the configuration of the ON_OFF_CONFIG command.

7.9.5.3 (02h) ON_OFF_CONFIG

Address:	02h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	03h: Always converting when power is present 16h: VR_EN pin only, Active High, Soft-Off 17h: VR_EN pin only, Active High, Immediate Off 1Bh: OPERATION command only Other possible values not shown. See the *Technical Reference Manual*
Description:	The ON_OFF_CONFIG command configures the combination of enable pin input and serial bus commands needed to enable/disable power conversion.

7.9.5.4 (03h) CLEAR_FAULTS

Address:	03h
Transaction Type:	Send Byte
Data Format:	Data-less
Paged / Phased:	Yes / No
Reset Value:	N/A
Updates Allowed:	On-the-fly
Supported Values:	N/A
Description:	CLEAR_FAULTS is used to clear any fault bits that have been set. This command simultaneously clears all bits in all status registers in the selected PAGE. At the same time, the device releases its SMB_ALERT# signal output, if SMB_ALERT# is asserted. CLEAR_FAULTS is a write-only command with no data.

7.9.5.5 (04h) PHASE

Address:	04h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	FFh
Updates Allowed:	On-the-fly
Supported Values:	FFh: Address all phases in the current PAGE 00h to 0Bh: Address individual phases. For example, 00h addresses Phase 1 (Order 0), and so on.
Description:	Selects which phase future PMBus commands address within the active PAGE.

7.9.5.6 (05h) PAGE_PLUS_WRITE

Address:	05h
Transaction Type:	Block Write
Data Format:	Unsigned Binary (variable block length)
Paged / Phased:	No
Reset Value:	N/A
Updates Allowed:	On-the-fly
Supported Values:	Per command description.
Description:	Utility to send PAGE along with a PMBus command write. See the *Technical Reference Manual* for more information.

7.9.5.7 (06h) PAGE_PLUS_READ

Address:	06h
Transaction Type:	Block-Write-Block-Read Process Call
Data Format:	Unsigned Binary (variable block size)
Paged / Phased:	No / No
Reset Value:	N/A
Updates Allowed:	On-the-fly
Supported Values:	Per command description.
Description:	Utility to send a PAGE and a PMBus read in the same transaction. See the *Technical Reference Manual* for more information.

7.9.5.8 (10h) WRITE_PROTECT

Address:	10h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Write protection disabled (all writeable commands are accessible) 20h: Disable writes to all commands except WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND. 40h: Disable writes to all commands except WRITE_PROTECT, OPERATION and PAGE 80h: Disable writes to all commands except WRITE_PROTECT
Description:	The WRITE_PROTECT command controls which commands are writeable by the PMBus host.

7.9.5.9 (15h) STORE_USER_ALL

Address:	15h
Transaction Type:	Send Byte
Data Format:	Data-less
Paged / Phased:	No / No
Reset Value:	N/A
Updates Allowed:	Not recommended for on-the-fly-use, but not explicitly blocked
Supported Values:	N/A
Description:	The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store memory.

7.9.5.10 (16h) RESTORE_USER_ALL

Address:	16h
Transaction Type:	Send Byte / N/A
Data Format:	Data-less
Paged / Phased:	No / No
Reset Value:	N/A
Updates Allowed:	Blocked During Regulation
Supported Values:	N/A
Description:	The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory.

7.9.5.11 (19h) CAPABILITY

Address:	19h
Transaction Type:	Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	D0h
Updates Allowed:	N/A
Supported Values:	D0h: PEC, 1MHz, SMB_ALERT, Supported, Linear format.
Description:	This command provides a way for the host to determine the capabilities of this PMBus device.

7.9.5.12 (1Bh) SMBALERT_MASK_WORD

Address:	1Bh (with CMD byte = 79h)
Transaction Type:	Write Word / Block-Write-Block-Read Process Call
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	One mask bit for each supported status bit
Description:	SMBALERT_MASK bits for the STATUS_WORD (upper byte of STATUS_BYTE) command.

7.9.5.13 (1Bh) SMBALERT_MASK_VOUT

Address:	1Bh (with CMD byte = 7Ah)
Transaction Type:	Write Word / Block-Write-Block-Read Process Call
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	One mask bit for each supported status bit
Description:	SMBALERT_MASK bits for the STATUS_VOUT command.

7.9.5.14 (1Bh) SMBALERT_MASK_IOUT

Address:	1Bh (with CMD byte = 7Bh)
Transaction Type:	Write Word / Block-Write-Block-Read Process Call
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	One mask bit for each supported status bit
Description:	SMBALERT_MASK bits for the STATUS_IOUT command.

7.9.5.15 (1Bh) SMBALERT_MASK_INPUT

Address:	1Bh (with CMD byte = 7Ch)
Transaction Type:	Write Word / Block-Write-Block-Read Process Call
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	One mask bit for each supported status bit
Description:	SMBALERT_MASK bits for the STATUS_INPUT command.

7.9.5.16 (1Bh) SMBALERT_MASK_TEMPERATURE

Address:	1Bh (with CMD byte = 7Dh)
Transaction Type:	Write Word / Block-Write-Block-Read Process Call
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	One mask bit for each supported status bit
Description:	SMBALERT_MASK bits for the STATUS_TEMPERATURE command.

7.9.5.17 (1Bh) SMBALERT_MASK_CML

Address:	1Bh (with CMD byte = 7Eh)
Transaction Type:	Write Word / Block-Write-Block-Read Process Call
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	One mask bit for each supported status bit
Description:	SMBALERT_MASK bits for the STATUS_CML command.

7.9.5.18 (1Bh) SMBALERT_MASK_MFR

Address:	1Bh (with CMD byte = 80h)
Transaction Type:	Write Word / Block-Write-Block-Read Process Call
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	One mask bit for each supported status bit
Description:	SMBALERT_MASK bits for the STATUS_MFR command.

7.9.5.19 (20h) VOUT_MODE

Address:	20h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	Blocked during regulation
Supported Values:	16h: Linear Mode, Absolute, Exponent = -10
Description:	Specifies the data format for all output voltage related commands.

7.9.5.20 (21h) VOUT_COMMAND

Address:	21h
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	Channel A: NVM or Pinstrap depending on the setting of PIN_DETECT_OVERRIDE for VBOOT_CHA Channel B: NVM only.
Updates Allowed:	on-the-fly
Supported Values:	0.000 to 1.87 V, VOUT_MAX ≤ 1.870 V 0.000 to 3.740 V, 1.870 < VOUT_MAX ≤ 3.740 V 0.000 to 5.500 V, VOUT_MAX > 3.74 V LSB = 2^N per VOUT_MODE
Description:	Updates the output voltage target for the controller when the OPERATION command is set to "Margin None."

7.9.5.21 (22h) VOUT_TRIM

Address:	22h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR16 (N = -10)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	on-the-fly
Supported Values:	-125 mV to +124 mV LSB = 2^N per VOUT_MODE
Description:	Used to apply a fixed offset voltage to the output voltage command value.

7.9.5.22 (24h) VOUT_MAX

Address:	24h
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	NVM If VBOOT pinstrapping is used, VOUT_MAX is initialized to 1.87 V, or 5.5 V based on the selected option.
Updates Allowed:	On-the-fly
Supported Values:	0.000 V to 5.500 V LSB = 2^N per VOUT_MODE
Description:	Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations.

7.9.5.23 (25h) VOUT_MARGIN_HIGH

Address:	25h
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	0.000 V
Updates Allowed:	On-the-fly
Supported Values:	Same as VOUT_COMMAND. LSB = 2^N per VOUT_MODE
Description:	Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High."

7.9.5.24 (26h) VOUT_MARGIN_LOW

Address:	26h
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	0.000 V
Updates Allowed:	On-the-fly
Supported Values:	Same as VOUT_COMMAND. LSB = 2^N per VOUT_MODE
Description:	Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin Low."

7.9.5.25 (27h) VOUT_TRANSITION_RATE

Address:	27h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -4)
Paged / Phased:	Yes / No
Reset Value:	Yes
Updates Allowed:	On-the-fly
Supported Values:	0.3125 to 40 mV/µs See the *Technical Reference Manual* for all supported values.
Description:	Sets the slew rate at which any output voltage changes during normal power conversion occur.

7.9.5.26 (28h) VOUT_DROOP

Address:	28h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -7)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0.0 to 1.0 mΩ with 7.8125 µΩ resolution 1.0 to 2.0 mΩ with 15.625 µΩ resolution 2.0 to 4.0 mΩ with 31.25 µΩ resolution 4.0 to 8.0 mΩ with 62.50 µΩ resolution
Description:	Sets the rate, in mV/A (mΩ) at which the output voltage decreases with increasing output current for use with adaptive voltage positioning. Also referred to as the DC Load Line (DCLL).

7.9.5.27 (29h) VOUT_SCALE_LOOP

Address:	29h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -3)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	Blocked during regulation
Supported Values:	1.000 0.500 (Recommended for output voltages greater than 3.74 V)
Description:	Sets the scaling factor between the output voltage and the input voltage to the controller VSP, VSN pins.

7.9.5.28 (2Bh) VOUT_MIN

Address:	2Bh
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	NVM Initialized to 0.00 V when VBOOT pinstrap is used.
Updates Allowed:	On-the-fly
Supported Values:	0.000 to 5.500 V LSB = 2^N per VOUT_MODE
Description:	Sets a lower limit on the output voltage the unit can command regardless of any other commands or combinations.

7.9.5.29 (33h) FREQUENCY_SWITCH

Address:	33h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = 0)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	300 to 2000 kHz, 50 kHz steps to 1800 kHz, 100 kHz steps after.
Description:	Sets the per-phase switching frequency for the controller.

7.9.5.30 (34h) POWER_MODE

Address:	34h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	00h or 03h depending if dynamic phase shedding is enabled
Updates Allowed:	On-the-fly
Supported Values:	00h: DPS enabled, Auto-DCM allowed on all phases 03h: DPS disabled, all phases FCCM 04h: DPS enabled, Auto-DCM allowd in 1 phase mode only
Description:	Change the power stage of the converter on-the-fly.

7.9.5.31 (35h) VIN_ON

Address:	35h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -2)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	4.25 to 11.50 V, in 0.25 V steps
Description:	Sets the value of the input voltage, in Volts, at which the unit starts power conversion.

7.9.5.32 (38h) IOUT_CAL_GAIN

Address:	38h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -7)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	4.500 to 5.493 mΩ in 7.8125 µΩ steps
Description:	Sets the ratio of the voltage at the current sense pins to the sensed current for the READ_IOUT command in miliohms.

7.9.5.33 (39h) IOUT_CAL_OFFSET

Address:	39h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -3)
Paged / Phased:	Yes / Yes
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	-4.000 to +3.750 A in 125 mA steps
Description:	Used to compensate for offset errors in the power stage for each individual phase, in amperes.

7.9.5.34 (40h) VOUT_OV_FAULT_LIMIT

Address:	40h
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	(VOUT_COMMAND + 32 mV) to (VOUT_COMMAND + 448 mV) in 32 mV steps LSB = 2^N per VOUT_MODE
Description:	Sets the value of the tracking overvoltage fault limit. Refer to MFR_PROTECTION_CONFIG to set the fixed overvoltage fault limit.

7.9.5.35 (41h) VOUT_OV_FAULT_RESPONSE

Address:	41h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Ignore 80h: Latch-Off immediately, require enable cycle to recover B8h: Hiccup immediately, infinite retrials, shutdown and restart after wait time.
Description:	Instructs the device on what action to take in response to an output overvoltage fault.

7.9.5.36 (42h) VOUT_OV_WARN_LIMIT

Address:	42h
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	(VOUT_COMMAND + 24 mV) to (VOUT_COMMAND + 448 mV) in 8 mV steps LSB = 2^N per VOUT_MODE
Description:	Sets the value of the output voltage at the sense or output pins that causes an output voltage high warning.

7.9.5.37 (43h) VOUT_UV_WARN_LIMIT

Address:	43h
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	(VOUT_COMMAND - 24 mV) to (VOUT_COMMAND - 448 mV) in 8 mV steps LSB = 2^N per VOUT_MODE
Description:	Sets the value of the output voltage at the sense or output pins that causes an output voltage low warning.

7.9.5.38 (44h) VOUT_UV_FAULT_LIMIT

Address:	44h
Transaction Type:	Write Word / Read Word
Data Format:	ULINEAR16 per VOUT_MODE
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	(VOUT_COMMAND - 32 mV) to (VOUT_COMMAND - 448 mV) in 32 mV steps LSB = 2^N per VOUT_MODE
Description:	Sets the value of the tracking undervoltage fault limit.

7.9.5.39 (45h) VOUT_UV_FAULT_RESPONSE

Address:	45h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Ignore 80h: Latch-off immediately, require enable cycle to recover. B8h: Hiccup immediately, infinite retrials, shutdown and restart after wait time. Other combinations are possible. See the *Techinical Reference Manual*.
Description:	Instructs the device on what action to take in response to an output undervoltage fault.

7.9.5.40 (46h) IOUT_OC_FAULT_LIMIT

Address:	46h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = 0)
Paged / Phased:	Yes / Yes
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0 to 1023 A per-page OCP in 1 A steps 17 A to 130 A per-phase OCL (shared among all phases) in 3 A steps to 80 A, 5 A steps after
Description:	Sets the total page overcurrent protection threshold in amperes when written with PHASE = FFh. Sets the per-phase overcurrent limit in amperes when written with PHASE ≠ FFh

7.9.5.41 (47h) IOUT_OC_FAULT_RESPONSE

Address:	47h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Ignore C0h: Latch-off immediately, require enable cycle to recover. F8h: Hiccup immediately, infinite retrials, shutdown and restart after wait time.
Description:	Instructs the device on what action to take in response to an output overcurrent fault.

7.9.5.42 (4Ah) IOUT_OC_WARN_LIMIT

Address:	4Ah
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = 0)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0 to 1023 A in 1 A steps
Description:	Sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning condition.

7.9.5.43 (4Fh) OT_FAULT_LIMIT

Address:	4Fh
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = 0)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	90°C to 160°C in 10°C steps
Description:	Sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition.

7.9.5.44 (50h) OT_FAULT_RESPONSE

Address:	50h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Ignore 80h: Latch-off immediately, require enable cycle to recover B8h: Hiccup immediately, infinite retrials, shutdown and restart after wait time. F8h: Hysteresis. Shutdown immediately and restart when the temperature falls.
Description:	Instructs the device on what action to take in response to an Over temperature Fault.

7.9.5.45 (51h) OT_WARN_LIMIT

Address:	51h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = 0)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	90°C to 160°C in 10°C steps
Description:	Sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature warning.

7.9.5.46 (55h) VIN_OV_FAULT_LIMIT

Address:	55h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = 0)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0.00 to 19.00 V in 1.0 V steps
Description:	Sets the value, in Volts, of the input voltage that causes an input overvoltage fault.

7.9.5.47 (56h) VIN_OV_FAULT_RESPONSE

Address:	56h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Ignore 80h: Latch-off immediately, require enable cycle to recover B8h: Hiccup immediately, infinite retrials, shutdown and restart after wait time.
Description:	Instructs the device on what action to take in response to an input overvoltage fault.

7.9.5.48 (57h) VIN_OV_WARN_LIMIT

Address:	57h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = 0)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0.00 to 19.00 V in 1.0 V steps
Description:	Sets the value, in Volts, of the input voltage that causes an input overvoltage warning.

7.9.5.49 (58h) VIN_UV_WARN_LIMIT

Address:	58h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -2)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	4.00 to 11.25 V in 0.25 V steps
Description:	Sets the value, in Volts, of the input voltage that causes an input undervoltage warning.

7.9.5.50 (59h) VIN_UV_FAULT_LIMIT

Address:	59h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -2)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	4.00 to 11.25 V in 0.25 V steps
Description:	Sets the value, in Volts, of the input voltage that causes an input undervoltage fault.

7.9.5.51 (5Ah) VIN_UV_FAULT_RESPONSE

Address:	5Ah
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Ignore 80h: Latch-off immediately, require enable cycle to recover B8h: Hiccup immediately, infinite retrials, shutdown and restart after wait time.
Description:	Instructs the device on what action to take in response to an input under-voltage fault.

7.9.5.52 (5Bh) IIN_OC_FAULT_LIMIT

Address:	5Bh
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = 0)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	4.0 to 128.0 A in 4 A steps
Description:	Sets the value of the input current, in Amperes, that causes an Input Overcurrent Fault.

7.9.5.53 (5Ch) IIN_OC_FAULT_RESPONSE

Address:	5Ch
Transaction Type:	Write Word / Read Word
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Ignore C0h: Latch-off immediately, require enable cycle to recover F8h: Hiccup immediately, infinite retrials, shutdown and restart after wait time
Description:	Instructs the device on what action to take in response to an input overcurrent fault.

7.9.5.54 (5Dh) IIN_OC_WARN_LIMIT

Address:	5Dh
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11(N = 0)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	4.0 to 128.0 A in 4 A steps
Description:	Sets the value of the input current, in Amperes, that causes an Input Overcurrent warning.

7.9.5.55 (60h) TON_DELAY

Address:	60h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -1)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0.0 to 127.5 ms in 0.5 ms steps
Description:	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.

7.9.5.56 (61h) TON_RISE

Address:	61h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -2)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0.00 to 31.75 ms in 0.25 ms steps This value used to calculate *slew rate* during boot only. Supported slew rates follow those of VOUT_TRANSITION_RATE.
Description:	Sets the desired rise time of the output voltage, which allows the device to calculate the slew rate setting during bootup.

7.9.5.57 (62h) TON_MAX_FAULT_LIMIT

Address:	62h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -2)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0.00 ms: function disabled. 0.00 to 31.75 ms in 0.25 ms steps
Description:	Sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the undervoltage fault limit (including droop).

7.9.5.58 (63h) TON_MAX_FAULT_RESPONSE

Address:	63h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	00h: Ignore 80h: Latch-off immediately, require enable cycle to recover B8h: Hiccup immediately, infinite retrials, shutdown and restart after wait time
Description:	Instructs the device on what action to take in response to TON_MAX fault.

7.9.5.59 (64h) TOFF_DELAY

Address:	64h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -1)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0.0 to 127.5 ms in 0.5 ms steps
Description:	Sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output.

7.9.5.60 (65h) TOFF_FALL

Address:	65h
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = -2)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0.00 to 31.75 ms in 0.25 ms steps This value used to calculate *slew rate* during soft-off only. Supported slew rates follow those of VOUT_TRANSITION_RATE.
Description:	Sets the desired fall time of the output voltage, which allows the device to calculate the slew rate setting during soft-off.

7.9.5.61 (6Bh) PIN_OP_WARN_LIMIT

Address:	6Bh
Transaction Type:	Write Word / Read Word
Data Format:	SLINEAR11 (N = +1)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	8.0 to 2048 W Non-uniform step size. See the *Technical Reference Manual*.
Description:	Sets the value of the input power, in watts, that causes a warning that the input power is high.

7.9.5.62 (78h) STATUS_BYTE

Address:	78h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	BUSY, OFF, VOUT_OV, IOUT_OC, VIN_UV, TEMP CML, OTHER
Description:	Returns one byte of information with a summary of the most critical faults.

7.9.5.63 (79h) STATUS_WORD

Address:	79h
Transaction Type:	Write Word / Read Word
Data Format:	Unsigned Binary (2 bytes)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	VOUT, IOUT, INPUT, MFR, PGOOD, plus the STATUS_BYTE
Description:	Returns two bytes of information with a summary of the most critical faults.

7.9.5.64 (7Ah) STATUS_VOUT

Address:	7Ah
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	VOUT_OVF, VOUT_OVW, VOUT_UVW, VOUT_UVF, VOUT_MINMAX, TON_MAX
Description:	Returns one data byte with information about output voltage related faults and warnings.

7.9.5.65 (7Bh) STATUS_IOUT

Address:	7Bh
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	IOUT_OCF, IOUT_OCW, CUR_SHAREF
Description:	Returns one data byte with information about output current related faults and warnings.

7.9.5.66 (7Ch) STATUS_INPUT

Address:	7Ch
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	VIN_OVF, VIN_OVW, VIN_UVW, VIN_UVF, LOW_VIN, IIN_OCF, IIN_OCW, PIN_OPW
Description:	Returns one data byte with information about input voltage/current related faults and warnings.

7.9.5.67 (7Dh) STATUS_TEMPERATURE

Address:	7Dh
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	OTF, OTW
Description:	Returns one data byte with information about temperature related faults and warnings.

7.9.5.68 (7Eh) STATUS_CML

Address:	7Eh
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	IVC, IVD, PEC, MEM, COMM, CML_OTHER
Description:	Returns one data byte with information about communication related warnings.

7.9.5.69 (7Fh) STATUS_OTHER

Address:	7Eh
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	FIRST_TO_ALERT
Description:	Returns one data byte with information about warnings not defined in the other standard status registers.

7.9.5.70 (80h) STATUS_MFR_SPECIFIC

Address:	80h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Updates Allowed:	On-the-fly
Supported Bits:	POR, EXT, PSFLT
Description:	Returns one data byte with information about manufacturer-defined warnings and faults.

7.9.5.71 (88h) READ_VIN

Address:	88h
Transaction Type:	Read Word
Data Format:	SLINEAR11 (variable exponent)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	150 µs update / 300 µs time filtering
Supported Range:	0.000 V to 18.700 V
Description:	Returns the sensed input voltage in volts.

7.9.5.72 (89h) READ_IIN

Address:	89h
Transaction Type:	Read Word
Data Format:	SLINEAR11 (variable exponent)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	16 µs update / 120 µs time filtering
Supported Range:	-5.0 to 100.0 A $(V_{CSPIN}\text{-}V_{VIN\_CSN})\times G_{IINSHUNT}$ = 800 mV max
Description:	Returns the sensed input current in amperes.

7.9.5.73 (8Bh) READ_VOUT

Address:	8Bh
Transaction Type:	Read Word
Data Format:	ULINEAR16
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	200 µs update / 250 µs time filtering
Supported Range:	0.00 to 3.74 V (VOUT_SCALE_LOOP = 1.0) 0.00 to 6.00 V (VOUT_SCALE_LOOP = 0.5)
Description:	Returns the sensed output voltage in volts.

7.9.5.74 (8Ch) READ_IOUT

Address:	8Ch
Transaction Type:	Read Word
Data Format:	SLINEAR11 (variable exponent)
Paged / Phased:	Yes / Yes
Reset Value:	Current Status
Update Rate:	16 µs update / 80 µs time filtering
Supported Range:	Per Channel: $(-10.0 \text{ to } +70.0\ A) \times N_{phases} \times (5.0\ m\Omega\ /\ IOUT\_CAL\_GAIN) + \Sigma(IOUT\_CAL\_OFFSET)_{Phases}$ Per Phase: $(-10.0 \text{ to } +70.0\ A) \times (5.0\ m\Omega\ /\ IOUT\_CAL\_GAIN) + (IOUT\_CAL\_OFFSET)_{Phases}$
Description:	Returns the sensed output current in amperes. Can be calibrated by IOUT_CAL_GAIN and IOUT_CAL_OFFSET. Read with PHASE = FFh to read total page current. Read with PHASE = 00h to read first phase (order 0) current, and so on.

7.9.5.75 (8Dh) READ_TEMPERATURE_1

Address:	8Dh
Transaction Type:	Read Word
Data Format:	SLINEAR11 (variable exponent)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	TBD
Supported Range:	-40.0°C to 150.0°C
Description:	Returns the sensed power stage temperature in degrees Celsius.

7.9.5.76 (96h) READ_POUT

Address:	96h
Transaction Type:	Read Word
Data Format:	SLINEAR11 (variable exponent)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Per READ_VOUT and READ_IOUT
Supported Range:	Per READ_VOUT and READ_IOUT
Description:	Returns the sensed output power in Watts.

7.9.5.77 (97h) READ_PIN

Address:	97h
Transaction Type:	Read Word
Data Format:	SLINEAR11 (variable exponent)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Per READ_VIN and READ_IIN
Supported Range:	Per READ_VIN and READ_IIN
Description:	Returns the sensed input power in Watts.

7.9.5.78 (98h) PMBUS_REVISION

Address:	98h
Transaction Type:	Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	33h
Updates Allowed:	N/A
Supported Values:	33h: PMBus 1.3, Part I and II
Description:	Reads the revision of the PMBus to which the device is compatible.

7.9.5.79 (99h) MFR_ID

Address:	99h
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (3 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-Fly
Supported Values:	000000h to FFFFFFh Arbitrary NVM for user tracking purposes.
Description:	3 bytes of arbitrarily writeable non-volatile memory intended for manufacturer identification.

7.9.5.80 (9Ah) MFR_MODEL

Address:	9Ah
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (3 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-Fly
Supported Values:	000000h to FFFFFFh Arbitrary NVM for user tracking purposes.
Description:	3 bytes of arbitrarily writeable non-volatile memory intended for model identification.

7.9.5.81 (9Bh) MFR_REVISION

Address:	9Bh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (3 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-Fly
Supported Values:	000000h to FFFFFFh Arbitrary NVM for user tracking purposes.
Description:	3 bytes of arbitrarily writeable non-volatile memory intended for revision identification.

7.9.5.82 (9Dh) MFR_DATE

Address:	9Dh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (3 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-Fly
Supported Values:	000000h to FFFFFFh Arbitrary NVM for user tracking purposes.
Description:	3 bytes of arbitrarily writeable non-volatile memory intended for date tracking.

7.9.5.83 (ADh) IC_DEVICE_ID

Address:	ADh
Transaction Type:	Read Block
Data Format:	Unsigned Binary (6 bytes)
Paged / Phased:	No / No
Reset Value:	5449536C7000h
Updates Allowed:	N/A
Supported Values:	5449536C7000h (TPS536C7B1)
Description:	Returns the part number of the device.

7.9.5.84 (AEh) IC_DEVICE_REV

Address:	AEh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (2 bytes)
Paged / Phased:	No / No
Reset Value:	Current Device Revision
Updates Allowed:	N/A
Supported Values:	Set by TI during device manufacturing.
Description:	Returns device revision.

7.9.5.85 (B1h) USER_DATA_01 (COMPENSATION_CONFIG)

Address:	B1h
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (8 bytes)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configures the control loop compensation parameters including AC load line, integration time constant, dynamic integration, compensating ramp, AC gain, integration gain.

7.9.5.86 (B2h) USER_DATA_02 (NONLINEAR_CONFIG)

Address:	B2h
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (5 bytes)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configures the nonlinear controller parameters including minimum on time, minimum off time, leading edge blanking time, USR and OSR thresholds.

7.9.5.87 (B3h) USER_DATA_03 (PHASE_CONFIG)

Address:	B3h
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (24 bytes)
Paged / Phased:	No / No
Reset Value:	NVM or Pinstrap
Updates Allowed:	Blocked during regulation.
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configures phase assignments: Assign phases to channels, phase number, and firing position.

7.9.5.88 (B4h) USER_DATA_04 (DVID_CONFIG)

Address:	B4h
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (6 bytes)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configures DVID options including dynamic AC and DC load lines.

7.9.5.89 (B7h) USER_DATA_07 (PHASE_SHED_CONFIG)

Address:	B7h
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (13 bytes)
Paged / Phased:	Yes / No
Reset Value:	NVM
Updates Allowed:	on-the-fly
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configures phase add/drop functionality and thresholds.

7.9.5.90 (BAh) USER_DATA_10 (ISHARE_CONFIG)

Address:	BAh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	Yes / Yes
Reset Value:	NVM
Updates Allowed:	on-the-fly
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configures the current sharing ratios for each phase for thermal balance management.

7.9.5.91 (BBh) USER_DATA_11 (MFR_PROTECTION_CONFIG)

Address:	BBh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (10 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	on-the-fly
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configures manufacturer-specific fault features such as the fixed overvoltage protection, hiccup wait time, and current share warning.

7.9.5.92 (BDh) USER_DATA_13 (MFR_CALIBRATION_CONFIG)

Address:	BDh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (15 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	on-the-fly
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configures telemetry calibration features including input current sensing gain/offset.

7.9.5.93 (CDh) MFR_SPECIFIC_CD (MULTIFUNCTION_PIN_CONFIG_1)

Address:	CDh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (32 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly (takes effect only after power on).
Supported Values:	Do not modify.
Description:	Device configuration bits which are set by TI during manufacturing. Do not change from default settings.

7.9.5.94 (CEh) MFR_SPECIFIC_CE (MULTIFUNCTION_PIN_CONFIG_2)

Address:	CEh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (31 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly (takes effect only after power on).
Supported Values:	Do not modify.
Description:	Device configuration bits which are set by TI during manufacturing. Do not change from default settings.

7.9.5.95 (CFh) SMBALERT_MASK_EXTENDED

Address:	CFh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (7 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	Refer to the *technical reference manual*.
Description:	SMBALERT MASK bits for STATUS_EXTENDED bits

7.9.5.96 (D1h) READ_VOUT_MIN_MAX

Address:	D1h
Transaction Type:	Write Block / Read Block
Data Format:	SLINEAR11 (2 MSB for min, 2 LSB for max)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Same as READ_VOUT.
Logging Control:	0000 0004h: Pause logging (min and max) 0000 0020h: Resume logging (min and max) 0000 0100h: Reset logs (min and max)
Description:	Returns maximum and minimum output voltage values logged since last reset.

7.9.5.97 (D2h) READ_IOUT_MIN_MAX

Address:	D2h
Transaction Type:	Write Block / Read Block
Data Format:	SLINEAR11 (2 MSB for min, 2 LSB for max)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Same as READ_IOUT.
Logging Control:	0000 0004h: Pause logging (min and max) 0000 0020h: Resume logging (min and max) 0000 0100h: Reset logs (min and max)
Description:	Returns maximum and minimum output current values logged since last reset.

7.9.5.98 (D3h) READ_TEMPERATURE_MIN_MAX

Address:	D3h
Transaction Type:	Write Block / Read Block
Data Format:	SLINEAR11 (2 MSB for min, 2 LSB for max)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Same as READ_TEMPERATURE_1.
Logging Control:	0000 0004h: Pause logging (min and max) 0000 0020h: Resume logging (min and max) 0000 0100h: Reset logs (min and max)
Description:	Returns maximum and minimum temperature values logged since last reset.

7.9.5.99 (D4h) READ_MFR_VOUT

Address:	D4h
Transaction Type:	Read Word
Data Format:	SLINEAR11 (variable exponent)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Per READ_VOUT.
Supported Range:	0.00 to 3.74 V (VOUT_SCALE_LOOP = 1.0) 0.00 to 6.00 V (VOUT_SCALE_LOOP = 0.5)
Description:	Returns the sensed output voltage in volts.

7.9.5.100 (D5h) READ_VIN_MIN_MAX

Address:	D5h
Transaction Type:	Write Block / Read Block
Data Format:	SLINEAR11 (2 MSB for min, 2 LSB for max)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Same as READ_VIN.
Logging Control:	0000 0004h: Pause logging (min and max) 0000 0020h: Resume logging (min and max) 0000 0100h: Reset logs (min and max)
Description:	Returns maximum and minimum input voltage values logged since last reset.

7.9.5.101 (D6h) READ_IIN_MIN_MAX

Address:	D6h
Transaction Type:	Write Block / Read Block
Data Format:	SLINEAR11 (2 MSB for min, 2 LSB for max)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Same as READ_IIN.
Logging Control:	0000 0004h: Pause logging (min and max) 0000 0020h: Resume logging (min and max) 0000 0100h: Reset logs (min and max)
Description:	Returns maximum and minimum input current values logged since last reset.

7.9.5.102 (D7h) READ_PIN_MIN_MAX

Address:	D7h
Transaction Type:	Write Block / Read Block
Data Format:	SLINEAR11 (2 MSB for min, 2 LSB for max)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Same as READ_PIN.
Logging Control:	0000 0004h: Pause logging (min and max) 0000 0020h: Resume logging (min and max) 0000 0100h: Reset logs (min and max)
Description:	Returns maximum and minimum input power values logged since last reset.

7.9.5.103 (D8h) READ_POUT_MIN_MAX

Address:	D8h
Transaction Type:	Write Block / Read Block
Data Format:	SLINEAR11 (2 MSB for min, 2 LSB for max)
Paged / Phased:	Yes / No
Reset Value:	Current Status
Update Rate:	Same as READ_POUT.
Logging Control:	0000 0004h: Pause logging (min and max) 0000 0020h: Resume logging (min and max) 0000 0100h: Reset logs (min and max)
Description:	Returns maximum and minimum output power values logged since last reset.

7.9.5.104 (DAh) READ_ALL

Address:	DAh
Transaction Type:	Read Block
Data Format:	Unsigned Binary (14 bytes)
Paged / Phased:	Yes / No
Reset Value:	0d
Updates Allowed:	On-the-fly
Supported Values:	Refer to the *technical reference manual*.
Description:	Read all supported telemetry values in a single block to reduce bus utilization.

7.9.5.105 (DBh) STATUS_ALL

Address:	DBh
Transaction Type:	Read Block
Data Format:	Unsigned Binary (18 bytes)
Paged / Phased:	Yes / No
Reset Value:	0d
Updates Allowed:	On-the-fly
Supported Values:	Refer to the *technical reference manual*.
Description:	Read all supported status registers in a single block to reduce bus utilization.

7.9.5.106 (DCh) STATUS_PHASES

Address:	DCh
Transaction Type:	Write Word / Read Word
Data Format:	Unsigned Binary (2 bytes)
Paged / Phased:	Yes / Yes
Reset Value:	0d
Updates Allowed:	On-the-fly
Supported Values:	Refer to the *technical reference manual*.
Description:	Identify which phases have experienced a phased fault.

7.9.5.107 (DDh) STATUS_EXTENDED

Address:	DDh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (7 bytes)
Paged / Phased:	Yes / Yes
Reset Value:	0d
Updates Allowed:	On-the-fly
Supported Values:	Refer to the *technical reference manual*.
Description:	Report non-standard status information which is not captured in STATUS_X registers or STATUS_PHASES.

7.9.5.108 (E3h) MFR_SPECIFIC_E3 (VR_FAULT_CONFIG)

Address:	E3h
Transaction Type:	Write Word / Read Word
Data Format:	Unsigned Binary (2 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	on-the-fly
Supported Values:	Bit 0: Set to 1b to assert VR_FAULT# for channels A and B, 0 channel A only otherwise Bit 1: Set to 1b to assert VRFAULT# for overcurrent faults, 0 otherwise Bit 2: Set to 1b to assert VRFAULT# for overtemperature faults, 0 otherwise
Description:	Configure the behavior of the VR_FAULT# pin.

7.9.5.109 (E4h) SYNC_CONFIG

Address:	E4h
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (6 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	Blocked during regulation.
Supported Values:	Refer to the *technical reference manual*.
Description:	Configure phase synchronization and frequency control.

7.9.5.110 (EDh) MFR_SPECIFIC_ED (MISC_OPTIONS)

Address:	EDh
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (5 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	on-the-fly
Supported Values:	See the *Technical Reference Manual* for a complete register map.
Description:	Configure miscellaneous options.

7.9.5.111 (EEh) MFR_SPECIFIC_EE (PIN_DETECT_OVERRIDE)

Address:	EEh
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 byte)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	on-the-fly (pin detection occurs on POR only).
Supported Values:	Set bit 0 to 0b to derive channel A VBOOT from NVM Set bit 1 to 0b to derive PMBus address from NVM. Set bit 4 to 0b to derive phase configuration from NVM.
Description:	Configure whether the device follows pinstrapping or NVM settings for the parameters associated with the VBOOT_CHA and ADDR_CONFIG pins.

7.9.5.112 (EFh) MFR_SPECIFIC_EF (SLAVE_ADDRESS)

Address:	EFh
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 bytes)
Paged / Phased:	No / No
Reset Value:	NVM or Pinstrap
Updates Allowed:	on-the-fly, only takes effect at power-on.
Supported Values:	00h to 7Fh (7 bit address right justified)
Description:	Configure the PMBus slave address, when the PIN_DETECT_OVERRIDE command is configured to ignore the ADDR_CONFIG pinstrap detection.

7.9.5.113 (F0h) MFR_SPECIFIC_F0 (NVM_CHECKSUM)

Address:	F0h
Transaction Type:	Read Word
Data Format:	Unsigned Binary (2 bytes)
Paged / Phased:	No / No
Reset Value:	Current Status
Updates Allowed:	Only following NVM Store/Restore Operations
Supported Values:	0000h to FFFFh
Description:	CRC16 of the internal NVM array. This can be used to verify proper NVM programming.

7.9.5.114 (F5h) MFR_SPECIFIC_F5 (USER_NVM_INDEX)

Address:	F5h
Transaction Type:	Write Byte / Read Byte
Data Format:	Unsigned Binary (1 bytes)
Paged / Phased:	No / No
Reset Value:	00h
Updates Allowed:	On-the-fly (Auto-increments with USER_NVM_EXECUTE access)
Supported Values:	00h to 08h
Description:	Used for batch-loading of NVM data via PMBus.

7.9.5.115 (F6h) MFR_SPECIFIC_F6 (USER_NVM_EXECUTE)

Address:	F6h
Transaction Type:	Write Block / Read Block
Data Format:	Unsigned Binary (32 bytes)
Paged / Phased:	No / No
Reset Value:	Current NVM status
Updates Allowed:	On-the-fly
Supported Values:	All NVM bytes
Description:	With USER_NVM_INDEX = 0, this command writes/returns 9 bytes of identifying information, plus the first 23 bytes of NVM data With USER_NVM_INDEX = 1 to 7, this command writes/returns the next 32 bytes of NVM data With USER_NVM_INDEX = 8, this command writes the last NVM data bytes, and automatically performs an NVM Store operation. Each time this command is accessed, USER_NVM_INDEX increments automatically.

7.9.5.116 (FAh) NVM_LOCK

Address:	FAh
Transaction Type:	Write Word / Read Word (when locked, this command does not read back the password value).
Data Format:	Unsigned Binary (2 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	0000-FFFEh
Description:	NVM password. Used to lock or unlock WRITE_PROTECT and MFR_WRITE_PROTECT commands, which in turn provide write protection.

7.9.5.117 (FBh) MFR_SPECIFIC_WRITE_PROTECT

Address:	FBh
Transaction Type:	Write Word / Read Word
Data Format:	Unsigned Binary (2 bytes)
Paged / Phased:	No / No
Reset Value:	NVM
Updates Allowed:	On-the-fly
Supported Values:	Refer to the *Technical Reference Manual* for a bit map
Description:	Provides additional resolution to WRITE_PROTECT, allowing different groups of commands to be write protected. Access to this command is controlled by NVM_LOCK.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Application

8.1.1 Application

The TPS536C7B1 is a fully PMbus 1.3.1 compliant step-down controller with dual channels. All programmable parameters can be configured by PMBus and stored in NVM as the new default value to minimize external component count.

This design uses a 0.88-V / 400-A, 1-V / 50-A design as an example. Use the following design procedure to select key components.

8.1.1.1 Schematic

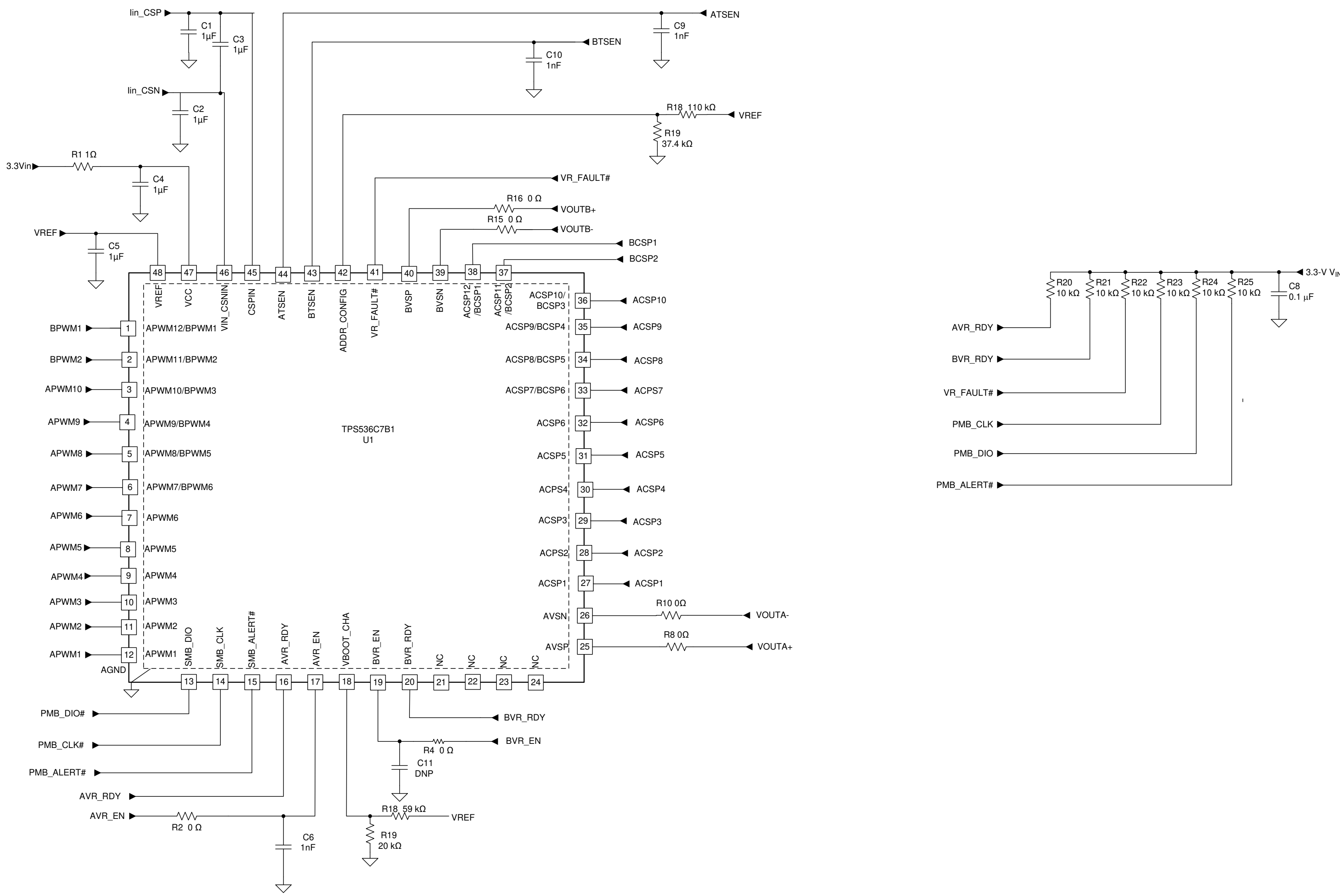


Figure 8-1. Controller Schematic

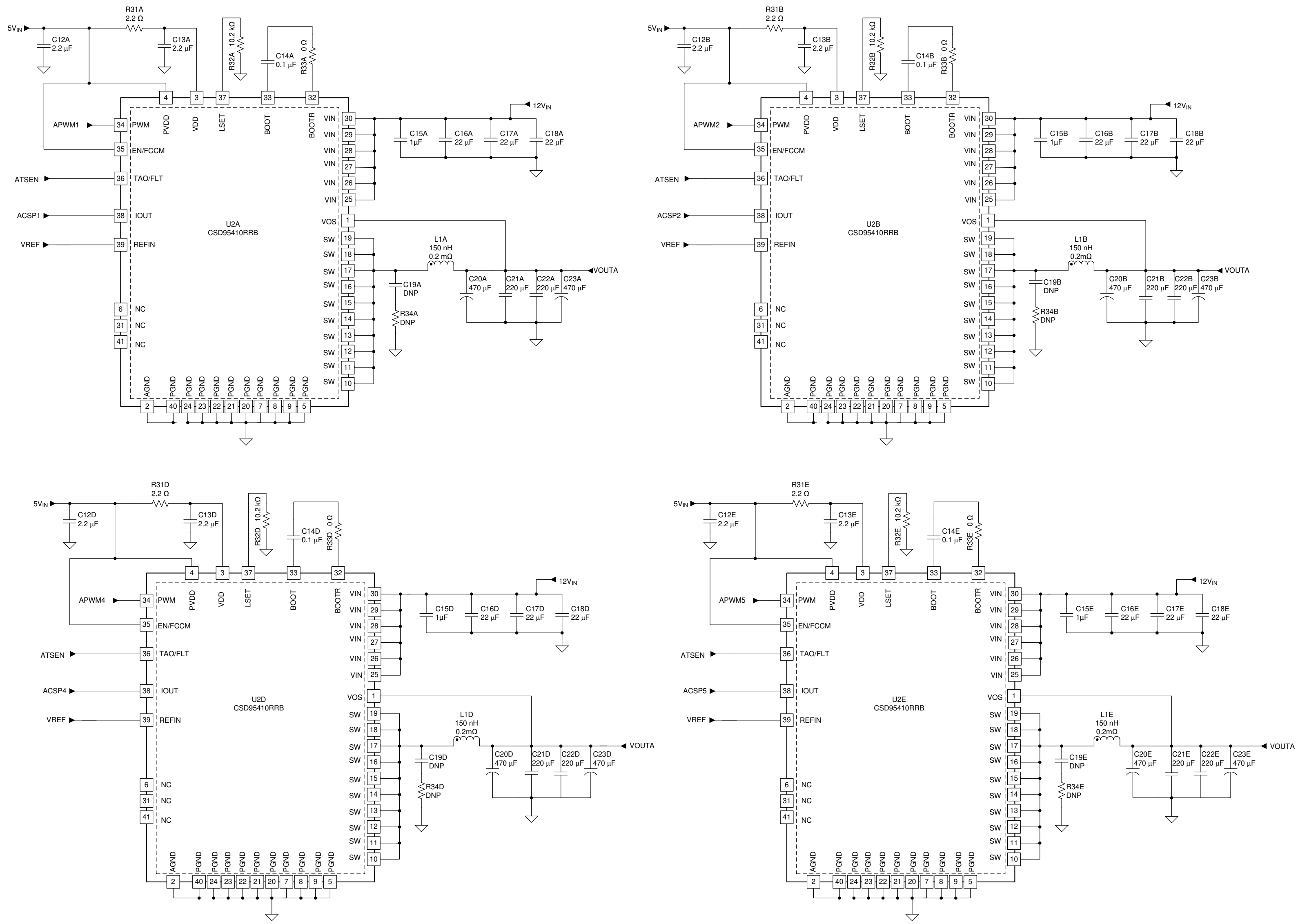


Figure 8-2. Powerstages Schematic (1/3)

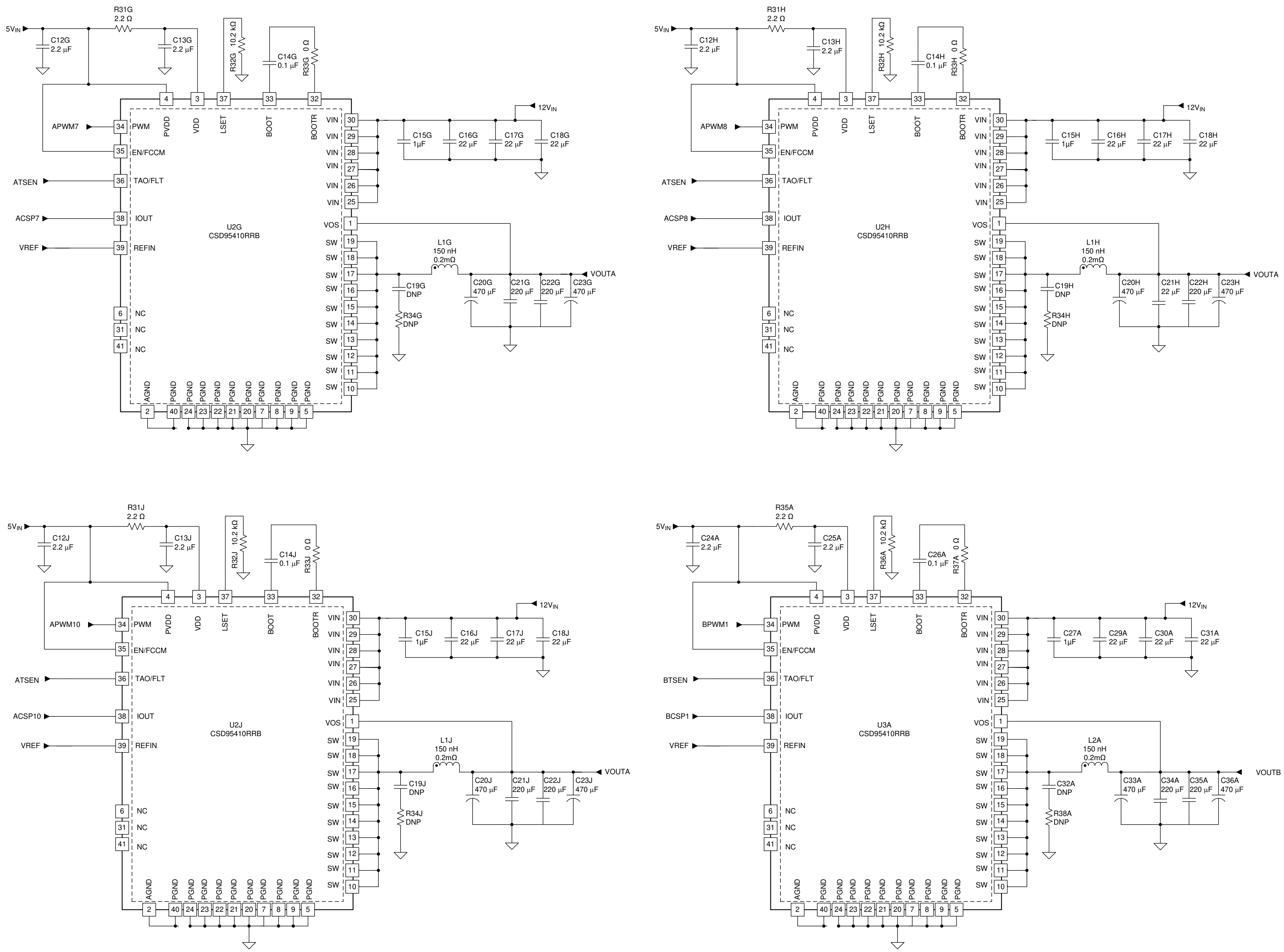


Figure 8-3. Powerstages Schematic (2/3)

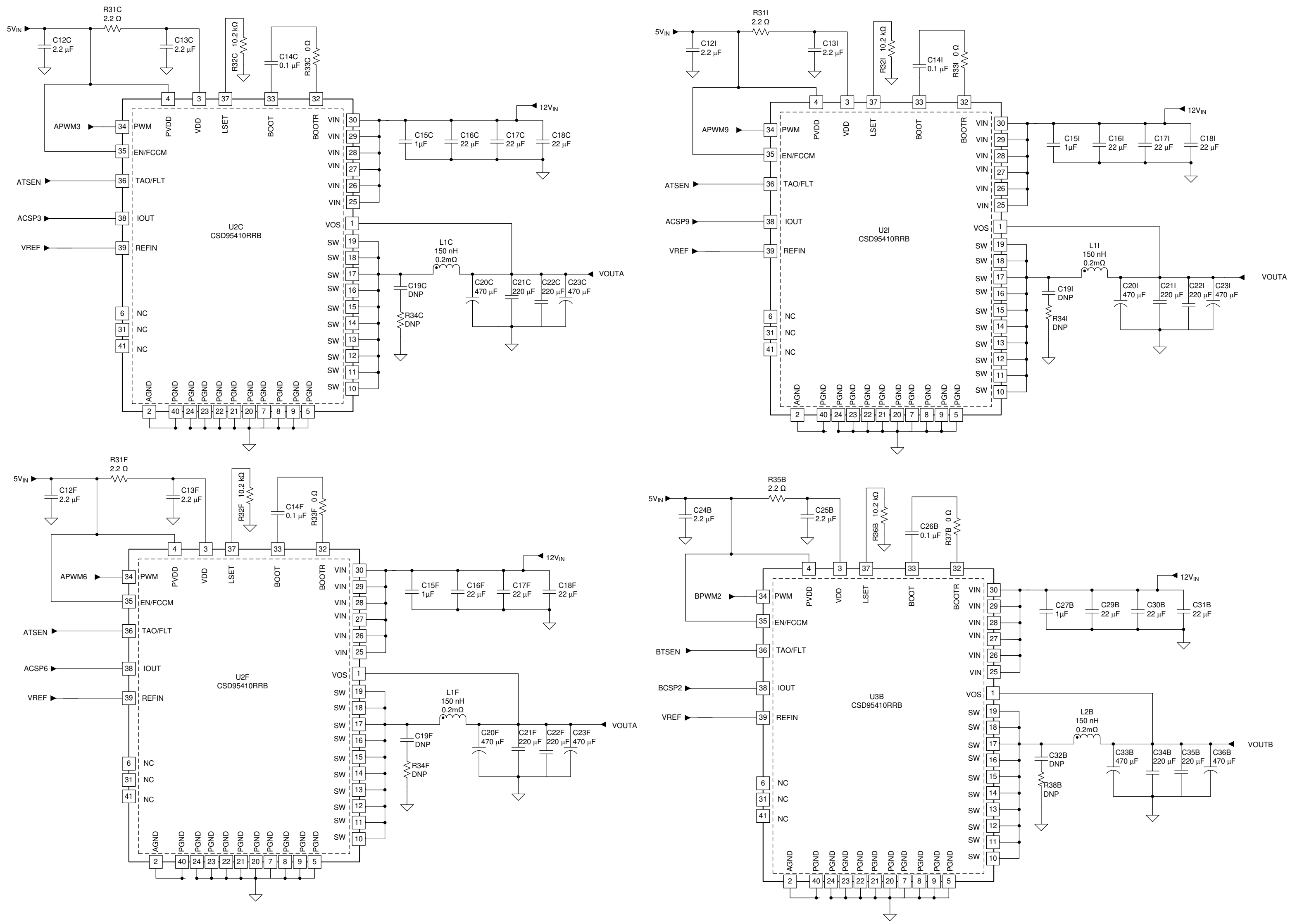


Figure 8-4. Powerstages Schematic (3/3)

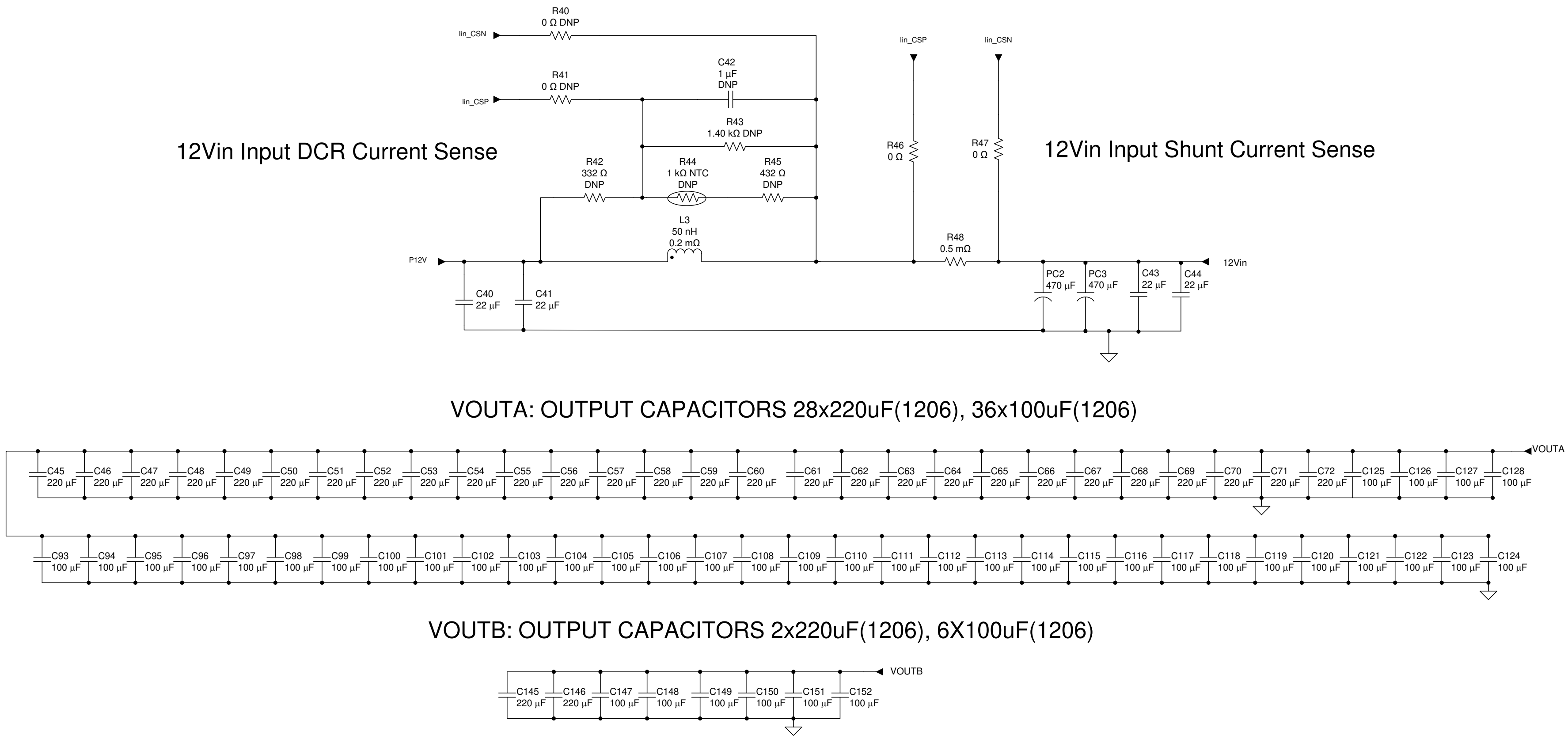


Figure 8-5. Ouptput Capacitors Schematic

8.1.1.2 Design Requirements

The key requirements for this design are summarized below.

Table 8-1. Design Parameters

SYMBOL	PARAMETER	Channel A	Channel B
N_{Φ}	Phase Number	10	2
V_{IN}	Operating input voltage	10.8 V to 13.2 V	
I_{IN}	Input current	0 to 80 A	
V_{BOOT}	Boot voltage	0.88 V	1.00 V
$I_{CC(max)}$	Maximum output current	400 A	50 A
$I_{CC(TDC)}$	Maximum Thermal DC current	350 A	45 A
$I_{CC(STEP)}$	Step transient current	225 A	12 A
R_{LL}	DC Load Line	0.0 mΩ	0.0 mΩ
TON_RISE	Output voltage rise time	1.25 ms	1.25 ms
TOFF_FALL	Output voltage fall time	1.25 ms	1.25 ms
T_{MAX}	Maximum temperature	100°C	100°C
SR_{FAST}	DVID slew rate	5 mV/µs	5 mV/µs
f_{SW}	Switching frequency	500 kHz	500 kHz
PMB_{ADDR}	PMBus address	96d / C0h	

8.1.1.3 Detailed Design Procedure

The following steps illustrate the key components selection for the 0.88V / 400A, 1V / 50A ASIC application.

Inductor Selection

Smaller inductance yields better transient performance, but leads to higher ripple current and lower efficiency. Higher inductance has the opposite effect. It is common practice to limit the ripple current to between 20%-40% of maximum per-phase current for balanced performance. In this design example, 30% of the maximum per-phase current is used for channel A.

$$\Delta I_{RIPPLE(target)} = \frac{I_{CC(MAX)}}{N_{\Phi}} \times 30\% = \frac{400A}{10phases} \times 0.3 = 12.0\ A \quad (48)$$

$$L_{target} = \frac{V_{OUT} \times (V_{in(max)} - V_{OUT})}{V_{in(max)} \times \Delta I_{RIPPLE(target)} \times f_{SW}} = \frac{0.88V \times (13.2V - 0.88V)}{13.2V \times 12A \times 500kHz} = 0.137\mu H \quad (49)$$

Considering the variation and derating of the inductance and a standard inductor value of 150nH with DCR 0.125 mΩ, is selected. Then use Equation 41 to re-calculate the actual output ripple.

$$I_{RIPPLE(actual)} = \frac{V_{OUT} \times (V_{in(max)} - V_{OUT})}{V_{in(max)} \times f_{SW} \times L_{actual}} = \frac{0.88V \times (13.2V - 0.88V)}{13.2V \times 500kHz \times 0.150\mu H} = 10.9A \quad (50)$$

With same design procedure for channel B, a standard inductor value of 150 nH with DCR 0.125 mΩ from ITG is chosen.

Output Capacitor Selection

Generally, consider output ripple and output voltage deviation during load transient when selecting output capacitors.

When available, follow the output capacitance recommendation for the load ASIC reference design. With TPS536C7B1 device, it is possible to meet the load transient with lower output capacitance due to the high-speed nature of DCAP+ control. Table 8-2 is the output capacitance recommendation for the above rail specification.

Table 8-2. Output Capacitor Recommendations

Capacitor location	Channel A	Channel B
Bulk capacitors near power stages	24x 470 µF / 2.5V / 3mΩ ESR	4x 470 µF / 2.5V / 3mΩ ESR
Top side	24x 220 µF / 4V / X5R/ 1206 18x 100 µF / 4V / X5R / 1206	4x 220 µF / 4V / X5R / 1206 3x 100 µF / 4V / X5R / 1206
Bottom side	24x 220 µF / 4V / X5R / 1206 18x 100 µF / 4V / X5R / 1206	4x 220 µF / 4V / X5R / 1206 3x 100 µF / 4V / X5R / 1206
Total output capacitance	24.4 mF	1874 µF

Select Per-Phase Valley Current Limit

Equation 42 shows the calculation of per-phase valley current limit based on maximum processor current, the operating phase number and per-phase current ripple $\Delta I_{RIPPLE(actual)}$.

For the channel A,

$$I_{OCL} = K_{margin} \times \frac{I_{CC(max)}}{N_{\Phi}} - \frac{\Delta I_{RIPPLE}}{2} = 1.25 \times \frac{400A}{10phases} - \frac{10.9A}{2} = 44.5A \quad (51)$$

Where K_{margin} is the maximum operating margin factor. Choose 125% margin to avoid triggering current limit during load transient events. For this design, choose the 47A valley current limit for channel A.

$$I_{SAT(min)} = I_{OCL} + \Delta I_{RIPPLE} = 47A + 10.9A = 57.9A \quad (52)$$

Equation 43 indicates the minimum saturation current for inductor. Using same design procedure, the valley current limit for channel B is selected to be 26 A.

Set USR threshold to improve load transient performance

There are two levels of undershoot reduction (USR1, USR2) options. USR1 enables up to 3, 4, 5 or all normal phases and USR2 enables all available phases. To select the proper value, start with each USR threshold set to be disabled, and then systematically lower the threshold, enabling fast-phase-addition to meet the load transient requirement.

For this design, phase shedding is disabled. USR1 and USR2 are selected to be disabled for both channel A and channel B.

Input Current Sensing (Shunt/ Calculated Iin/ Inductor DCR)

TPS536C7B1 has three input current sensing options: shunt current sensing, calculated input current sensing and inductor DCR current sensing. Either option may be chosen for precision input current reporting.

Shunt current sensing

In this design, the external shunt resistor 0.5 mΩ ± 1%, 3 W, 4026 package is selected. Once properly calibrated, Input current reporting is within the tolerance target.

Calculated input current sensing

TPS536C7B1 includes an option to impute input current for situations in which the addition of a shunt or input inductor is prohibitive. Connect pins 46 (VIN_CSNIN) and 47 (CSPIN) together, and place a minimum 1 µF effective capacitance bypass cap from pin 46 to GND, then connect pin 46 to input supply (12 V nominally) before input inductor. Configure the calculated input current option through the NVM settings in MFR_SPECIFIC_ED (MISC OPTIONS).

Inductor DCR Current Sensing

This section describes the procedure to determine an inductor DCR thermal compensation network design. Figure 8-6 shows a typical DCR sensing circuit. From Equation 44 and Equation 45, when the time constant of the RC network is equal to the L/R time constant of the inductor, the capacitor voltage V_C across the C_{SENSE} capacitor can be used to obtain the inductor current. However, inductor windings have a positive temperature coefficient of approximately 3900 ppm/°C. So an NTC thermistor is used to cancel thermal variation from the inductor DCR.

The design goal is for the DCR value to be invariant with the temperature. Therefore, the voltage across sense capacitor would be only dependent on the inductor current over the temperature range of interest.

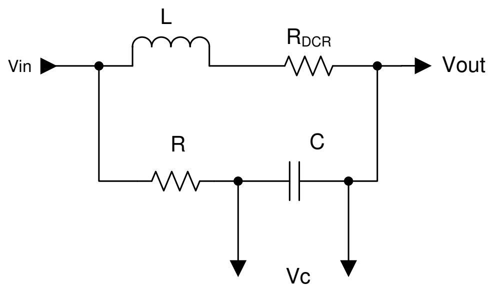


Figure 1

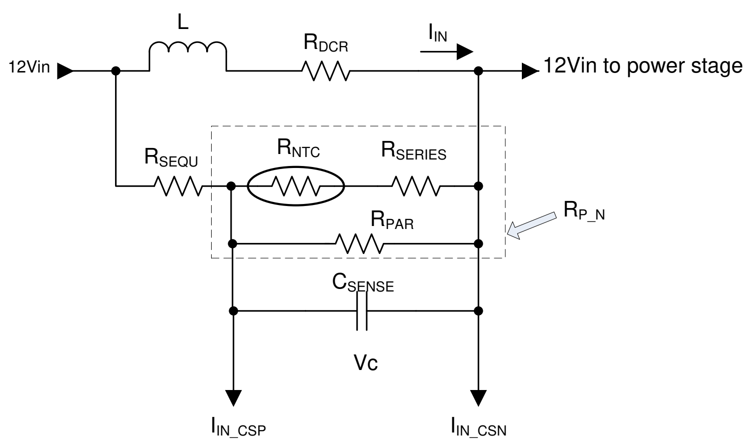


Figure 2

Figure 8-6. Input DCR Network

$$C_{SENSE} \times R_{EQ} = \frac{L}{R_{DCR}} \tag{53}$$

$$I_{IN} \times R_{DCR} = V_{DCR} \tag{54}$$

The equivalent resistance of the R_{SEQU}, R_{NTC}, R_{SERIES} and R_{PAR} values is given by R_{EQ} in Equation 46. Use Equation 46, Equation 47 and Equation 48 to derive the values of R_{SEQU}, R_{NTC}, R_{SERIES} and R_{PAR}.

$$R_{EQ} = \frac{R_{P\_N}}{R_{P\_N} + R_{SEQU}} s \tag{55}$$

$$R_{P\_N} = \frac{R_{PAR} \times (R_{NTC} + R_{SERIES})}{R_{PAR} + R_{NTC} + R_{SERIES}} \tag{56}$$

$$V_C = V_{DCR} \times R_{EQ} = \frac{I_{IN} \times R_{DCR} \times R_{P\_N}}{R_{P\_N} + R_{SEQU}} = \beta \times I_{IN} \quad (57)$$

Finally the value of β, given in Equation 49 represents the effective current sense gain after thermal compensation. This value can be used as the sense element resistance to derive the PMBus settings as described in Input current calibration (measured).

$$\beta = \frac{R_{DCR} \times R_{P\_N}}{R_{P\_N} + R_{SEQU}} \quad (58)$$

For this design, select thermistor RNTC as 1 kΩ, 5%, 0603, B-constant is 3650k, P/N: NCP18XQ102J03B from Murata. Select C_{SENSE} as 1 µF X7R or better dielectric (C0G preferred).

In order to solve the value of R_{SEQU}, R_{SERIES} and R_{PAR}, the β at three temperature points are set equal. set β = 0.15 mΩ equally at temperature 0 °C, 25 °C and 75 °C. With the calculation, three resistors value can be found as R_{SEQU} = 332 Ω, R_{SERIES} = 432 Ω, R_{PAR} = 1.40 kΩ.

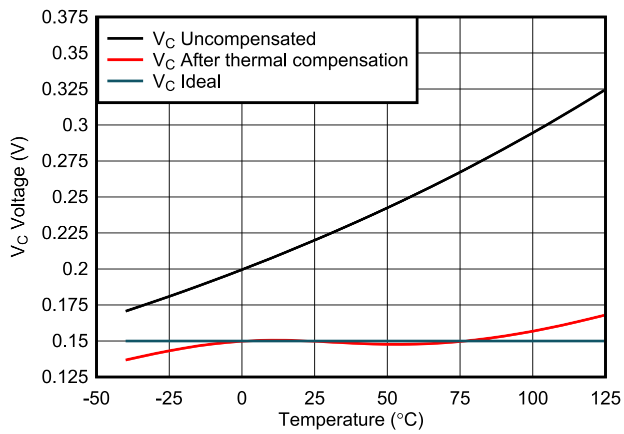


Figure 8-7. Inductor DCR sensing voltage over temperature

TI offers an application note and excel spreadsheet to streamline input DCR netowrk calculations. Contact your local field/sales representative to get a copy of the document.

Loop compensation design

- 5 mΩ: Typical gain from power stage current sense
- ACLL: Programmable AC load line, provides direct output voltage feedback.
- DCLL: Programmable DC load line, provides adaptive voltage positioning
- K_{DIV} : Fixed scalar with value of 0.5
- τ_{INT} : Programmable integration time constant, adjustable from 1µs to 16 µs (scale = 1 µs)
- K_{INT} : Programmable integration gain which can be adjustable from 0.5x, 1x, 1.5x, 2x
- K_{AC} : Programmable AC gain which is adjustable from 0.5x, 1x, 1.5x, 2x
- V_{RAMP} : Programmable ramp voltage which is adjustable from 80 mV to 320 mV(scale = 40 mV)

For this design, the optimal loop compensation values were derived by tuning. The final valuea are listed .

Table 8-3.

PARAMETER	Channel A	Channel B
DCLL	0.0 mΩ	0.0 mΩ
ACLL	0.2 mΩ	0.5 mΩ
τ_{INT}	1 µs	7 µs
K_{INT}	2.0	1.0
K_{AC}	1.0	1.0

Table 8-3. (continued)

PARAMETER	Channel A	Channel B
V_{RAMP}	320 mV	200 mV

Select ADDR_CONFIG pin resistors

Based on the design requirements of PMBus address select the upper and lower ADDR_CONFIG pin resistors, R_{HA} and R_{LA} according to #none##none##none#.

Table 8-4.

Phase configuration	PMBus address	R_{HA}	R_{LA}
10+2	96d / C0h	110 kΩ	37.4 kΩ

Select the boot voltage V_{BOOT} for each channel

The boot voltage for channel A is determined by pinstrapping on the VBOOT_CHA pin. Based on #none##none##none##none#, select R_{HB} = 20.0 kΩ and R_{LB} = 59.0 kΩ to select 0.88 V as the channel A boot voltage.

The boot voltage for channel B is stored in NVM. Update the NVM value for VOUT_COMMAND to 1.0 V , and store the value to non-volatile memory.

8.1.1.4 Application Performance Plots

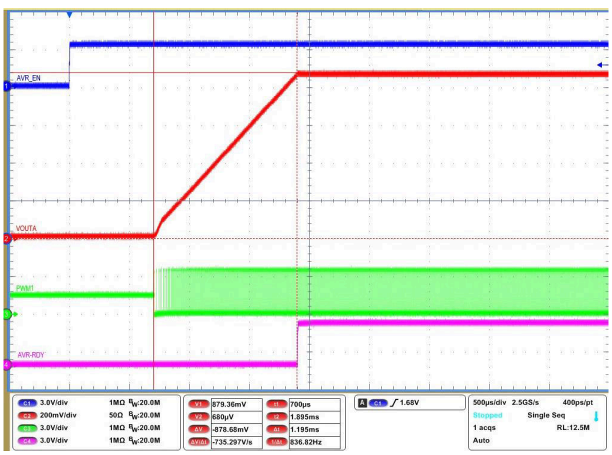


Figure 8-8. Soft-start channel A (0 ms TON_DELAY)

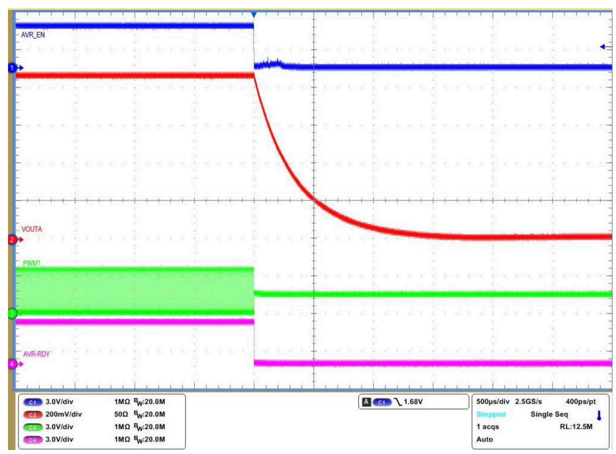


Figure 8-9. Shutdown (immediate off) channel A

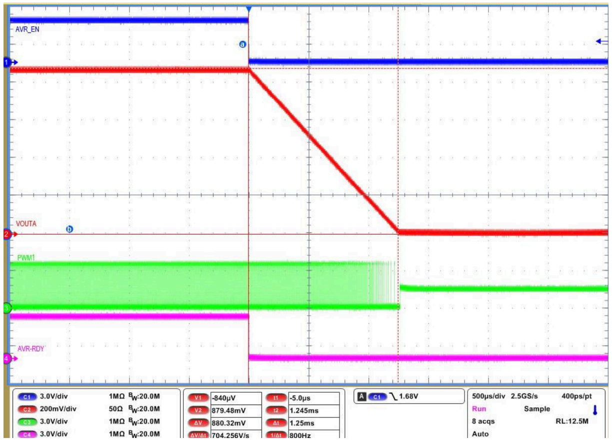


Figure 8-10. Soft-stop channel A (0 ms TOFF_DELAY)

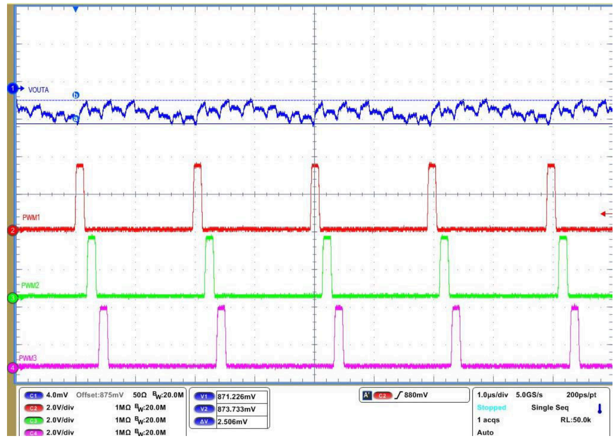


Figure 8-11. Steady-state ripple channel A

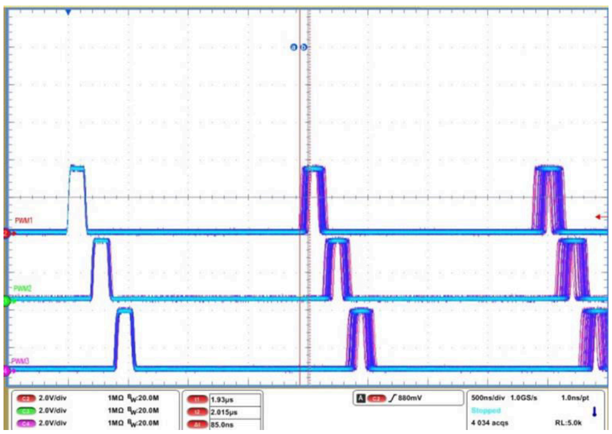


Figure 8-12. Steady-state PWM jitter channel A

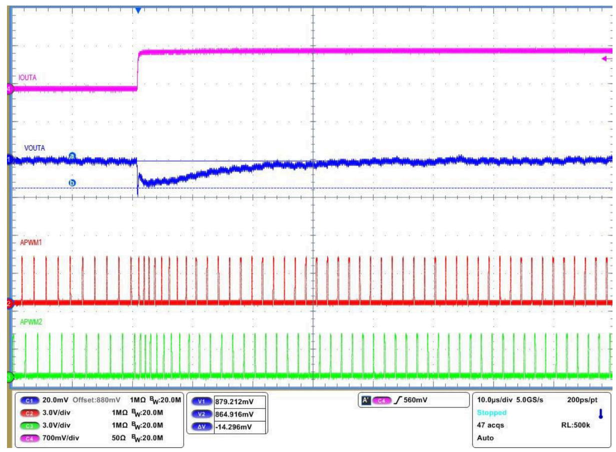


Figure 8-13. Load step response channel A

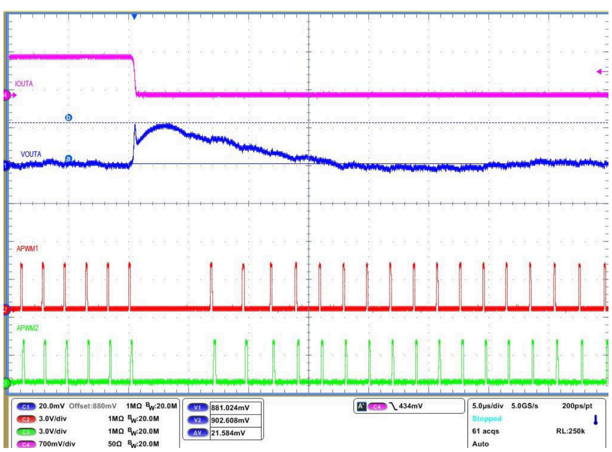


Figure 8-14. Load release response channel A

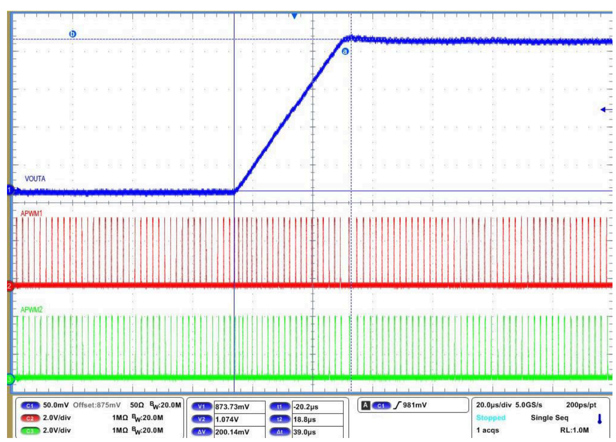


Figure 8-15. DVID up transition channel A

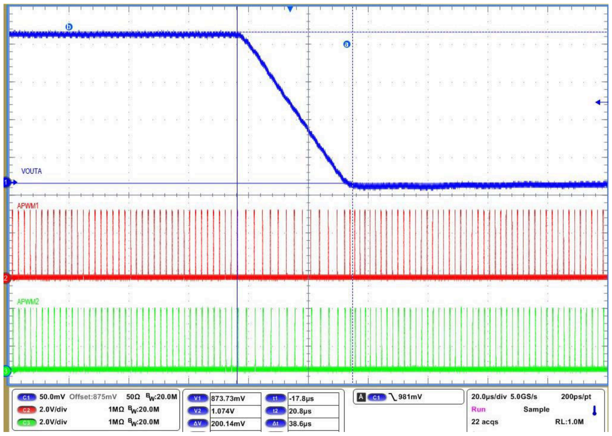


Figure 8-16. DVID down transition channel A

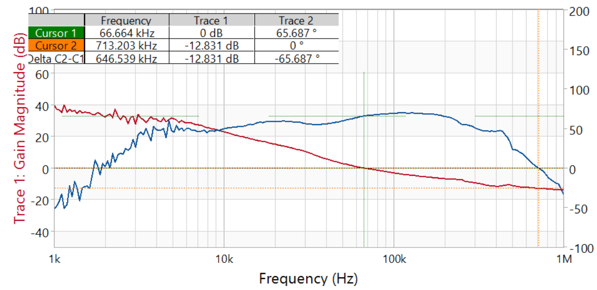


Figure 8-17. Closed loop bode plot channel A

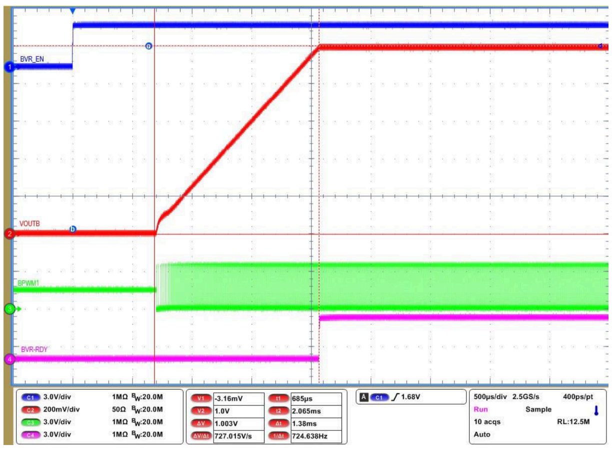


Figure 8-18. Soft-start Channel B (0 ms TON_DELAY)

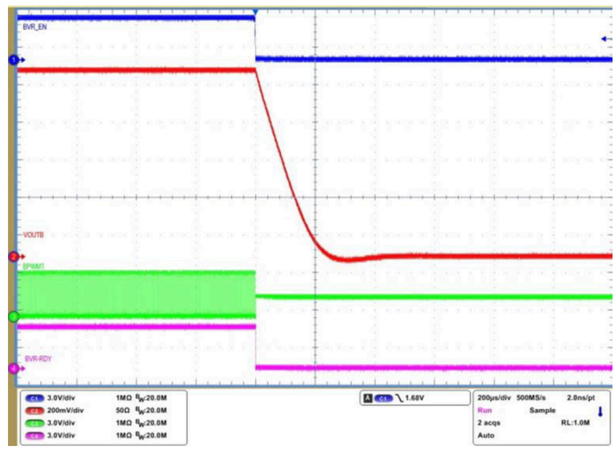


Figure 8-19. Shutdown (immediate off) channel B

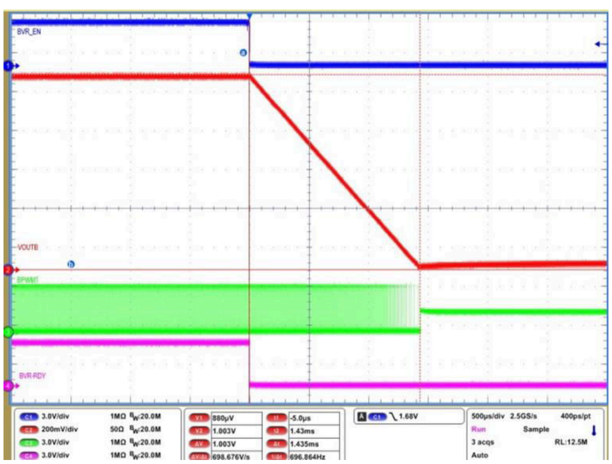


Figure 8-20. Soft-stop channel B (0 ms TOFF_DELAY)

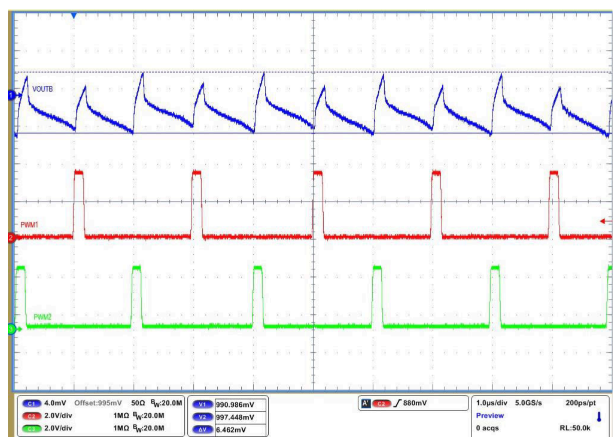


Figure 8-21. Steady-state ripple channel B

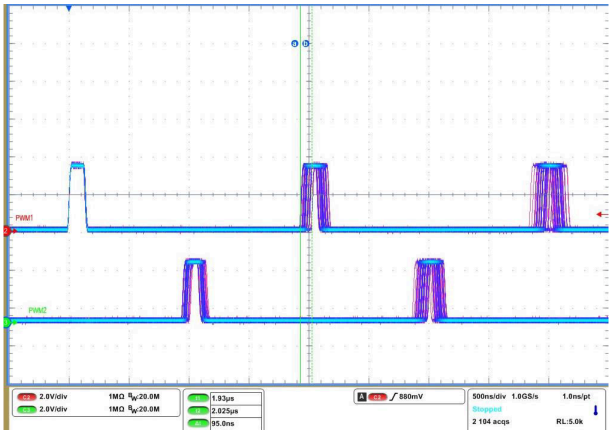


Figure 8-22. Steady-state PWM jitter channel B

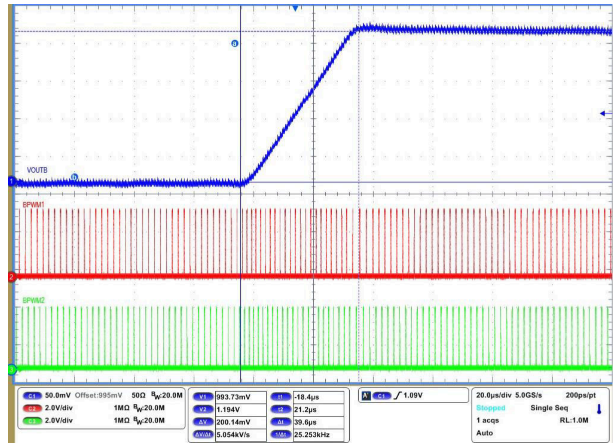


Figure 8-23. DVID transition up channel B

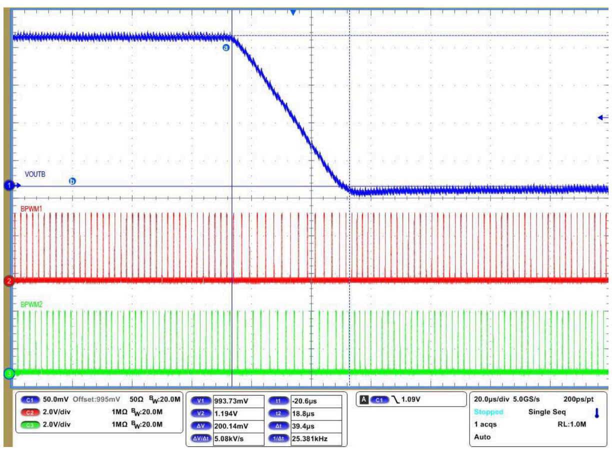


Figure 8-24. DVID transition down channel B

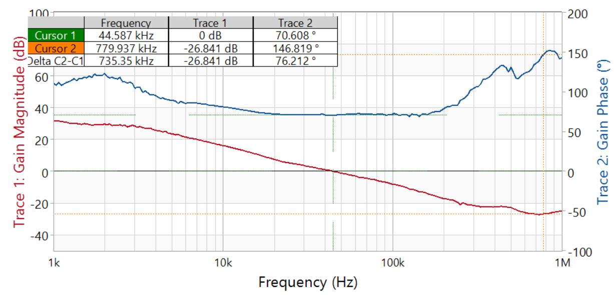


Figure 8-25. Closed loop bode plot channel B

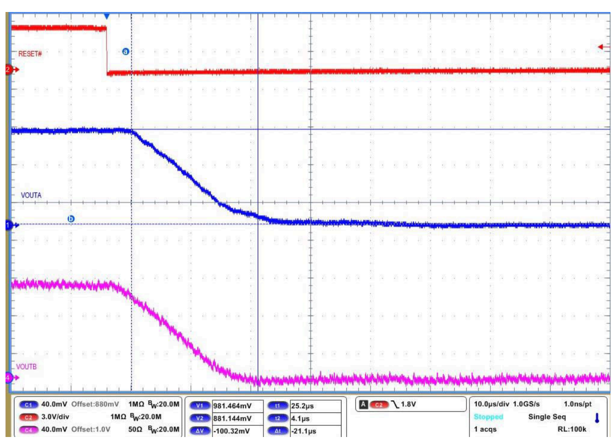


Figure 8-26. RESET# pin function

9 Power Supply Recommendations

The TPS536C7B1 does not have strict power sequencing requirements. The VCC supply, power stage VDD 5V supply, VIN_CSNIN and CSPIN supplies may be safely powered up independently of each other, even if the VCC supply voltage is off and low-impedance. Do not raise pull-up voltages for open-drain pins AVR_RDY, BVR_RDY, SMB_ALRT#, SMB_DIO, VR_FAULT# before the VCC supply, or pull them to voltages above the VCC voltage during operation. If system sequencing requirements mandate raising the pull-up voltages for these pins prior to VCC being established, limit the pin current to 1.0 mA to avoid damage to the device.

The minimum pull-up resistor value for open drain pins AVR_RDY, BVR_RDY, SMB_ALRT#, SMB_DIO, VR_FAULT# is limited by the allowable sinking current for the pin. The maximum pull-up resistor value is limited by the off-state leakage current for the pin, and the logic level of any downstream device using the pin as an input. Table 9-1 summarizes the allowable sinking current and off-state leakage for open drain IO pins.

Table 9-1. Open Drain Pin Current Capability

Open-drain Pin	Maximum Current	
	On-state Sinking (mA)	Off-state leakage[1] (µA)
AVR_RDY	25.0	1.0
BVR_RDY	25.0	1.0
SMB_ALRT#	20.0	1.0
SMB_DIO	20.0	1.0
VR_FAULT#	20.0	4.0

1. T_J = 125°C

For input pins ACSPx, BCSPx, AVR_EN, BVR_EN, SYNC, RESET#, which exceed the VCC pin value during operation, during power-on or otherwise, include a series resistor of 10.0 kΩ or greater to limit the current into the pin.

It is safe to power-on the VDD 5V supply to TI smart power stage devices prior to TPS536C7B1 VCC. TI smart power stage devices do not source any unsafe voltages or currents into TPS536C7B1 ACSPx, BCSPx, ATSEN, BTSEN, APWMx, BPWMx pins when the VCC pin is not powered.

TI smart power stages (CSD95xxx) provide hysteresis current on their PWM input pins to improve noise immunity. This current is active when the power stage is powered by 5V VDD and enabled, regardless of the status of VCC. When the VCC pin of TPS536C7B1 is unpowered, this hysteresis current flows through the PWM pins, to ESD structures in the controller, causing the PWM pin voltage to float low, out of the tri-state window. This can cause the power stage device to switch its low-side power MOSFET on. As a result, in any case where the power stage VDD 5V power supply is enabled prior to VCC, supply, TI recommends to control the power stage enable pin to be low until both supply voltages are established.

TPS536C7B1 voltage and current protections become active when the controller VCC supply is powered. TI recommends the VCC voltage be powered first, prior to power stage 5V, or VIN_CSNIN/CSPIN voltages. In general, TI recommends to assert the AVR_EN/BVR_EN pins last in the power sequence.

Other sequences are permissible, but may not be able to make use of the controller protection features. For example, if a board assembly issue causes the power input supply (e.g. nominally 12V supply) to charge the output voltage, the TPS536C7B1 over-voltage protection can protect the load device by forcing the PWM pins low, causing the power stage devices to discharge the output voltage, but only if the VCC supply is established by the time the power input voltage rises.

10 Layout

Proper layout techniques are critical to power supply performance. The recommendations given in this document are meant to minimize risk and give the highest possibility of first pass success. Other layout designs are possible but may carry higher risk of performance issues. Contact your TI local field/sales representative for in-depth guidance and layout reviews.

The driverless controller architecture makes it easy to separate noisy driver interface lines from sensitive controller signals. Because the power stage is external to the device, all gate drive and switch node traces must be local to the inductor and power stages.

Controller Layout Guidelines

- Keep minimum 800 mil distance between the controller and the closest power stage
- Ensure the controller and all power stages must share a common ground plane
- Route CSPx /VREF differentially from controller to IOUT/REFIN pin of each power stages on a quiet inner layer. Alternately, create a small VREF copper plane between controller and power stages, and embed the CSPx traces inside VREF plane.
- PWMx must be routed on a different quiet inner layer and not on the same layer next to CSPx/VREF differential pairs.

Note

MOST IMPORTANT LAYOUT RECOMMENDATION: Must keep min 40mil clearance between 12Vin copper/vias/traces and sensitive analog interface lines.

Power stage layout guidelines

- Use the recommended land and via pattern for power stage footprint
- Make layer 2 on the PCB stack a solid ground plane
- Maximize the phase pitch between adjacent phases whenever possible to prevent any cross-coupling noise between devices (9 mm or higher is preferred)
- In cases where the phase pitch is tighter, adjust the controller phase firing order to minimize noise coupling between devices.
- The input voltage bypass capacitors require a minimum two vias per pad(for both Vin and GND)
- Place additional GND vias along the sides of device as space allows
- For multi-phase systems, ensure that the GND pour connects all phases.
- Connect the VOS pin feedback point to the inner edge of the inductor output pad.
- Place VDD and PVDD bypass capacitors directly next to pins on the same layer of the device.

Layout example

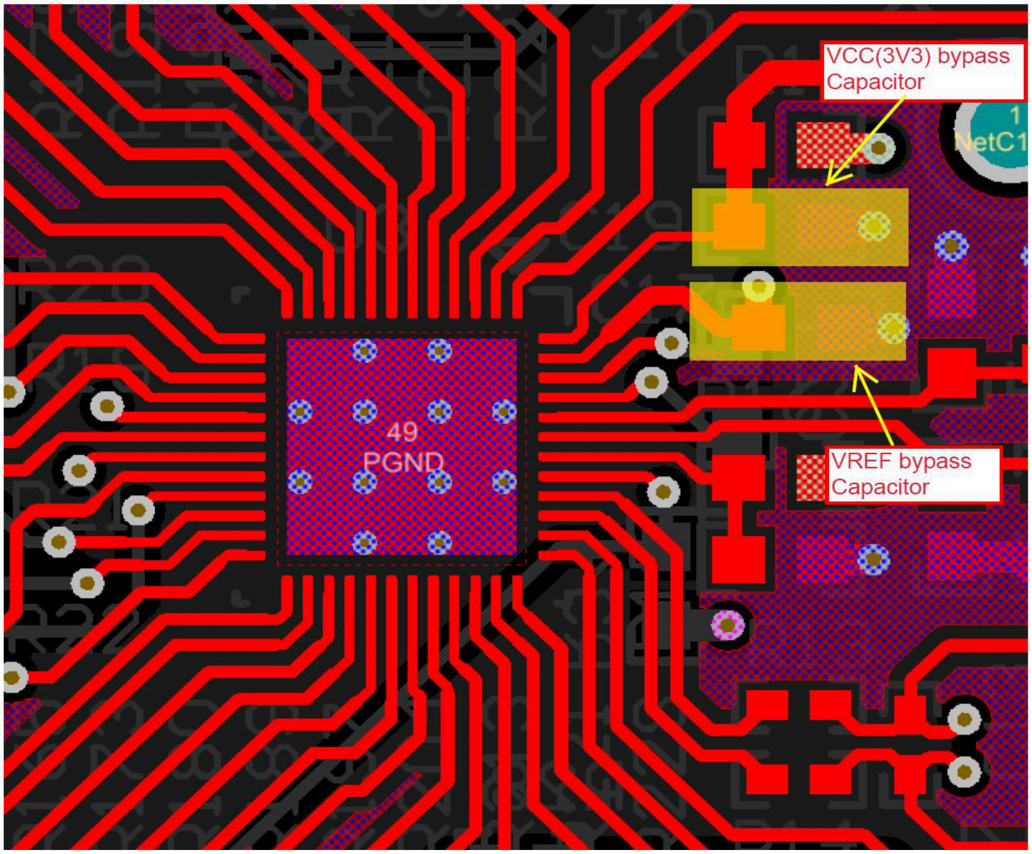


Figure 10-1. Controller layout example

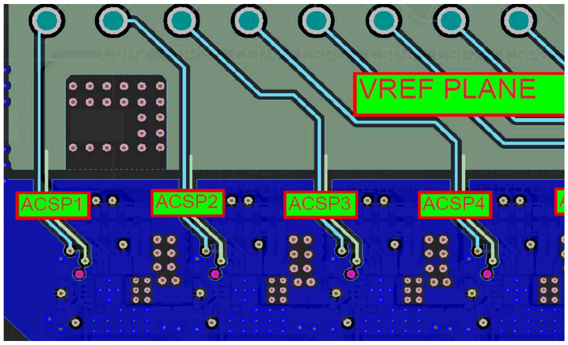


Figure 10-2. CSP signal routing example

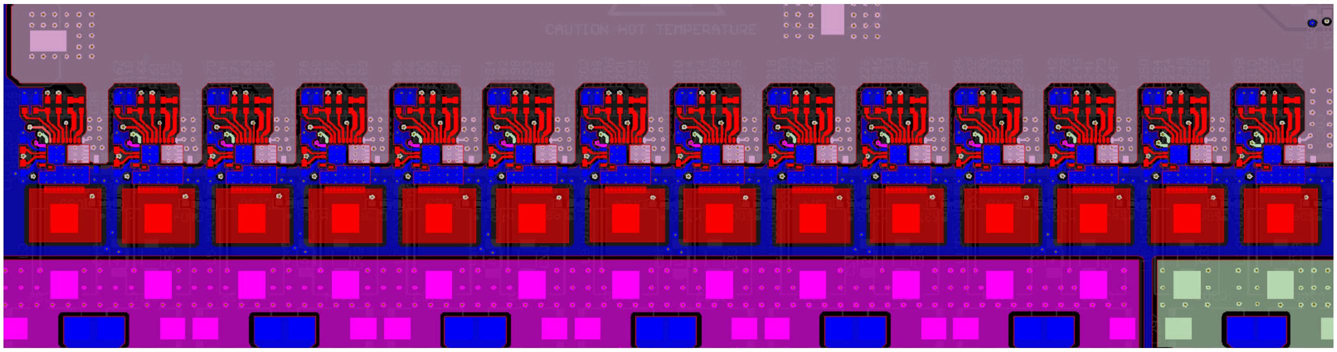


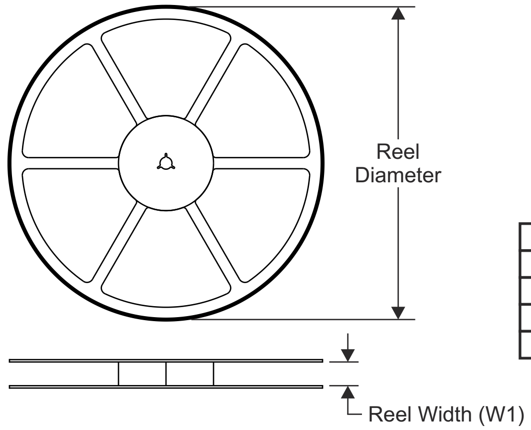
Figure 10-3. Power stage placement example

11 Mechanical, Packaging, and Orderable Information

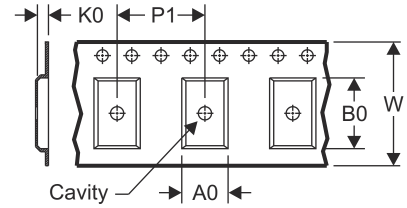
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

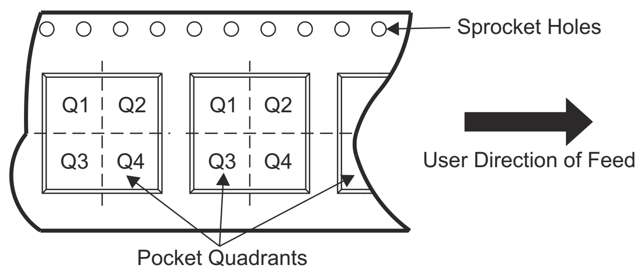


TAPE DIMENSIONS



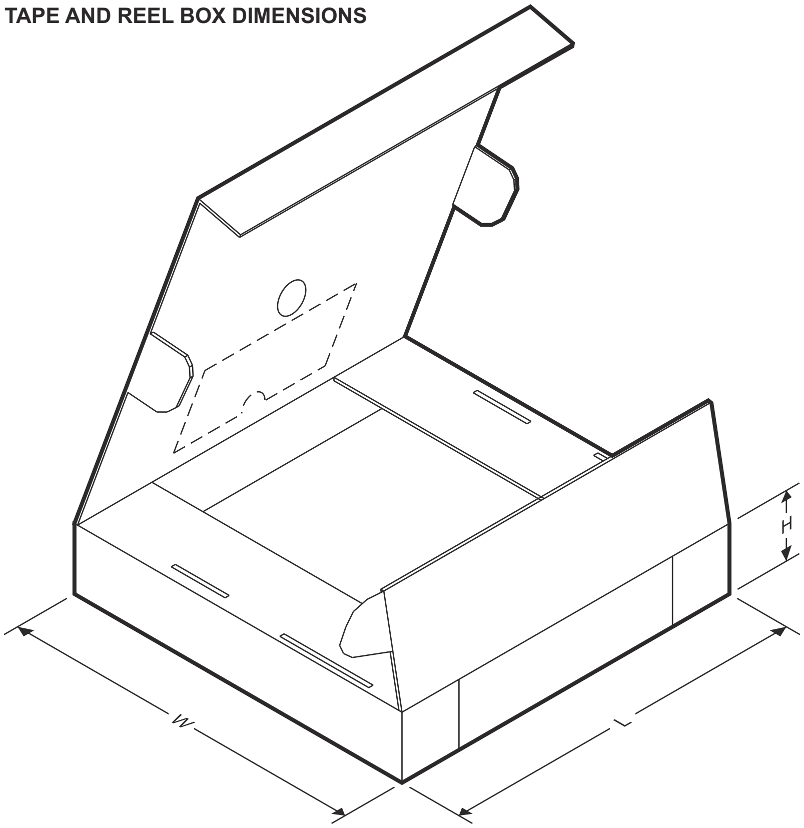
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS536C7B1RSLR	VQFN	RSL	48	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS536C7B1RSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS536C7B1RSLR	VQFN	RSL	48	3000	367.0	367.0	38.0
TPS536C7B1RSLT	VQFN	RSL	48	250	210.0	185.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS536C7B1RSLR	ACTIVE	VQFN	RSL	48	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS 536C7B1	Samples
TPS536C7B1RSLT	ACTIVE	VQFN	RSL	48	250	RoHS & Green	Call TI | NIPDAUAG	Level-3-260C-168 HR	-40 to 125	TPS 536C7B1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

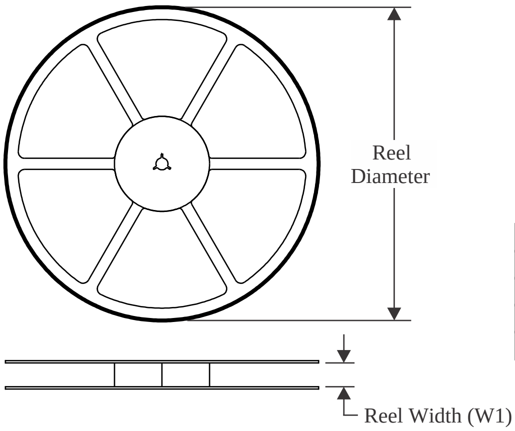
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

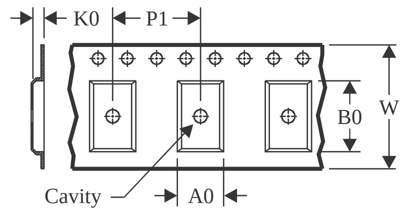
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

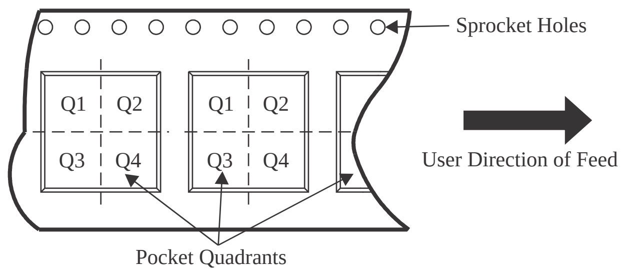
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





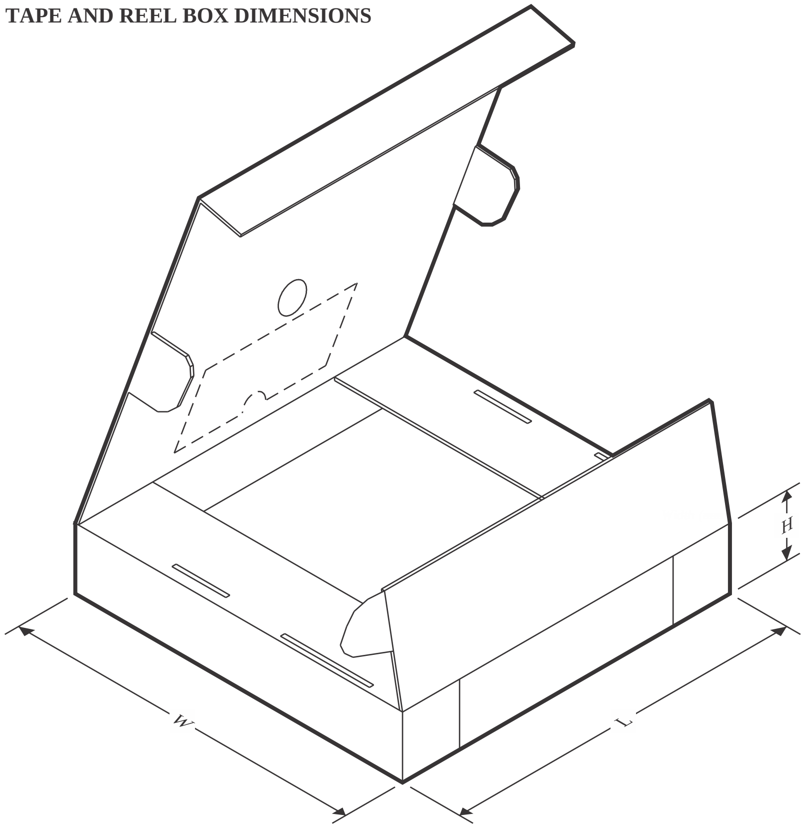
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS536C7B1RSLR	VQFN	RSL	48	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

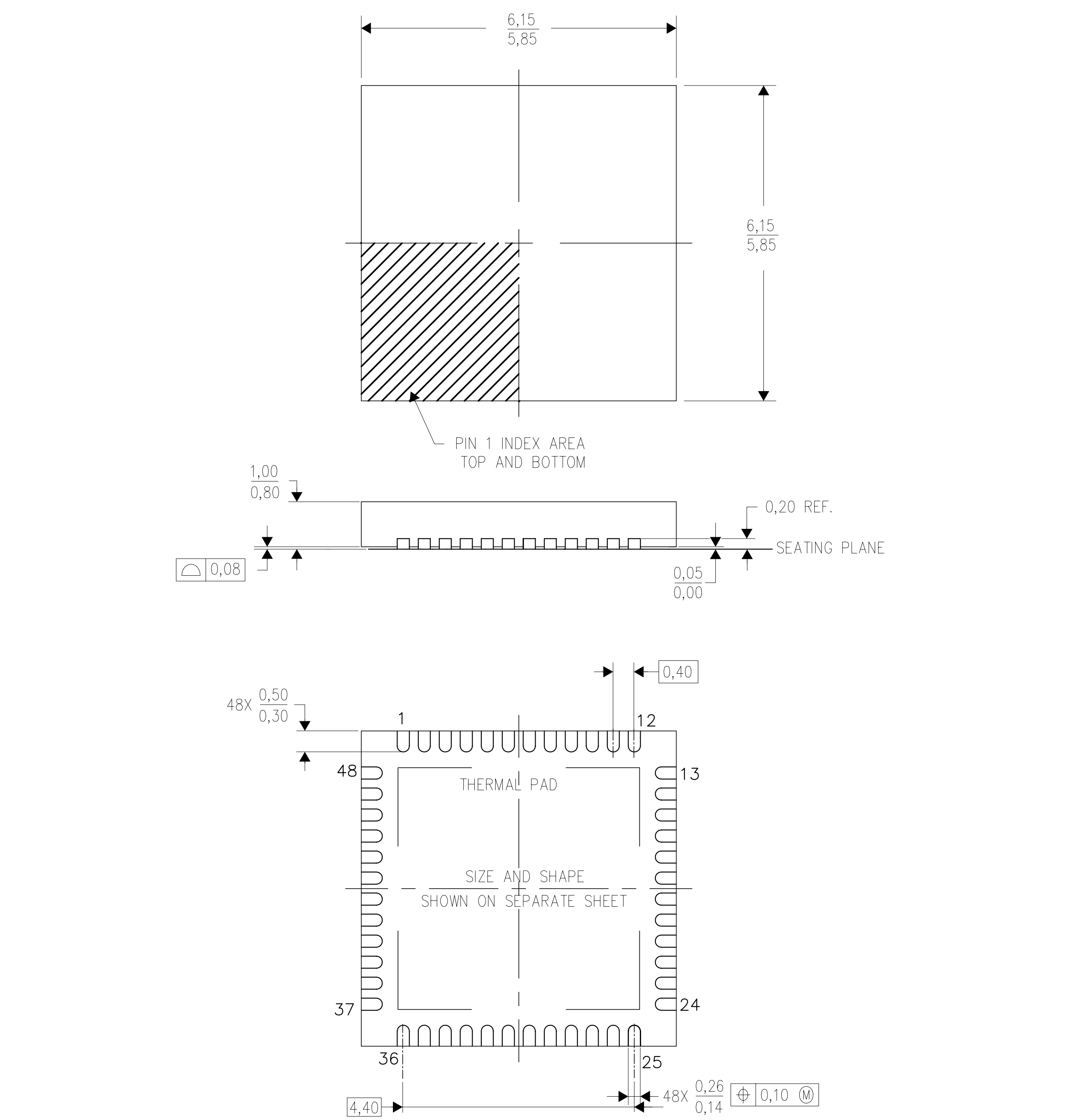
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS536C7B1RSLR	VQFN	RSL	48	3000	367.0	367.0	38.0

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



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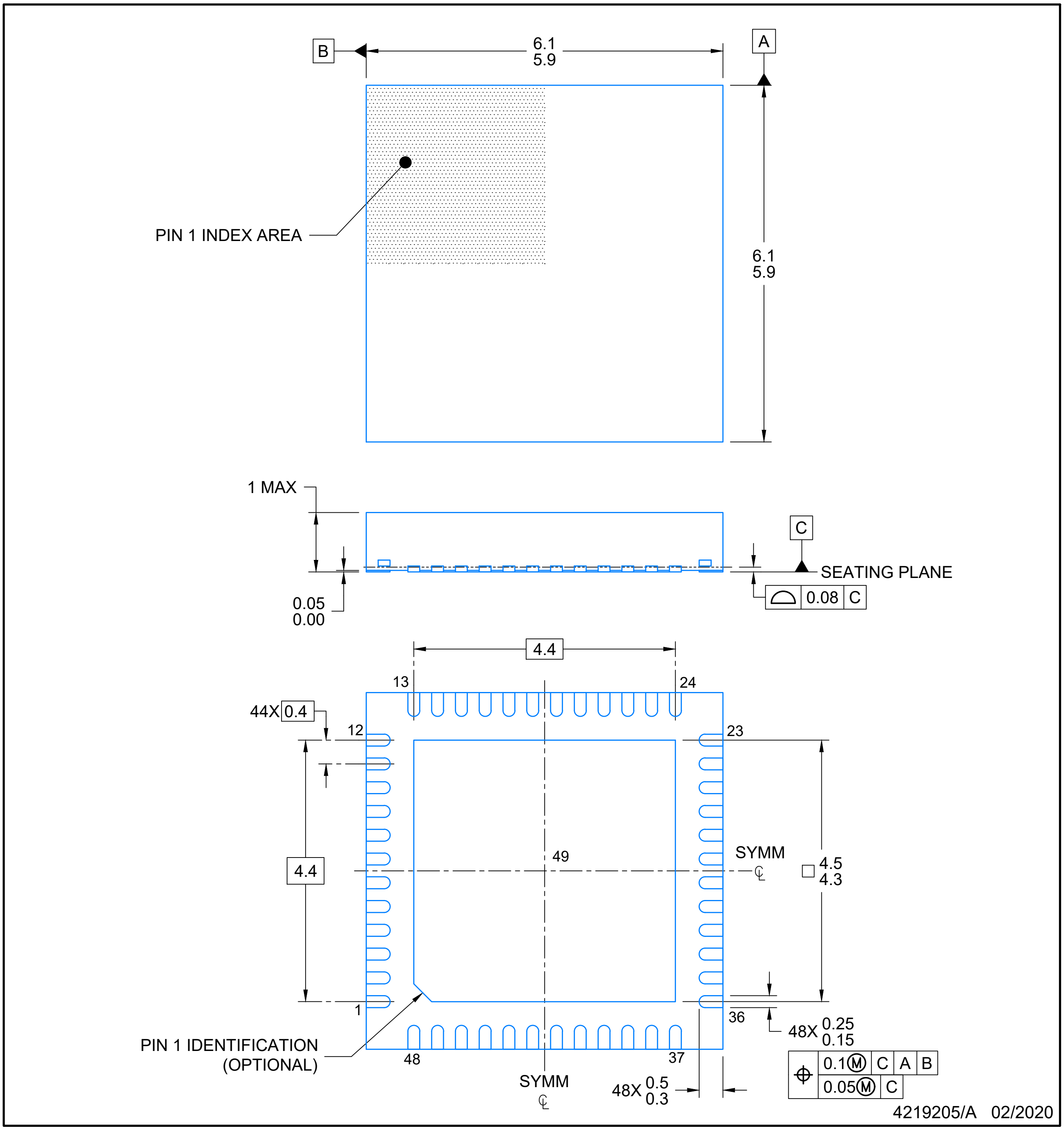
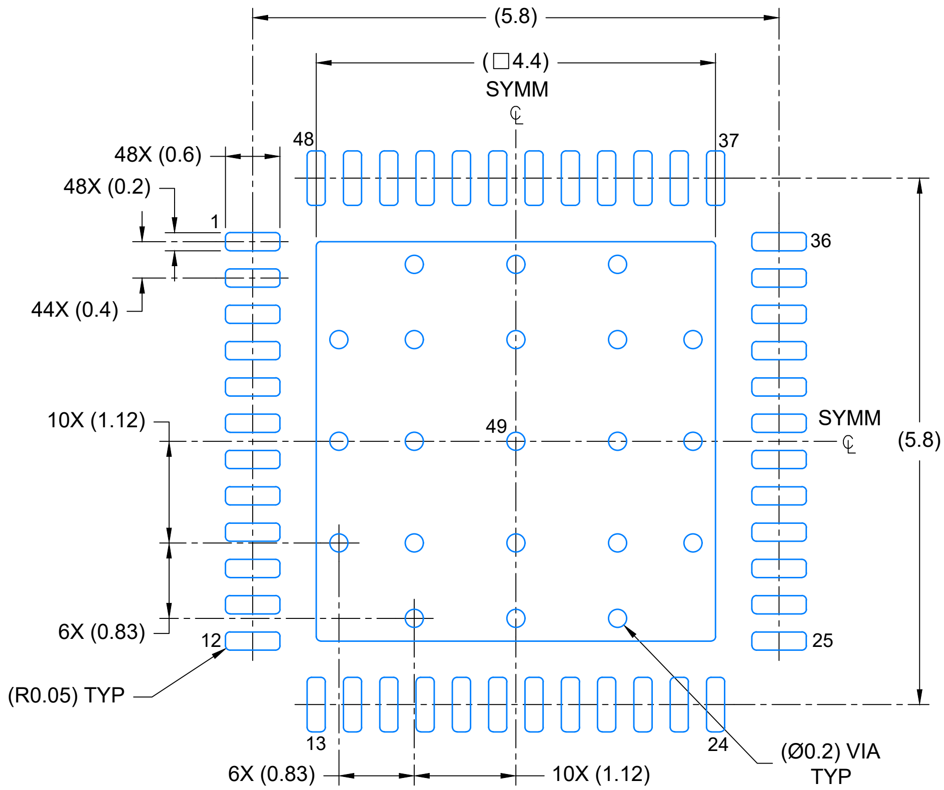
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

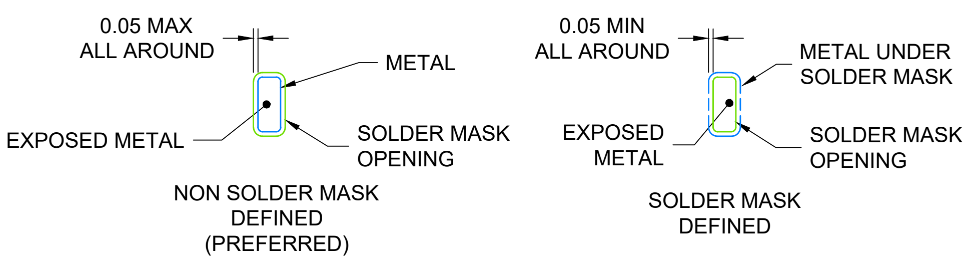


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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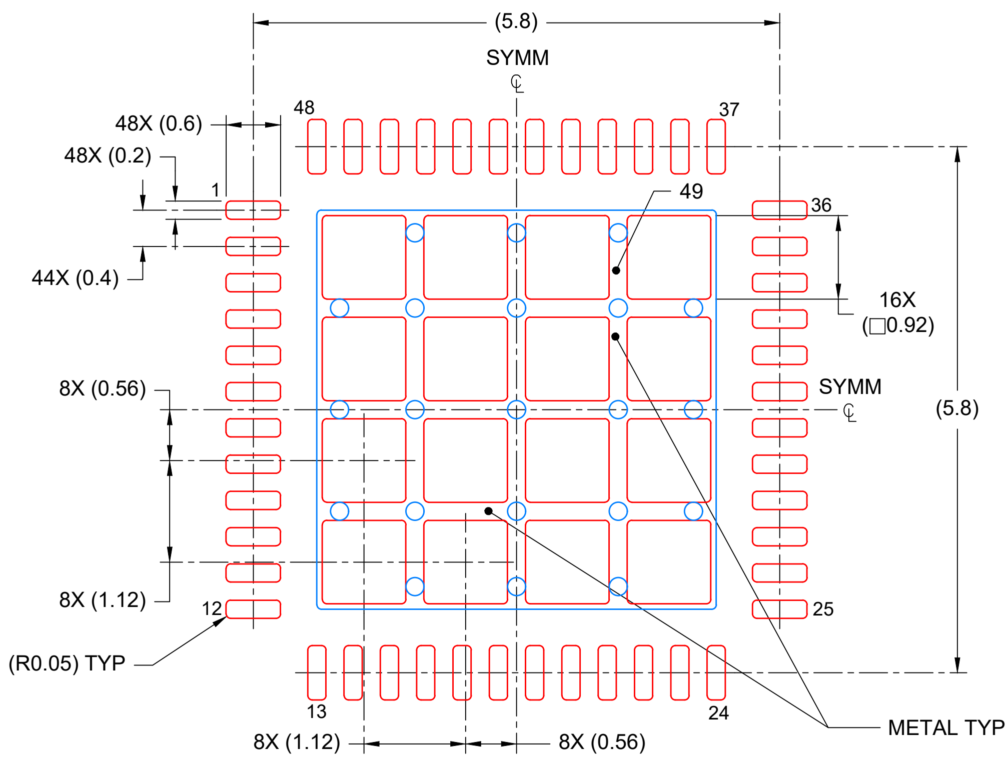
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 12X

4219205/A 02/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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