TPS536C9T Dual-channel (N + M ≤ 12 phase) D-CAP+™, Step-down, Multiphase Controllers with TLVR support, PMBus and VR14 SVID Interfaces

1 Features

- Input voltage range: 4.5 V to 17 V
- Output voltage range: 0.25 V to 5.5 V
- Dual output supporting N+M phase configurations (N+M ≤ 12, M ≤ 6)
- Native trans-inductor voltage regulator (TLVR) topology support, with L_C open and short protection
- Fully compatible with TI smart power stages
- Supports voltage- and current-source Imon power stages, with internal 1 kΩ resistor
- Support for traditional (legacy mode) and limp mode power stage fault identification
- Supports dual side power delivery with 12"+ trace length
- Intel® VR14 SVID compliant with PSYS support
- Backward compatible to VR13.HC/VR13.0 SVID
- Automatic NVM fault status logging
- Enhanced D-CAP+ control to provider superior transient performance with excellent dynamic current sharing
- Dynamic phase shedding with programmable thresholds for optimizing efficiency at light and heavy loads
- Configurable with non-volatile memory (NVM) for low external component count
- Individual per-phase IMON calibration, with multi-slope gain calibration to increase system accuracy
- Diode braking with programmable timeout for reduced transient overshoot
- Programmable per-phase valley current limit (OCL)
- PMBus™ v1.3.1 system interface for telemetry of voltage, current, power, temperature, and fault conditions
- Programmable loop compensation through PMBus
- 6.00 mm × 6.00 mm, 48-pin, QFN package

2 Applications

- Data center & enterprise computing rack server
- Hardware accelerator
- Network interface card (NIC)
- ASIC and high performance client

3 Description

The TPS536C9T is a VR14 SVID compliant step down controller with trans-inductor voltage regulator (TLVR) topology support, two channels, built-in non-volatile memory (NVM), and PMBus™ interface, and is fully compatible with TI smart power stages. Advanced control features such as the D-CAP+ architecture provide fast transient response, low output capacitance, and good dynamic current sharing. Adjustable control of output voltage slew rate and adaptive voltage positioning are natively supported. In addition, the device supports the PMBus communication interface for reporting the telemetry of voltage, current, power, temperature, and fault conditions to the host system. All programmable parameters can be configured through the PMBus interface and can be stored in NVM as the new default values, to minimize the external component count.

Package Information

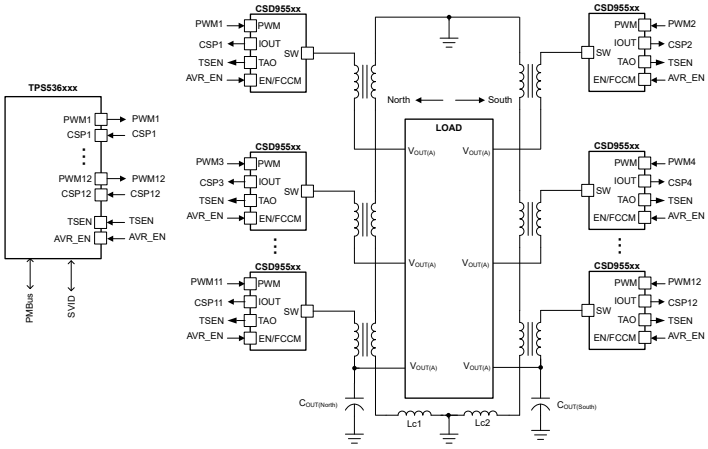
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS536C9T	RSL (QFN, 48)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER(1)	PHASE COUNT
TPS536C9T	12 phases

(1) See the *Device Comparison Table*



Simplified Application (Interleaved TLVR)

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2023	*	Initial Release

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Documentation Support

5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS536C9TRSLR	ACTIVE	VQFN	RSL	48	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 536C9T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

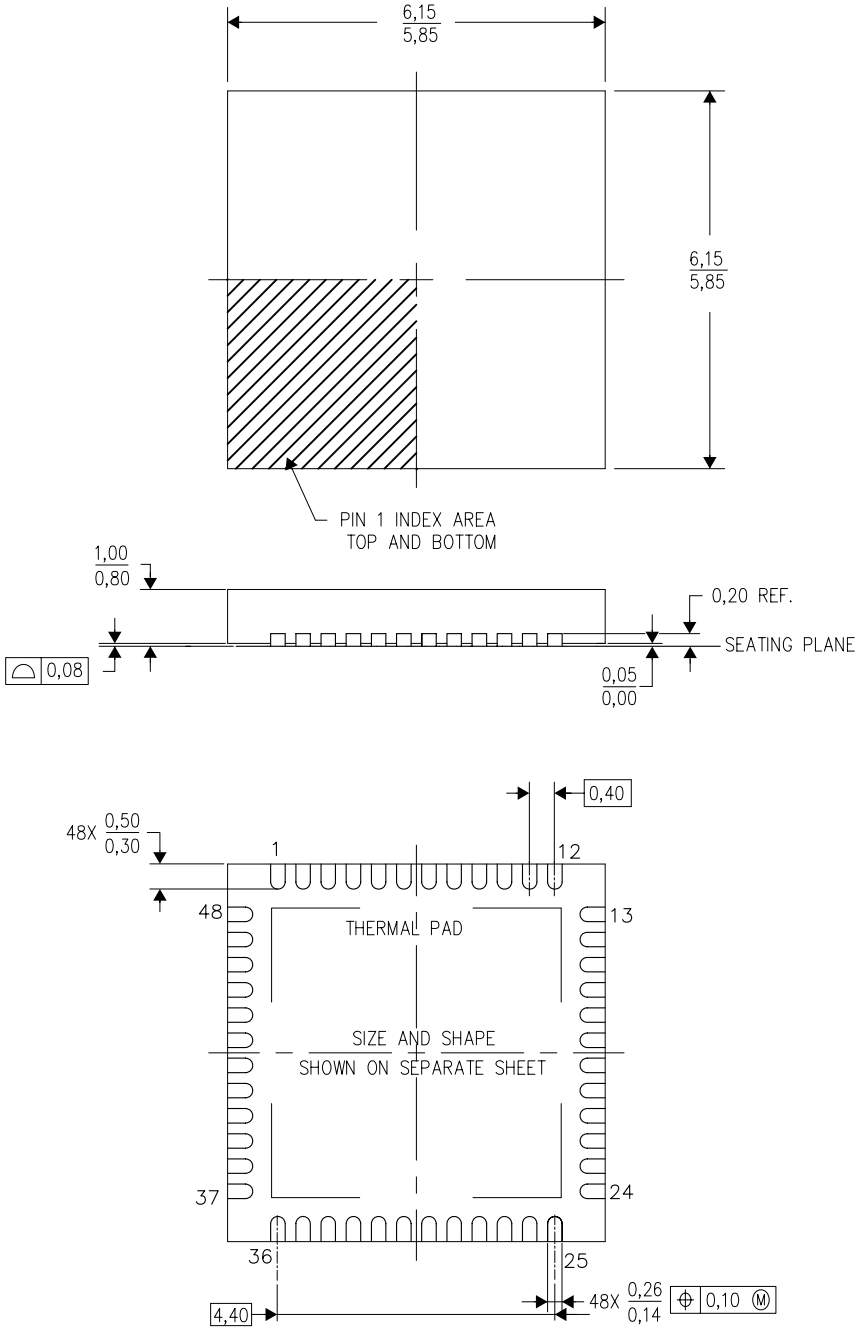
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



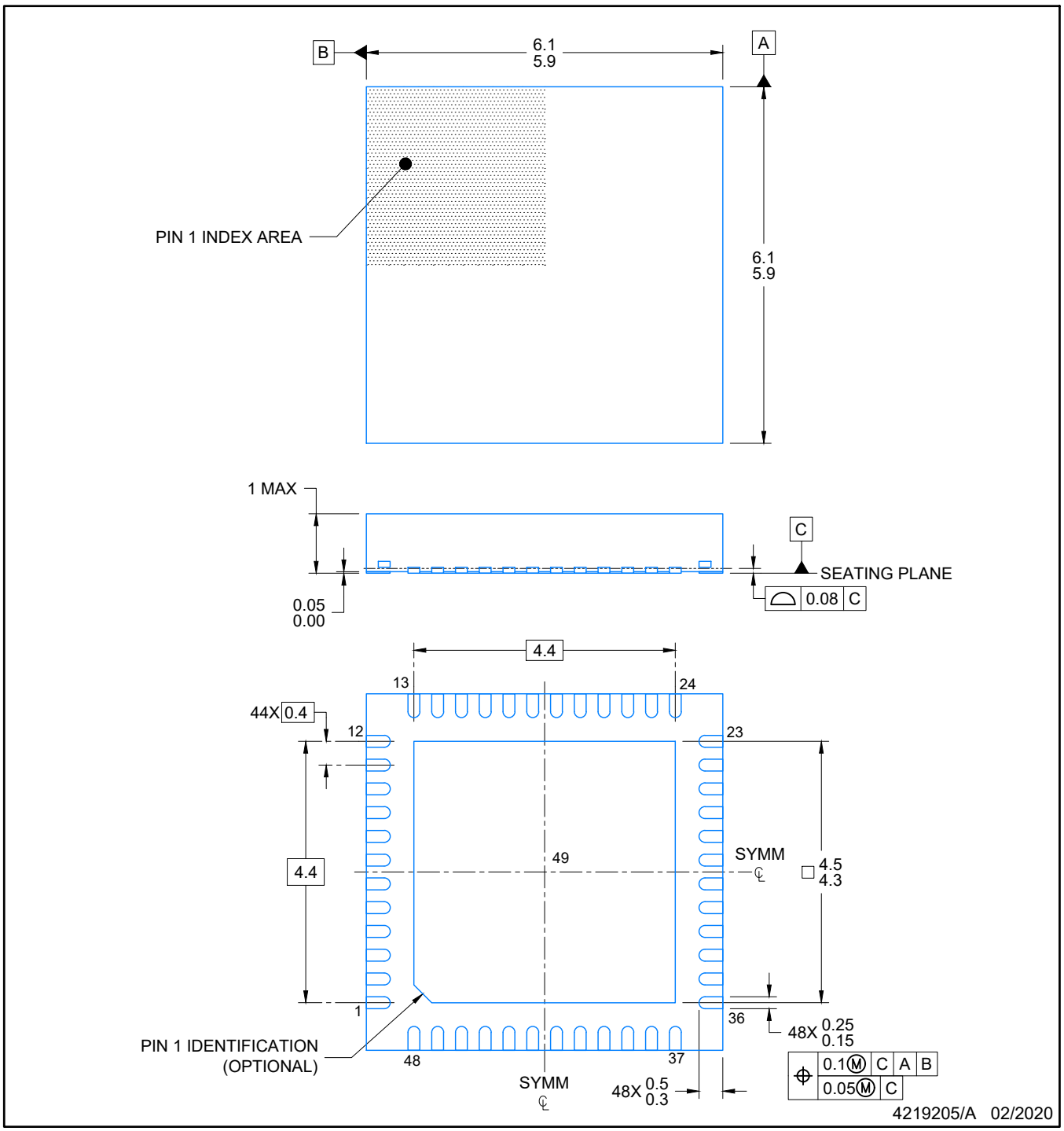
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

PACKAGE OUTLINE

RSL0048B

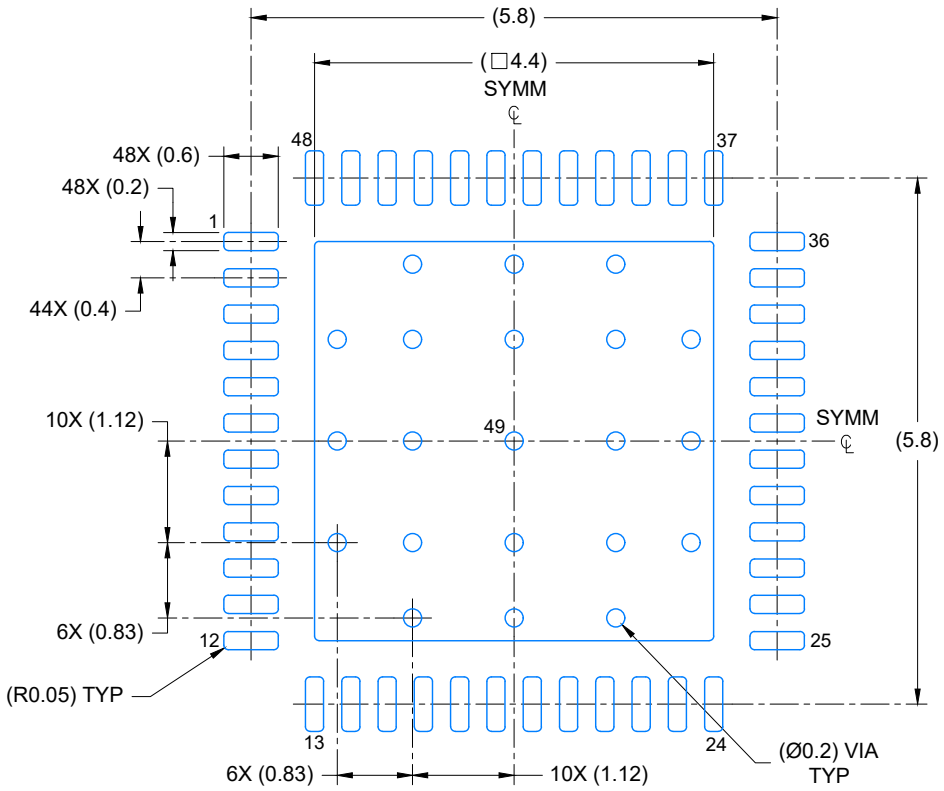
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

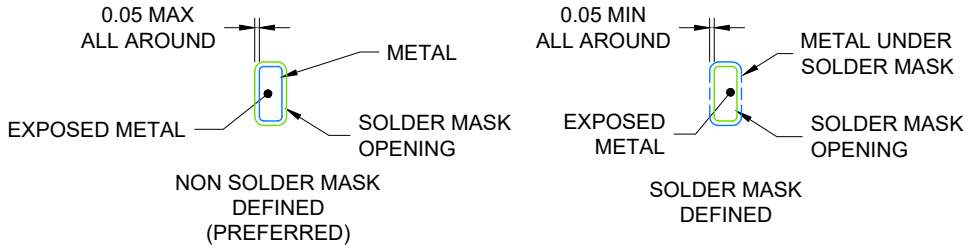


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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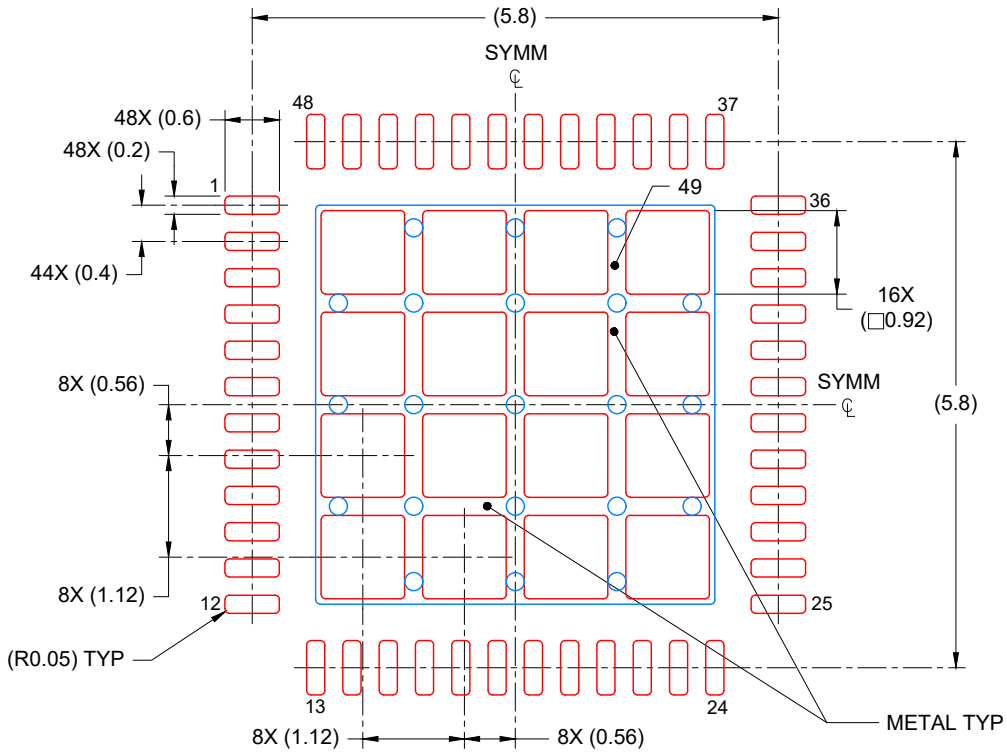
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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