LCD Bias with Integrated Gamma Reference for Notebook PCs, Tablet PCs and Monitors

Check for Samples: TPS65642

1 Introduction

1.1 Features

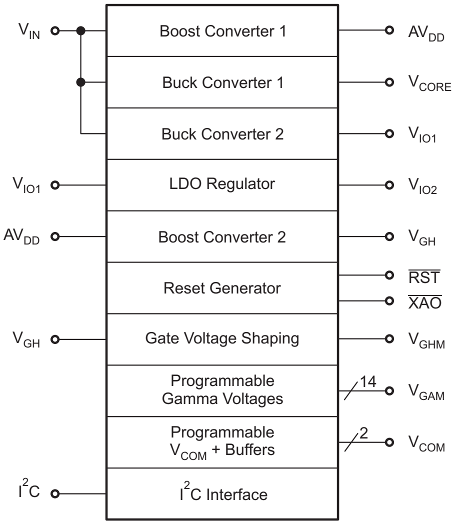
- **2.6 V to 6 V Input Voltage Range**
- **Synchronous Boost Converter (AV_{DD})**
- **Non-Synchronous Boost Converter with Temperature Compensation (V_{GH})**
- **Synchronous Buck Converter (V_{CORE})**
- **Synchronous Buck Converter (V_{IO1})**
- **Low Dropout Linear Regulator (V_{IO2})**
- **Programmable V_{COM} Calibrator with Two Integrated Buffer Amplifiers**
- **Gate Voltage Shaping**
- **Panel Discharge Signal ($\overline{XAO}$)**
- **System Reset Signal ($\overline{RST}$)**
- **14-Channel, 10-Bit Programmable Gamma Voltage Correction**
- **On-Chip EEPROM with Write Protect**
- **I^2C™ Interface**
- **Thermal Shutdown**
- **Supports GIP and Non-GIP Displays**
- **56-Ball, 3.16 mm x 3.45 mm 0.4 mm Pitch DSBGA**

1.2 Applications

- **Notebook PCs**
- **Tablet PCs**
- **Monitors**

1.3 Description

The TPS65642 is a compact LCD bias solution primarily intended for use in Notebook and Tablet PCs. The device comprises two boost converters to supply the LCD panel's source driver and gate driver/level shifter; two buck converters and an LDO linear regulator to supply the system's logic voltages; a programmable V_{COM} generator with two high-speed amplifiers; 14-channel gamma voltage correction; and a gate voltage shaping function.



2 Electrical Specifications

2.1 ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65642YFF	3.16 mm × 3.45 mm DSBGA, 0.4 mm pitch	TPS65642

(1) The device is supplied taped and reeled, with 3000 devices per reel.

2.2 ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage	VIN, SW2, VCORE, SW3, VIO1, VIO2 RSET, COMP, SCL, SDA, EN, FLK, WP, TCOMP, $\overline{\text{XAO}}$, $\overline{\text{RST}}$	–0.3	7	V
	AVDD, SW1, OUT1, OUT2, OUTA-OUTN	–0.3	12	V
	SW4	–0.3	36(2)	V
	POS1, NEG1, POS2, NEG2	–0.3	12(3)	V
	|POS1-NEG1|(4), |POS2-NEG2|(4)		2	V
	VGH, VGHM, RE	–0.3	40(5)	V
ESD Rating	Human Body Model		2000	V
	Machine Model		200	V
	Charged Device Model		700	V
Ambient temperature, T_A		-40	85	°C
Junction temperature, T_J		-40	150	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) V_{GH} supplies up to 40 V can be generated, but require an external cascode transistor or charge pump.

(3) For supply voltages less than 12 V, the absolute maximum input voltage is equal to the supply voltage.

(4) Differential input voltage.

(5) The combination of low temperatures and high V_{GH} voltages can cause increased leakage current through the RE pin. In GIP applications that do not use the gate-voltage shaping function it is recommended to leave the RE pin open to minimize this effect.

2.3 THERMAL INFORMATION(1)

THERMAL METRIC		TPS65642 YFF 56 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	45	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	
θ_{JB}	Junction-to-board thermal resistance	6.4	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	6.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

2.4 RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.6		6	V
BOOST CONVERTER 1					
AV_{DD}	Boost converter 1 output voltage range	6		9.1	V
IAV_{DD}	Boost converter 1 output current when 6 V ≥ V_{IN} ≥ 4 V			700(1)	mA
	Boost converter 1 output current when 3.63 V ≥ V_{IN} ≥ 2.64 V			400(1)	mA
L	Boost converter 1 inductor range	2.2	4.7	10	µH
C_{OUT}	Boost converter 1 output capacitance	10			µF
BOOST CONVERTER 2					
AV_{DD}	Input voltage range	6	8.1	9.1(2)	V
V_{GH}	Output voltage range	16	24	40(3)	V
I_{GH}	Output current		15	40	mA
L	Inductor	10	15		µH
C_{OUT}	Output capacitance	1	4.7		µF
R_{NTC}	Thermistor resistance at 25°C		10		kΩ
BUCK CONVERTER 1 (V_{CORE})					
V_{CORE}	Output voltage	1	1.1	1.3	V
I_{CORE}	Output current			600	mA
L	Inductor	1	2.2	4.7	µH
C_{OUT}	Output capacitance	4.7	10	22	µF
BUCK CONVERTER 2 (V_{IO1})					
V_{IO1}	Output voltage	1.7		2.5	V
I_{IO1}	Output current			200(4)	mA
L	Inductor	1	2.2	4.7	µH
C_{OUT}	Output capacitance	4.7	10	22	µF
LDO Regulator (V_{IO2})					
V_{IO2}	Output voltage	1.7		1.8	V
I_{IO}	Output current			200	mA
C_{OUT}	Output capacitance		4.7	10	µF
PROGRAMMABLE VCOM					
I_{SET}	Programmable V_{COM} set current		50		µA
PROGRAMMABLE GAMMA CORRECTION					
I_{GAM}	Output current per channel	-100		100	µA
C_{GAM}	Output capacitance			50	pF

(1) This value includes the current that must be supplied to the input of boost converter 2.
(2) $V_{GH}-AV_{DD}$ must be greater than 9 V.
(3) Output voltages greater than 36 V require an external cascode transistor.
(4) This value includes the current supplied to the input of the linear regulator.

2.5 ELECTRICAL CHARACTERISTICS

V_{IN} = 3.3 V, V_{CORE} = 1.1 V, V_{IO1} = 1.7 V, V_{IO2} = 1.8 V(1), AV_{DD} = 8.1 V, V_{GH} = 24 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{IN}	Supply current into VIN pins	Converters not switching			1.9	3	mA
	Supply current into AVDD pins	Pin G5.			0.1	1	mA
		Pin B7. No load on gamma reference outputs			4.3	6	
		Pin F4. No load on op-amp outputs			4.0	7.5	
	Supply current into VGH	No load on VGHM			0.1	1	mA
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising		2.3	2.42	2.5	V
		V_{IN} falling		2.1	2.19	2.4	
	Hysteresis				0.23		
CONTROL PINS (EN, FLK, WP)							
V_{IH}	EN high-level input voltage threshold	EN rising	V_{IN} = 2.64 V		1.0	1.8	V
			V_{IN} = 3.3 V		1.1	1.8	
			V_{IN} = 6 V		1.7	1.8	
V_{IL}	EN low-level input voltage threshold	EN falling	V_{IN} = 2.64 V	0.7	0.9		V
			V_{IN} = 3.3 V	0.7	1.0		
			V_{IN} = 6 V	0.7	1.6		
I_{IH}	EN high-level input current	EN = 2.5 V		–100		100	nA
I_{IL}	EN low-level input current	EN = 0 V		–100		100	nA
V_{IH}	FLK high-level input voltage threshold	FLK rising	V_{IN} = 2.64 V		0.9	1.8	V
			V_{IN} = 3.3 V		1	1.8	
			V_{IN} = 6 V		1.4	1.8	
V_{IL}	FLK low-level input voltage threshold	FLK falling	V_{IN} = 2.64 V	0.6	0.8		V
			V_{IN} = 3.3 V	0.6	0.9		
			V_{IN} = 6 V	0.6	1.3		
I_{IH}	FLK high-level input current	FLK = 2.5 V		–100		100	nA
I_{IL}	FLK-low-level input current	FLK = 0 V		–100		100	nA
V_{IH}	WP high-level input voltage threshold	WP rising	V_{IN} = 2.64 V		1	1.8	V
			V_{IN} = 3.3 V		1.1	1.8	
			V_{IN} = 6 V		1.7	1.8	
V_{IL}	WP low-level input voltage threshold	WP falling	V_{IN} = 2.64 V	0.7	0.9		V
			V_{IN} = 3.3 V	0.7	1		
			V_{IN} = 6 V	0.7	1.6		
$R_{PULL-UP}$	WP internal pull-up resistance			30	52	75	kΩ
BOOST CONVERTER 1 (AV_{DD})							
AV_{DD}	Output voltage range			6		9.1	V
	Tolerance			–1%		1%	
V_{UVP}	Undervoltage protection threshold	AV_{DD} falling		65	70	75	% of AV_{DD}
V_{SCP}	Short-circuit threshold	AV_{DD} falling		25	30	35	% of AV_{DD}
I_{LK}	Switch leakage current	V_{SW} = V_{IN} = 3.3 V, EN = 0 V, T_J = –40°C to 85°C				10	µA
$r_{DS(ON)}$	Switch ON resistance	I_{SW} = 1 A			114	250	mΩ
I_{LIM}	Switch current limit			2.5	3.0	3.5	A
$r_{DS(ON)}$	Rectifier ON resistance	I_{SW} = 1 A			242	400	mΩ
f_{SW}	Switching frequency (see Figure 4-15)	FREQ = 0			750		kHz
		FREQ = 1			1200		
$r_{DS(ON)}$	Discharge ON resistance	I_{AVDD} = 10 mA			76	100	Ω

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(1) When V_{IO1}= 1.7 V or 1.8 V, the LDO regulator is disabled. When V_{IO1} = 2.5 V, the LDO regulator is enabled.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.3 V, V_{CORE} = 1.1 V, V_{IO1} = 1.7 V, V_{IO2} = 1.8 V(1), AV_{DD} = 8.1 V, V_{GH} = 24 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BUCK CONVERTER 1 (V_{CORE})							
V_{CORE}	Output voltage			1	1.1	1.3	V
	Tolerance			–3%		3%	
V_{UVP}	Undervoltage protection threshold	V_{CORE} falling		65	70	75	% of V_{CORE}
V_{SCP}	Short-circuit threshold	V_{CORE} falling		25	30	35	% of V_{CORE}
I_{LIMA}	Switch current limit	I_{SW} ramps from 0 A to 2 A		0.8	1.0	1.2	A
$r_{DS(ON)}$	Switch ON resistance	High-side, I_{SW} = I_{LIM}			183	310	mΩ
		Low-side, I_{SW} = 1 A			95	150	
t_{OFF}	Off time	V_{IN} = 3.3 V		260	370	480	ns
		V_{IN} = 5 V		380	560	750	
BUCK CONVERTER 2 (V_{IO1})							
V_{IO1}	Output voltage			1.7	1.8	2.5	V
	Tolerance			–3%		3%	
V_{UVP}	Undervoltage protection threshold	V_{IO1} falling		65	70	75	% of V_{IO1}
V_{SCP}	Short-circuit threshold	V_{IO1} falling		25	30	35	% of V_{IO1}
I_{LIM}	High-side switch current limit	High-side, I_{SW} ramps from 0 A to 2 A		0.8	1	1.2	A
$r_{DS(ON)}$	High-side switch ON resistance	I_{SW} = I_{LIM}			183	350	mΩ
	Low-side switch ON resistance	I_{SW} = 1 A			255	400	
t_{OFF}	Off time	V_{IN} = 3.3		170	250	330	µs
		V_{IN} = 5 V		250	370	500	
$r_{DS(ON)}$	Discharge ON resistance	Measured with 10 mA			14.6	50	Ω
LINEAR REGULATOR (V_{IO2})(2)							
V_{IO2}	Output voltage	I_{IO2} = 1 mA		1.7	1.8	1.8	V
	Tolerance			–3%		3%	
V_{UVP}	Undervoltage protection threshold	V_{IO2} falling		65	70	75	% of V_{IO2}
V_{SCP}	Short circuit threshold	V_{IO2} falling		25	30	35	% of V_{IO2}
BOOST CONVERTER 2 (V_{GH})							
V_{GH}	Output voltage range			16		40(3)	V
	Tolerance			–3%		3%	
V_{UVP}	Undervoltage protection threshold	V_{GH} falling		65	70	75	% of V_{GH}
V_{SCP}	Short-circuit threshold	V_{GH} falling		25	30	35	% of V_{GH}
I_{LK}	Switch leakage current	V_{EN}=0 V; V_{SW4}=36 V				10	µA
$r_{DS(ON)}$	Switch ON resistance	I_{SW}=1 A			0.41	1	Ω
$t_{ON(MAX)}$	Maximum t_{ON} time			1	1.67	2.5	µs
t_{OFF}	t_{OFF} time			1.5	2.11	3	µs
I_{TCOMP}	Thermistor reference current	I_{SET} = 50 µA, V_{TCOMP} = 1 V	85°C	48		54	µA
			25 °C		50		
RESET ($\overline{RST}$)							
t_{RESET}	Reset pulse duration range	Measured from end of V_{CORE}'s ramp to 50% of $\overline{RST}$'s rising edge with a 10k pull-up resistor.		2		16	ms
	Tolerance			–20%		30%	
V_{OL}	Low output voltage	$I_{\overline{RST}}$ = 1 mA (sinking)			0.27	0.5	V
I_{OH}	High output current	$V_{\overline{RST}}$=2.5 V		–1		1	µA
PROGRAMMABLE GAMMA CORRECTION							
V_{DROPH}	High-side output voltage drop	Code = 1023; load = 10 µA, sourcing			5.6	100	mV
		Code = 1023; load = 100 µA, sourcing			44.2	200	
V_{DROPL}	Low-side output voltage drop	Code = 0; load = 10 µA, sinking			49.1	100	mV
		Code = 0; load = 100 µA, sinking			65.5	200	

(2) LDO is enabled, when V_{IO1} = 2.5 V.

(3) Output voltages greater than 36V require an external cascode transistor or charge pump circuit.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.3 V, V_{CORE} = 1.1 V, V_{IO1} = 1.7 V, V_{IO2} = 1.8 V(1), AV_{DD} = 8.1 V, V_{GH} = 24 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Offset	Code = 512		–25		25	mV
INL	Integral nonlinearity	No load, V_{GAMH} = AV_{DD} – 0.25 V, V_{GAML} = 0.25 V		–3.6		5.9	LSB
DNL	Differential nonlinearity	No load, V_{GAMH} = AV_{DD} – 0.25 V, V_{GAML} = 0.25 V		–1		1.5	LSB
PROGRAMMABLE V_{COM} CALIBRATOR							
SET_{ZSE}	Set zero-scale error			–1		1	LSB
SET_{FSE}	Set full-scale error			–7		7	LSB
V_{RSET}	Voltage on RSET pin	I_{RSET}=50 µA		–2%	1.25	2%	V
DNL	Differential nonlinearity			–1		1.5	LSB
A_{VOL}	Open loop gain	V_{CM} = AV_{DD}/2, V_{OUT1} = 2 V, V_{OUT2} = AV_{DD} – 2 V, R_L= ∞		70	91		dB
V_{IO}	Input offset voltage	V_{CM} = AV_{DD}/2, V_{OUT} = AV_{DD}/2		–15		15	mV
I_B	Input bias current	V_{CM} = AV_{DD}/2, V_{OUT} = AV_{DD}/2		–150		150	nA
V_{DROPH}	High-side voltage drop	V_{POS} = AV_{DD}/2, V_{NEG} = AV_{DD}/2–1 V, I_{OUT} = 10 mA sourcing			0.05	0.1	V
V_{DROPL}	Low-side voltage drop	V_{POS} = AV_{DD}/2, V_{NEG} = AV_{DD}/2+1 V, I_{OUT} = 10 mA sinking			0.03	0.1	V
I_{PK}	High-side peak output current	V_{CM} = AV_{DD}/2, V_{SIGNAL} = 2 V_{PP}, open-loop, R_L = ∞, C_L = 1 µF		200	294		mA
	Low-side peak output current				–349	–200	
CMRR	Common-mode rejection ratio	V_{CM1} = 2 V, V_{CM2} = AV_{DD}–2 V, V_{OUT} = AV_{DD}/2		40	78		dB
PSRR	Power supply rejection ratio	AV_{DD1} = 6 V, AV_{DD2} = 9.1 V, V_{CM} = 3 V, V_{OUT} = 3 V		40	110		dB
SR	Slew rate	Open-loop, V_{POS} = AV_{DD}/2±1 V	T_A = –40°C	18	30		V/µs
			T_A = 25°C to 85°C	25	38		
GATE VOLTAGE SHAPING							
$r_{DS(ON)}$	VGH to VGHM ON resistance	V_{GH} = 24 V, I_{GHM} = 10 mA, FLK = 2.5 V			12	25	Ω
	VGHM to RE ON resistance	V_{GHM} = 24 V, I_{GHM} = 10 mA, FLK = 0 V			12	25	
		V_{GHM} = 6 V, I_{GHM} = 10 mA, FLK = 0 V			12	25	
t_{PLH}	Propagation delay	V_{GHM} rising, 2.5 V, 50% thresholds, C_{OUT} = 150 pF, R_E = 0 Ω			72	175	ns
t_{PHL}		V_{GHM} falling, 2.5 V, 50% thresholds, C_{OUT} = 150 pF, R_E = 0 Ω			81	200	
PANEL RESET / LCD BIAS READY ($\overline{XAO}$)							
V_{OL}	Low output voltage	$I_{\overline{XAO}}$ = 1 mA (sinking)			0.23	0.5	V
I_{OH}	High output current	$V_{\overline{XAO}}$ = 2.5 V				1	µA
V_{DET}	$\overline{XAO}$ threshold voltage	$\overline{XAO}$ falling		2.2		3.9	V
	Tolerance			–2.5%		2.5%	
	Hysteresis	$\overline{XAO}$ rising		3%	6.3%	11%	
TIMING							
t_{DLY1}	Boost converter 1 delay range			0		70	ms
	Tolerance			–20%		30%	
t_{DLY6}	Gate voltage shaping / LCD bias ready delay range			0		35	ms
	Tolerance			–20%		30%	
t_{SS1}	Soft-start ramp time	V_{CORE}, V_{IO1}, V_{IO2}		0.5		4	ms
	Tolerance			–20%		30%	
t_{SS2}	Soft-start ramp time	AV_{DD}, V_{GH}		4.0		7.5	ms
	Tolerance			–20%		30%	
t_{UVP}	Undervoltage protection timeout			40	50	65	ms
I^2C INTERFACE							
ADDR	Configuration parameters slave address				74h		
	Programmable VCOM slave address				4Fh		
V_{IL}	Low level input voltage	Rising Edge, standard and fast mode				0.75	V

ELECTRICAL CHARACTERISTICS *(continued)*

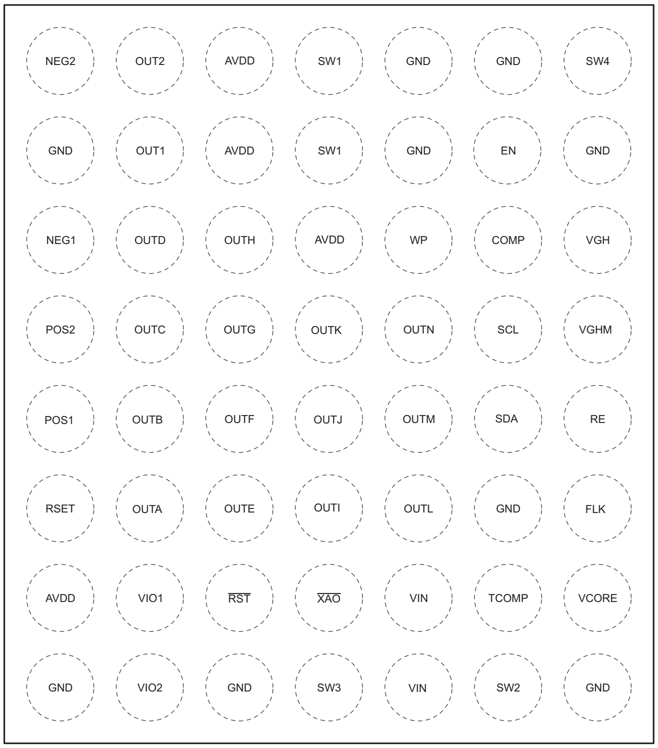
V_{IN} = 3.3 V, V_{CORE} = 1.1 V, V_{IO1} = 1.7 V, V_{IO2} = 1.8 V(1), AV_{DD} = 8.1 V, V_{GH} = 24 V, T_A = −40°C to 85°C. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	Rising edge, standard and fast modes	1.75			V
V_{HYS}	Hysteresis	Applicable to fast mode only	125			mV
V_{OL}	Low level output voltage	Sinking 3 mA			500	mV
C_I	Input capacitance				10	pF
f_{SCL}	Clock frequency	Standard mode			100	kHz
		Fast mode			400	
t_{LOW}	Clock low period	Standard mode	4.7			µs
		Fast mode	1.3			
t_{HIGH}	Clock high period	Standard mode	4.0			µs
		Fast mode	0.6			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
$t_{hd:STA}$	Hold time for a repeated START condition	Standard mode	4			µs
		Fast mode	0.6			
$t_{su:STA}$	Set-up time for a repeated START condition	Standard mode	4			µs
		Fast mode	0.6			
$t_{su:DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
$t_{hd:DAT}$	Data hold time	Standard mode	0.05		3.45	µs
		Fast mode	0.05		0.9	
t_{RCL1}	Rise time of SCL after a repeated START condition and after an ACK bit	Standard mode	$20+0.1C_B$		1000	ns
		Fast mode	$20+0.1C_B$		1000	
t_{RCL}	Rise time of SCL	Standard mode	$20+0.1C_B$		1000	ns
		Fast mode	$20+0.1C_B$		300	
t_{FCL}	Fall time of SCL	Standard mode	$20+0.1C_B$		300	ns
		Fast mode	$20+0.1C_B$		300	
t_{RDA}	Rise time of SDA	Standard mode	$20+0.1C_B$		1000	ns
		Fast mode	$20+0.1C_B$		300	
t_{FDA}	Fall time of SDA	Standard mode	$20+0.1C_B$		300	ns
		Fast mode	$20+0.1C_B$		300	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
C_B	Capacitive load on SDA and SCL	Standard mode			400	pF
		Fast mode			400	
EEPROM						
N_{WRITE}	Number of write cycles		1000			
t_{WRITE}	Write time				100	ms
	Data retention	Storage temperature=150 °C	100			1000 hrs
THERMAL SHUTDOWN						
T_{SD}(4)	Thermal shutdown threshold		120	150	180	°C

(4) Once triggered, thermal shutdown will remain in the shutdown state until the device is powered down.

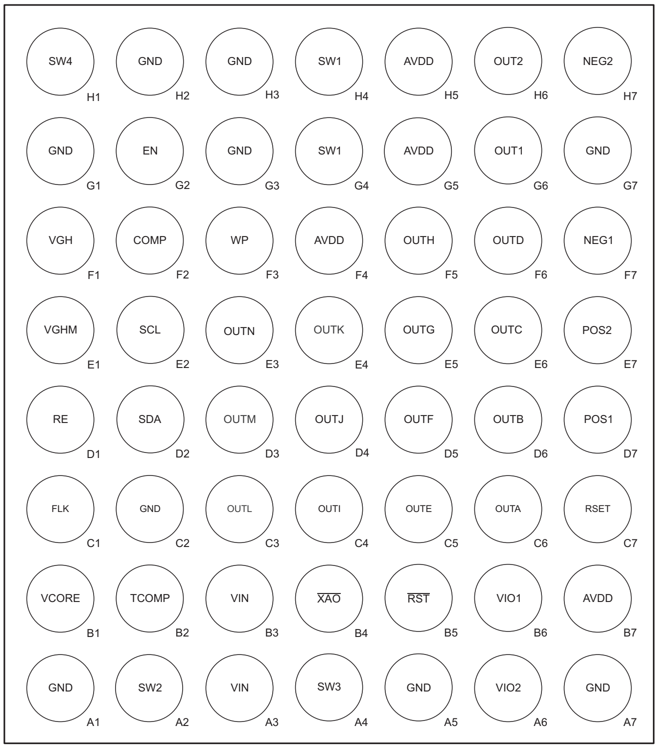
3 Pin Description

3.1 Pin Assignment



NEG2	OUT2	AVDD	SW1	GND	GND	SW4
GND	OUT1	AVDD	SW1	GND	EN	GND
NEG1	OUTD	OUTH	AVDD	WP	COMP	VGH
POS2	OUTC	OUTG	OUTK	OUTN	SCL	VGHM
POS1	OUTB	OUTF	OUTJ	OUTM	SDA	RE
RSET	OUTA	OUTE	OUTI	OUTL	GND	FLK
AVDD	VIO1	$\overline{\text{RST}}$	$\overline{\text{XAO}}$	VIN	TCOMP	VCORE
GND	VIO2	GND	SW3	VIN	SW2	GND

TOP VIEW



SW4 H1	GND H2	GND H3	SW1 H4	AVDD H5	OUT2 H6	NEG2 H7
GND G1	EN G2	GND G3	SW1 G4	AVDD G5	OUT1 G6	GND G7
VGH F1	COMP F2	WP F3	AVDD F4	OUTH F5	OUTD F6	NEG1 F7
VGHM E1	SCL E2	OUTN E3	OUTK E4	OUTG E5	OUTC E6	POS2 E7
RE D1	SDA D2	OUTM D3	OUTJ D4	OUTF D5	OUTB D6	POS1 D7
FLK C1	GND C2	OUTL C3	OUTI C4	OUTE C5	OUTA C6	RSET C7
VCORE B1	TCOMP B2	VIN B3	$\overline{\text{XAO}}$ B4	$\overline{\text{RST}}$ B5	VIO1 B6	AVDD B7
GND A1	SW2 A2	VIN A3	SW3 A4	GND A5	VIO2 A6	GND A7

BOTTOM VIEW

3.2 Pin Assignment

Table 3-1. PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	A1	P	Ground.
SW2	A2	O	Buck converter 1 (V_{CORE}) switch pin.
VIN	A3	P	Supply voltage.
SW3	A4	O	Buck converter 2 (V_{IO1}) switch pin.
GND	A5	P	Ground.
VIO2	A6	O	Linear regulator (V_{IO2}) output and output sense.
GND	A7	P	Ground.
VCORE	B1	I	Buck converter 1 (V_{CORE}) output sense.
TCOMP	B2	I	Boost converter 2 (V_{GH}) thermistor network connection.
VIN	B3	P	Supply voltage.
$\overline{\text{XAO}}$	B4	O	Panel discharge.
$\overline{\text{RST}}$	B5	O	System reset.
VIO1	B6	I	Buck converter 2 (V_{IO1}) output sense. (Internally connected as supply voltage for LDO regulator.)
AVDD	B7	I	Boost converter 1 (AV_{DD}) output sense. (Internally connected as supply voltage for programmable gamma correction.)
FLK	C1	I	Gate voltage shaping flicker clock.
GND	C2	P	Ground.
OUTL	C3	O	Gamma correction.

Table 3-1. PIN DESCRIPTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUTI	C4	O	Gamma correction.
OUTE	C5	O	Gamma correction.
OUTA	C6	O	Gamma correction.
RSET	C7	O	Reference current-setting resistor connection.
RE	D1	O	Gate voltage shaping discharge resistor connection.
SDA	D2	I/O	I^2C serial data.
OUTM	D3	O	Gamma correction.
OUTJ	D4	O	Gamma correction.
OUTF	D5	O	Gamma correction.
OUTB	D6	O	Gamma correction.
POS1	D7	I	V_{COM} 1 non-inverting input.
VGHM	E1	O	Gate voltage shaping output.
SCL	E2	I/O	I^2C serial clock.
OUTN	E3	O	Gamma correction.
OUTK	E4	O	Gamma correction.
OUTG	E5	O	Gamma correction.
OUTC	E6	O	Gamma correction.
POS2	E7	I	V_{COM2} non-inverting input.
VGH	F1	I	Boost converter 2 (V_{GH}) output sense. (Internally connected as supply voltage for the gate voltage shaping.)
COMP	F2	O	Boost converter 1 (AV_{DD}) compensation network connection.
WP	F3	I	EEPROM write protect.
AVDD	F4	I	V_{COM1} and V_{COM2} supply voltage.
OUTH	F5	O	Gamma correction.
OUTD	F6	O	Gamma correction.
NEG1	F7	I	V_{COM1} inverting input.
GND	G1	P	Ground.
EN	G2	I	Boost converter 1 (AV_{DD}) enable.
GND	G3	P	Ground.
SW1	G4	O	Boost converter 1 (AV_{DD}) switch pin.
AVDD	G5	O	Boost converter 1 (AV_{DD}) rectifier output.
OUT1	G6	O	V_{COM1} output.
GND	G7	P	Ground.
SW4	H1	O	Boost converter 2 (V_{GH}) switch pin.
GND	H2	P	Ground
GND	H3	P	Ground.
SW1	H4	O	Boost converter 1 (AV_{DD}) switch pin.
AVDD	H5	O	Boost converter 1 (AV_{DD}) rectifier output.
OUT2	H6	O	V_{COM2} output.
NEG2	H7	I	V_{COM2} inverting input.

4 Typical Characteristics

4.1 Table of Graphs

PARAMETER		TEST CONDITIONS		FIGURE
Boost Converter 1 (AV_{DD})	Efficiency	AV_{DD} = 6 V, 8 V, 9.1 V FREQ = 0, FREQ = 1	V_{IN} = 3.3 V	Figure 4-1
			V_{IN} = 5 V	Figure 4-2
	Line Regulation	V_{IN} = 2.6 V to 6.0 V, AV_{DD} = 8 V, IAV_{DD} = 100 mA		Figure 4-3
	Load Regulation	V_{IN} = 3.4 V, 5.0 V, AV_{DD} = 8 V, IAV_{DD} = 1 mA to 500 mA		Figure 4-4
	Line Transient Response	V_{IN} = 3 V to 4.8 V (dV/dt = 7.5 V/ms), AV_{DD} = 8.1 V	R_L = 82 Ω	Figure 4-5
			R_L = 33 Ω	Figure 4-6
	Load Transient Response	AV_{DD} = 8.1 V, IAV_{DD} = 20 mA – 200 mA	V_{IN} = 3.3 V	Figure 4-7
			V_{IN} = 5.0 V	Figure 4-8
	Output Voltage Ripple	AV_{DD} = 8.1 V, R_L = 82 Ω	V_{IN}= 3.3 V	Figure 4-9
			V_{IN} = 5.0 V	Figure 4-10
	Switching Waveforms	V_{IN} = 3.3 V, AV_{DD} = 8.1 V FREQ = 0	R_L = 820 Ω	Figure 4-11
			R_L = 82 Ω	Figure 4-12
		V_{IN}= 3.3 V, AV_{DD}= 8.1 V FREQ = 1	R_L = 820 Ω	Figure 4-13
			R_L = 82 Ω	Figure 4-14
	Switching Frequency	V_{IN} = 2.6 V to 6 V, AV_{DD} = 6 V, 8 V, 9.1 V	R_L = 82 Ω	Figure 4-15
Buck Converter 1 (V_{CORE})	Efficiency	V_{CORE} = 1 V, 1.1 V, 1.2 V, 1.3 V, I_{CORE} = 1 mA to 500 mA	V_{IN} = 3.4 V	Figure 4-16
			V_{IN} = 5.0 V	Figure 4-17
	Line Regulation	V_{IN} = 2.6 V to 6.V, V_{CORE} = 1.1 V, I_{CORE} = 300 mA		Figure 4-18
	Load Regulation	V_{IN} = 3.4 V, 5 V, V_{CORE} = 1.1 V, I_{CORE} = 1 mA to 700 mA		Figure 4-19
	Line Transient Response	V_{IN} = 3 V to 4.8 V (dV/dt = 7.5 V/ms), V_{CORE} = 1.1 V, Load = 3.9 Ω		Figure 4-20
	Load Transient Response	V_{CORE} = 1.1 V, I_{CORE} = 50 mA to 200 mA	V_{IN} = 3.3 V	Figure 4-20
			V_{IN} = 5 V	Figure 4-22
	Output Voltage Ripple	V_{CORE} = 1.1 V, R_L = 3.9 Ω	V_{IN} = 3.3 V	Figure 4-23
			V_{IN} = 5 V	Figure 4-24
	Switching Waveforms	V_{IN} = 3.3 V, V_{CORE} = 1.1 V	R_L = 120 Ω	Figure 4-25
			R_L = 3.9 Ω	Figure 4-26
	Switching Frequency	V_{IN} = 2.6 V to 6 V, V_{CORE} = 1.1 V	R_L = 12 Ω	Figure 4-27
Buck Converter 2 (V_{IO1})	Efficiency	V_{IO1} = 1.7 V, 1.8 V, 2.5 V, I_{IO1} = 1 mA to 500 mA	V_{IN} = 3.3 V	Figure 4-28
			V_{IN} = 5 V	Figure 4-29
	Line Regulation	V_{IN} = 2.6 V to 6 V, V_{IO1} = 1.7 V, I_{IO1} = 100 mA		Figure 4-30
	Load Regulation	V_{IN} = 3.4 V, 5 V, V_{IO1} = 1.7 V, I_{IO1} = 1 mA to 400 mA		Figure 4-31
	Line Transient Response	V_{IN} = 3 V to 4.8 V (dV/dt = 7.5 V/ms), V_{IO1} = 1.7 V,R_L = 27 Ω		Figure 4-32
	Load Transient Response	V_{IO1} = 1.7 V, I_{IO1} = 50 mA to 100 mA	V_{IN} = 3.3 V	Figure 4-33
			V_{IN} = 5 V	Figure 4-34
	Output Voltage Ripple	V_{IO1} = 1.7 V, R_L = 27 Ω	V_{IN} = 3.3 V	Figure 4-35
			V_{IN} = 5 V	Figure 4-36
	Switching Waveforms	V_{IN} =3 .3 V, V_{IO1} = 1.7 V	R_L = 270 Ω	Figure 4-37
			R_L = 27Ω	Figure 4-38
	Switching Frequency	V_{IN} = 2.6 V to 6 V, V_{IO1} = 1.7 V	R_L = 27 Ω	Figure 4-39
LDO Regulator (V_{IO2})	Load Regulation	V_{IO1} = 2.5 V, V_{IO2} = 1.8 V, I_{IO2} = 1 mA to 100 mA		Figure 4-40
	Line Transient Response	V_{IN} = 3 V to 4.8 V (dV/dt = 7.5 V/ms), V_{IO1} = 2.5 V, V_{IO2} = 1.8 V, R_L = 27 Ω		Figure 4-41
	Load Transient Response	V_{IN} = 3.3 V, V_{IO1} = 2.5 V, V_{IO2} = 1.8 V, I_{IO2} = 50 mA to 150 mA		Figure 4-42
	Output Voltage Ripple	V_{IN} = 3.3 V, V_{IO1} = 2.5 V, V_{IO2} = 1.8 V, R_L = 27 Ω		Figure 4-43

PARAMETER		TEST CONDITIONS		FIGURE
Boost Converter 2 (V_{GH})	Efficiency	AV_{DD} = 8.1 V, V_{GH} = 20 V, 24 V, 28 V, 31 V		Figure 4-44
	Line Regulation	AV_{DD} = 6 V to 9.1 V, I_{GH} = 10 mA		Figure 4-45
	Load Regulation	AV_{DD} = 8.1 V, V_{GH} = 24 V, I_{GH} = 1 mA to 50 mA		Figure 4-46
	Line Transient Response	V_{IN} = 3V to 4.8 V (dV/dt = 7.5 V/ms), V_{GH} = 24 V	R_L = 4.8 kΩ	Figure 4-47
			R_L = 1.2 kΩ	Figure 4-48
	Load Transient Response	V_{IN} = 5 V, AV_{DD} = 8.1 V, V_{GH} = 24 V	I_{GH} = 5 mA to 10 mA	Figure 4-49
			I_{GH} = 10 mA to 30 mA	Figure 4-50
	Output Voltage Ripple	V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{GH} = 24 V	R_L = 4.8 kΩ	Figure 4-51
			R_L = 1.2 kΩ	Figure 4-52
	Switching Waveforms	V_{IN} = 3.3 V, AV_{DD} = 8.1 V, Load = 82 Ω, V_{GH} = 24 V	R_L = 4.8 kΩ	Figure 4-53
			R_L = 1.2 kΩ	Figure 4-54
	Switching Frequency	V_{IN} = 3.3 V, AV_{DD} = 7 V, 8 V, 9 V, V_{GH} = 16 V to 31 V		Figure 4-55
Power-Up Behavior	V_{IN}, V_{IO1}, V_{IO2}, V_{CORE}	V_{IN} = 3.3 V, t_{SS1} = 0.5 ms, V_{IO1} = 2.5 V, R_L = 27 Ω, V_{IO2} = 1.8 V, R_L = ∞, V_{CORE} = 1.1 V	R_L = 3.9 Ω	Figure 4-56
	EN, AV_{DD}, V_{GH}	V_{IN} = 3.3 V, t_{SS2} = 4.0 ms, AV_{DD} = 8.1 V, R_L = 33 Ω, V_{GH} = 24 V, 1.2 kΩ	t_{DLY1} = 0 ms	Figure 4-57
			t_{DLY1} = 10 ms	Figure 4-58
	$\overline{XAO}$, AV_{DD}, V_{GH}, V_{GHM}	V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 33 Ω, V_{GH} = 24 V, R_L = 1.2 kΩ, GIP = 0	t_{DLY6} = 0 ms	Figure 4-59
			t_{DLY6} = 10 ms	Figure 4-60
	$\overline{XAO}$, AV_{DD}, V_{GH}, V_{GHM}	V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 33 Ω, V_{GH} = 24 V, R_L = 1.2 kΩ, GIP = 1	t_{DLY6} = 0 ms	Figure 4-61
			t_{DLY6} = 10 ms	Figure 4-62
	AV_{DD}, V_{GH}, V_{COM}, V_{GAMA}	V_{IN} = 3.3 V, AV_{DD} = 8.1 V, V_{GH} = 24 V, V_{COM} = 4.05 V, V_{GAMA} = 4.05 V		Figure 4-63
Power-Down Behavior	$\overline{RST}$, V_{IO1}, V_{IO2}, V_{CORE}	V_{DET} = 2.5 V	R_{MODE} = 0	Figure 4-64
			R_{MODE} = 1	Figure 4-65
	V_{IN}, $\overline{XAO}$, AV_{DD}, V_{GHM}	GIP = 0		Figure 4-66
	AV_{DD}, V_{GH}, V_{COM}, V_{GAMA}		SMODE = 0	Figure 4-67
			SMODE = 1	Figure 4-68
Gate Voltage Shaping	FLK, V_{GHM}	V_{IN} = 3.3 V, R_E = 1 kΩ, C_L = 10 nF, AV_{DD} = 8.1 V, R_L= 33 Ω, V_{GH} = 24 V, R_L = 1.2 kΩ		Figure 4-69
Op-Amp	Large-Signal Response	V_{POS} = 3.8 V ± 0.5 V		Figure 4-70
	Small-Signal Bandwidth	AV_{DD} = 8.1 V, V_{POS2} = 63 mV_{PP}, A_V = +1, R_F = 0 Ω		Figure 4-71
	Gain Bandwidth	AV_{DD} = 8.1 V, V_{POS2} = 63 mV_{PP}, A_V = +1, R_F = 0 Ω		Figure 4-72
	Peak Output Current	AV_{DD} = 8.1 V, R_L = 2 kΩ to AV_{DD}/2, C_L = 1 µF		Figure 4-73
	Line Transient Response	V_{IN} = 3.0 V to 4.8 V (dV/dt = 7.5 V/ms), AV_{DD} = 8.1 V, V_{COM} = 4 V, R_L = ∞		Figure 4-74
	Output Voltage Ripple and Noise	V_{IN} = 3.3 V, 8.1 V, R_L = 82 Ω, V_{COM} = 4 V, R_L = ∞		Figure 4-75
Programmable Gamma	Dynamic Response	AV_{DD} = 8.1 V, R_L = 909 kΩ, C_L = 55 pF	GAMA = 0x0ff/0x2ff	Figure 4-76
			GAMA = 0x2ff/0x0ff	Figure 4-77
	Line Transient Response	V_{IN} = 3.0 V to 4.8 V (dV/dt = 7.5 V/ms), AV_{DD} = 8.1 V	GAMA = 0x0ff	Figure 4-78
			GAMA = 0x1ff	Figure 4-79
			GAMA = 0x2ff	Figure 4-80
	Output Voltage Ripple and Noise	V_{IN} = 3.3 V, 8.1 V, R_L = 82 Ω	GAMA = 0x1ff	Figure 4-81

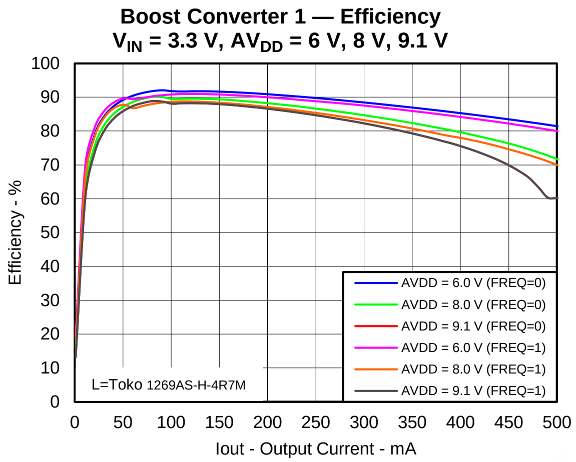

Boost Converter 1 — Efficiency
V_{IN} = 3.3 V, AV_{DD} = 6 V, 8 V, 9.1 V

Figure 4-1.

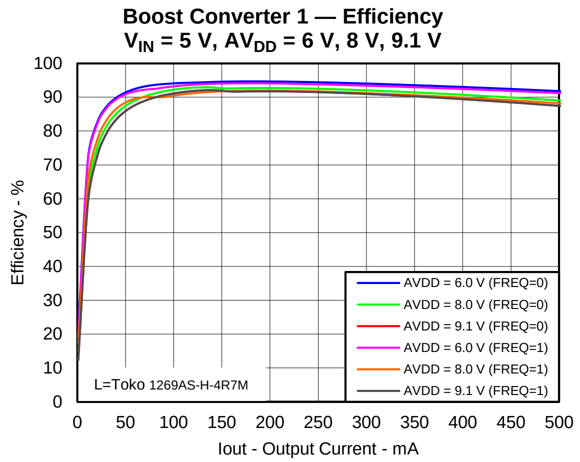

Boost Converter 1 — Efficiency
V_{IN} = 5 V, AV_{DD} = 6 V, 8 V, 9.1 V

Figure 4-2.

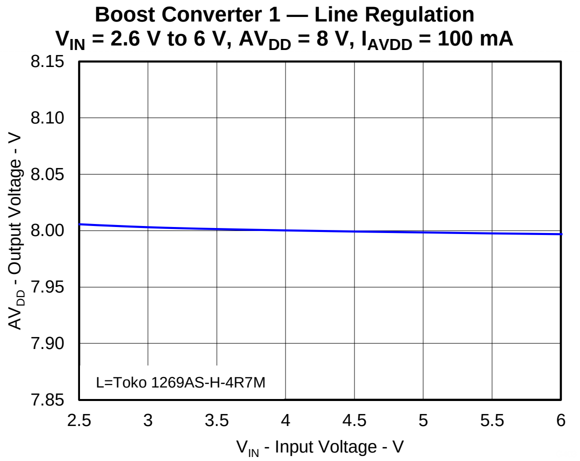

Boost Converter 1 — Line Regulation
V_{IN} = 2.6 V to 6 V, AV_{DD} = 8 V, I_{AVDD} = 100 mA

Figure 4-3.

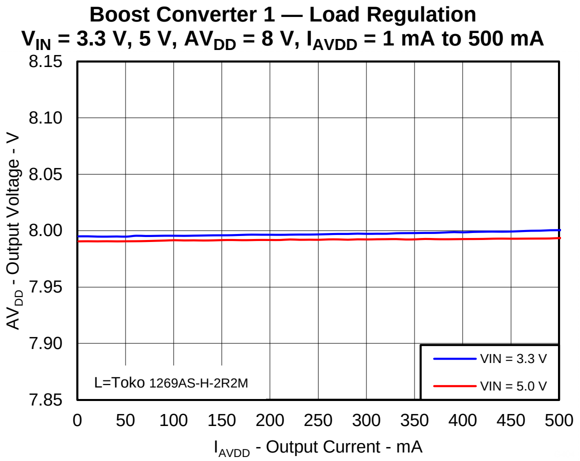

Boost Converter 1 — Load Regulation
V_{IN} = 3.3 V, 5 V, AV_{DD} = 8 V, I_{AVDD} = 1 mA to 500 mA

Figure 4-4.

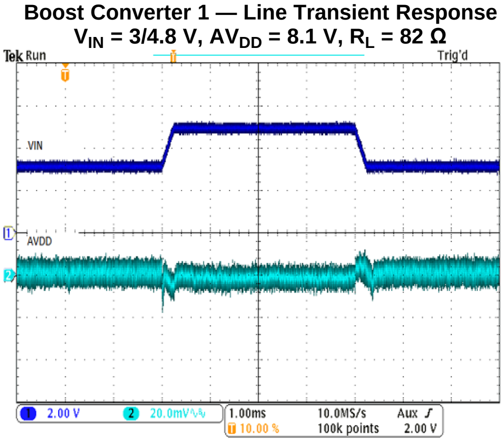

Boost Converter 1 — Line Transient Response
V_{IN} = 3/4.8 V, AV_{DD} = 8.1 V, R_L = 82 Ω

Figure 4-5.

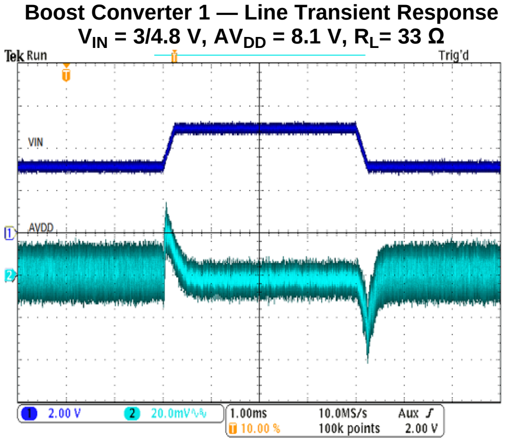

Boost Converter 1 — Line Transient Response
V_{IN} = 3/4.8 V, AV_{DD} = 8.1 V, R_L= 33 Ω

Figure 4-6.

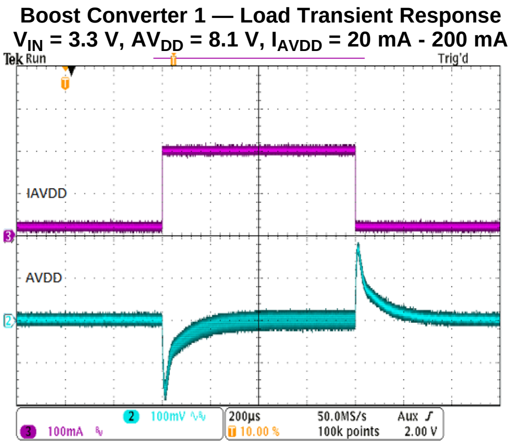

Boost Converter 1 — Load Transient Response
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, I_{AVDD} = 20 mA - 200 mA

Figure 4-7.

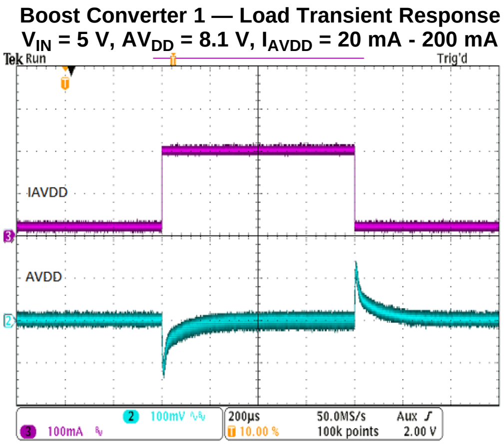

Boost Converter 1 — Load Transient Response
V_{IN} = 5 V, AV_{DD} = 8.1 V, I_{AVDD} = 20 mA - 200 mA

Figure 4-8.

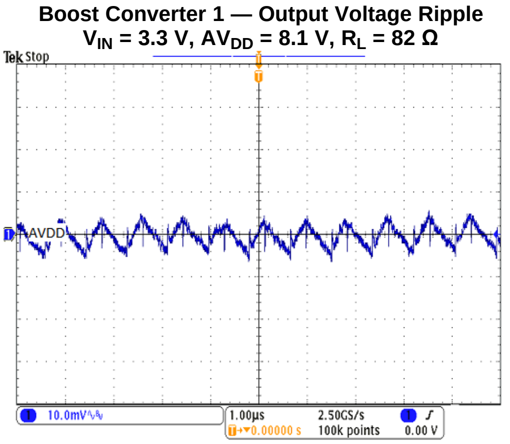

Boost Converter 1 — Output Voltage Ripple
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω

Figure 4-9.

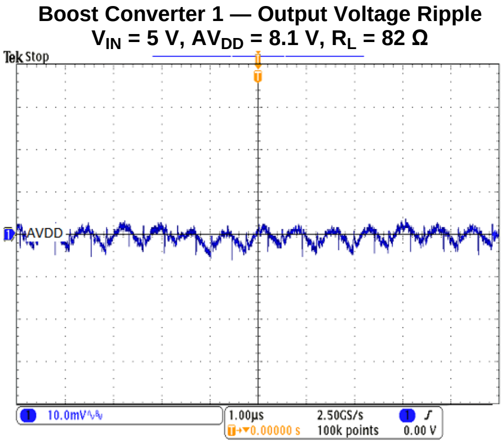

Boost Converter 1 — Output Voltage Ripple
V_{IN} = 5 V, AV_{DD} = 8.1 V, R_L = 82 Ω

Figure 4-10.

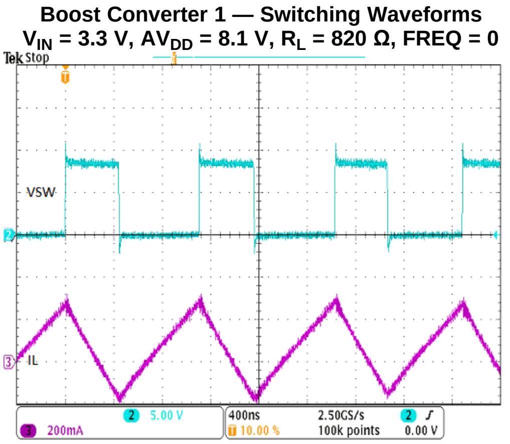

Boost Converter 1 — Switching Waveforms
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 820 Ω, FREQ = 0

Figure 4-11.

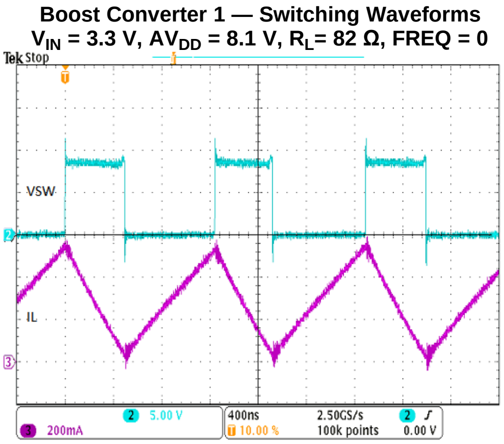

Boost Converter 1 — Switching Waveforms
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L= 82 Ω, FREQ = 0

Figure 4-12.

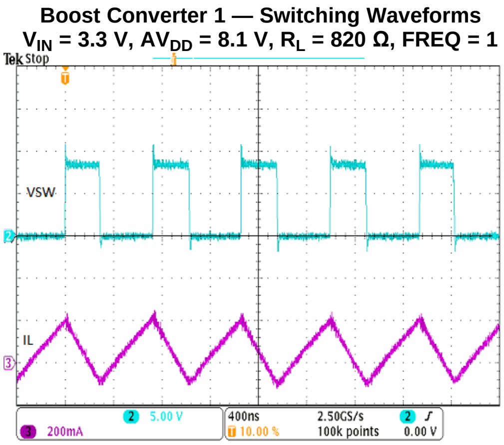

Boost Converter 1 — Switching Waveforms
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 820 Ω, FREQ = 1

Figure 4-13.

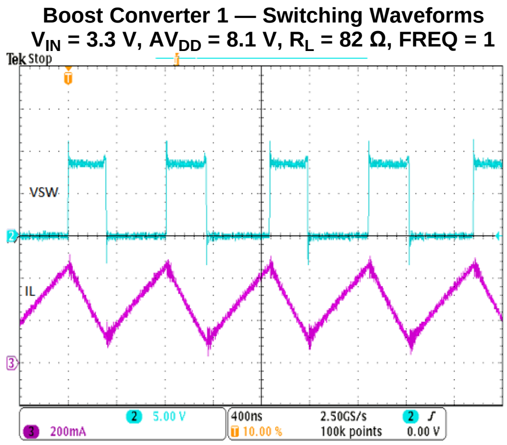

Boost Converter 1 — Switching Waveforms
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, FREQ = 1

Figure 4-14.

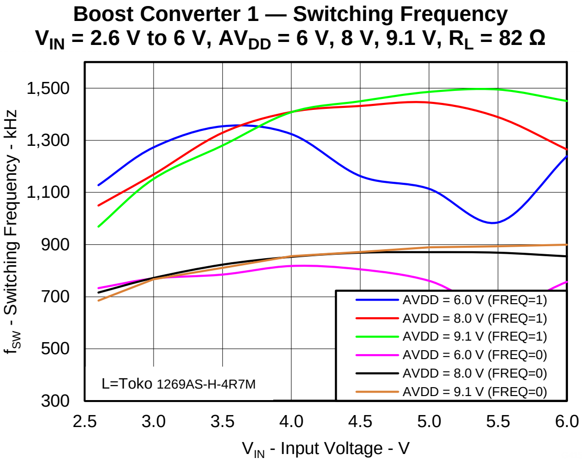

Boost Converter 1 — Switching Frequency
V_{IN} = 2.6 V to 6 V, AV_{DD} = 6 V, 8 V, 9.1 V, R_L = 82 Ω

Figure 4-15.

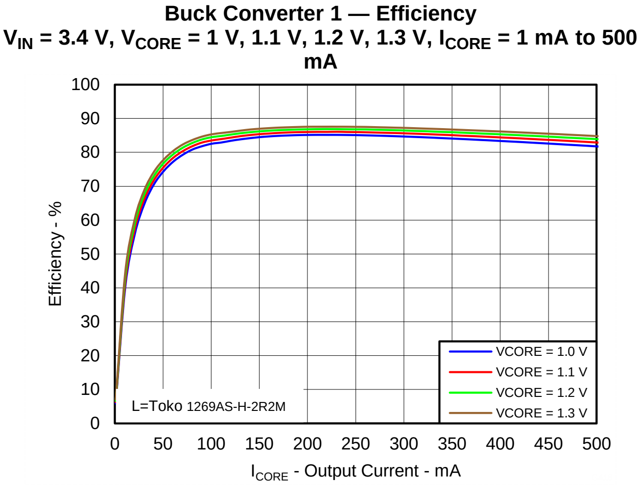

Buck Converter 1 — Efficiency
V_{IN} = 3.4 V, V_{CORE} = 1 V, 1.1 V, 1.2 V, 1.3 V, I_{CORE} = 1 mA to 500 mA

Figure 4-16.

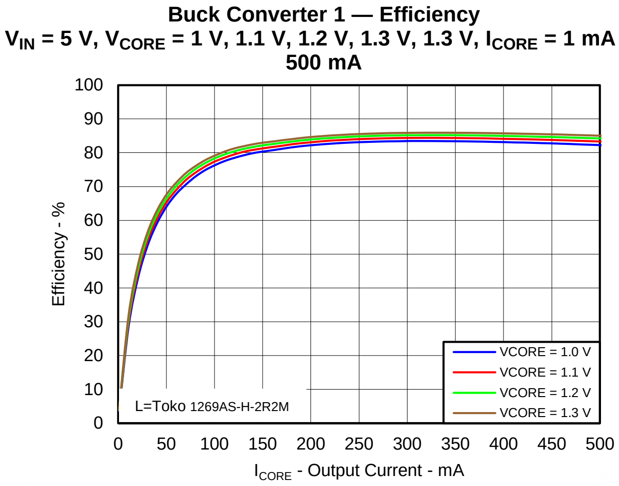

Buck Converter 1 — Efficiency
V_{IN} = 5 V, V_{CORE} = 1 V, 1.1 V, 1.2 V, 1.3 V, 1.3 V, I_{CORE} = 1 mA to 500 mA

Figure 4-17.

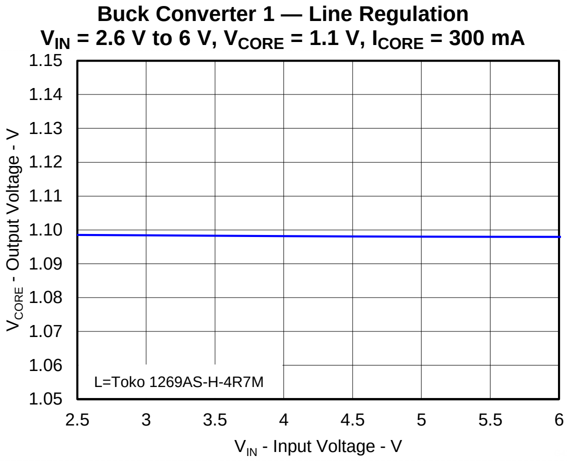
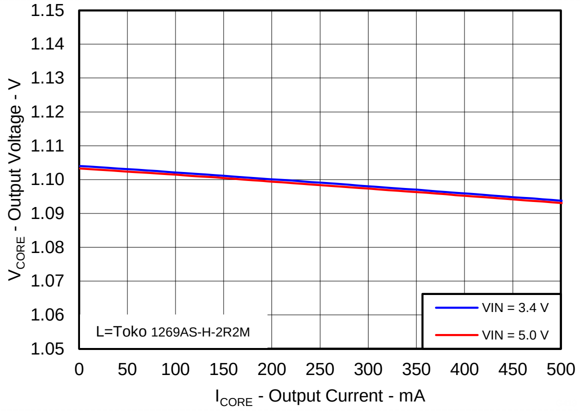
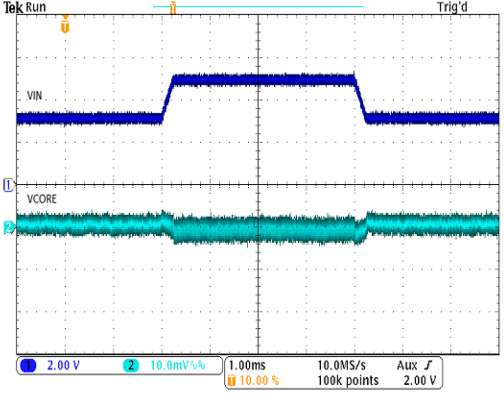

Buck Converter 1 — Line Regulation
V_{IN} = 2.6 V to 6 V, V_{CORE} = 1.1 V, I_{CORE} = 300 mA

Figure 4-18.



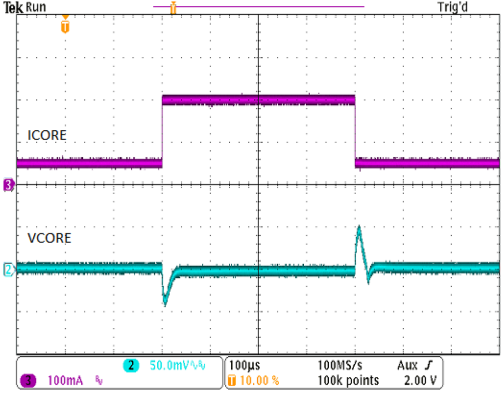
Buck Converter 1 — Load Regulation
V_{IN} = 3.4 V, 5 V, V_{CORE} = 1.1 V, I_{CORE} = 0 mA to 500 mA

Figure 4-19.



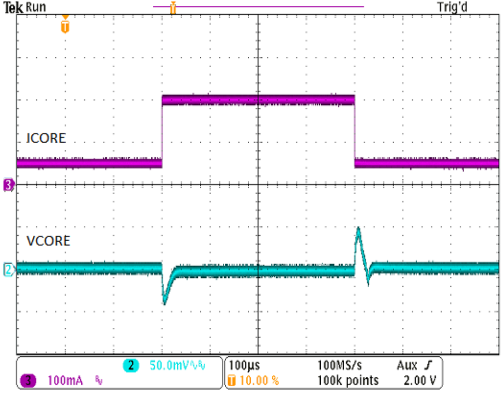
Buck Converter 1 — Line Transient Response
V_{IN} = 3 V/4.8 V, V_{CORE} = 1.1 V, R_L = 3.9 Ω

Figure 4-20.



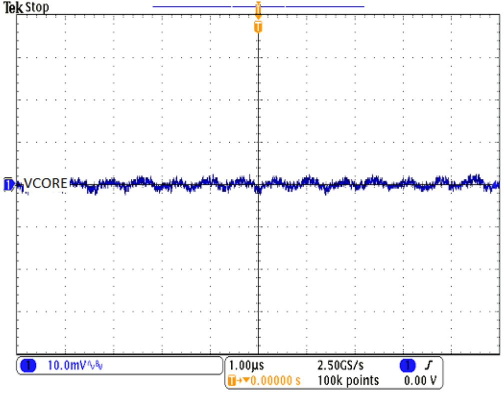
Buck Converter 1 — Load Transient Response
V_{IN} = 3.3 V, V_{CORE} = 1.1 V, I_{CORE} = 50 mA - 200 mA

Figure 4-21.



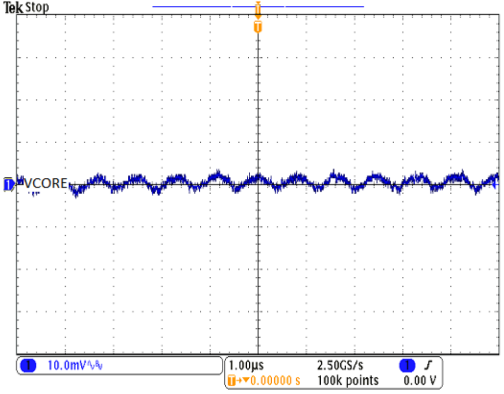
Buck Converter 1 — Load Transient Response
V_{IN} = 5 V, V_{CORE} = 1.1 V, I_{CORE} = 50 mA - 200 mA

Figure 4-22.



Buck Converter 1 — Output Voltage Ripple
V_{IN} = 3.3 V, V_{CORE} = 1.1 V, R_L = 3.9 Ω

Figure 4-23.



Buck Converter 1 — Output Voltage Ripple
V_{IN} = 5 V, V_{CORE} = 1.1 V, R_L = 3.9 Ω

Figure 4-24.

Buck Converter 1 — Switching Waveforms
V_{IN} = 3.3 V, V_{CORE} = 1.1 V, R_L = 120 Ω

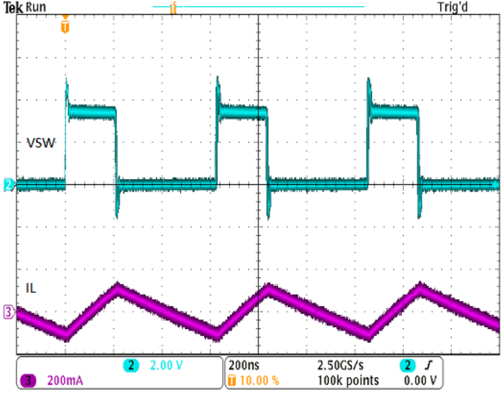


Figure 4-25.

Buck Converter 1 — Switching Waveforms
V_{IN} = 3.3 V, V_{CORE} = 1.1 V, R_L = 3.9 Ω

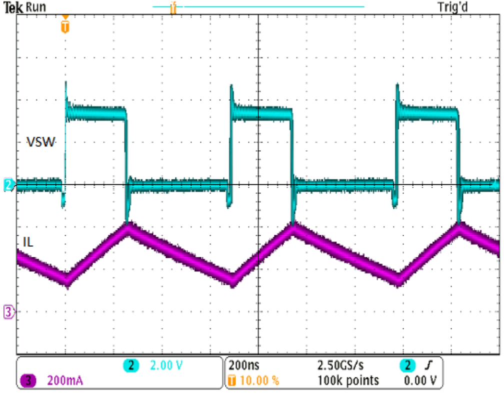


Figure 4-26.

Buck Converter 1 — Switching Frequency
V_{CORE} = 1.1 V, R_L = 12 Ω

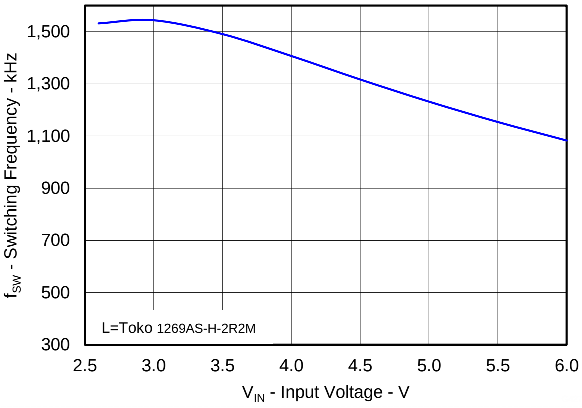


Figure 4-27.

Buck Converter 2 — Efficiency
V_{IN} = 3.3 V, V_{IO1} = 1.7 V, 1.8 V, 2.5 V, I_{IO1} = 1 mA to 500 mA

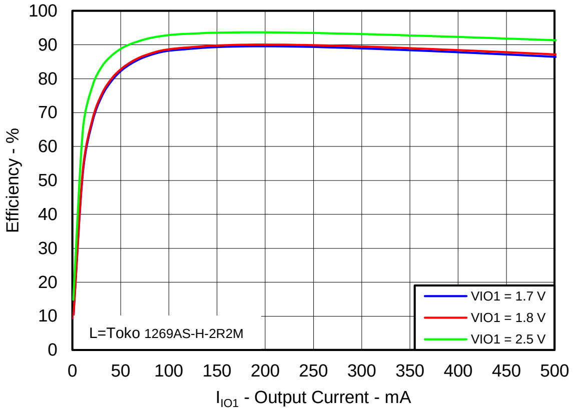


Figure 4-28.

Buck Converter 2 — Efficiency
V_{IN} = 5 V, V_{IO1} = 1.7 V, 1.8 V, 2.5 V, I_{IO1} = 1 mA to 500 mA

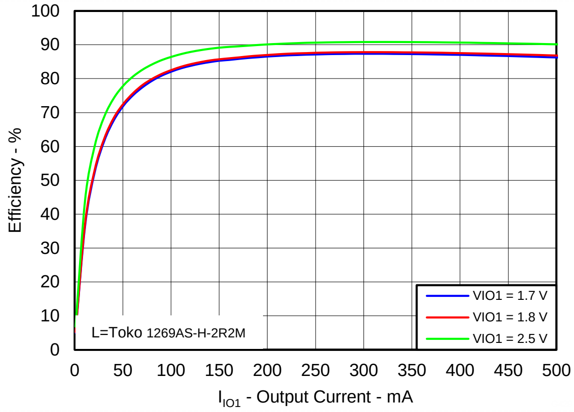


Figure 4-29.

Buck Converter 2 — Line Regulation
V_{IN} = 2.6 V to 6 V, V_{IO1} = 1.7 V, I_{IO1} = 100 mA

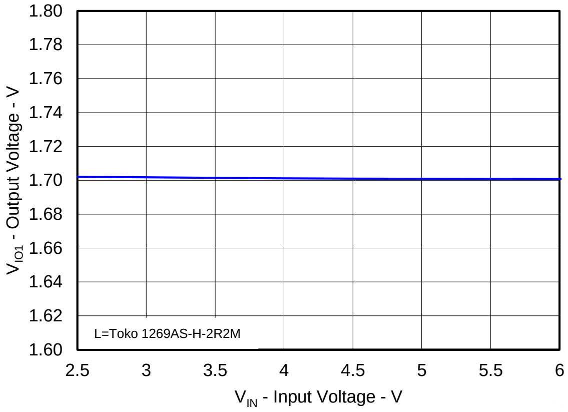
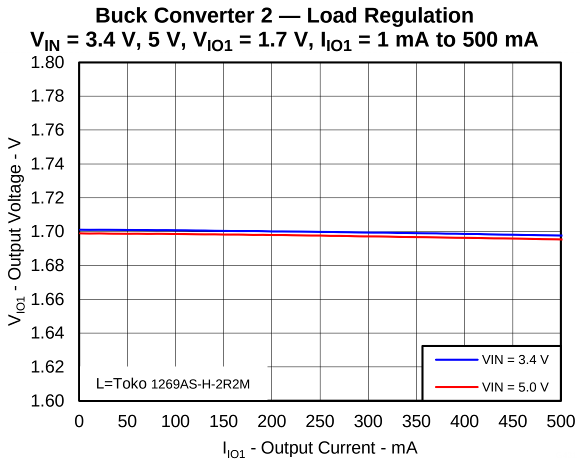
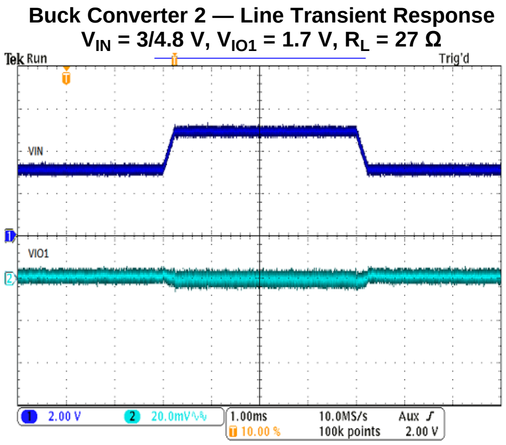


Figure 4-30.



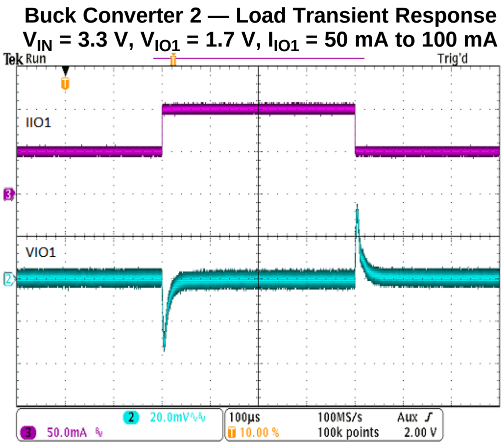
Buck Converter 2 — Load Regulation
V_{IN} = 3.4 V, 5 V, V_{IO1} = 1.7 V, I_{IO1} = 1 mA to 500 mA

Figure 4-31.



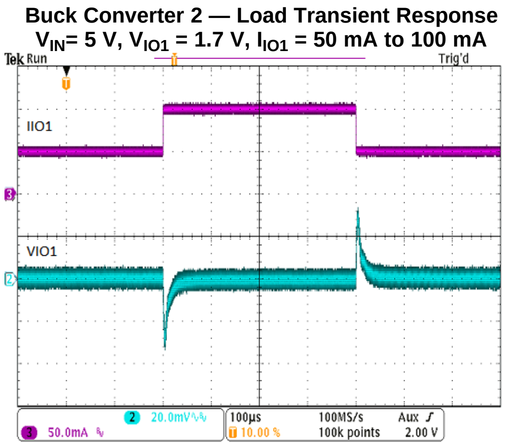
Buck Converter 2 — Line Transient Response
V_{IN} = 3/4.8 V, V_{IO1} = 1.7 V, R_L = 27 Ω

Figure 4-32.



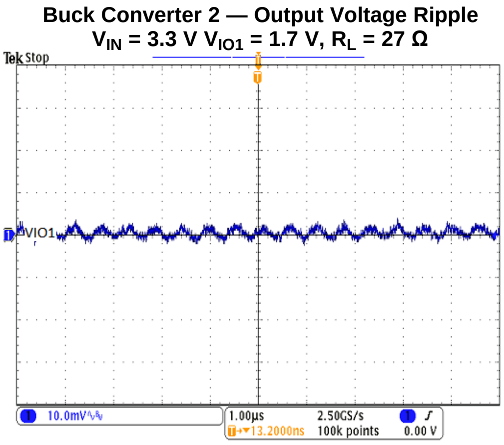
Buck Converter 2 — Load Transient Response
V_{IN} = 3.3 V, V_{IO1} = 1.7 V, I_{IO1} = 50 mA to 100 mA

Figure 4-33.



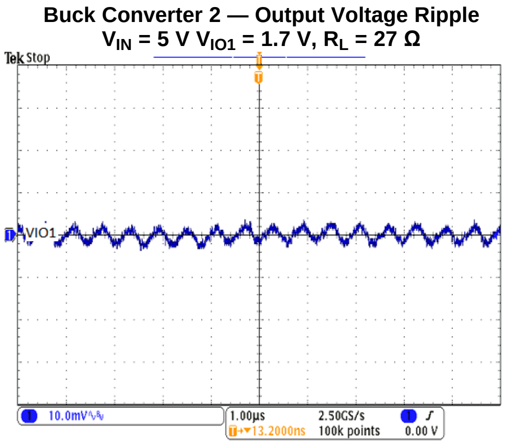
Buck Converter 2 — Load Transient Response
V_{IN}= 5 V, V_{IO1} = 1.7 V, I_{IO1} = 50 mA to 100 mA

Figure 4-34.



Buck Converter 2 — Output Voltage Ripple
V_{IN} = 3.3 V V_{IO1} = 1.7 V, R_L = 27 Ω

Figure 4-35.



Buck Converter 2 — Output Voltage Ripple
V_{IN} = 5 V V_{IO1} = 1.7 V, R_L = 27 Ω

Figure 4-36.

Buck Converter 2 — Switching Waveforms
V_{IN}= 3.3 V, V_{IO1} = 1.7 V, R_L = 270 Ω

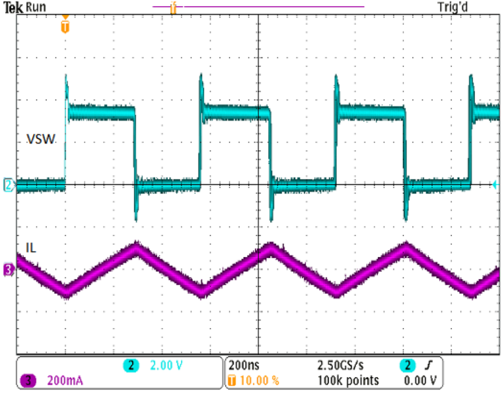


Figure 4-37.

Buck Converter 2 — Switching Waveforms
V_{IN} = 3.3 V, V_{IO1} = 1.7 V, R_L = 27 Ω

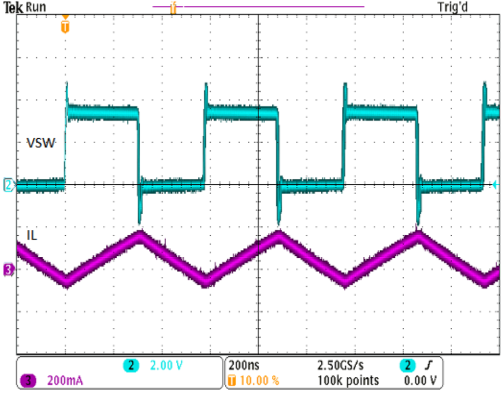


Figure 4-38.

Buck Converter 2 — Switching Frequency
V_{IN} = 2.6 V to 6 V, V_{IO1} = 1.7 V, R_L = 27 Ω

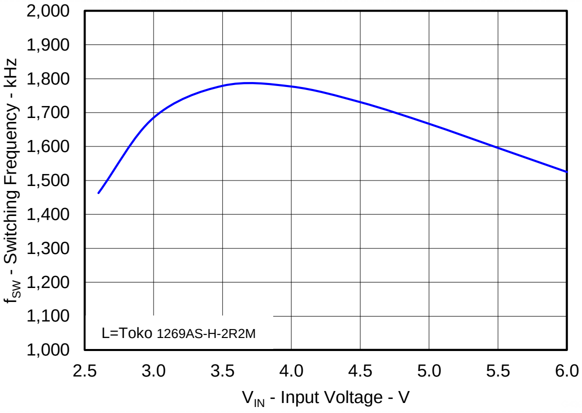


Figure 4-39.

LDO Regulator — Load Regulation
V_{IO1} = 2.5 V, V_{IO2} = 1.8 V, I_{IO2} = 1 mA to 100 mA

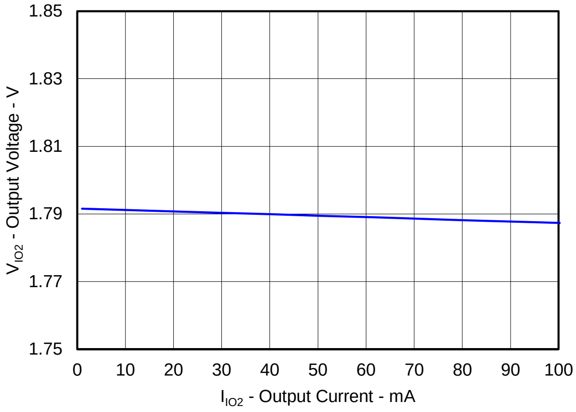


Figure 4-40.

LDO Regulator — Line Transient Response
V_{IN} = 3/4.8 V, V_{IO2} = 1.8 V, R_L = 27 Ω

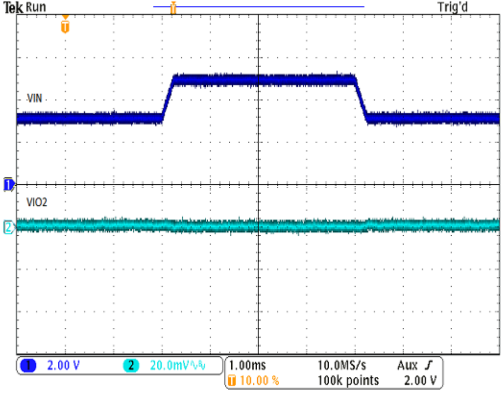


Figure 4-41.

LDO Regulator — Load Transient Response
V_{IN} = 3.3 V, V_{IO1} = 2.5 V, V_{IO2} = 1.8 V, I_{IO2} = 50 mA - 100 mA

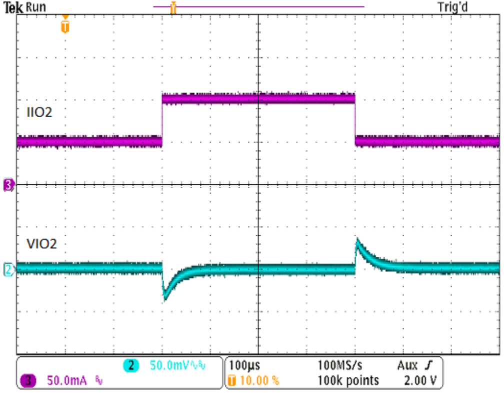


Figure 4-42.

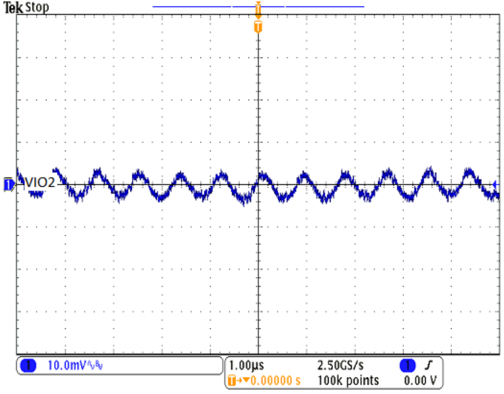

LDO Regulator — Output Voltage Ripple
V_{IN} = 3.3 V, V_{IO1} = 2.5 V, V_{IO2} = 1.8 V, R_L = 27 Ω

Figure 4-43.

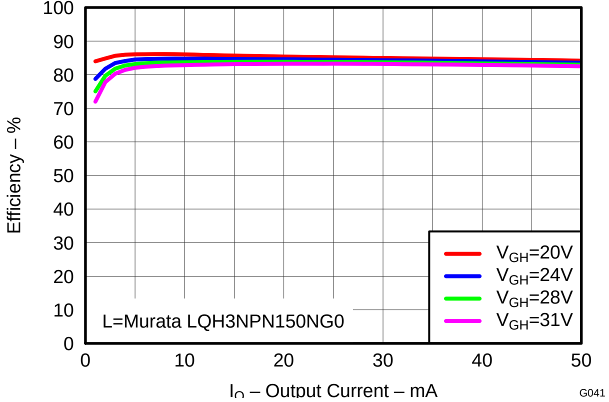

Boost Converter 2 — Efficiency
AV_{DD} = 8.1 V, V_{GH} = 20 V, 24 V, 28 V, 31 V

Figure 4-44.

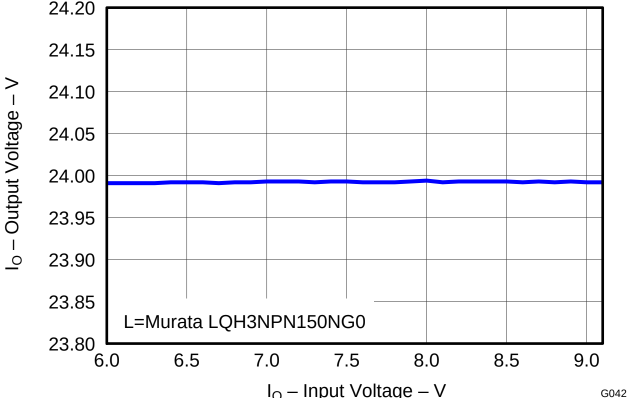

Boost Converter 2 — Line Regulation
AV_{DD} = 6 V to 9.1 V, V_{GH} = 24 V, I_{GH} = 10 mA

Figure 4-45.

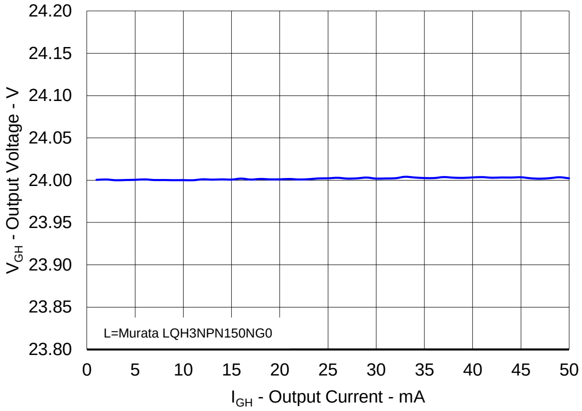

Boost Converter 2 — Load Regulation
AV_{DD} = 8.1 V, V_{GH} = 24 V, IGH = 1 mA to 50 mA

Figure 4-46.

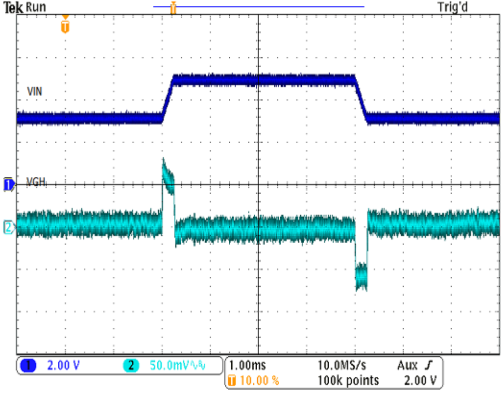

Boost Converter 2 — Line Transient Response
V_{IN} = 3/4.8 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{GH} = 24 V, R_L = 4.8 kΩ

Figure 4-47.

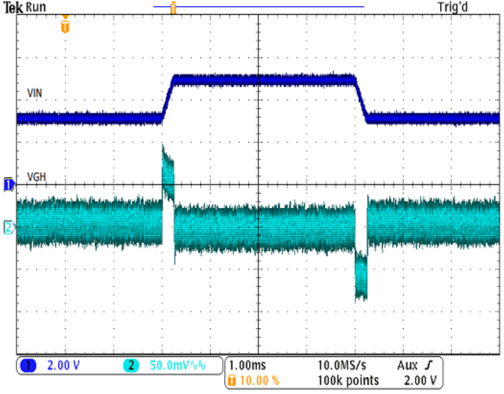

Boost Converter 2 — Line Transient Response
V_{IN} = 3/4.8 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{GH} = 24 V, R_L = 1.2 kΩ

Figure 4-48.

Boost Converter 2 — Load Transient Response
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{GH} = 24 V, I_{GH} = 5-10 mA

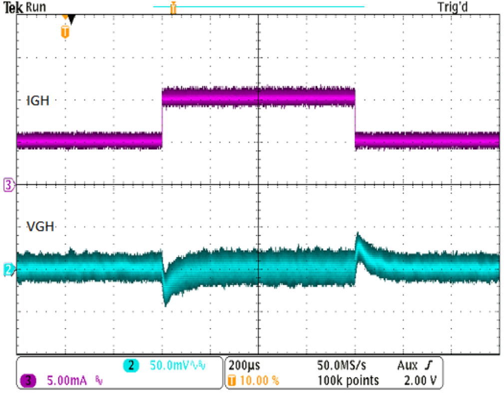


Figure 4-49.

Boost Converter 2 — Load Transient Response
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L= 82 Ω, V_{GH} = 24 V, I_{GH} = 10-30 mA

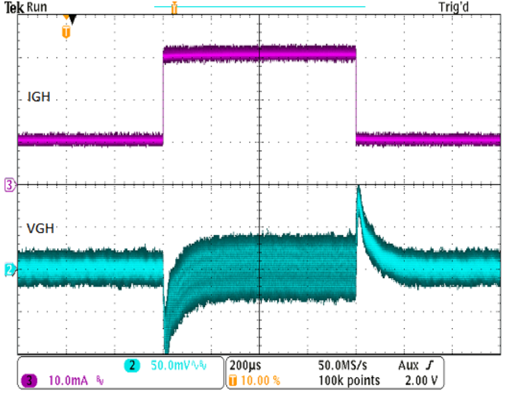


Figure 4-50.

Boost Converter 2 – Output Voltage Ripple
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{GH} = 24 V, R_L = 4.8 kΩ

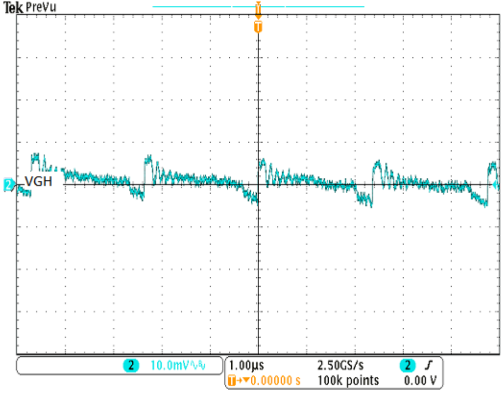


Figure 4-51.

Boost Converter 2 – Output Voltage Ripple
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{GH} = 24 V, R_L = 1.2 kΩ

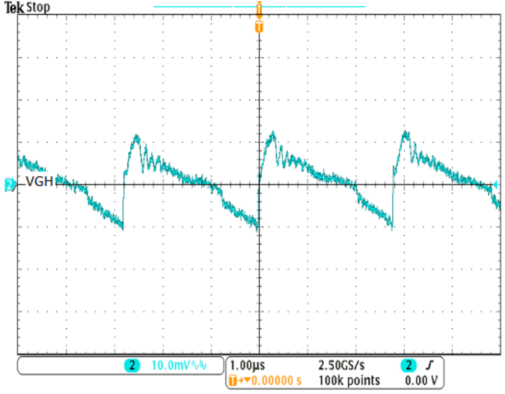


Figure 4-52.

Boost Converter 2 – Switching Waveforms
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{GH} = 24 V, R_L = 4.8 kΩ

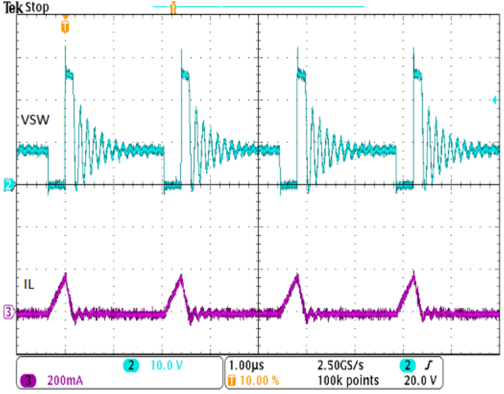


Figure 4-53.

Boost Converter 2 – Switching Waveforms
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{GH} = 24 V, R_L = 1.2 kΩ

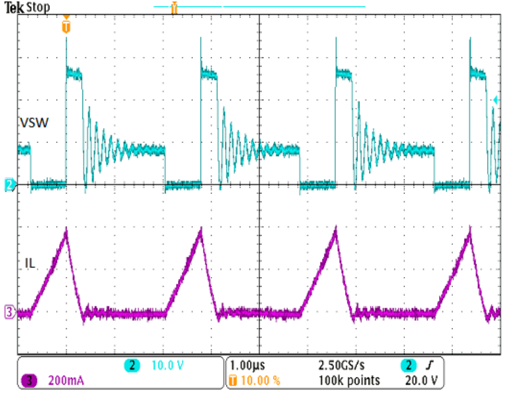


Figure 4-54.

Boost Converter 2 – Switching Frequency
AV_{DD} = 7 V, 8 V, 9 V, V_{GH} = 16 V to 24 V, R_L = 4.8 kΩ

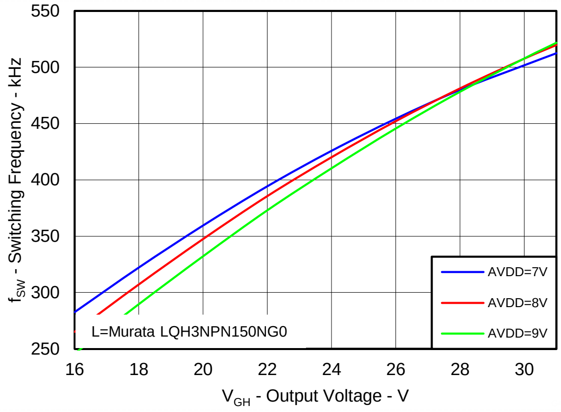


Figure 4-55.

Power-up Sequencing
V_{IN}, V_{IO1}, V_{IO2}, V_{CORE}

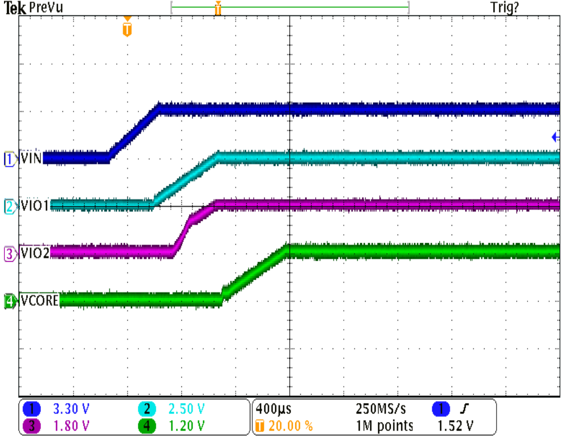


Figure 4-56.

Power-up Sequencing
EN, AV_{DD}, V_{GH} (t_{DLY1} = 0 ms)

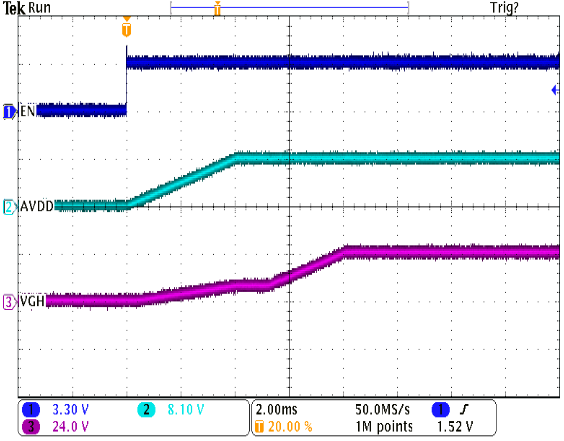


Figure 4-57.

Power-up Sequencing
EN, AV_{DD}, V_{GH} (t_{DLY1} = 10 ms)

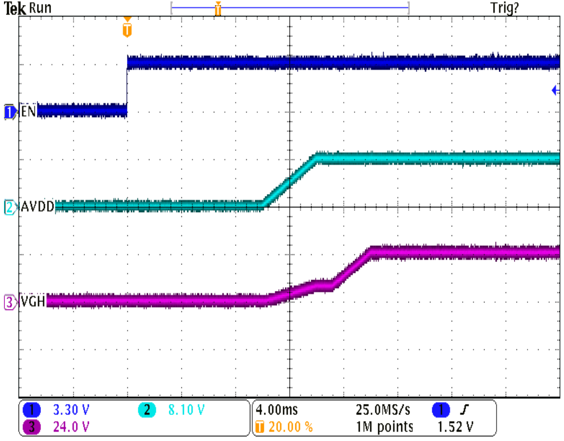


Figure 4-58.

Power-up Sequencing – GIP = 0
XAO, AV_{DD}, V_{GH}, V_{GHM}, t_{DLY6} = 0 ms

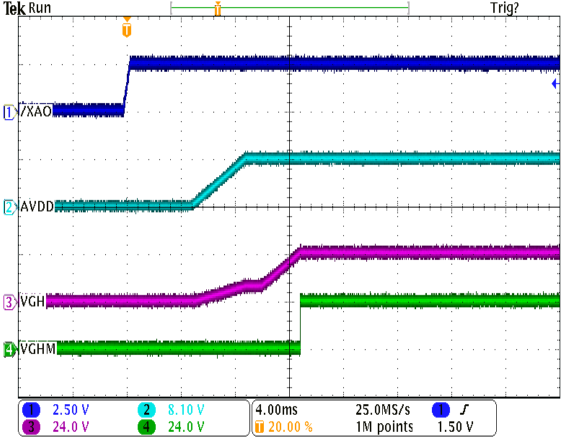


Figure 4-59.

Power-up Sequencing – GIP = 0
XAO, AV_{DD}, V_{GH}, V_{GHM}, t_{DLY6} = 10 ms

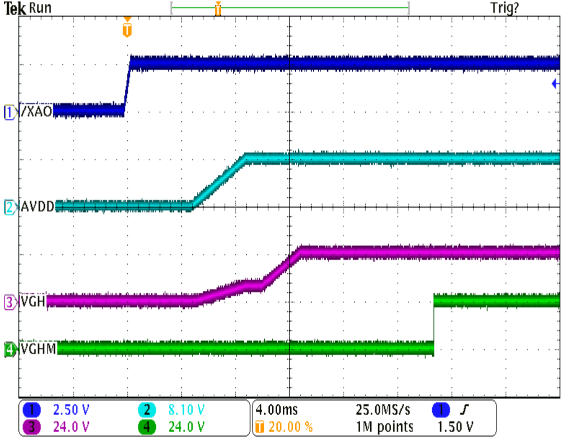


Figure 4-60.

Power-up Sequencing – GIP = 1

$\overline{\text{XAO}}$, AV_{DD}, V_{GH}, V_{GHM}, t_{DLY6} = 0 ms

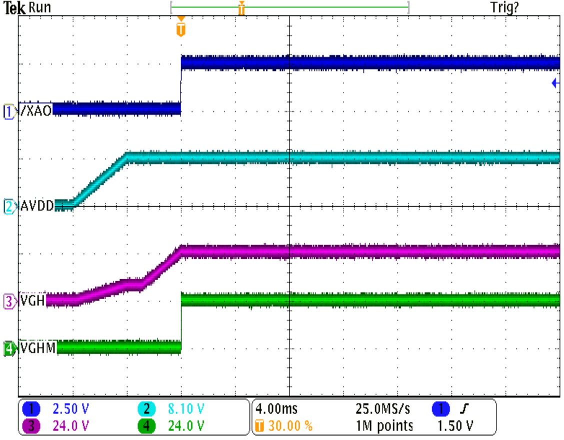


Figure 4-61.

Power-up Sequencing – GIP = 1

$\overline{\text{XAO}}$, AV_{DD}, V_{GH}, V_{GHM}, t_{DLY6} = 10 ms

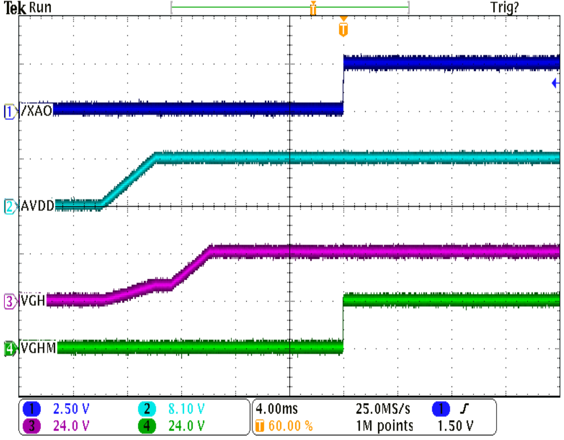


Figure 4-62.

Power-up Sequencing

AV_{DD}, V_{GH}, V_{COM}, V_{GAMA}

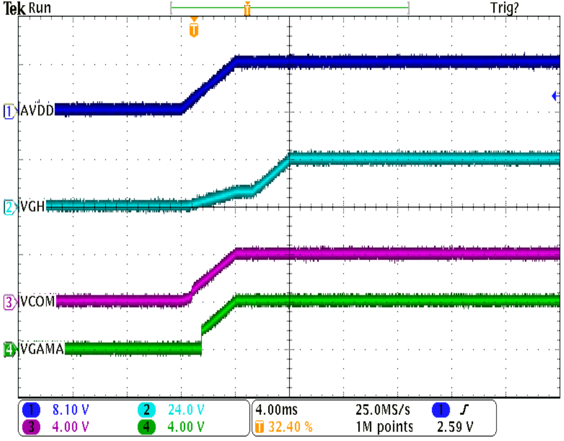


Figure 4-63.

Power-down Sequencing — RMODE = 0

$\overline{\text{RST}}$, V_{IO1}, V_{IO2}, V_{CORE}

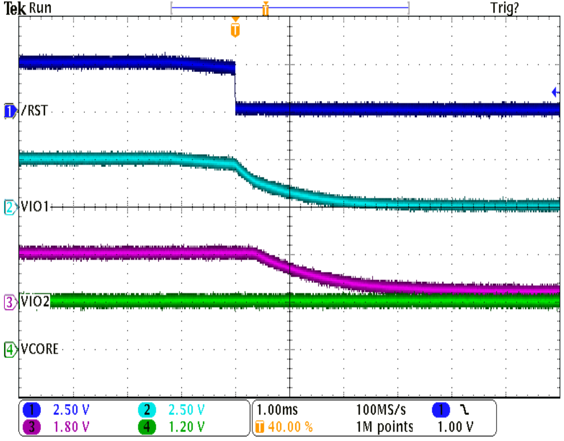


Figure 4-64.

Power-down Sequencing – RMODE = 1, V_{DET} = 2.5 V

$\overline{\text{RST}}$, V_{IO1}, V_{IO2}, V_{CORE}

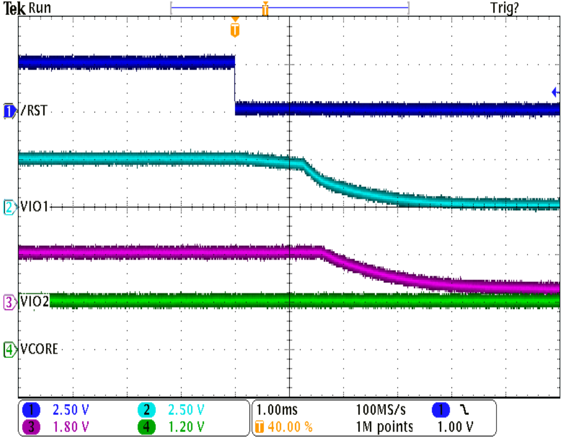


Figure 4-65.

Power-down Sequencing – GIP = 0

V_{IN}, $\overline{\text{XAO}}$, AV_{DD}, V_{GHM}

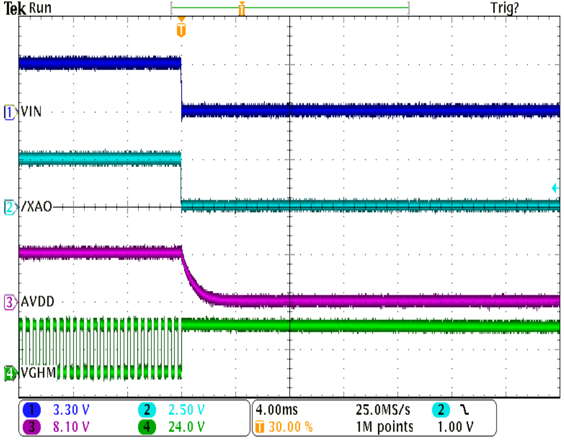


Figure 4-66.

Power-down Sequencing – SMODE = 0
AV_{DD}, V_{GH}, V_{COM}, V_{GAMA}

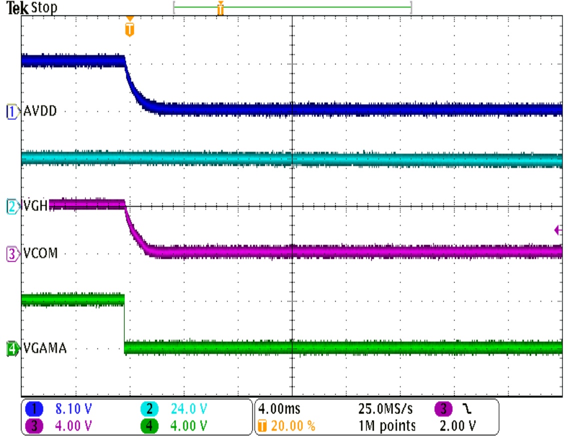


Figure 4-67.

Power-down Sequencing – SMODE = 1
AV_{DD}, V_{GH}, V_{COM}, V_{GAMA}

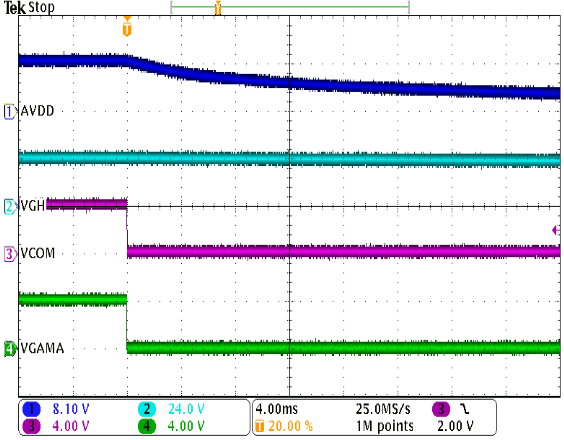


Figure 4-68.

Gate Voltage Shaping — FLK, V_{GHM}
AV_{DD} = 8.1 V, R_L = 33 Ω, V_{GH} = 24 V, R_L = 1.2 kΩ, R_E = 1 kΩ, C_L = 10 nF

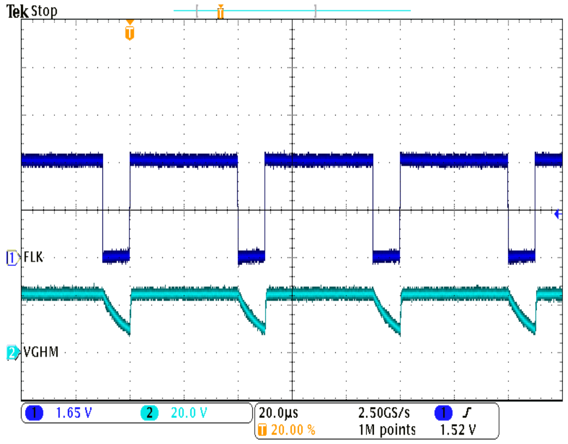


Figure 4-69.

VCOM Buffer — Large Signal Response
AV_{DD} = 7.6 V, R_L= 82 Ω, V_{POS} = 3.8 V + 0.5 V_{PP}

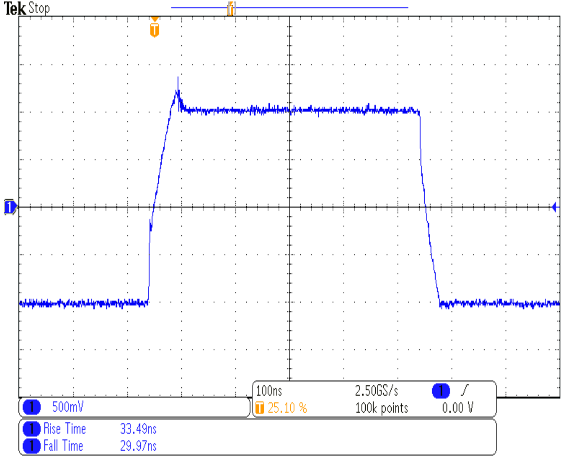


Figure 4-70.

VCOM Buffer — Small-Signal Bandwidth
AV_{DD} = 8.1 V, V_{POS} = 4 V + 65 mV_{pp}

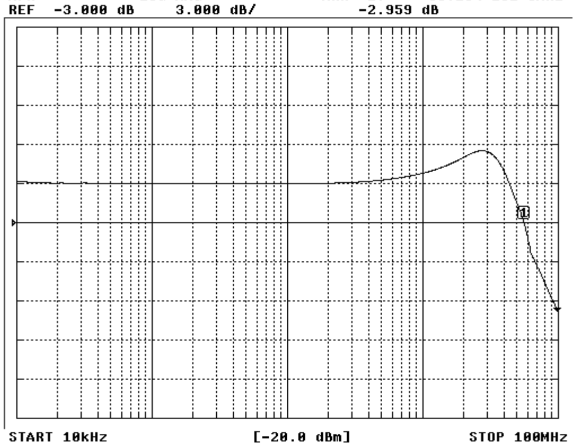


Figure 4-71.

VCOM Buffer — Gain-Bandwidth Product
AV_{DD} = 8.1 V, V_{POS} = 4 V + 65 mV_{pp}

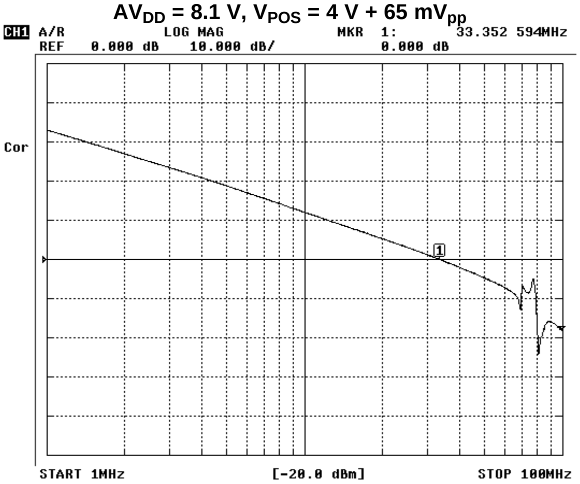


Figure 4-72.

VCOM Buffer — Peak Output Current
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 2 kΩ to $AV_{DD}/2$, C_L = 1 μF

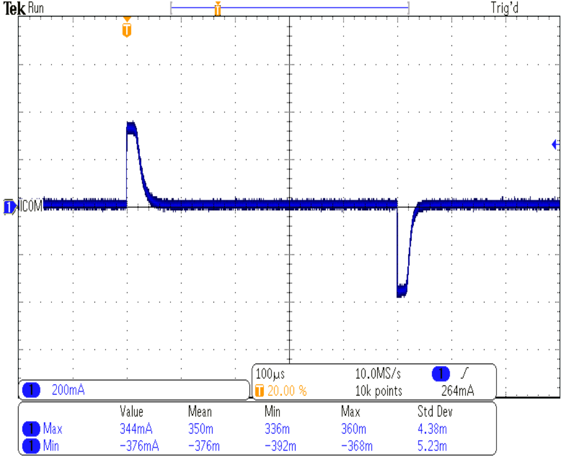


Figure 4-73.

VCOM Buffer — Line Transient Response
V_{IN} = 3/4.8 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{COM}= 4 V, R_L = ∞

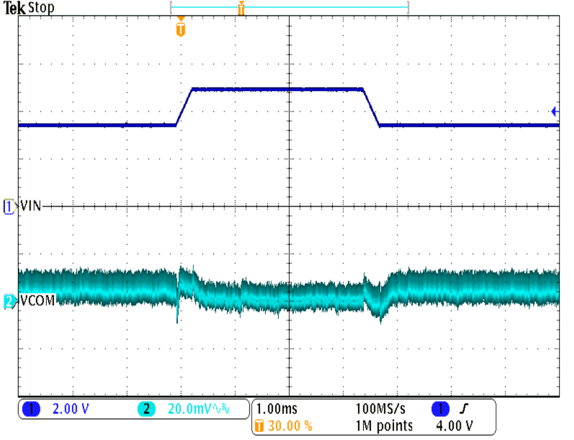


Figure 4-74.

VCOM Buffer — Output Voltage Ripple & Noise
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, V_{COM} = 4 V, R_L = ∞

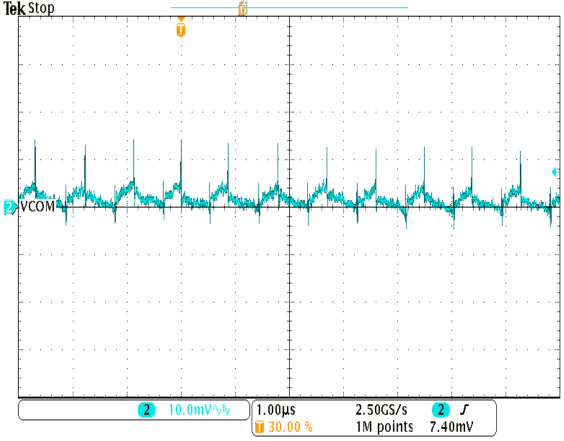


Figure 4-75.

Programmable GAMMA — Dynamic Response
GAMA = 0x0ff to 0x2ff, R_L = 909 kΩ, C_L = 55 pF

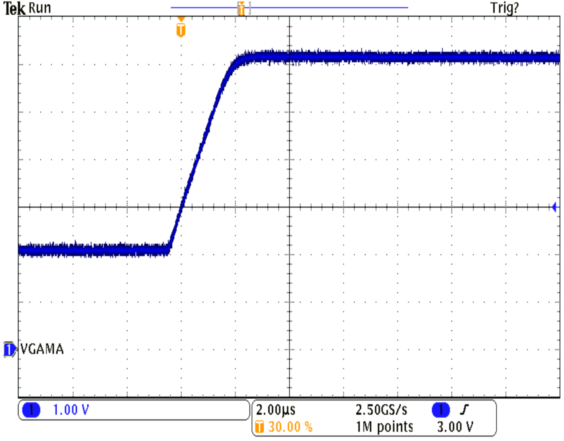


Figure 4-76.

GAMMA Voltage — Dynamic Response
GAMA = 0x2ff to 0x0ff, R_L = 909 kΩ, C_L = 55 pF

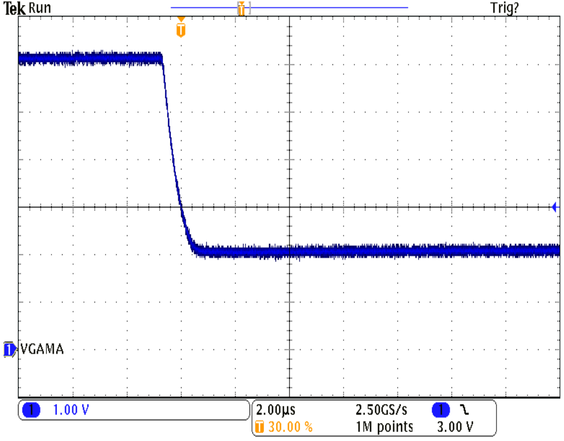


Figure 4-77.

Programmable GAMMA — Line Transient Response
V_{IN} = 3.3/4.8 V, AV_{DD} = 8.1 V, R_L = 82 Ω, GAMA = 0x0ff

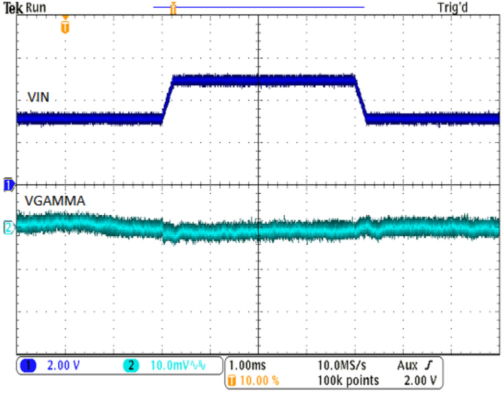


Figure 4-78.

Programmable GAMMA — Line Transient Response
V_{IN} = 3.3/4.8 V, AV_{DD} = 8.1 V, R_L = 82 Ω, GAMA = 0x1ff

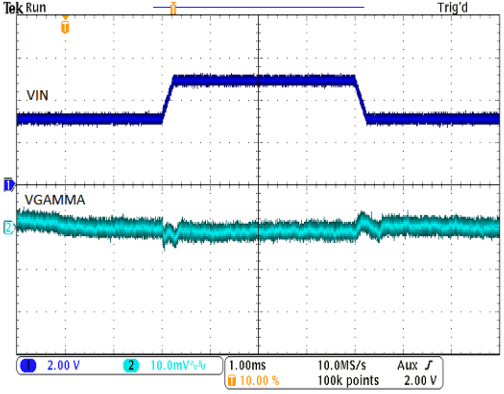


Figure 4-79.

Programmable GAMMA — Line Transient Response
V_{IN} = 3.3/4.8 V, AV_{DD} = 8.1 V, R_L = 82 Ω, GAMA = 0x2ff

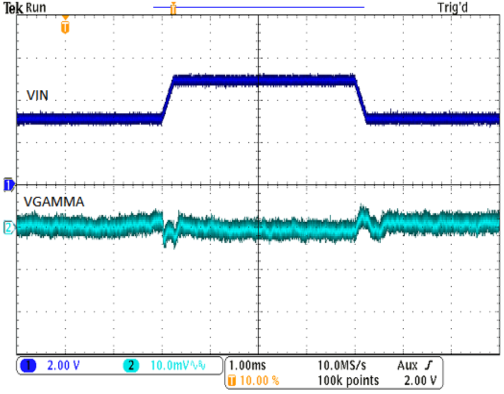


Figure 4-80.

Programmable GAMMA — Output Voltage Ripple & Noise
V_{IN} = 3.3 V, AV_{DD} = 8.1 V, R_L = 82 Ω, GAMA = 0x1ff

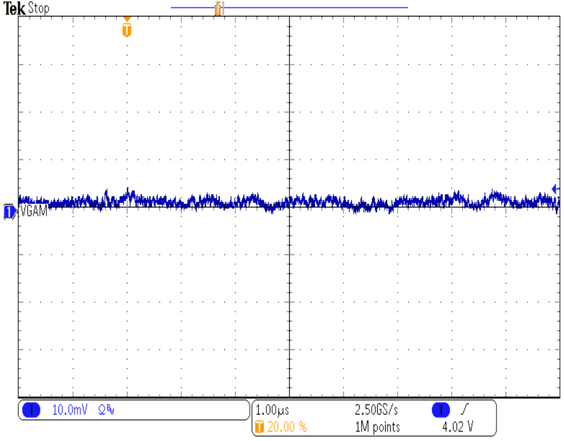


Figure 4-81.

5 Detailed Description

An internal block diagram of the TPS65642 is shown in Figure 5-1.

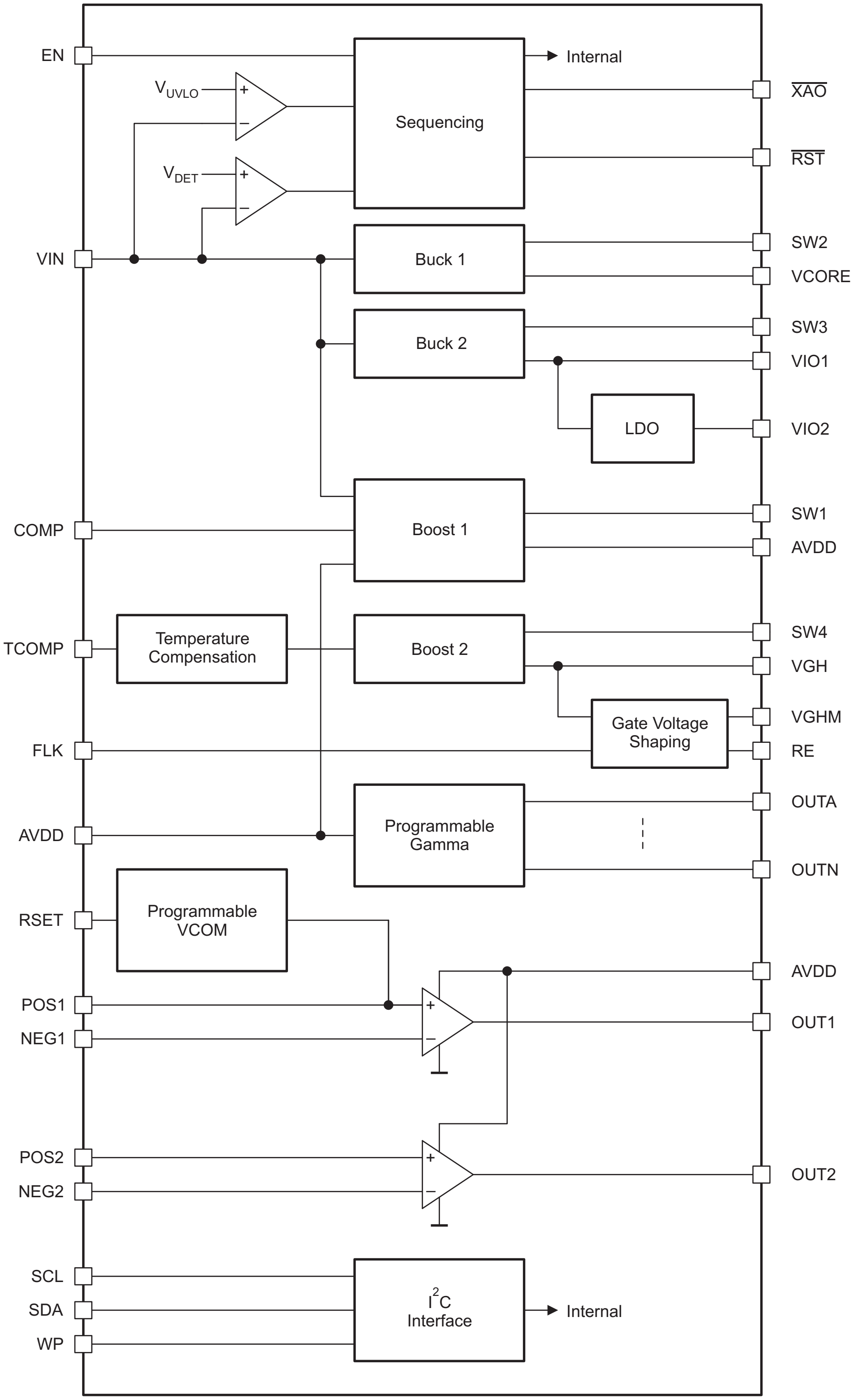


Figure 5-1. Internal Block Diagram

5.1 BOOST CONVERTER 1 (AV_{DD})

Boost converter 1 is synchronous and uses a virtual current mode topology that:

- achieves high efficiencies
- allows the converter to work in continuous conduction mode under all operating conditions, simplifying compensation
- provides a better drive signal for the negative charge pump connected to the switch node (because the converter always runs in continuous conduction mode, even at low output currents)
- provides true input-output isolation when the boost converter is disabled

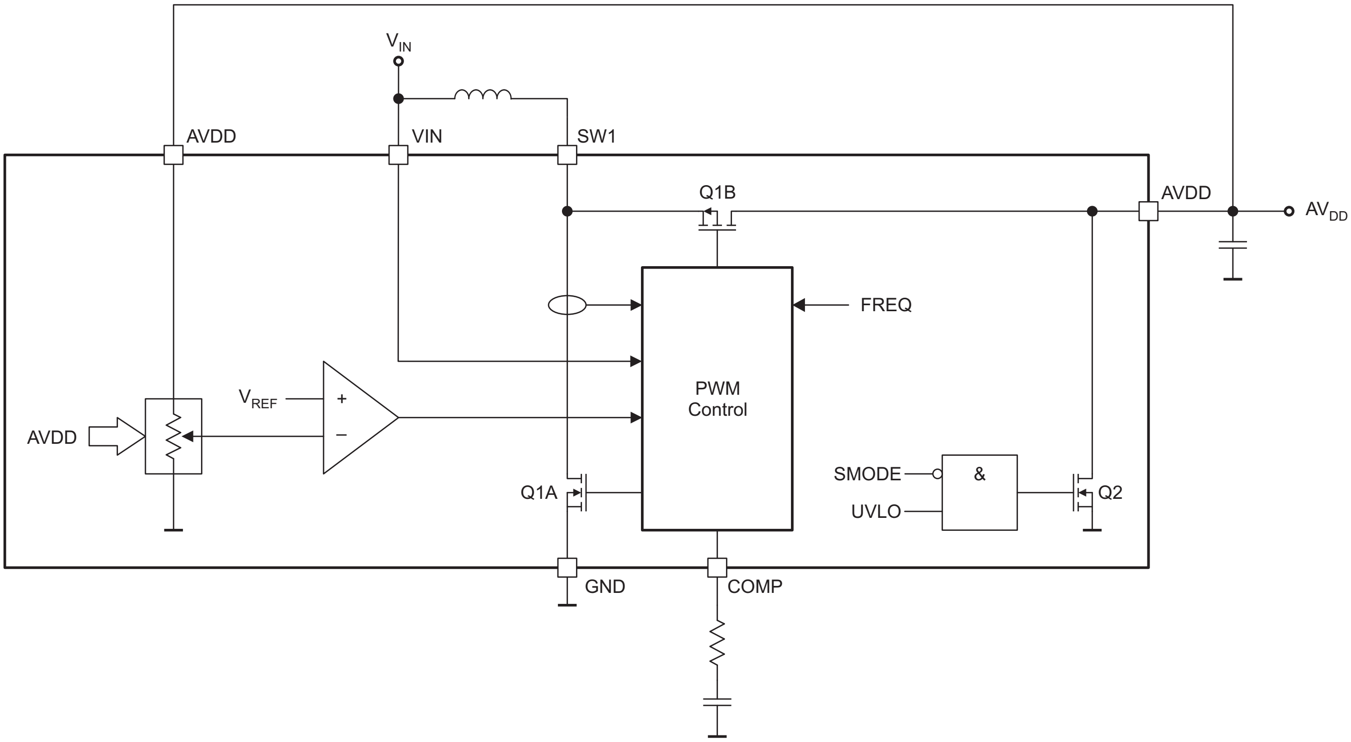


Figure 5-2. Boost Converter 1 Internal Block Diagram

5.1.1 Switching Frequency (Boost Converter 1)

Boost converter 1's nominal switching frequency can be programmed to 750 kHz or 1200 kHz using the FREQ bit in the MISC register.

5.1.2 Compensation (Boost Converter 1)

Boost converter 1 uses an external compensation network connected to the COMP pin to stabilize its feedback loop. A simple series R-C network connected between the COMP pin and ground is sufficient to achieve good performance, that is, stable and with good transient response. Good starting values, which will work for most applications, are 100 kΩ and 1 nF for 1200 MHz AV_{DD} switching frequency and 56 kΩ and 1.5 nF for 750 kHz AV_{DD} switching frequency.

In some applications (e.g. those using electrolytic output capacitors), it may be necessary to include a second compensation capacitor between the COMP pin and ground (typically 22 pF). This has the effect of adding an additional pole in the feedback loop's frequency response, which cancels the zero introduced by the output capacitor's ESR.

The COMP pin is directly connected to the input of the converter's current comparator, which means that any noise present on this pin can directly affect converter operation. In practical applications the most likely source of noise is the converter's switch pin, and for proper operation it is essential that the stray capacitance between the SW1 and the COMP pins is minimized. This can be ensured using good PCB layout practices, such as:

- locating the compensation components close to the COMP pin
- removing the GND plane from underneath the SW1 PCB tracks (to prevent this high dV/dt signal from inducing currents locally in the GND plane)
- connecting the ground side of the compensation components to a noise-free GND location, that is, away from noisy power ground signals

For the most robust operation, it is recommended to ensure that the parasitic capacitance between the SW1 and COMP is below 0.1 pF.

5.1.3 Power-Up (Boost Converter 1)

Boost converter 1 starts t_{DLY1} milliseconds after EN or $\overline{RST}$ goes high, whichever occurs later. Delay time t_{DLY1} can be programmed from 0 ms to 70 ms using the DLY1 register. Once asserted, the EN signal must remain high to ensure normal device operation. Once disabled (EN = 0), boost converter 1 remains disabled until the device is powered down (even if EN is re-asserted).

To minimize inrush current during start-up, boost converter 1 ramps its output voltage in t_{SS2} milliseconds. Start-up time t_{SS2} can be programmed from 4 ms to 7.5 ms using the SS2 register. Longer soft-start times generate lower inrush currents.

The same ramp rate is also used for boost converter 2 – changing the SS2 register affects both boost converters.

The soft-start function is not implemented if boost converter 1's output voltage is re-programmed during operation. This is not a problem during normal operation (when AV_{DD} remains constant), however, it may cause problems during production if AV_{DD} is changed while the converter is enabled. Problems can occur under such conditions because, without a soft-start, the converter draws a high inrush current when its output voltage is changed. If the converter is supplied from a high-impedance source, this inrush current can, under certain circumstances, pull V_{IN} below the UVLO threshold, disabling the IC and interrupting the writing of the configuration parameters. One or more of the following recommendations can be used to ensure trouble-free configuration during production:

- program the configuration parameters before the IC is soldered to the PCB
- supply the PCB with a voltage high enough to ensure that the voltage on the VIN pin remains above the UVLO threshold when the value of AV_{DD} is changed
- ensure that the supply impedance is low enough to ensure that the voltage on the VIN pin remains above the UVLO threshold when the value of AV_{DD} is changed
- disable boost converter 1 while the value of AV_{DD} is changed

5.1.4 Power-Down (Boost Converter 1)

Boost converter 1 is disabled when EN=0 or $V_{IN}<V_{UVLO}$. When disabled, boost converter 2 actively discharges AV_{DD} by turning on Q2. The active discharge feature can be disabled by setting SMODE=1 in the CONFIG register. Once disabled (EN = 0), boost converter 1 remains disabled until the device is powered down (even if EN is re-asserted).

5.1.5 Isolation (Boost Converter 1)

The synchronous topology of boost converter 1 ensures that AV_{DD} is fully isolated from V_{IN} when the converter is disabled.

5.1.6 Output Voltage (Boost Converter 1)

Boost converter 1's output voltage can be programmed from 6.0 V to 9.1 V in 100 mV steps using the AVDD register.

5.1.7 Input Supply Characteristics

Boost converter 1 exhibits a fast response with excellent line transient performance. Its fast reaction to changes in input voltage means that excessive input impedance can cause the converter to become unstable. This can happen, for example, if V_{IN} is supplied via an excessively long cable, in which case the cable's parasitic inductance forms a resonant circuit with the IC's input capacitance. The following guidelines help avoid such problems and ensure proper operation:

- minimize supply cable inductance
- minimize supply cable resistance
- maximize input capacitance
- avoid using ceramic types for the bulk input capacitance - capacitors with higher ESR help to damp any tendency to ring on the part of the input cable

5.2 BUCK CONVERTER 1 (V_{CORE})

Buck converter 1 is synchronous and uses a constant off-time topology that offers high efficiency, fast transient response, and constant ripple current amplitude under all operating conditions. The output voltage V_{CORE} can be programmed by the user. The converter's off-time is inversely proportional to its output voltage, and therefore constant when the converter is in regulation. Thus for a given V_{IN} the converter operates at a constant frequency that changes temporarily when the converter reacts to load changes.

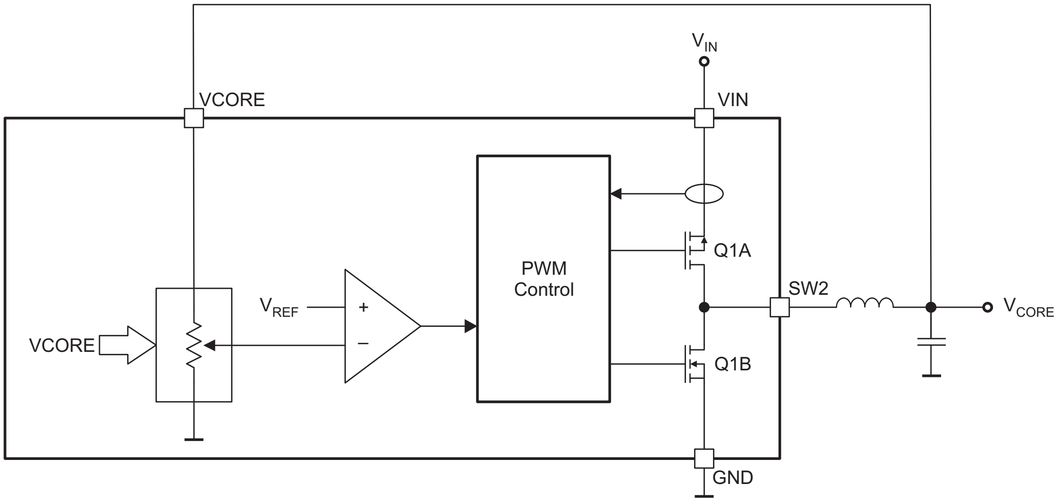


Figure 5-3. Buck Converter 1 Block Diagram

5.2.1 Output Voltage (Buck Converter 1)

Buck converter 1's output voltage can be programmed from 1 V to 1.3 V in 100 mV steps.

5.2.2 Power-Up (Buck Converter 1)

Buck converter 1 starts as soon as buck converter 2 and the LDO regulator have finished ramping up.

To minimize inrush current during start-up, buck converter 1 ramps V_{CORE} from zero to its final value in t_{SS1} milliseconds. Soft-start time t_{SS1} can be programmed from 0.5 ms to 4 ms using the SS1 register.

The same ramp rate is used for both buck converters and the linear regulator. Changing SS1 affects all three regulators.

5.2.3 *Power-Down (Buck Converter 1)*

Buck converter 1 is disabled when $V_{IN} < V_{UVLO}$. Its output is not actively discharged.

5.3 BUCK CONVERTER 2 (V_{IO1})

Buck converter 2 is a low-power synchronous buck converter that in typical applications generates the I/O supply voltage for the timing controller and source drivers. It is essentially the same as buck converter 1, also the output voltage V_{IO1} can be programmed by the user but the output is actively discharged during power-down.

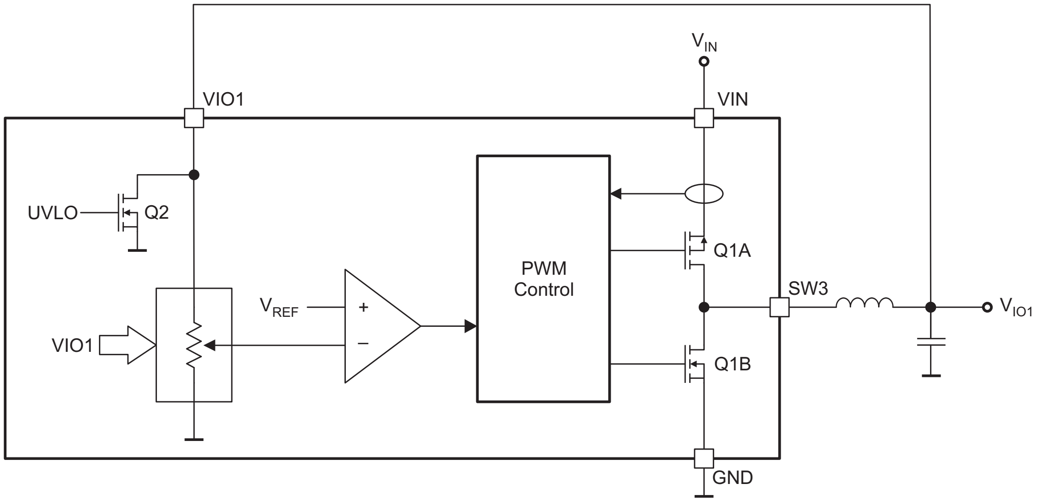


Figure 5-4. Buck Converter 2 Internal Block Diagram

5.3.1 *Output Voltage (Buck Converter 2)*

Buck converter 2's output voltage can be programmed to 1.7 V, 1.8 V, or 2.5 V using the VIO register. When V_{IO1} = 1.7 V or 1.8 V, the LDO regulator is disabled.

5.3.2 *Power-Up (Buck Converter 2)*

Buck converter 2 starts as soon as $V_{IN} > V_{UVLO}$ (the same time the LDO regulator starts), and implements the same voltage ramping as buck converter 1.

5.3.3 *Power-Down (Buck Converter 2)*

Buck converter 2 is disabled and actively discharges its output when $V_{IN} < V_{UVLO}$.

5.4 LDO REGULATOR (V_{IO2})

In applications in which the timing controller and source drivers use different I/O voltages, the LDO regulator can be used to generate the lower I/O supply voltage V_{IO2}. The LDO regulator is supplied from the VIO1 pin, which is the output of buck converter 2.

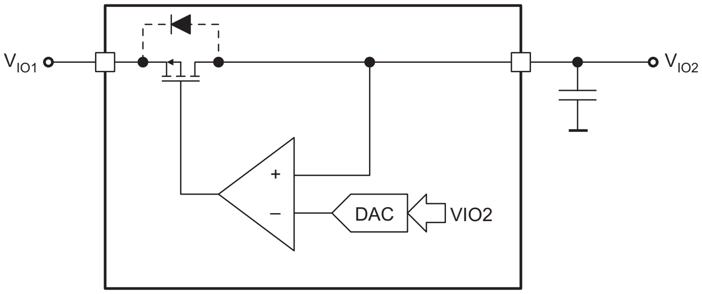


Figure 5-5. Linear Regulator Block Diagram

5.4.1 *Output Voltage (LDO Regulator)*

When V_{IO1} = 2.5 V, the LDO regulator's output voltage can be programmed to 1.7 V or 1.8 V using the VIO register. To ensure reliable LDO programming, EN has to be "high" and the power-up sequence must be over (t_{DLY6}). When V_{IO1} = 1.7 V or 1.8 V, the LDO regulator is disabled.

5.4.2 *Power-Up (LDO Regulator)*

At power up, the LDO regulator starts as soon as $V_{IN} > V_{UVLO}$ (the same time buck converter 1 and buck converter 2 starts). It ramps its output linearly from zero to V_{IO2} in t_{SS1} milliseconds. Soft-start time t_{SS1} can be programmed from 0.5 ms to 4 ms using the SS1 register.

The same ramp rate is used for both buck converters and the LDO regulator. Changing the SS1 register affects all three regulators.

When the LDO is turned on/off during normal device operation (that is, programming V_{IO1} from 1.7V to 2.5V or vice versa), the ramp or discharge characteristic is defined by the load connected.

5.4.3 *Power-Down (LDO Regulator)*

The LDO regulator is supplied from the VIO1 pin, which is actively discharged during power-down. The LDO regulator's output therefore discharges through transistor Q1's body diode as long as VIO2 is high enough to forward bias it. Thereafter, V_{IO2} continues to discharge through the load connected to it.

5.5 BOOST CONVERTER 2 (V_{GH})

Boost converter 2 is non-synchronous, and uses a constant off-time topology. The converter's switching frequency is not constant, but adapts itself to V_{IN} and V_{GH}. Boost converter 2 uses peak current control and is designed to operate permanently in discontinuous conduction mode (DCM), thereby allowing the internal compensation circuit to achieve stable operation over a wide range of output voltages and currents, that is, when temperature compensation is used.

A simplified block diagram of boost converter 2 is shown in Figure 5-6.

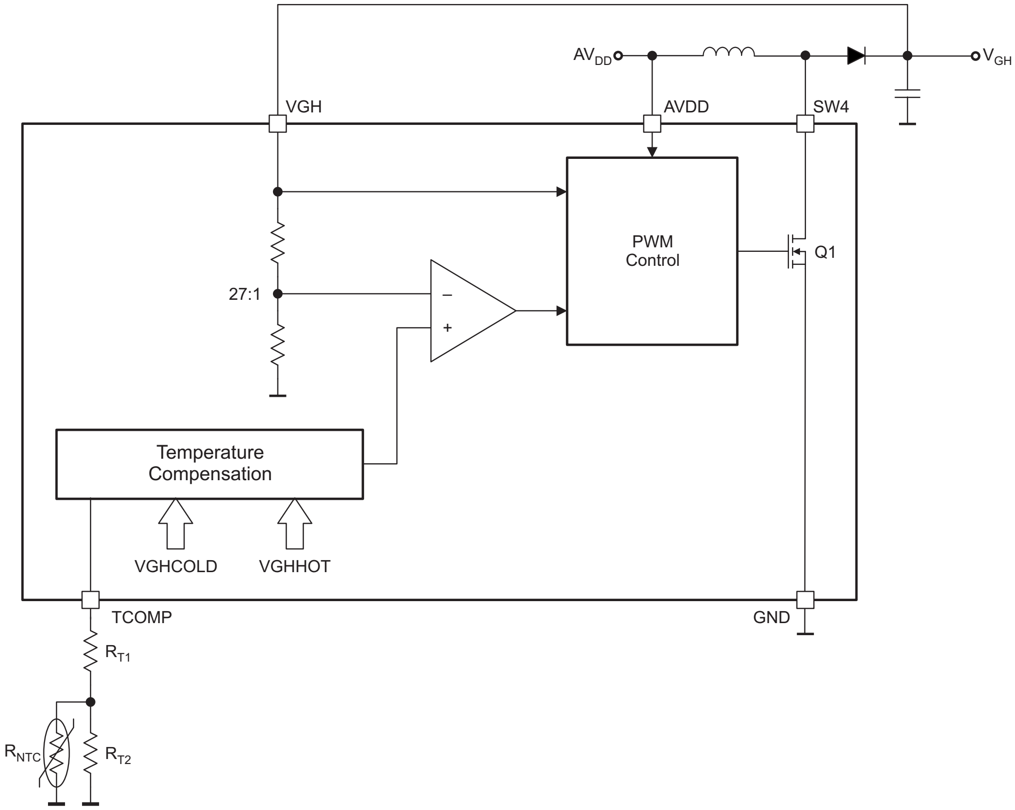


Figure 5-6. Boost Converter 2 Block Diagram

Boost converter 2 can be temperature compensated, allowing its output voltage to transition from a higher voltage at low temperatures $V_{GH(COLD)}$ to a lower voltage at high temperatures $V_{GH(HOT)}$ (see Figure 5-7 and Figure 5-8). The values of $V_{GH(HOT)}$ and $V_{GH(COLD)}$ are programmed using the VGHHOT and VGHCOLD registers. The values of T_{HOT} and T_{COLD} are programmed by selecting the appropriate resistor values for the thermistor network connected to the TCOMP pin.

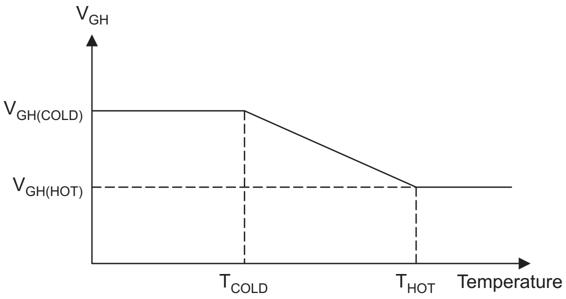


Figure 5-7. Boost Converter 2 Temperature Compensation Characteristic

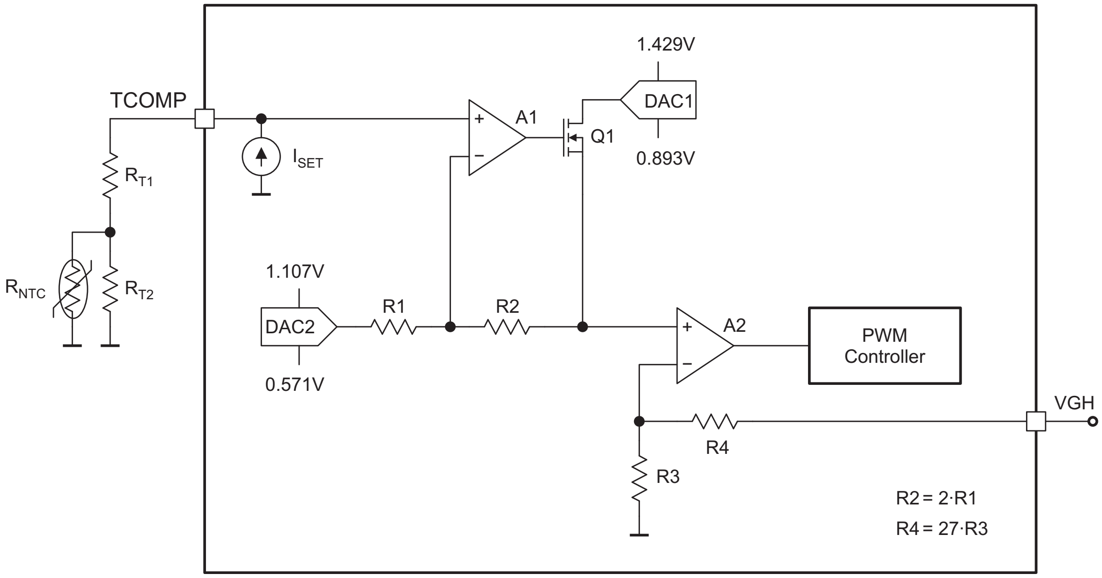


Figure 5-8. Boost Converter 2 Temperature Compensation Block Diagram

Referring to Figure 5-8, temperature compensation works as follows:

The thermistor network formed by R_{T1}, R_{T2} and R_{NTC} (1) generates a voltage at the TCOMP pin whose value decreases with increasing temperature.

With proper selection of the external components R_{T1}, R_{T2} and R_{NTC}, temperatures T_{HOT} and T_{COLD} can be configured to suit each display's characteristics. A Microsoft Excel® spreadsheet allowing easy calculation of component values is available from Texas Instruments free of charge.

5.5.1 Power-Up (Boost Converter 2)

Boost converter 2 is enabled when AV_{DD} has finished ramping up. To minimize inrush current during start-up, boost converter 2 ramps V_{GH} linearly to its programmed value in t_{SS2} seconds. Soft-start time t_{SS2} can be programmed from 4 ms to 7.5 ms using the SS2 register. The same ramp rate is also used for boost converter 1. Changing SS2 affects both boost converters.

5.5.2 Power-Down (Boost Converter 2)

Boost converter 2 is disabled when EN = 0 or $V_{IN} < V_{UVLO}$. The converter's output is not actively discharged when the converter is disabled. Once disabled (EN = 0), boost converter 1 remains disabled until the device is powered down (even if EN is re-asserted).

5.5.3 Setting the Output Voltage (Boost Converter 2)

The output voltage of boost converter 2 at cold temperatures can be programmed from 25 V to 40 V (2) using the VGHCOLD register. The output voltage of boost converter 2 at hot temperatures can be programmed from 16 V to 31 V using the VGHHOT register.

Note that if the VGHCOLD register is programmed with a lower voltage than the VGHHOT register, the output voltage V_{GH} will be regulated at $V_{GH(HOT)}$, regardless of the temperature.

In applications that do not require temperature compensation, the TCOMP pin should be tied to ground and the VGHHOT register used to set the voltage of V_{GH}.

From **Figure 5-8**, it can be seen that, between V_{GHHOT} and V_{GHCOLD}, boost converter 2's output voltage is given by

$$V_{GH} = 28 \times \left(V_{DAC2} + 3 \times \left(V_{TCOMP} - V_{DAC2}\right)\right) \tag{1}$$

---

(1) R_T should be a negative temperature coefficient (NTC) type whose resistance at 25°C is 10 kΩ.

(2) Output voltages greater than 36 V require an external cascode transistor.

Equation 1 can be used to calculate the voltage required on the TCOMP pin at temperatures T_{HOT} and T_{COLD}.

$$V_{TCOMPHOT} = \frac{V_{GHHOT}}{28} \tag{2}$$

$$V_{TCOMPCOLD} = \frac{2 \times V_{GHHOT} + V_{GHCOLD}}{84} \tag{3}$$

Equation 4 can be used to calculate the appropriate value for R_{T2}

$$R_{T2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{4}$$

Where

$$a = R_{NTCCOLD} - R_{NTCHOT} - \frac{V_{TCOMPCOLD} - V_{TCOMPHOT}}{I_{SET}} \tag{5}$$

$$b = (R_{NTCCOLD} + R_{NTCHOT}) \times \left(\frac{V_{TCOMPCOLD} - V_{TCOMPHOT}}{I_{SET}} \right) \tag{6}$$

$$c = (R_{NTCCOLD} \times R_{NTCHOT}) \times \left(\frac{V_{TCOMPCOLD} - V_{TCOMPHOT}}{I_{SET}} \right) \tag{7}$$

and $R_{NTCCOLD}$ and $R_{NTCCOLD}$ are the resistances of the thermistor at temperatures T_{COLD} and T_{HOT} respectively.

Once the value of R_{T2} has been calculated, Equation 8 can be used to calculate the appropriate value of R_{T1}.

$$R_{RT1} = \times \left(\frac{V_{TCOMPCOLD}}{I_{SET}} \right) - \left(\frac{R_{NTCCOLD} \times R_{T2}}{R_{NTCCOLD} + R_{T2}} \right) \tag{8}$$

5.5.4 *Protection (AV_{DD}, V_{CORE}, V_{IO1}, V_{IO2}, V_{GH})*

Each voltage regulator is protected against short-circuits and undervoltage conditions. An undervoltage condition is detected if a regulator output falls below 70% of its programmed voltage for longer than 50 ms, in which case the IC is disabled. To recover normal operation following an undervoltage condition, the cause of the error condition must be removed and the supply voltage V_{IN} cycled. A short-circuit condition is detected if a regulator output falls below 30% of its programmed voltage, in which case the IC is disabled immediately. To recover normal operation following a short-circuit condition, the cause of the error must be removed and the supply voltage V_{IN} cycled.

5.6 RESET GENERATOR

The $\overline{\text{RST}}$ pin generates an active-low reset signal for the timing controller. During power-up, the reset timer starts when V_{CORE} has finished ramping. The reset pulse duration t_{RESET} can be programmed from 2 ms to 16 ms using the RESET register. The $\overline{\text{RST}}$ signal is latched when it goes high and will not be taken low again until the device is powered down (even if V_{CORE} temporarily falls out of regulation). The active power-down threshold (V_{UVLO} or V_{DET}) can be selected using the RMODE bit in the CONFIG register.

The $\overline{\text{RST}}$ output is an open-drain type that requires an external pull-up resistor. Pull-up resistor values in the range 10 kΩ to 100 kΩ are recommended for most applications.

5.7 GATE VOLTAGE SHAPING

The gate voltage shaping function can be used to reduce image sticking in LCD panels by modulating the LCD panel's gate ON voltage (V_{GH}). Figure 5-9 shows a block diagram of the gate voltage shaping function and Figure 5-10 shows the typical waveforms during operation.

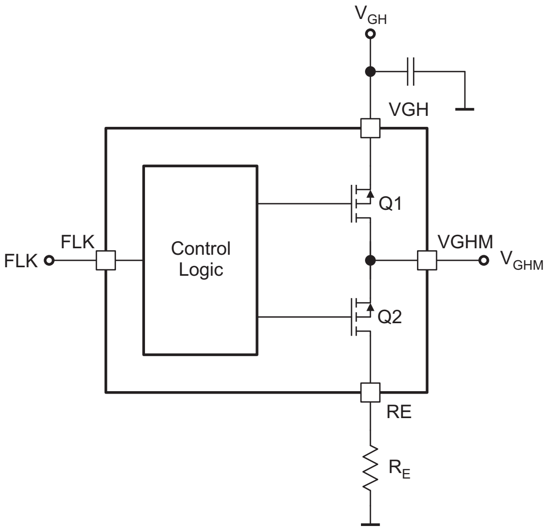


Figure 5-9. Gate Voltage Shaping Block Diagram

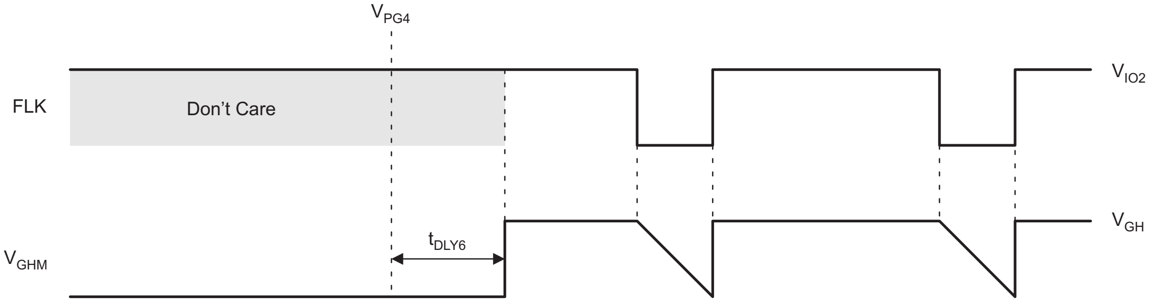


Figure 5-10. Gate Voltage Shaping Waveforms

Gate voltage shaping is controlled by the FLK input. When FLK is high, Q1 is on, Q2 is off, and V_{GHM} is equal to V_{GH}. On the falling edge of FLK, Q1 is turned off, Q2 is turned on, and the LCD panel load connected to the VGHM pin discharges through the external resistor connected to the RE pin.

During power-up Q2 is held permanently on and Q1 permanently off, regardless of the state of the FLK signal, until t_{DLY6} milliseconds after boost converter 2 (V_{GH}) has finished ramping. The value of t_{DLY6} can be programmed from 0ms to 35ms using the DLY6 register.

During power-down Q1 is held permanently on and Q2 permanently off, regardless of the state of the FLK signal.

5.7.1 Recommended Connection when Gate Voltage Shaping not Used

Non-GIP/Non-ASG panels that do not use the gate voltage shaping function should leave the RE pin floating and connect the FLK pin to either V_{IN} or GND.

5.8 PANEL RESET / LCD BIAS READY ($\overline{\text{XAO}}$)

The TPS65642 provides an output signal via its $\overline{\text{XAO}}$ pin that can be used to reset a level shifter or gate driver IC during power-up and power-down. The GIP bit in the CONFIG register defines whether the $\overline{\text{XAO}}$ pin works in GIP mode or non-GIP mode.

The primary purpose of the $\overline{\text{XAO}}$ signal in non-GIP applications is to drive the outputs of the display panel's gate driver IC high during power-down by generating an active-low signal. When the GIP = 0, the $\overline{\text{XAO}}$ pin is pulled low whenever $V_{IN} < V_{DET}$. The V_{DET} threshold voltage can be configured using the VDET register.

When the GIP = 1, the $\overline{\text{XAO}}$ output is used to delay the start of level shifter activity during power-up. The delay time t_{DLY6} starts when V_{GH} has finished ramping up, and can be configured using the DLY6 register.

The $\overline{\text{XAO}}$ output is an open-drain type and requires an external pull-up, typically in the range 10 kΩ to 100 kΩ.

5.9 PROGRAMMABLE VCOM CALIBRATOR (V_{COM})

The programmable VCOM calibrator uses a digital-to-analog converter (DAC) to generate an offset current I_{DAC} for an external resistor divider connected to AV_{DD} (see Figure 5-11 and Figure 5-12). Higher values of the 7-bit digital word N written to the DAC generate higher I_{DAC} sink currents, and therefore lower V_{COM} voltages.

Figure 5-11 shows the recommended circuit for the most commonly used application, when the LCD panel requires only one V_{COM} supply voltage. The second op-amp is shown wired as a unity-gain buffer whose input is tied to GND (the recommended configuration if it is not used), however, it is perfectly acceptable to use it for other things, such as generating a half-AV_{DD} supply rail.

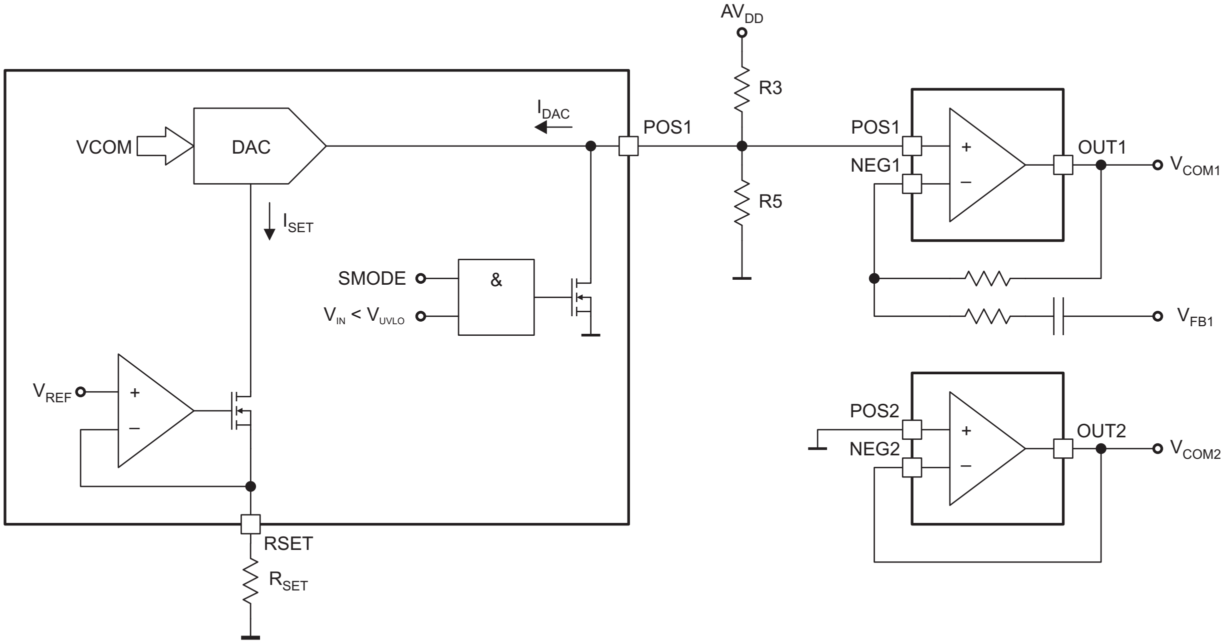


Figure 5-11. Single Programmable V_{COM} Supply

The external resistor R_{SET} generates a reference current I_{SET} for the DAC. Since this reference current is also used by boost converter 2's temperature compensation function, care should be taken to ensure that a suitable value is chosen. For most applications, a value of 24.9 kΩ is recommended, which generates a reference current given by

$$I_{SET} = \frac{V_{REF}}{R_{SET}}$$

$$I_{SET} = \frac{1.25\,\text{V}}{24.9\,\text{k}\Omega} = 50.2\,\mu\text{A} \qquad (9)$$

The output current I_{DAC} sunk by the DAC is given by:

$$I_{DAC} = \frac{(N+1) \times I_{SET}}{128} \qquad (10)$$

where N is the 7-bit word written to the DAC, and ranges from 0 to 127.

Equation 11 and Equation 12 can be used to select appropriate values for R3 and R5.

$$R3 = \frac{128 \times \Delta V_{COM} \times AV_{DD}}{I_{SET} \times \left(127 \times V_{COM(MAX)} + \Delta V_{COM}\right)} \tag{11}$$

$$R5 = \frac{128 \times \Delta V_{COM} \times R3}{\left(127 \times I_{SET} \times R3\right) - \left(128 \times \Delta V_{COM}\right)} \tag{12}$$

Figure 5-12 shows the recommended connection for the case when two V_{COM} supplies V_{COM1} and V_{COM2} are to be generated.

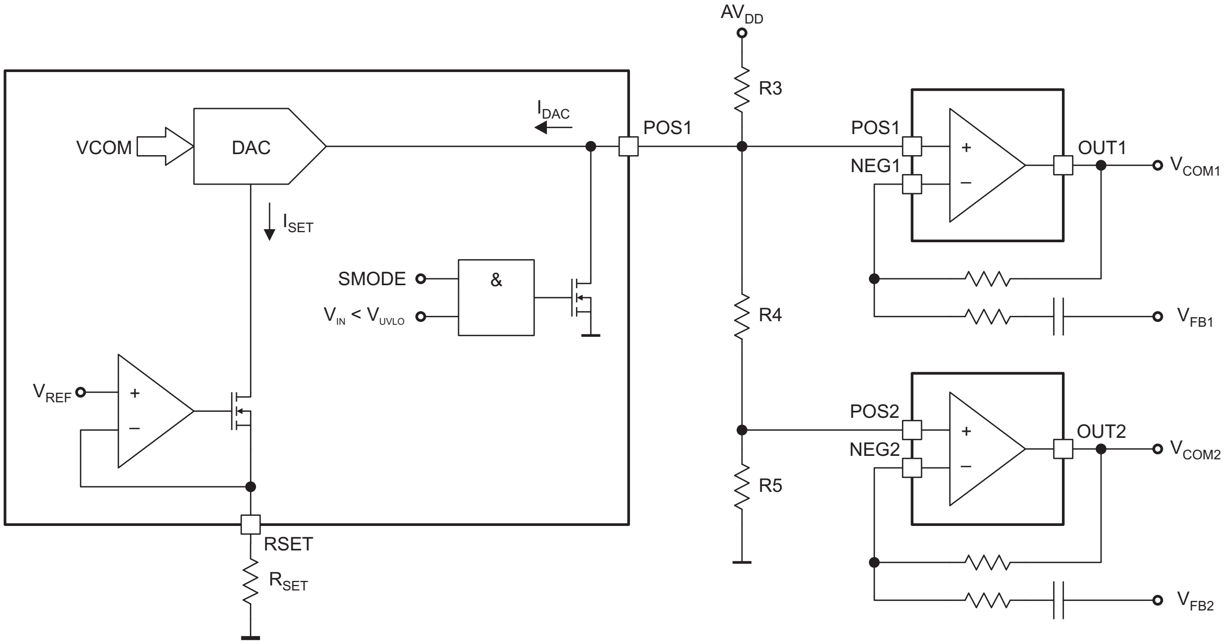


Figure 5-12. Dual Programmable V_{COM} Supplies

In Figure 5-12, the voltage V_{COM2} generated by the second op-amp is slightly lower than V_{COM1}. If two identical V_{COM} supplies are required, these can be generated by setting R4=0.

Equation 13 through Equation 15 can be used to calculate the correct values for R3 through R5 for the case when two (slightly different) V_{COM} voltages are required:

$$R3 = \frac{128 \times \Delta V_{COM} \times AV_{DD}}{I_{SET} \times \left(127 \times V_{COM1(MAX)} + \Delta V_{COM}\right)} \tag{13}$$

$$R4 = \left(\frac{V_{COM2(MAX)}}{V_{COM1(MAX)}}\right) \times \left(\frac{128 \times \Delta V_{COM} \times R3}{\left(127 \times I_{SET} \times R3\right) - \left(128 \times \Delta V_{COM}\right)}\right) \tag{14}$$

$$R5 = \left(\frac{V_{COM1(MAX)} - V_{COM2(MAX)}}{V_{COM1(MAX)}}\right) \times \left(\frac{128 \times \Delta V_{COM} \times R3}{\left(127 \times I_{SET} \times R3\right) - \left(128 \times \Delta V_{COM}\right)}\right) \tag{15}$$

A Microsoft Excel® spreadsheet is available free of charge that calculates the values of R3, R4 and R5 – contact your local sales representative for a copy.

5.9.1 Operational Amplifier Performance

Like most op amps, the V_{COM} op amps are not designed to drive purely capacitive loads, so it is not recommended to connect a capacitor directly to their outputs in an attempt to increase performance; however, the amplifiers are capable of delivering high peak currents that make such capacitors unnecessary.

High-speed op amps such as those in the TPS65642 require care when using them. The most common problem is when parasitic capacitance at the inverting input creates a pole with the feedback resistor, reducing amplifier stability. Two things can be done to minimize the likelihood of this happening. Both of these work by shifting the pole (which can never be completely eliminated) to a frequency outside the op amp's bandwidth, where it has no effect.

- Reduce the value of the feedback resistor. In applications where no feedback from the panel is used, the feedback resistor can be made zero. In applications where a non-zero feedback resistor has to be used, a small capacitor (10pF–100pF) across the feedback resistor will minimize ringing.
- Minimize the parasitic capacitance at the op amp's inverting input. This is achieved by using short PCB traces between the feedback resistor and the inverting input, and by removing ground planes and other copper areas above and below this PCB trace.

5.9.2 Power-Up (Programmable VCOM)

The programmable V_{COM} is enabled when $AV_{DD} > \approx 3$ V.

5.9.3 Power-Down (Programmable VCOM)

The programmable V_{COM} supports two kinds of power-down behavior, and the SMODE bit in the CONFIG register determines which one is active (see Figure 5-41 and Figure 5-42).

If SMODE = 0, the active discharge transistor Q1 is permanently disabled; during power-down, V_{COM} tracks AV_{DD} until it is too low to support operation. If SMODE = 1, Q1 turns on when $V_{IN} < V_{UVLO}$, actively pulling V_{COM} low.

5.10 PROGRAMMABLE GAMMA VOLTAGE GENERATOR

The gamma voltage correction supplies fourteen reference voltages that can be used by the system's source driver IC to match the LCD panel's luminance characteristics more closely to the response of the human eye.

The gamma correction voltages can be programmed individually using the I^2C interface. During power-up, the default gamma voltage for each channel is loaded from EEPROM into the corresponding DAC.

During operation, the DACs' output voltages can be changed by programming new values via the I^2C interface. Values programmed to the DACs but not transferred to EEPROM will be lost when power is removed from the device – the next time the device is powered up, the DACs will be programmed with whatever values are stored in the EEPROM. The current DAC settings can be transferred to EEPROM (thereby becoming the new default values used during power-up) at any time by sending the appropriate command to the Control Register via the I^2C interface.

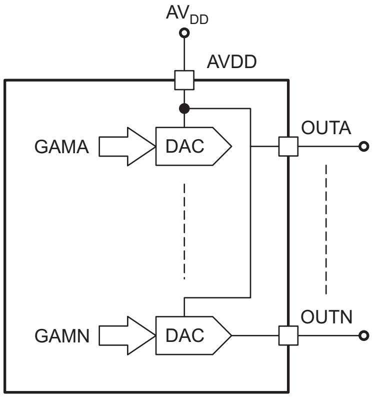


Figure 5-13. Gamma Correction Block Diagram

The output stages of the gamma correction block are capable of extending close to the supply rails (AV_{DD} and ground); however, they can only achieve this rail-to-rail performance with the specified accuracy if the outputs are lightly loaded. The gamma reference outputs are only intended to drive high impedance loads such as those presented by a gamma buffer or a high impedance source driver input.

The output voltage V_{GAM} of each channel is given by:

$$V_{GAM} = \frac{N}{1024} \cdot AV_{DD} \tag{16}$$

Where N is the 10-bit digital word programmed to the gamma register and ranges from 0 to 1023.

Any non-used output can be left open and should, to save power, be programmed to their maximum voltage (~ 180 µA saving per output).

5.11 Configuration

The TPS65642 divides the configuration parameters into two categories:

- V_{COM}
- all other configuration parameters

In typical applications, all configuration parameters except V_{COM} are programmed by the subcontractor during PCB assembly, and V_{COM} is programmed by the display manufacturer during display calibration.

5.11.1 RAM, EEPROM, and Write Protect

Configuration parameters can be changed by writing the desired values to the appropriate RAM register(s). The RAM registers are volatile and their contents are lost when power is removed from the device. By writing to the Control Register, it is possible to store the active configuration in non-volatile EEPROM; during power-up, the contents of the EEPROM are copied into the RAM registers and used to configure the device.

An active high Write Protect (WP) pin prevents the configuration parameters from being changed by accident. This pin is internally pulled high and must be actively pulled low to access to the EEPROM or RAM registers. Note that the WP pin disables all I^2C traffic to/from the TPS65642, and must also be pulled low during read operations. This is to ensure that noise present on the I^2C lines does not erroneously overwrite the active configuration stored in RAM (which would not be protected by a simple EEPROM write-protect scheme).

5.11.2 Configuration Parameters (Excluding VCOM)

Table 5 shows the memory map of the configuration parameters.

Table 5-1. Configuration Memory Map

REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
00h	CONFIG	00h	Sets miscellaneous configuration bits
01h	AVDD	10h	Sets the output voltage of boost converter 1
02h	VGHHOT	00h	Sets the output voltage of boost converter 2 at high temperatures
03h	VGHCOLD	00h	Sets the output voltage of boost converter 2 at low temperatures
04h	VIO	00h	Sets the output voltage of buck converter 2 and the LDO regulator
05h	MISC	05h	Sets the output voltage of buck converter 1 (V_{CORE}) and the switching frequency of boost converter 1 (AV_{DD})
06h	SS1	03h	Sets the soft-start time for buck converters 1 and 2 and the linear regulator
07h	SS2	00h	Sets the soft-start time for boost converters 1 and 2
08h	RESET	01h	Sets the reset pulse duration
09h	DLY1	02h	Sets the boost converter 1 start-up delay

Table 5-1. Configuration Memory Map (continued)

REGISTER ADDRESS	REGISTER NAME	FACTORY DEFAULT	DESCRIPTION
0Ah	DLY6	04h	Sets the gate voltage shaping / LCD ready start-up delay
0Bh	VDET	00h	Sets the threshold of the /RST and /XAO signals
0Ch	GAMMA-A	02h	Contains the 2 MSBs of the 10-bit gamma voltage A
0Dh		00h	Contains the 8 LSBs of the 10-bit gamma voltage A
0Eh	GAMMA-B	02h	Contains the 2 MSBs of the 10-bit gamma voltage B
0Fh		00h	Contains the 8 LSBs of the 10-bit gamma voltage B
10h	GAMMA-C	02h	Contains the 2 MSBs of the 10-bit gamma voltage C
11h		00h	Contains the 8 LSBs of the 10-bit gamma voltage C
12h	GAMMA-D	02h	Contains the 2 MSBs of the 10-bit gamma voltage D
13h		00h	Contains the 8 LSBs of the 10-bit gamma voltage D
14h	GAMMA-E	02h	Contains the 2 MSBs of the 10-bit gamma voltage E
15h		00h	Contains the 8 LSBs of the 10-bit gamma voltage E
16h	GAMMA-F	02h	Contains the 2 MSBs of the 10-bit gamma voltage F
17h		00h	Contains the 8 LSBs of the 10-bit gamma voltage F
18h	GAMMA-G	02h	Contains the 2 MSBs of the 10-bit gamma voltage G
19h		00h	Contains the 8 LSBs of the 10-bit gamma voltage G
1Ah	GAMMA-H	02h	Contains the 2 MSBs of the 10-bit gamma voltage H
1Bh		00h	Contains the 8 LSBs of the 10-bit gamma voltage H
1Ch	GAMMA-I	02h	Contains the 2 MSBs of the 10-bit gamma voltage I
1Dh		00h	Contains the 8 LSBs of the 10-bit gamma voltage I
1Eh	GAMMA-J	02h	Contains the 2 MSBs of the 10-bit gamma voltage J
1Fh		00h	Contains the 8 LSBs of the 10-bit gamma voltage J
20h	GAMMA-K	02h	Contains the 2 MSBs of the 10-bit gamma voltage K
21h		00h	Contains the 8 LSBs of the 10-bit gamma voltage K
22h	GAMMA-L	02h	Contains the 2 MSBs of the 10-bit gamma voltage L
23h		00h	Contains the 8 LSBs of the 10-bit gamma voltage L
24h	GAMMA-M	02h	Contains the 2 MSBs of the 10-bit gamma voltage M
25h		00h	Contains the 8 LSBs of the 10-bit gamma voltage M
26h	GAMMA-N	02h	Contains the 2 MSBs of the 10-bit gamma voltage N
27h		00h	Contains the 8 LSBs of the 10-bit gamma voltage N
FFh	Control	00h	Controls whether read and write operations access RAM or EEPROM registers

5.11.3 CONFIG (00h)

Figure 5-14. CONFIG Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					RMODE	SMODE	GIP
					R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-2. CONFIG Register Field Descriptions

Bit	Field	Value	Description
7–3	Not implemented.	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
2	RMODE		Configures the $\overline{\text{RST}}$ power-down threshold voltage.
		0	**V_{UVLO} threshold used.**
		1	V_{DET} Threshold used.
1	SMODE		Configures the power-down behavior of AV_{DD} and V_{COM}.
		0	**AV_{DD} is actively discharged (but not V_{COM}).**
		1	V_{COM} is actively discharged (but not AV_{DD}).
0	GIP		This bit configures the device for use with either GIP or non-GIP LCD panels.
		0	**The device operates in non-GIP mode, and XAO functions as a panel reset during power-down.**
		1	The device operates in GIP mode, and the $\overline{\text{XAO}}$ functions as an enable for the panel's level shifter

5.11.4 AVDD (01h)

Figure 5-15. AVDD Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented			AVDD				
			R/W-*1*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-3. AVDD Register Field Descriptions

Bit	Field	Value	Description
7–4	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
4–0	AVDD		These bits configure boost converter 1's output voltage (AV_{DD}).
		00h	6.0 V
		01h	6.1 V
		02h	6.2 V
		03h	6.3 V
		04h	6.4 V
		05h	6.5 V
		06h	6.6 V
		07h	6.7 V
		08h	6.8 V
		09h	6.9 V
		0Ah	7.0 V
		0Bh	7.1 V
		0Ch	7.2 V
		0Dh	7.3 V
		0Eh	7.4 V
		0Fh	7.5 V
		10h	**7.6 V**
		11h	7.7 V
		12h	7.8 V
		13h	7.9 V
		14h	8.0 V
		15h	8.1 V
		16h	8.2 V
		17h	8.3 V
		18h	8.4 V
		19h	8.5 V
		1Ah	8.6 V
		1Bh	8.7 V
		1Ch	8.8 V
		1Dh	8.9 V
		1Eh	9.0 V
		1Fh	9.1 V

5.11.5 VGHHOT (02h)

Figure 5-16. VGHHOT Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				VGHHOT			
				R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-4. VGHHOT Register Field Descriptions

Bit	Field	Value	Description
7–4	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
3–0	VGHHOT		These bits configure boost converter 2's output voltage (V_{GH}) at high temperatures.
		0h	**16 V**
		1h	17 V
		2h	18 V
		3h	19 V
		4h	20 V
		5h	21 V
		6h	22 V
		7h	23 V
		8h	24 V
		9h	25 V
		Ah	26 V
		Bh	27 V
		Ch	28 V
		Dh	29 V
		Eh	30 V
		Fh	31 V

5.11.6 VGHCOLD (03h)

Figure 5-17. VGHCOLD Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented				VGHCOLD			
				R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-5. VGHCOLD Register Field Descriptions

Bit	Field	Value	Description
7–4	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
3–0	VGHCOLD		These bits configure boost converter 2's output voltage (V_{GH}) at low temperatures.
		0h	**25 V**
		1h	26 V
		2h	27 V
		3h	28 V
		4h	29 V
		5h	30 V
		6h	31 V
		7h	32 V
		8h	33 V
		9h	34 V
		Ah	35 V
		Bh	36 V
		Ch	37 V
		Dh	38 V
		Eh	39 V
		Fh	40 V

5.11.7 VIO (04h)

Figure 5-18. VIO Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented						VIO	
						R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-6. VIO Register Field Descriptions

Bit	Field	Value	Description
7–2	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
1–0	VIO		These bits configure the output voltage of buck converter 2 (V_{IO1}) and the LDO regulator (V_{IO2}). To ensure reliable LDO programming, EN has to be "high" and the power-up sequence must be over (t_{DLY6}).
		0h	**V_{IO1}=1.7 V, LDO regulator disabled.**
		1h	V_{IO1}=1.8 V, LDO regulator disabled.
		2h	V_{IO1}=2.5 V, V_{IO2}=1.7 V.
		3h	V_{IO1}=2.5 V, V_{IO2}=1.8 V.

5.11.8 MISC (05h)

Figure 5-19. MISC Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					FREQ	VCORE	
					R/W-*1*	R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-7. MISC Register Field Descriptions

Bit	Field	Value	Description
7–3	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
2	FREQ		This bit configures the switching frequency of boost converter 1 (AV_{DD}).
		0h	750 kHz
		1h	**1200 kHz**
1–0	VCORE		These bits configure the output voltage of buck converter 1 (V_{CORE}).
		0h	1.0 V
		1h	**1.1 V**
		2h	1.2 V
		3h	1.3 V

5.11.9 SS1 (06h)

Figure 5-20. SS1 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					SS1		
					R/W-*0*	R/W-*1*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-8. SS1 Register Field Descriptions

Bit	Field	Value	Description
7–3	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
2–0	SS1		These bits configure the soft-start time for buck converter 1 (V_{CORE}), buck converter 2 (V_{IO1}) and the LDO linear regulator (V_{IO2}).
		0h	0.5 ms
		1h	1.0 ms
		2h	1.5 ms
		3h	**2.0 ms**
		4h	2.5 ms
		5h	3.0 ms
		6h	3.5 ms
		7h	4.0 ms

5.11.10 SS2 (07h)

Figure 5-21. SS2 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					SS2		
					R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-9. SS2 Register Field Descriptions

Bit	Field	Value	Description
7–3	Not Implemented	N/A 0 1	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
2–0	SS2		These bits configure the soft-start time for boost converter 1 (AV_{DD}) and boost converter 2 (V_{GH}).
		0h	**4.0 ms**
		1h	4.5 ms
		2h	5.0 ms
		3h	5.5 ms
		4h	6.0 ms
		5h	6.5 ms
		6h	7.0 ms
		7h	7.5 ms

5.11.11 RESET (08h)

Figure 5-22. RESET Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented						RESET	
						R/W-*0*	R/W-*1*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-10. RESET Register Field Descriptions

Bit	Field	Value	Description
7–2	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
1–0	RESET		These bits configure the duration of the reset pulse during start-up.
		0h	2 ms
		1h	**4 ms**
		2h	8 ms
		3h	16 ms

5.11.12 DLY1 (09h)

Figure 5-23. DLY1 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					DLY1		
					R/W-*0*	R/W-*1*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-11. DLY1 Register Field Descriptions

Bit	Field	Value	Description
7–3	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
2–0	DLY1		These bits configure the start-up delay for boost converter 1 (AV_{DD}).
		0h	0 ms
		1h	10 ms
		2h	**20 ms**
		3h	30 ms
		4h	40 ms
		5h	50 ms
		6h	60 ms
		7h	70 ms

5.11.13 DLY6 (0Ah)

Figure 5-24. DLY6 Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					DLY6		
					R/W-*1*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-12. DLY6 Register Field Descriptions

Bit	Field	Value	Description
7–3	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
2–0	DLY6		These bits configure the delay between V_{GH} reaching its final value and gate voltage shaping or $\overline{\text{XAO}}$ being enabled.
		0h	0 ms
		1h	5 ms
		2h	10 ms
		3h	15 ms
		4h	**20 ms**
		5h	25 ms
		6h	30 ms
		7h	35 ms

5.11.14 VDET (0Bh)

Figure 5-25. VDET Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented					VDET		
					R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-13. VDET Register Field Descriptions

Bit	Field	Value	Description
7–3	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
2–0	VDET		These bits configure the threshold for $\overline{\text{XAO}}$ and $\overline{\text{RST}}$ (if RMODE is "1" in the CONFIG register).
		0h	**2.2 V**
		1h	2.3 V
		2h	2.4 V
		3h	2.5 V
		4h	3.6 V
		5h	3.7 V
		6h	3.8 V
		7h	3.9 V

5.11.15 GAMxHI (0Ch, 0Eh…26h)

Figure 5-26. GAMxHI Register Bit Allocation

7	6	5	4	3	2	1	0
Not Implemented						GAMxHI	
						R/W-*1*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = factory default

Table 5-14. GAMxHI Register Field Descriptions

Bit	Field	Value	Description
7–2	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
1–0	GAMxHI	0h–3h	These bits form the two most significant bits of the 10-bit GAMx value used to program the gamma correction voltage for channel x.

5.11.16 GAMxLO (0Dh, 0Fh…27h)

Figure 5-27. GAMxLO Register Bit Allocation

7	6	5	4	3	2	1	0
GAMxLO							
R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = factory default

Table 5-15. GAMxLO Register Field Descriptions

Bit	Field	Value	Description
7–0	GAMxLO	00h–FFh	These bits form the least significant eight bits of the 10-bit value used to program the gamma correction voltage for channel x.

5.11.17 Control (FFh)

Figure 5-28. CONTROL Register Bit Allocation

7	6	5	4	3	2	1	0
WED	Not Implemented						RED
R/W-*0*							R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-16. CONTROL Register Field Descriptions

Bit	Field	Value	Description
7	RED		This bit configures the data returned by read operations.
		0	**Read operations return the contents of the DAC registers.**
		1	Read operations return the content of the EEPROM registers.
6–1	Not Implemented	N/A	These bits are not implemented in hardware. During write operations data for these bits is ignored, and during read operations 0 is returned.
0	WED		Setting this bit forces the contents of all DAC registers to be copied to the EEPROM, thereby making them the default values during power-up.
		0	**Not used. This bit is automatically reset to 0 when the contents of the DAC registers have been copied to EEPROM.**
		1	The contents of all DAC registers are copied to the EEPROM, making them the new default values following power-up.

5.11.18 Example – Writing to a Single RAM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65642 acknowledges
4. Bus master sends address of RAM register (00h)
5. TPS65642 acknowledges
6. Bus master sends data to be written
7. TPS65642 acknowledges
8. Bus master sends STOP condition

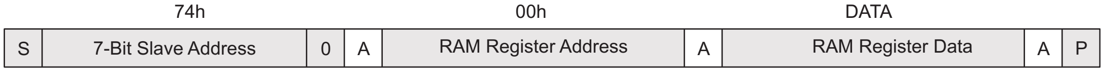


Figure 5-29. Writing to a Single RAM Register

5.11.19 Example – Writing to Multiple RAM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h).
3. TPS65642 acknowledges
4. Bus master sends address of first RAM register to be written to (00h)
5. TPS65642 acknowledges
6. Bus master sends data to be written to first RAM register
7. TPS65642 acknowledges
8. Bus master sends data to be written to RAM register at next higher address (auto-increment)
9. TPS65642 acknowledges
10. Steps (8) and (9) repeated until data for final RAM register has been sent
11. TPS65642 acknowledges
12. Bus master sends STOP condition

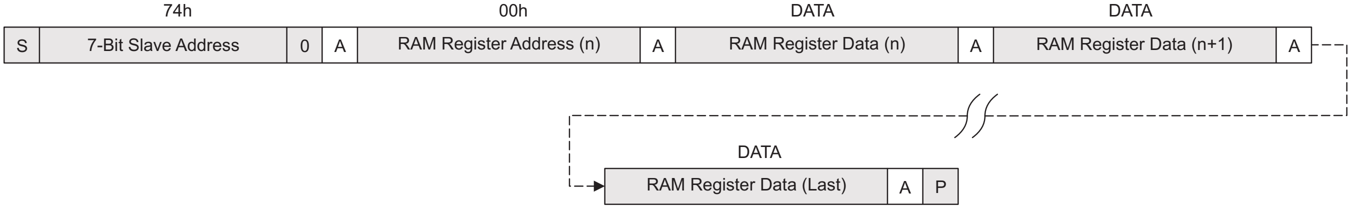
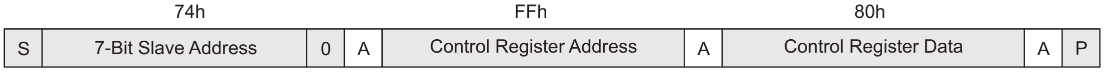


Figure 5-30. Writing to Multiple RAM Registers

5.11.20 Example – Saving Contents of all RAM Registers to EEPROM

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65642 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65642 acknowledges
6. Bus master sends data to be written to the Control Register (80h)
7. TPS65642 acknowledges
8. Bus master sends STOP condition



	74h			FFh		80h		
S	7-Bit Slave Address	0	A	Control Register Address	A	Control Register Data	A	P

Figure 5-31. Saving Contents of all RAM Registers to E^2PROM

5.11.21 Example – Reading from a Single RAM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65642 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65642 acknowledges
6. Bus master sends data for Control Register (00h)
7. TPS65642 acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (E8h)
11. TPS65642 acknowledges
12. Bus master sends address of RAM register (00h)
13. TPS65642 acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (E9h)
16. TPS65642 acknowledges
17. TPS65642 sends RAM register data
18. Bus master does not acknowledge
19. Bus master sends STOP condition

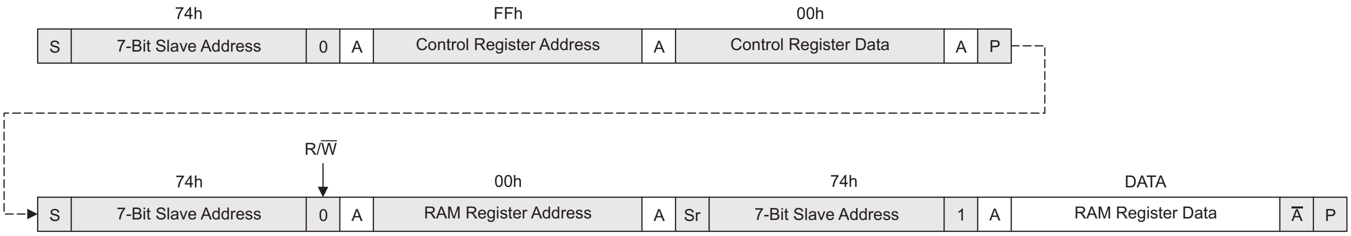


Figure 5-32. Reading from a Single RAM Register

5.11.22 Example – Reading from a Single EEPROM Register

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65642 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65642 acknowledges
6. Bus master sends data for Control Register (01h)
7. TPS65642 acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (E8h)
11. TPS65642 acknowledges
12. Bus master sends address of EEPROM register (00h)
13. TPS65642 acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (E9h)
16. TPS65642 acknowledges
17. TPS65642 sends EEPROM register data
18. Bus master does not acknowledge
19. Bus master sends STOP condition

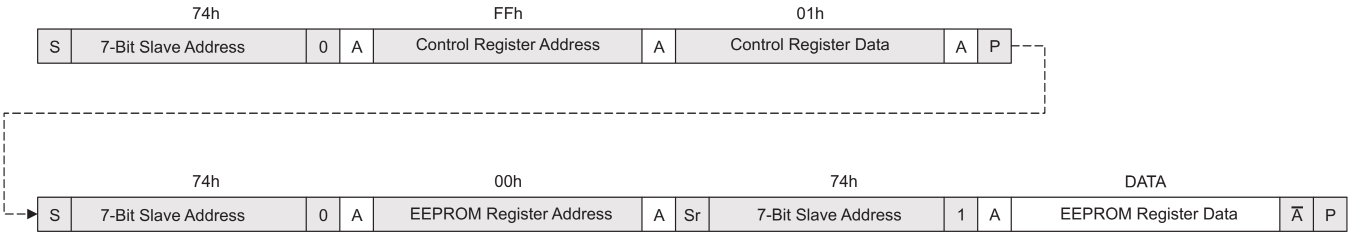


Figure 5-33. Reading from a Single EEPROM Register

5.11.23 Example – Reading from Multiple RAM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65642 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65642 acknowledges
6. Bus master sends data for Control Register (00h)
7. TPS65642 acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (E8h)
11. TPS65642 acknowledges
12. Bus master sends address of first register to be read (00h)
13. TPS65642 acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (E9h)
16. TPS65642 acknowledges
17. TPS65642 sends contents of first RAM register to be read
18. Bus master acknowledges
19. TPS65642 sends contents of second RAM register to be read
20. Bus master acknowledges
21. TPS65642 sends contents of third (last) RAM register to be read
22. Bus master does not acknowledge
23. Bus master sends STOP condition

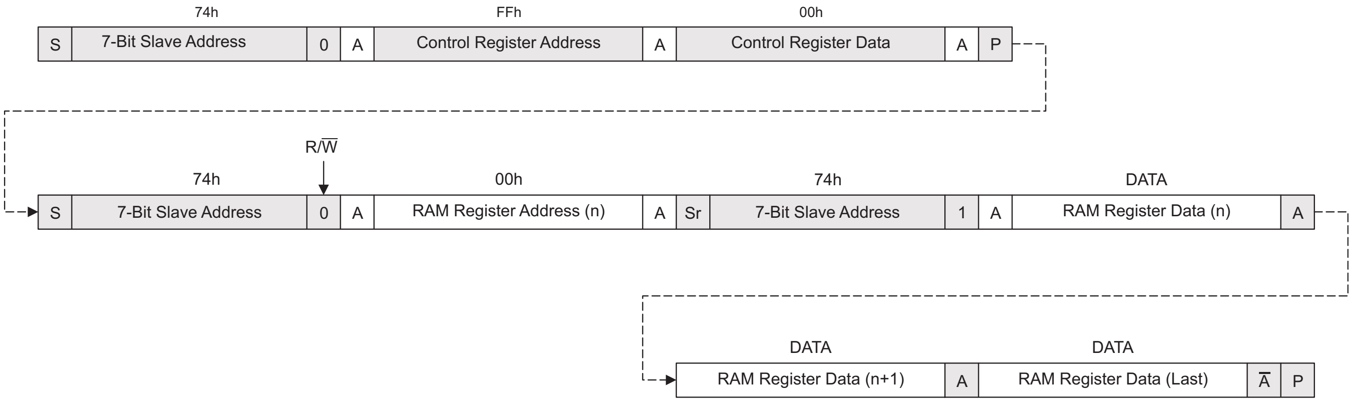


Figure 5-34. Reading from Multiple RAM Registers

5.11.24 Example – Reading from Multiple EEPROM Registers

1. Bus master sends START condition
2. Bus master sends 7-bit slave address plus low R/W bit (E8h)
3. TPS65642 acknowledges
4. Bus master sends address of Control Register (FFh)
5. TPS65642 acknowledges
6. Bus master sends data for Control Register (01h)
7. TPS65642 acknowledges
8. Bus master sends STOP condition
9. Bus master sends START condition
10. Bus master sends 7-bit slave address plus low R/W bit (E8h)
11. TPS65642 acknowledges
12. Bus master sends address of first EEPROM register to be read (00h)
13. TPS65642 acknowledges
14. Bus master sends REPEATED START condition
15. Bus master sends 7-bit slave address plus high R/W bit (E9h)
16. TPS65642 acknowledges
17. TPS65642 sends contents of first EEPROM register to be read
18. Bus master acknowledges
19. TPS65642 sends contents of second EEPROM register to be read
20. Bus master acknowledges
21. TPS65642 sends contents of third (last) EEPROM register to be read
22. Bus master does not acknowledge
23. Bus master sends STOP condition

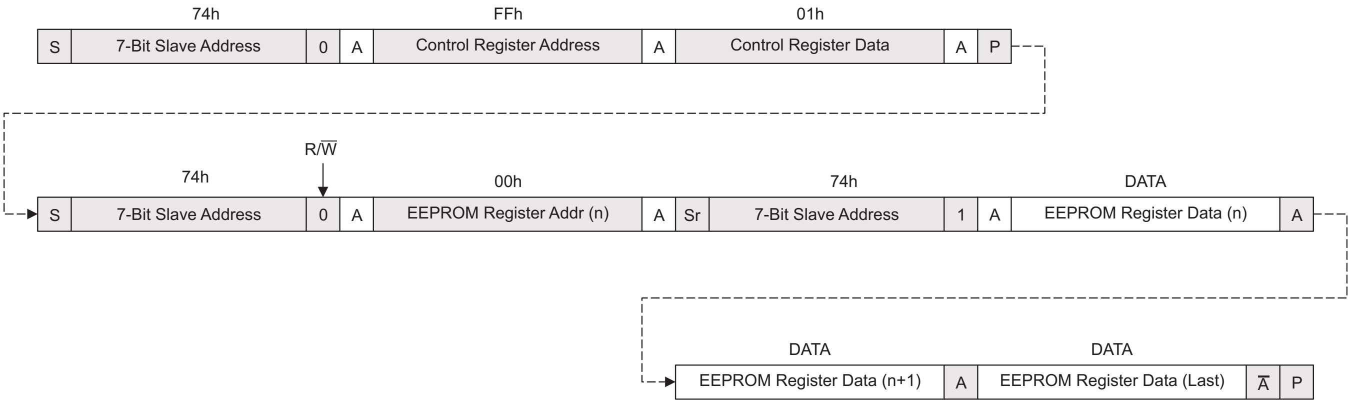


Figure 5-35. Reading from Multiple EEPROM Registers

5.11.25 Configuration Parameter VCOM

Figure 5-36. VCOM Register Bit Allocation

7	6	5	4	3	2	1	0
VCOM							P
R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*	R/W-*0*

LEGEND: R/W = Read/Write; R = Read only; -*n* = **factory default**

Table 5-17. VCOM Register Field Descriptions

Bit	Field	Value	Description
7–1	VCOM	00h–7Fh	During write operations these bits contain the data to be written. During read operations these bits contain the contents of the EEPROM register. $I_{OUT} = \frac{V_{REF}}{R_{SET}} \times \frac{VCOM + 1}{128}$
0	P		During write operations this bit configures the destination for data.
		0	**Data is written to the DAC register and EEPROM.**
		1	Data is written to the DAC register only.
			During read operations this bit indicates whether the contains of the RAM register and EEPROM are the same or not.
		0	**DAC register and EEPROM contents are the same.**
		1	DAC register and EEPROM contents are different.

5.11.26 Example – Writing a VCOM Value of 77h to RAM Register Only

1. Bus master sends a START condition.
2. Bus master sends 9E hexadecimal (7-bit slave address plus low R/W bit).
3. TPS65642 slave acknowledges.
4. Bus master sends EF hexadecimal (data to be written plus LSB = '1').
5. TPS65642 slave acknowledges.
6. Bus master sends a STOP condition.

	4Fh			77h			
S	7-Bit Slave Address	0	A	Data to be Written	1	A	P

Figure 5-37. Writing a VCOM Value of 77h to RAM Only

5.11.27 Example – Writing a VCOM Value of 77h to EEPROM and RAM

1. Bus master sends a START condition.
2. Bus master sends 9E hexadecimal (7-bit slave address plus low R/W bit).
3. TPS65642 slave acknowledges.
4. Bus master sends EE hexadecimal (data to be written plus LSB = '0').
5. TPS65642 slave acknowledges.
6. Bus master sends a STOP condition.

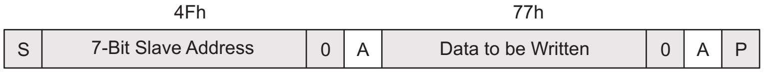


Figure 5-38. Writing a VCOM Value of 77h to EEPROM and RAM

5.11.28 Example – Reading a VCOM Value of 77h from EEPROM when RAM Contents are Identical

1. Bus master sends a START condition.
2. Bus master sends 9F hexadecimal (7-bit slave address plus high R/W bit).
3. TPS65642 slave acknowledges.
4. TPS65642 sends EE hexadecimal from EEPROM (data to be read plus LSB = '0').
5. Bus master does not acknowledge.
6. Bus master sends a STOP condition.

Figure 5-39. Reading 77h from EEPROM when RAM Contents are Identical

5.11.29 Example – Reading a VCOM Value of 77h from EEPROM when RAM Contents are Different

1. Bus master sends a START condition.
2. Bus master sends 9F hexadecimal (7-bit slave address plus high R/W bit).
3. TPS65642 slave acknowledges.
4. TPS65642 sends EF hexadecimal from RAM (data to be read plus LSB = '0').
5. Bus master does not acknowledge.
6. Bus master sends a STOP condition.

Figure 5-40. Reading 77h from EEPROM when RAM Contents are Different

5.11.30 I²C Interface

Configuration parameters and the V_{COM} voltage setting are programmed via an industry standard I^2C serial interface. TheTPS65642 always works as a slave device and supports standard (100 kbps) and fast (400 kbps) modes of operation. During write operations, all further attempts to access its slave addresses are ignored until the current write operation has completed.

The I^2C interface contains a known bug. If a new start condition appears on the bus before transfer of the slave address byte from a previously initiated read/write operation is complete, the I^2C interface may hang. Normal operation is recovered after cycling V_{IN}.

5.12 Power Sequencing

Buck converter 2 (V_{IO1}) and the linear regulator (V_{IO2}) start as soon as $V_{IN} > V_{UVLO}$.

Buck converter 1 (V_{CORE}) starts as soon as V_{IO1} and V_{IO2} have finished ramping up.

The reset generator holds $\overline{RST}$ low until t_{RESET} seconds after V_{CORE} has reached power good status.

Boost converter 1 starts t_{DLY1} milliseconds after EN goes high (or $\overline{RST}$ has gone high, whichever occurs later). Once asserted, the EN signal must remain high to ensure normal device operation. Once disabled (EN = 0), boost converter 1 remains disabled until the device is powered down (even if EN is re-asserted).

Boost converter 2 starts as soon as AV_{DD} has reached power good status.

In non-GIP mode, V_{GHM} is held high impedance until t_{DLY6} milliseconds after V_{GH} reaches power good status; $\overline{XAO}$ goes high when $V_{IN} > V_{DET}$ and low when $V_{IN} < V_{DET}$.

In GIP mode, $\overline{XAO}$ is held low until t_{DLY6} milliseconds after V_{GH} reaches power good status.

Figure 5-41 and Figure 5-42 show the typical power-up/down characteristic of the TPS65642.

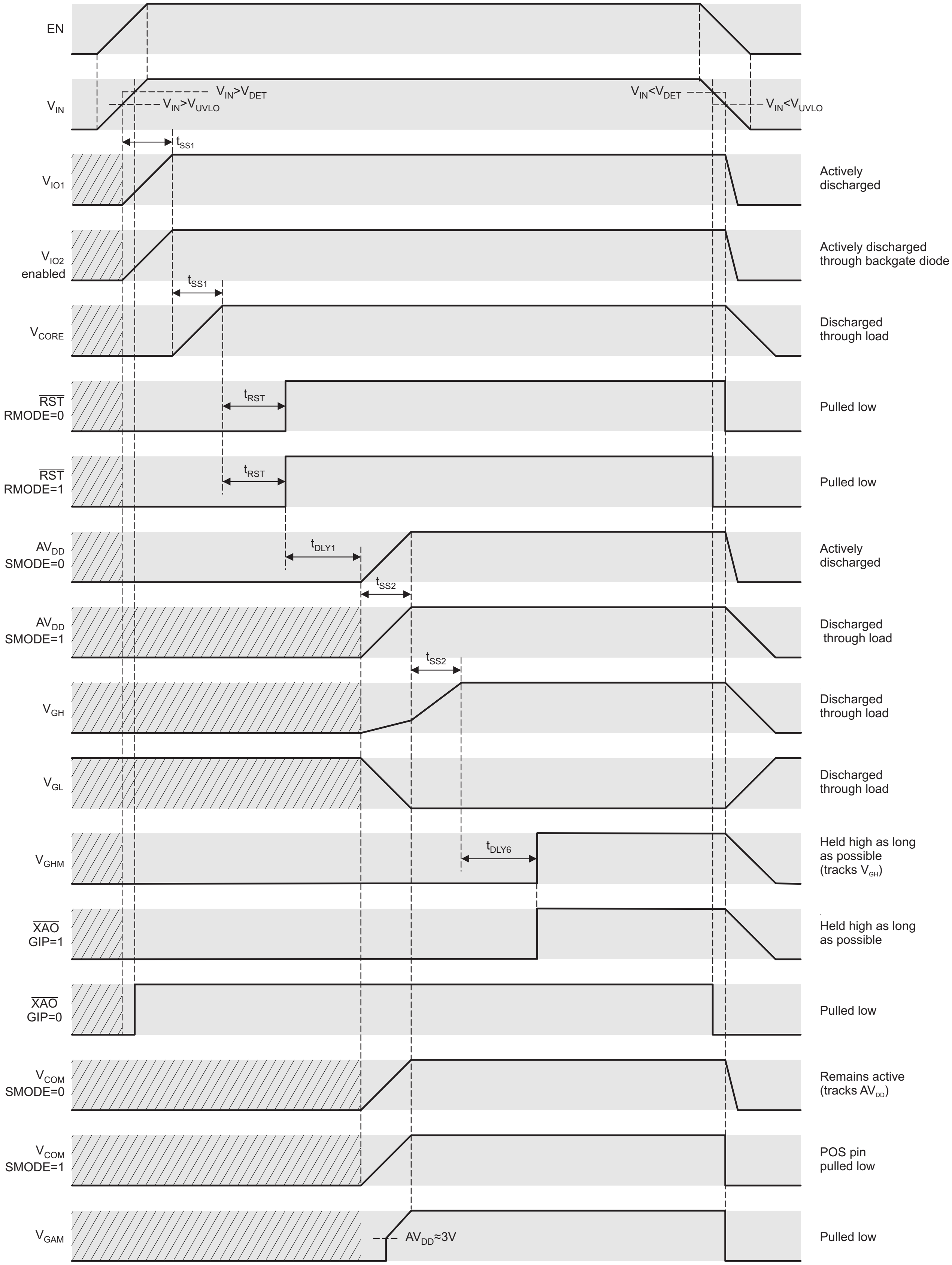


Figure 5-41. Power Up/Down Sequencing with EN Connected to V_{IN}

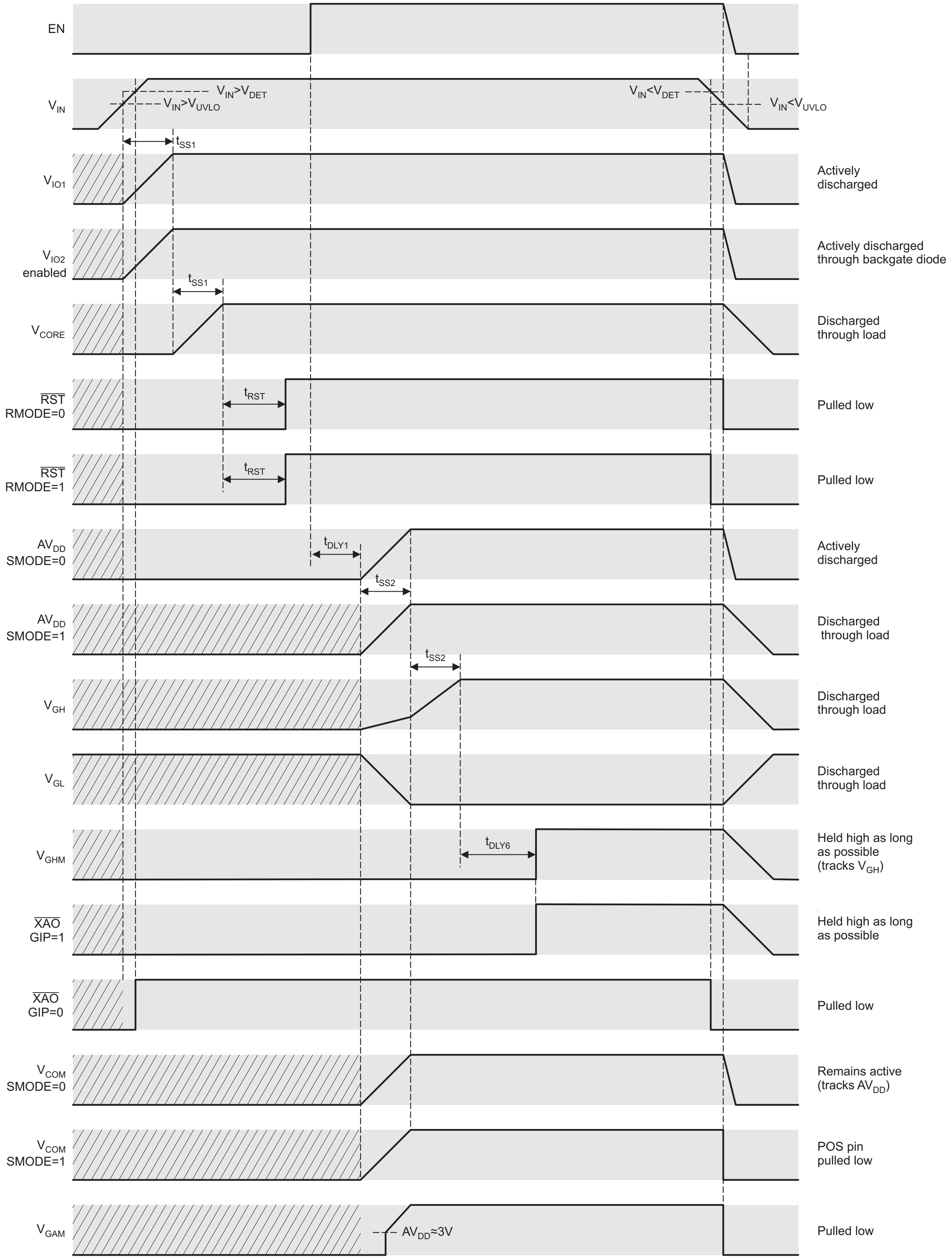


Figure 5-42. Power Up/Down Sequencing with EN Connected to T-CON Ready

5.13 Undervoltage Lockout

An undervoltage lockout function disables the TPS65642 when the supply voltage is too low for proper operation.

6 Application Information

6.1 External Component Selection

Care should be applied to the choice of external components since they greatly affect overall performance. The TPS65642 was developed with the twin goals of high performance and small/low-profile solution size. Since these two goals are often in direct opposition to one another (e.g. larger inductors tend to achieve higher efficiencies), some trade-off is always necessary.

Inductors must have adequate current capability so that they do not saturate under worst-case conditions. For high efficiency, they should also have low dc resistance (DCR).

Capacitors must have adequate *effective* capacitance under the applicable dc bias conditions they experience in the application. MLCC capacitors typically exhibit only a fraction of their nominal capacitance under real-world conditions and this must be taken into consideration when selecting them. This problem is especially acute in low profile capacitors, in which the dielectric field strength is higher than in taller components. In general, the capacitance values shown in circuit diagrams in this data sheet refer to the *effective* capacitance after dc bias effects have been taken into consideration. Reputable capacitor manufacturers provide capacitance versus dc bias curves that greatly simplify component selection.

The following tables list some components suitable for use with the TPS65642. The list is not exhaustive – other components may exist that are equally suitable (or better), however, these components have been proven to work well and were used extensively during the development of the TPS65642.

Table 6-1. Boost Converter 1 External Components

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	THICKNESS
L	Chip Inductor, 4.7 µH, ±20%	1269AS-H-4R7N	Toko	<1.0mm
C_{IN}	Ceramic Capacitor, X5R, 10 µF, 16 V, ±20%	GRM319R61H475MA12	Murata	<0.85mm
C_{OUT}				

Table 6-2. Buck Converter 1 External Component Recommendations

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	THICKNESS
L	Chip Inductor	1269AS-H-2R2N	Toko	<1.0mm
C_{OUT}	Ceramic Capacitor, X5R, 10 µF, 6.3 V, ±20%	GRM319R61H475MA12	Murata	<0.85mm

Table 6-3. Buck Converter 2 External Component Recommendations

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	THICKNESS
L	Chip Inductor	1269AS-H-2R2	Toko	<1.0mm
C_{OUT}	Ceramic Capacitor, X5R, 10 µF, 6.3 V, ±20%	GRM319R61H475MA12	Murata	<0.85mm

Table 6-4. LDO Regulator External Component Recommendations

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	THICKNESS
C_{OUT}	Ceramic Capacitor, X5R, 10 µF, 6.3 V, ±20%	GRM319R61H475MA12	Murata	<0.85mm

Table 6-5. Boost Converter 2 External Components

REF.	DESCRIPTION	PART NUMBER	MANUFACTURER	THICKNESS
L	Wirewound Inductor, 15 µH, ±20%	1156AS-150M	Toko	<1.0mm
L	Wirewound Inductor, 15 µH, ±20%	LQH3NPN150NG0	Murata	<1.0mm
C_{OUT}	Ceramic Capacitor, X5R, 4.7 µF, 50 V, ±20%	GRM319R61H475MA12	Murata	<0.85mm
D	Switching Diode, 150 mA, 75 V, 350 mW	BAS16W	Infineon	<1.0mm

6.2 Typical Application Circuit

Figure 6-1 and Figure 6-2 show the recommended application circuits for non-GIP and GIP displays respectively. Minor changes may be needed to optimize the circuit for a specific application, however, the basic circuit is unlikely to change significantly.

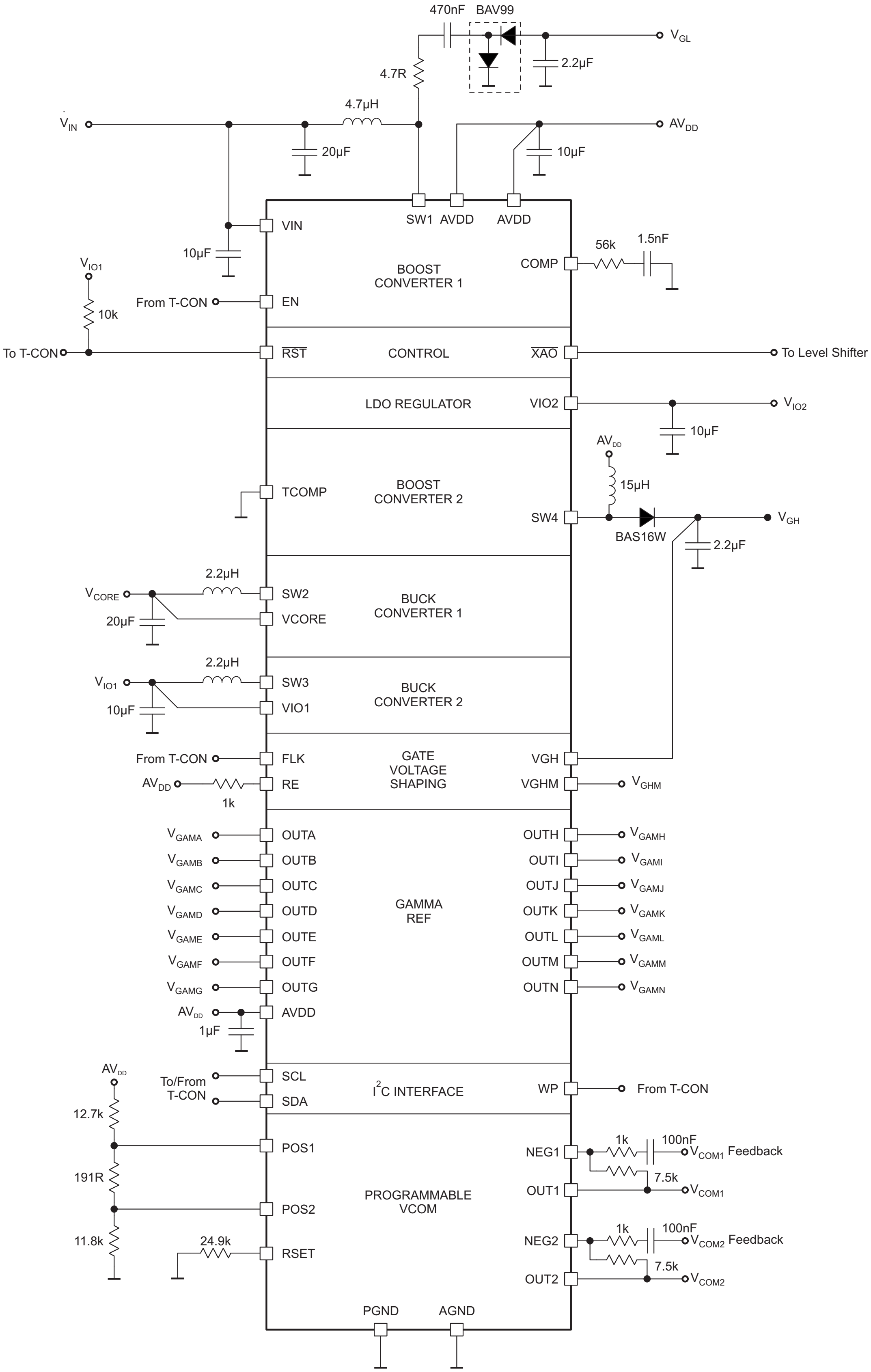


Figure 6-1. Typical Application Circuit for Non-GIP Displays

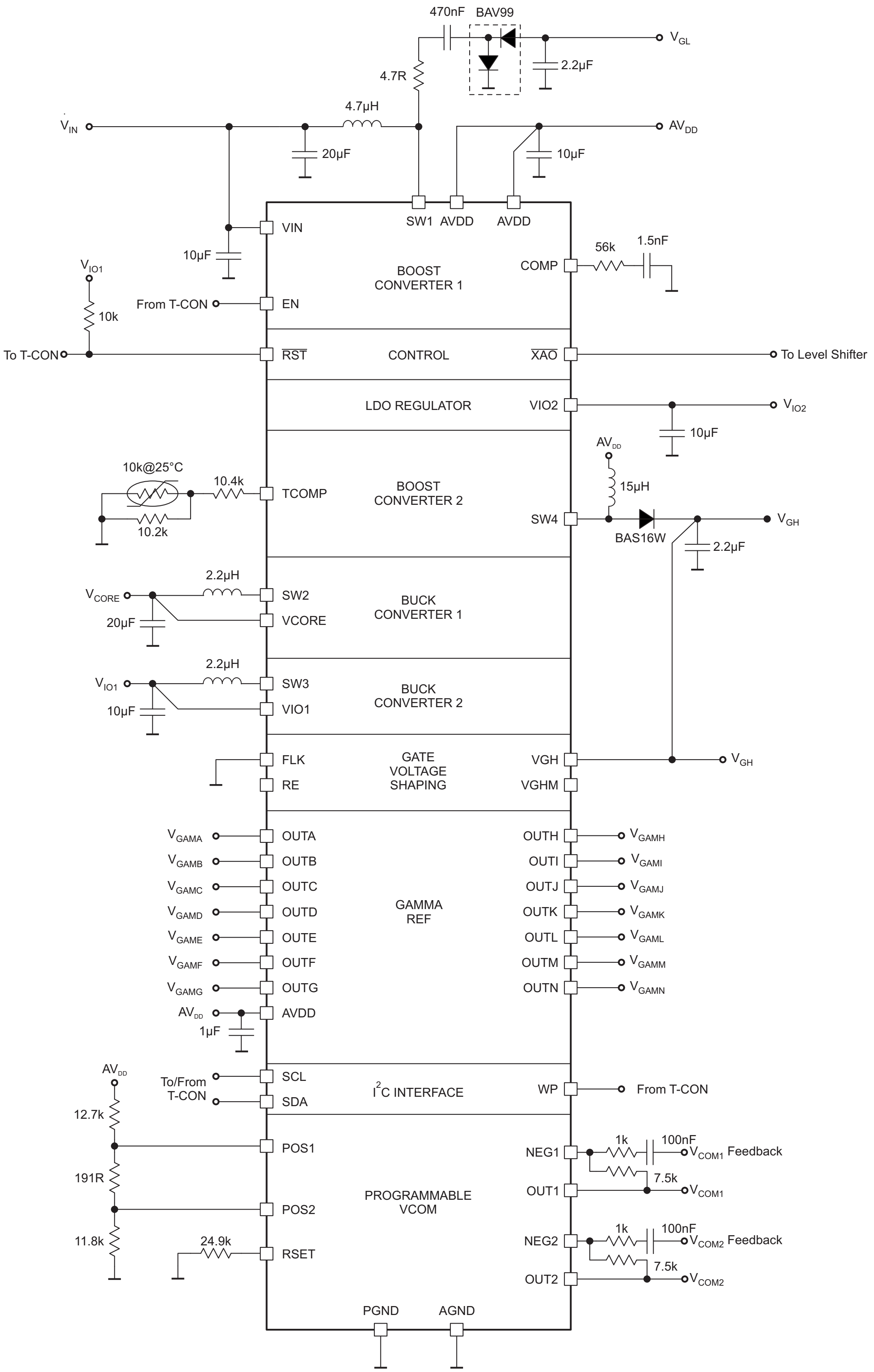


Figure 6-2. Typical Application Circuit for GIP Displays

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65642YFFR	ACTIVE	DSBGA	YFF	56	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS65642	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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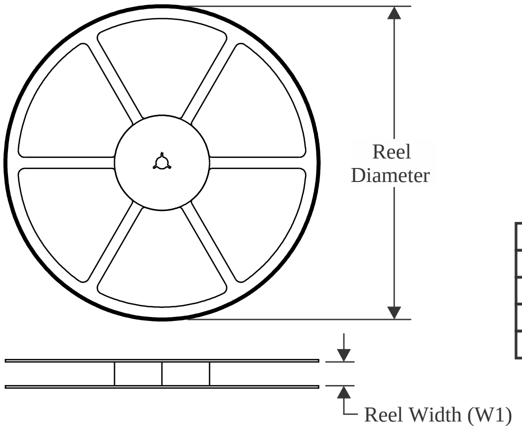
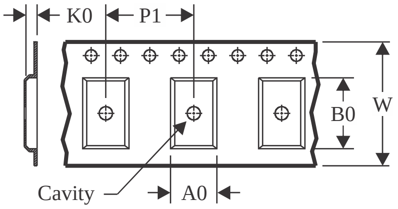
TAPE AND REEL INFORMATION

REEL DIMENSIONS

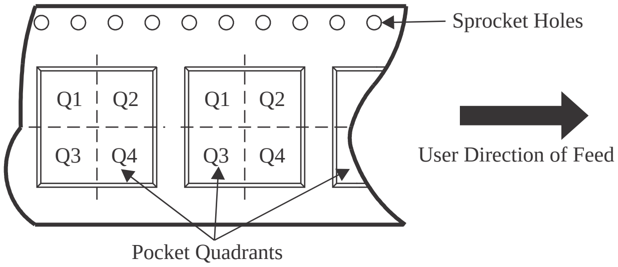


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

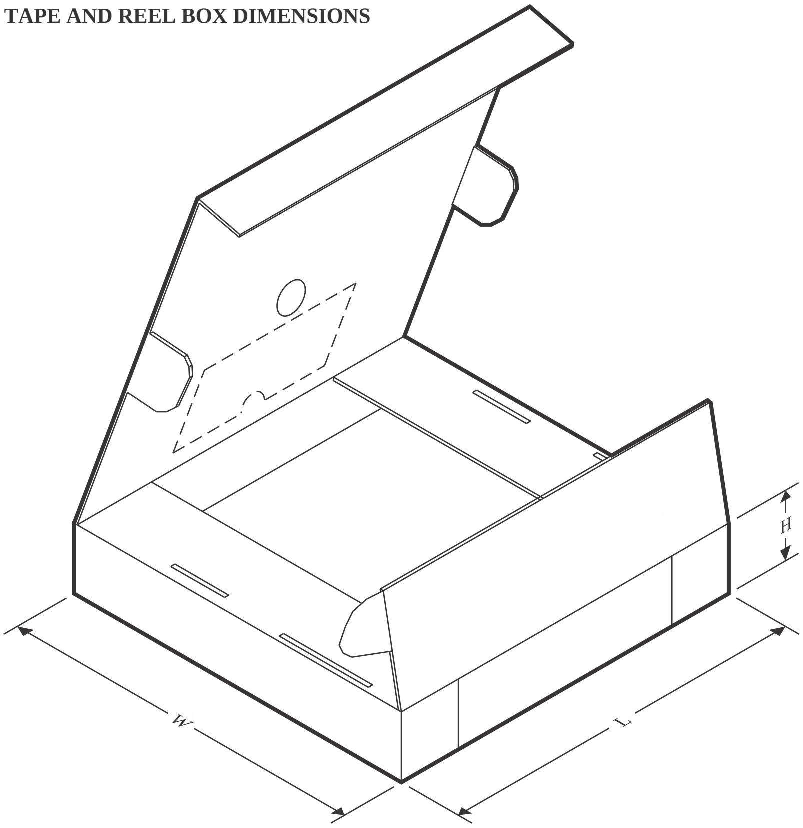
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

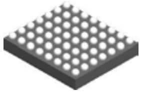
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65642YFFR	DSBGA	YFF	56	3000	330.0	12.4	3.0	3.55	0.81	8.0	12.0	Q1

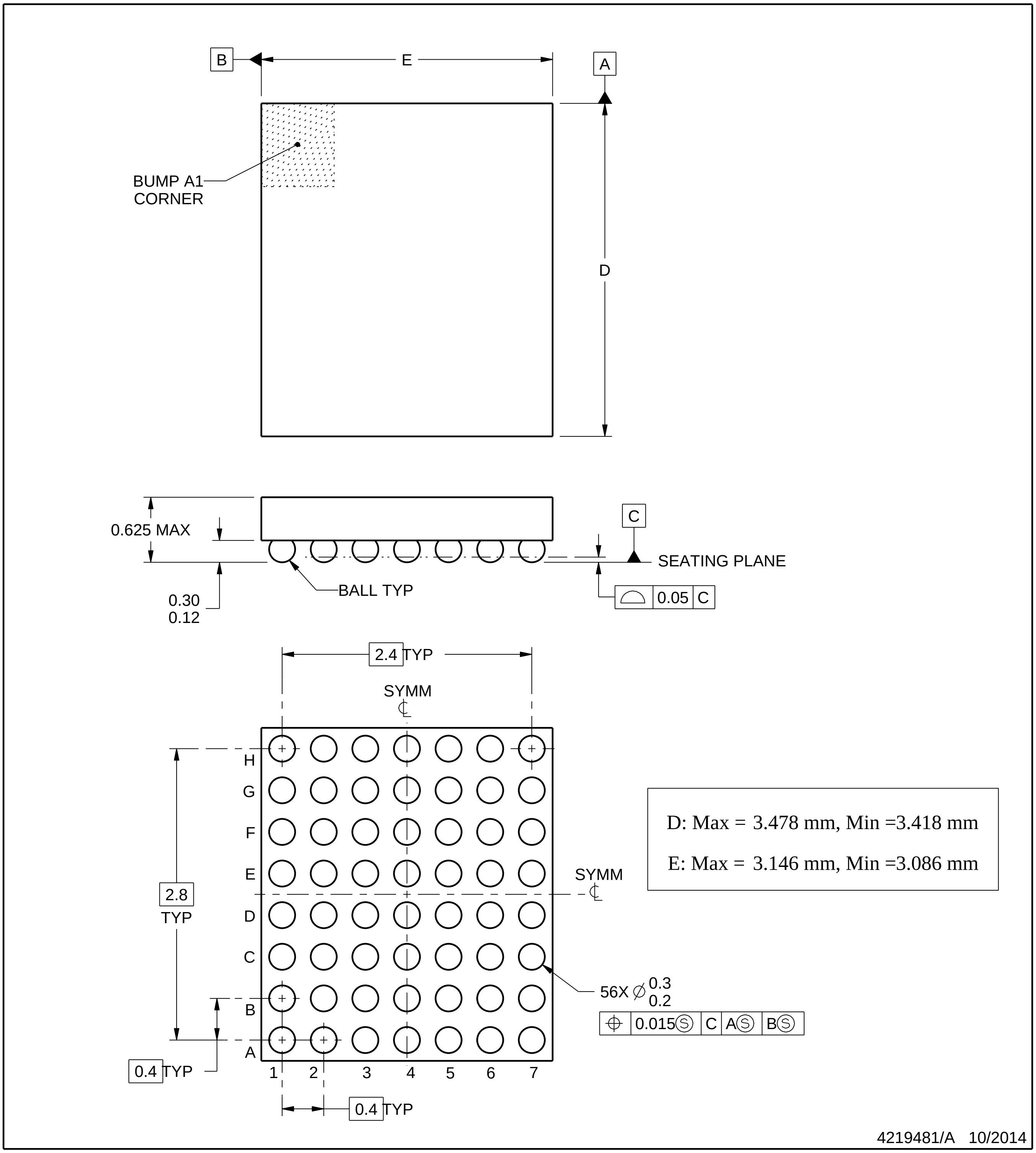
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65642YFFR	DSBGA	YFF	56	3000	335.0	335.0	25.0





D: Max = 3.478 mm, Min =3.418 mm

E: Max = 3.146 mm, Min =3.086 mm

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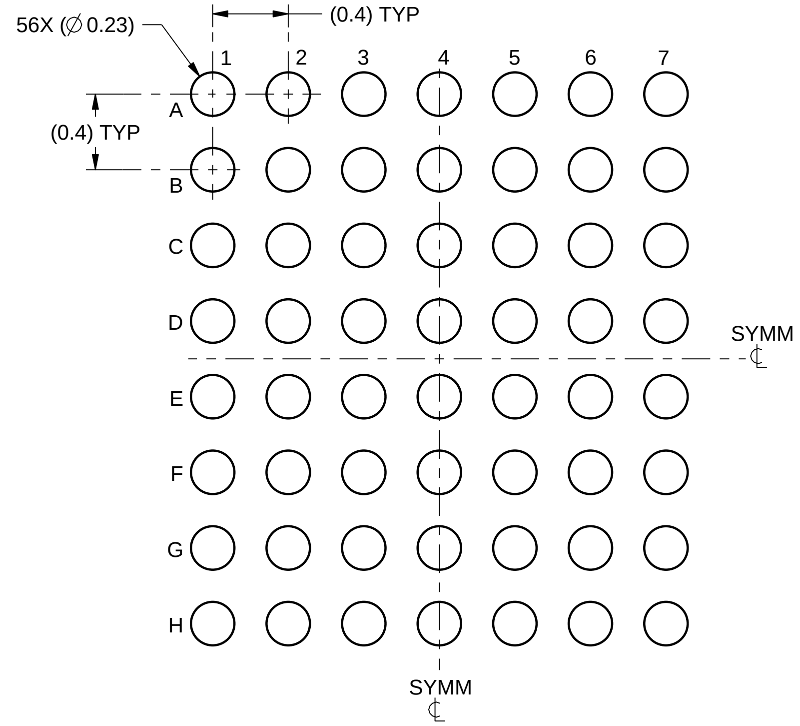
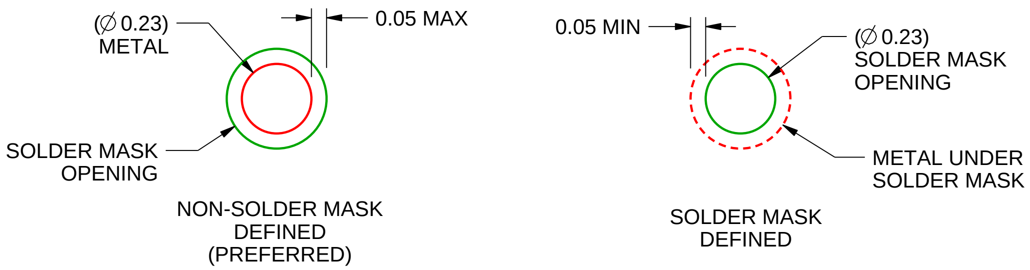
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



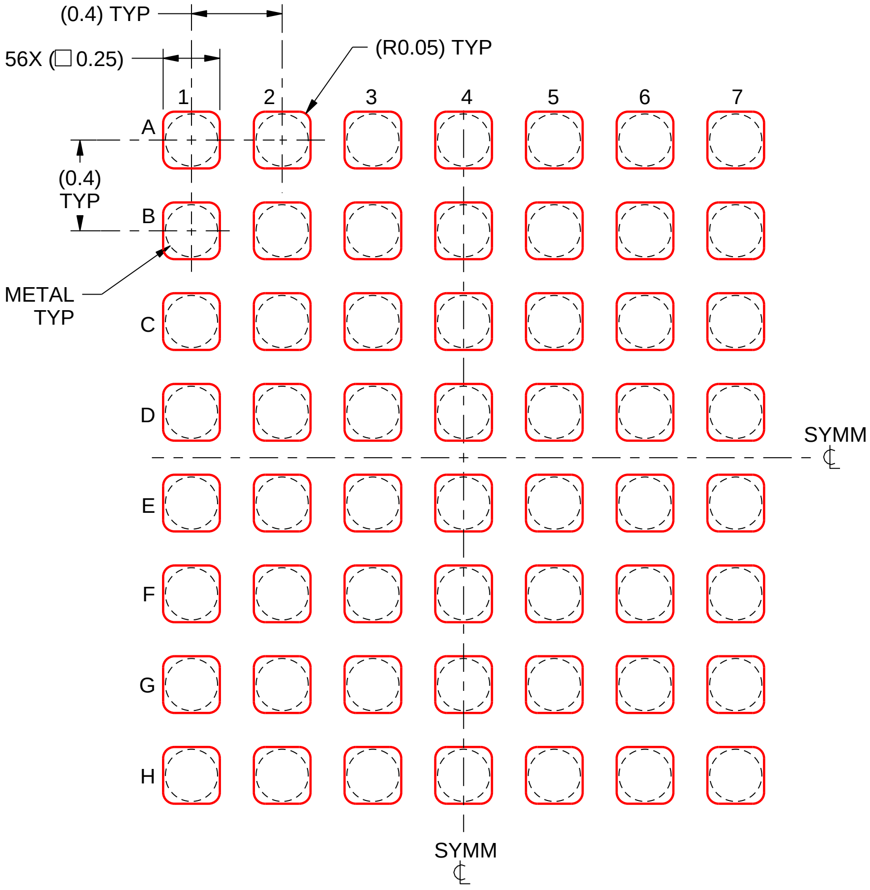
LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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