TEXAS INSTRUMENTS
TPS65994AE
SLVSG37 – JUNE 2021

TPS65994AE Dual Port USB Type-C® and USB PD Controller with Integrated Source Power Switches

1 Features

- USB Power Delivery (PD) controller
  - USB PD 3.0 compliant
  - Fast role swap support
  - Physical layer and policy engine
  - Configurable at Boot and host-controlled
- USB Type-C specification compliant
  - Cable attach and orientation detection
  - Default, 1.5-A or 3-A power advertisement
  - Integrated VCONN switch
- Integrated VBUS sourcing port power switch
  - Two 5-V, 3-A, 29-mΩ sourcing switches
  - Adjustable current limiting
  - Undervoltage and overvoltage protection
  - Fast turn-on mode to support fast-role swap
- UL recognized component (E169910)
- High-voltage gate drivers for two sinking paths
  - Reverse current protection
  - Slew rate control
  - Overvoltage protection
- Alternate mode support
  - DisplayPort source
  - Thunderbolt™
- USB type-C connector system software interface (USCI) support
- Power management
  - Power supply from 3.3 V or VBUS source
  - 3.3-V LDO output for dead battery support
- QFN package (0.4-mm pitch)

2 Applications

- Notebook PCs
- Desktop computers
- Docking Station DFP port
- Monitor
- Industrial PC

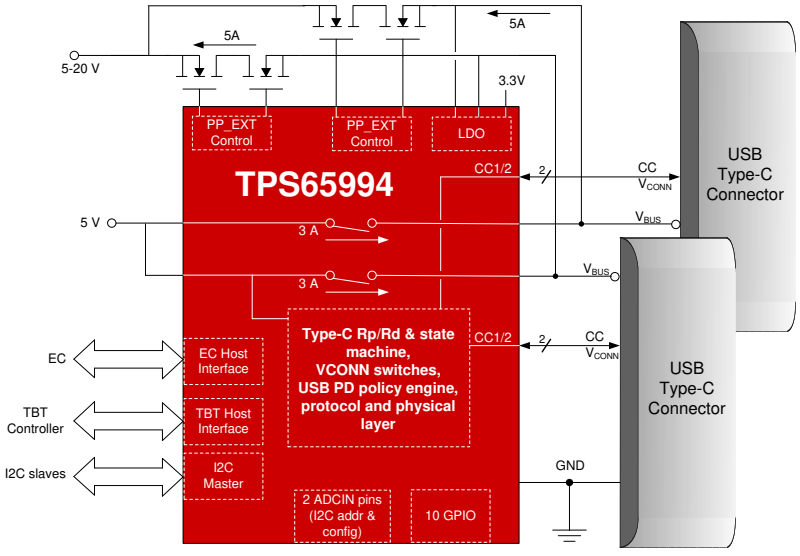
3 Description

The TPS65994AE is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C connectors. Upon cable attachment, the TPS65994AE performs cable detection according to the USB Type-C specification. It also communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65994AE enables the appropriate power path and configures alternate mode settings for external multiplexers.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS65994AE	QFN (RSL)	6.0 mm x 6.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

DATE	REVISION	NOTES
June 2021	*	Initial Release

5 Pin Configuration and Functions

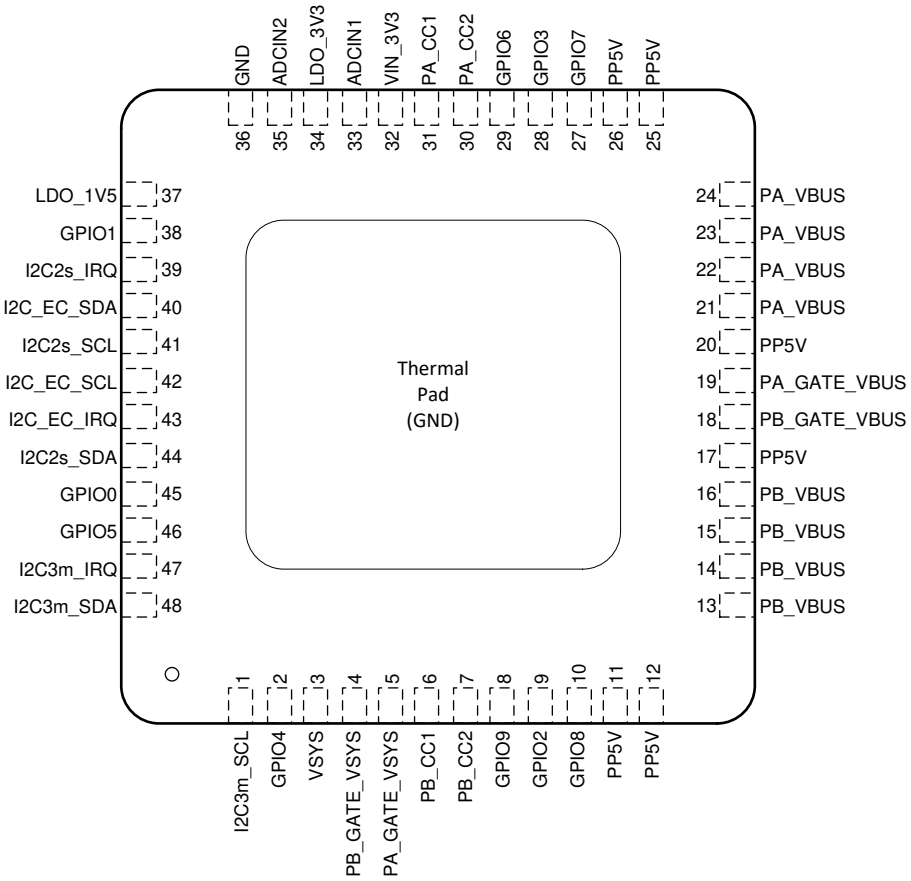


Figure 5-1. RSL Package 48-pin QFN Top View

Table 5-1. Pin Functions

PIN		TYPE	RESET	Description
NAME	NO.			
ADCIN1	33	I	Hi-Z	Configuration input. Connect to a resistor divider to LDO_3V3.
ADCIN2	35	I	Hi-Z	Configuration input. Connect to a resistor divider to LDO_3V3.
GND	36	—	—	Ground. Connect to ground plane.
GPIO0	45	I/O	Hi-Z	General purpose digital I/O. Tie to PP5V or ground when unused. May be used as DisplayPort HPD signal for Port B.
GPIO1	38	I/O	Hi-Z	General purpose digital I/O. Tie to PP5V or ground when unused. May be used as DisplayPort HPD signal for Port A.
GPIO2	9	I/O	Hi-Z	General purpose digital I/O. Tie to PP5V or ground when unused.
GPIO3	28	I/O	Hi-Z	General purpose digital I/O. Tie to PP5V or ground when unused.
GPIO4	2	I/O	Hi-Z	General purpose digital I/O. May be used as an ADC input. Tie to PP5V or ground when unused.
GPIO5	46	I/O	Hi-Z	General purpose digital I/O. May be used as an ADC input. Tie to PP5V or ground when unused.
GPIO6	29	I/O	Hi-Z	General purpose digital I/O. Tie to PP5V or ground when unused.
GPIO7	27	I/O	Hi-Z	General purpose digital I/O. Tie to PP5V or ground when unused.
GPIO8	10	I/O	Hi-Z	General purpose digital I/O. Tie to PP5V or ground when unused.

Table 5-1. Pin Functions (continued)

PIN		TYPE	RESET	Description
NAME	NO.			
GPIO9	8	O	Hi-Z	General purpose digital output. Tie to PP5V or ground when unused.
I2C_EC_SCL	42	I	Hi-Z	I2C slave serial clock input. Tie to pullup voltage through a resistor. May be grounded if unused. Connect to Embedded Controller (EC).
I2C_EC_SDA	40	I/O	Hi-Z	I2C slave serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused. Connect to Embedded Controller (EC).
$\overline{\text{I2C\_EC\_IRQ}}$	43	O	Hi-Z	I2C slave interrupt. Active low. Connect to external voltage through a pull-up resistor. Connect to Embedded Controller (EC). This can be re-configured to GPIO10. May be grounded if unused.
I2C2s_SCL	41	I	Hi-Z	I2C slave serial clock input. Tie to pull-up voltage through a resistor. May be grounded if unused.
I2C2s_SDA	44	I/O	Hi-Z	I2C slave serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused.
$\overline{\text{I2C2s\_IRQ}}$	39	O	Hi-Z	I2C slave interrupt. Active low. Connect to external voltage through a pull-up resistor. Tie to PP5V or ground when unused. This can be re-configured to GPIO11.
I2C3m_SCL	1	O	Hi-Z	I2C master serial clock. Open-drain output. Tie to pullup voltage through a resistor when used or unused.
I2C3m_SDA	48	I/O	Hi-Z	I2C master serial data. Open-drain input/output. Tie to pullup voltage through a resistor when used or unused.
$\overline{\text{I2C3m\_IRQ}}$	47	I	Hi-Z	I2C master interrupt. Active low. Connect to external voltage through a pull-up resistor. Tie to PP5V or ground when unused. This can be re-configured to GPIO12.
LDO_1V5	37	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	34	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
PA_CC1	31	I/O	Hi-Z	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{Px_CCy}).
PA_CC2	30	I/O	Hi-Z	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{Px_CCy}).
PA_GATE_VSYS	5	O	Hi-Z	Connect to the PortA N-ch MOSFET that has source tied to VSYS.
PA_GATE_VBUS	19	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to PA_VBUS.
PA_VBUS	21,22,23,24	I/O	—	5-V to 20-V input or 5-V output from PP5V. Bypass with capacitance C_{VBUS} to GND.
PB_CC1	6	I/O	Hi-Z	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{Px_CCy}).
PB_CC2	7	I/O	Hi-Z	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{Px_CCy}).
PB_GATE_VSYS	4	O	Hi-Z	Connect to the Port B N-ch MOSFET that has source tied to VSYS.
PB_GATE_VBUS	18	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to PB_VBUS.
PB_VBUS	13,14,15,16	I/O	—	5-V to 20-V input or 5-V output from PP5V. Bypass with capacitance C_{VBUS} to GND.
PP5V	11,12,17,20,25, 26	I	—	5-V System Supply to VBUS, supply for Px_CCy pins as VCONN.
VSYS	3	I	—	High-voltage sinking node in the system. It is used to implement reverse-current-protection (RCP) for the external sinking paths controlled by PA_GATE_VSYS and PB_GATE_VSYS.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance C_{VIN_3V3} to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range (2)	PP5V	–0.3	6	V
	VIN_3V3	–0.3	4	
	ADCIN1, ADCIN2	–0.3	4	
	VSYS, PA_VBUS, PB_VBUS (4)	–0.3	28	V
	PA_CC1, PA_CC2, PB_CC1, PB_CC2	–0.5	6	
	GPIO0-GPIO9, $\overline{\text{I2C_EC_IRQ}}$, $\overline{\text{I2C2s_IRQ}}$, $\overline{\text{I2C3m_IRQ}}$,	-0.3	6	
	I2C_EC_SDA, I2C_EC_SCL,I2C2s_SDA, I2C2s_SCL, I2C3m_SDA, I2C3m_SCL	–0.3	4	
Output voltage range (2)	LDO_1V5(3)	–0.3	2	V
	LDO_3V3(3)	–0.3	4	
Output voltage range (2)	PA_GATE_VBUS, PA_GATE_VSYS, PB_GATE_VBUS, PB_GATE_VSYS (3)	–0.3	40	V
V_{GS}	$V_{Px\_GATE\_VBUS}$ - V_{Px_VBUS}, $V_{Px\_GATE\_SYS}$ - V_{VSYS}	–0.5	12	V
Source current	Source or sink current PA_VBUS, PB_VBUS		internally limited	A
	Positive source current on PA_CC1, PA_CC2, PB_CC1, PB_CC2		1	
	Positive sink current on PA_CC1, PA_CC2, PB_CC1, PB_CC2 while VCONN switch is enabled		1	
	GPIO0-GPIO9		0.005	
	positive sink current for I2C_EC_SDA, I2C_EC_SCL, I2C2s_SDA, I2C2s_SCL, I2C3m_SDA, I2C3m_SCL,		internally limited	
	positive source current for LDO_3V3, LDO_1V5		internally limited	
T_J Operating junction temperature		–40	175	°C
T_{STG} Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(3) Do not apply voltage to these pins.
(4) For Px_VBUS a TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200. For Px_VBUS a Schottky diode is recommended to ensure the MIN voltage is not violated.

6.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage range (1)	VIN_3V3	3.0	3.6	V
		PP5V (2)	4.9	5.5	
		PA_VBUS, PB_VBUS (3)	4	22	
V_I	Input voltage range (1)	VSYS	0	22	V
V_{IO}	I/O voltage range (1)	I2Cx_SDA, I2Cx_SCL, ADCIN1, ADCIN2	0	3.6	V
		GPIOx, $\overline{\text{I2C_EC_IRQ}}$, $\overline{\text{I2C2s_IRQ}}$, $\overline{\text{I2C3m_IRQ}}$,	0	5.5	
		PA_CC1, PA_CC2, PB_CC1, PB_CC2	0	5.5	
I_O	Output current (from PP5V)	PA_VBUS, PB_VBUS		3	A
		PA_CC1, PA_CC2, PB_CC1, PB_CC2		315	mA
I_O	Output current (from LDO_3V3)	GPIOx		1	mA
I_O	Output current (from VBUS LDO)	sum of current from LDO_3V3 and GPIO0-9.		5	mA
T_A	Ambient operating temperature	$I_{PP\_5Vx} \le 1.5$ A, $I_{PP\_5Vy} \le 3.0$ A, $I_{PP\_CABLEx} \le 315$ mA	–40	105	°C
		$I_{PP\_5Vx} \le 3.0$ A, $I_{PP\_CABLEx} \le 315$ mA	–40	85	
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(2) Maximum current sourced from PP5V to PA_VBUS or PB_VBUS. Resistance from Px_VBUS to Type-C connector less than or equal 30 mΩ. Short all PP5V bumps together.
(3) All PA_VBUS bumps should be shorted together. All PB_VBUS bumps should be shorted together.

6.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{VIN_3V3}	Capacitance on VIN_3V3	6.3 V	5	10		µF
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3 V	5	10	25	µF
C_{LDO_1V5}	Capacitance on LDO_1V5	4 V	4.5		12	µF
C_{Px_VBUS}	Capacitance on VBUS(3)	25 V	1	4.7	10	µF
C_{PP5V}	Capacitance on PP5V	10 V	120			µF
C_{VSYS}	Capacitance on VSYS Sink from VBUS	25 V		47	100	µF
C_{Px_CCy}	Capacitance on Px_CCy pins(2)	6.3 V	200	320	480	pF

(1) Capacitance values do not include any derating factors. For example, if 5.0 µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 µF.
(2) This includes all capacitance to the Type-C receptacle.
(3) The device can be configured to quickly disable PP_EXT upon certain events. When such a configuration is used, a capacitance on the higher side of this range is recommended.

6.5 Thermal Information

THERMAL METRIC(1)		TPS65994AE QFN (RSL) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.8	°C/W

6.5 Thermal Information (continued)

THERMAL METRIC(1)		TPS65994AE QFN (RSL) 48 PINS	UNIT
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance	15.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.5	°C/W
$R_{\theta JC}$ (bottom)	Junction-to-case (bottom GND pad) thermal resistance	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_3V3, Px_VBUS						
V_{VIN3V3_UVLO}	voltage required on VIN_3V3 for power on	rising, V_{Px_VBUS}=0	2.56	2.66	2.76	V
		falling, V_{Px_VBUS}=0	2.44	2.54	2.64	
		hysteresis		0.12		
V_{VBUS_UVLO}	UVLO comparator for Px_VBUS	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		
LDO_3V3, LDO_1V5						
V_{LDO_3V3}	voltage on LDO_3V3	V_{VIN_3V3} = 0V, I_{LDO_3V3} ≤ 5 mA, V_{PA_VBUS} ≥ 3.9V or V_{PB_VBUS} ≥ 3.9V	2.7	3.4	3.6	V
R_{LDO_3V3}	Rdson of VIN_3V3 to LDO_3V3	I_{LDO_3V3}=50mA			1.5	Ω
V_LDO_1V5	Output voltage of LDO_1V5	up to maximum internal loading condition.		1.55		V

6.7 Power Consumption

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V, no loading on GPIO pins

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN\_3V3,ActSrc}$	current into VIN_3V3	Active Source mode: V_{PP5V}=5.0V, V_{VIN_3V3}=3.3V		4.5	12	mA
$I_{VIN\_3V3,ActSnk}$	current into VIN_3V3	Active Sink mode: 22V ≥ V_{PA_VBUS} ≥ 4.0V, 22V ≥ V_{PB_VBUS} ≥ 4.0V, V_{VIN_3V3}=3.3V		4.8	12	mA
I_{VSYS}	current into VSYS			10		µA
$I_{VIN\_3V3,IdlSrc}$	current into VIN_3V3	Idle Source mode: V_{PA_VBUS}=5.0V, V_{PB_VBUS}=5.0V, V_{VIN_3V3}=3.3V		1.1		mA
$I_{VIN\_3V3,IdlSnk}$	current into VIN_3V3	Idle Sink mode: 22V ≥ V_{PA_VBUS} ≥ 4.0V, 22V ≥ V_{PB_VBUS} ≥ 4.0V, V_{VIN_3V3}=3.3V		1.1		mA
$P_{MstbySnk}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Sink Mode	Modern Standby Sink Mode: V_{PP5V} = 5V, V_{VIN_3V3}=3.3V, V_{PA_VBUS}=5.0V, V_{PB_VBUS}=0V		3.7		mW
$P_{MstbySrc}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Source Mode	Modern Standby Source Mode: V_{PP5V} = 5V, V_{VIN_3V3}=3.3V, I_{Px_VBUS}=0		4.5		mW
$I_{VIN\_3V3,Sleep}$	current into VIN_3V3	Sleep mode: V_{PA_VBUS}=0V, V_{PB_VBUS}=0V, V_{VIN_3V3}=3.3V, T_J ≤ 25ºC		67		µA

6.8 PP_5V Power Switch Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_5V}	Resistance from PP5V to Px_VBUS	I_{LOAD} = 3 A, T_J≤25ºC		36	40	mΩ
		I_{LOAD} = 3 A, T_J≤125ºC		36	52	
I_{PP5V_REV}	Px_VBUS to PP5V leakage current	V_{PP5V} = 0V, V_{Px_VBUS} = 5.5V, PP_5V disabled, T_J≤85ºC, measure I_{PP5V}		0	3	µA
I_{PP5V_FWD}	PP5V to Px_VBUS leakage current	V_{PP5V} = 5.5V, V_{Px_VBUS} = 0V, PP_5V disabled, T_J≤85ºC, measure I_{Px_VBUS}		0	15	µA
I_{LIM5V}	Current limit setting	Configure to setting 0	1.15		1.36	A
I_{LIM5V}	Current limit setting	configure to setting 1	1.61		1.90	A
I_{LIM5V}	Current limit setting	configure to setting 2	2.3		2.70	A
I_{LIM5V}	Current limit setting	configure to setting 3	3.04		3.58	A
I_{LIM5V}	Current limit setting	configure to setting 4	3.22		3.78	A
$V_{PP\_5V\_RCP}$	RCP clears and PP_5Vx starts turning on when V_{Px_VBUS} – V_{PP5V} < $V_{PP\_5V\_RCP}$. Measure V_{Px_VBUS} – V_{PP5V}		10	15	20	mV
$t_{iOS\_PP\_5V}$	response time to VBUS short circuit	Px_VBUS to GND through 10mΩ, C_{Px_VBUS}=0		1.15		µs
$t_{PP\_5V\_ovp}$	response time to V_{Px_VBUS} > $V_{OVP4RCP}$	Enable PP_5Vx, ramp V_{Px_VBUS} from 4V to 20V at 100 V/ms		4.5		µs
$t_{PP\_5V\_uvlo}$	response time to V_{PP5V} < V_{PP5V_UVLO}, PP_VBUS is deemed off when V_{Px_VBUS} < 0.8V	R_L = 100 Ω, no external capacitance on Px_VBUS		4		µs
$t_{PP\_5V\_rcp}$	response time to V_{PP5V} < V_{Px_VBUS}+$V_{PP\_5V\_RCP}$	V_{PP5V}=5.5V, enable PP_5Vx, ramp V_{Px_VBUS} from 4V to 21.5V at 10 V/µs		0.7		µs
t_{FRS_on}	Time allowed to enable the pass FET in PP_5Vx with 3A current limit.	Initial V_{Px_VBUS} = 0V, 2µF ≤ C_{Px_VBUS} ≤ 20µF, 0 ≤ I_{Px_VBUS} ≤ 0.5 A, FET is deemed enabled when V_{Px_VBUS} > 4.75V.		54	150	µs
t_{ILIM}	Current clamping deglitch time			5		ms
t_{ON}	from enable signal to Px_VBUS at 90% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	2.6	3.5	4.4	ms
t_{OFF}	from disable signal to Px_VBUS at 10% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	0.30	0.45	0.6	ms
t_{RISE}	Px_VBUS from 10% to 90% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	1.2	1.7	2.2	ms
t_{FALL}	Px_VBUS from 90% to 10% of initial value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	0.06	0.1	0.14	ms

6.9 PP_EXT Power Switch Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Px\_GATE\_ON}$	Gate driver sourcing current	0 ≤ $V_{Px\_GATE\_VSYS}$-V_{VSYS} ≤ 6 V, 0 V ≤ V_{VSYS} ≤ 22 V, V_{Px_VBUS} > 4 V, measure $I_{Px\_GATE\_VSYS}$	8.5	10	11.5	µA
		0 ≤ $V_{Px\_GATE\_VBUS}$-V_{Px_VBUS} ≤ 6 V, 4 V ≤ V_{Px_VBUS} ≤ 22 V, measure $I_{Px\_GATE\_VBUS}$	8.5	10	11.5	µA
V_{GATE_ON}	sourcing voltage (ON)	0 ≤ V_{VSYS} ≤ 22 V, $I_{Px\_GATE\_VSYS}$ < 4 µA, measure $V_{Px\_GATE\_VSYS}$ – V_{VSYS}, V_{Px_VBUS} > 4 V.	6		12	V
		4 V ≤ V_{Px_VBUS} ≤ 22 V, $I_{Px\_GATE\_VBUS}$ < 4 µA, measure $V_{Px\_GATE\_VBUS}$ – V_{Px_VBUS}.	6		12	V
V_{RCP}	comparator mode RCP threshold, V_{VSYS} - V_{Px_VBUS}.	setting 0, 4 V ≤ V_{Px_VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	2	6	10	mV
		setting 1, 4 V ≤ V_{Px_VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	4	8	12	mV
		setting 2, 4 V ≤ V_{Px_VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	6	10	14	mV
		setting 3, 4 V ≤ V_{Px_VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	8	12	16	mV
$I_{Px\_GATE\_OFF}$	Sinking strength	normal turnoff: V_{VSYS} = 5V, $V_{Px\_GATE\_VSYS}$=6V	13			µA
		normal turnoff: V_{Px_VBUS} = 5V, $V_{Px\_GATE\_VBUS}$=6V, V_{VSYS} = 5 V	13			µA
$R_{Px\_GATE\_FSD}$	Sinking strength	fast turnoff: V_{VSYS} = 5V, $V_{Px\_GATE\_VSYS}$=6V,			85	Ω
		fast turnoff: V_{Px_VBUS} = 5V, $V_{Px\_GATE\_VBUS}$=6V, V_{VSYS} = 5 V			85	Ω
$R_{Px\_GATE\_OFF\_UVLO}$	Sinking strength in UVLO (safety)	V_{VIN_3V3}=0V, V_{Px_VBUS}=3.0V, $V_{Px\_GATE\_VSYS}$=0.1V			1.5	MΩ
$t_{Px\_GATE\_VBUS\_OFF}$	Time allowed to disable the external FET via Px_GATE_VBUS in normal shutdown mode.(1)	V_{Px_VBUS}=20V, Gate is off when V_{GS} < 1 V		260		µs
$t_{Px\_GATE\_VBUS\_OVP}$	Time allowed to disable the external FET via Px_GATE_VBUS in fast shutdown mode ($V_{OVP4RCP}$ exceeded).(1)	OVP: $V_{OVP4RCP}$= setting 57, V_{Px_VBUS}=20V initially, then raised to 23V in 50ns, Gate is off when V_{GS} < 1 V		3		µs
$t_{Px\_GATE\_VBUS\_RCP}$	Time allowed to disable the external FET via Px_GATE_VBUS in fast shutdown mode (V_{RCP} exceeded).(1)	RCP: V_{RCP}= setting 0, V_{Px_VBUS}=5V, V_{VSYS}=5V initially, then raised to 5.5V in 50ns, Gate is off when V_{GS} < 1 V		1.2		µs
$t_{Px\_GATE\_VSYS\_OFF}$	Time allowed to disable the external FET via Px_GATE_VSYS in normal shutdown mode(1)	V_{VSYS}=20V, Gate is off when V_{GS} < 1 V		0.25		ms

6.9 PP_EXT Power Switch Characteristics (continued)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{Px\_GATE\_VSYS\_FSD}$	Time allowed to disable the external FET via Px_GATE_VSYS in fast shutdown mode (OVP or FRS)(1)	V_{VSYS}=V_{VBUS}=20V initially, then V_{VBUS} raised to 23V in 50ns, Gate is off when V_{GS}< 1 V		0.25		µs
$t_{Px\_GATE\_VBUS\_ON}$	time to enable Px_GATE_VBUS (1)	measure time from when V_{GS}=0V until V_{GS}>3V		0.25		ms

(1) These values depend upon the characteristics of the external N-ch MOSFET. The typical values were measured when Px_GATE_VSYS and Px_GATE_VBUS were used to drive two CSD17571Q2 in common drain back-to-back configuration.

6.10 Power Path Supervisory

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OVP4RCP}$	VBUS over voltage protection typical threshold for RCP programmable range (setting 0 to setting 63).	OVP detected when V_{Px_VBUS} > $V_{OVP4RCP}$	5.25		22.9	V
	Tolernance of $V_{OVP4RCP}$ threshold		-5		5	%
V_{OVPLSB}	VBUS over voltage protection range for RCP			280		mV
$V_{OVP4RCPH}$	hysteresis		1.75	2	2.25	%
r_{OVP}	ratio of OVP4RCP input used for OVP4VSYS comparator. r_{OVP}*$V_{OVP4VSYS}$ = $V_{OVP4RCP}$	setting 0	1	1	1	V/V
		setting 1	0.925	0.95	0.975	V/V
		setting 2	0.875	0.90	0.925	V/V
		setting 3	0.85	0.875	0.9	V/V
$V_{OVP4VSYS}$	VBUS over voltage protection range for VSYS protection	OVP detected when r_{OVP}*V_{Px_VBUS} > $V_{OVP4RCP}$	5		27.5	V
$V_{OVP4VSYS}$	hysteresis	VBUS falling, % of $V_{OVP4VSYS}$		2		%
V_{PP5V_UVLO}	Voltage required on PP5V	rising	3.9	4.1	4.3	V
		falling	3.8	4.0	4.2	
		hysteresis		0.1		
I_{DSCH}	VBUS discharge current (1)	V_{Px_VBUS} = 22V, measure I_{Px_VBUS}	4		13	mA

(1) The discharge is enabled automatically when needed to meet USB specifications. It is not always enabled.

6.11 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Source (Rp pull-up)						
$V_{OC\_3.3}$	Unattached Px_CCy open circuit voltage while Rp enabled, no load	$V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, R_{CC} = 47 kΩ	1.85			V
V_{OC_5}	Attached Px_CCy open circuit voltage while Rp enabled, no load	V_{PP5V_UVLO} < V_{PP5V} < 5.5 V, R_{CC} = 47 kΩ	2.95			V
I_{Rev}	Unattached reverse current on Px_CCy	V_{Px_CCy} = 5.5V, V_{Px_CCx} = 0V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 3.8 V , measure current into Px_CCy			10	µA
		V_{Px_CCy} = 5.5V, V_{Px_CCx} = 0V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 0, -10°C≤T_J≤85°C, measure current into Px_CCy			10	

6.11 CC Cable Detection Parameters (continued)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RpDef}	current source - USB Default	0 < V_{Px_CCy} < 1.0 V, measure I_{Px_CCy}	64	80	96	µA
$I_{Rp1.5}$	current source - 1.5A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{Px_CCy} < 1.5 V, measure I_{Px_CCy}	166	180	194	µA
$I_{Rp3.0}$	current source - 3.0A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{Px_CCy} < 2.45 V, measure I_{Px_CCy}	304	330	356	µA
Type-C Sink (Rd pull-down)						
V_{SNK1}	Open/Default detection threshold when Rd applied to Px_CCy	rising	0.2		0.24	V
	Open/Default detection threshold when Rd applied to Px_CCy	falling	0.16		0.20	V
	hysteresis			0.04		V
V_{SNK2}	Default/1.5A detection threshold	falling	0.62		0.68	V
	Default/1.5A detection threshold	rising	0.63	0.66	0.69	V
	hysteresis			0.01		V
V_{SNK3}	1.5A/3.0A detection threshold when Rd applied to Px_CCy	falling	1.17		1.25	V
	1.5A/3.0A detection threshold when Rd applied to Px_CCy	rising	1.22		1.3	V
	hysteresis			0.05		V
R_{SNK}	Rd pulldown resistance	0.25 V ≤ V_{Px_CCy} ≤ 2.1 V, measure resistance on Px_CCy	4.1		6.1	kΩ
R_{VCONN_DIS}	VCONN discharge resistance	0V ≤ V_{Px_CCy} ≤ 5.5 V, measure resistance on Px_CCy	4.1		6.1	kΩ
V_{CLAMP}	Dead battery Rd clamp	V_{VIN_3V3}=0V, 64 µA < I_{Px_CCy}<96 µA	0.25		1.32	V
		V_{VIN_3V3}=0V, 166 µA < I_{Px_CCy}<194 µA	0.65		1.32	
		V_{VIN_3V3}=0V, 304 µA < I_{Px_CCy}< 356 µA	1.20		2.18	
R_{Open}	resistance from Px_CCy to GND when configured as open.	V_{Px_VBUS} = 0, V_{VIN_3V3}=3.3V, V_{Px_CCy}=5 V, measure resistance on Px_CCy	500			kΩ
		V_{Px_VBUS} = 5V, V_{VIN_3V3} = 0, V_{Px_CCy}=5 V, measure resistance on Px_CCy	500			kΩ
V_{FRS}	Fast Role swap request voltage detection threshold on Px_CCy (falling)		495	515	535	mV
V_{FRS}	hysteresis			0.01		V
t_{FRS_DET}	Fast role swap signal detection time	V_{Px_CCy} must be below V_{FRS} for at least this long before the FRS signal is detected	30		35	µs
t_{FRS_Resp}	response time of the Fast role swap comparator (rising)	V_{Px_CCy} rises from 0.24V to 0.64V			0.6	µs
Common (Source and Sink)						
t_{CC}	deglitch time for comparators on Px_CCy			3.2		ms

6.12 CC VCONN Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_CABLE}	Rdson of the VCONN path	V_{PP5V}=5V, I_L = 250 mA, measure resistance from PP5V to Px_CCy		0.4	0.7	Ω
I_{LIMVC}	short circuit current limit	setting 0, V_{PP5V}=5V, R_L=10mΩ , measure I_{Px_CCy}	350	410	470	mA
I_{LIMVC}	short circuit current limit	setting 1, V_{PP5V}=5V, R_L=10mΩ , measure I_{Px_CCy}	540	605	670	mA
$I_{CC2PP5V}$	Reverse leakage current through VCONN FET	VCONN disabled, T_J ≤ 85ºC, V_{Px_CCy} = 5.5 V, V_{PP5V}=0 V, V_{Px_VBUS}=5V, LDO forced to draw from VBUS, measure I_{Px_CCy}		0	10	µA
t_{VCILIM}	Current clamp deglitch time			1.28		ms
$t_{PP\_CABLE\_off}$	from disable signal to Px_CCy at 10% of final value	I_L = 250 mA, V_{PP5V} = 5V, C_L=0	100	171	300	µs
$t_{iOS\_PP\_CABLE}$	response time to short circuit	V_{PP5V}=5V, for short circuit R_L = 10mΩ.		2		µs

6.13 CC PHY Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V or V_{Px_VBUS} ≥ 3.9 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V_{TXHI}	Transmit high voltage on Px_CCy	Standard External load	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage on Px_CCy	Standard External load	-75		75	mV
Z_{DRIVER}	Transmit output impedance while driving the CC line using Px_CCy	measured at 750 kHz	33		75	Ω
t_{Rise}	Rise time. 10 % to 90 % amplitude points on Px_CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{Px_CCy}= 520 pF	300			ns
t_{Fall}	Fall time. 90 % to 10 % amplitude points on Px_CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{Px_CCy}= 520 pF	300			ns
Receiver						
Z_{BMCRX}	receiver input impedance on Px_CCy	Does not include pull-up or pulldown resistance from cable detect. Transmitter is Hi-Z.	10			MΩ
C_{CC}	Receiver capacitance on Px_CCy(1)	Capacitance looking into the CC pin when in receiver mode			120	pF
$V_{RX\_SNK\_R}$	Rising threshold on Px_CCy for receiver comparator	sink mode (rising)	499	525	551	mV
$V_{RX\_SRC\_R}$	Rising threshold on Px_CCy for receiver comparator	source mode (rising)	784	825	866	mV
$V_{RX\_SNK\_F}$	Falling threshold on Px_CCy for receiver comparator	sink mode (falling)	230	250	270	mV
$V_{RX\_SRC\_F}$	Falling threshold on Px_CCy for receiver comparator	source mode (falling)	523	550	578	mV

(1) C_{CC} includes only the internal capacitance on a Px_CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{Px_CCy} externally.

6.14 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		hysteresis		15		°C
T_{SD_PP5V}	Temperature controlled shutdown threshold. The power paths for each port sourcing from PP5V have local sensors that disables them when this temperature is exceeded.	Temperature rising	135	150	165	°C
		hysteresis		5		°C

6.15 ADC Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	least significant bit	3.6V max scaling, voltage divider of 3		14		mV
		25.2V max scaling, voltage divider of 21		98		mV
		4.07A max scaling		16.5		mA
GAIN_ERR	Gain error	0.05V ≤ V_{ADCINx} ≤ 3.6V, V_{ADCINx} ≤ V_{LDO_3V3}	–2.7		2.7	%
		0.05V ≤ V_{GPIOx} ≤ 3.6V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7V ≤ V_{LDO_3V3} ≤ 3.6V	–2.4		2.4	
		0.6V ≤ V_{Px_VBUS} ≤ 22V	–2.1		2.1	
VOS_ERR	Offset error(1)	0.05V ≤ V_{ADCINx} ≤ 3.6V, V_{ADCINx} ≤ V_{LDO_3V3}	–4.1		4.1	mV
		0.05V ≤ V_{GPIOx} ≤ 3.6V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7V ≤ V_{LDO_3V3} ≤ 3.6V	-4.1		4.1	
		0.6V ≤ V_{Px_VBUS} ≤ 22V	-4.1		4.1	

(1) The offset error is specified after the voltage divider.

6.16 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO0-8 (Inputs)						
GPIO_VIH	GPIOx high-Level input voltage	V_{LDO_3V3} = 3.3V	1.3			V
GPIO_VIL	GPIOx low-level input voltage	V_{LDO_3V3} = 3.3V			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	V_{LDO_3V3} = 3.3V	0.09			V
GPIO_ILKG	GPIOx leakage current	V_{GPIOx} = 3.45 V	–1		1	µA
GPIO_RPU	GPIOx internal pull-up	pull-up enabled	50	100	150	kΩ
GPIO_RPD	GPIOx internal pull-down	pull-down enabled	50	100	150	kΩ
GPIO_DG	GPIOx input deglitch			20		ns
GPIO0-9 (Outputs)						
GPIO_VOH	GPIOx output high voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx}= -2mA	2.9			V
GPIO_VOL	GPIOx output low voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx}=2mA			0.4	V
ADCIN1, ADCIN2						
ADCIN_ILKG	ADCINx leakage current	V_{ADCINx} ≤ V_{LDO_3V3}	–1		1	µA

6.16 Input/Output (I/O) Characteristics (continued)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BOOT}	time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

6.17 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{I2C\_EC\_IRQ}$, $\overline{I2C2s\_IRQ}$						
OD_VOL_IRQ	Low level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, V_{I2Cx_IRQ} = 3.45 V	–1		1	µA
I2C3m_IRQ						
IRQ_VIH	High-Level input voltage	V_{LDO_3V3} = 3.3V	1.3			V
IRQ_VIH_THRESH	High-Level input voltage threshold	V_{LDO_3V3} = 3.3V	0.72		1.3	V
IRQ_VIL	low-level input voltage	V_{LDO_3V3} = 3.3V			0.54	V
IRQ_VIL_THRESH	low-level input voltage threshold	V_{LDO_3V3} = 3.3V	0.54		1.08	V
IRQ_HYS	input hysteresis voltage	V_{LDO_3V3} = 3.3V	0.09			V
IRQ_DEG	input deglitch			20		ns
IRQ_ILKG	$\overline{I2C3m\_IRQ}$ leakage current	V_{I2C3m_IRQ} = 3.45 V	–1		1	µA
SDA and SCL Common Characteristics (Master, Slave)						
V_{IL}	Input low signal	V_{LDO_3V3}=3.3V,			0.54	V
V_{IH}	Input high signal	V_{LDO_3V3}=3.3V,	1.3			V
V_{HYS}	Input hysteresis	V_{LDO_3V3}=3.3V	0.165			V
V_{OL}	Output low voltage	I_{OL}=3 mA			0.36	V
I_{LEAK}	Input leakage current	Voltage on pin = V_{LDO_3V3}	–3		3	µA
I_{OL}	Max output low current	V_{OL}=0.4 V	15			mA
I_{OL}	Max output low current	V_{OL}=0.6 V	20			mA
t_f	Fall time from 0.7*V_{DD} to 0.3*V_{DD}	V_{DD} = 1.8V, 10 pF ≤ C_b ≤ 400 pF	12		80	ns
		V_{DD} = 3.3V, 10 pF ≤ C_b ≤ 400 pF	12		150	ns
t_{SP}	I2C pulse width surpressed				50	ns
C_I	pin capacitance (internal)				10	pF
C_b	Capacitive load for each bus line (external)				400	pF
$t_{HD;DAT}$	Serial data hold time	V_{DD} = 1.8V or 3.3V	0			ns
SDA and SCL Standard Mode Characteristics (Slave)						
f_{SCLS}	Clock frequency	V_{DD} = 1.8V or 3.3V			100	kHz
$t_{VD;DAT}$	Valid data time	Transmitting Data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Slave)						
f_{SCLS}	Clock frequency	V_{DD} = 1.8V or 3.3V	100		400	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.9	µs

6.17 I2C Requirements and Characteristics (continued)

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA and SCL Fast Mode Plus Characteristics (Slave)						
f_{SCLS}	Clock frequency (1)	V_{DD} = 1.8V or 3.3V, master controls SCL frequency such that: $t_{LOW} > t_{VD;ACK} + t_{SU;DAT}$, $T_J \le 65^oC$	400		1000	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid, $T_J \le 65^oC$			0.55	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low, $T_J \le 65^oC$			0.55	µs
SDA and SCL Fast Mode Characteristics (Master)						
f_{SCLM}	Clock frequency for master(3)	V_{DD} = 3.3V		390	410	kHz
$t_{HD;STA}$	Start or repeated start condition hold time	V_{DD} = 3.3V	0.6			µs
t_{LOW}	Clock low time	V_{DD} = 3.3V	1.3			µs
t_{HIGH}	Clock high time	V_{DD} = 3.3V	0.6			µs
$t_{SU;STA}$	Start or repeated start condition setup time	V_{DD} = 3.3V	0.6			µs
$t_{SU;DAT}$	Serial data setup time	Transmitting data, V_{DD} = 3.3V	100			ns
$t_{SU;STO}$	Stop condition setup time	V_{DD} = 3.3V	0.6			µs
t_{BUF}	Bus free time between stop and start	V_{DD} = 3.3V	1.3			µs
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 3.3V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 3.3V, ACK signal from SCL low to SDA (out) low			0.9	µs

(1) Fast Mode Plus is only recommended during boot when the device is in PTCH mode.
(2) The master or slave connected to the device follows I^2C specifications.
(3) Actual frequency is dependent upon bus capacitance.

6.18 Typical Characteristics

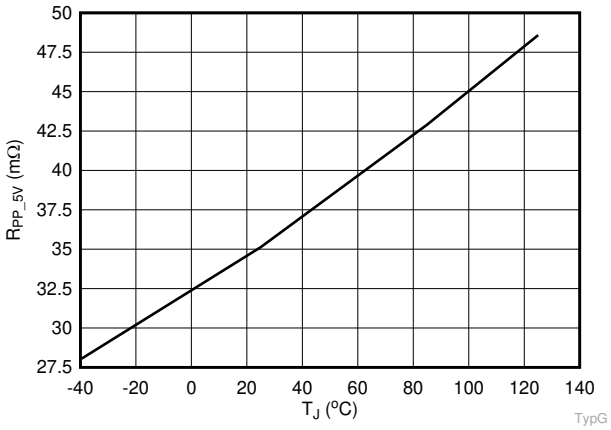


Figure 6-1. PP_5Vx Rdson vs. Temperature

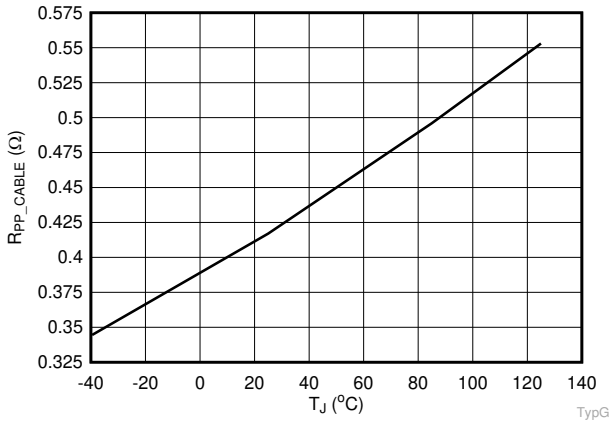


Figure 6-2. PP_CABLEx Rdson vs. Temperature

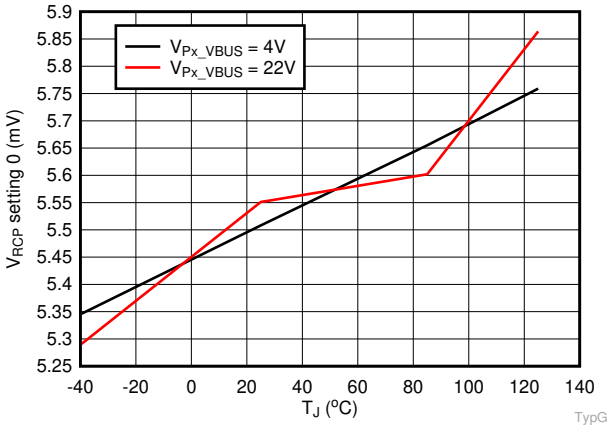


Figure 6-3. V_{RCP} vs. Temperature

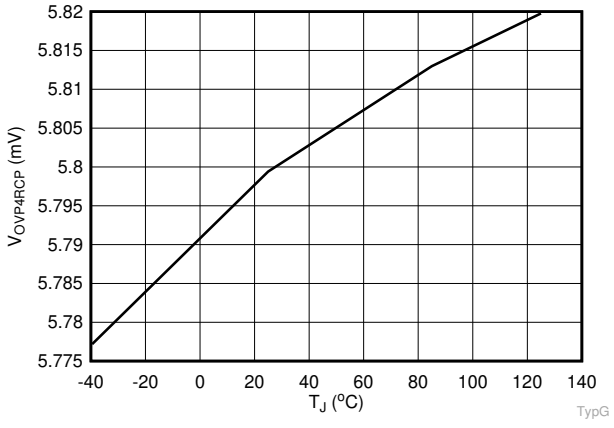


Figure 6-4. $V_{OVP4RCP}$ (Setting 2) vs. Temperature

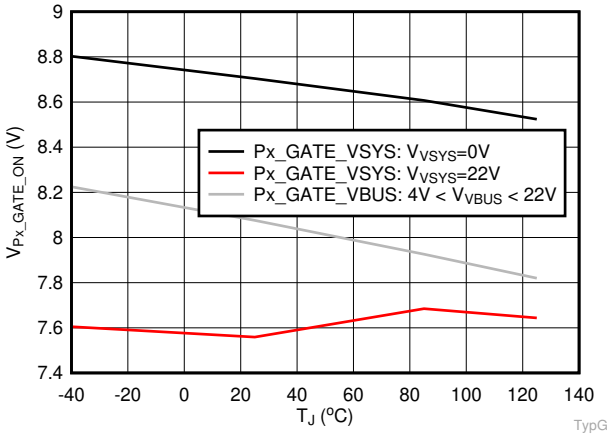


Figure 6-5. $V_{Px\_GATE\_ON}$ vs. Temperature

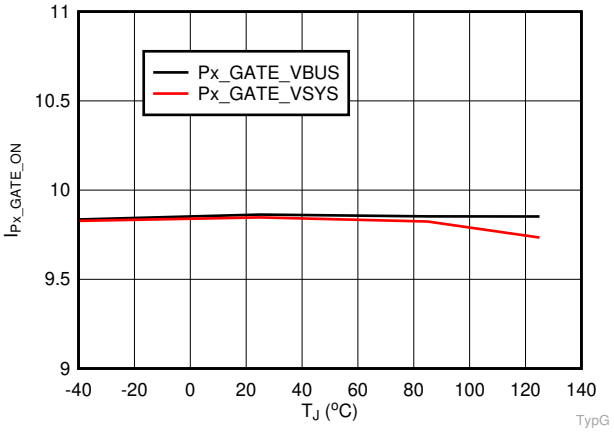


Figure 6-6. $I_{PX\_GATE\_ON}$ vs. Temperature

7 Parameter Measurement Information

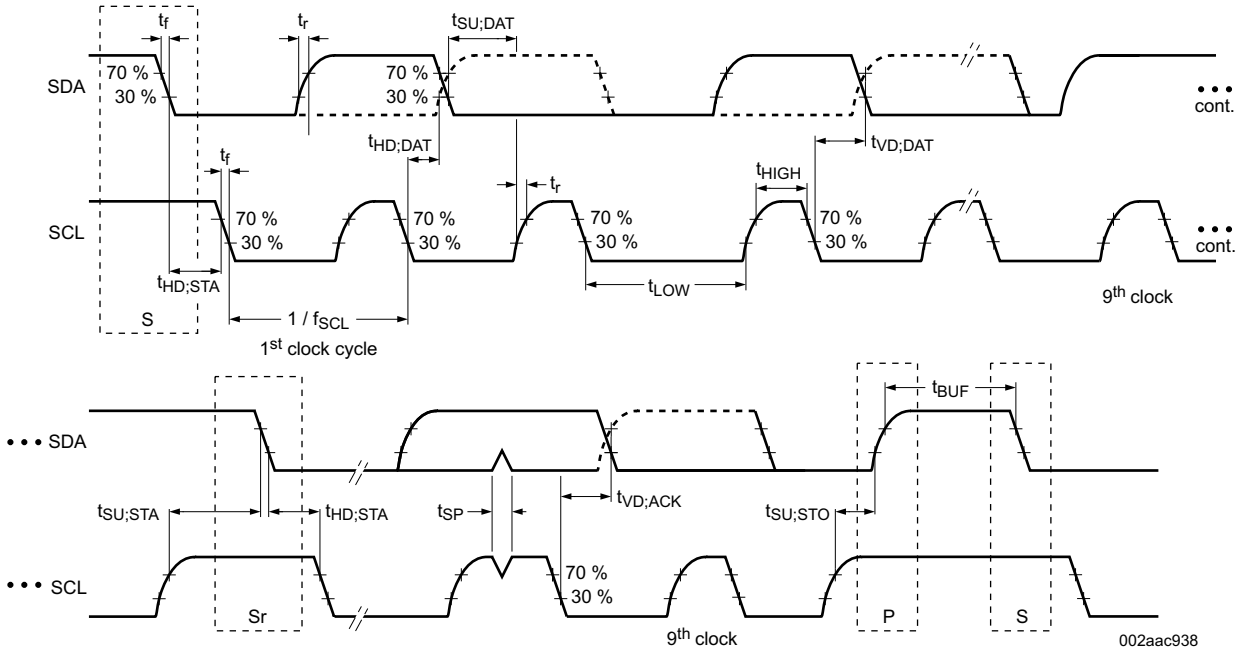


Figure 7-1. I²C Slave Interface Timing

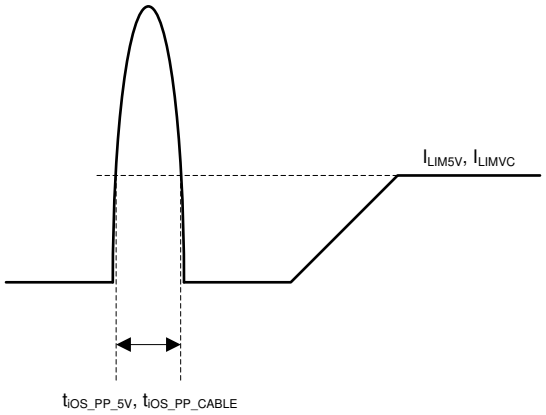


Figure 7-2. Short-Circuit Response Time for Internal Power Paths PP_5Vx and PP_CABLEx

8 Detailed Description

8.1 Overview

The TPS65994AE is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for two USB Type-C and PD receptacles. The TPS65994AE communicates with the cable and another USB Type-C and PD device at the opposite end of the cable, enables integrated port power switch for sourcing, controls a high current port power switch for sinking and negotiates alternate modes for each port. The TPS65994AE may also control an attached super-speed multiplexer to simultaneously support USB data and DisplayPort video.

Each Type-C port controlled by the TPS65994AE is functionally identical and supports the full range of the USB Type-C and PD standards.

The TPS65994AE is divided into several main sections: the USB-PD controller, the cable plug and orientation detection circuitry, the port power switches, the power management circuitry and the digital core.

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the Px_CC1 pin or the Px_CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features and more detailed circuitry, see the *USB-PD Physical Layer* section.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, see the *Cable Plug and Orientation Detection*.

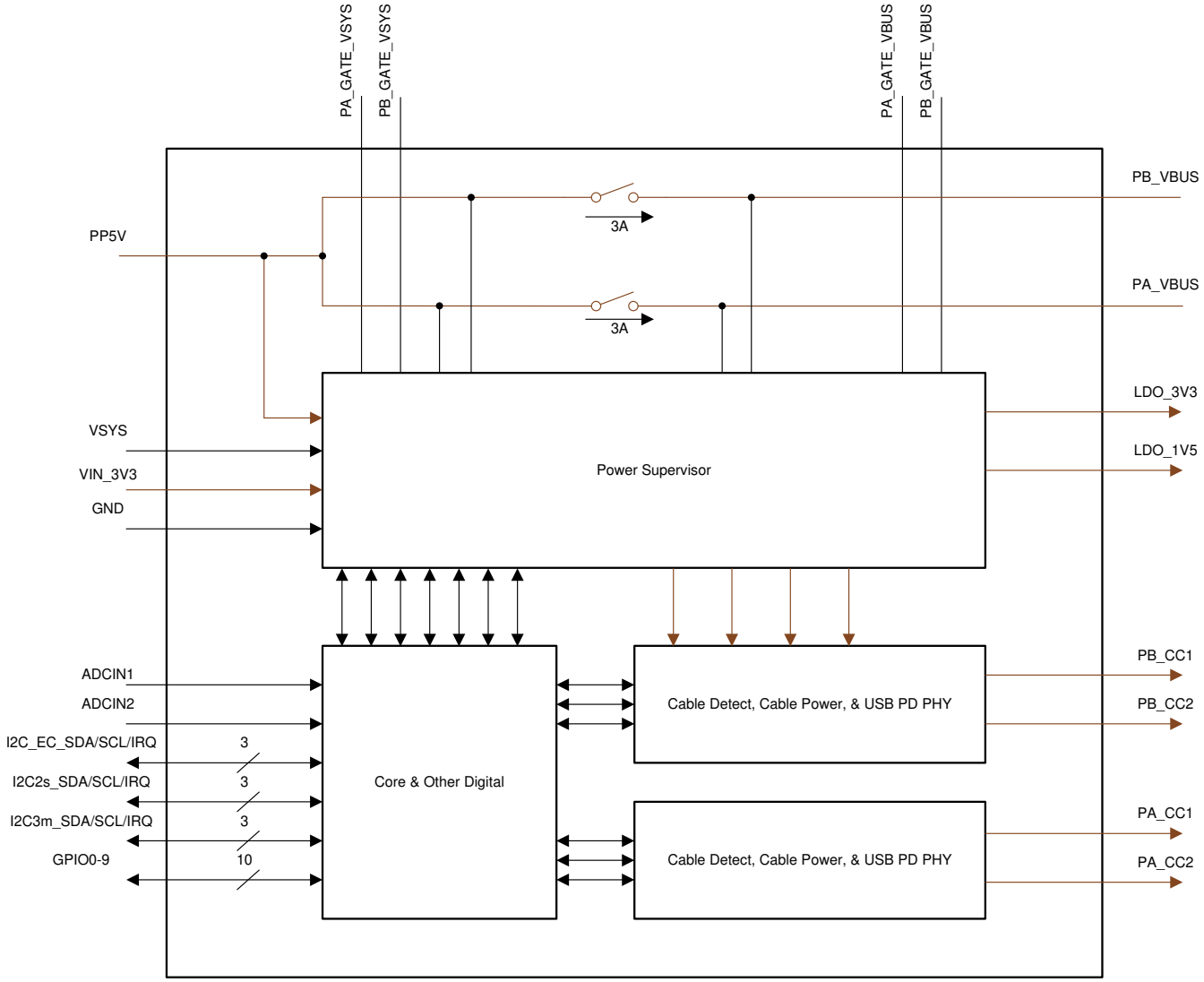
The port power switches provide power to the Px_VBUS pin and also to the Px_CC1 or Px_CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features and more detailed circuitry, see the *Power Paths*.

The digital core provides the engine for receiving, processing and sending all USB-PD packets as well as handling control of all other TPS65994AE functionality. A portion of the digital core contains ROM memory which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM, called boot code, is capable of initializing the TPS65994AE, loading of device configuration information and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of its features and more detailed circuitry, see the *Digital Core* section.

The digital core of the TPS65994AE also interprets and uses information provided by the analog-to-digital converter ADC (see the *ADC*), is configurable to read the status of general purpose inputs and trigger events accordingly, and controls general outputs which are configurable as push-pull or open-drain types with integrated pull-up or pull-down resistors. The TPS65994AE has two I^2C slave ports to be controlled by host processors , and one I^2C master to write to and read from external slave devices such as multiplexor, retimer, or an optional external EEPROM memory (see the *I^2C Interface*).

The TPS65994AE also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB-PD Physical Layer

Figure 8-1 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block. This block is duplicated for the second TPS65994AE port.

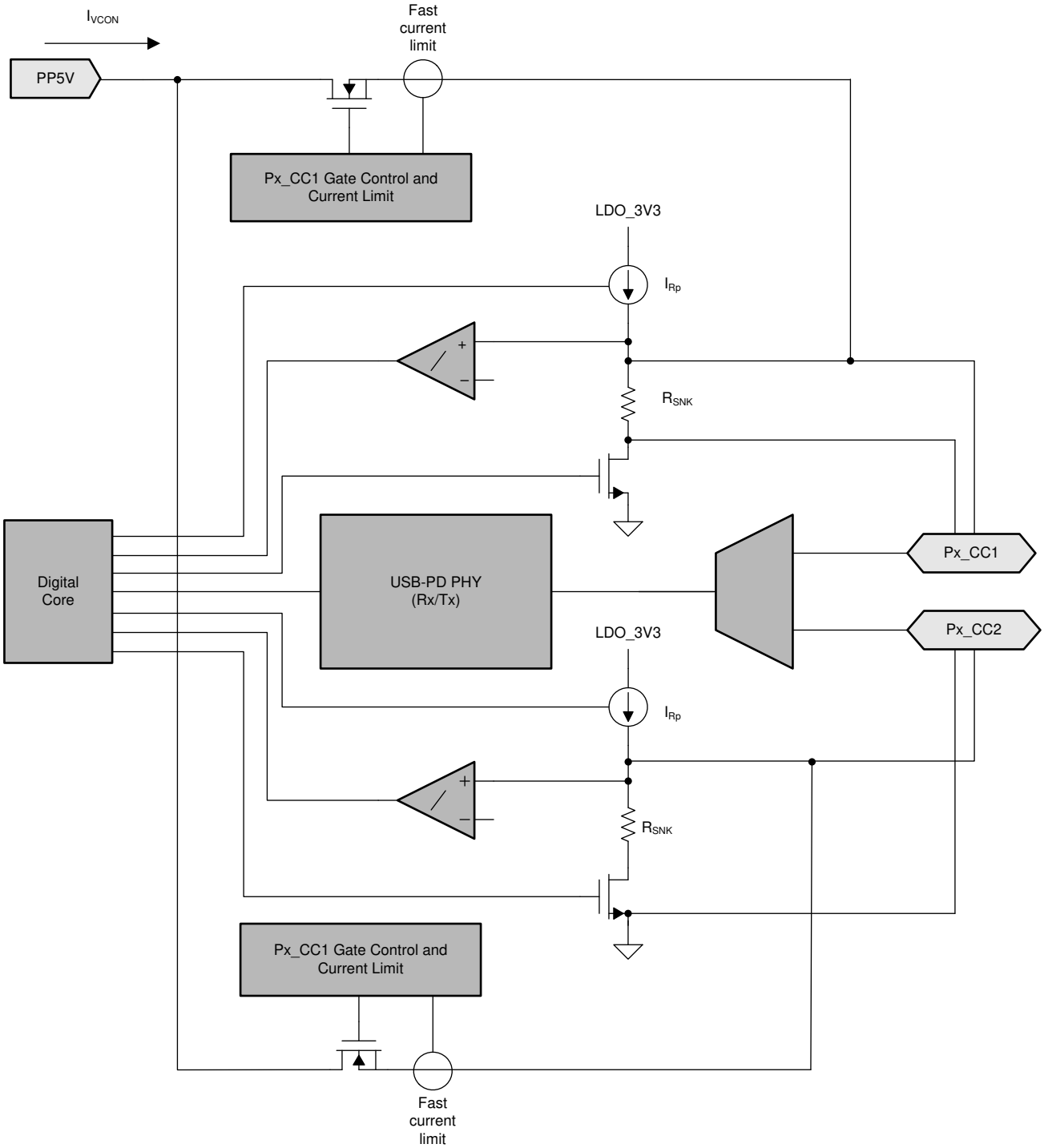


Figure 8-1. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (Px_CC1 or Px_CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism.

8.3.1.1 USB-PD Encoding and Signaling

Figure 8-2 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 8-3 illustrates the high-level block diagram of the baseband USB-PD receiver.

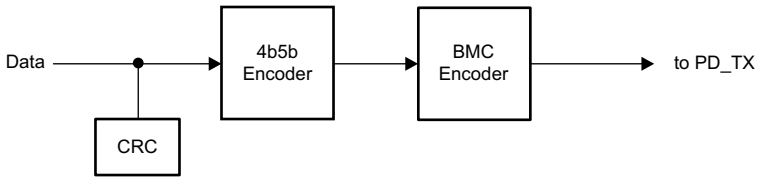


Figure 8-2. USB-PD Baseband Transmitter Block Diagram

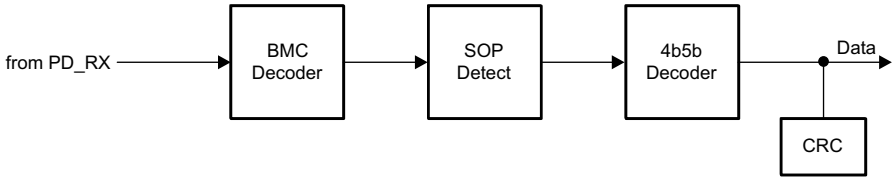


Figure 8-3. USB-PD Baseband Receiver Block Diagram

8.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS65994AE is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Figure 8-4 illustrates Biphase Mark Coding.

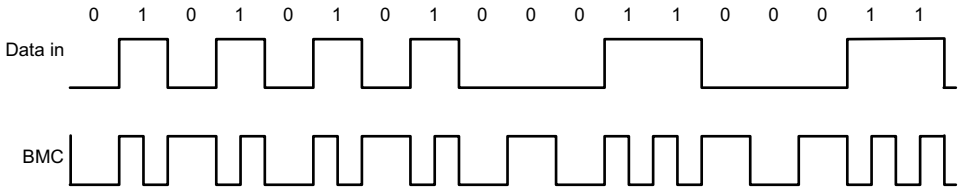


Figure 8-4. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the Px_CC1 or Px_CC2 pin with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

8.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Since a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the *USB-PD Specifications* for more details.

8.3.1.4 USB-PD BMC Transmitter

The TPS65994AE transmits and receives USB-PD data over one of the Px_CCy pins for a given CC pin pair (one pair per USB Type-C port). The Px_CCy pins are also used to determine the cable orientation and maintain

the cable/device attach detection. Thus, a DC bias exists on the Px_CCy pins. The transmitter driver overdrives the Px_CCy DC bias while transmitting, but returns to a Hi-Z state allowing the DC voltage to return to the Px_CCy pin when not transmitting. While either Px_CC1 or Px_CC2 may be used for transmitting and receiving, during a given connection only the one that mates with the CC pin of the plug is used; so there is no dynamic switching between Px_CC1 and Px_CC2. Figure 8-5 shows the USB-PD BMC TX and RX driver block diagram.

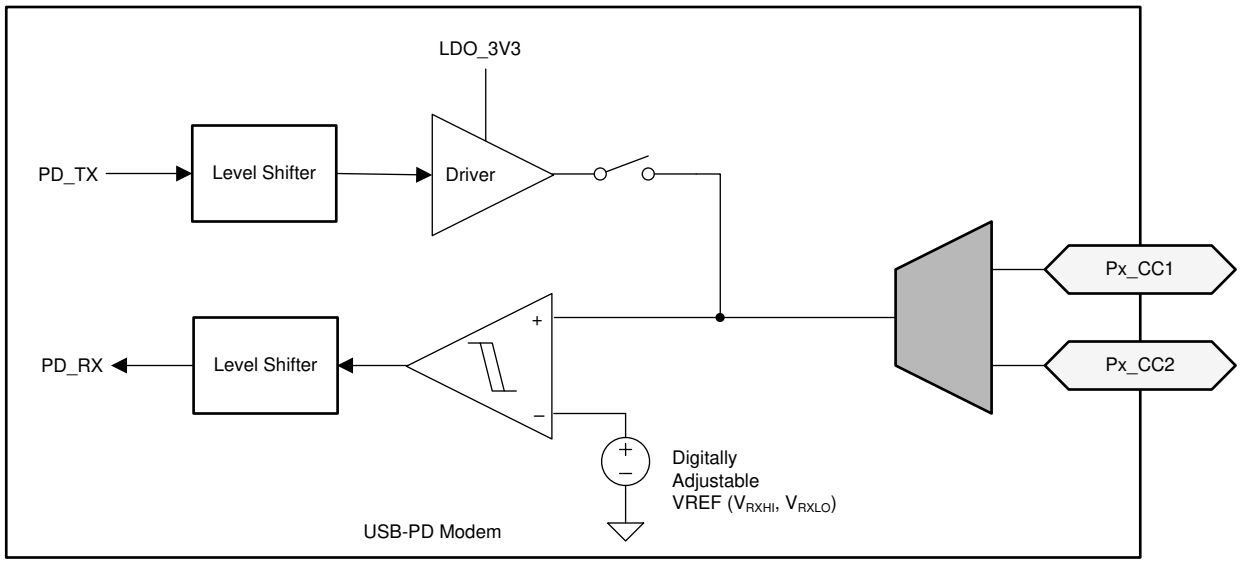


Figure 8-5. USB-PD BMC TX/Rx Block Diagram

Figure 8-6 shows the transmission of the BMC data on top of the DC bias. Note, The DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This means that the DC bias can be above or below the VOH of the transmitter driver.

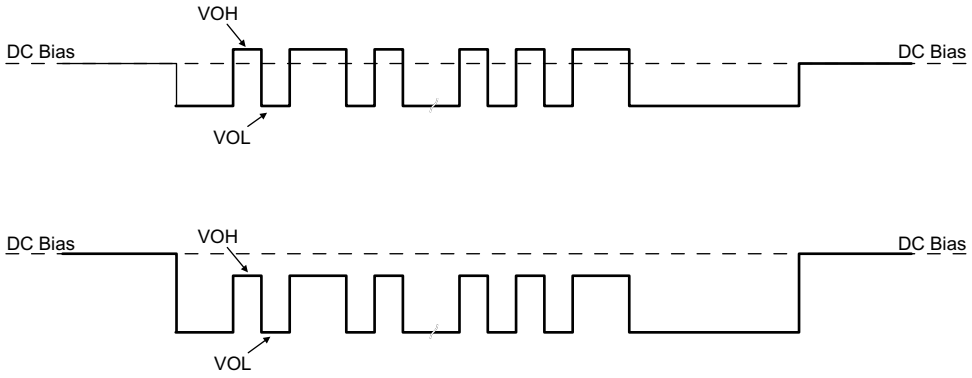


Figure 8-6. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the Px_CCy lines. The signal peak, V_{TXHI}, is set to meet the TX masks defined in the *USB-PD Specifications*. Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER}. Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingression in the cable.

Figure 8-7 shows the simplified circuit determining Z_{DRIVER}. It is specified such that noise at the receiver is bounded.

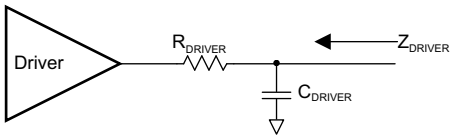


Figure 8-7. ZDRIVER Circuit

8.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS65994AE receives a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

Figure 8-8 shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The *USB-PD Specification* also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

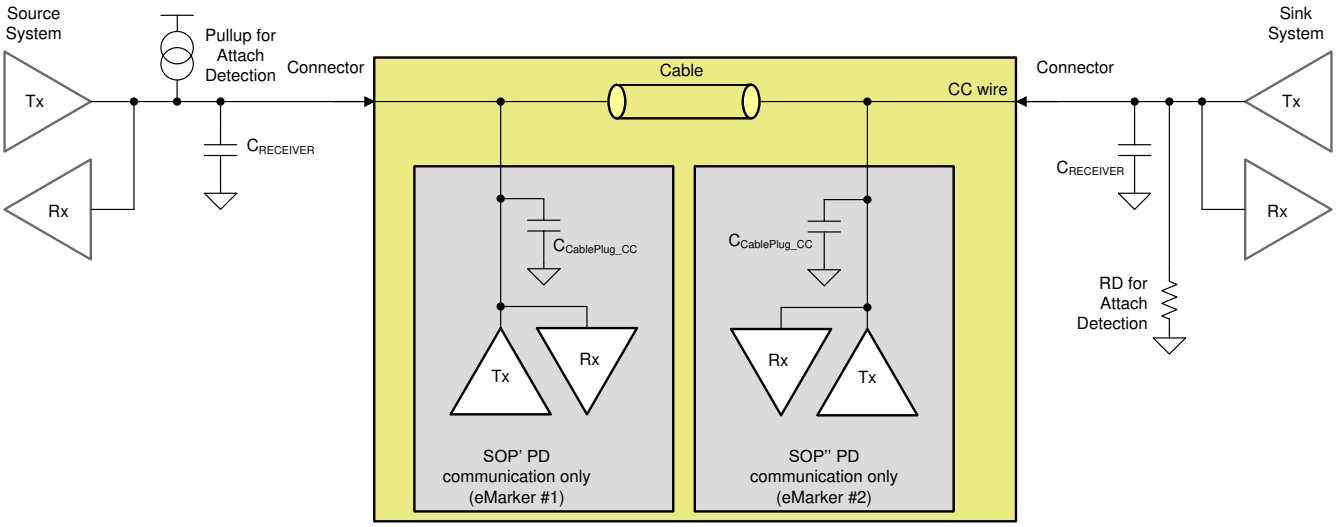


Figure 8-8. Example USB-PD Multi-Drop Configuration

8.3.1.6 Squelch Receiver

The TPS65994AE has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification.

8.3.2 Power Management

The TPS65994AE power management block receives power and generates voltages to provide power to the TPS65994AE internal circuitry. These generated power rails are LDO_3V3 and LDO_1V5. LDO_3V3 may also be used as a low power output for external EEPROM memory. The power supply path is shown in Figure 8-9.

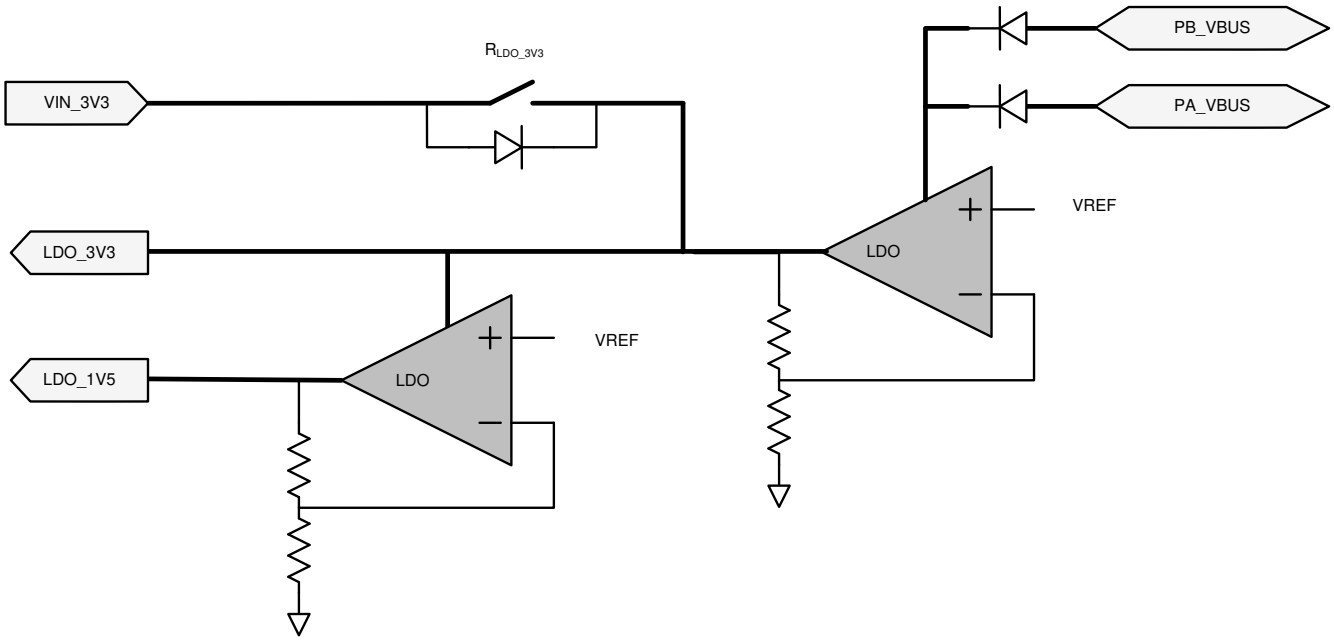


Figure 8-9. Power Supplies

The TPS65994AE is powered from either VIN_3V3, PA_VBUS, or PB_VBUS. The normal power supply input is VIN_3V3. When powering from VIN_3V3, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V5 to power the 1.5-V core digital circuitry. When VIN_3V3 power is unavailable and power is available on PA_VBUS, or PB_VBUS it is referred to as the dead-battery startup condition. In a dead-battery startup condition, the TPS65994AE opens the VIN_3V3 switch until the host clears the dead-battery flag via I^2C. Therefore, the TPS65994AE is powered from the VBUS input with the higher voltage during the dead-battery startup condition and until the dead-battery flag is cleared. When powering from a VBUS input, the voltage on PA_VBUS, or PB_VBUS is stepped down through an LDO to LDO_3V3.

8.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

8.3.2.2 VBUS LDO

The TPS65994AE contains an internal high-voltage LDO which is capable of converting Px_VBUS to 3.3 V for powering internal device circuitry. The VBUS LDO is only used when VIN_3V3 is low (the dead-battery condition). The VBUS LDO is powered from either PA_VBUS, or PB_VBUS ; the one with the highest voltage.

8.3.3 Power Paths

The TPS65994AE has internal sourcing power paths: PP_5V1, PP_5V2, PP_CABLE1, and PP_CABLE2. It also has control for external power paths: PP_EXT1, and PP_EXT2. Each power path is described in detail in this section.

8.3.3.1 Internal Sourcing Power Paths

Figure 8-10 shows the TPS65994AE internal sourcing power paths. The TPS65994AE features four internal 5-V sourcing power paths. The path from PP5V to PA_VBUS is called PP_5V1 , and the path from PP5V to PB_VBUS is called PP_5V2. The path from PP5V to PA_CCx is called PP_CABLE1 , and the path from PP5V to PB_CCy is called PP_CABLE2. Each path contains current clamping protection, overvoltage protection, UVLO protection and temperature sensing circuitry. PP_5V1 and PP_5V2 may each conduct up to 3 A continuously, while PP_CABLE1 and PP_CABLE2 may conduct up to 315 mA continuously. When disabled, the blocking FET protects the PP5V rail from high-voltage that may appear on Px_VBUS.

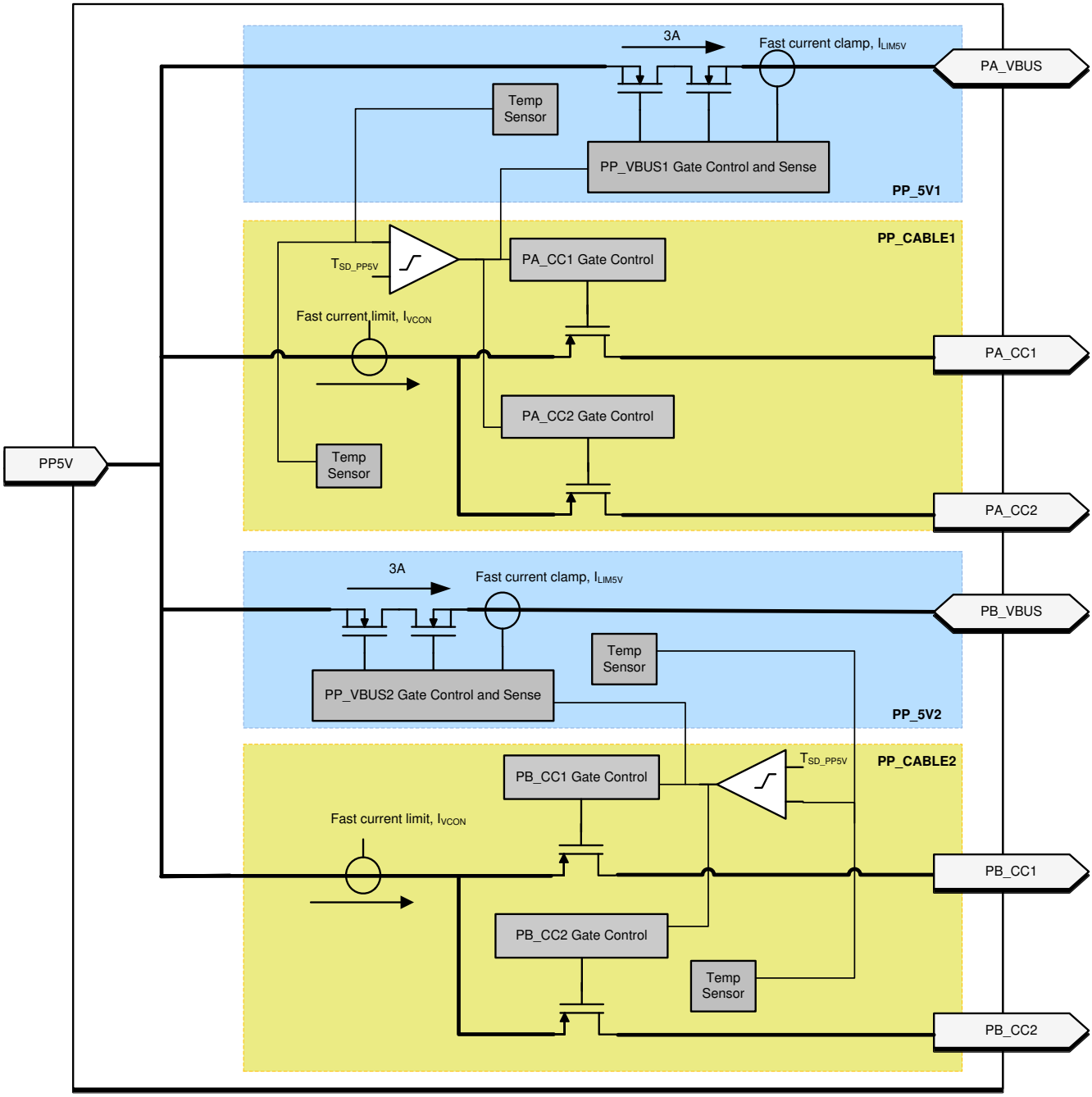


Figure 8-10. Port Power Switches

8.3.3.1.1 PP_5Vx Current Clamping

The current through the internal PP_5Vx paths are current limited to I_{LIM5V}. The I_{LIM5V} value is configured by application firmware. When the current through the switch exceeds I_{LIM5V}, the current limiting circuit activates within $t_{iOS\_PP\_5V}$ and the path behaves as a constant current source. If the duration of the overcurrent event exceeds t_{ILIM}, the PP_5V switch is disabled.

8.3.3.1.2 PP_5Vx Local Overtemperature Shut Down (OTSD)

When PP_5Vx clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP_5Vx or PP_CABLEx detect that $T_J > T_{SD\_PP5V}$ the PP_5Vx switch is disabled and the affected port enters the USB Type-C ErrorRecovery state.

8.3.3.1.3 PP_5Vx Current Sense

The current from PP5V to Px_VBUS is sensed through the switch and passed to the internal ADC.

8.3.3.1.4 PP_5Vx OVP

The overvoltage protection level is automatically configured based on the expected maximum V_{BUS} voltage, which depends upon the USB PD contract. When the voltage on a port's Px_VBUS pin exceeds the configured value ($V_{OVP4RCP}$) while PP_5Vx is enabled, then PP_5Vx is disabled within $t_{PP\_5V\_ovp}$ and the affected port enters into the Type-C ErrorRecovery state.

8.3.3.1.5 PP_5Vx UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}) while PP_5Vx is enabled, then PP_5Vx is disabled within $t_{PP\_5V\_uvlo}$ and the port that had PP_5Vx enabled enters into the Type-C ErrorRecovery state.

8.3.3.1.6 PP_5Vx Reverse Current Protection

If V_{Px_VBUS} - V_{PP5V} > $V_{PP\_5V\_RCP}$, then the PP_5Vx path is automatically disabled within $t_{PP\_5V\_rcp}$. If the RCP condition clears, then the PP_5Vx path is automatically enabled within t_{ON}.

8.3.3.1.7 Fast Role Swap

The TPS65994AE supports Fast Role Swap as defined by USB PD. The PP_5Vx path has a fast turn-on mode that application firmware selectively enables to support Fast Role Swap. When enabled it is engaged when

V_{Px_VBUS} - V_{PP5V}<$V_{PP\_5V\_RCP}$, and turns on the switch within t_{FRS_on}.

8.3.3.1.8 PP_CABLE Current Clamp

When enabled and providing VCONN power the TPS65994AE PP_CABLE power switches clamp the current to I_{VCON}. When the current through the PP_CABLEx switch exceeds I_{VCON}, the current clamping circuit activates within $t_{iOS\_PP\_CABLE}$ and the switch behaves as a constant current source. The switches do not have reverse current blocking when the switch is enabled and current is flowing to either Px_CC1 or Px_CC2.

8.3.3.1.9 PP_CABLE Local Overtemperature Shut Down (OTSD)

When PP_CABLEx clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP_5Vx or PP_CABLEx detect that T_J>T_{SD_PP5V} the PP_CABLEx switch is disabled and latched off within $t_{PP\_CABLE\_off}$. The port then enters the USB Type-C ErrorRecovery state.

8.3.3.1.10 PP_CABLE UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}), then both PP_CABLE1 and PP_CABLE2 switches are automatically disabled within $t_{PP\_CABLE\_off}$.

8.3.3.2 Sink Path Control

The sink-path control includes overvoltage protection (OVP), and reverse current protection (RCP).

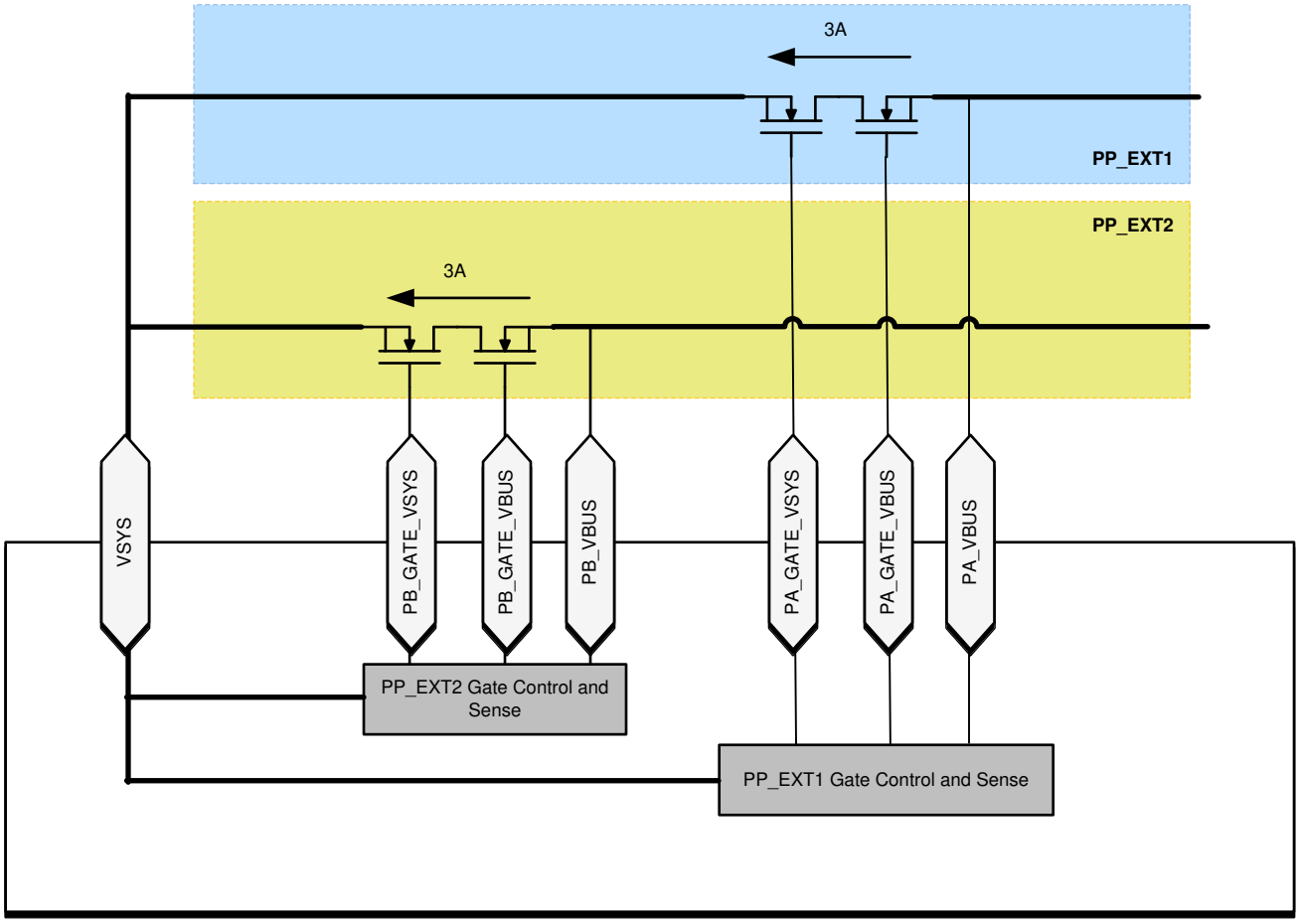


Figure 8-11. Sink Path Control

The following figure shows the Px_GATE_VSYS gate driver in more detail.

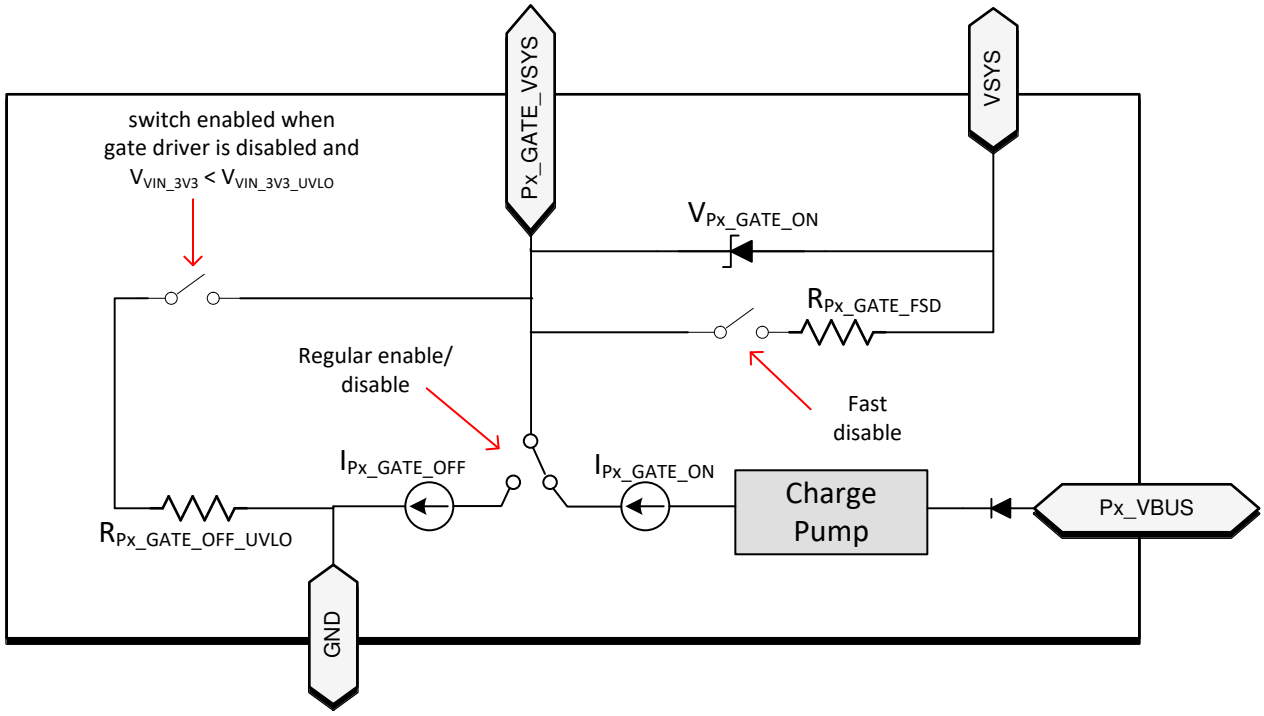


Figure 8-12. Details of the Px_GATE_VSYS gate driver.

8.3.3.2.1 Overvoltage Protection (OVP)

The application firmware enables the OVP and configures it based on the expected Px_VBUS voltage. If the voltage on Px_VBUS surpasses the configured threshold $V_{OVP4VSYS}$ = $V_{OVP4RCP}/r_{OVP}$, then Px_GATE_VSYS is automatically disabled within $t_{Px\_GATE\_VSYS\_FSD}$ to protect the system. If the voltage on Px_VBUS surpasses the configured threshold $V_{OVP4RCP}$ then Px_GATE_VBUS is automatically disabled within $t_{Px\_GATE\_VBUS\_OVP}$. When V_{Px_VBUS} falls below $V_{OVP4RCP}$ - $V_{OVP4RCPH}$Px_GATE_VBUS is automatically re-enabled within $t_{Px\_GATE\_VBUS\_ON}$ since the OVP condition has cleared. This allows two sinking power paths to be enabled simultaneously and Px_GATE_VBUS will be disabled when necessary to ensure that V_{Px_VBUS} remains below $V_{OVP4RCP}$.

While the TPS65994AE is in the BOOT mode in a dead-battery scenario (that is VIN_3V3 is low) it handles an OVP condition slightly differently. As long as the OVP condition is present Px_GATE_VBUS and Px_GATE_VSYS are disabled. Once the OVP condition clears, both Px_GATE_VBUS and Px_GATE_VSYS are re-enabled (unless ADCINx are configured in SafeMode). Since this is a dead-battery condition, the TPS65994AE will be drawing approximately $I_{VIN\_3V3,ActSnk}$ from PA_VBUS or PB_VBUS during this time to help discharge it.

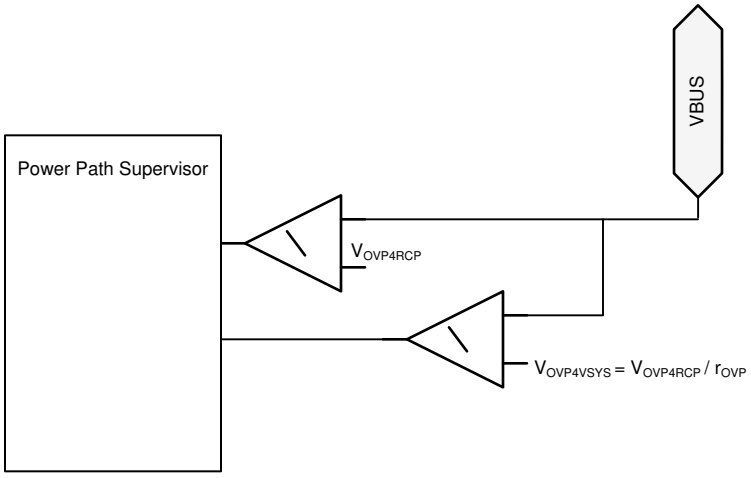


Figure 8-13. Diagram for OVP Comparators

8.3.3.2.2 Reverse-Current Protection (RCP)

The VSYS gate control circuit monitors the VSYS and Px_VBUS voltages and detects reverse current when the V_{VSYS} surpasses V_{Px_VBUS} by more than V_{RCP}. When the reverse current condition is detected, Px_GATE_VBUS is disabled within $t_{Px\_GATE\_VBUS\_RCP}$. When the reverse current condition is cleared, Px_GATE_VBUS is re-enabled within $t_{Px\_GATE\_VBUS\_ON}$. This limits the amount of reverse current that may flow from VSYS to Px_VBUS through the external N-ch MOSFETs.

In reverse current protection mode, the power switch controlled by Px_GATE_VBUS is allowed to behave resistively until the current reaches V_{RCP}/ R_{ON} and then blocks reverse current from VSYS to Px_VBUS , where R_{ON} is the resistance of the external back-to-back N-ch MOSFET. Figure 8-14 shows the behavior of the switch.

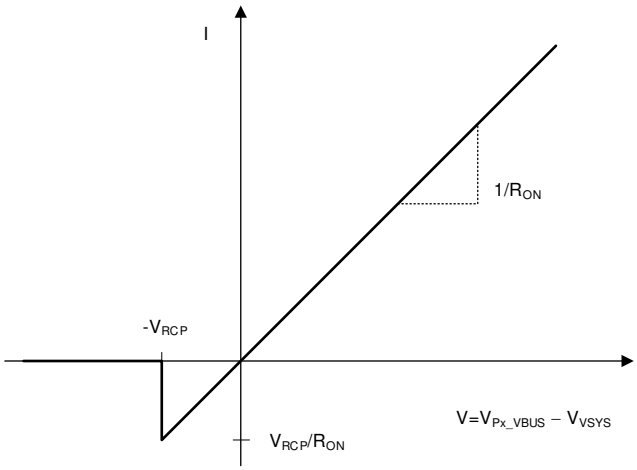


Figure 8-14. Switch I-V Curve for RCP on External Switches

8.3.3.2.3 VBUS UVLO

The TPS65994AE monitors Px_VBUS voltage and detects when it falls below V_{VBUS_UVLO}. When the UVLO condition is detected, Px_GATE_VBUS is disabled within $t_{Px\_GATE\_VBUS\_RCP}$. When the UVLO condition is cleared, Px_GATE_VBUS is re-enabled within $t_{Px\_GATE\_VBUS\_ON}$.

8.3.3.2.4 Discharging VBUS to Safe Voltage

The TPS65994AE has an integrated active pull-down (I_{DSCH}) on Px_VBUS for discharging from high voltage to VSAFE0V (0.8 V). This discharge is applied when it is in an Unattached Type-C state.

8.3.4 Cable Plug and Orientation Detection

Figure 8-15 shows the plug and orientation detection block at each Px_CCy pin (PA_CC1, PA_CC2, PB_CC1, PB_CC2). Each pin has identical detection circuitry.

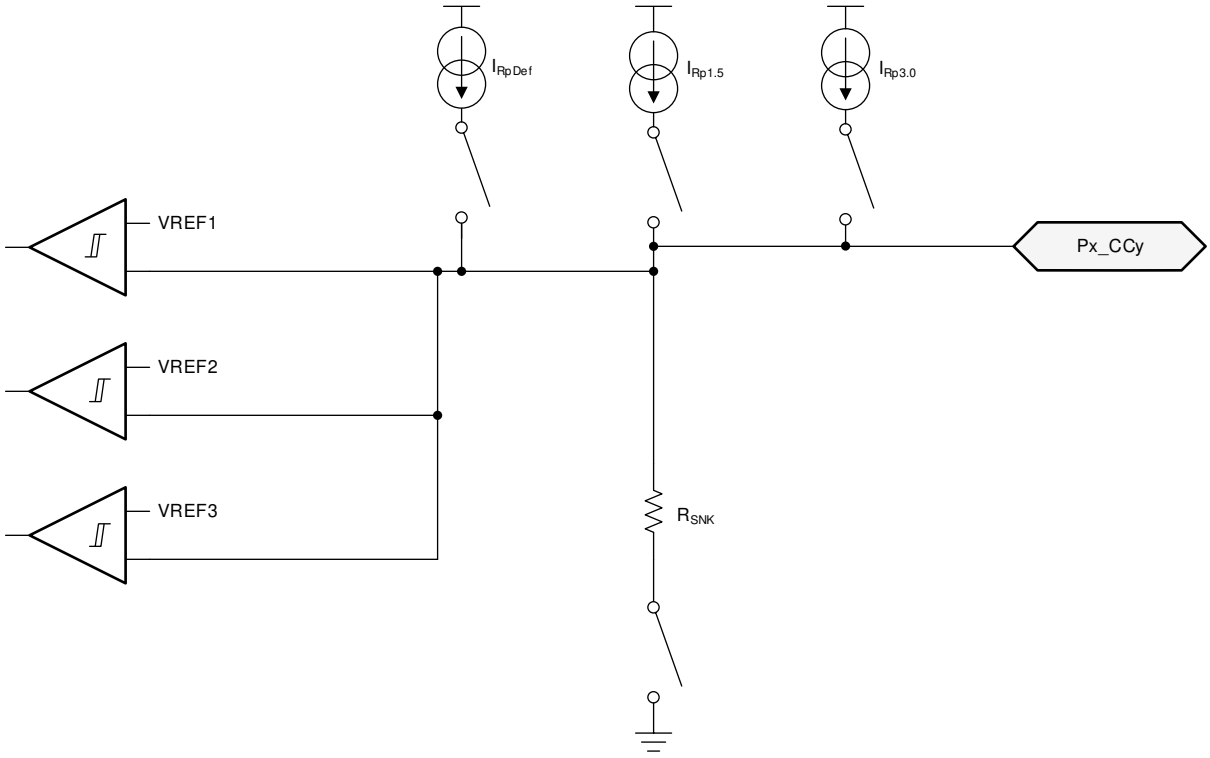


Figure 8-15. Plug and Orientation Detection Block

8.3.4.1 Configured as a Source

When configured as a source, the TPS65994AE detects when a cable or a Sink is attached using the Px_CC1 and Px_CC2 pins. When in a disconnected state, the TPS65994AE monitors the voltages on these pins to determine what, if anything, is connected. See *USB Type-C Specification* for more information.

Table 8-1 shows the Cable Detect States for a Source.

Table 8-1. Cable Detect States for a Source

Px_CC1	Px_CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both Px_CCy pins for attach. Power is not applied to Px_VBUS or VCONN.
Rd	Open	Sink attached	Monitor Px_CC1 for detach. Power is applied to Px_VBUS but not to VCONN (Px_CC2).
Open	Rd	Sink attached	Monitor Px_CC2 for detach. Power is applied to Px_VBUS but not to VCONN (Px_CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor Px_CC2 for a Sink attach and Px_CC1 for cable detach. Power is not applied to Px_VBUS or VCONN (Px_CC1).
Open	Ra	Powered Cable-No UFP attached	Monitor Px_CC1 for a Sink attach and Px_CC2 for cable detach. Power is not applied to Px_VBUS or VCONN (Px_CC1).
Ra	Rd	Powered Cable-UFP Attached	Provide power on Px_VBUS and VCONN (Px_CC1) then monitor Px_CC2 for a Sink detach. Px_CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on Px_VBUS and VCONN (Px_CC2) then monitor Px_CC1 for a Sink detach. Px_CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either Px_CCy pin for detach.

Table 8-1. Cable Detect States for a Source (continued)

Px_CC1	Px_CC2	CONNECTION STATE	RESULTING ACTION
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either Px_CCy pin for detach.

When a TPS65994AE port is configured as a Source, a current I_{RpDef} is driven out each Px_CCy pin and each pin is monitored for different states. When a Sink is attached to the pin a pull-down resistance of Rd to GND exists. The current I_{RpDef} is then forced across the resistance Rd generating a voltage at the Px_CCy pin. The TPS65994AE applies I_{RpDef} until it closes the switch from PP5V to Px_VBUS, at which time application firmware may change to $I_{Rp1.5A}$ or $I_{Rp3.0A}$.

When the Px_CCy pin is connected to an active cable VCONN input, the pull-down resistance is different (Ra). In this case the voltage on the Px_CCy pin will be lower and the TPS65994AE recognizes it as an active cable.

The voltage on Px_CCy is monitored to detect a disconnection depending upon which Rp current source is active. When a connection has been recognized and the voltage on Px_CCy subsequently rises above the disconnect threshold for t_{CC}, the system registers a disconnection.

8.3.4.2 Configured as a Sink

When a TPS65994AE port is configured as a Sink, the TPS65994AE presents a pull-down resistance R_{SNK} on each Px_CCy pin and waits for a Source to attach and pull-up the voltage on the pin. The Sink detects an attachment by the presence of VBUS. The Sink determines the advertised current from the Source based on the voltage on the Px_CCy pin.

8.3.4.3 Configured as a DRP

When a TPS65994AE port is configured as a DRP, the TPS65994AE alternates the port's Px_CCy pins between the pull-down resistance, R_{SNK}, and pull-up current source, I_{Rp}.

8.3.4.4 Fast Role Swap Signal Detection

The TPS65994AE cable plug block contains additional circuitry that may be used to support the Fast Role Swap (FRS) behavior defined in the *USB Power Delivery Specification*. The circuitry provided for this functionality is detailed in Figure 8-16.

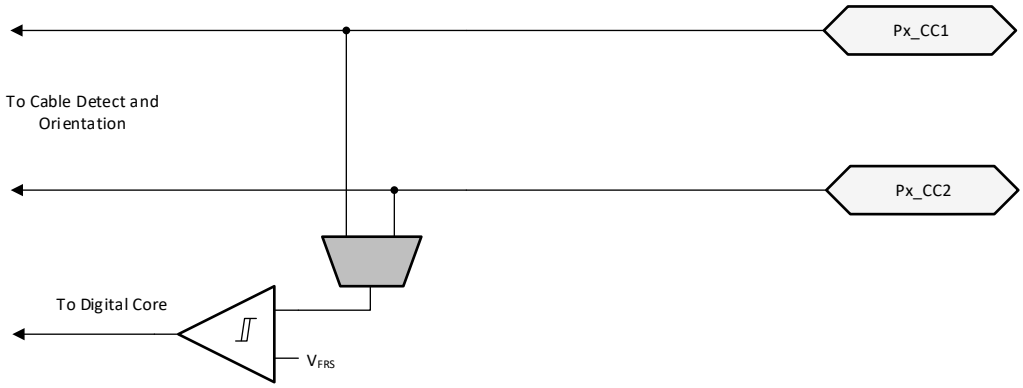


Figure 8-16. Fast Role Swap Detection and Signaling

When a TPS65994AE port is operating as a sink with FRS enabled, the TPS65994AE monitors the CC pin voltage. If the CC voltage falls below V_{FRS} for t_{FRS_DET} a fast role swap signal is detected and indicated to the digital core. When this signal is detected the TPS65994AE ceases operating as a sink (disables Px_GATE_VSYS and Px_GATE_VBUS) and begins operating as a source.

8.3.5 Default Behavior Configuration (ADCIN1, ADCIN2)

Note

This functionality is firmware controlled and subject to change.

The ADCINx inputs to the internal ADC control the behavior of the TPS65994AE in response to PA_VBUS or PB_VBUS being supplied when VIN_3V3 is low (that is the dead-battery scenario). The ADCINx pins must be externally tied to the LDO_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these two values to determine start-up behavior. The available start-up configurations include options for I^2C slave address of I2C_EC_SCL/SDA, sink path control in dead-battery, and default configuration.

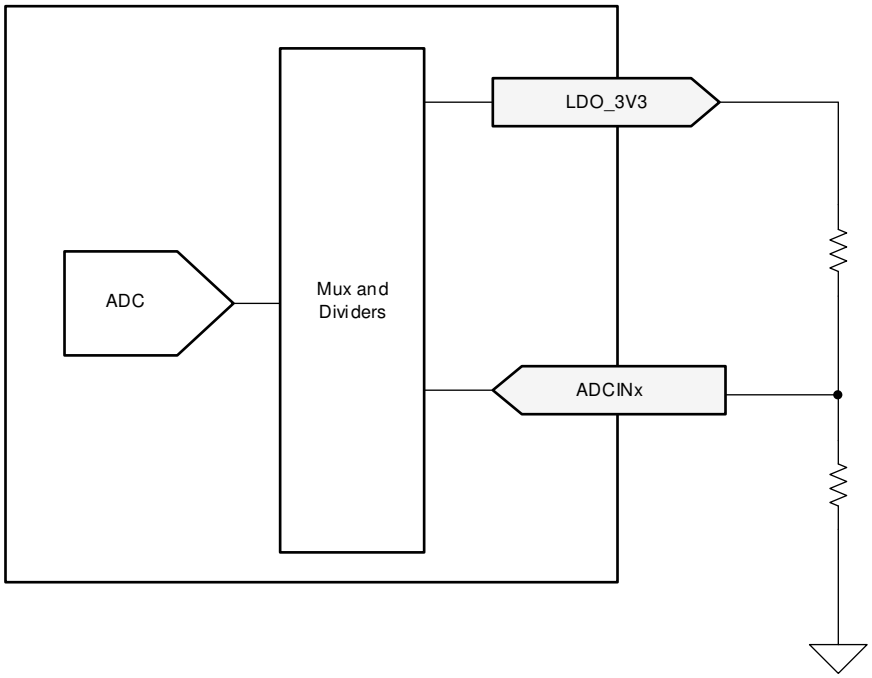


Figure 8-17. ADCINx Resistor Divider

The device behavior is determined in several ways depending upon the decoded value of the ADCIN1 and ADCIN2 pins. The following table shows the decoded values for different resistor divider ratios. See *Pin Strapping to Configure Default Behavior* for details on how the ADCINx configurations determine default device behavior. See *I^2C Address Setting* for details on how ADCINx decoded values affects default I^2C slave address.

Table 8-2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)			Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

(1) External resistor tolerance of 1% is recommended. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values. For convenience, the Target column shows this value.

8.3.6 ADC

The TPS65994AE ADC is shown in Figure 8-18. The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware.

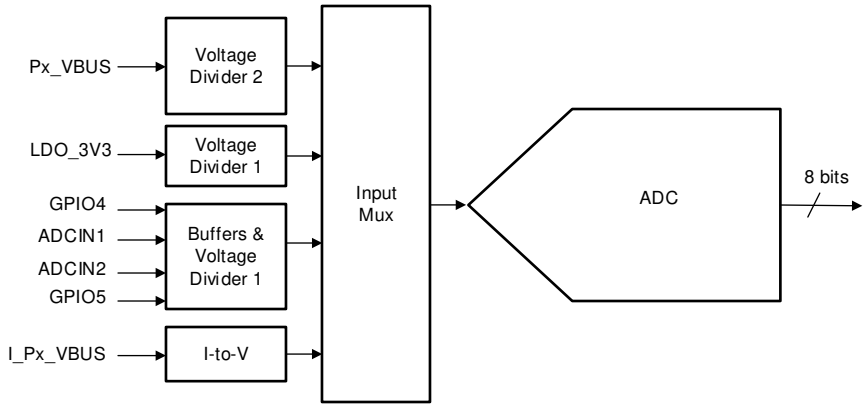


Figure 8-18. SAR ADC

8.3.7 DisplayPort Hot-Plug Detect (HPD)

The TPS65994AE supports the DisplayPort alternate mode as a DP source . It is recommended to use the virtual HPD functionality through I^2C. However, the TPS65994AE also supports the HPD converter functions on GPIO pins (See Table 8-3). The core will translate PD messaging events onto the HPD pin.

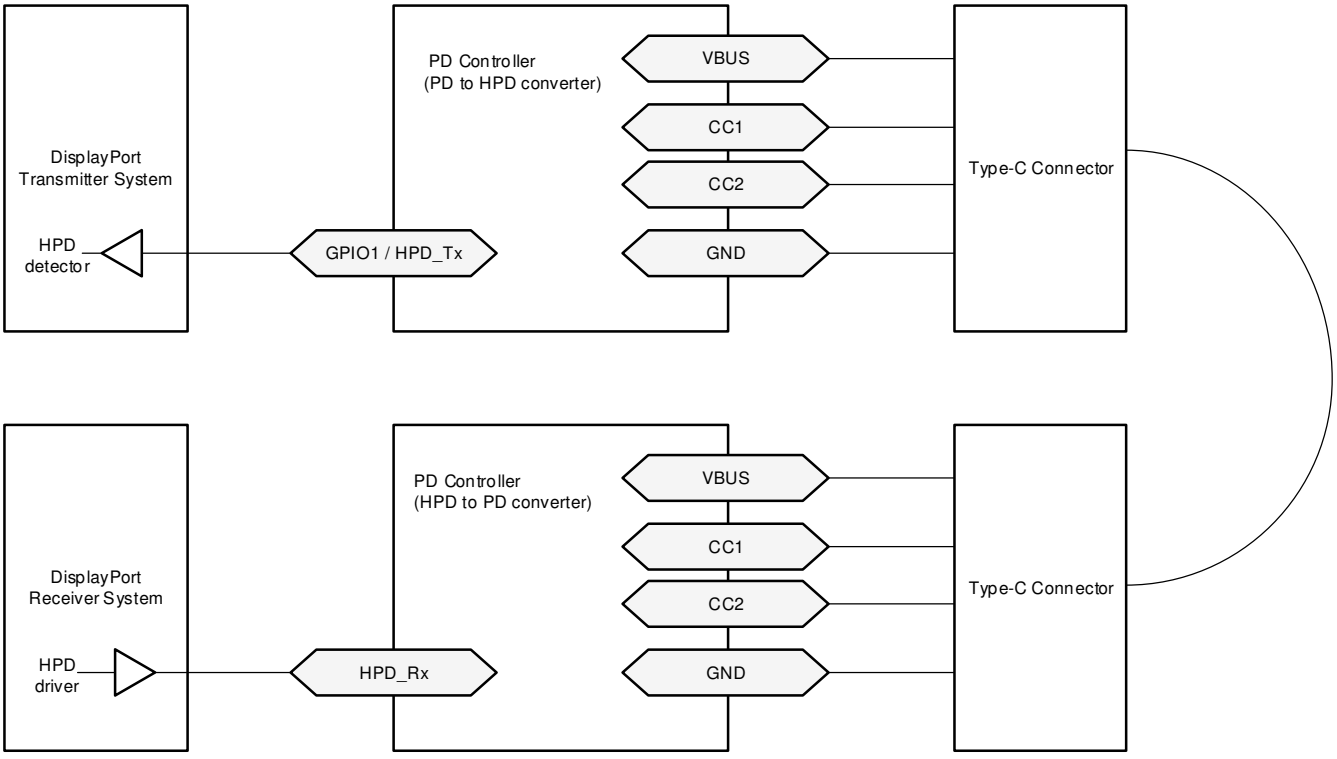


Figure 8-19. Illustration of how a PD-to-HPD Converter Passes the HPD Signal Along in a DisplayPort System

8.3.8 Digital Interfaces

The TPS65994AE contains several different digital interfaces which may be used for communicating with other devices. The available interfaces include two I²C Slaves and one I²C Master, and additional GPIOs.

8.3.8.1 General GPIO

GPIOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input or an analog input to the ADC (only a subset of the GPIO's are ADC inputs see table below). The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO_3V3 and LDO_1V5 to the input buffer. When interfacing with non 3.3-V I/O devices the output buffer may be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

Table 8-3. GPIO Functionality Table

Pin Name	Type	Special Functionality
GPIO0	I/O	HPD_Tx for Port B
GPIO1	I/O	HPD_Tx for Port A
GPIO2	I/O	
GPIO3	I/O	
GPIO4	I/O	ADC Input,
GPIO5	I/O	ADC Input,
GPIO6	I/O	
GPIO7	I/O	
GPIO8	I/O	
GPIO9	O	PROCHOT#
$\overline{\text{I2C\_EC\_IRQ}}$(GPIO10)	O	IRQ for I2C_EC, or used as a general-purpose output
$\overline{\text{I2C2s\_IRQ}}$(GPIO11)	O	IRQ for I2C2, or used as a general-purpose output
$\overline{\text{I2C3m\_IRQ}}$(GPIO12)	I	IRQ for I2C3, or used as a general-purpose input

8.3.8.2 I²C Interface

The TPS65994AE features three I²C interfaces that each use an I²C I/O driver like the one shown in Figure 8-20. This I/O consists of an open-drain output and in input comparator with de-glitching.

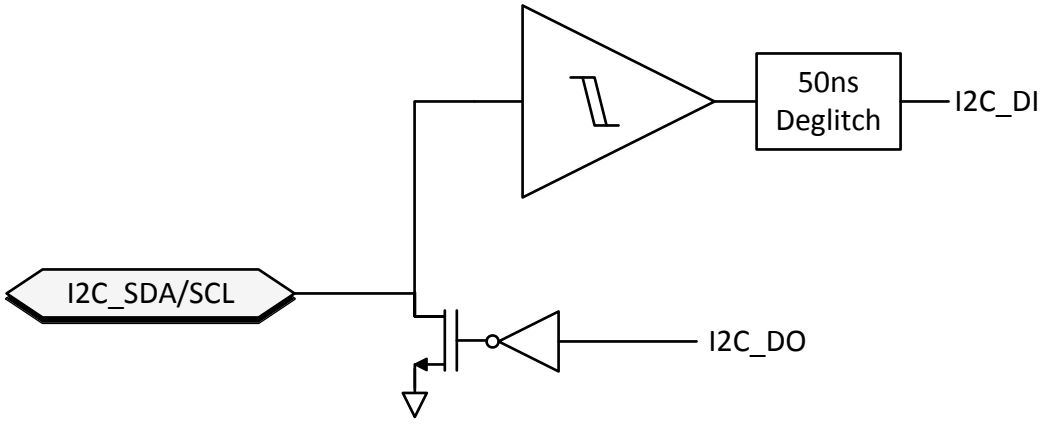


Figure 8-20. I²C Buffer

8.3.9 Digital Core

Figure 8-21 shows a simplified block diagram of the digital core.

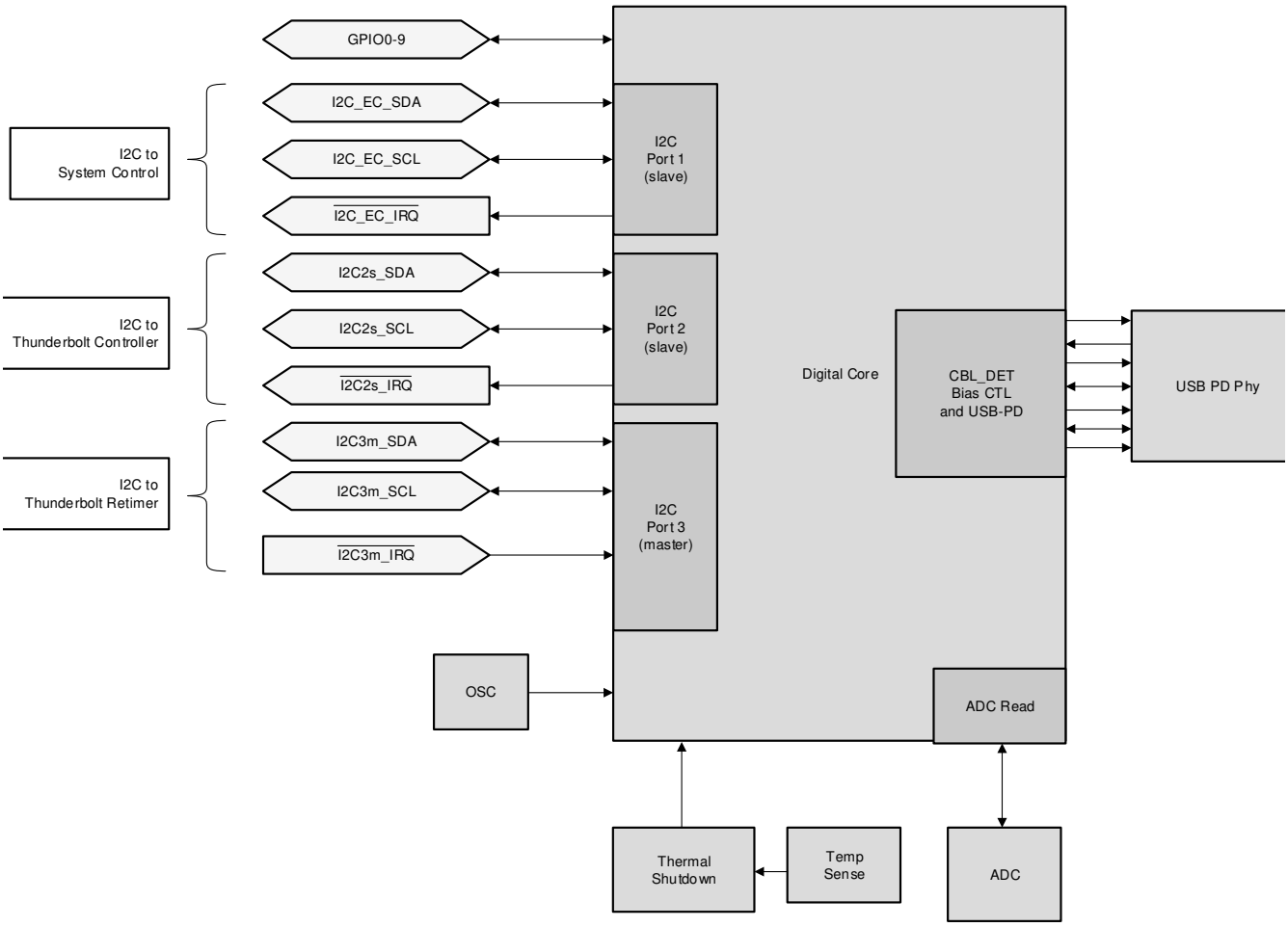


Figure 8-21. Digital Core Block Diagram

8.3.10 I²C Interface

The TPS65994AE has two I²C slave interface ports: I2C_EC and I2C2s. I²C port I2C_EC is comprised of the I2C_EC_SDA, I2C_EC_SCL, and $\overline{\text{I2C\_EC\_IRQ}}$ pins. I²C I2C2s is comprised of the I2C2s_SDA, I2C2s_SCL, and $\overline{\text{I2C2s\_IRQ}}$ pins. These interfaces provide general status information about the TPS65994AE, as well as the ability to control the TPS65994AE behavior, supporting communications to/from a connected device and/or cable supporting BMC USB-PD, and providing information about connections detected at the USB-C receptacle.

When the TPS65994AE is in 'APP ' mode it is recommended to use Standard Mode or Fast Mode (that is a clock speed no higher than 400 kHz). However, in the 'BOOT' mode when a patch bundle is loaded Fast Mode Plus may be used (see f_{SCLS}).

The TPS65994AE has one I²C master interface port: I2C3m. I2C3m is comprised of the I2C3m_SDA, I2C3m_SCL, and $\overline{\text{I2C3m\_IRQ1}}$ pins. This interface can be used to read from or write to external slave devices. During boot the TPS65994AE attempts to read patch and Application Configuration data from an external EEPROM with a 7-bit slave address of 0x50. The EEPROM should be at least 32 kilo-bytes.

Table 8-4. I²C Summary

I2C Bus	Type	Typical Usage
I2C_EC	Slave	Connect to an Embedded Controller (EC). Used to load the patch and application configuration.
I2C2s	Slave	Connect to a TBT controller or second master.

Table 8-4. I²C Summary (continued)

I2C Bus	Type	Typical Usage
I2C3m	Master	Connect to a TBT retimer, USB Type-C mux, I²C EEPROM, or other slave. Use the LDO_3V3 pin as the pull-up voltage. Multi-master configuration is not supported.

8.3.10.1 I²C Interface Description

The TPS65994AE supports Standard and Fast mode I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Figure 8-22 shows the start and stop conditions of the transfer. Figure 8-23 shows the SDA and SCL signals for transferring a bit. Figure 8-24 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

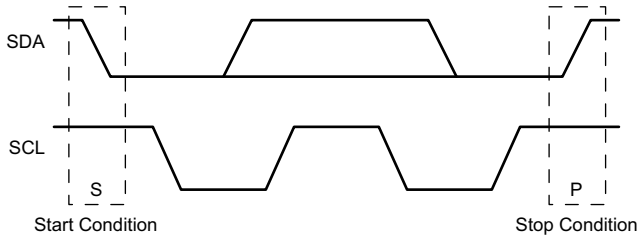


Figure 8-22. I²C Definition of Start and Stop Conditions

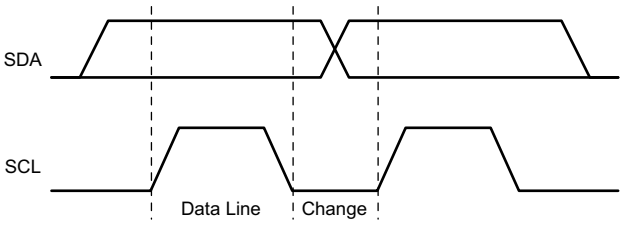


Figure 8-23. I²C Bit Transfer

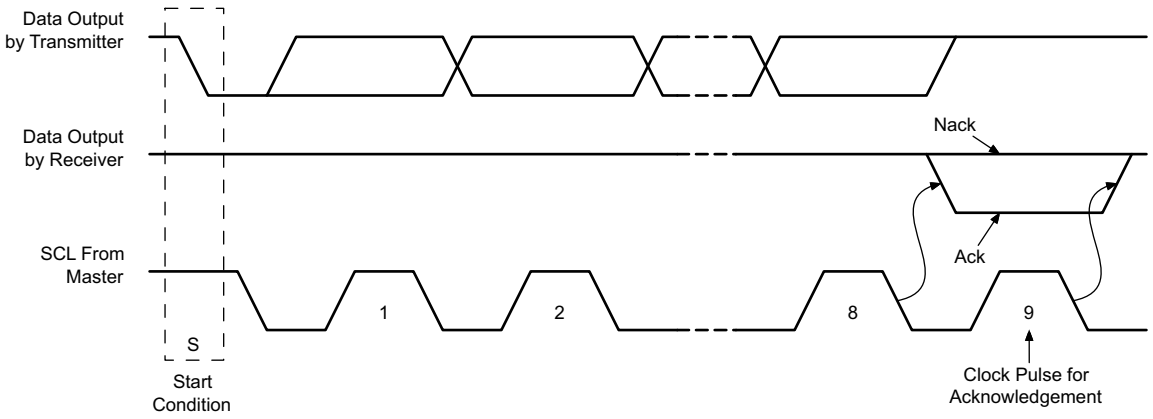


Figure 8-24. I²C Acknowledgment

8.3.10.2 I²C Clock Stretching

The TPS65994AE features clock stretching for the I²C protocol. The TPS65994AE slave I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

8.3.10.3 I²C Address Setting

The host should only use I2C_EC_SCL/SDA for loading a patch bundle. Once the boot process is complete, each port has a unique slave address on the I2C_EC_SCL/SDA bus as selected by the ADCINx pins. The slave address used by each port on the I2C2s bus are determined from the application configuration. The Port A slave address should be used for pushing the patch bundle since the Port B slave address is not available during the BOOT mode.

Table 8-5. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)(1)	Port	Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	A	0	1	0	0	0	0	0	R/W	Yes
#1	B	0	1	0	0	1	0	0	R/W	No
#2	A	0	1	0	0	0	0	1	R/W	Yes
#2	B	0	1	0	0	1	0	1	R/W	No
#3	A	0	1	0	0	0	1	0	R/W	Yes
#3	B	0	1	0	0	1	1	0	R/W	No
#4	A	0	1	0	0	0	1	1	R/W	Yes
#4	B	0	1	0	0	1	1	1	R/W	No

(1) See Table 8-2 details about ADCIN1 and ADCIN2 decoding.

8.3.10.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS65994AE. The I²C Slave sub-address is used to receive or respond to Host Interface protocol commands. Figure 8-25 and Figure 8-26 show the write and read protocol for the I²C slave interface, and a key is included in Figure 8-27 to explain the terminology used. The TPS65994AE Host interface utilizes a different unique address to identify each of the two USB Type-C ports controlled by the TPS65994AE. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

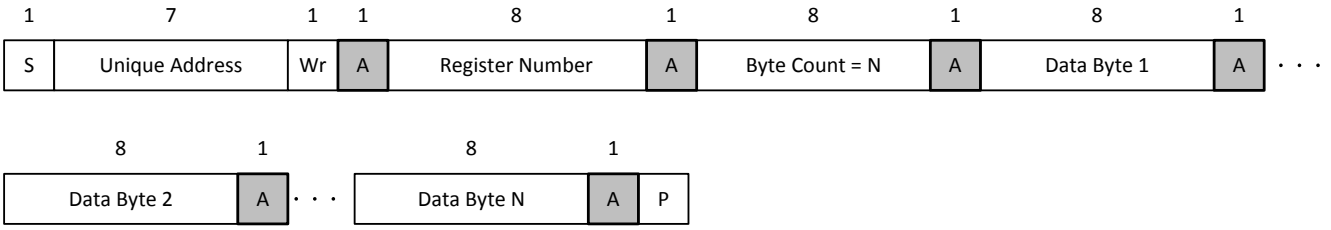


Figure 8-25. I²C Unique Address Write Register Protocol

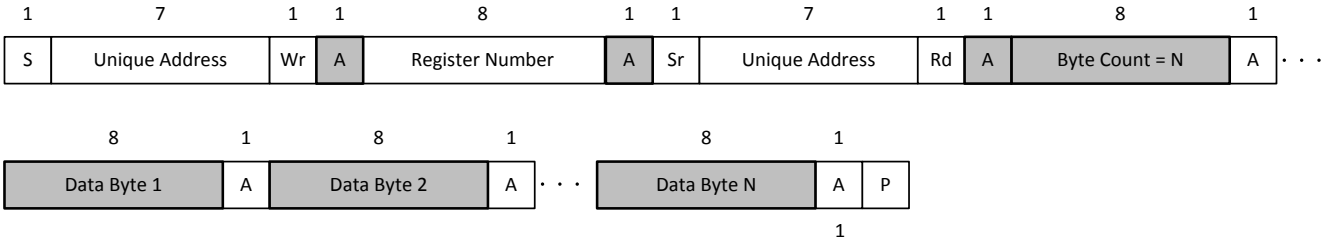


Figure 8-26. I²C Unique Address Read Register Protocol

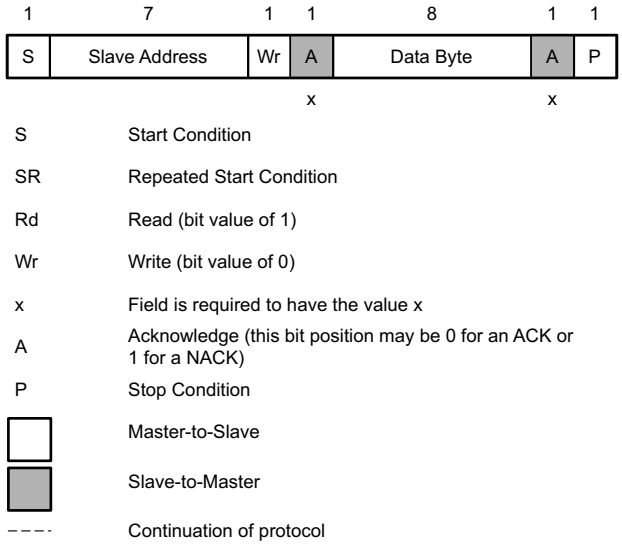


Figure 8-27. I²C Read/Write Protocol Key

8.4 Device Functional Modes

8.4.1 Pin Strapping to Configure Default Behavior

During the boot procedure, the device will read the ADCINx pins and set the configurations based on the table below. Then it will attempt to load a configuration from an external EEPROM on the I2C3m bus. If no EEPROM is detected, then the device will wait for an EC to load a configuration.

When an external EEPROM is used, each device is connected to a unique EEPROM, it cannot be shared for multiple devices. The external EEPROM shall be at 7-bit slave address 0x50.

Table 8-6. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 decoded value (2)	ADCIN2 decoded value (2)	I²C address Index (1)	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A: The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	6	#1	SinkRequires_1.5A: The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
6	5	#3	
6	7	#4	
7	3	#1	NegotiateHighVoltage: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the 'APP ' mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V. This cannot be used when a patch is loaded from EEPROM.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode: The device does not enable the sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode. This is recommended when the application loads the patch from EEPROM.
0	0	#2	
6	0	#3	
5	7	#4	

(1) See Table 8-5 to see the exact meaning of I²C Address Index.
(2) See Table 8-2 for how to configure a given ADCINx decoded value.

8.4.2 Power States

The TPS65994AE may operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in the following table. The device will automatically transition between the three power states based on the circuits that are active and required, see the following figure. In the Sleep State the TPS65994AE will detect a Type-C connection. Transitioning between the Active mode to the Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message.
- Change in CC status.
- GPIO input event.
- I²C transactions.
- Voltage alert.
- Fault alert.

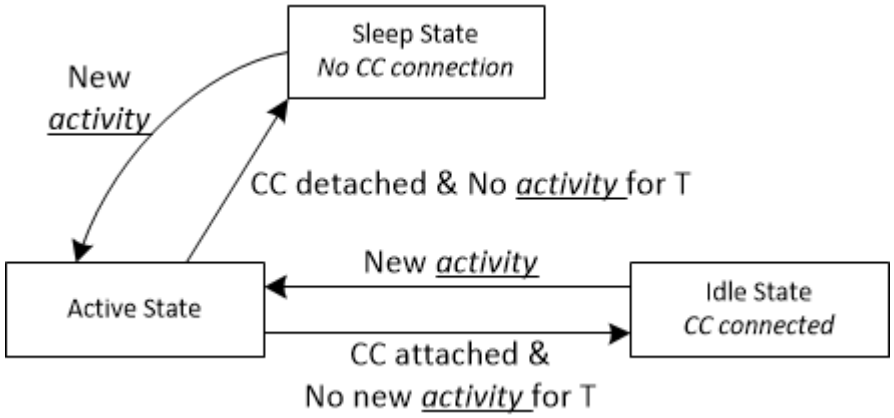


Figure 8-28. Flow Diagram For Power States

Table 8-7. Power Consumption States

	Active Source Mode(1)	Active Sink Mode(6)	Idle Source Mode(2)	Idle Sink Mode(7)	Modern Standby Source Mode(4)	Modern Standby Sink Mode(5)	Sleep Mode(3)
PP_5V1	enabled	disabled	enabled	disabled	enabled	disabled	disabled
PP_5V2	enabled	disabled	enabled	disabled	disabled	disabled	disabled
PP_EXT 1	disabled	enabled	disabled	enabled	disabled	disabled	disabled
PP_EXT2	disabled	enabled	disabled	enabled	disabled	disabled	disabled
PP_CABLE1	enabled	enabled	enabled	enabled	disabled	disabled	disabled
PP_CABLE2	enabled	enabled	enabled	enabled	disabled	disabled	disabled
external PA_CC1 termination	Rd	Rp 3.0A	Rd	Rp 3.0A	Rd	Rp 3.0A	open
external PA_CC2 termination	open	open	open	open	open	open	open
external PB_CC1 termination	Rd	Rp 3.0A	Rd	Rp 3.0A	open	open	open
external PB_CC2 termination	open	open	open	open	open	open	open

(1) This mode is used for: $I_{VIN\_3V3,ActSrc}$.
(2) This mode is used for: $I_{VIN\_3V3,IdlSrc}$
(3) This mode is used for: $I_{VIN\_3V3,Sleep}$
(4) This mode is used for: $P_{MstbySrc}$
(5) This mode is used for: $P_{MstbySnk}$
(6) This mode is used for: $I_{VIN\_3V3,ActSnk}$
(7) This mode is used for: $I_{VIN\_3V3,IdlSnk}$

8.4.3 Thermal Shutdown

The TPS65994AE features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD_MAIN}. The temperature shutdown has a hysteresis of T_{SDH_MAIN} and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal PP5V-to-VBUS power path and disables both power paths and the VCONN power path when either exceeds T_{SD_PP5V}. Once the temperature falls by at least T_{SDH_PP5V} the path can be configured to resume operation or remain disabled until re-enabled by firmware.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS65994AE firmware implements a host interface over I2C to allow for the configuration and control of all device options.Initial device configuration is configured through a configuration bundle loaded on to the device during boot.The bundle may be loaded through the I2C_EC port or it may be loaded over I2C3m from an external EEPROM.The TPS65994AE configuration bundle and host interface allow the device to be customized for each specific application. The configuration bundle can be generated through the Application Customization Tool.

9.2 Typical Application

9.2.1 Type-C VBUS Design Considerations

USB Type-C and PD allows for voltages up to 20 V with currents up to 5 A. This introduces power levels that could damage components touching or hanging off of VBUS. Under normal conditions, all high power PD contracts should start at 5 V and then transition to a higher voltage. However, there are some devices that are not compliant to the USB Type-C and Power Delivery standards and could have 20 V on VBUS. This could cause a 20-V hot plug that can ring above 30 V. Adequate design considerations are recommended below for these non-compliant devices.

9.2.1.1 Design Requirements

Table 9-1 shows VBUS conditions that can be introduced to a USB Type-C and PD Sink. The system should be able to handle these conditions to ensure that the system is protected from non-compliant and/or damaged USB PD sources. A USB Sink should be able to protect from the following conditions being applied to its VBUS. The *Section 9.2.1.2* section explains how to protect from these conditions.

Table 9-1. VBUS Conditions

CONDITION	VOLTAGE APPLIED
Abnormal VBUS Hot Plug	4 V - 21.5 V
VBUS Transient Spikes	4 V - 43 V

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Type-C Connector VBUS Capacitors

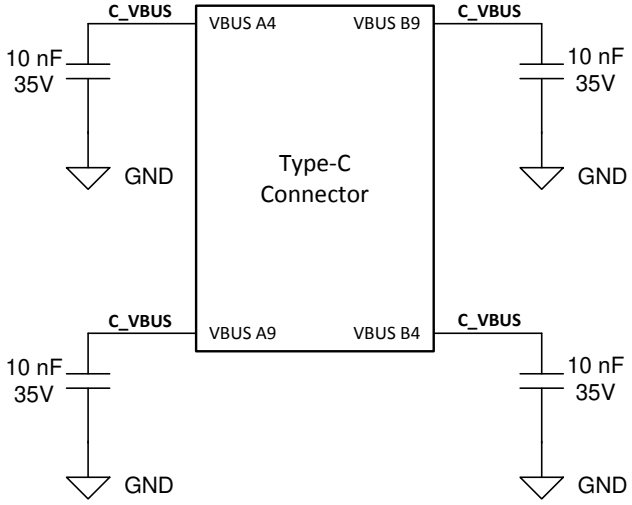


Figure 9-1. Type-C Connector VBUS Capacitors

The first level of protection starts at the Type-C connector and the VBUS pin capacitors. These capacitors help filter out high frequency noise but can also help absorb short voltage transients. Each VBUS pin should have a 10-nF capacitor rated at or above 25 V and placed as close to the pin as possible. The GND pin on the capacitors should have very short path to GND on the connector. The derating factor of ceramic capacitors should be taken into account as they can lose more than 50% of their effective capacitance when biased. Adding the VBUS capacitors can help reduce voltage spikes by 2 V to 3 V.

9.2.1.2.2 VBUS Schottky and TVS Diodes

Schottky diodes are used on VBUS to help absorb large GND currents when a Type-C cable is removed while drawing high current. The inductance in the cable will continue to draw current on VBUS until the energy stored is dissipated. Higher currents could cause the body diodes on IC devices connected to VBUS to conduct. When the current is high enough it could damage the body diodes of IC devices. Ideally, a VBUS Schottky diode should have a lower forward voltage so it can turn on before any other body diodes on other IC devices. Schottky diodes on VBUS also help during hard shorts to GND which can occur with a faulty Type-C cable or damaged Type-C PD device. VBUS could ring below GND which could damage devices hanging off of VBUS. The Schottky diode will start to conduct once VBUS goes below the forward voltage. When the TPS65994AE is the only device connected to VBUS, place the Schottky Diode close to the VBUS pin of the TPS65994AE. The two figures below show a short condition with and without a Schottky diode on VBUS. In Figure 9-3 the test is with TVS2200 but without Schottky diode and in Figure 9-4 is with both TVS2200 and the Schottky diode. As the graphs are almost identical and the voltage ring below ground are within 300mV of one another, a TVS diode such as the TVS2200 can be used in lieu of a Schottky diode.

TVS Diodes help suppress and clamp transient voltages. Most TVS diodes can fully clamp around 10 ns and can keep the VBUS at their clamping voltage for a period of time. Looking at the clamping voltage of TVS diodes after they settle during a transient will help decide which TVS diode to use. The peak power rating of a TVS diode must be able to handle the worst case conditions in the system. A TVS diode can also act as a “pseudo schottky diode” as they will also start to conduct when VBUS goes below GND.

9.2.1.2.3 VBUS Snubber Circuit

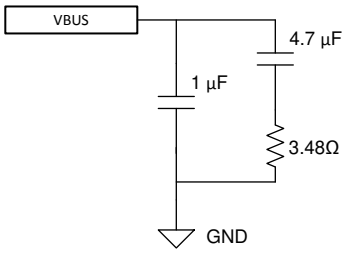


Figure 9-2. VBUS Snubber

Another method of clamping the USB Type-C VBUS is to use a VBUS RC Snubber. An RC Snubber is a great solution because in general it is much smaller than a TVS diode, and typically more cost effective as well. An RC Snubber works by modifying the characteristic of the total RLC response in the USB Type-C cable hot-plug from being under-damped to critically-damped or over-damped. So rather than clamping the over-voltage directly, it changes the hot-plug response from under-damped to critically-damped, so the voltage on VBUS does not ring at all; so the voltage is limited, but without requiring a clamping element like a TVS diode.

However, the USB Type-C and Power Delivery specifications limit the range of capacitance that can be used on VBUS for the RC snubber. VBUS capacitance must have a minimum 1 µF and a maximum of 10 µF. The RC snubber values chosen support up to 4 m USB Type-C cable (maximum length allowed in the USB Type-C specification) being hot plugged, is to use 4.7-µF capacitor in series with a 3.48-Ω resistor. In parallel with the RC Snubber a 1µF capacitor is used, which always ensures the minimum USB Type-C VBUS capacitance specification is met. This circuit can be seen in Figure 9-2.

9.2.1.3 Application Curves

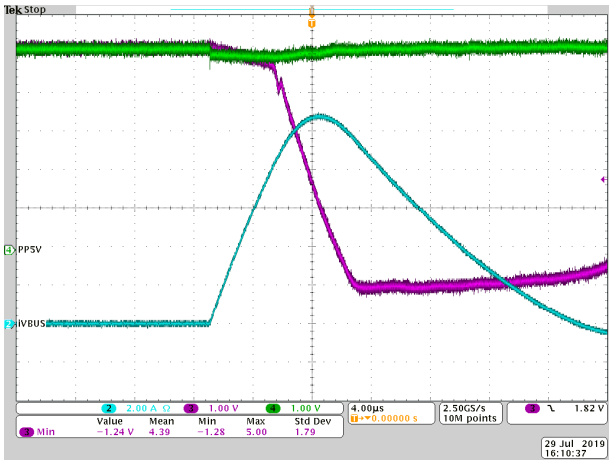


Figure 9-3. Px_VBUS Short with TVS2200, but Without Schottky Diode

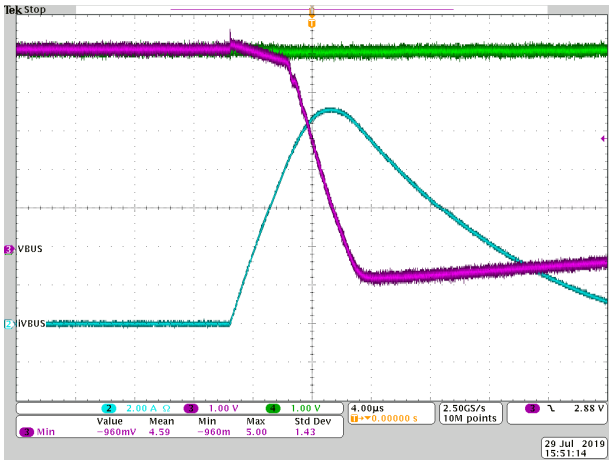


Figure 9-4. Px_VBUS Short with TVS2200 and Schottky Diode

9.2.2 Notebook Design Supporting PD Charging

The TPS65994AE works very well in single port Notebooks that support PD charging. The internal power path for the TPS65994AE source System 5 V from PP5V to the VBUS pins. Additionally, the TPS65994AE can control an external Common Drain N-FET power path to sink power into the system. The TPS65994AE offers full reverse-current protection on the external power path through the N-FET gate driver. The System 5-V connected to PP5V on the TPS65994AE also supplies power to VCONN of Type-C e-marked cables and Type-C accessories. An embedded controller EC is used for additional control of the TPS65994AE and to relay information back to the operating system. An embedded controller enables features such as entering and exiting sleep modes, changing source and sink capabilities depending on the state of the battery, UCSI support, control alternate modes, and so forth.

9.2.2.1 USB and DisplayPort notebook Supporting PD Charging

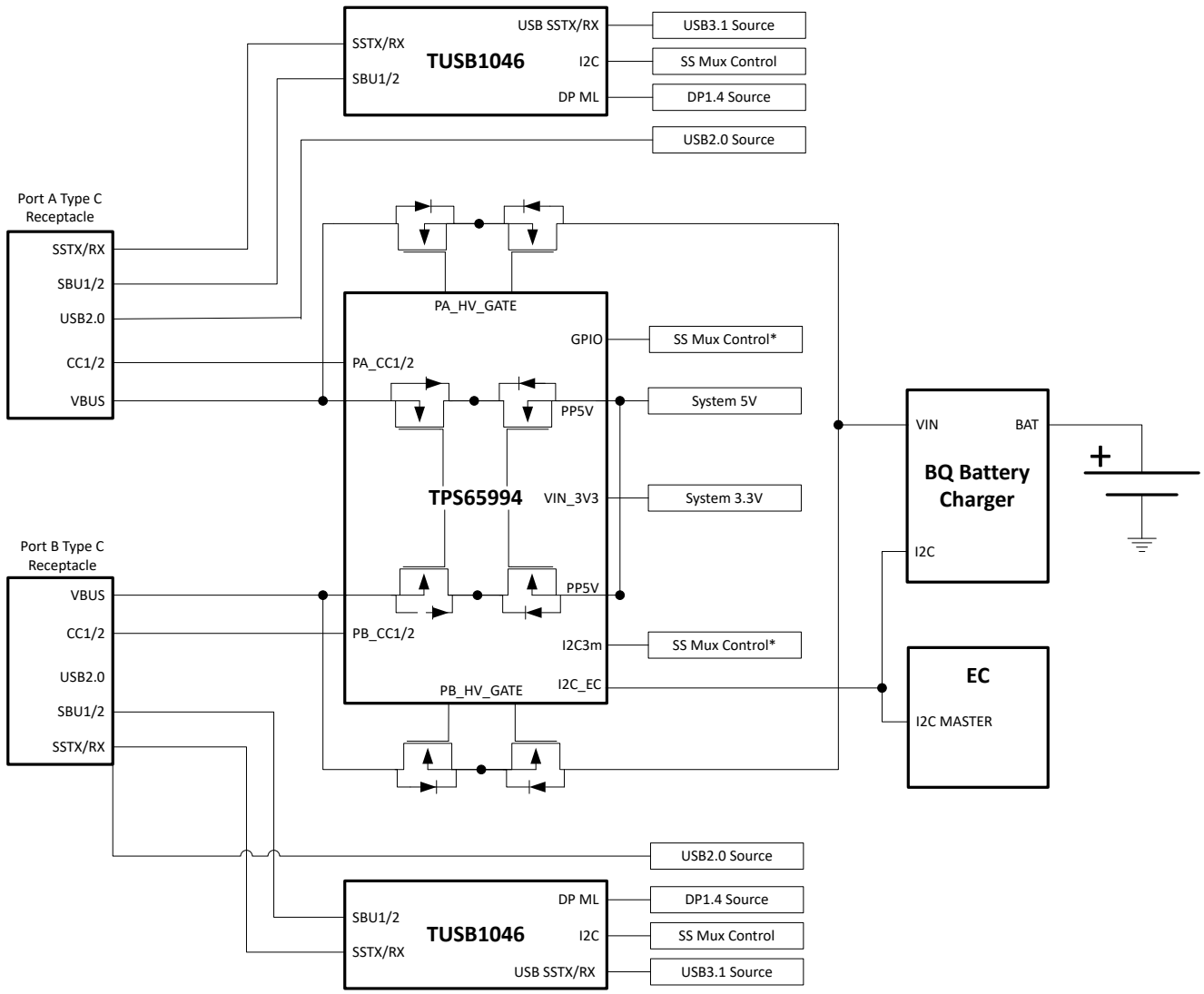


Figure 9-5. USB and DisplayPort Architecture

9.2.2.1.1 Design Requirements

Table 9-2 summarizes the Power Design parameters for an USB Type-C PD Notebook.

Table 9-2. Power Design Parameters

POWER DESIGN PARAMETERS	VALUE	CURRENT PATH
PP5V Input Voltage, Current	5 V, 2 A	VBUS Source & VCONN Source
NFET PP_EXT Voltage, Current	5 V – 20 V, 3 A **(5 A Max)**	VBUS Sink
VIN_3V3 Voltage, Current	3.3 V, 50 mA	Internal TPS65994AE Circuitry

9.2.2.1.2 Detailed Design Procedure

9.2.2.1.2.1 USB Power Delivery Source Capabilities

Most Type-C dongles (video and data) draw less than 900 mA and supplying 1.5 A on each Type-C port is sufficient for a notebook supporting USB and DisplayPort. Table 9-3 shows the PDO for the Type-C port.

Table 9-3. Source PDOs

SOURCE PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	1.5 A

9.2.2.1.2.2 USB Power Delivery Sink Capabilities

Most notebooks support buck/boost charging which allows them to charge the battery from 5 V to 20 V. USB PD sources must also follow the Source Power Rules defined by the USB Power Delivery specification. It is recommended for notebooks to support all the voltages in the Source Power Rules to ensure compatibility with most PD chargers/adapters.

Table 9-4. Sink PDOs

SINK PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	3 A
PDO2	Fixed	9 V	3 A
PDO3	Fixed	15 V	3 A
PDO4	Fixed	20 V	3 A **(5 A Max)**

9.2.2.1.2.3 USB and DisplayPort Supported Data Modes

Table 9-5 summarizes the data capabilities of the notebook supporting USB3 and DisplayPort.

Table 9-5. Data Capabilities

PROTOCOL	DATA	DATA ROLE
USB Data	USB3.1 Gen2	Host
DisplayPort	DP1.4	Host DFP_D (Pin Assignment C, D, and E)

9.2.2.1.2.4 TUSB1046 Super Speed Mux GPIO Control

The TUSB1046 requires GPIO control in GPIO control mode to determine whether if there is USB or DisplayPort data connection. Table 9-6 summarizes the TPS65994AE GPIO Events and the control pins for the TUSB1046. Note that the pin strapping on the TUSB1046 will set the GPIO control mode and the required equalizer settings. For more details refer to the TUSB1046 datasheet.

Table 9-6. GPIO Events for Super Speed Mux

TPS65994AE GPIO EVENT	TUSB1046 CONTROL
Cable_Orientation_Event_Port1	FLIP
USB3_Event_Port1	CTL0
DP_Mode_Selection_Event_Port1	CTL1

9.2.2.2 Thunderbolt Notebook Supporting PD Charging

A Thunderbolt system is capable of sourcing USB, DisplayPort, and Thunderbolt data. There is an I^2C connection between the TPS65994AE and the Thunderbolt controller. The TPS65994AE will determine the connection on the Type-C port and will generate an interrupt to the Thunderbolt controller to generate the appropriate data output. An external mux for SBU may be needed to mux the LSTX/RX and AUX_P/N signal from the Thunderbolt controller to the Type-C Connector. The TPD6S300 provides additional protection such as short to VBUS on the CC and SBU pins and ESD for the USB2 DN/P. See Figure 9-6 for a block diagram of the system.

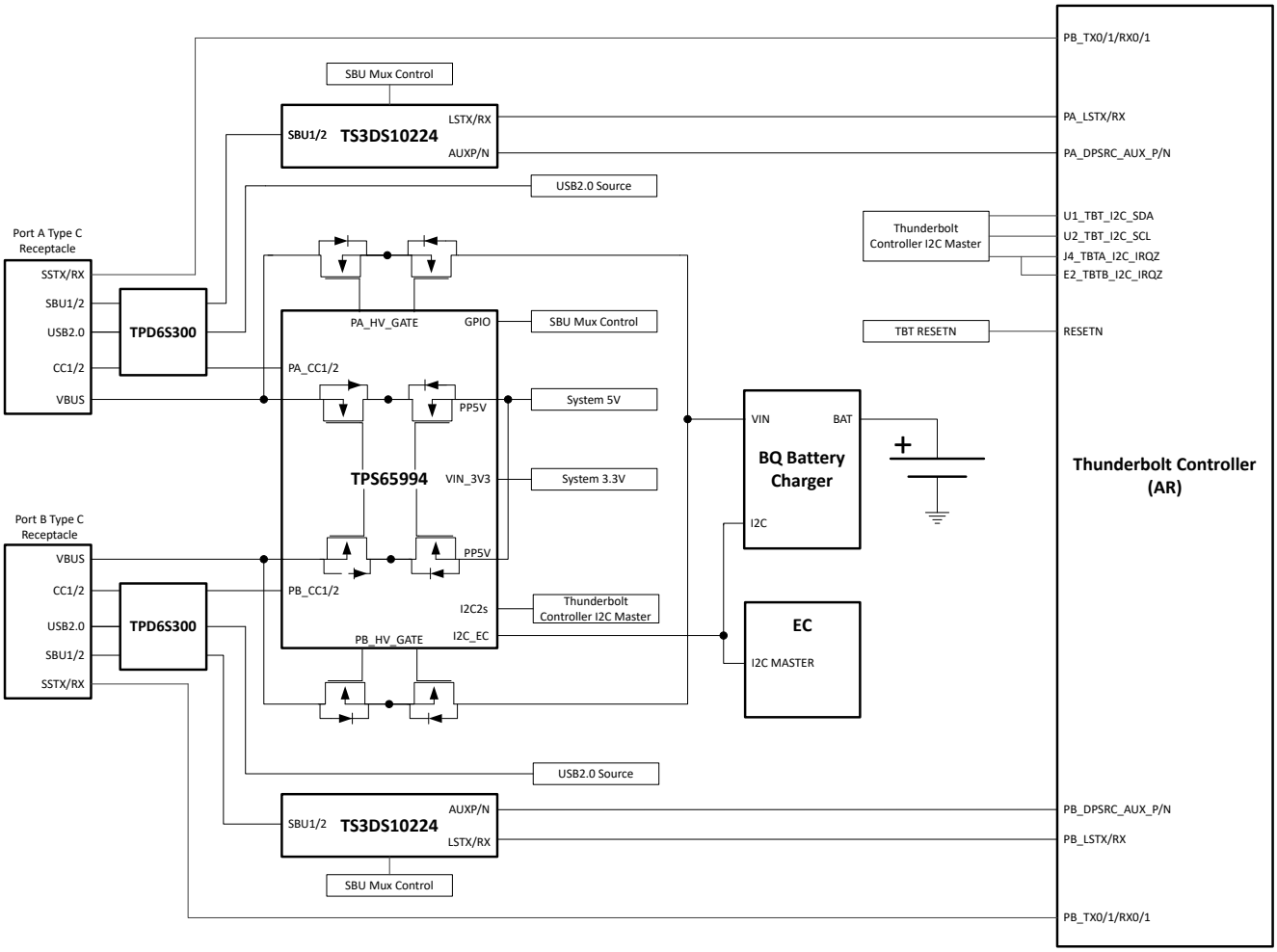


Figure 9-6. Thunderbolt Architecture

9.2.2.2.1 Design Requirements

Table 9-7 summarizes the Power Design parameters for an USB Type-C PD Thunderbolt Notebook.

Table 9-7. Power Design Parameters

POWER DESIGN PARAMETERS	VALUE	CURRENT PATH
PP5V Input Voltage, Current	5 V, 3.5 A	VBUS Source & VCONN Source
NFET PP_EXT Voltage, Current	5 V – 20 V, 3 A **(5 A Max)**	VBUS Sink
VIN_3V3 Voltage, Current	3.3 V, 50 mA	Internal TPS65994AE Circuitry

9.2.2.2.2 Detailed Design Procedure

9.2.2.2.2.1 USB Power Delivery Source Capabilities

All Type-C Ports that support Thunderbolt must support sourcing 5 V at 3 A (15 W). See the Table 9-8 for the PDO information.

Table 9-8. Source PDOs

SOURCE PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	3 A

9.2.2.2.2 USB Power Delivery Sink Capabilities

Most notebooks support buck/boost charging which allows them to charge the battery from 5 V to 20 V. USB PD sources must also follow the Source Power Rules defined by the USB Power Delivery specification. It is recommended for notebooks to support all the voltages in the Source Power Rules to ensure compatibility with most PD chargers/adapters.

Table 9-9. Sink PDOs

SINK PDO	PDO TYPE	VOLTAGE	CURRENT
PDO1	Fixed	5 V	3 A
PDO2	Fixed	9 V	3 A
PDO3	Fixed	15 V	3 A
PDO4	Fixed	20 V	3 A **(5 A Max)**

9.2.2.2.3 Thunderbolt Supported Data Modes

Thunderbolt Controllers are capable of generating USB3, DisplayPort and Thunderbolt Data. The Thunderbolt controller is also capable of muxing the appropriate super speed signal to the Type-C connector. Thunderbolt systems do not need a super speed mux for the Type-C connector. Table 9-10 summarizes the data capabilities of each Type-C port supporting Thunderbolt.

Table 9-10. Data Capabilities

PROTOCOL	DATA	DATA ROLE
USB Data	USB3.1 Gen2	Host
DisplayPort	DP1.4	Host DFP_D (Pin Assignment C, D, and E)
Thunderbolt	PCIe/DP	Host/Device

9.2.2.2.4 I2C Design Requirements

The I^2C connection from the TPS65994AE and the Thunderbolt control allows the Thunderbolt controller to read the current data status from the TPS65994AE when there is a connection on the Type-C port. The Thunderbolt controller has an interrupt assigned for the TPS65994AE and the Thunderbolt controller will read the I^2C address corresponding to the Type-C port. The I2C2s on the TPS65994AE is always connected to the Thunderbolt controller.

9.2.2.2.5 TS3DS10224 SBU Mux for AUX and LSTX/RX

The SBU signals must be muxed from the Type-C connector to the Thunderbolt controller. The AUX for DisplayPort and LSTX/RX for Thunderbolt are connected to the TS3DS10224 and then muxed to the SBU pins. The SBU mux is controlled through GPIOs from the TPS65994AE. Table 9-11 shows the TPS65994AE GPIO events and the control signals from the TS3DS10224.

Table 9-11. GPIO Events for SBU Mux

TPS65994AE GPIO EVENT	TS3DS10224 CONTROL
Cable_Orientation_Event_Port1	SAO, SBO
DP_Mode_Selection_Event_Port1	ENA
TBT_Mode_Selection_Event_Por1	ENB
N/A	SAI tied to VCC
N/A	SBI tied to GND

Table 9-12 shows the connections for the AUX, LSTXRX, and SBU pins for the TS3DS10224.

Table 9-12. TS3DS10224 Pin Connections

TS3DS10224 PIN	SIGNAL
INA+	SBU1
INA-	SBU2

Table 9-12. TS3DS10224 Pin Connections (continued)

TS3DS10224 PIN	SIGNAL
OUTB0+	LSTX
OUTB0-	LSRX
OUTB1+	LSRX
OUTB1-	LSTX
OUTA0+	AUX_P
OUTA0-	AUX_N
OUTA1+	AUX_N
OUTA1-	AUX_P

10 Power Supply Recommendations

10.1 3.3-V Power

10.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply of the TPS65994AE device. The VIN_3V3 switch (see *Power Management*) is a uni-directional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when the 3.3 V supply is available. The recommended capacitance C_{VIN_3V3} (see the Recommended Capacitance in the *Specifications* section) should be connected from the VIN_3V3 pin to the GND pin).

10.1.2 VBUS 3.3-V LDO

The 3.3 V LDO from Px_VBUS to LDO_3V3 steps down voltage from the PA_VBUS pin to LDO_3V3 which allows the TPS65994AE device to be powered from VBUS when VIN_3V3 is unavailable. This LDO steps down any recommended voltage on the PA_VBUS pin. When VBUS reaches 20 V, which is allowable by USB PD, the internal circuitry of the TPS65994AE device operates without triggering thermal shutdown; however, a significant external load on the LDO_3V3 pin or any GPIOx pin can increase temperature enough to trigger thermal shutdown. Keep the total load on LDO_3V3 within the limits from the *Recommended Operating Conditions* in the Specifications section. Connect the recommended capacitance C_{Px_VBUS} (see *Recommended Capacitance* in the Specifications section) from the VBUS pin to the GND pin.

10.2 1.5-V Power

The internal circuitry is powered from 1.5 V. The 1.5-V LDO steps the voltage down from LDO_3V3 to 1.5 V. The 1.5-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, and memory. The 1.5-V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance C_{LDO_1V5} (see the Recommended Capacitance in the *Specifications* section) from the LDO_1V5 pin to the GND pin.

10.3 Recommended Supply Load Capacitance

The Recommended Capacitance in the *Specifications* section lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

11 Layout

11.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with board manufacturing to verify manufacturing capabilities.

11.1.1 Top TPS65994AE Placement and Bottom Component Placement and Layout

When the TPS65994AE is placed on top and its components on bottom the solution size will be at its smallest.

11.2 Layout Example

Follow the differential impedances for Super and High Speed signals defined by their specifications (DisplayPort - AUXN/P and USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will utilize all of the I/O on the TPS65994AE.

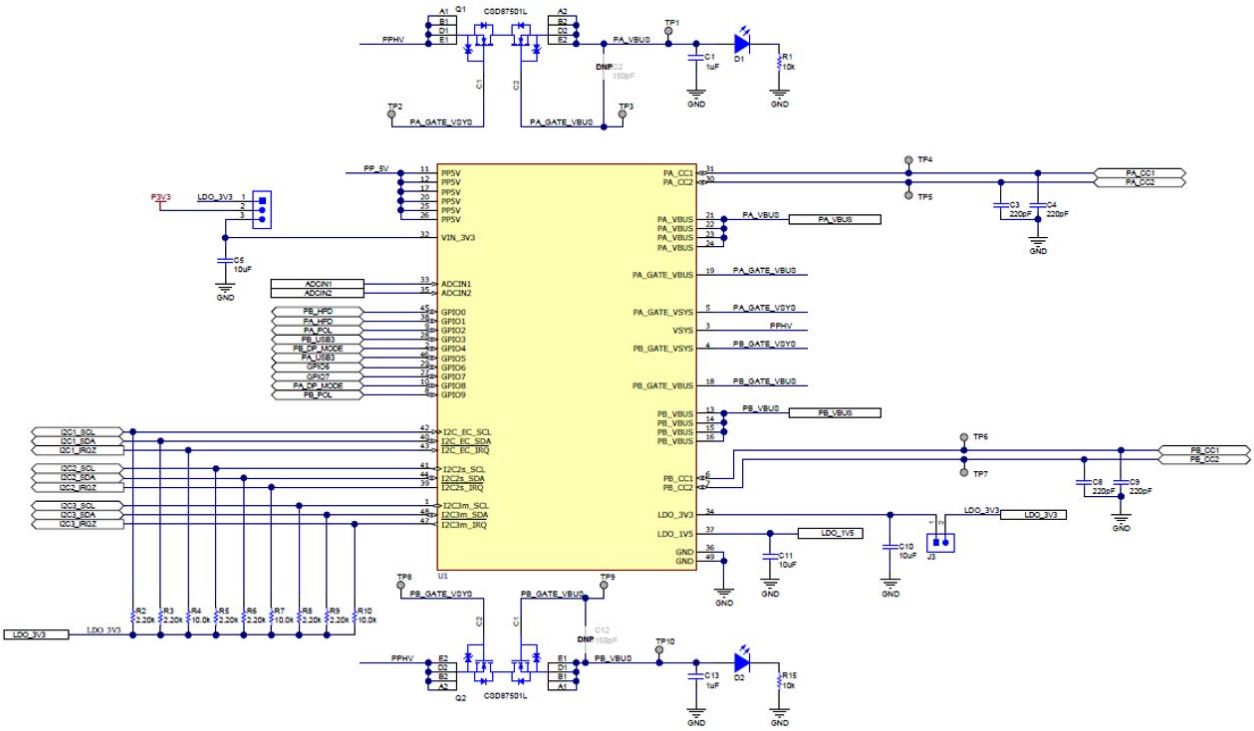


Figure 11-1. Example Schematic

11.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS65994AE is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, it is recommended that they are placed directly under the TPS65994AE. When placing the VBUS and PPHV capacitors it is easiest to place them with the GND terminal of the capacitors to face outward from the TPS65994AE or to the side since the drain connection pads on the bottom layer should not be connected to anything and left floating. All other components that are for pins on the GND pad side of the TPS65994AE should be placed where the GND terminal is underneath the GND pad.

The CC capacitors should be placed on the same side as the TPS65994AE close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

The ADCIN1/2 voltage divider resistors can be placed where convenient. In this layout example they are placed on the opposite layer of the TPS65994AE close to the LDO_3V3 pin to simplify routing.

The figures below show the placement in 2-D and 3-D.

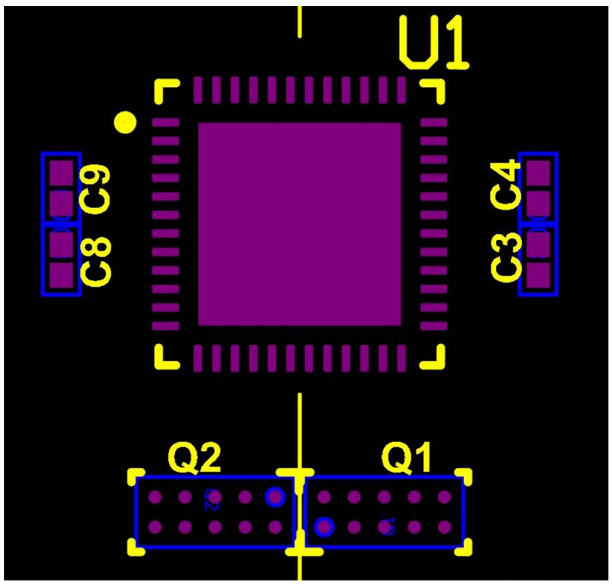


Figure 11-2. Top View Layout

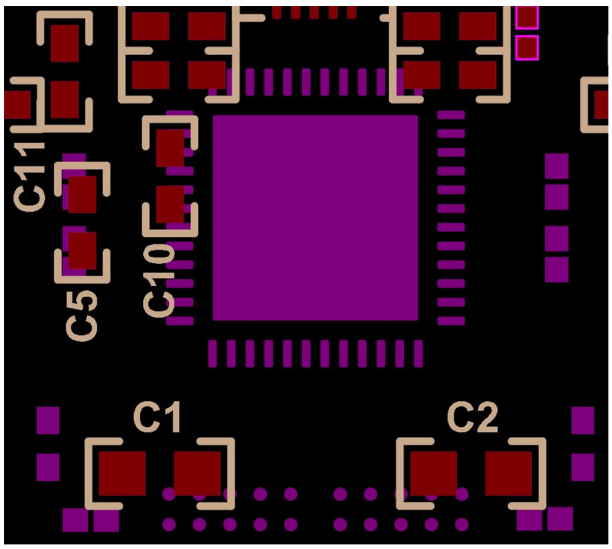


Figure 11-3. Bottom View Layout (Flipped)

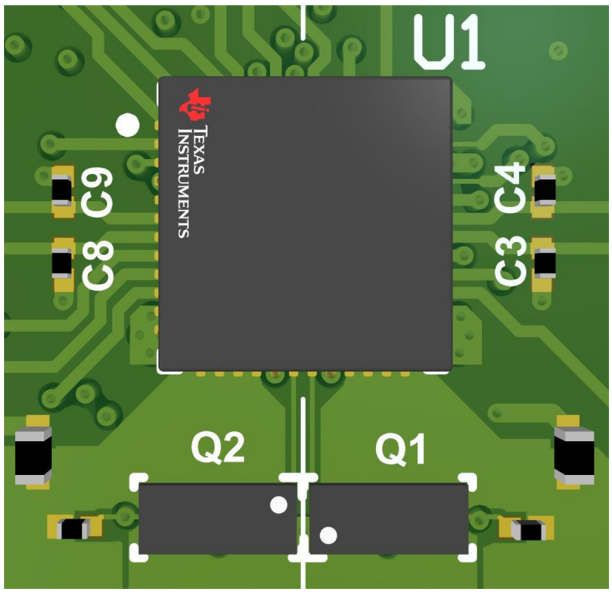


Figure 11-4. Top View 3-D

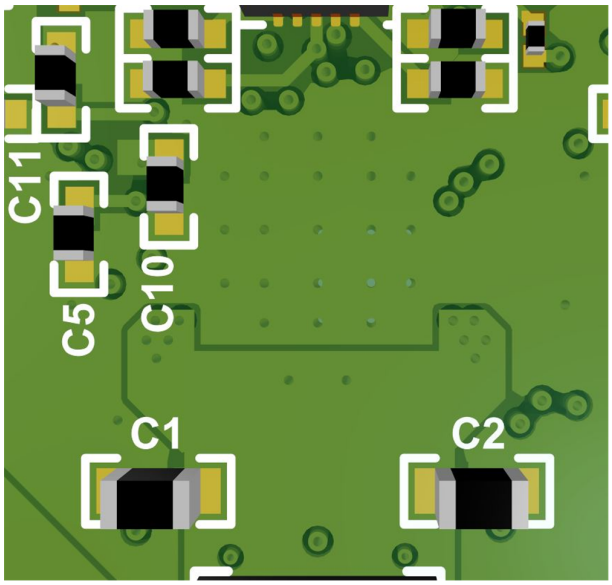


Figure 11-5. Bottom View 3-D

11.4 Routing PP_5V, VBUS, VIN_3V3, LDO_3V3, LDO_1V5

On the top side, create pours for PP_5V and VBUS1/2. Connect PP5V from the top layer to the bottom layer using at least 7 8-mil hole and 16-mil diameter vias. See Figure 11-6 and Figure 11-7 for top and bottom layer via placement and copper pours respectively.

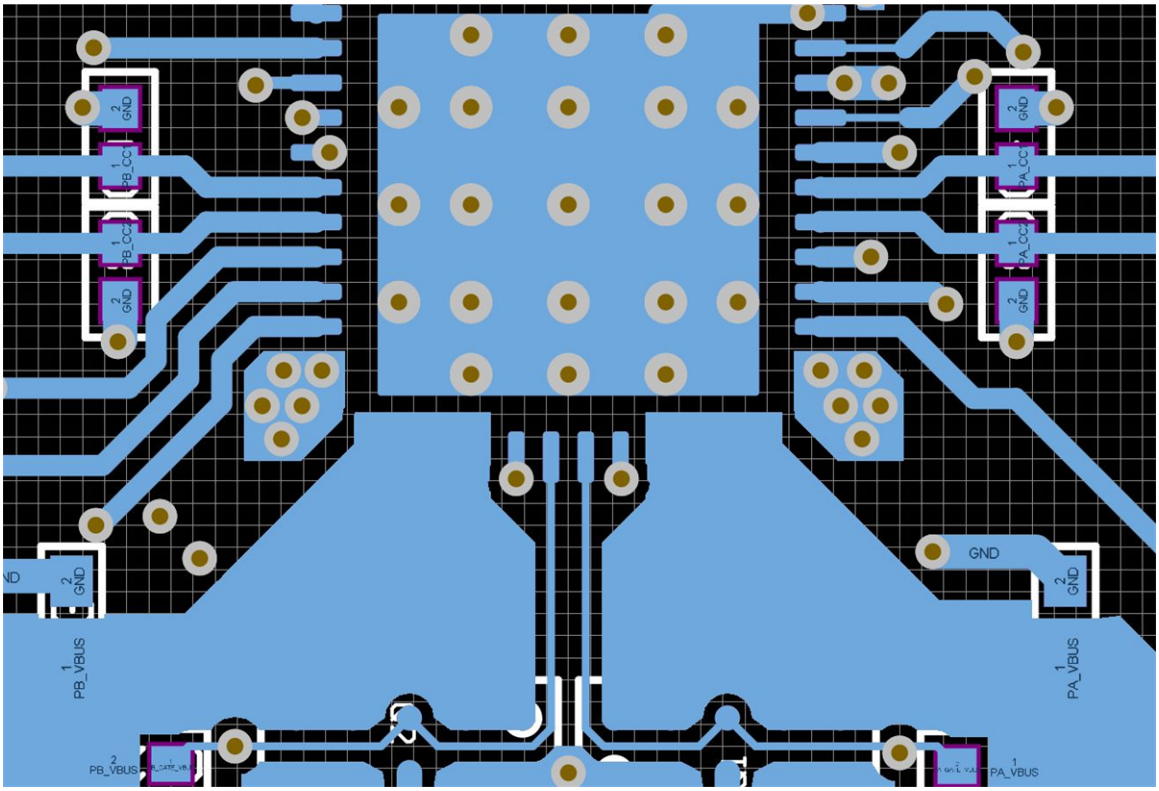


Figure 11-6. VBUS1 and VBUS2 Copper Pours and Via Placement (Top)

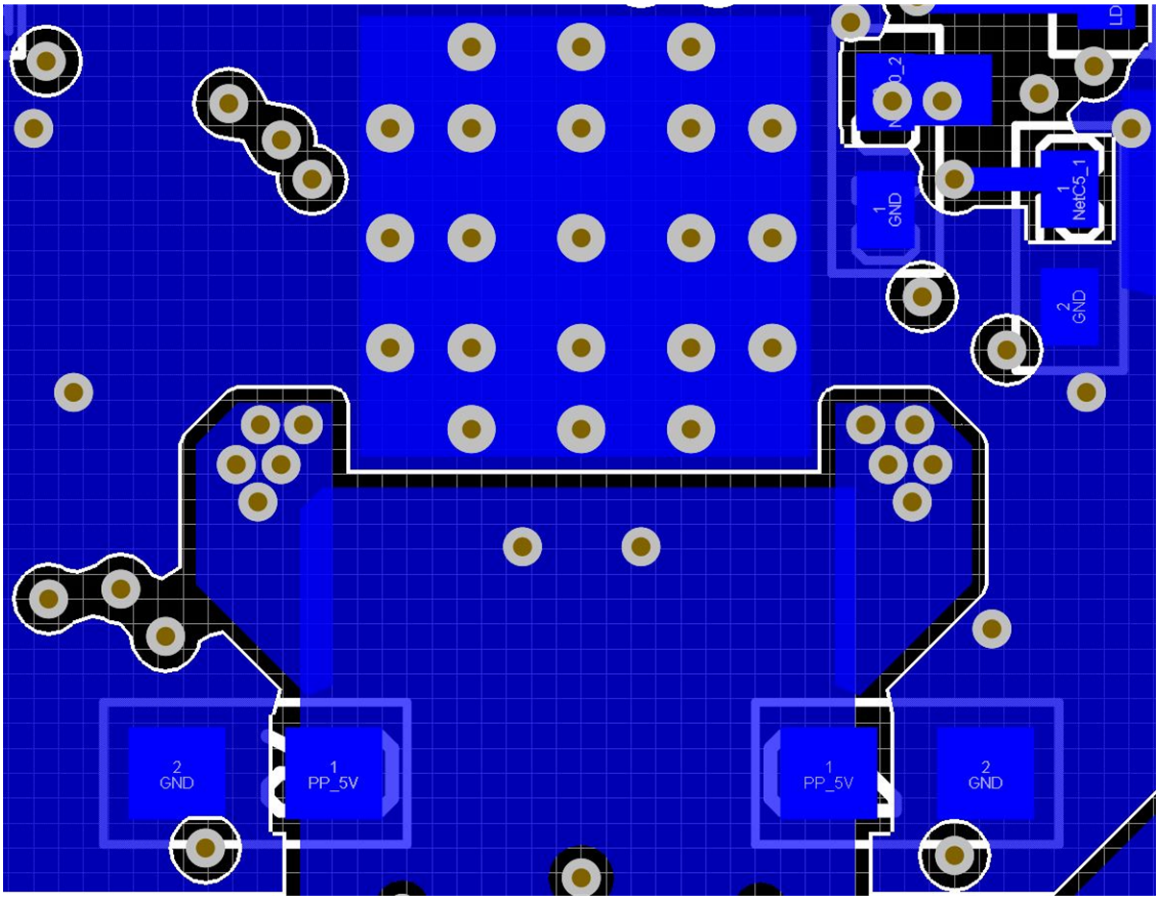


Figure 11-7. PP5V Copper Pours and Via Placement (Bottom)

Next, VIN_3V3, LDO_3V3, and LDO_1V5 will be routed to their respective decoupling capacitors. This is highlighted in Figure 8. Connect the bottom side VIN_3V3, LDO_1V5, and LDO_3V3 capacitors with traces through a via. The vias should have a straight connection to the respective pins.

As shown in Figure 11-5 (3D view) these decoupling capacitors are in the bottom layer.

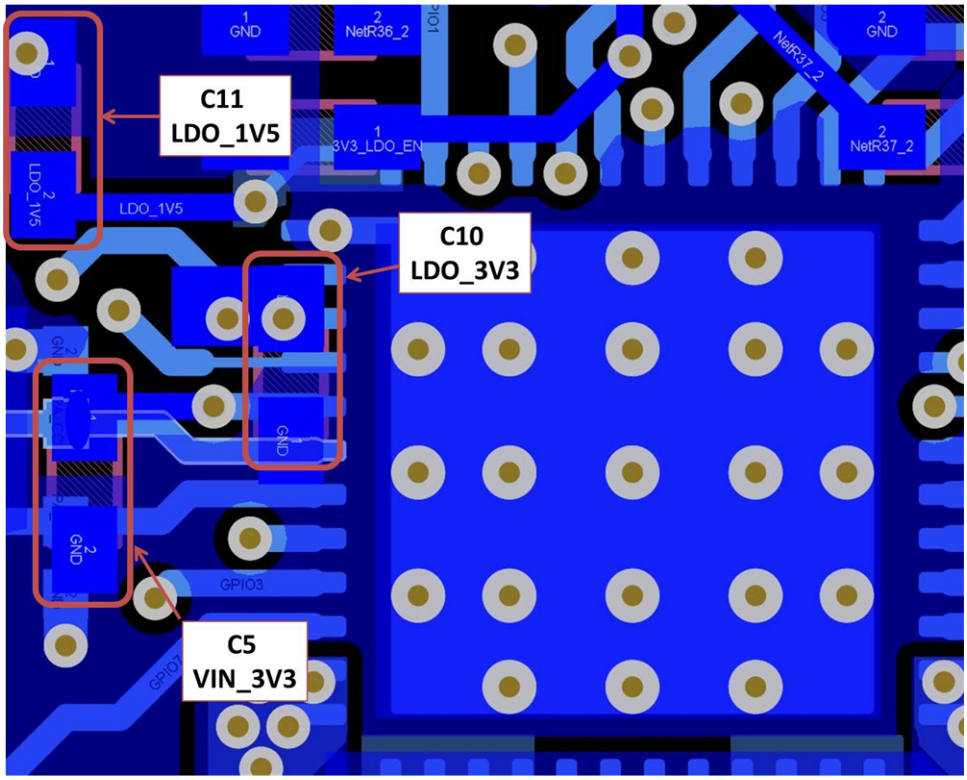


Figure 11-8. VIN_3V3, LDO_3V3, and LDO_1V5 Routing

11.5 Routing CC and GPIO

Routing the CC lines with a 10-mil trace will ensure the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top or bottom layer using either a 6-mil trace or a 8-mil trace. The following images highlight how the CC lines and GPIOs are routed out.

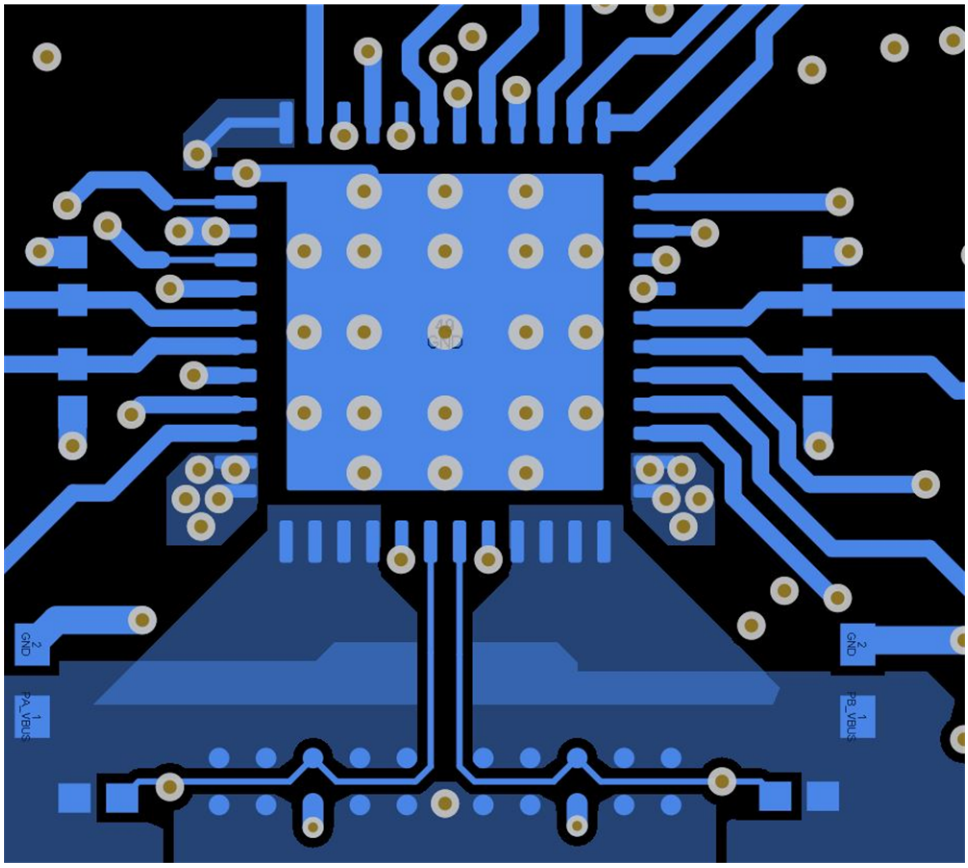


Figure 11-9. Top Layer GPIO Routing

Table 11-1. Routing Widths

ROUTE	WIDTH (mil minimum)
PA_CC1, PA_CC2, PB_CC1, PB_CC2	8
VIN_3V3, LDO_3V3, LDO_1V5	6
Component GND	10
GPIO	4

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

- *USB-PD Specifications*
- *USB Power Delivery Specification*

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65994AERSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS65994 AE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

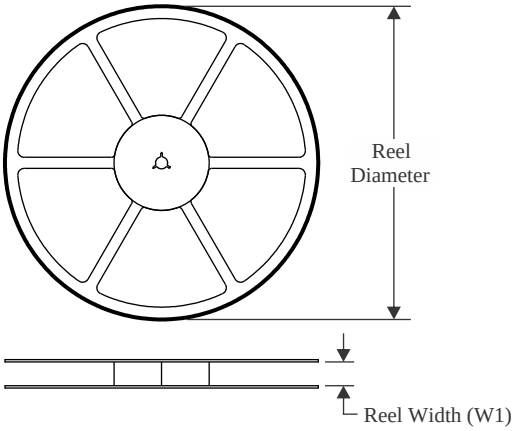
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

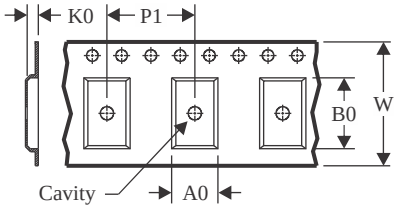
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

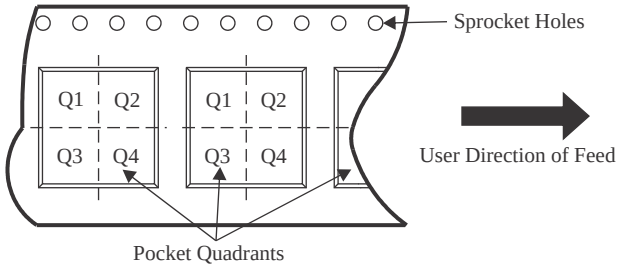


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

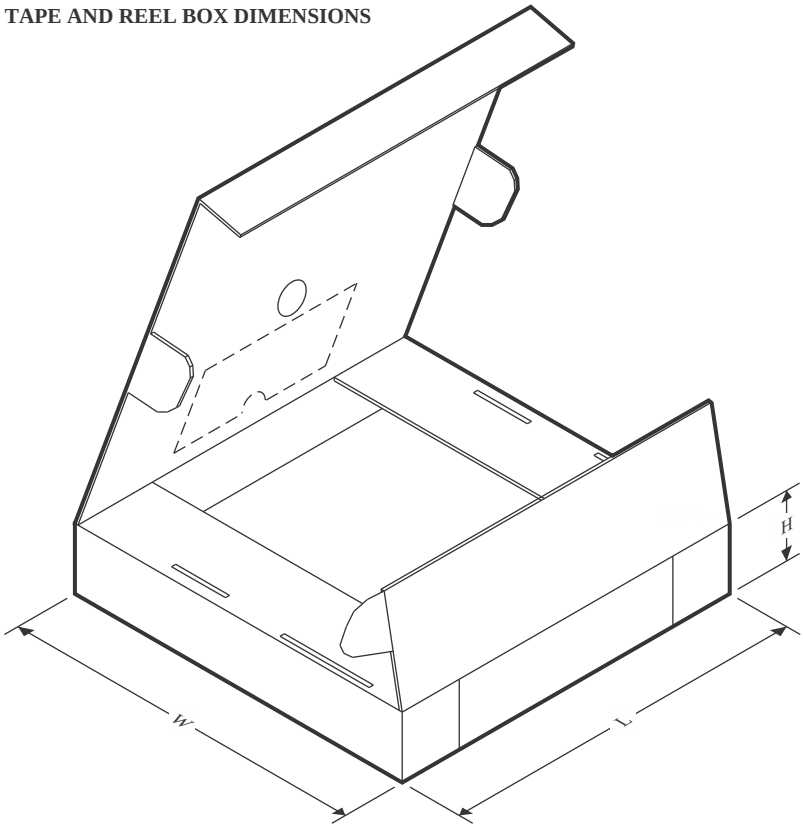
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65994AERSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65994AERSLR	VQFN	RSL	48	2500	367.0	367.0	35.0

GENERIC PACKAGE VIEW

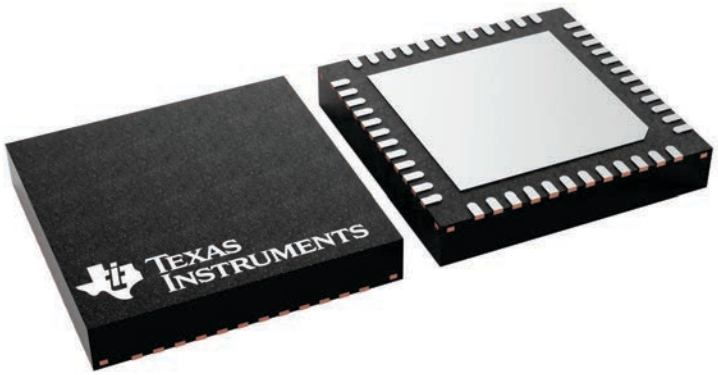
RSL 48

VQFN - 1 mm max height

6 x 6, 0.4 mm pitch

QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



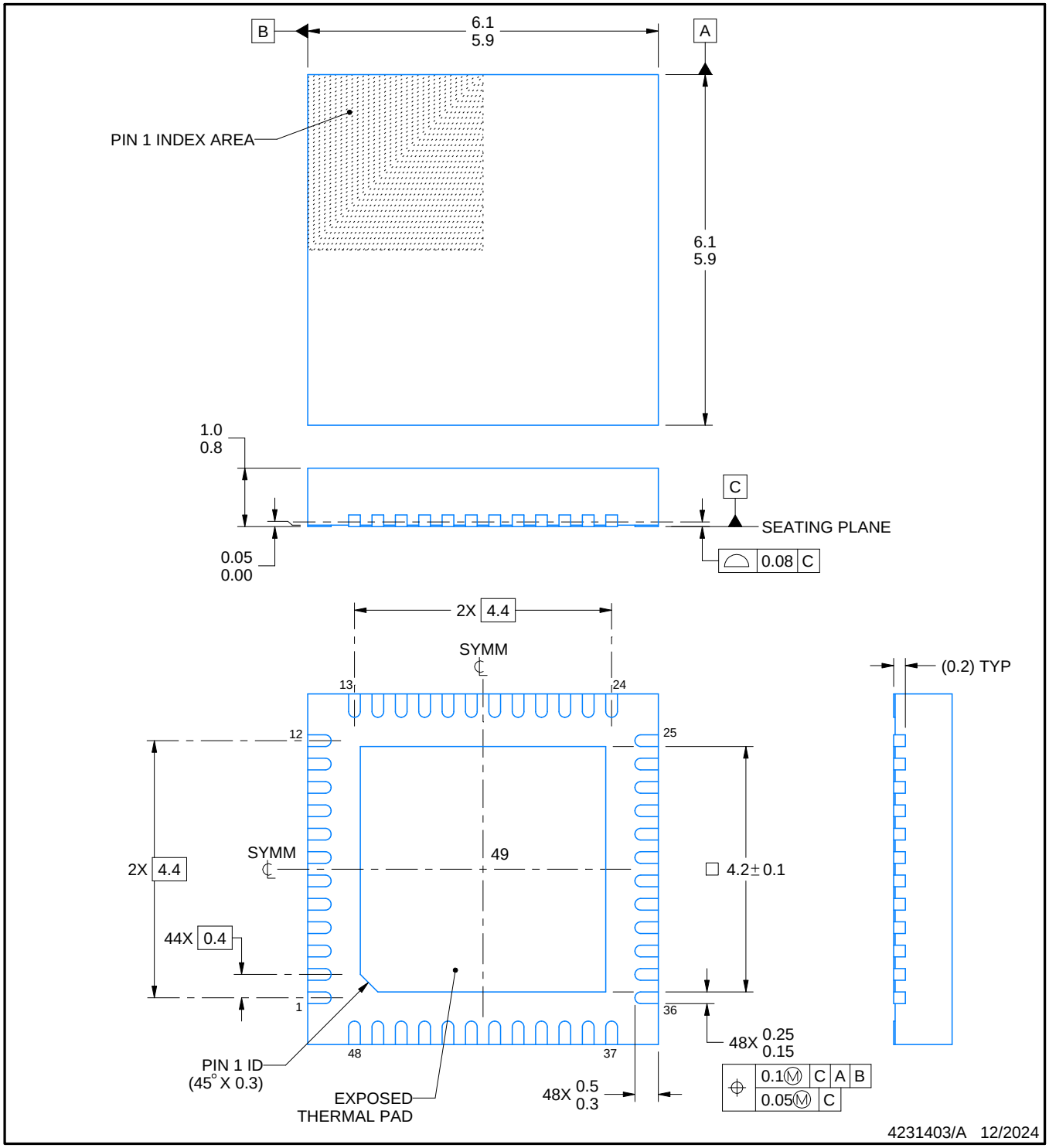
4225749/A

RSL0048G

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

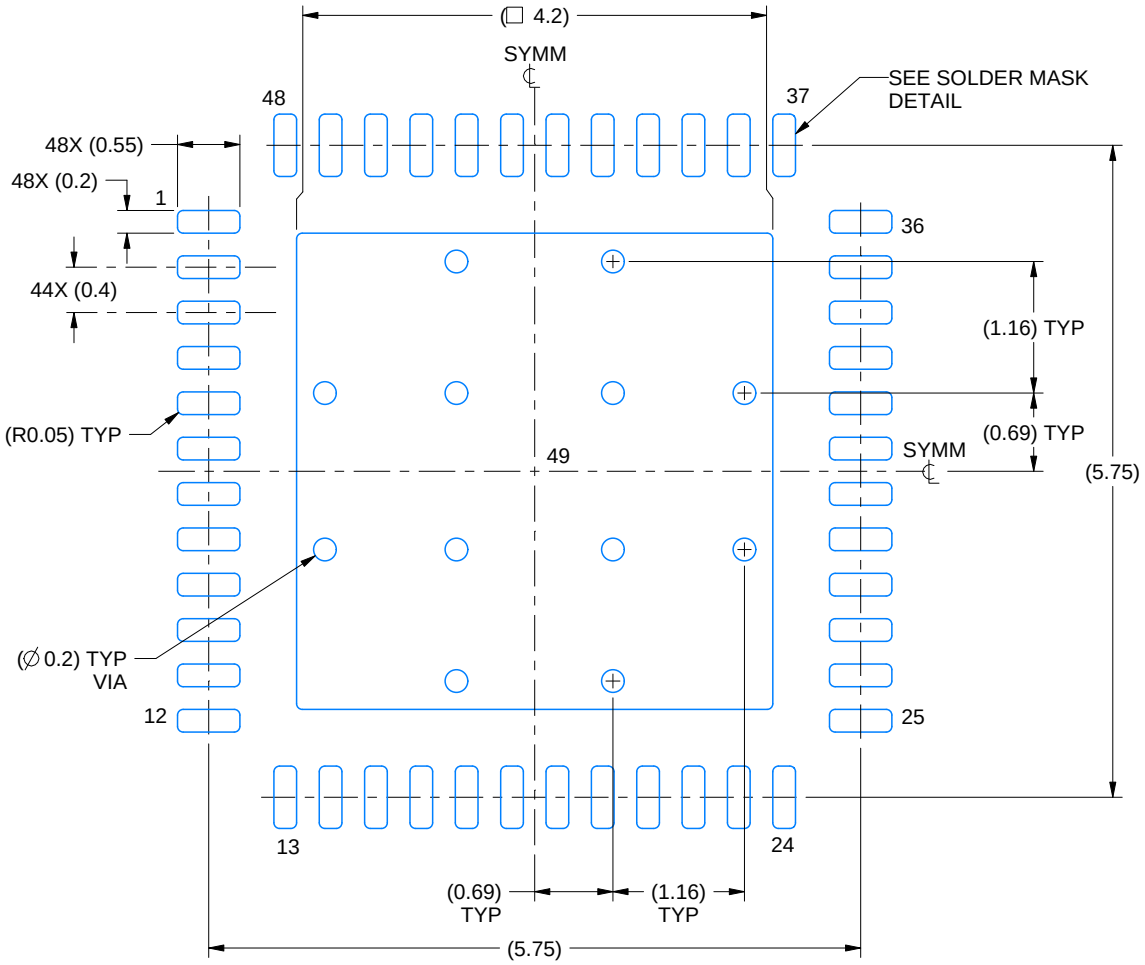
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

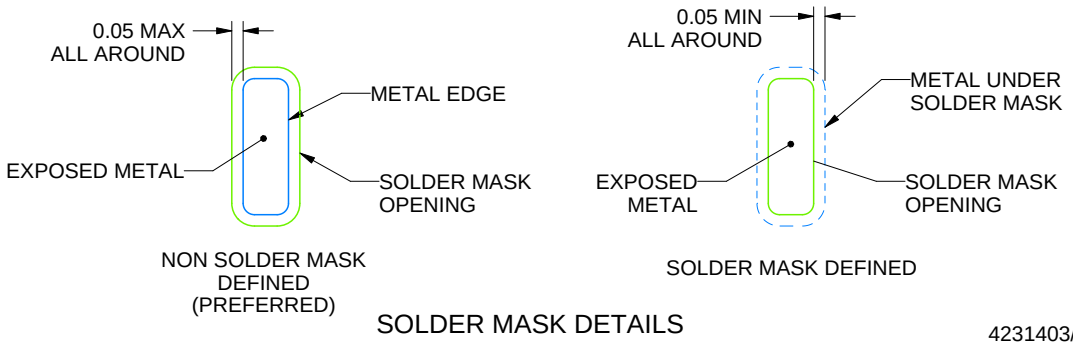
RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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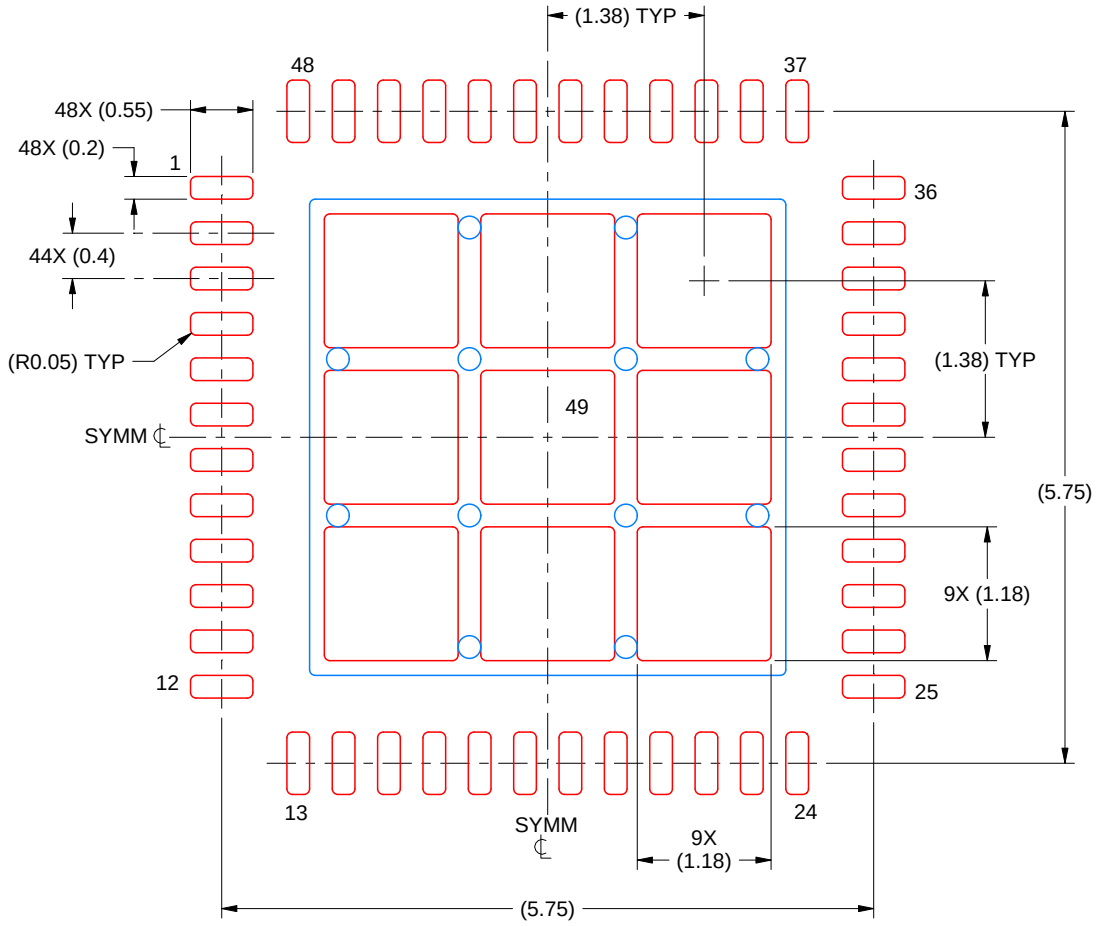
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 49
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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