Application Report
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Important Considerations to Assure a Safe POR

Herbert Braisz, Wendy Fang *Data Acquisition Products*

ABSTRACT

This application report explains specific and important considerations related to the automatic power-on reset feature of the TSC2007 touch-screen controller. It also discusses several possible issues that may arise as a result of improperly powering the device on or off, and provides application solutions to ensure proper TSC2007 operation under various power-supply conditions.

Contents

1 TSC2007 Power-On/-Off Requirements

Based on design principles and extensive tests with the TSC2007 touch-screen controller, the power to the device must meet specific on/off timing and sequence requirements in order to ensure that the Power-On Reset (POR) feature is implemented each time the device powers on. These requirements prevent the TSC2007 from entering a possible abnormal operating state, called a *lockup* in this context. One example of a lockup is that the TSC2007 does not reply with an ACK upon being called by the host.

1.1 Functions of TSC2007 POR

The POR brings the TSC2007 to a known working state (the default condition) by initializing the internal storage elements (flip-flops) and recognizing its connections (such as identifying the status of pins A1 and A0 as high or low, which is how the TSC2007 I^2C™ slave address can be decided). Without the POR feature, the TSC2007 may start up in a random state and thus may cause a lockup.

The TSC2007 POR circuit was designed so that it does not consume power during normal operation, keeping the power-down current as low as possible (see the product data sheet, Ref 1).

1.2 Specifications Related to POR

Figure 1 and Table 1 contain the recommended power-off times and ON/OFF ramp specifications (note that the supply voltage range of the device is 1.2V to 3.6V).

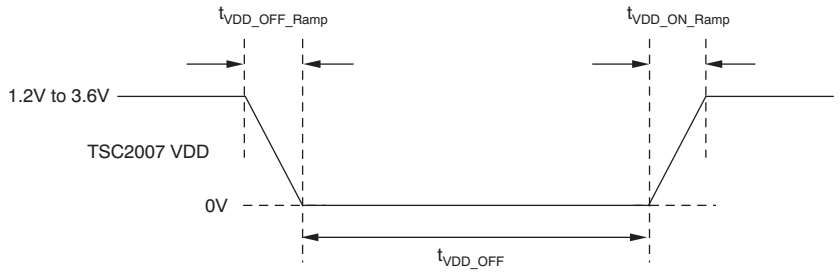

Figure 1. POR Sequence

Table 1. Required POR Timings

Temperature Range	Min $t_{VDD\_OFF\_ramp}$	Min $t_{VDD\_ON\_ramp}$	Min t_{VDD_OFF} (1)
+85°C to –20°C	2kV/sec	12kV/sec	300ms
–21°C to –40°C	12kV/sec	12kV/sec	1.2sec

(1) t_{VDD_OFF} time starts when TSC2007 VDD reaches 0V and remains at that level.

Why Request a Minimal t_{VDD_OFF} Time?

The POR circuit of the TSC2007 contains a capacitor that is charged when the device powers up, and generates an internal reset signal when the voltage at the capacitor reaches a certain level. This capacitor in the POR circuit is discharged after the TSC2007 supply switches off. The TSC2007 is designed for low-power operation; therefore, the POR takes time to charge and discharge the capacitor, especially under cold temperatures (< –20°C).

If the VDD OFF time is insufficient, the device may lock up, and only cycling the power will resolve this lockup condition.

Why Request a Minimal $t_{VDD\_OFF\_ramp}$ and $t_{VDD\_ON\_ramp}$ Ramp?

To ensure the proper initialization of the TSC2007, it is required that the device reach a certain voltage before the internal POR signal is released. If the power supply on ramp is too slow, the device may power up in a random state, and may lock up.

The internal POR capacitor must be discharged through the TSC2007 VDD pin. To support a proper discharge, it is recommended to have a specified VDD off ramp and also provide a low-resistance path on the VDD pin when the TSC2007 supply switches off.

2 Potential Issues with TSC2007 POR

Any situation that cannot ensure the power-on/-off requirements discussed in Section 1 could affect the TSC2007 POR circuit and may result in a device lockup. This section reviews some of the more common situations that may result in this problem.

2.1 Effects from TSC2007 $\overline{\text{PENIRQ}}$ Pin

The TSC2007 $\overline{\text{PENIRQ}}$ pin is a typical digital output. It must be connected to a digital input at the other end (for example, the host processor).

It is well-known that the TSC2007 has the best electrostatic discharge (ESD) protection available in today's market. Every TSC2007 pin is well-protected against both positive and negative ESD shocks. Consider the $\overline{\text{PENIRQ}}$ pin as an example: internally, there is an ESD protection diode between $\overline{\text{PENIRQ}}$ and the ground pin, and another diode between the $\overline{\text{PENIRQ}}$ and VDD pins, as shown in Figure 2.

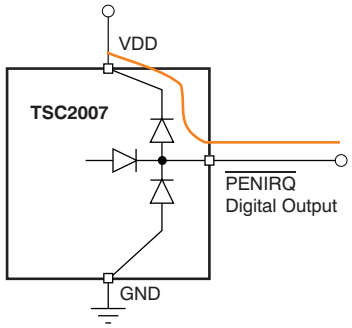

Figure 2. TSC2007 $\overline{\text{PENIRQ}}$ Pin Internal ESD Protection Diodes

If by any chance, the $\overline{\text{PENIRQ}}$ pin is pulled or driven high while the TSC2007 VDD is not applied (which should not be allowed during normal operation), the TSC2007 could be *powered up* from the $\overline{\text{PENIRQ}}$ pin through the connected internal diode between the pin and VDD. This possible situation is illustrated by the orange line in Figure 2.

Such false power-up events do not ensure the required power supply to TSC2007; the POR would not be ensured, and a lockup may occur.

2.2 Effects from TSC2007 I^2C Pins

The potential POR effects from the SCL and SDA pins were eliminated during silicon revision C of the TSC2007. In this revision, the secondary ESD protection diode from SCL (or SDA) to VDD was removed.

2.3 Effects from VDD Glitches During Normal Operation

A VDD power glitch during normal operation of the TSC2007 may cause a lockup condition. Therefore, it is important that the system be able to cycle the power in the system according to the requirements outlined in Figure 1 and Table 1.

2.4 Effects from Power Off Cycles During Normal Operation

The TSC2007 is a low-power device (see the power-down supply current specification in the product data sheet). Therefore, it is not necessary and not recommended to switch the TSC2007 device off during normal operation.

Every power cycle (power on→ power off → power on) must meet the requirements given in Figure 1 and Table 1.

3 Application Solutions

To avoid any potential lockup while the device powers up, it is essential that the VDD always meet the requirements for its on/off slope, timing, and sequence (shown in Figure 1 and Table 1).

If the TSC2007 VDD cannot meet the specified power-on/-off requirements, additional circuitry is needed to insert a power cycle capability; that is, a power off and on cycle as described in Figure 1, or connecting an individual power source to the TSC2007 itself. The following sections show two example circuits that accomplish this purpose.

3.1 Cycle Power Circuitry

Figure 3 illustrates a circuit that uses a controllable power switch to cycle the TSC2007 supply on the VDD pin. This switch could be activated after a system power on sequence or if the host identifies a lockup situation.

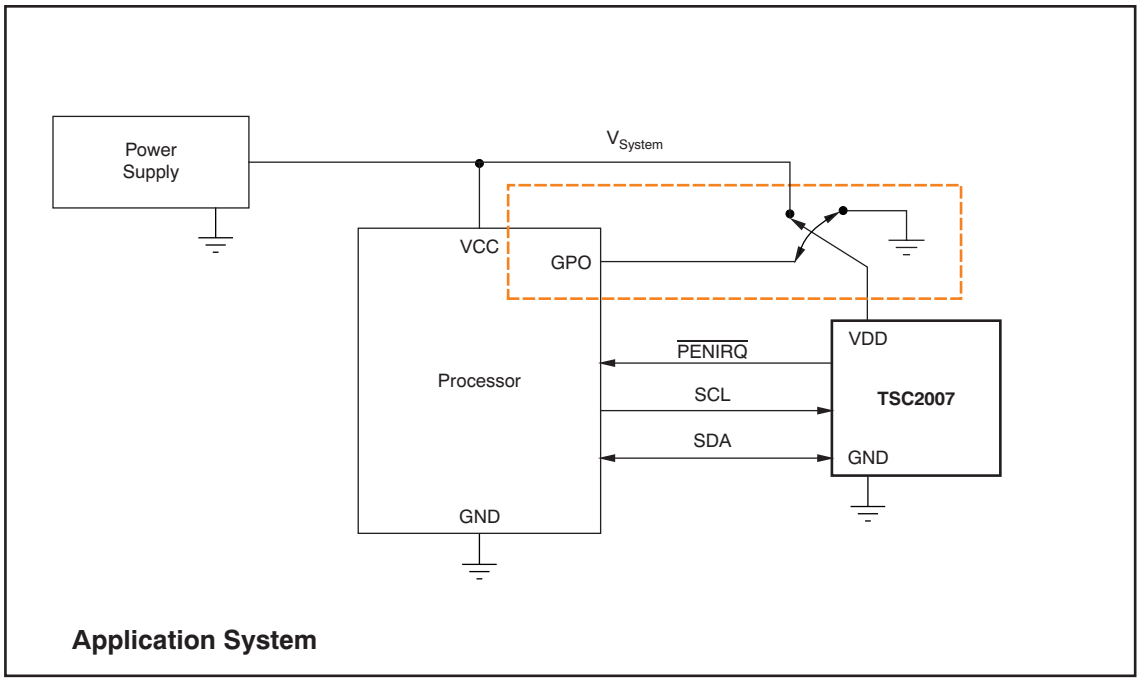

Figure 3. Cycle Power to TSC2007 by Controllable Power Switch

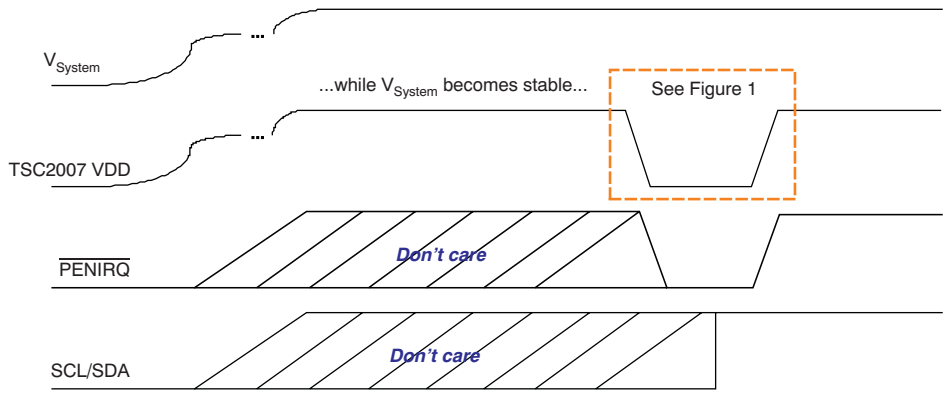

Figure 4. Power and Digital Interface Waveforms during Power Up (with Figure 3 Method)

Figure 4 shows the power-supply waveforms (to the host processor and to the TSC2007) during the course of a system power on. After the system is powered up and the system power supply is stable, the host processor initiates a power cycle for the TSC2007 using a GPO port (refer to the orange blocks in Figure 3 and Figure 4).

3.2 Individual Power Supply for the TSC2007

If the power supply of the application system is different from the devices and circuitry around the TSC2007, an individual linear regulator (LDO) may be required. If the power regulator or LDO is individually controllable, designers may use the method shown in Figure 5.

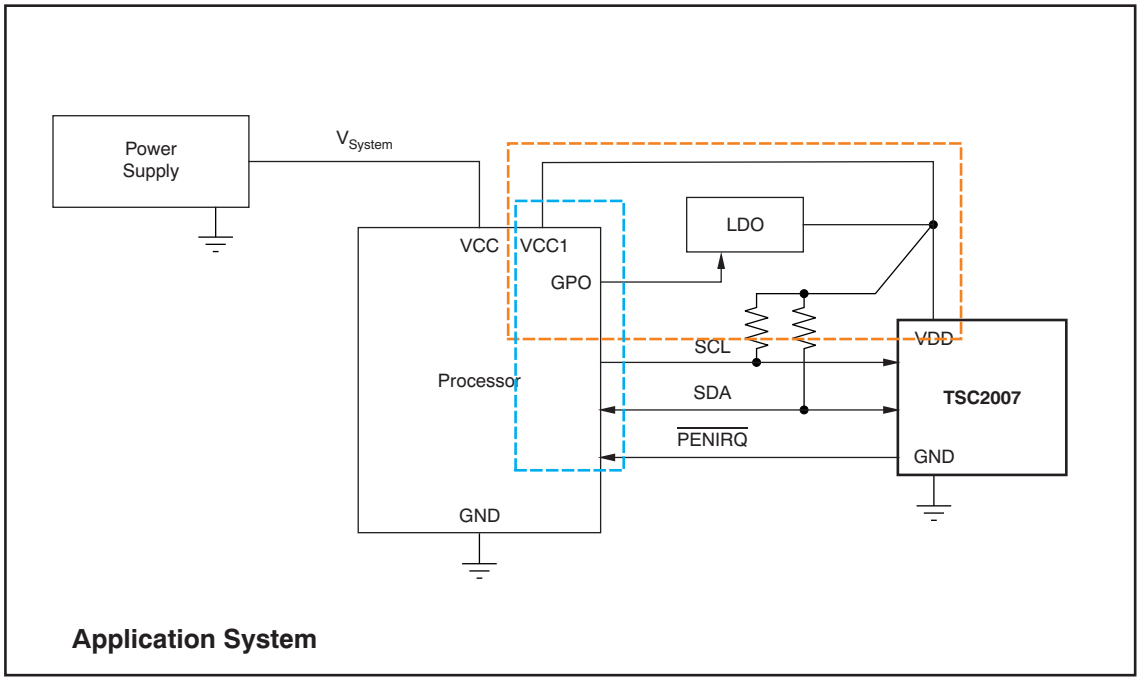

Figure 5. Individual, Controllable Power Supply for the TSC2007

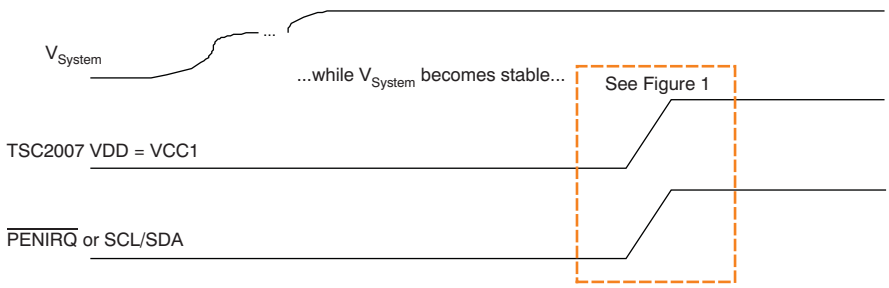

Figure 6. Power and Digital Interface Waveforms during Power Up (with Figure 5 Method)

Figure 6 shows the power-supply waveforms (to the host processor and to the TSC2007) during the course of a system power on. Note that the power supply at both ends of the circuit (that is, the TSC2007 and the host processor) of the digital interface (SCL, SDA, and $\overline{\text{PENIRQ}}$) must be at the same voltage level (as shown in Figure 5). A GPO at the host processor is used to enable/disable the LDO, and thus controls the power to the TSC2007.

4 References

This document can be downloaded from the Texas Instruments web site at www.ti.com.

1. TSC2007: Nano-Power Touch Screen Controller with I^2C Serial Interface. Product data sheet SBAS405. Available for download at www.ti.com/tsc2007.

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