

# Using the Dynamic Range Enhancer in TLV320ADC5140/6140 and PCM5140-Q1/PCM6140-Q1



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## ABSTRACT

TLV320ADC5140 and TLV320ADC6140 devices are quad-channel, high-performance, audio analog-to-digital converters that have an extensive set of features that includes the following:

- Programmable Gain Amplifier (PGA)
- Digital volume control
- A programmable microphone bias voltage
- A phase-locked loop (PLL)
- A programmable high pass filter (HPF)
- Automatic Gain Control (DRE)
- Dynamic Range Enhancer (DRE)
- Linear phase or low-latency filter modes for sample rates up-to 768 kHz

This application note describes how to configure the dynamic range enhancer (DRE) feature in TLV320ADC5140, TLV320ADC6140, PCM5140-Q1 and PCM6140-Q1 devices.

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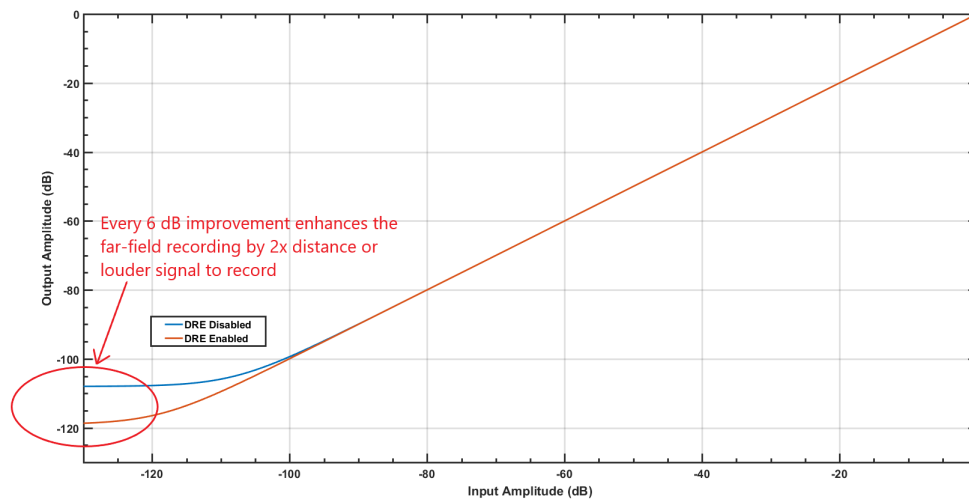
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## 1 Introduction

TLV320ADC5140, TLV320ADC6140, PCM5140-Q1, and PCM6140-Q1 devices from TI's Audio ADC portfolio features an algorithm called Dynamic Range Enhancer (DRE) that can be used to improve the far-field recording performance by improving the dynamic range of the ADC channel at low signal levels. The DRE is a digitally-assisted algorithm that dynamically adjusts the front-end programmable gain amplifier (PGA) to improve the signal-to-noise ratio of low-level signals while preventing high-level signals from saturating the PGA and ADC. Far-field recording performance can also be improved by using a high PGA gain, but it can degrade near-field recording performance since a dynamic change to high-input levels combined with a high fixed-gain PGA can saturate the PGA and ADC. The DRE provides the ability to improve the far-field recording performance without degrading the near-field recording performance. Figure 1-1 shows the improvements in channel performance with DRE. With DRE, the ADC channel performance is not limited by the ADC noise floor and improves the recording performance even for signals below the noise floor of the ADC. Every 6 dB improvement in dynamic range increases the far-field recording distance by a factor of two.

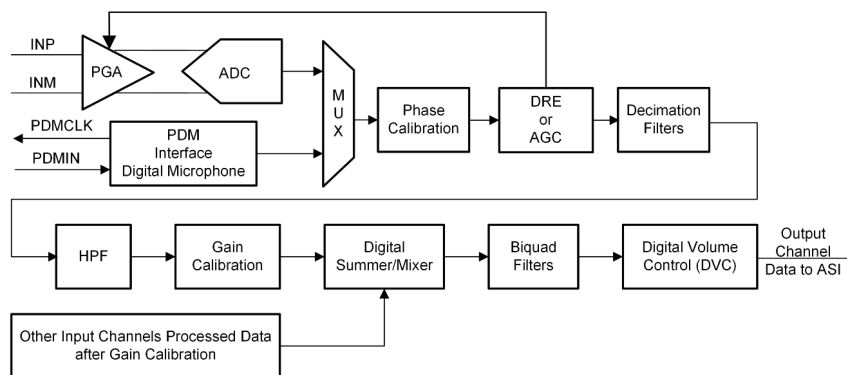


**Figure 1-1. DRE Performance**

DRE is supported on all ADC channels of TLV320ADC5140, TLV320ADC6140, PCM5140-Q1, and PCM6140-Q1 devices. This application note describes the operation of the DRE, the tunable parameters, and the device configurations required to use DRE.

## 2 Dynamic Range Enhancer

Figure 2-1 shows the signal processing chain for TLV320ADC5140, TLV320ADC6140, PCM5140-Q1, and PCM6140-Q1 devices. The dynamic range performance of the front-end PGA in TLV320ADC5140/PCM5140-Q1 and TLV320ADC6140/PCM6140-Q1 devices are 120 dB and 122 dB respectively. The subsequent delta-sigma ADC has 108 dB dynamic range for the TLV320ADC5140/PCM5140-Q1 and 113 dB dynamic range for the TLV320ADC6140/PCM6140-Q1. Without the DRE, the ultra-low noise performance of the PGA is limited by the ADC performance and the overall channel dynamic range is determined by the dynamic range of the ADC. With the DRE, the overall channel dynamic range can be improved beyond the dynamic range of the ADC and is limited more by the dynamic range of the PGA.



**Figure 2-1. Signal Processing Block Diagram**

The DRE algorithm monitors the input signal and increases the gain of the analog PGA for signal levels below a threshold. At the same time, the DRE algorithm creates a corresponding reciprocal attenuation in the digital circuits so the net effect of the analog PGA gain and digital attenuation cancel each other out. Thus the DRE improves the dynamic range without increasing the overall channel gain. The DRE does not gain signals above the threshold. Boosting the low-level signals in analog keeps the input to the ADC significantly above its noise floor and thus prevents the ADC performance from being the limiting factor. Subsequent processing is done using a high-performance, 32-bit, digital signal processor with very low quantization noise, and, therefore, the PGA performance becomes the limiting factor in the overall channel performance.

TLV320ADC5140, TLV320ADC6140, PCM5140-Q1, and PCM6140-Q1 devices support up to four analog input channels. All analog input channels support DRE. The devices support differential or single-ended signals from an analog microphone source or auxiliary line input. The analog microphone inputs support electret condenser and microelectrical-mechanical (MEMS) microphones. Even though the devices also support digital pulse density modulated (PDM) digital microphones, the DRE does not support the digital channels as the analog gain of the digital microphone cannot be controlled.

The TLV320ADCx140/PCMX140-Q1 family of devices also support an automatic gain control (AGC) algorithm on the analog channels to maintain a constant nominal output level. AGC and DRE algorithms cannot be used simultaneously since both the algorithms control the PGA. DRE or AGC selection is done using AGC\_DRE\_SEL field of DSP\_CFG1 register (page = 0x00, address = 0x6C) as shown in Table 2-1.

**Table 2-1. DRE Selection Using DSP\_CFG1 Register**

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	AGC_DRE_SEL	R/W	0h	DRE or DRE selection when is enabled for any channel. 0d = DRE is selected. 1d = DRE is selected.

DRE can be independently enabled or disabled for each channel using the following register bits:

- CH1\_DREEN (P0\_R60\_D0)
- CH2\_DREEN (P0\_R65\_D0)
- CH3\_DREEN (P0\_R70\_D0)
- CH4\_DREEN (P0\_R75\_D0)

## 2.1 High Pass Filter

To remove any DC offset that leads to incorrect input level estimates, the DRE algorithm processes the input signal through a high-pass filter (HPF). This HPF is exclusive to the DRE and is different from the second-order HPF filters used by the decimation filters.

The transfer function implemented by the HPF is given by [Equation 1](#).

$$H(z) = \frac{N0 + N1 \times z^{-1}}{1 + D1 \times z^{-1}} \quad (1)$$

The HPF is a first order filter implemented using three coefficients: DRE\_HPFB0, DRE\_HPFB1, and DRE\_HPFA1. The transfer function parameters (N0, N1, and D1) are converted to coefficients using [Equation 2](#), [Equation 3](#), and [Equation 4](#).

$$DRE\_HPFB0 = \text{round}(2^8 \times N0) \quad (2)$$

$$DRE\_HPFB1 = \text{round}(2^8 \times N1) \quad (3)$$

$$DRE\_HPFA1 = \text{round}(2^8 \times D1) \quad (4)$$

These coefficients are user-programmable to set a different cutoff frequency from the default cutoff (3 dB point) frequency of 10 Hz for a 48 kHz operation. Increasing the cutoff frequency results in faster settling of signal-level estimates. Decreasing the cutoff frequency improves the accuracy of the signal-level estimate. The default filter coefficients provide a good balance between speed and accuracy and are suitable for most applications. [Table 2-2](#) shows the coefficient registers of the HPF. The coefficients are represented in 2s-complement, 32-bit format.

**Table 2-2. Programmable Registers for High Pass Filter Coefficients**

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_HPFB0	0x06	0x6C	0x7F	DRE_HPFB0 Byte[31:24]
	0x06	0x6D	0xFF	DRE_HPFB0 Byte[23:16]
	0x06	0x6E	0xFF	DRE_HPFB0 Byte[15:8]
	0x06	0x6F	0xFF	DRE_HPFB0 Byte[7:0]
DRE_HPFB1	0x06	0x70	0x80	DRE_HPFB1 Byte[31:24]
	0x06	0x71	0x00	DRE_HPFB1 Byte[23:16]
	0x06	0x72	0x00	DRE_HPFB1 Byte[15:8]
	0x06	0x73	0x01	DRE_HPFB1 Byte[7:0]
DRE_HPFA1	0x06	0x74	0x7E	DRE_HPFA1 Byte[31:24]
	0x06	0x75	0xEE	DRE_HPFA1 Byte[23:16]
	0x06	0x76	0xD8	DRE_HPFA1 Byte[15:8]
	0x06	0x77	0xE2	DRE_HPFA1 Byte[7:0]

## 2.2 DRE Parameters

[Table 2-3](#) show the parameters of the DRE algorithm. Two of the parameters are controlled by writing to the device registers. The other parameters reside in the 32-bits wide coefficient memory (Book 0, Page 5, Page 6, and Page 7) of the device.

**Table 2-3. List of DRE Parameters**

DRE PARAMETER	FUNCTION/DESCRIPTION
DRE threshold (dB)	The signal level above which the DRE is inactive.
Maximum Gain (dB)	Upper limit of gain applied by DRE.
Release Time Constant (seconds)	How fast the DRE circuitry responds with a PGA gain increase when the input signal falls below DRE threshold.

**Table 2-3. List of DRE Parameters (continued)**

DRE PARAMETER	FUNCTION/DESCRIPTION
Attack Time Constant (seconds)	How fast the DRE circuitry responds with a PGA gain decrease when the input signal rises above DRE threshold.
Release Hysteresis (dB)	Amount of signal-level decrease in dB past the DRE threshold that forces the DRE to increase gain and start a release.
Attack Hysteresis (dB)	Amount of signal-level increase in dB past the DRE threshold that forces the DRE to decrease gain and start an attack.
Release Debounce (samples)	The number of consecutive input samples that falls below the DRE threshold after an attack event before the DRE starts a release and increases the PGA gain.
Attack Debounce (samples)	The number of consecutive input samples that rises above the DRE threshold after a release event before the DRE starts an attack and decreases the PGA gain.

**DRE threshold:** The signal level above which the DRE stops modifying the PGA and sets it to unity gain. The threshold level is expressed relative to full scale (dBFS) of the ADC output. [Table 2-4](#) lists the DRE threshold configuration settings. The default is -54 dB. Setting a high threshold level reduces the headroom available for the DRE to react when there is a sudden increase in the signal level and can result in digital clipping and PGA saturation. Therefore, the DRE threshold has to be set with enough margin to prevent clipping with large dynamic changes in input levels.

**Table 2-4. DRE Trigger Threshold Level Programmable Settings**

P0_R109_D[7:4] : DRE_LVL[3:0]	DRE TRIGGER THRESHOLD LEVEL
0000	The DRE target threshold is the -12 dB output signal level.
0001	The DRE target threshold is the -18 dB output signal level.
0010	The DRE target threshold is the -24 dB output signal level.
...	...
0111 (default)	The DRE target threshold is the -54 dB output signal level.
...	...
1001	The DRE target threshold is the -66 dB output signal level.
1010 to 1111	Reserved (do not use these settings)

**Maximum Gain:** The maximum gain represents the upper limit of gain applied by the DRE for signals below the DRE threshold. [Table 2-5](#) lists the Maximum Gain configuration settings. The default value is 24 dB. It can be programmed from 2 dB to 30 dB with steps of 2 dB.

**Table 2-5. DRE Maximum Gain Programmable Settings**

P0_R109_D[3:0] : DRE_MAXGAIN[3:0]	DRE MAXIMUM GAIN ALLOWED
0000	The DRE maximum gain allowed is 2 dB.
0001	The DRE maximum gain allowed is 4 dB.
0010	The DRE maximum gain allowed is 6 dB.
...	...
1011 (default)	The DRE maximum gain allowed is 24 dB.
...	...
1110	The DRE maximum gain allowed is 30 dB.
1111	Reserved (do not use this setting)

**Release Time Constant:** How fast the DRE circuitry increases the PGA gain when the input signal falls below the DRE threshold. The Release Time Constant is controlled by two coefficients: DRE\_REL\_ALPHA and DRE\_REL\_BETA. [Equation 5](#) and [Equation 6](#) show how to compute the DRE\_REL\_ALPHA and DRE\_REL\_BETA parameters from the following time constant.

$$DRE\_REL\_ALPHA = \text{round}(2^{31} * e^{-\ln(9)/48000 * RT}) \quad (5)$$

$$\text{DRE\_REL\_BETA} = 2^{31} - \text{round}(2^{31} * e^{-\ln(9)/48000 * \text{RT}}) \quad (6)$$

where

- RT is the Release Time Constant in seconds
- FSYNC is the sample rate of the ADC in Hz

Table 2-6 shows the registers that control the DRE\_REL\_ALPHA and DRE\_REL\_BETA parameters. These parameters are each 32-bits wide, and have to be written in 2s-complement representation. The default values for DRE\_REL\_ALPHA and DRE\_REL\_BETA corresponds to a time constant of 20 milliseconds.

**Table 2-6. Programmable Registers for Release Time Constant Parameter**

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_REL_ALPHA	0x05	0x7C	0x7F	DRE_REL_ALPHA Byte[31:24]
	0x05	0x7D	0xB5	DRE_REL_ALPHA Byte[23:16]
	0x05	0x7E	0x16	DRE_REL_ALPHA Byte[15:8]
	0x05	0x7F	0x50	DRE_REL_ALPHA Byte[7:0]
DRE_REL_BETA	0x06	0x08	0x00	DRE_REL_BETA Byte[31:24]
	0x06	0x09	0x4A	DRE_REL_BETA Byte[23:16]
	0x06	0x0A	0xE9	DRE_REL_BETA Byte[15:8]
	0x06	0x0B	0xB0	DRE_REL_BETA Byte[7:0]

**Attack Time Constant:** How fast the DRE circuitry decreases the PGA gain when input signal rises above the DRE threshold. The Attack Time Constant is controlled by two coefficients: DRE\_ATT\_ALPHA and DRE\_ATT\_BETA. Equation 7 and Equation 8 show how to compute the DRE\_ATT\_ALPHA and DRE\_ATT\_BETA parameters from the following time constant.

$$\text{DRE\_ATT\_ALPHA} = \text{round}(2^{31} * e^{-\ln(9)/48000 * \text{AT}}) \quad (7)$$

$$\text{DRE\_ATT\_BETA} = 2^{31} - \text{round}(2^{31} * e^{-\ln(9)/48000 * \text{AT}}) \quad (8)$$

where

- AT is the Attack Time Constant in seconds
- FSYNC is the sample rate of the ADC in Hz

DRE\_ATT\_ALPHA and DRE\_ATT\_BETA coefficients are each 32-bits wide, 2s-complement representations. Table 2-7 shows the registers that control DRE\_ATT\_ALPHA and DRE\_ATT\_BETA parameters. The default values for DRE\_ATT\_ALPHA and DRE\_ATT\_BETA corresponds to a time constant of 0.1 milliseconds.

**Table 2-7. Programmable Registers for Attack Time Constant Parameter**

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_ATT_ALPHA	0x06	0x0C	0x50	DRE_ATT_ALPHA Byte[31:24]
	0x06	0x0D	0xFC	DRE_ATT_ALPHA Byte[23:16]
	0x06	0x0E	0x64	DRE_ATT_ALPHA Byte[15:8]
	0x06	0x0F	0x5C	DRE_ATT_ALPHA Byte[7:0]
DRE_ATT_BETA	0x06	0x10	0x2F	DRE_ATT_BETA Byte[31:24]
	0x06	0x11	0x03	DRE_ATT_BETA Byte[23:16]
	0x06	0x12	0x9B	DRE_ATT_BETA Byte[15:8]
	0x06	0x13	0xA4	DRE_ATT_BETA Byte[7:0]

**Release Hysteresis:** Amount of signal-level decrease past the DRE threshold that forces the DRE to increase gain and start a release. Release Hysteresis is specified in dB. Equation 9 shows the computation of the DRE\_REL\_HYST parameter.

$$\text{DRE\_REL\_HYST} = \text{round}(2^8 * \text{RH}) \tag{9}$$

where

- RH (>= 0) is the Release Hysteresis in dB

The default value of DRE\_REL\_HYST is 0x00000300, which corresponds to a hysteresis of 3 dB. [Table 2-8](#) shows the registers that control the DRE\_REL\_HYST parameter.

**Table 2-8. Programmable Registers for Release Hysteresis Parameter**

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_REL_HYST	0x06	0x34	0x00	DRE_REL_HYST Byte[31:24]
	0x06	0x35	0x00	DRE_REL_HYST Byte[23:16]
	0x06	0x36	0x03	DRE_REL_HYST Byte[15:8]
	0x06	0x37	0x00	DRE_REL_HYST Byte[7:0]

**Attack Hysteresis:** Amount of signal-level increase past DRE threshold that forces the DRE to decrease the gain and start an attack. [Equation 10](#) shows the computation of the DRE\_ATT\_HYST parameter.

$$\text{DRE\_ATT\_HYST} = \text{round}(2^8 * \text{AH}) \tag{10}$$

where

- AH (>= 0) is the Attack Hysteresis in dB

The default value of Attack Hysteresis is 1 dB. The default can be changed by writing to the registers listed in [Table 2-9](#).

**Table 2-9. Programmable Registers for Attack Hysteresis Parameter**

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_ATT_HYST	0x06	0x3C	0x00	DRE_ATT_HYST Byte[31:24]
	0x06	0x3D	0x00	DRE_ATT_HYST Byte[23:16]
	0x06	0x3E	0x01	DRE_ATT_HYST Byte[15:8]
	0x06	0x3F	0x00	DRE_ATT_HYST Byte[7:0]

**Attack Debounce:** The number of consecutive input samples that rises above the DRE threshold after a release event before the DRE starts attack and decreases the PGA. The default value of this parameter is 2 samples at 48 kHz (0.01 milliseconds). [Equation 11](#) shows the computation of DRE\_ATT\_CNT parameter.

$$\text{DRE\_ATT\_CNT} = \text{round}(2^8 * \text{FSYNC} * \text{AD}) \tag{11}$$

where

- AD (>= 0) is specified in seconds
- FSYNC is the sample rate of the ADC in Hz

[Table 2-10](#) shows the registers controlling the DRE\_ATT\_CNT parameter.

**Table 2-10. Programmable Registers for Attack Debounce Parameter**

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_ATT_CNT	0x06	0x18	0x00	DRE_ATT_CNT Byte[31:24]
	0x06	0x19	0x00	DRE_ATT_CNT Byte[23:16]
	0x06	0x1A	0x02	DRE_ATT_CNT Byte[15:8]
	0x06	0x1B	0x00	DRE_ATT_CNT Byte[7:0]

**Release Debounce:** The number of consecutive input samples that falls below DRE threshold after an attack event before the DRE starts releasing and increasing the PGA. The default value of Release Debounce is 25 milliseconds at 48 kHz. Equation 12 shows the computation of the DRE\_REL\_CNT parameter.

$$\text{DRE\_REL\_CNT} = \text{round}(2^8 * \text{FSYNC} * \text{RD}) \quad (12)$$

where

- RD ( $\geq 0$ ) is the Release Debounce specified in seconds
- FSYNC is the sample rate of the ADC in Hz

Table 2-11 lists the registers controlling the DRE\_REL\_CNT parameter.

**Table 2-11. Programmable Registers for Release Debounce Parameter**

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_REL_CNT	0x06	0x1C	0x00	DRE_REL_CNT Byte[31:24]
	0x06	0x1D	0x04	DRE_REL_CNT Byte[23:16]
	0x06	0x1E	0xB0	DRE_REL_CNT Byte[15:8]
	0x06	0x1F	0x00	DRE_REL_CNT Byte[7:0]

## 2.3 Sample Rate Support

The DRE algorithm does not support all sampling rates and all channel combinations. Table 2-12 shows the sample rates and the corresponding number of channels supported at that sample rate by the DRE algorithm. For sample rates from 16 or 14.7 kHz to 48 or 44.1 kHz, the DRE algorithm supports all four analog channels. At a 96 or 88.2 kHz sample rate, the DRE algorithm only supports a maximum of two channels. At a 192 or 176.4 kHz sample rate, DRE is restricted to just one channel.

**Table 2-12. Sample Rates Supported by DRE Algorithm**

SAMPLE RATE (kHz)	NUMBER OF CHANNELS
16/14.7	4
24/22.05	4
32/29.4	4
48/44.1	4
96/88.2	2
192/176.4	1



### 3 Example

The DRE default parameters work well for most applications. The default DRE trigger threshold is -54 dB. This provides sufficient headroom for the DRE to react in a timely manner to a sudden loud signal. Increasing the DRE trigger threshold improves the small-signal performance, but it decreases the headroom available before switching to an attack cycle. This can be mitigated by decreasing the attack time. This section shows an example where a higher DRE trigger threshold is set and time constants adjusted to make the DRE respond faster.

- Target Level = -54 dB
- Maximum Gain = 24 dB
- Attack Time = 0.01 ms
- Release Time = 20 ms
- Attack Hold = 0.0417 ms
- Release Hold = 20 ms
- Attack Hysteresis = 1 dB
- Release Hysteresis = 3 dB

```
# Key: w 98 XX YY ==> write to I2C address 0x98, to register 0xxx, data 0xyy
# # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Differential 4-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2, INP3/INM3 - Ch3 and INP4/INM4 - Ch4
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
#####
#
# Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# wait for 1ms.
#
w 98 00 00 # Goto Page 0
w 98 02 81 # Exit Sleep mode
d 10      # wait for 16 ms
w 98 6C 40 # Enable DRE in DSP_CFG1
w 98 3C 01 # Select DRE on Ch. 1 using CH1_CFG0
w 98 41 01 # Select DRE on Ch. 2 using CH2_CFG0
w 98 74 01 # Select DRE on Ch. 3 using CH3_CFG0
w 98 75 01 # Select DRE on Ch. 4 using CH4_CFG0
w 98 6D 4B # DRE LVL = -36 dB, DRE GAIN = 24 dB
w 98 00 05      # Goto Page 5
w 98 7C 7F B5 16 50 # DRE Release Time Alpha
w 98 00 05      # Goto Page 6
w 98 08 00 4A E9 B0 # DRE Release Time Beta
w 98 0C 01 50 DB 39 # DRE Attack Time Alpha
w 98 10 7E B5 16 50 # DRE Attack Time Beta
w 98 18 00 00 02 00 # DRE Attack Debounce
w 98 1C 00 04 B0 00 # DRE Release Debounce
w 98 3C 00 00 01 00 # DRE Attack Hysteresis
w 98 34 00 00 03 00 # DRE Release Hysteresis

w 98 00 00 # Goto Page 0
w 98 07 30 # TDM Mode with 32 Bits/Channel
w 98 73 f0 # Enable Ch.1 - Ch.4
w 98 74 f0 # Enable ASI Output channels
w 98 75 e0 # Power up ADC
```

## 4 References

- Texas Instruments, [TLV320ADC5140 Quad-Channel, 768-kHz, Burr-Brown Audio ADC](#), data sheet.
- Texas Instruments, [TLV320ADC3140 Quad-Channel, 768-kHz, Burr-Brown Audio ADC](#), data sheet.
- Texas Instruments, [PCM5140-Q1 Quad-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet](#).
- Texas Instruments, [PCM3140-Q1 Quad-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet](#).

## 5 Revision History

<b>Changes from Revision * (September 2019) to Revision A (December 2023)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added PCM5140-Q1 and PCM3140-Q1 throughout the document.....	1

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