User's Guide

ADS8860EVM-PDK

Art Kay

ABSTRACT

This user's guide describes the operation and use of the ADS8860 evaluation module (EVM). The ADS8860 is a 16-bit, pseudo-differential, unipolar, successive approximation register (SAR), analog-to-digital converter (ADC) with a maximum throughput of 1 MSPS. The device is a very low-power ADC with excellent noise and distortion performance for ac or dc signals. The performance demonstration kit (PDK) eases EVM evaluation with additional hardware and software for computer connectivity through a universal serial bus (USB). The ADS8860EVM-PDK includes the ADS8860EVM as a daughter card, Precision Host Adaptor (PHI) digital controler, and a A-to-B USB cable. This user's guide covers circuit description, schematic diagram, and bill of materials for the ADS8860EVM daughter card.

Table 1-1. Related Documentation

Device	Literature Number
ADS8860	SBAS547
OPA320	SBOS351
REF6050	SBOS410
TPS7A4700	SLOS432
TPS3836K33	SLVS382

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1 EVM Overview

Table 1-1 lists the related documents that are available for download from Texas Instruments at www.ti.com.

1.1 ADS8860EVM Kit

The ADS8860 evaluation module kit includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8860 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS8860 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft Windows™7, Windows 8, and Windows 10 operating systems
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

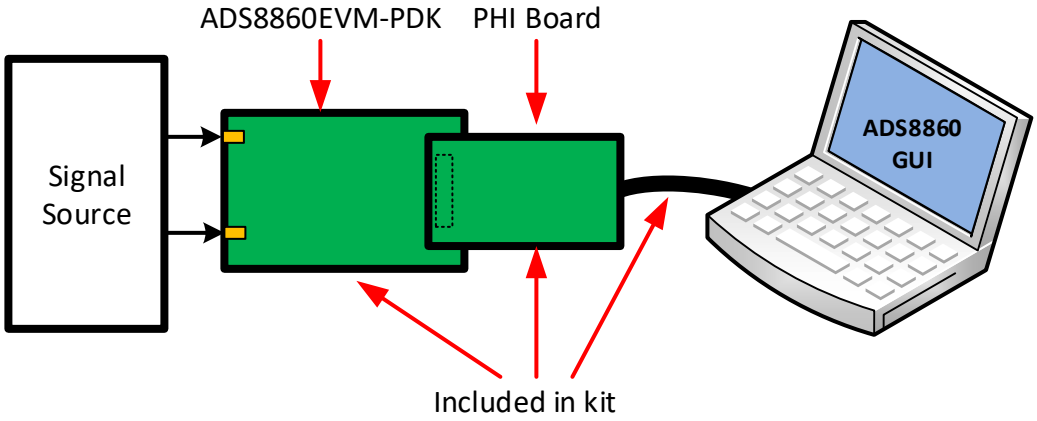


Figure 1-1. System Connection for Evaluation

1.2 ADS8860EVM Board

The ADS8860EVM board includes:

- An external single-ended signal source applied to the SMA connector.
- The amplifier driver and voltage reference circuit can be used as a reference design. These components are optimized to meet the ADS8860 data sheet performance at 1 MSPS.
- The serial interface connects to the PHI controller via a 60-pin connector (J2).
- Test-point connection monitor digital signals with a logic analyzer.
- An onboard ultra-low noise low-dropout (LDO) regulator provides an excellent 3.3-V and 5.3-V voltage range.
- The REF6050 precision 5-V voltage reference is optimized for the SAR ADC V_{REF} input.

2 EVM Analog Interface

The ADS8860EVM is an evaluation module built to the TI Modular EVM system specifications. The EVM by itself has no microprocessor and cannot run software. Thus, the EVM is available as part of the ADS8860EVM-PDK kit that combines the ADS8860EVM as a daughter board with PHI controller using software as a graphical user interface (GUI).

2.1 ADC Drive Amplifier and Filter

The circuit shown in Figure 2-1 shows a typical amplifier drive circuit for the ADS8860. The amplifier (U4) and its associated output filter (R13, R14, and C7) are designed for good SNR and THD performance at a maximum sampling rate (1 MSPS). In general, the *OPAx320* was selected for its wide bandwidth and low output impedance. This device also has rail-to-rail input and output swing without crossover distortion. The input filter (R1 and C1) are used to minimize input noise and can be adjusted according to your requirements. For more details on this circuit, see the *SAR ADC Front End Component Selection*.

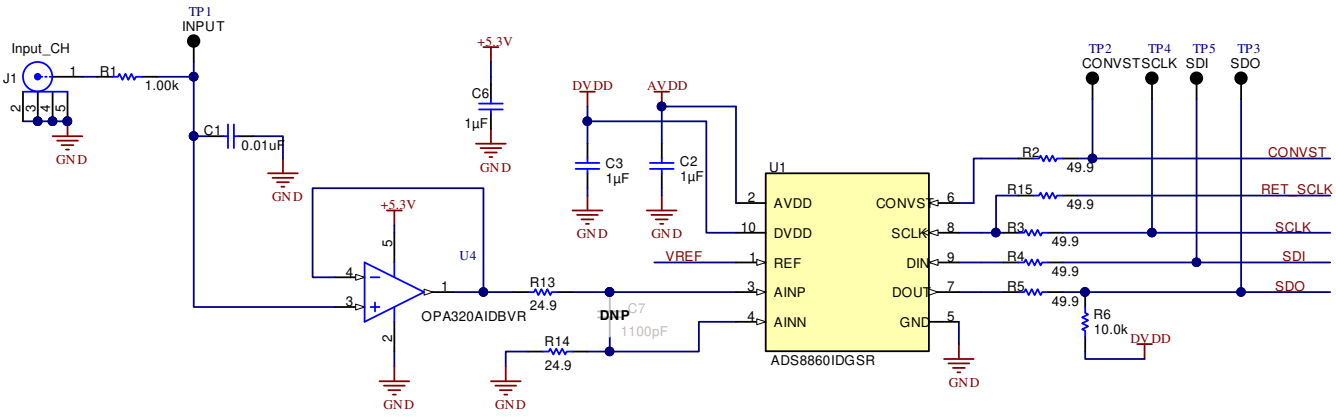


Figure 2-1. ADS8860 Input Drive Circuit

2.2 Reference Drive

The circuit shown in Figure 2-2 shows the voltage reference input drive for the SAR ADC. For many SAR ADCs, such as the ADS8860, the reference input is a switched capacitor input. This type of input requires a wide-bandwidth, low-impedance signal source. Many standard voltage reference require an external wide bandwidth buffer to drive the reference input. The *REF60xx* has a built-in, wide-bandwidth driver, and is therefore optimized for driving SAR ADC reference inputs. The output filter network (R11 and C12) are the standard components recommended in the *REF60xx* for stable, low-noise operation.

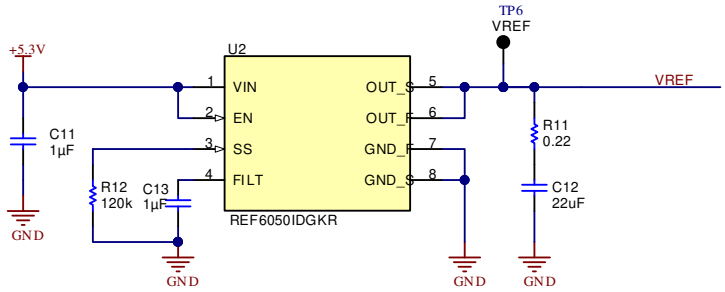


Figure 2-2. Reference Input Drive

3 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS8860 ADC (over SPI) and the EEPROM (over I^2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS8860 platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 Serial Interface (SPI)

The ADS8860 ADC uses an SPI serial communication in mode 1 (CPOL = 0, CPHA = 1) with high-speed clocks higher than 30 MHz; for slower clocks, mode 0 is used (CPOL = 0, CPHA = 0). Because the serial clock (SCLK) frequency can be as fast as 80 MHz, the ADS8860EVM offers 47-Ω resistors between the SPI signals and J2 to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 47-Ω resistors slow down the signal edges in order to minimize signal overshoot.

3.2 I^2C Bus for the Onboard EEPROM

The circuit shown in Figure 3-1 is used with the EVM controler (PHI) for EVM identification. This circuit is not required by the ADS8860 for operation. The switch (S2) is write protected and does not need to be changed for EVM operation.

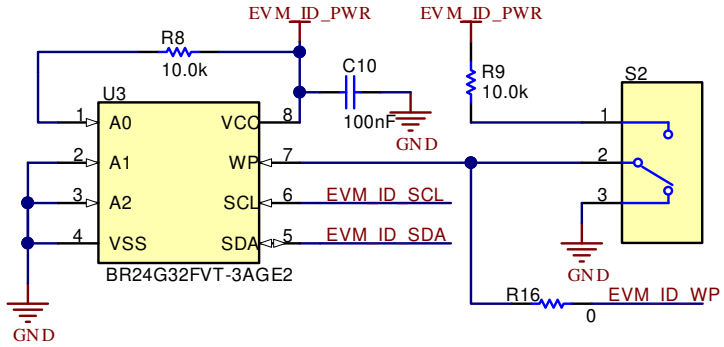


Figure 3-1. EEPROM for the EVM ID

4 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the USB supply of the computer. The EEPROM on the ADS8860EVM uses a 3.3-V power supply generated directly by the PHI. The EVM_REG_5V5 is a 5.5-V supply from the PHI and is applied to the input of two LDOs to generate other supplies on the EVM. The analog supply of the ADC (AVDD = 3.3 V) is powered by the TPS7A4700RGWR (U11) LDO. A 5.3-V supply is also generated using TPS7A4700RGWR (U9) LDO. This supply powers the voltage reference (U2) and amplifier (U4). The ADC digital supply (DVDD = 3.3 V), is generated by the PHI. Three LEDs are connected to the 5.3-V, AVDD, and DVDD supplies. These LEDs illuminate after the software GUI loads and the PHI turns on its output power supplies.

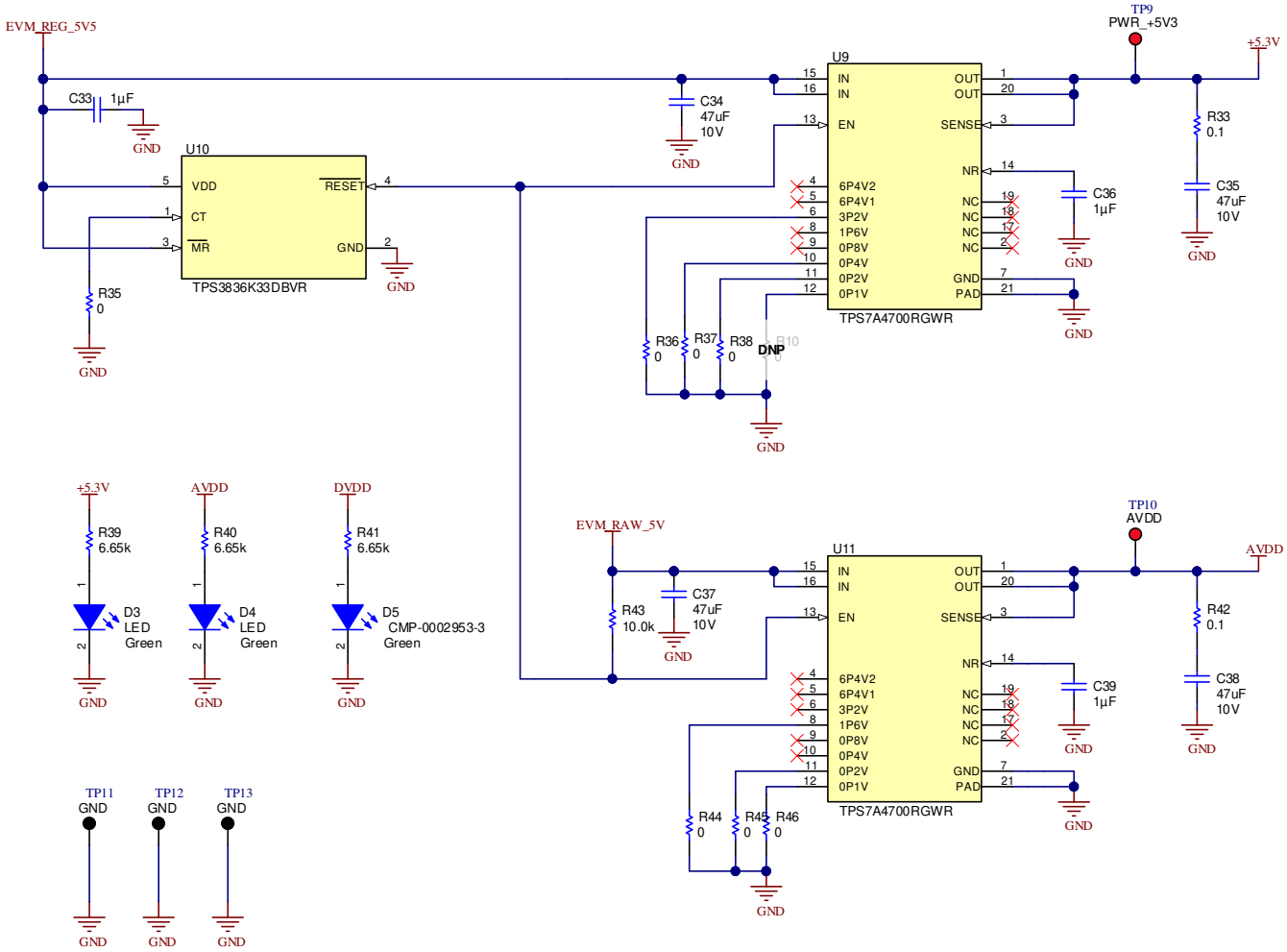


Figure 4-1. Power Supplies, Regulators, and Indicators

5 ADS8860EVM Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for properly operating the ADS8860EVM.

5.1 Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS8860EVM and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the installer. The exe file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 5-1 to complete the installation.

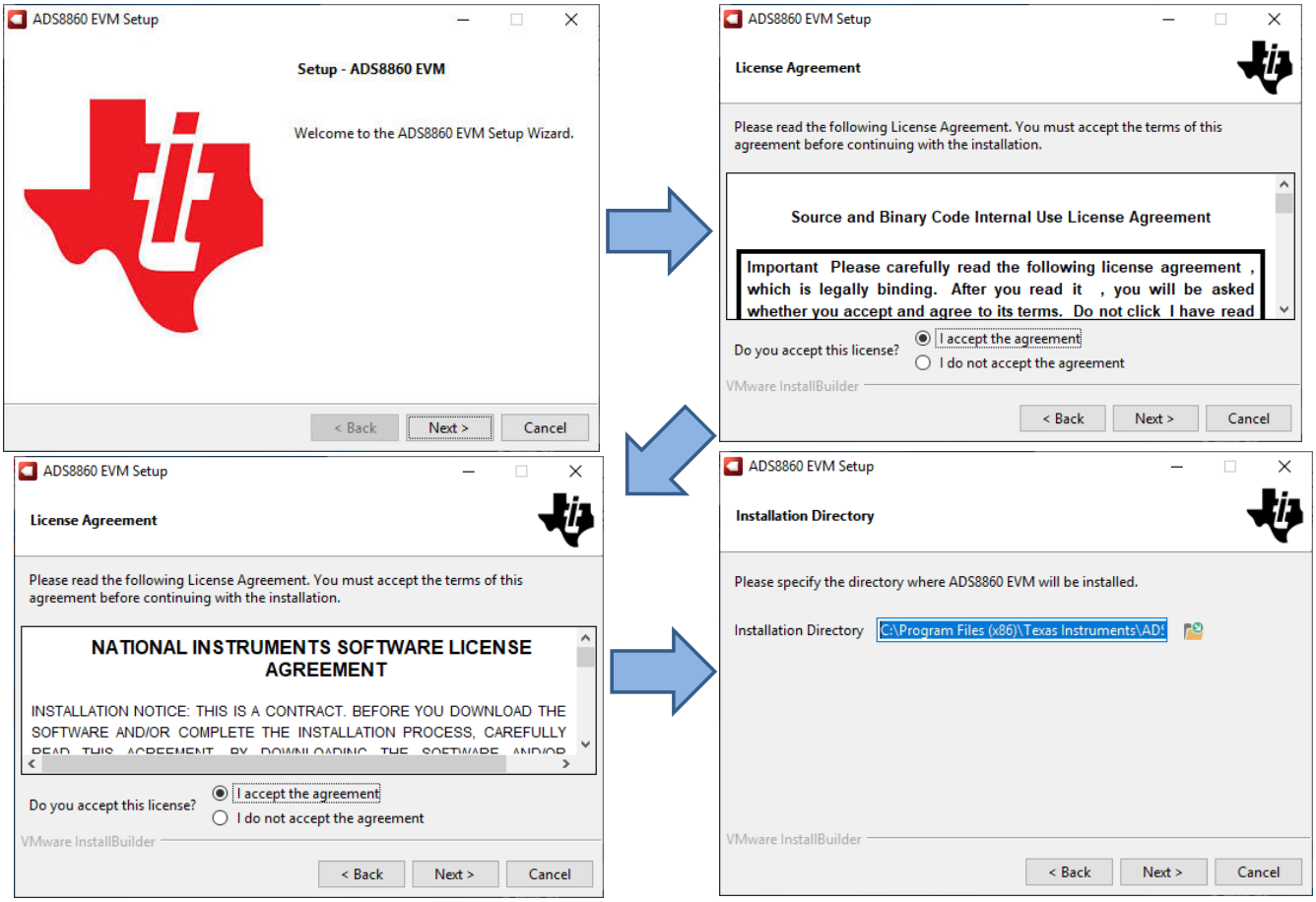


Figure 5-1. ADS8860 Software Installation Prompts

As a part of the ADS8860EVM GUI installation, a prompt with a *Device Driver Installation* (as shown in Figure 5-2) appears on the screen. Click *Next* to proceed.

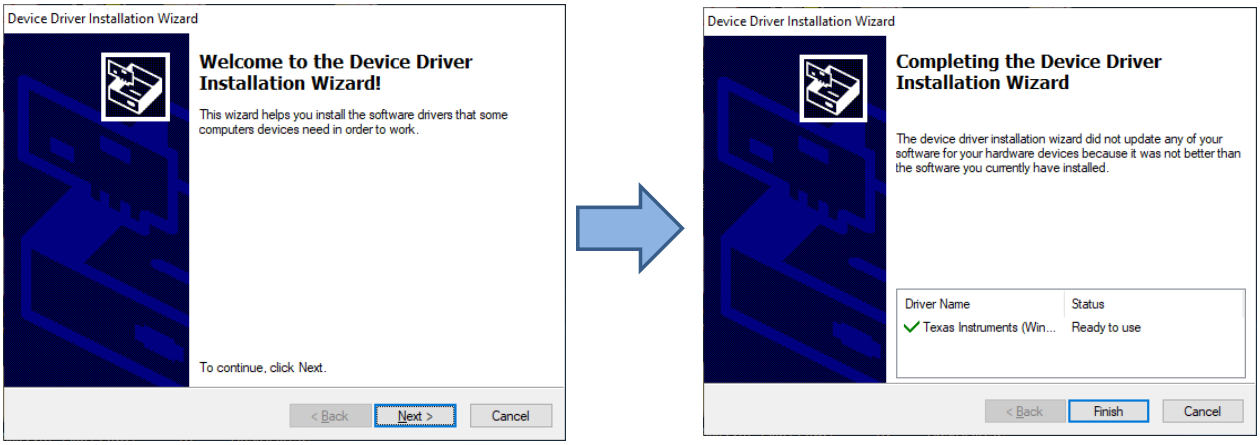


Figure 5-2. Device Driver Installation Wizard Prompts

The ADS8860EVM requires the LabVIEW™ run-time engine and may prompt for the installation of this software, as shown in Figure 5-3, if not already installed.

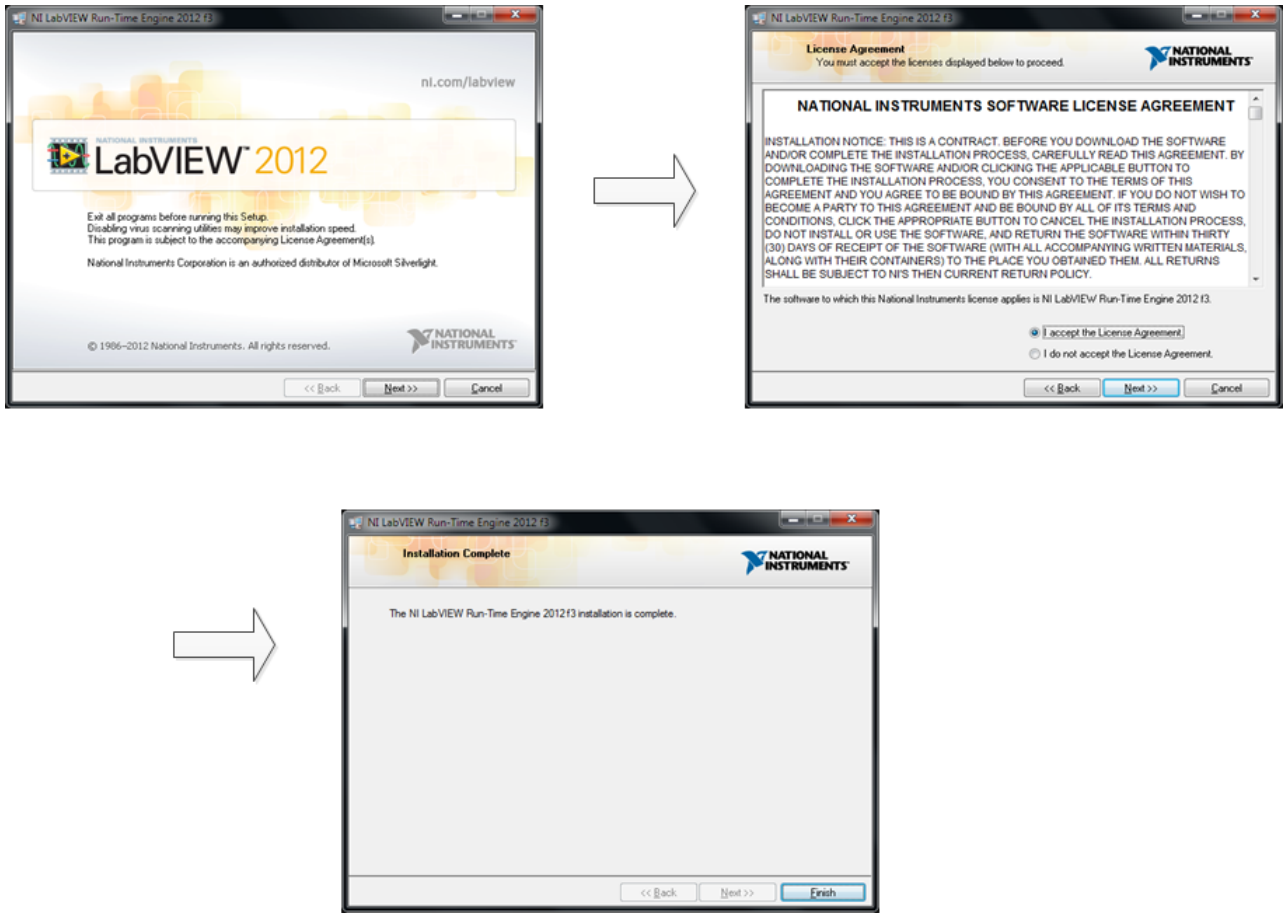


Figure 5-3. LabVIEW Run-Time Engine Installation

Verify that *C:\Program Files (x86)\Texas Instruments\ADS8860EVM* is as shown in Figure 5-4 after these installations.

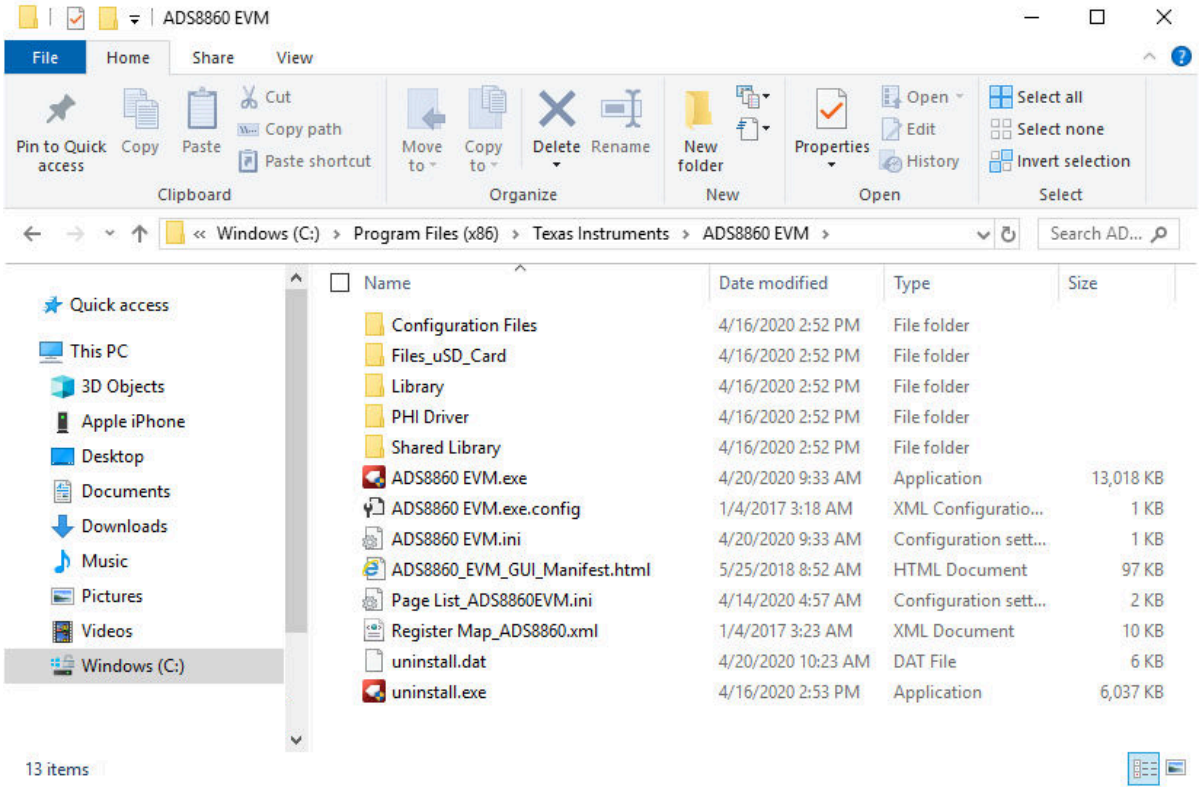


Figure 5-4. ADS8860EVM GUI Folder Post-Installation

6 EVM Operation

The following instructions are a step-by-step guide to connecting the ADS8860EVM to the computer and evaluating the performance of the ADS8860:

6.1 Connecting the Hardware

Connect the EVM as shown in Figure 6-1 after installing the software:

1. Physically connect P2 of the PHI to J2 of the ADS8860EVM. Install the screws to assure a robust connection.
2. Connect the USB on the PHI to the computer first.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up
   - LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 6-1 shows the resulting LED indicators
3. Start the software GUI as shown in Figure 6-2. Notice that the LEDs blink slowly while the FPGA firmware is loaded on the PHI. This process takes a few seconds, then the AVDD and DVDD power supplies turn on.
4. Connect the signal generator. The input range is 0 V to 5 V. A common input signal applied is a 4.9-V_{PP} signal with a 2.5-V offset. This signal is adjusted just below the full-scale range to avoid clipping.

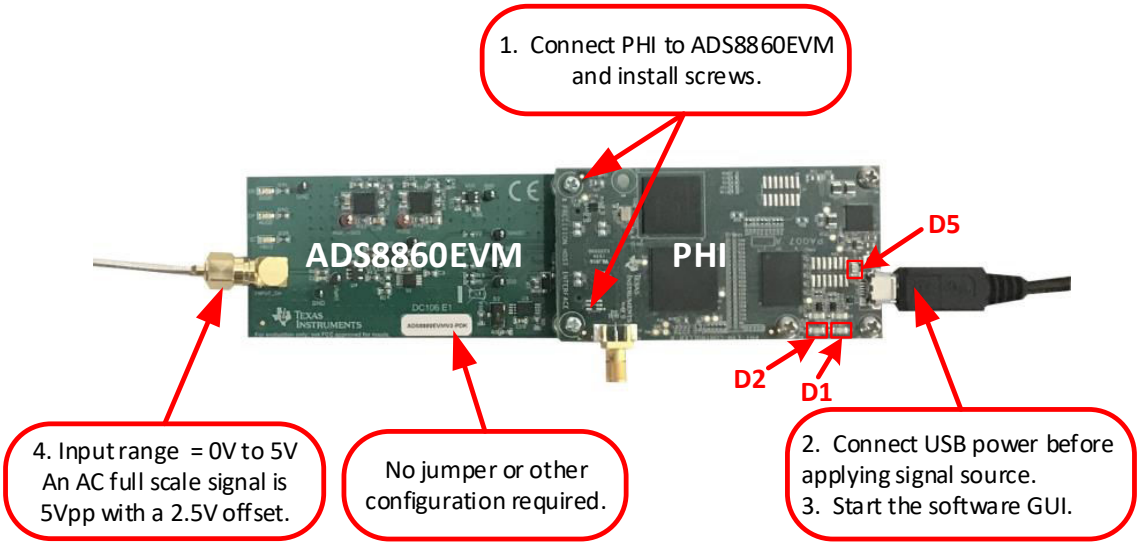


Figure 6-1. ADS8860EVM Hardware Setup and LED Indicators

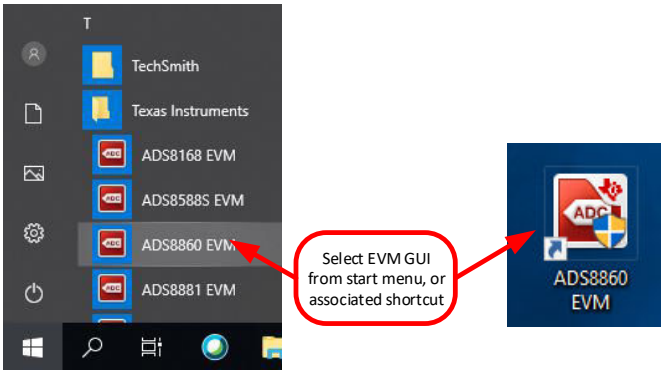


Figure 6-2. Launch the EVM GUI Software

6.2 Using the Optional Precision Signal Injector (PSI)

The ADS8860 has excellent AC specifications (typically SNR = 93 dB, THD = -108 dB). Many commercial signal generators cannot generate a signal with low enough noise and distortion to properly evaluate this device. Texas Instruments offers a evaluation module that acts as a high-fidelity signal generator (for f = 2 kHz). This signal generator uses a 2-kHz, fifth-order, band-pass filter to generate a very low noise, low distortion signal. Jumper positions for single-ended operation are provided in Table 6-1. See the PSIEVM for more information on this EVM.

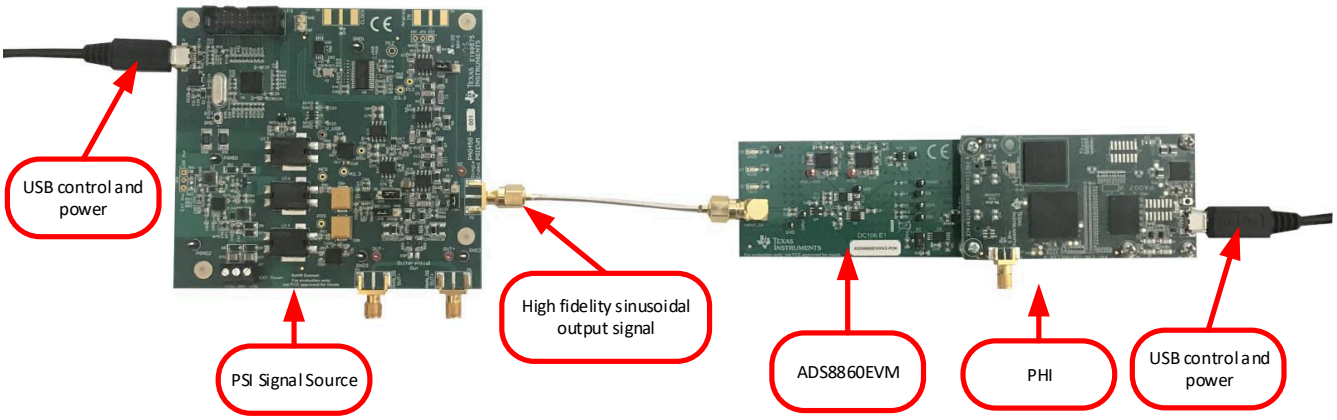


Figure 6-3. PSI Signal Generator Connection

Table 6-1. Jumper Positions for PSI

Jumper	Position	Comment
JP1	FILT	Connects a 2-kHz filter
JP3	FILT	Connects a 2-kHz filter
JP4	VCM	Common-mode control for single-ended signals enabled
JP8	GND	Common-mode control for differential signals disabled

6.3 EVM GUI Global Settings for ADC Control

Figure 6-4 shows that the EVM Global controls are located on the right hand side of the GUI. These controls choose the page display, SPI mode, SCLK frequency, and sampling frequency.

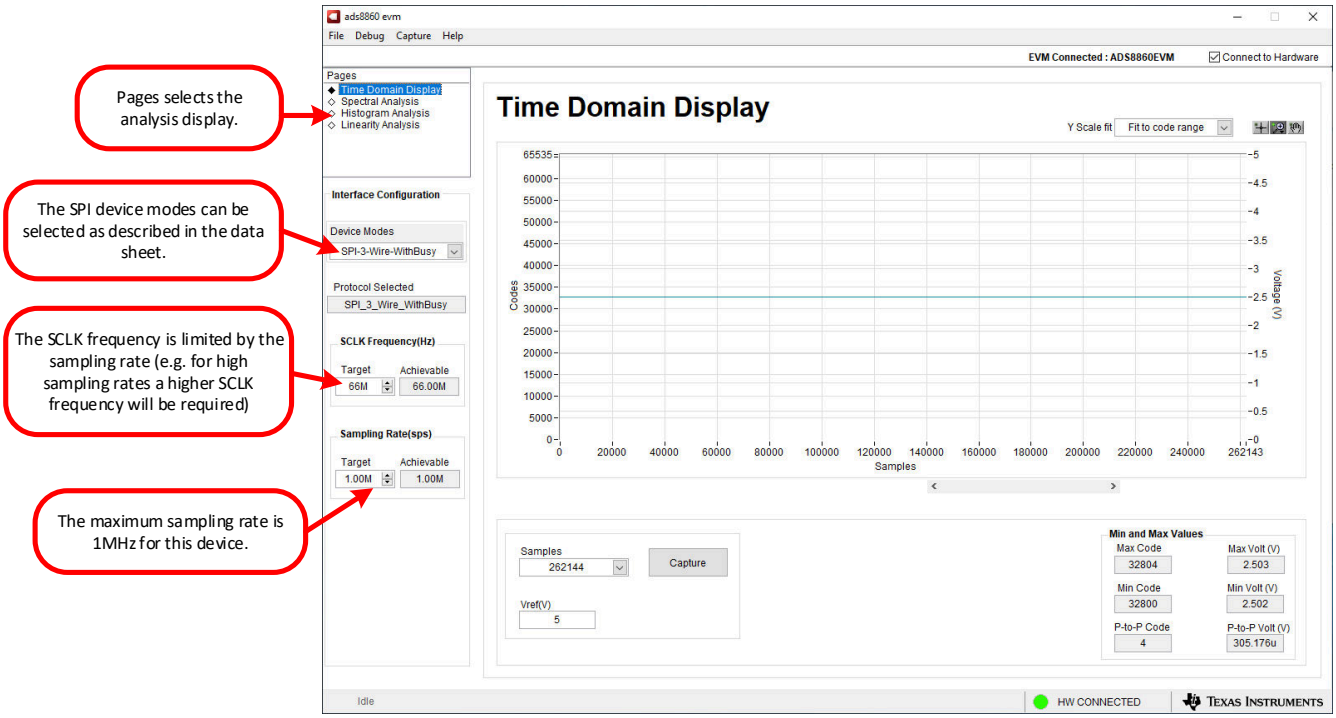


Figure 6-4. EVM GUI Global Input Controls

6.4 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. The user can trigger data capture of the selected number of samples from the ADS8860EVM, as per the current interface mode settings indicated in Figure 6-5 by using the Capture button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

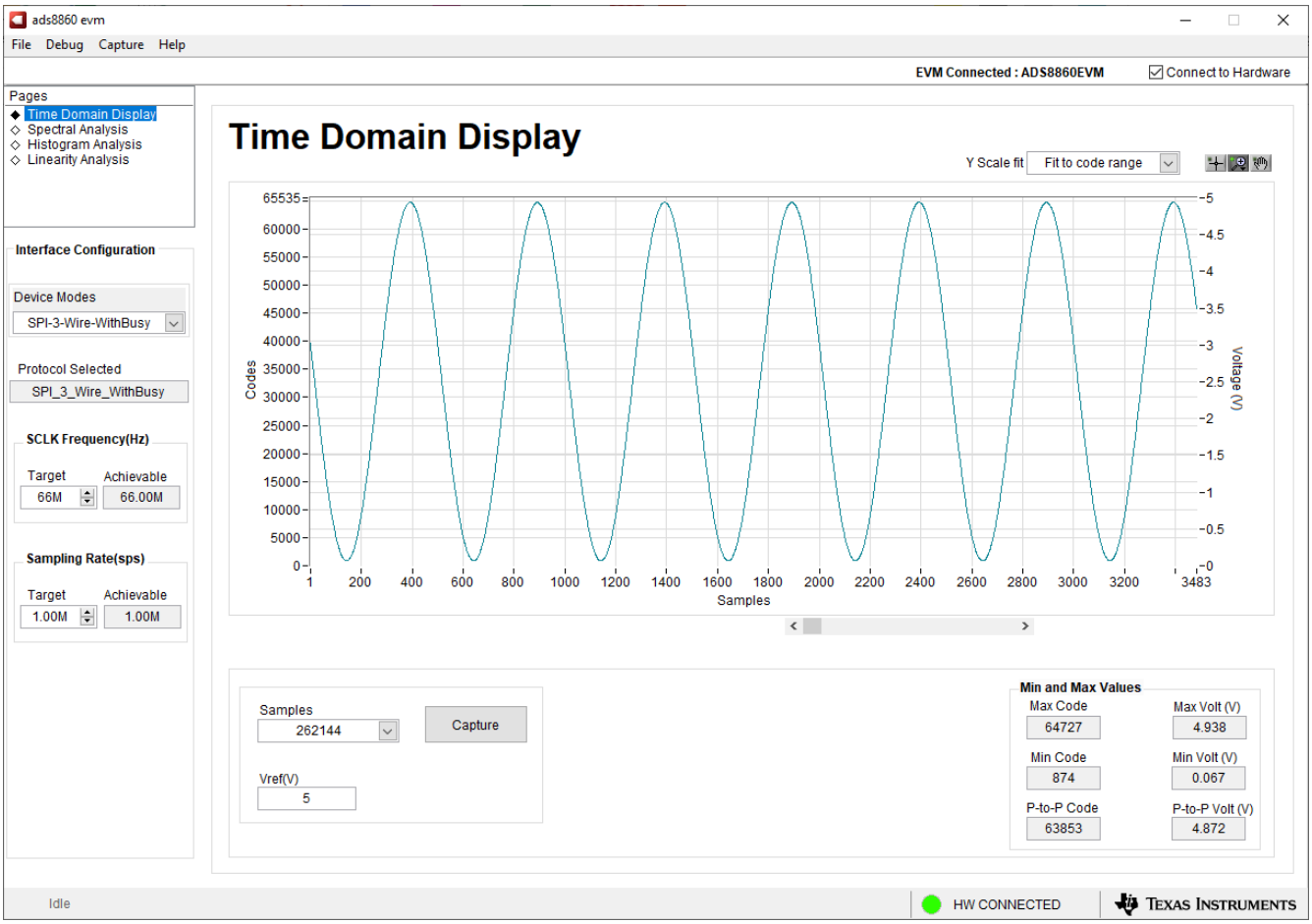


Figure 6-5. Time Domain Display Tool Options

6.5 Frequency Domain Display

The spectral analysis tool, shown in Figure 6-6, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8860 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The None option corresponds to not using a window (or using a rectangular window) and is not recommended.

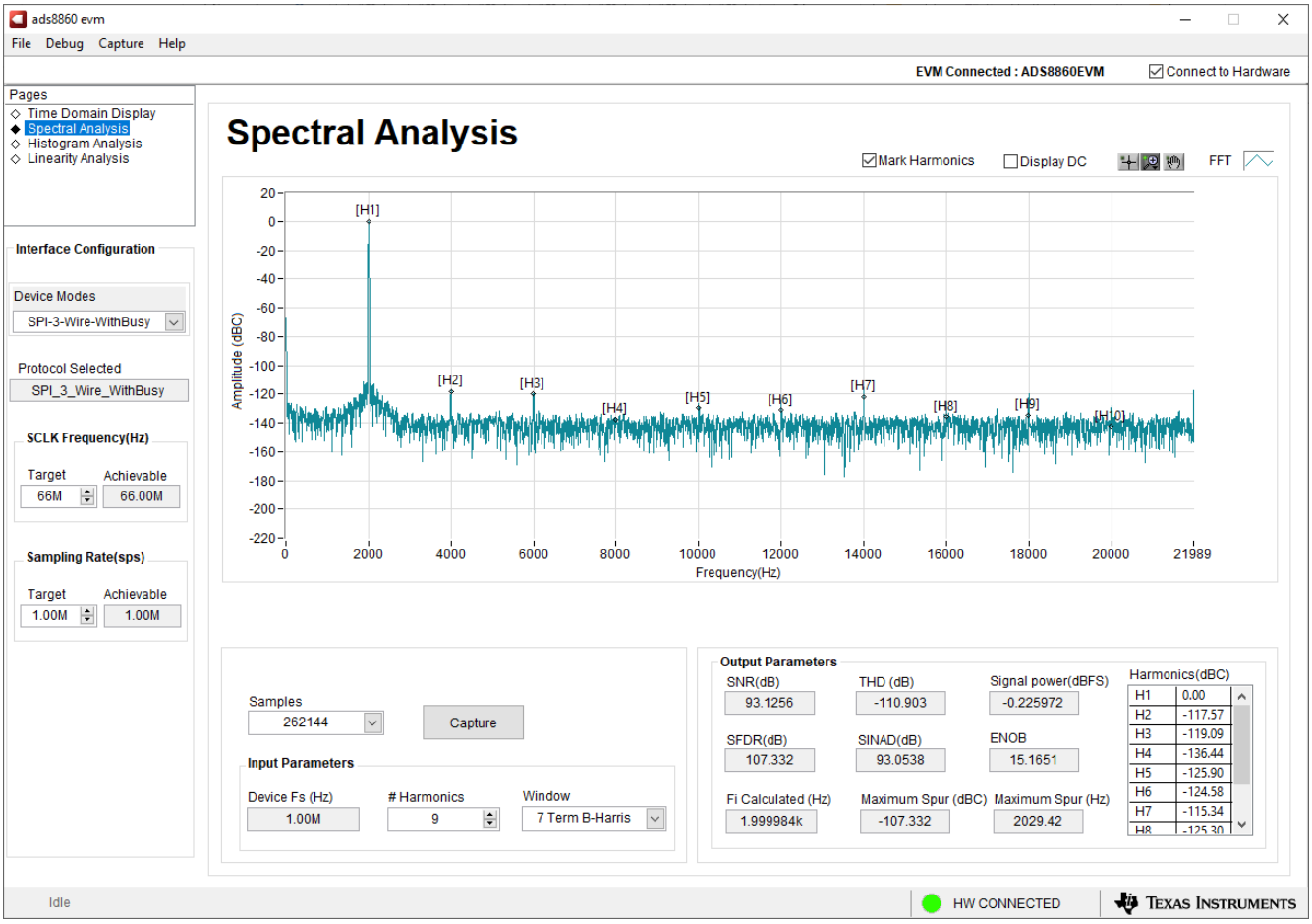


Figure 6-6. Spectral Analysis Tool

6.6 Histogram Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel. As shown in Figure 6-7, the histogram corresponding to a DC input is displayed on clicking the Capture button.

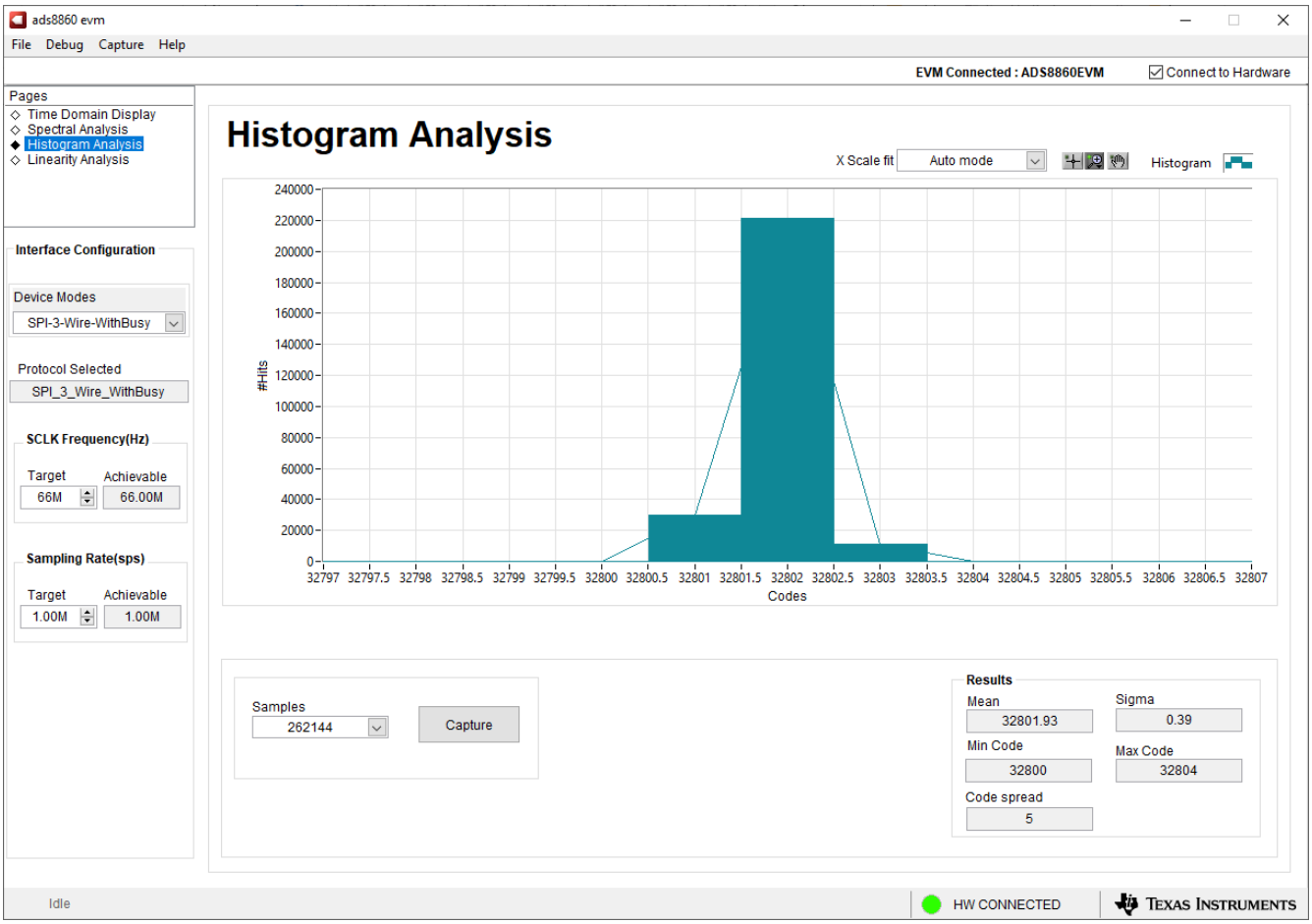


Figure 6-7. Histogram Analysis Tool

7 Bill of Materials, Schematics, and Layout

The bill of materials provided in Table 7-1 shows the PCB layouts for the ADS8860EVM.

7.1 Bill of Materials

Note

All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, refer to www.ti.com.)

Table 7-1. ADS8860EVM Bill of Materials

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
1	!PCB1	1		DC106	Any	Printed Circuit Board	
2	@H3, @H4	2		MPMS 002 0005 PH	BF Fastener Supply	MACHINE SCREW PAN PHILLIPS M2	
3	C1	1	0.01uF	C1608NP01H103J080AA	TDK	CAP, CERM, 0.01 uF, 50 V, +/- 5%, C0G/NP0, 0603	0603
4	C2, C3, C6, C11, C13, C33, C36, C39	8	1uF	C1608X7R1C105K	TDK	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	0603
5	C4, C5, C8, C9	4	10uF	CL21A106KAFN3NE	Samsung Electro-Mechanics	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	0805
6	C10	1	0.1uF	C0603C104K5RACTU	Kemet	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603
7	C12	1	22uF	CL21A226MAQNNNE	Samsung Electro-Mechanics	CAP, CERM, 22 uF, 25 V, +/- 20%, X5R, 0805	0805
8	C34, C35, C37, C38	4	47uF	C2012X5R1A476M125AC	TDK	CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 0805	0805
9	D1	1	3.6V	MMSZ4685T1G	ON Semiconductor	Diode, Zener, 3.6 V, 500 mW, SOD-123	SOD-123
10	D3, D4, D5	3	Green	APT2012LZGCK	Kingbright	LED, Green, SMD	LED_0805
11	H3, H4	2		9774050243R	Wurth Elektronik	ROUND STANDOFF M2 STEEL 5MM	ROUND STANDOFF M2 STEEL 5MM
12	J1	1		901-143-6RFX	Amphenol RF	JACK, SMA, 50 Ohm, Gold, R/A, TH	SMA Jack, 50 Ohm, R/A, TH
13	J2	1		QTH-030-01-L-D-A	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT
14	LBL1	1		THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch
15	R1	1	1.00k	RT0603BRB071KL	Yageo America	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603
16	R2, R3, R4, R5, R15	5	49.9	CRCW040249R9FKED	Vishay-Dale	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
17	R6, R43	2	10.0k	RT0402BRD0710KL	Yageo America	RES, 10.0 k, .1%, .0625 W, 0402	0402

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
18	R7, R16, R35, R36, R37, R38, R44, R45, R46	9	0	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603
19	R8, R9	2	10.0k	RC0603FR-0710KL	Yageo	RES, 10.0 k, 1%, 0.1 W, 0603	0603
20	R11	1	0.22	ERJ-3RQFR22V	Panasonic	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603
21	R12	1	120k	RC0603FR-07120KL	Yageo	RES, 120 k, 1%, 0.1 W, 0603	0603
22	R13, R14	2	24.9	CRCW060324R9FKEA	Vishay-Dale	RES, 24.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603
23	R33, R42	2	0.1	ERJ-3RSFR10V	Panasonic	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603
24	R39, R40, R41	3	6.65k	RC0603FR-076K65L	Yageo	RES, 6.65 k, 1%, 0.1 W, 0603	0603
25	S2	1		CAS-120TA	Copal Electronics	Switch, Slide, SPDT 100mA, SMT	Switch, 5.4x2.5x2.5mm
26	TP1, TP2, TP3, TP4, TP5, TP6, TP11, TP12, TP13	9		5001	Keystone	Test Point, Miniature, Black, TH	Black Miniature Testpoint
27	TP9, TP10	2		5005	Keystone	Test Point, Compact, Red, TH	Red Compact Testpoint
28	U1	1		ADS8860IDGSR	Texas Instruments	16 bit 1 MSPS, Serial, Pseudo-Differential Input, Micro Power, Miniature, SAR ADC, DGS0010A (VSSOP-10)	DGS0010A
29	U2	1		REF6050IDGKR	Texas Instruments	5ppm/C High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A
30	U3	1		BR24G32FVT-3AGE2	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8
31	U4	1		OPA320AIDBVR	Texas Instruments	Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV5), Green (RoHS & no Sb/Br)	DBV0005A
32	U9, U11	2		TPS7A4700RGWR	Texas Instruments	36V, 1A, 4.17µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A
33	U10	1		TPS3836K33DBVR	Texas Instruments	NanoPower Supervisory Circuits, DBV0005A (SOT-23-5)	DBV0005A
34	C7	1	1100pF	GRM1885C1E112JA01D	MuRata	CAP, CERM, 1100 pF, 25 V, +/-5%, C0G/NP0, 0603	0603
35	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	N/A
36	R10	0	0	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603

7.2 Board Layouts

Figure 7-1 and Figure 7-2 show the PCB layouts for the ADS8860EVM.

Note

Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS8860EVM PCBs.

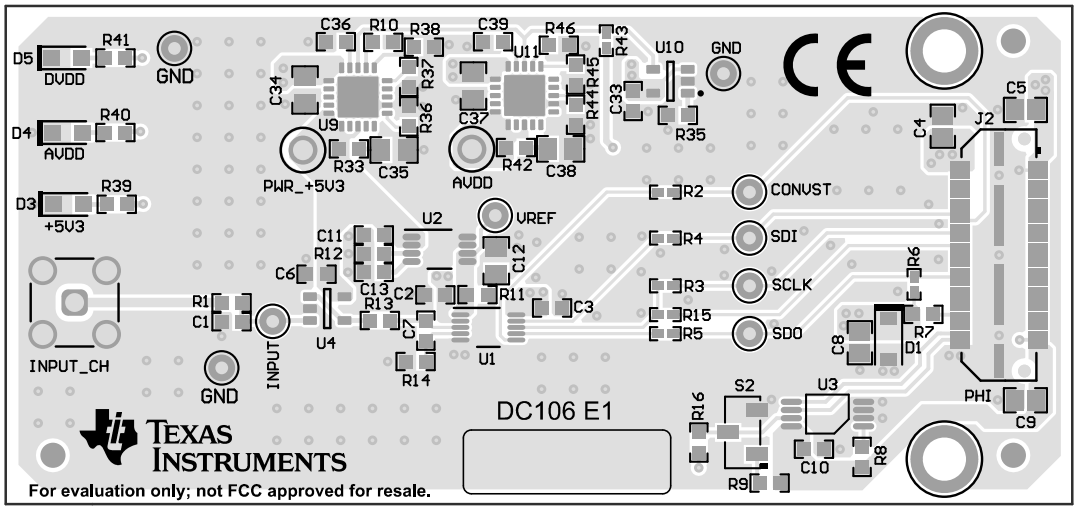


Figure 7-1. ADS8860EVM PCB: Ground Layer

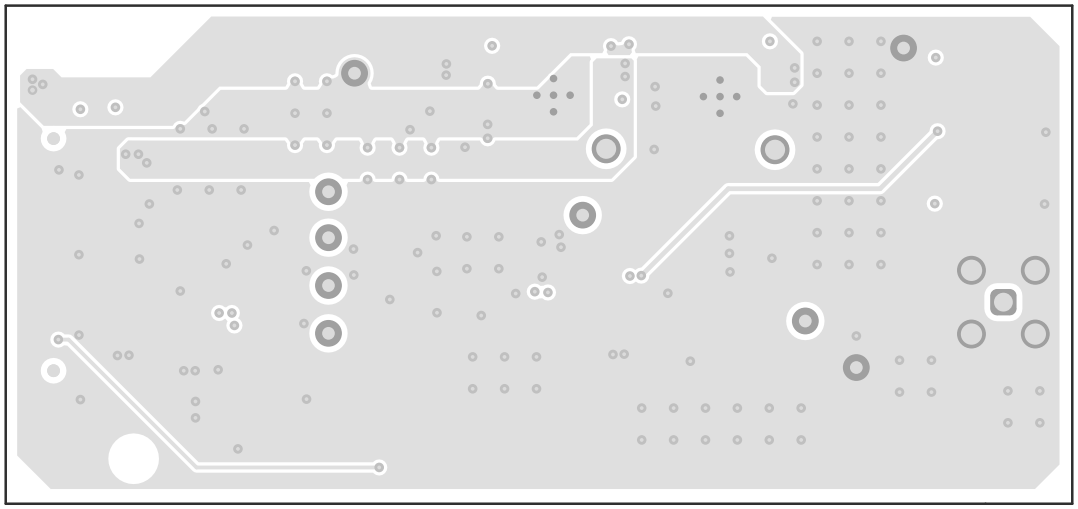
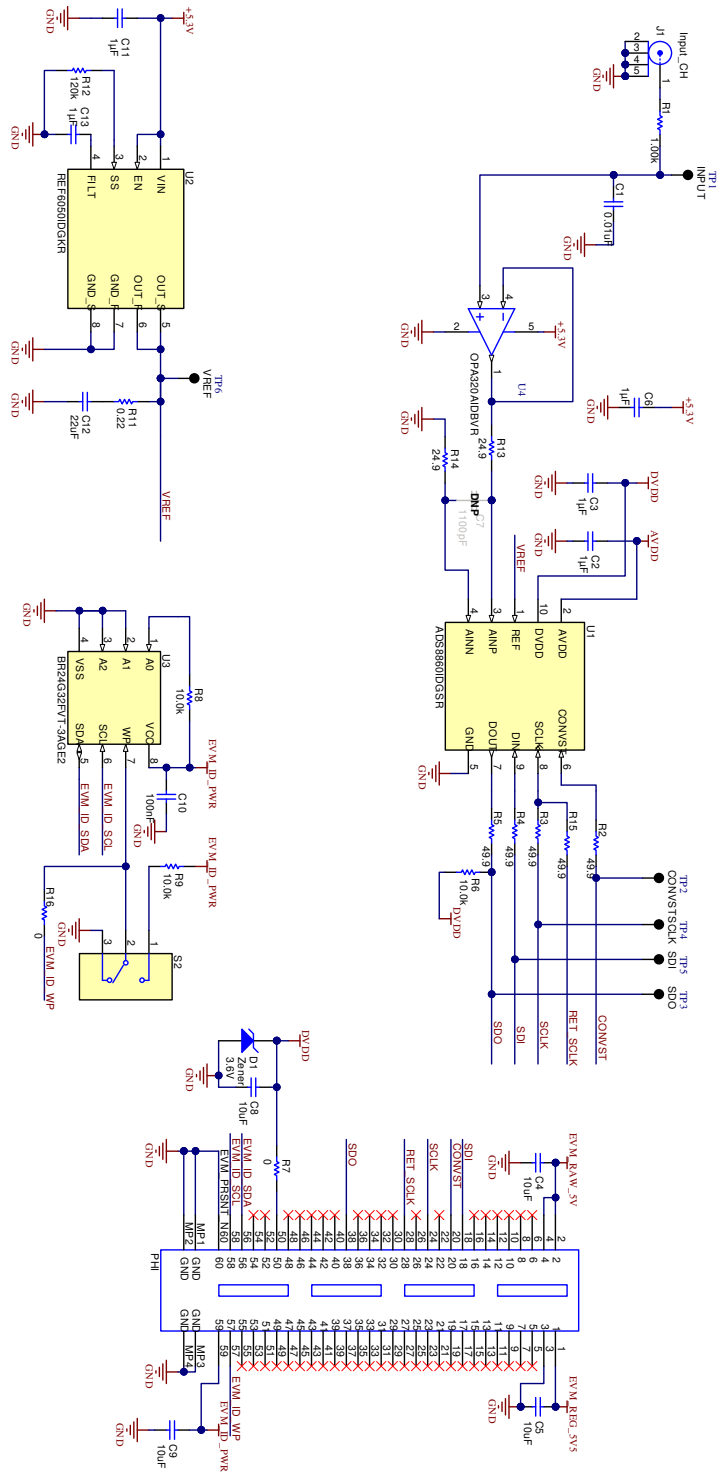
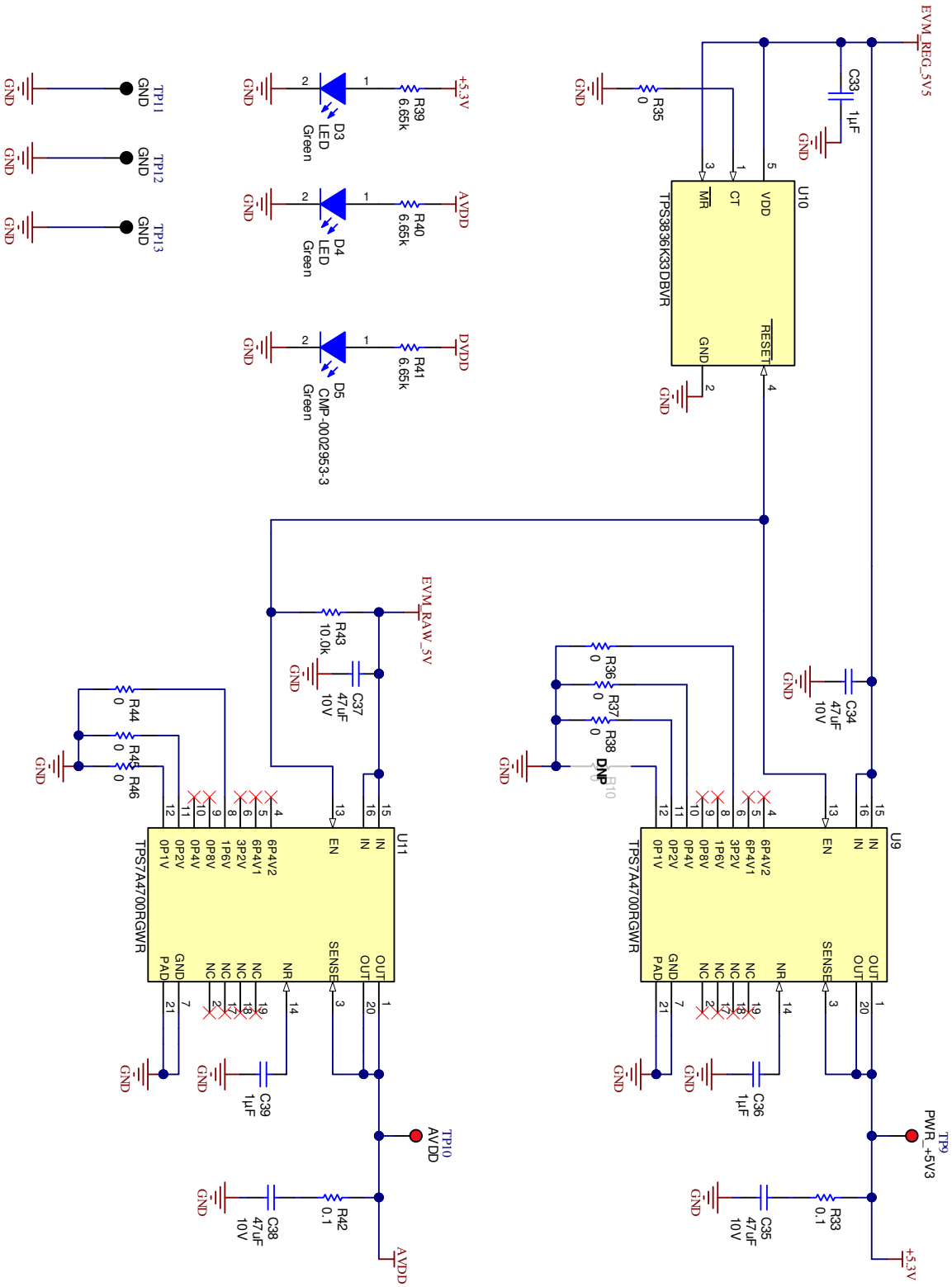


Figure 7-2. ADS8860EVM PCB: Bottom Layer (GND)

7.3 Schematics

This section provides the schematics for the ADS8860EVM.





8 Reference

- Texas Instruments: *OPAx320xPrecision,20-MHz,0.9-pA,Low-Noise,RRIO, CMOSOperationalAmplifierWith Shutdown Data Sheet*
- Texas Instruments: *REF60xxHigh-PrecisionVoltageReferenceWith IntegratedADC Drive Buffer Data Sheet*

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2013) to Revision A (July 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	3
• Changed document to reflect edits to the change in EVM controller platform	3

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