Application Report
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Power Supply Rejection to Noise in Sinusoidal Clock Buffers: CDC3S04

Mariajose Perez Ferrando *ICP/CTP*

ABSTRACT

This application report is an overview on how power supply noise affects some key specifications of the CDC3S04 sine wave buffer. The ripple in the power supply induces additional harmonics in the frequency spectrum and spurs in the phase noise plot, thus degrading the overall jitter and EMI performance. Decoupling capacitors significantly minimize these effects. This document provides guidelines to choose those decoupling capacitors.

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1 Introduction

When using switching power supplies, the switching frequency may not be completely filtered; if not, that tone causes a degradation of buffer performance. Typical frequencies for switching power supplies range from 10 kHz up to 2 MHz. For this reason, the ripple frequency was chosen in that band for measurements described in this document. On the other hand, when using linear regulators, the noise is not focused in one noise frequency.

This document shows how decoupling capacitors help to reduce the effect of noise in the power supply in the device's performance.

2 Power Supply Noise Rejection of CDC3S04

Power supply noise may induce spurs in the phase noise plot (deterministic jitter) as well as deteriorate the rms jitter in a given integration bandwidth. The power and frequency of the spur depends on the amplitude and frequency of the ripple in the supply, the CDC3S04 input clock, and the rejection of the CDC3S04 against that supply noise.

A typical clipped sine wave out of a TCXO (temperature-compensated crystal oscillator) was used for measurements. Figure 1 shows the spectral view of one of the signals used and also illustrates the EMI reduction of more than 20 dB when using a clipped sinusoidal or sinusoidal over a square wave signal.

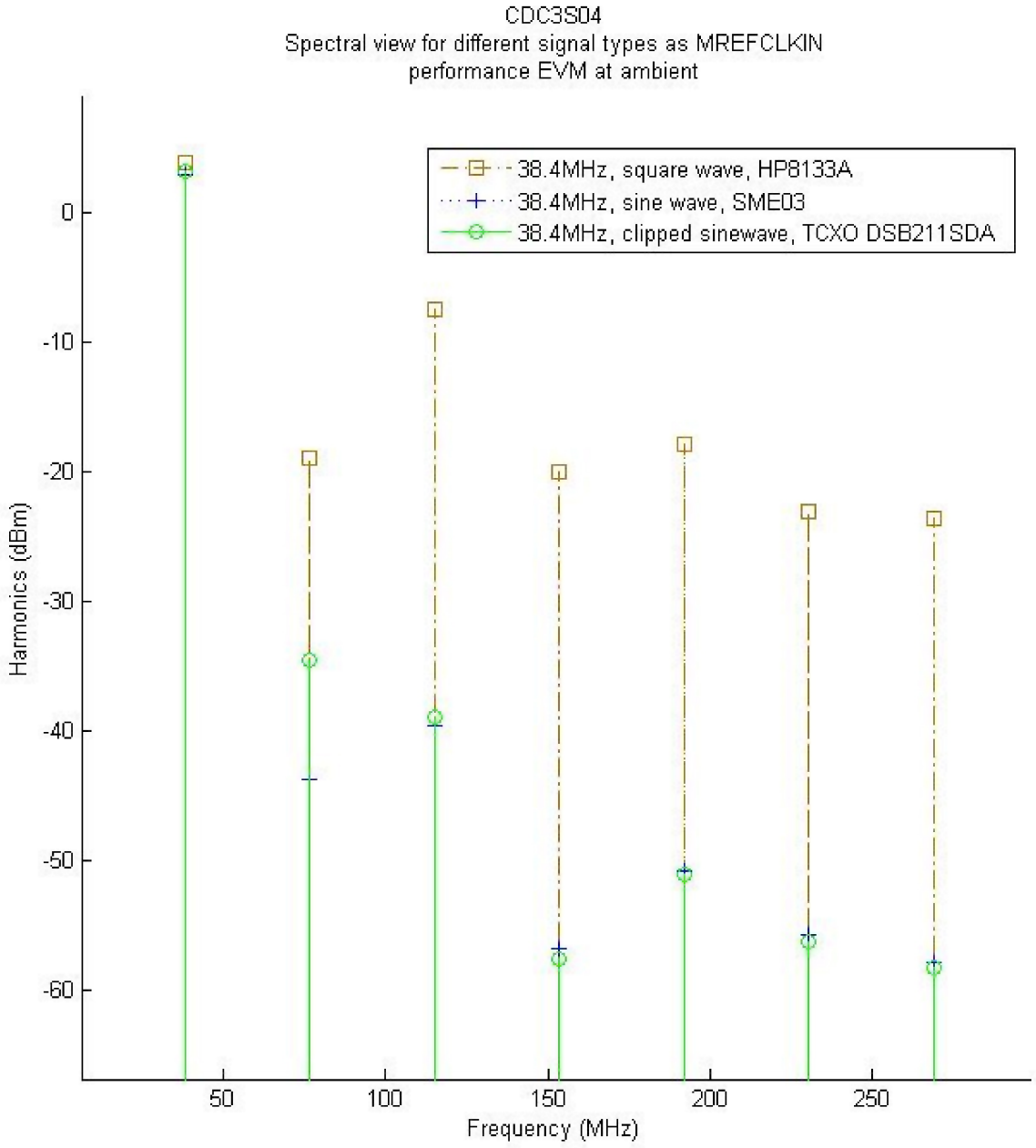

Figure 1. CDC3S04 Spectral View Comparison: Square Wave, Sine Wave, and Clipped-Sine Wave

The peak signal-to-noise ratio (PSNR) was measured with the Agilent E5052B SSA signal source analyzer setting the Spurious 'ON' in 'Power(dBc)' mode. When adding a sinusoidal ripple to the DC power supply, spurs are induced in the clock output's phase noise plot. As expected, the main spur (with the highest dBc) appears at the ripple's frequency. In Figure 2 can be seen how the biggest power spur depends on the ripple amplitude and the input clock characteristics of the CDC3S04 (frequency/slew rate). Each point on Figure 2's right plot represents the main spur measured by the E5052B (phase noise plot on the bottom left) at a specific ripple condition and MREFCLKIN frequency/type of signal (clipped sinusoidal).

The CDC3S04 presents worse PSNR the higher the slew rate is. Figure 3 shows both CLKIN signals in the time domain. As expected, the sinusoidal buffer is showing better noise immunity at slower edges, the opposite than from a standard LVCMOS clock buffer (i.e., the CDCV304, CDCLVC1104 present worse noise immunity at slower edges).

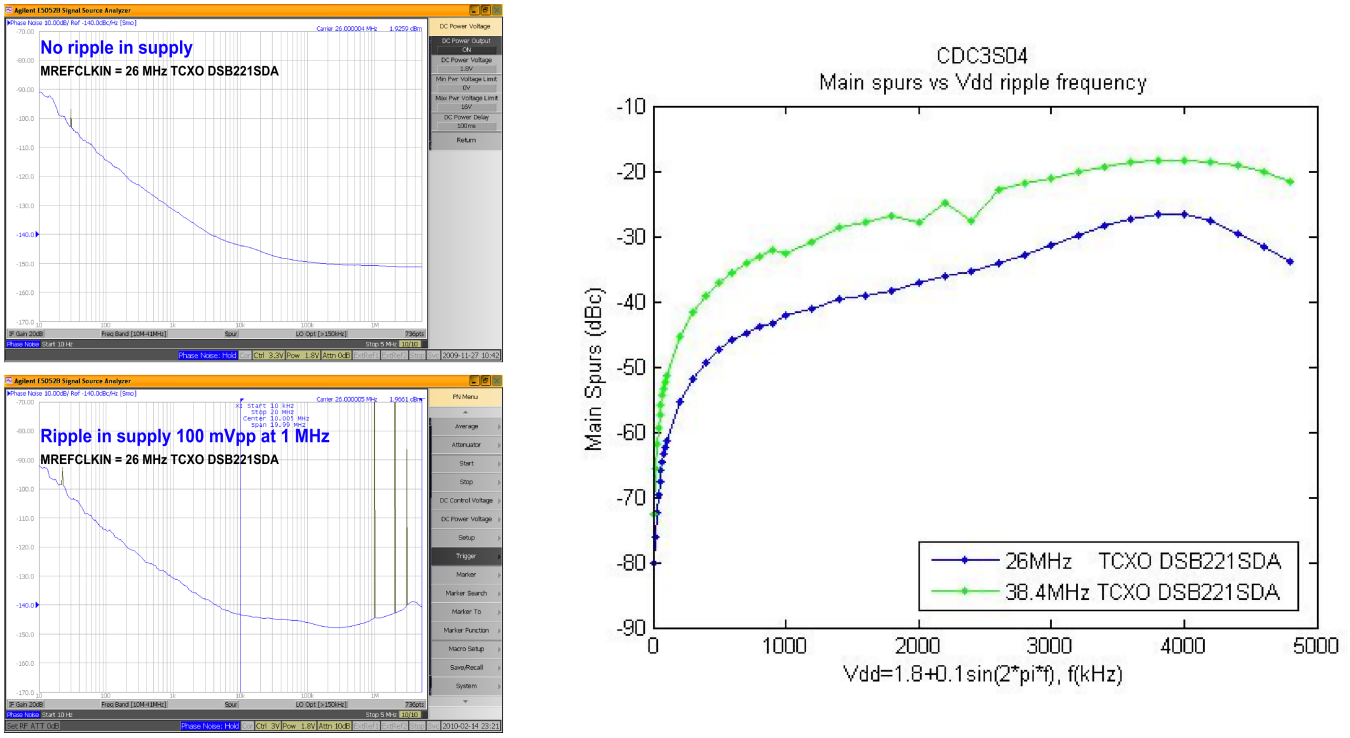

Figure 2. CDC3S04 Main Spurs, Vdd = 1.8-Vdc Signal + Variable-Frequency Sinusoidal

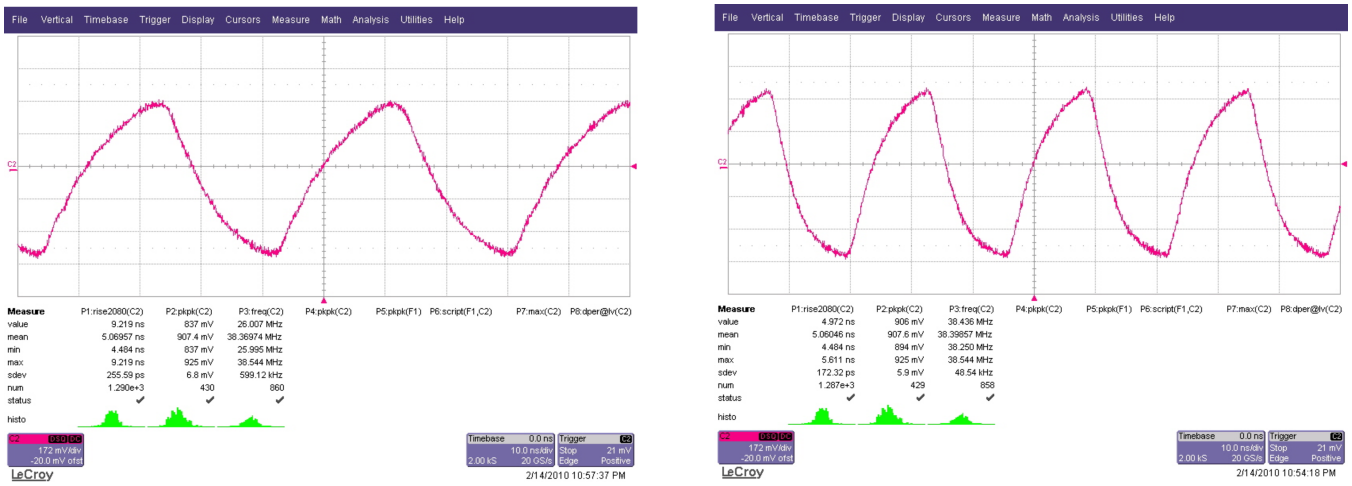

Figure 3. CLKIN to the CDC3S04, Left: 26-MHz TCXO DSB221SDA Oscillator, Right: 38.4-MHz TCXO DSB221SDA Oscillator

Figure 4 shows how the immunity to noise in the supply is smaller the greater is the amplitude of the supply ripple. This phenomenon can be seen at two different frequencies. Two phase noise plots are shown on the left, where can be seen not only the main spur represented on the left plot, but also the sub spurs, and how the ripple noise affects the rms jitter for an integration bandwidth. This is shown in more detail in Figure 5.

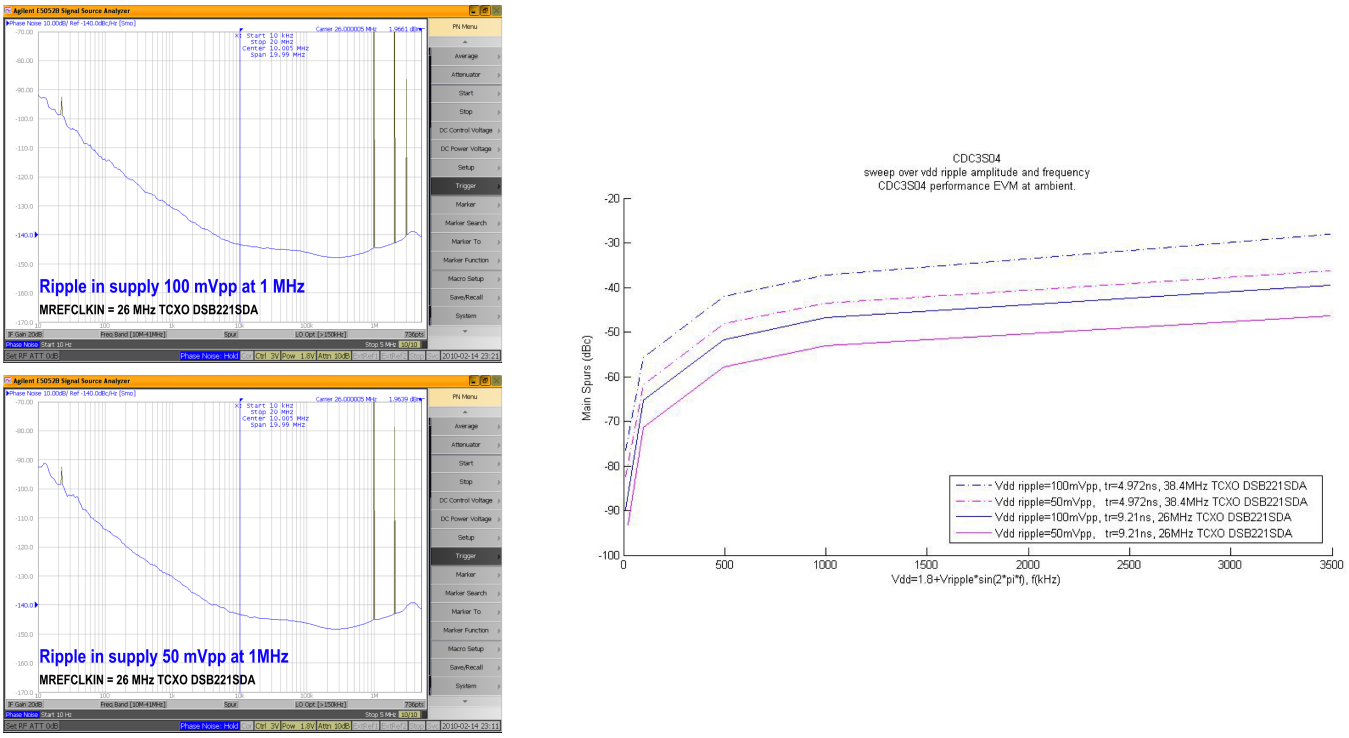

Figure 4. CDC3S04 Main Spurs Variance With Vdd Ripple Amplitude and Frequency, CLKIN = 26-MHz TCXO and 38.4-MHz TCXO DSB221SDA

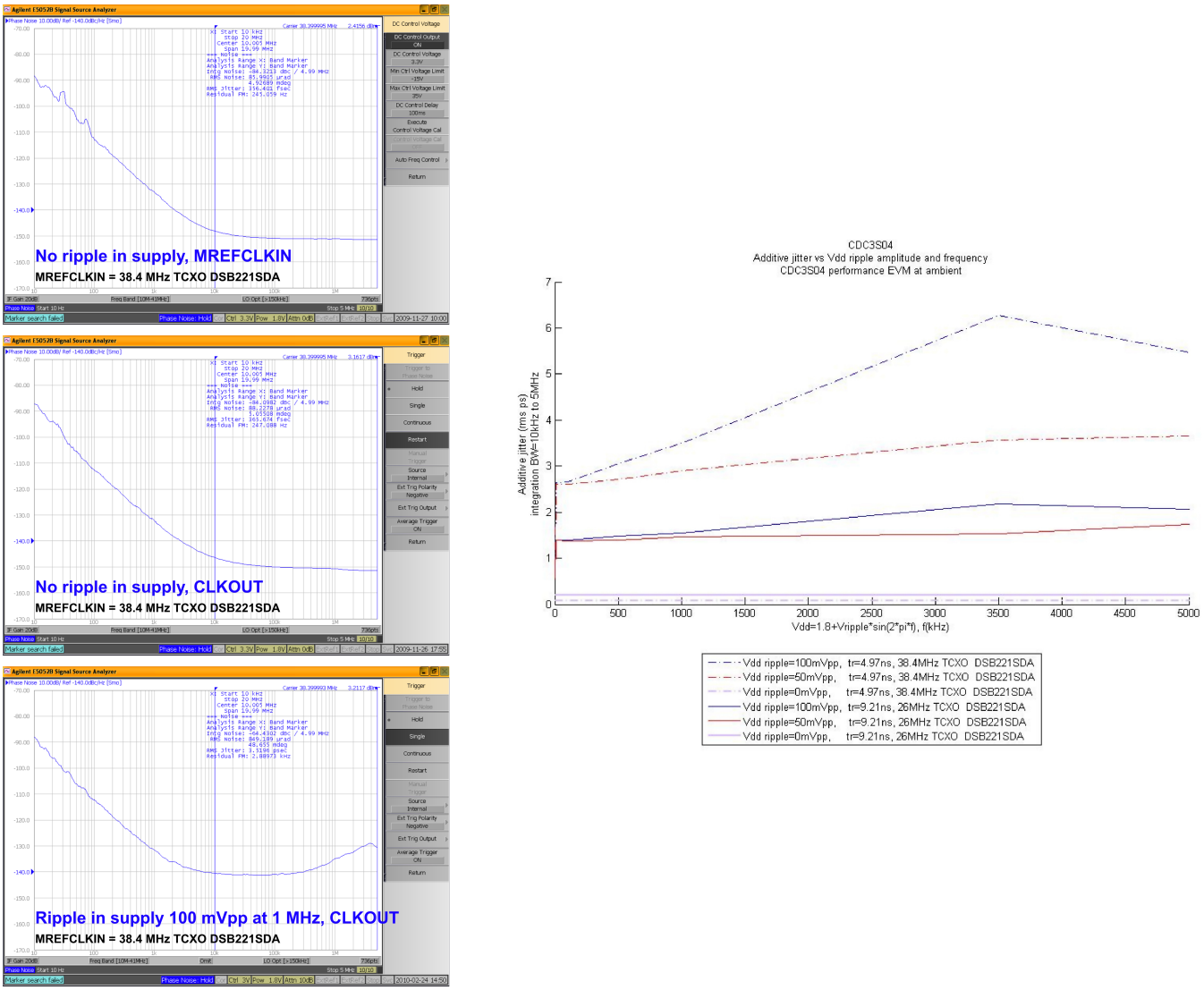

Figure 5. CDC3S04 Additive Jitter for Integration Bandwidth of 10 kHz to 5 MHz, Vdd Ripple Amplitude and Frequency Varied for Different Clock Inputs: 26-MHz TCXO and 38.4-MHz TCXO DSB221SDA

The ripple in the power supply degrades the additive jitter by worsening the rms jitter of the output clock for the integration bandwidth of interest, in Figure 5, IBW=10 kHz to 5 MHz. The additive jitter represents the rms jitter added by the buffer to the MREFCLKIN's rms jitter, calculated with the formula:

$$AJ(rms) = \sqrt{(Jrms^2_{CLKOUT} - Jrms^2_{MREFCLKIN})} \quad (1)$$

Additive jitter increases with the increase of the MREFCLKIN frequency, as expected from Figure 4 results.

Rms jitter (Jrms) is an integration of the phase noise on a specific bandwidth, and it is inversely proportional to the carrier frequency. For that reason, even when two different clock outputs present the same phase noise values, the rms jitter is worse for the clock output with the carrier at the lower frequency.

As can be seen in Figure 5, the higher frequency clock output presents the higher additive jitter and Jrms for the integration bandwidth from 10 kHz to 5 MHz.

The additive jitter with no ripple in the supply is better for the lower clock output. Therefore, Figure 5 compares them and shows that this situation is reversed by introducing noise in the power supply.

3 Choosing Decoupling Capacitors

Decoupling capacitors can be used to minimize the effect of the noise in the power supply that degrades the EMI, rms jitter, and deterministic jitter in the output clock.

These decoupling capacitors connected between Vdd and GND must be placed as close as possible to the CDC3S04 supply pins and laid out with short loops to reduce inductance. Then, some frequencies provide a very low impedance path for the supply noise. Their quantity and recommended values are detailed in this section.

A capacitor can be modeled as a parasitic resistance ESR (typical 0.1 Ω) in series with the ideal capacitor in series with a parasitic inductance ESL (typical 2 nH). At the resonation frequency, it behaves like a very low value resistor (ESR). After the resonation frequency, the capacitor behaves like an inductor. The lower the ESR, the higher is the attenuation at that frequency; therefore, choosing capacitors with the lowest ESR is recommended. Usually, the ceramic and tantalum type present the lowest ESR. Placing capacitors in parallel results in a summing of the individual capacitors' values and decreasing the overall parasitic ESR. Therefore, it is common practice to use instead one single capacitor of value C AND place in parallel n capacitors with C/n value; so, the effective ESR is ESR/n.

Ceramic multiple layer capacitors were used to attenuate the ripple noise in the measurements shown. Figure 6 shows how a big capacitor decouples low frequencies, and the smaller capacitor impacts high frequencies. Typical values are 22 µF or 10 µF (with lowest ESR) for the low frequencies and 0.1 µF (with lowest ESL) for the high frequencies. The 0.1-µF capacitor injects current to the IC while its outputs are switching until the power supply can recover. The large 22-µF or 10-µF capacitor recharges all the individual 0.1-µF capacitors. Figure 6 shows the CDC3S04 main spurs that are induced by sweeping the ripple in the power supply in frequency and amplitude by using different configurations of decoupling capacitors.

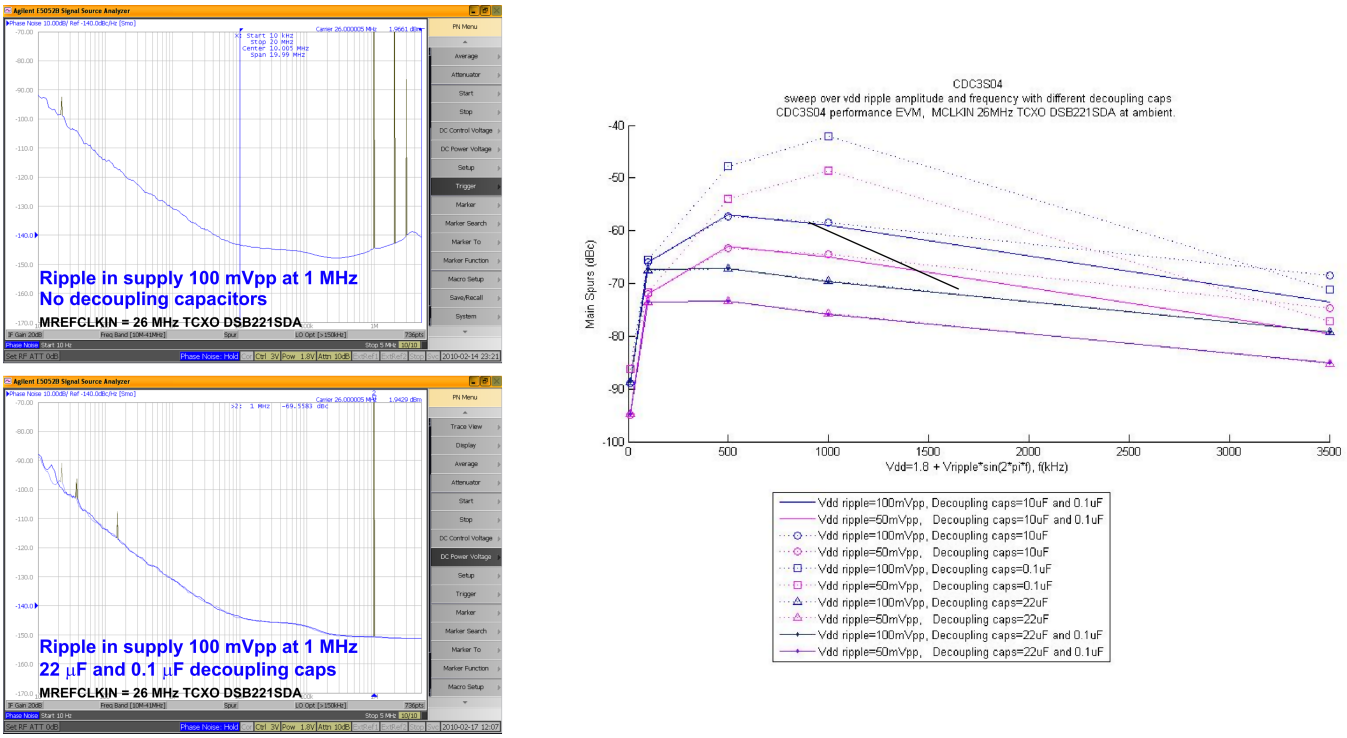

Figure 6. CDC3S04 Main Spurs

All the inducted spurs decrease their power at frequencies lower than 3.5 MHz by using only the big decoupling capacitor. The bigger this value is, the greater the attenuation. The phase noise plots on the left of Figure 6 show the worst case (biggest spur at ripple of 1-MHz frequency with 100-mVpp amplitude) without decoupling capacitors and with decoupling capacitors. The right plot of Figure 6 shows the impact on decoupling capacitors at different ripple conditions. Using a 22-µF decoupling capacitor or 22 µF plus 0.1 µF shows the same spur attenuation in the integration bandwidth.

Decoupling capacitors reduce EMI, as shown in Figure 7 and Figure 8. The top left and bottom left plots of Figure 7 show the spectrum when the CDC3S04 analog supply had a ripple of 100-mVpp amplitude and 1-MHz frequency with no decoupling capacitors and with decoupling capacitors (22 µF and 0.1 µF), respectively. The plot on the right was generated by the EVM board with and without decoupling capacitors when the reference clock was 38.4 MHz TCXO DSB221SDA. This plot shows both overlapping, where it is more visible of how the spurs are eliminated by the decoupling capacitors. The less the spurs are, the lower the EMI is.

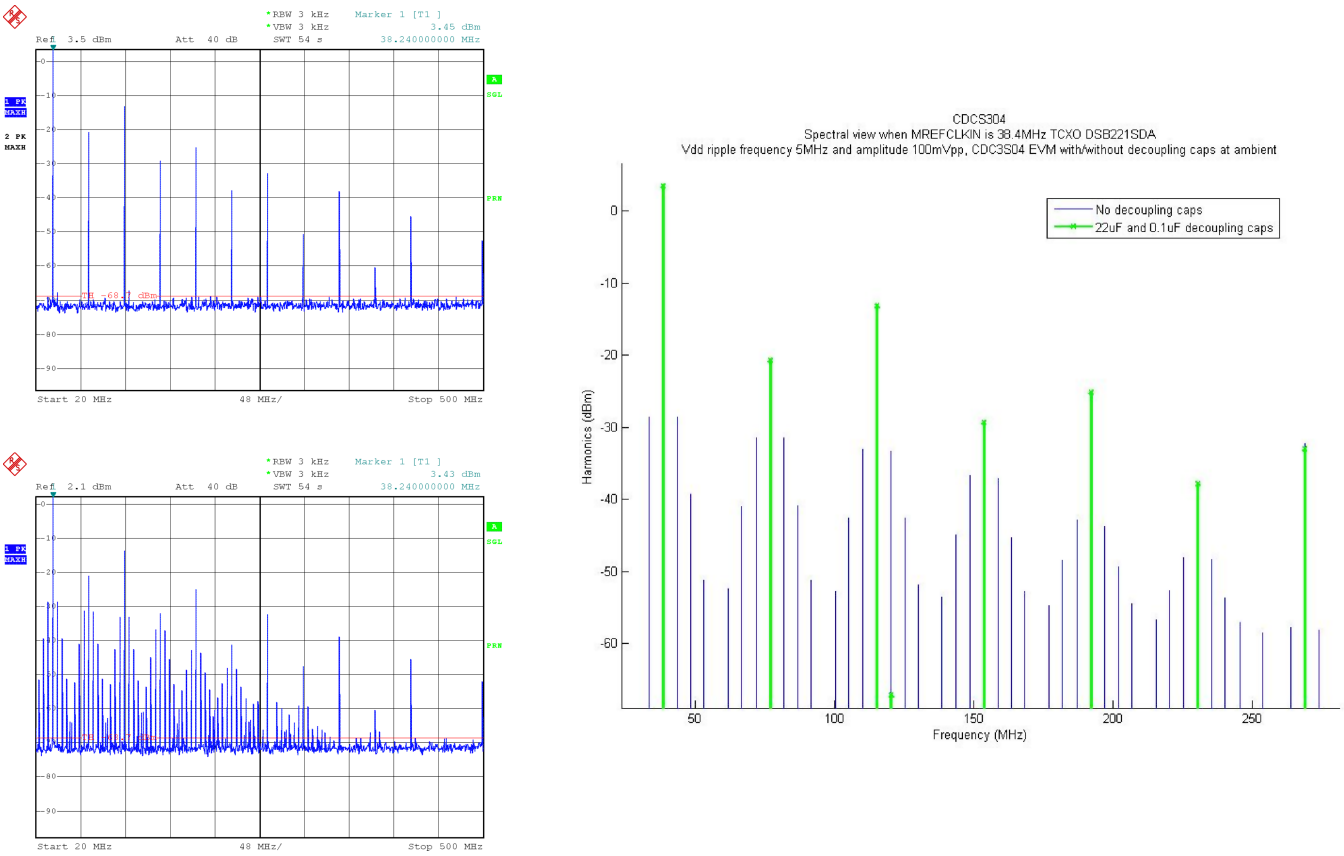

Figure 7. CDC3S04 Frequency Spectrum With Supply Ripple of 100-mVpp Amplitude and 5-MHz Frequency

In Figure 8, the plot was generated from the EVM board with and without decoupling capacitors when the reference clock was a 38.4 MHz TCXO DSB221SDA.

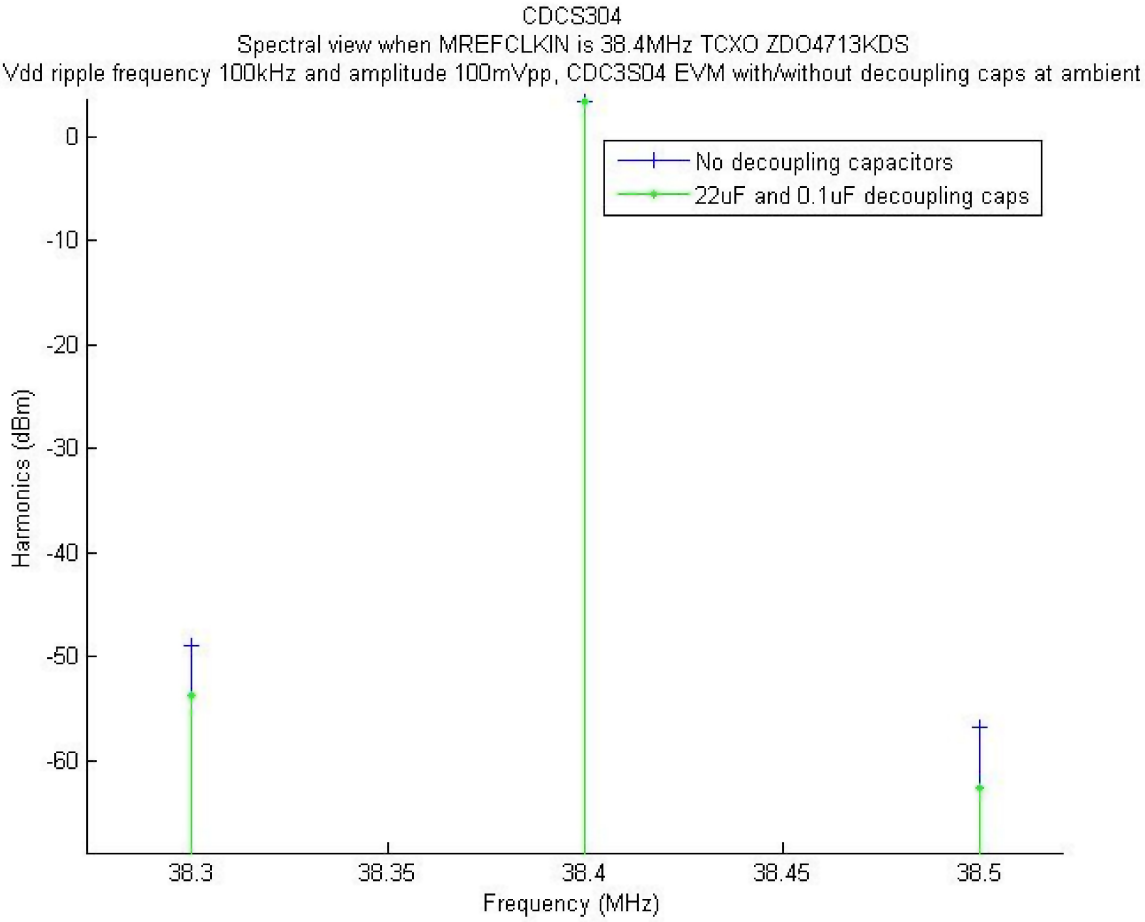

Figure 8. CDC3S04 Frequency Spectrum With Supply Ripple of 50-mVpp Amplitude and 100-kHz Frequency

Additive jitter is also improved considerably as well as the power of the spurs at the supply's ripple frequency. When using the big-value capacitor and ripple is in the supply, the additive jitter is almost the same as if no ripple were in the supply in the integration bandwidth of interest.

Figure 9 shows CDC3S04 additive jitter when sweeping the ripple in the power supply in frequency and amplitude. The left plot of Figure 9 was generated using different configurations of decoupling capacitors; the right plot is the zoomed plot.

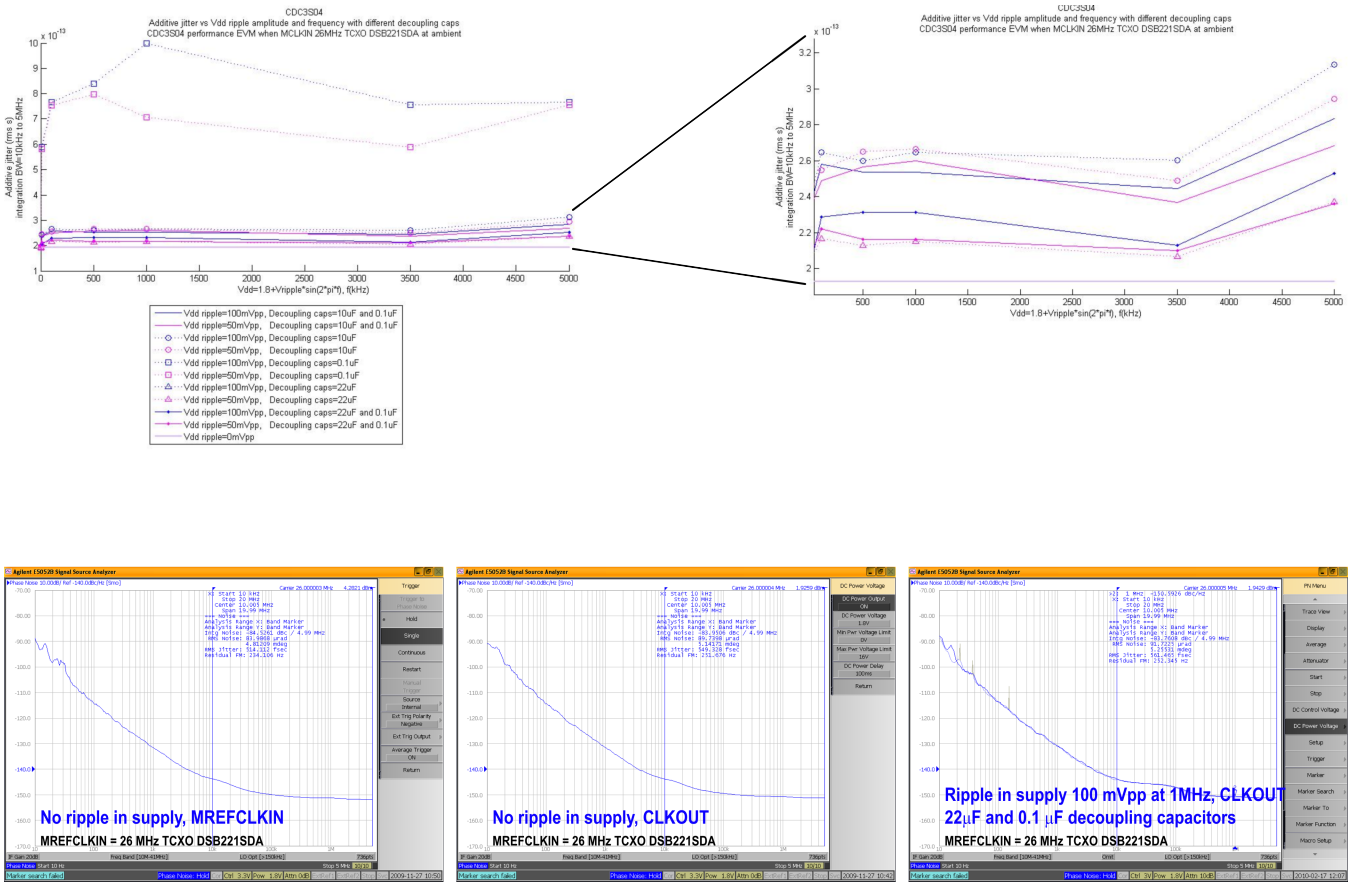

Figure 9. CDC3S04 Additive Jitter When Sweeping the Ripple in the Power Supply in Frequency and Amplitude

4 References

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3. *Introduction to Choosing MLC Capacitors For Bypass/Decoupling Applications*, Yun Chase, AVX
4. *Assess Power-Supply Noise Rejection in Low-Jitter PLL Clock Generators*, Sharon Wang and John Abcarius, Maxim AN 4457
5. TCXO DSB221SDA 26.000 MHz: KDS part number 1XXB26000CLA
6. TCXO DSB211SDA 38.400 MHz: KDS part number 1XXD38400CAA

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