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Texas Instruments Enhanced Plastic Products Reliability Report

(Subject To Attached Disclaimers)

Device Type/Device Family:	UCC2895MDWREP
Package Type:	20 Pin SOIC (Ti Designator DW)
Wafer Fabrication Facility:	SFAB
Assembly/Test Facility:	Carsem
Compiled:	10/11

Biased Life Test

Test Method:	JESD22-A108
Test Condition:	150°/500 hours or equivalent
Sample Size:	4010
Rejects:	0
Activation Energy (eV):	.7
Equivalent Device Hours:	7.519E7
Failure Rate (FIT)*:	13.3

*Derated to +55°C with a 60% Confidence Level

Note: Data for EP product is specific to device technology and foundry. For this reason the FIT rate above may differ from Ti's external web page. This does not reflect a difference in quality but only a difference in sample size.

Package Related Tests

Description	Condition	Referenced Method	Sample Size/Rejects	
Biased Humidity or HAST**	85°C / 85% / 1000 hours or **130°C / 85% / 96 hours**	JESD22-A101 JESD22-A110	308/0	*
Autoclave	121 °C @ 2 atmospheres absolute for 96 hours	JESD22-A102	231/0	*
Temperature Cycle	-65 °C to +150 °C non-biased for 1000 cycles	JESD22-A104	303/0	*
High Temp Storage	**170 °C / 420 hours**	JESD22-A103-A	77/0	*

* Preconditioning per JEDEC Std. 22, Method A112/A113

** This device has been qualified to the elevated standard of 250 Hrs 130/85 HAST (Highly Accelerated Stress Test). This qualification level surpasses JEDEC requirements.

Initial Product Qualification

The subject Enhanced Plastic device, device family, and/or package family have passed Texas Instruments product qualification as follows:

Description	Condition	Sample Size	Referenced Method	
Electrical Characterization	TI Data Sheet	50 units/lot	N/A	
Electrostatic Discharge Sensitivity	HBM MM	3 units/voltage	EIA/JESD22-A114 EIA/JESD22-A115	
Latch-up	Per Technology	5/0 units/lot	EIA/JESD78	
Physical Dimensions	TI Data Sheet	5/0	EIA/JESD22- B100	
Thermal Impedance	Theta-JA on board	Per Pin-Package	EIA/JESD51	
Bias Life Test	125°C / 1000 hours or equivalent	116/0	JESD22-A108	*
Biased Humidity	85°C / 85% / 1000 hours	77/0	JESD22-A101	*
HAST	or 130°C / 85% / 96 hours		JESD22-A110	
Autoclave	121 °C @ 2 atmospheres absolute for 96 hours	77/0	JESD22-A102	*
Temperature Cycle	-65 °C to +150 °C non-biased for 1,000 cycles	77/0	JESD22-A104	*
Solder Heat	260 °C for 10 seconds	22/0	JESD22-B106	
Resistance to Solvents	Ink symbol only	12/0	JESD22-B107	
Solderability	Condition A (steam age for 8 hours)	22/0	ANSI/J-STD-002-92	
Flammability	Method A / Method B	5/0	UL-1964	
Bond Strength	-	76/0 wires	ASTM F-459	
Die Shear	-	5/0	MIL-STD-883 Method 2019	
High Temp Storage	150 °C / 1,000 hours	45/0	JESD22-A103-A	*
Moisture Sensitivity	Surface Mount Only	12/0	J-STD-020-A * Precondition performed	

Supplemental Device Characteristics

Device Type:

Die Revision:	-	Assembly Site:	CRS
Master Die:	SMSAN2895IS	Package Type:	SOIC (DW)
Wafer Fab:	SFAB	Pin Count:	20
Fab Technology:	CMOS	Mold Compound:	Sumitomo G600C
Fab Process:	IMP-PWR2	Mount Compound:	Ablestik 8290
Process Code:	N/A	Bond:	1.3 mil Au
Passivation:	Nitride	Lead Composition:	Cu
Metal 1:	AlCu2	Lead Finish:	NiPdAu
Metal 2:	TiW/AlCu2	Die Size:	128.7 X 70.5 Mils

Quality and Reliability Data Disclaimer

The attached quality and reliability information is specific to the TI Enhanced Plastic product family of plastic encapsulated commercial-off-the-shelf (COTS) semiconductor products and components. Due to possible differences in product assembly and test baselines, this information is NOT APPLICABLE to TI standard, industrial, or automotive catalog commercial products.

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