

TMUX73XXF Evaluation Module

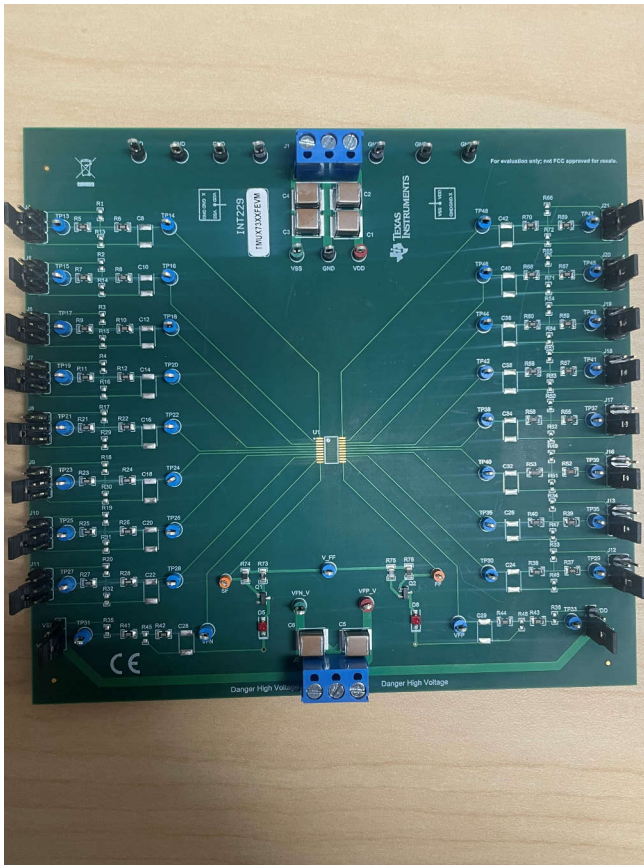


Description

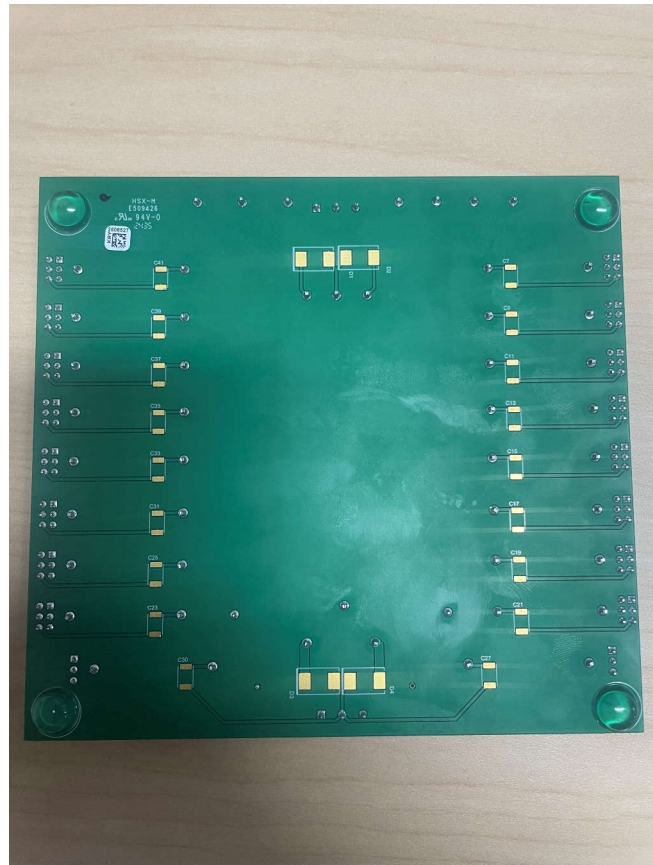
This user guide outlines the TMUX73XXF evaluation module (EVM) and its intended applications. This board facilitates rapid prototyping and DC characterization of Texas Instruments' TMUX73XXF series of components in the TSSOP (PW) package. Additionally, it features onboard test points that provide the flexibility to test various signals.

Features

- 2 power supply decoupling capacitors from VDD to GND ($2 \times 3.3 \mu\text{F}$; $2 \times 1 \mu\text{F}$)
- 2 power supply decoupling capacitors from VSS to GND ($2 \times 3.3 \mu\text{F}$; $2 \times 1 \mu\text{F}$)
- Protection diode pads are available near VDD and VSS input.
- $3.3\mu\text{F}$ supply decoupling capacitor to Ground on both VFP_V and VFN_V supplies
- Terminal block power supply connection
- DUT footprint compatible with 16-pin PW (TSSOP), and 20-pin PW (TSSOP) packages
- 16 length-matched signal inputs
- Terminal block OVP Triggering Threshold supply connection
- General and Specific Fault Indicator Flag LED circuits included on EVM
- Selectable connections to VDD, VSS, or GND for each signal input using a 2.54 mm shunt
- Footprints for pull-up and pull-down resistors for each signal input (on each of 16 signals and 2 OVP Trigger Thresholds)
- Footprints for series resistors for each signal input (on each of 16 signals and 2 OVP Trigger Thresholds)
- Footprints for decoupling capacitors for each input (footprint on each of 16 signals and 2 OVP Trigger Thresholds)
- 2 test points for each signal and OVP Trigger Thresholds
- Multiple GND test point connections around the board



TMUX73XXF-EVM (Front Side)



TMUX73XXF-EVM (Back Side)

1 Evaluation Module Overview

1.1 Introduction

This user guide describes the TMUX73XXF-EVM evaluation module (EVM) and its intended use. This board allows for the quick prototyping and characterization of TI's TMUX73XXF multiplexers.

1.2 Kit Contents

The EVM kit includes the following:

1. TMUX73XXF-EVM board

1.3 Specification

The TMUX73XXF-EVM features two test points for each I/O and OVP Trigger Threshold, resulting in thirty-four test points available for testing the TMUX73XXF line of devices. Seven extra ground test points are included to facilitate easier board testing.

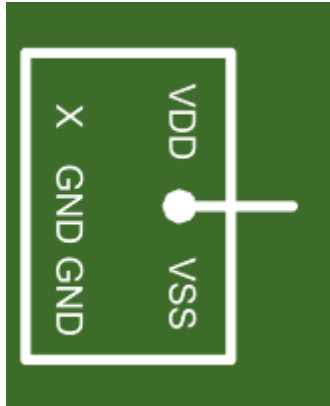
2 Hardware

2.1 Power Requirements

The TMUX73XXF-EVM requires a power supply connected either through the J1 terminal or directly to the red VDD test point. This setup establishes a passive signal pathway between the Sx and Dx pins based on the selected logic. When testing TMUX734XF devices, the Fault Indicator Flag LED circuits can be activated by applying a voltage to the V_FF pin. Additionally, the Over Voltage Protection (OVP) Trigger Thresholds can be powered using either the J2 terminal or the VFP_V and VFN_V pins.

2.2 Setup

1. All 16 generic signal pathway headers contain six pins. [Figure 2-1](#) and [Figure 2-2](#) show the generalized pinout of the headers for the left and right sides of the board respectively. Note that the orientation is based on J1 being on the top of the board.



2.

Figure 2-1. Left Side Jumper (J4-J11) Configuration or Pinout

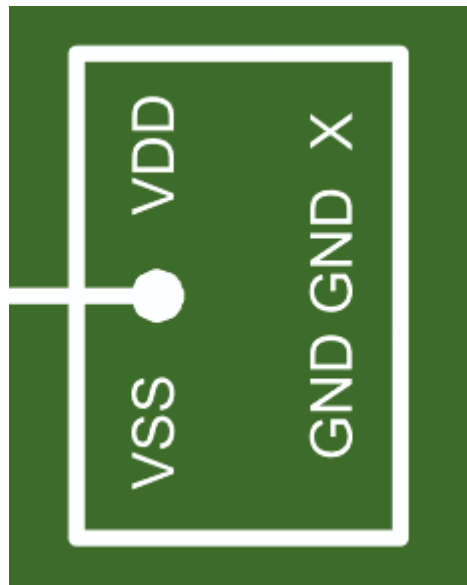


Figure 2-2. Right Side Jumper (J12,13,J16-J21) Configuration or Pinout

2.3 Jumper Information

For the left side header, pin 1 is at the top left corner pin (denoted as an X). The right side header has pin 1 (denoted as an X), which is at the top right corner. [Table 2-1](#) shows the jumper configurations. Note: U1 refers to the signal pathway that connects to the U1 TMUX73XXF footprint.

Table 2-1. Jumper Pinout Map

Jumper ID	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6
J4	Floating	VDD	GND	U1 Pin 1	GND	VSS
J5	Floating	VDD	GND	U1 Pin 2	GND	VSS
J6	Floating	VDD	GND	U1 Pin 3	GND	VSS
J7	Floating	VDD	GND	U1 Pin 4	GND	VSS
J8	Floating	VDD	GND	U1 Pin 5	GND	VSS
J9	Floating	VDD	GND	U1 Pin 6	GND	VSS
J10	Floating	VDD	GND	U1 Pin 7	GND	VSS
J11	Floating	VDD	GND	U1 Pin 8	GND	VSS
J12	Floating	VDD	GND	U1 Pin 13	GND	VSS
J13	Floating	VDD	GND	U1 Pin 14	GND	VSS
J14	VSS	U1 Pin 9	VFN_V	N/A	N/A	N/A
J15	VDD	U1 Pin 12	VFP_V	N/A	N/A	N/A
J16	Floating	VDD	GND	U1 Pin 15	GND	VSS
J17	Floating	VDD	GND	U1 Pin 16	GND	VSS
J18	Floating	VDD	GND	U1 Pin 17	GND	VSS
J19	Floating	VDD	GND	U1 Pin 18	GND	VSS
J20	Floating	VDD	GND	U1 Pin 19	GND	VSS
J21	Floating	VDD	GND	U1 Pin 20	GND	VSS

Check the device-specific data sheet for the pin-out. For power (VDD or VSS) and ground (GND), lines connect shunts on the appropriate jumpers to short the U1 pin to the respective VDD, VSS, or GND line. For testing where control pins do not change state (such as the select or enable pin always being at a logic '1' for the duration of testing), shunts can be connected on the appropriate jumpers to short the U1 control pins to VDD or GND. For the remaining I/O pins (VDD, VSS, and GND), signals can be applied using shunts in the same manner as before or the shunt can be removed and an external signal can be applied to the U1 pin of the jumper or the respective test point.

In cases where the tests require pull-up or pull-down resistors versus directly attaching the source to the respective U1 pin, all 16 generic pathways contain 0603 resistor pads to add these components. [Table 2-2](#) shows the IDs.

During the evaluation of TMUX734X devices, it is recommended to use the shunts on J14 and J15 to connect the multiplexer's VFP and VFN pins to the desired VFP/VFN threshold voltage. The VFP_V and VFN_V threshold supplies can be either powered through the J2 terminal block or connected directly to the VFP_V and VFN_V test points. Additionally, the fault flag voltage (VFF_V) can be connected and powered through the V_FF blue test point.

Table 2-2. Pull-Up or Pull-Down Resistor Configuration Map

0603 Sized Resistor Pad ID	Jumper ID	Function
R1	J4	Pull up
R13	J4	Pull down
R2	J5	Pull up
R14	J5	Pull down
R3	J6	Pull up
R15	J6	Pull down
R4	J7	Pull up
R16	J7	Pull down
R17	J8	Pull up
R29	J8	Pull down
R18	J9	Pull up
R30	J9	Pull down
R19	J10	Pull up
R31	J10	Pull down
R20	J11	Pull up
R32	J11	Pull down
R33	J12	Pull up
R46	J12	Pull down
R34	J13	Pull up
R47	J13	Pull down
R35	J14	Pull Up
R45	J14	Pull down
R36	J15	Pull Up
R48	J15	Pull down
R49	J16	Pull Up
R61	J16	Pull down
R50	J17	Pull Up
R62	J17	Pull down
R51	J18	Pull Up
R63	J18	Pull down
R54	J19	Pull Up
R64	J19	Pull down
R65	J20	Pull Up
R71	J20	Pull down
R66	J21	Pull Up
R72	J21	Pull down

Now loads can be attached to the board. If a pull-down pad was unused, then this pad can now be used as a pad for a resistive load. There are also pads for capacitive loads for each of the 16 generic signal paths and 2 OVP Trigger Thresholds that can also be utilized. [Table 2-3](#) shows the corresponding pad and jumper IDs.

Note

The 1812-sized capacitor pads are on the bottom side of the EVM.

Table 2-3. RC Load Configuration Map

Jumper ID	0603 Sized Resistor Pad ID	1206 Sized Capacitor Pad ID	1812 Sized Capacitor Pad ID
J4	R13	C8	C7
J5	R14	C10	C9
J6	R15	C12	C11
J7	R16	C14	C13
J8	R29	C16	C15
J9	R30	C18	C17
J10	R31	C20	C19
J11	R32	C22	C21
J12	R46	C24	C23
J13	R47	C26	C25
J14	R45	C28	C27
J15	R48	C29	C30
J16	R61	C32	C31
J17	R62	C34	C33
J18	R63	C36	C35
J19	R64	C38	C37
J20	R71	C40	C39
J21	R72	C42	C41

Now that the loading is complete for the board, additional supply decoupling capacitance to ground can be added for the VDD or VSS lines. [Table 2-4](#) shows the power supply decoupling capacitance for each VDD or VSS line. If the default capacitance is enough, then move on to step 8.

Table 2-4. Capacitors

Capacitor Pad ID	Pad Size (LxW)	Associated Power Signal
C1	6mm × 5mm	VDD
C2	6mm × 5mm	VDD
C3	6mm × 5mm	VSS
C4	6mm × 5mm	VSS

Finally, attach the supply signals (VDD, GND, or VSS) to the appropriate pins of the terminal block labeled J1. Power is now ready to be applied to the board. For test points, please see the next section.

2.4 Test Points

There are multiple test points (48) on the board that can be used to either measure the associated trace or apply external signals for testing purposes. [Table 2-5](#) shows the test points for the sixteen generic U1 connections and 2 OVP Trigger Thresholds. There are two test points per pin of the IC, which are colored blue.

Table 2-5. Test Points for Jumpers Map

Jumper ID	Test Point ID	Test Point ID	U1 Pin
J4	TP13	TP14	1
J5	TP15	TP16	2
J6	TP17	TP18	3
J7	TP19	TP20	4
J8	TP21	TP22	5
J9	TP23	TP24	6
J10	TP25	TP26	7
J11	TP27	TP28	8
J12	TP29	TP30	13
J13	TP35	TP36	14
J14	TP31	VFN	9
J15	TP33	VFP	12
J16	TP39	TP40	15
J17	TP37	TP38	16
J18	TP41	TP42	17
J19	TP43	TP44	18
J20	TP45	TP46	19
J21	TP47	TP48	20

Test points also connect to VSS, VDD, and GND planes. In addition, there are test points for the fault flag indicator led circuits and OVP Trigger Thresholds.

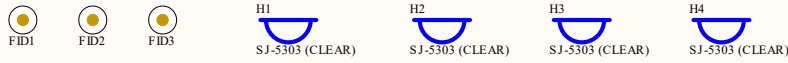
[Table 2-6](#) shows these test points.

Table 2-6. Test Points

Test Point ID	Color	Signal
VDD	Red	VDD
GND	Black	GND
VSS	Green	VSS
VFP_V	Red	VFP Threshold Supply
VFN_V	Green	VFN Threshold Supply
V_FF	Blue	Fault Flag Indicator Led Circuits Supply
SF	Orange	Specific Fault Flag
FF	Orange	General Fault Flag

3 Hardware Design Files

3.1 Schematics



PCB Number:
PCB Rev:

PCB LOGO
Texas Instruments



PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

LBL1
PCB Label
THF-14-423-10
Size: 0.65" x 0.20 "

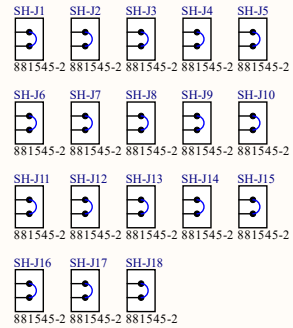
ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

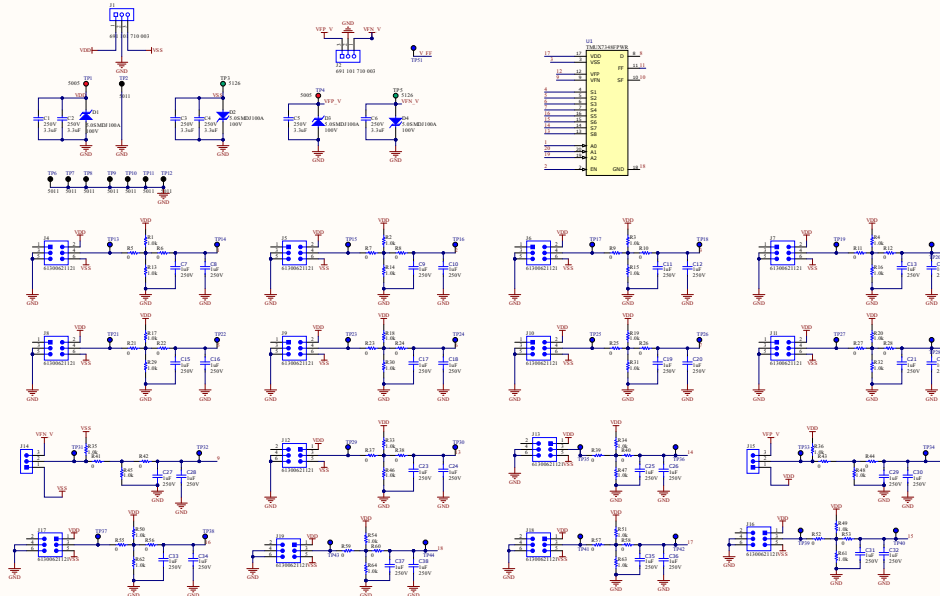
ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

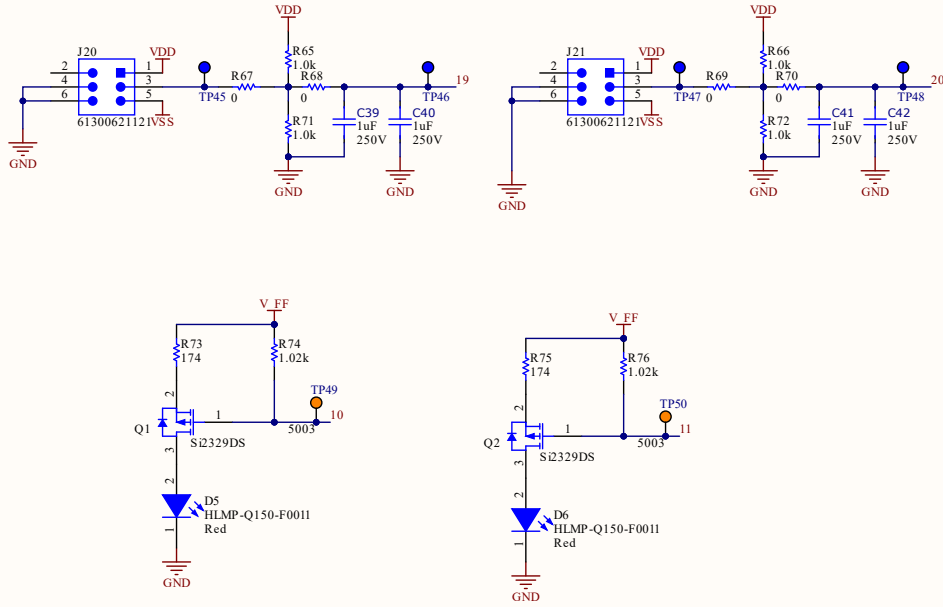
ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Variant/Label Table	
Variant	Label Text
001	TMUX73XXF EVM



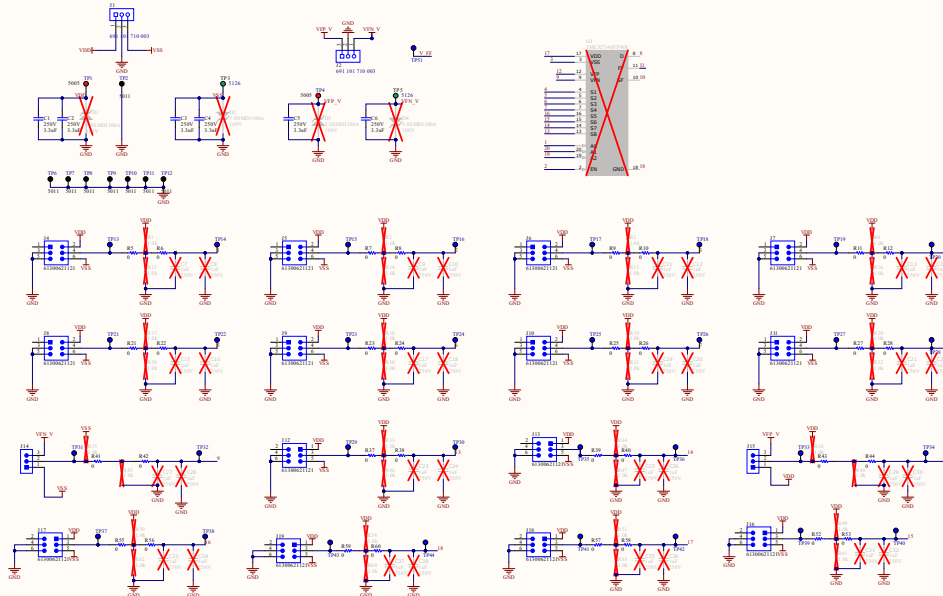
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Date:	11/06/2024	Sheet of
File:	C:\Users\...MNT229_Sch.SchDoc	Drawn By:

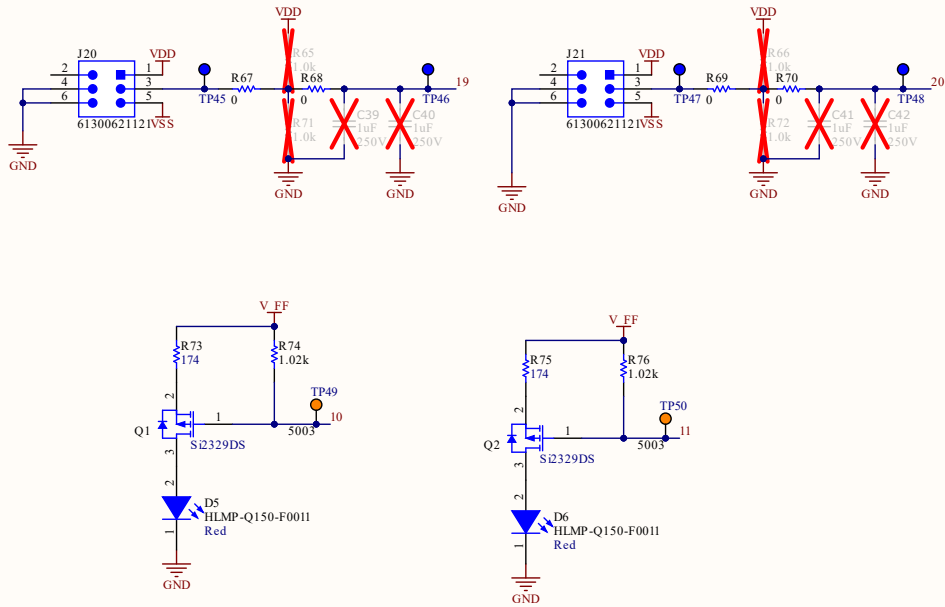




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Figure 3-1. Main Schematic – TMUX73XXF-EVM All Components Shown





Title		
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A		
Date:	11/06/2024	Sheet of
File:	C:\Users\...\INT229_Page2.SchDoc	Drawn By:

Figure 3-2. Main Schematic – TMUX73XXF-EVM Default

3.2 PCB Layouts

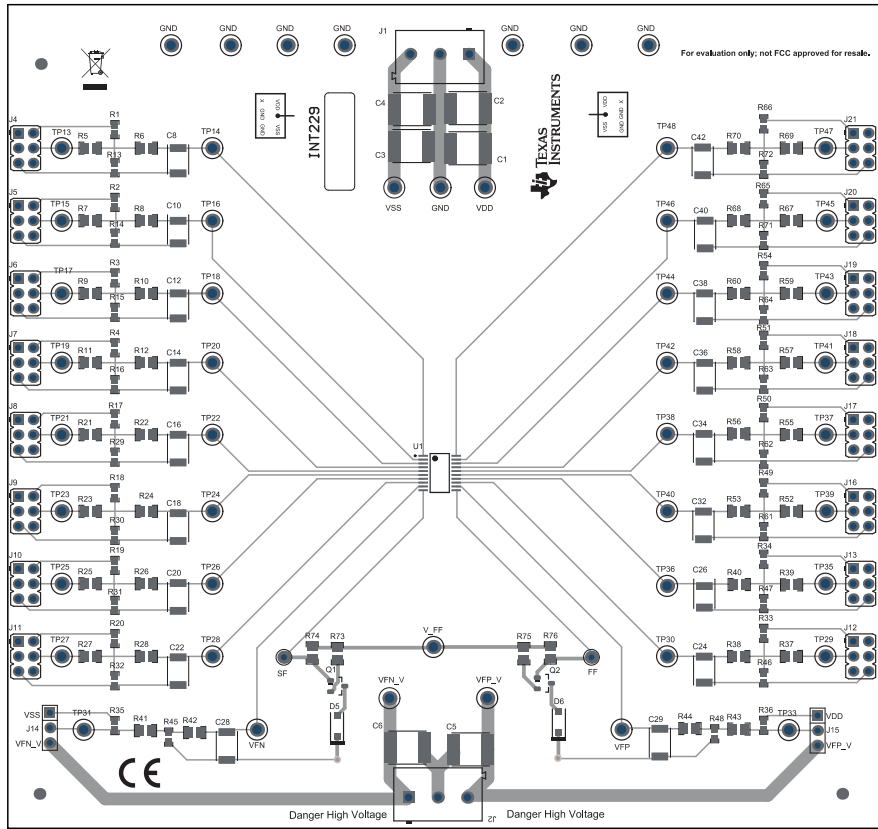


Figure 3-3. TMUX73XXF-EVM Top Layer Layout

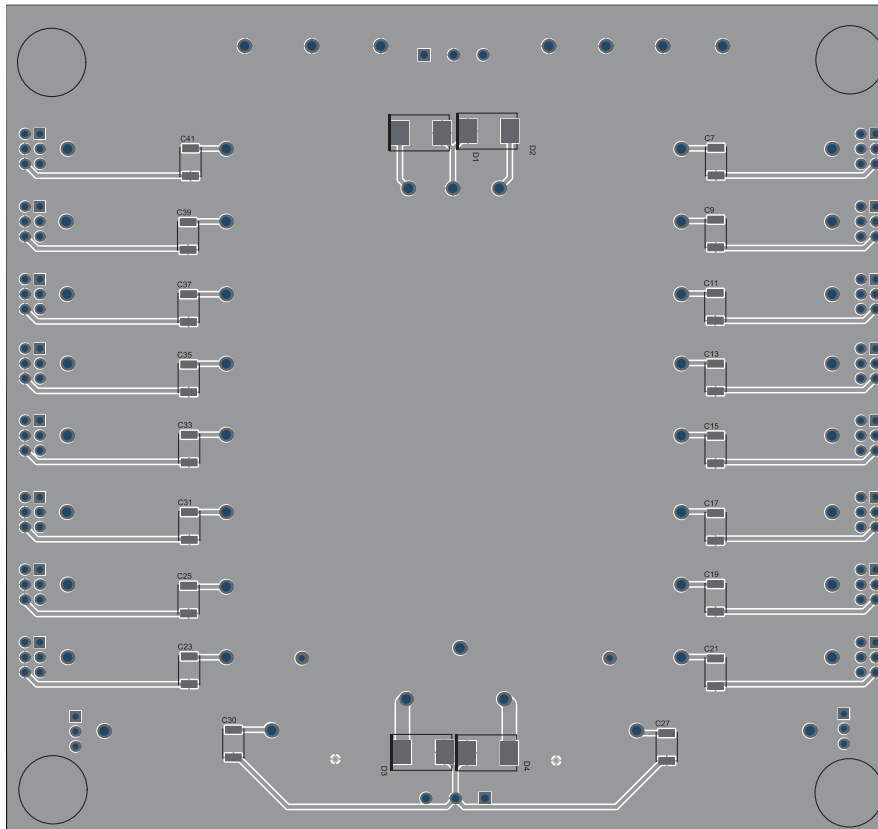


Figure 3-4. TMUX73XXF-EVM Bottom Layer Layout

3.3 Bill of Materials (BOM)

Table 3-1. Bill of Materials

Description	Designator	PartNumber	Quantity	Manufacturer	PackageReference	Value
Printed Circuit Board			1	Any		
CAP, CERM, 3.3 uF, 250 V, +/- 20%, X7T, AEC-Q200 Grade 1, 6x5x5mm	C1, C2, C3, C4, C5, C6	CKG57NX7T2 E335M500JH	6	TDK	6x5x5mm	3.3uF
LED, Red, SMD	D5, D6	HLMP-Q150-F0011	2	Avago	2.08x2.21mm	Red
Fiducial mark. There is nothing to buy or mount.	FID1, FID2, FID3	N/A	3	N/A	N/A	
Bumpon, Hemisphere, 0.44 X 0.20, Clear	H1, H2, H3, H4	SJ-5303 (CLEAR)	4	3M	Transparent Bumpon	
Terminal Block, 5 mm, 3x1, Tin, TH	J1, J2	691 101 710 003	2	Würth Elektronik	Terminal Block, 5 mm, 3x1, TH	
Header, 2.54mm, 3x2, Gold, TH	J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J16, J17, J18, J19, J20, J21	61300621121	16	Würth Elektronik	Header, 2.54mm, 3x2, TH	
Header, 100mil, 3x1, Gold, TH	J14, J15	PBC03SAAN	2	Sullins Connector Solutions	PBC03SAAN	
Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	LBL1	THT-14-423-10	1	Brady	PCB Label 0.650 x 0.200 inch	
MOSFET, P-CH, -8 V, -5.3 A, SOT-23	Q1, Q2	Si2329DS	2	Vishay-Semiconductor	SOT-23	-8V

Table 3-1. Bill of Materials (continued)

Description	Designator	PartNumber	Quantity	Manufacturer	PackageReference	Value
RES, 0, 0%, W, AEC-Q200 Grade 0, 0805	R5, R6, R7, R8, R9, R10, R11, R12, R21, R22, R23, R24, R25, R26, R27, R28, R37, R38, R39, R40, R41, R42, R43, R44, R52, R53, R55, R56, R57, R58, R59, R60, R67, R68, R69, R70	PMR10EZPJ000	36	Rohm	0805	0
RES, 174, 0.1%, 0.125 W, 0805	R73, R75	RT0805BRD07174RL	2	Yageo America	0805	174
RES, 1.02 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	R74, R76	CRCW08051K02FKEA	2	Vishay-Dale	0805	1.02k
Shunt, 100mil, Gold plated, Black	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16, SH-J17, SH-J18	881545-2	18	TE Connectivity	Shunt 2 pos. 100 mil	
Test Point, Compact, Red, TH	TP1, TP4	5005	2	Keystone	Red Compact Testpoint	

Table 3-1. Bill of Materials (continued)

Description	Designator	PartNumber	Quantity	Manufacturer	PackageReference	Value
Test Point, Multipurpose, Black, TH	TP2, TP6, TP7, TP8, TP9, TP10, TP11, TP12	5011	8	Keystone	Black Multipurpose Testpoint	
Test Point, Multipurpose, Green, TH	TP3, TP5	5126	2	Keystone	Green Multipurpose Testpoint	
Test Point, Compact, Blue, TH	TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43, TP44, TP45, TP46, TP47, TP48, TP51	5122	37	Keystone	Blue Compact Testpoint	
Test Point, Miniature, Orange, TH	TP49, TP50	5003	2	Keystone	Orange Miniature Testpoint	

Table 3-1. Bill of Materials (continued)

Description	Designator	PartNumber	Quantity	Manufacturer	PackageReference	Value
Multilayer Ceramic Capacitors 1uF ±10% 250V X7T SMD 1812	C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42	C4532X7T2E1 05K250KA	0	TDK	1812	1µF
Diode, TVS, Uni, 100 V, 162 Vc, SMC	D1, D2, D3, D4	5.0SMDJ100A	0	Littelfuse	SMC	100V
RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	R1, R2, R3, R4, R13, R14, R15, R16, R17, R18, R19, R20, R29, R30, R31, R32, R33, R34, R35, R36, R45, R46, R47, R48, R49, R50, R51, R54, R61, R62, R63, R64, R65, R66, R71, R72	CRCW06031K 00JNEA	0	Vishay-Dale	0603	1.0k

Table 3-1. Bill of Materials (continued)

Description	Designator	PartNumber	Quantity	Manufacturer	PackageReference	Value
+60 V or -60 V Tolerant, Fault-protected, Latch-up Immune, Single-Ended 8:1 Multiplexers with Adjustable Fault Threshold	U1	TMUX7348FP WR	0	Texas Instruments	TSSOP20	

4 Additional Information

4.1 Trademarks

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