Application of the SN74SSTV32852 in Stacked, Low-Profile (1U) PC-1600/2100 DIMMs

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ABSTRACT

Many memory-module manufacturers are turning to low-profile (1U) DIMM designs that significantly increase memory density in computer workstations and servers. The reduction in DIMM height consequently affects the design and layout of the boards. The stacked 1U DIMMs present a unique and challenging problem due partly to the reduction in area for mounting components and also due to the load. The TI SN74SSTV32852 24-bit to 48-bit registered buffer with SSTL_2 inputs and outputs in the GKF LFBGA package is a single-chip solution to the problem. This application report discusses functional and electrical characteristics, performance, routing, and layout analysis of the SN74SSTV32852 in the stacked 1U PC-1600/2100 DIMM, and its use in the intended application. The information in this report, with the data sheet, should enable a memory-module designer to successfully design a stacked 1U PC-1600/2100 DIMM.

Keywords: 1U, buffer, DDR, DIMM, low profile, PC1600, PC2100, register, SSTL_2, stacked DIMM, SN74SSTV32852, LFBGA package

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Introduction

Design of low-profile, 1.75-in.-tall (1U), high-performance, server and workstation computer systems capable of meeting the needs imposed by modern operating systems and software includes the use of large banks of double data rate-synchronous dynamic random access memories (DDR-SDRAMs) on dual in-line memory modules (DIMMs). To meet the demands of stable functionality over the broad spectrum of operating environments, to meet system timing needs, and to support data integrity, the loads presented by the large banks of SDRAMs on the DIMMs require the use of registered buffers in the address and control signal paths. The selection of a register component is integral to the execution of a successful DIMM design. This application report discusses the logic solution that Texas Instruments has available for the registered 1U PC-1600/2100 DIMMs that provide improved performance, cost savings, and design optimization.

Figure 1 shows a 1U server mounted on a rack.

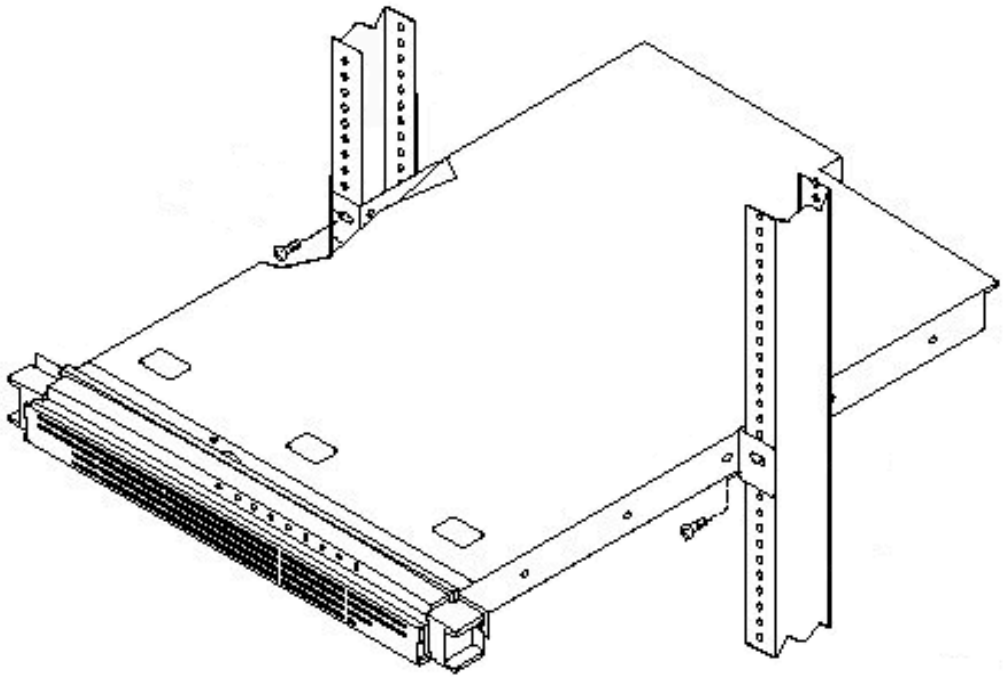


Figure 1. 1U Form-Factor Server

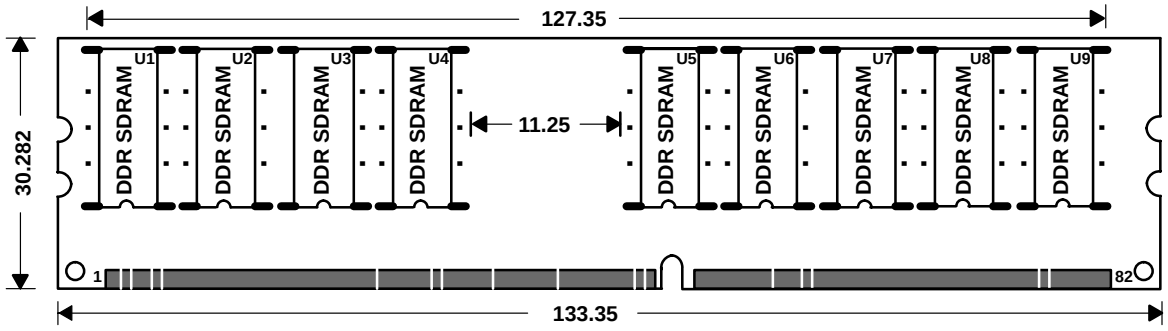
Background

The 184-pin, registered, DDR-SDRAM DIMM is a JEDEC-defined standard for 1.7-in.-tall modules. However, the current trend is to migrate to a module that has a maximum height of 1.2 in. to accommodate applications in 1U form-factor systems. This smaller 1U form factor for DIMMs presents new layout and trace-routing design challenges, especially for the fully populated, stacked DIMM.

Statement of Problems

On a stacked DDR DIMM, there are 36 SDRAM integrated circuits (ICs), with a DDR-SDRAM IC density of up to 512 Mbit. This presents a large, highly capacitive load on the address and control signal paths to the memory controller. This load must be buffered with a logic registered-buffer IC. However, the space available in which to mount this IC and route its associated PCB traces is very small. The registered-buffer IC choice that the designer makes is a way of differentiating the DIMM design to provide a competitive edge.

Figure 2 shows the component placement of the SDRAMs on the 1U DIMM and the space available for placing the support components. The available area is not enough to mount two SN74SSTV16859 devices in the 64-pin TSSOP package, which currently is the accepted solution of the 1.7-in., high-profile, JEDEC-standard DIMM design.



All dimensions are in millimeters.

Figure 2. 1U Form-Factor DIMM Showing Available Space for Mounting Register

Proposed Solution

The proposed solution is one SN74SSTV32852 device per DIMM module.

The factors that must be considered in IC selection include functionality, package size, trace layout, and manufacturability that, when properly considered, can result in a DIMM design that is simpler, more reliable, and more cost effective. To satisfy these needs, TI offers the SN74SSTV32852 in the 114-ball GKF LFBGA package. This application report addresses this device, with respect to this application.

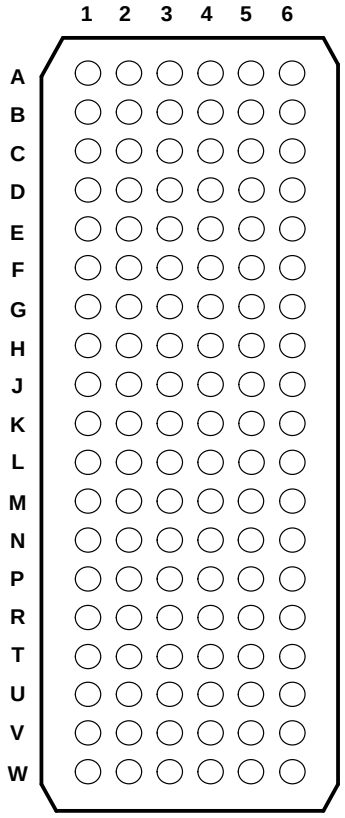
The design choices to be made in the layout of a DIMM are affected by the packaging of the components.

Device Description

Functional Characteristics

The SN74SSTV32852 is a 24-bit-input to 48-bit-output registered buffer. The 1-to-2 architecture supports the heavy loads of stacked DDR DIMMs, and the bottom-in/top-out pinout optimizes the DIMM PCB layout and trace routing. Figure 3 shows the pinout and terminal assignments of the SN74SSTV32852. This device is designed for 2.3-V to 2.7-V V_{CC} operation. All inputs are SSTL_2 compliant, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

GKF PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	Q2A	Q1A	CLK	$\overline{\text{CLK}}$	Q1B	Q2B
B	Q3A	V_{DDQ}	GND	GND	V_{DDQ}	Q3B
C	Q5A	Q4A	V_{DDQ}	V_{DDQ}	Q4B	Q5B
D	Q7A	Q6A	GND	GND	Q6B	Q7B
E	Q8A	GND	V_{DDQ}	V_{DDQ}	GND	Q8B
F	Q10A	Q9A	V_{DDQ}	V_{DDQ}	Q9B	Q10B
G	Q12A	Q11A	GND	GND	Q11B	Q12B
H	Q13A	V_{CC}	V_{DDQ}	V_{DDQ}	V_{CC}	Q13B
J	Q14A	Q15A	GND	GND	Q15B	Q14B
K	Q17A	Q16A	V_{DDQ}	V_{DDQ}	Q16B	Q17B
L	Q18A	Q19A	GND	GND	Q19B	Q18B
M	Q20A	V_{DDQ}	GND	GND	V_{DDQ}	Q20B
N	Q22A	Q21A	V_{DDQ}	V_{DDQ}	Q21B	Q22B
P	Q23A	V_{DDQ}	GND	GND	V_{DDQ}	Q23B
R	Q24A	V_{CC}	$\overline{\text{RESET}}$	V_{REF}	V_{CC}	Q24B
T	D2	D1	D6	D18	D13	D14
U	D4	D3	D10	D22	D15	D16
V	D5	D7	D11	D23	D19	D17
W	D8	D9	D12	D24	D21	D20

Figure 3. SN74SSTV32852 GKF Package Pinout and Terminal Assignments

The SN74SSTV32852 operates from a differential clock (CLK and $\overline{CLK}$). Data are registered at the crossing of CLK going high and $\overline{CLK}$ going low. The device supports low-power standby operation. When $\overline{RESET}$ is low, the differential input receivers are disabled and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{RESET}$ input always must be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up. Figure 4 shows the function table and logic diagram of the SN74SSTV32852.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{RESET}$	CLK	$\overline{CLK}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

LOGIC DIAGRAM (POSITIVE LOGIC)

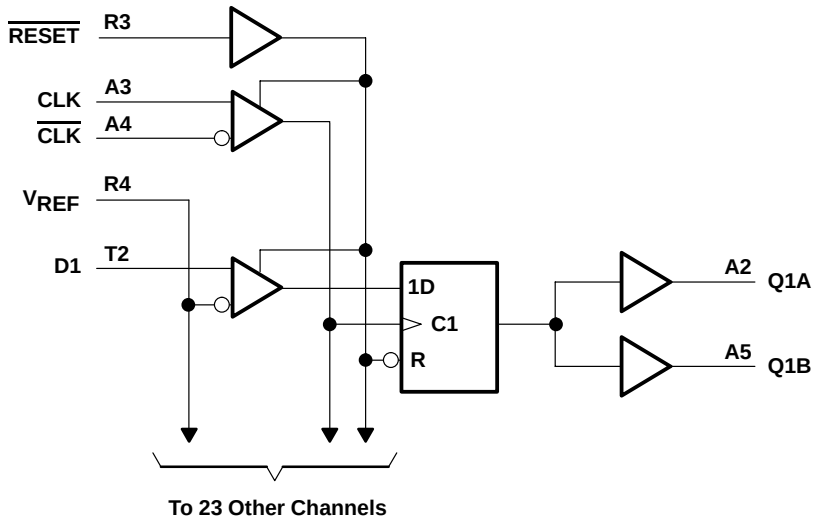


Figure 4. Function Table and Logic Diagram of SN74SSTV32852

Electrical Characteristics

The electrical characteristics of the register are a critical aspect of a successful DIMM design. This section discusses the ac and dc performances of the register.

AC Performance

Table 1 shows a comparison of the TI SN74SSTV32852 characteristics with the requirements published by JEDEC in the *DDR SDRAM Registered DIMM Design Specification, Revision 1.0.*

Table 1. Timing and Switching Characteristics of the SN74SSTV32852

PARAMETER			JEDEC SPECIFICATION (SEE NOTE 4)		TI SN74SSTV32852 (SEE NOTE 4)		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		60	170		200	MHz
t_{su}	Setup time	Fast slew rate (see Notes 1 and 3)	0.75	—	0.75	—	ns
		Slow slew rate (see Notes 2 and 3)	0.90	—	0.90	—	
t_h	Hold time	Fast slew rate (see Notes 1 and 3)	0.75	—	0.75	—	ns
		Slow slew rate (see Notes 2 and 3)	0.90	—	0.90	—	
t_{pd}	Clock (CLK or $\overline{CLK}$) to output time (see Note 5)		1.1	2.8	1.1	3.1	ns
t_{PHL}	Reset ($\overline{RESET}$) to output time		—	5	—	5	ns

NOTES: 1. For data signal, the input slew rate is ≥1 V/ns.
2. For data signal, the input slew rate is ≥ 0.5 V/ns and <1 V/ns.
3. For CLK and $\overline{CLK}$ signal, input slew rates are ≥1 V/ns.
4. V_{CC} = 2.5 V ± 0.2 V and T_A = 0°C to 70°C
5. Specified with 30 pF from output to GND and 50 Ω from output to V_{TT}

Table 1 shows that the SN74SSTV32852 meets and exceeds the PC-1600/2100 application requirements. The SN74SSTV32852 clock-to-output time (t_{pd}) appears to be 300 ps slower than the JEDEC specification outlined in the *DDR SDRAM Registered DIMM Design Specification, Revision 1.0.* However, the postregister timing budget specified for a typical DDR PC-1600 DIMM has a margin of 3.475 ns, which corresponds to a 975-ps margin for a typical DDR PC-2100. Therefore, considering the additional 300-ps delay through the register, there is a 3.175-ns margin for PC-1600 applications and a 675-ps margin for PC-2100 applications when using the SN74SSTV32852.

DC Performance

Table 2 shows the dc performance of the SN74SSTV32852. Note that the $\overline{RESET}$ input of the device must be held at V_{CC} or ground to ensure proper operation of the device. The differential inputs must not be floating unless $\overline{RESET}$ is low. Refer to the TI application reports, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004, and *Low-Power Support Using Texas Instruments SN74SSTV16857 and SN74SSTV16859 DDR-DIMM Registers,* literature number SCEA020, for additional information.

Table 2. Electrical Characteristics of the SN74SSTV32852

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage	2.3		2.7	V
V_{REF}	Reference voltage (V_{REF} =V_{DDQ} /2)	1.15	1.25	1.35	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	AC high-level input voltage (data input)	V_{REF} + 310 mV			V
	DC high-level input voltage (data input)	V_{REF} + 150 mV			
V_{IL}	AC low-level input voltage (data input)			V_{REF} – 310 mV	V
	DC low-level input voltage (data input)			V_{REF} – 150 mV	
V_{IH}	High-level input voltage ($\overline{\text{RESET}}$ input)	1.7			V
V_{IL}	Low-level input voltage ($\overline{\text{RESET}}$ input)			0.7	V
V_{ICR}	Common-mode input voltage range (CLK, $\overline{\text{CLK}}$ inputs)	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage (CLK, $\overline{\text{CLK}}$ inputs)	360			mV
I_{OH}	High-level output current			–20	mA
I_{OL}	Low-level output current			20	mA
V_{OH}	High-level output voltage (I_{OH} = –100 μA)†	V_{DDQ} – 0.2			V
	High-level output voltage (I_{OH} = –16 mA)‡	1.95			
V_{OL}	Low-level output voltage (I_{OL} = 100 μA)†			0.20	V
	Low-level output voltage (I_{OL} = 16 mA)‡			0.35	

† Specified for 2.3 V = V_{DDQ} = 2.7 V
‡ Specified for V_{DDQ} = 2.3 V

CLK, $\overline{\text{CLK}}$ Input Capacitance

In the *DDR SDRAM Registered DIMM Design Specification, Revision 1.0,* JEDEC specifies the input capacitance of the CLK and $\overline{\text{CLK}}$ pins as 2.5 pF to 3.5 pF. However, the SN74SSTV32852 has an input capacitance specification of 3 pF to 4 pF on the CLK and $\overline{\text{CLK}}$ pins. The reason for this difference is capacitance due to the number of registers required per module.

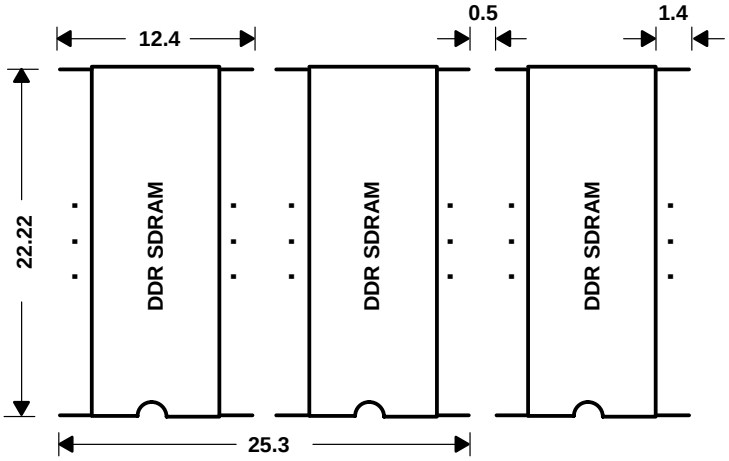
The JEDEC-standard DIMM requires two registers per module. The respective CLK and $\overline{\text{CLK}}$ inputs of the JEDEC-standard registers are tied in parallel and driven by the PLL. Therefore, the PLL sees twice the input capacitance (5 pF to 7 pF) on the CLK and $\overline{\text{CLK}}$ lines for the JEDEC-standard solution.

A stacked, low-profile DIMM requires only one SN74SSTV32852 register per DIMM. With this solution, the PLL driving the CLK and $\overline{\text{CLK}}$ inputs sees the specified input capacitance (3 pF to 4 pF) at the register pins. With the SN74SSTV32852 solution, the input capacitance on the CLK and $\overline{\text{CLK}}$ lines, as seen by the PLL, does not exceed the doubled capacitance seen by the PLL in the JEDEC-standard solution.

Application

Layout and Routing Analysis

Figure 5 shows the SDRAMs and the design rules used for the placement of the SDRAMs on the DIMM.



All dimensions are in millimeters.

Figure 5. Design Rules for SDRAM Placement

The total component-placement-area length on a DDR DIMM is 127.35 mm per side (see Figure 2). The total length occupied by nine SDRAM stacks per side is 116.1 mm per side (12.4-mm/SDRAM-stack width + 0.5-mm/SDRAM-stack space), or less, with wider alternate stacking technologies. This means that the width of the available space on each side in which to mount logic components is, at most, 11.25 mm per side. At 22.22-mm height, there is a total area available on each side of approximately 250 mm^2 for logic devices.

Based on the assumption that most DIMM vendors do not want to qualify a new PLL package type, the use of the standard TSSOP-packaged CDCV857 is the best choice for clock buffering. The area consumed by this device, along with an SPD component, take up over 125 mm^2, most of the component mounting area on one side of the DIMM. Figure 6 shows one side of the DIMM layout with the SDRAMs, PLL, and SPD mounted.

Figure 6. One Side of DIMM With SDRAMs, PLL, and SPD Mounted

Having the PLL and SPD on one side of the DIMM leaves only one free side, or about 250 mm^2 in which to place and route a buffered register. Figure 7 shows the other side of the DIMM with the SN74SSTV32852 in the 114-ball GKF LFBGA package.

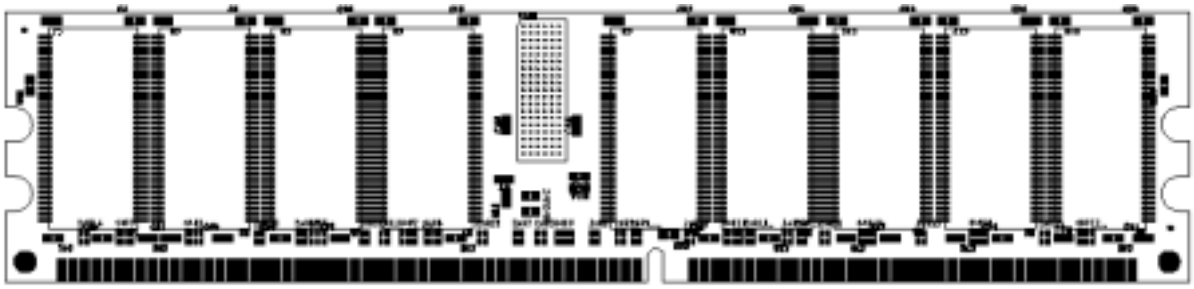


Figure 7. Other Side of DIMM With SN74SSTV32852 Mounted

The SN74SSTV32852 register is housed in a 114-ball GKF LFBGA package. The signals can be easily brought out of the device and routed on the DIMM. Figure 8 shows an example routing of the SN74SSTV32852.

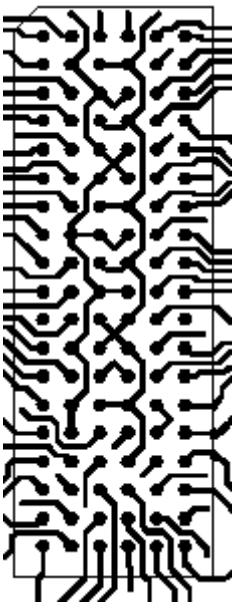


Figure 8. Example Routing of SN74SSTV32852 Register

Simulation Analysis

One of the most important measures of a device's dynamic performance is the effect of varying conditions on signal integrity. To facilitate preliminary analyses of the characteristics of the SN74SSTV32852, a SPICE analysis graph and table of results are presented in this section. These analyses are the outputs of SPICE simulation using the JEDEC-standard DDR-DIMM Raw-Card C load, which comprises two banks of ×4-stacked SDRAMs. In this application, any pair of the 24 1-to-2 drivers in the SN74SSTV32852 registered buffer drives 36 loads. Consequently, each output drives 18 loads. In the simulation analyses, the outputs are measured one at a time, with one input transition per measurement.

Figure 9 shows the SPICE simulation results of the device output switching characteristics. The results were obtained by simulating a single-bit device model into an address/command net of the Raw-Card C DIMM application with 36 loads, using nominal process models at 40°C (ambient temperature of 25°C), with $V_{CC} = V_{DDQ} = 2.5$ V.

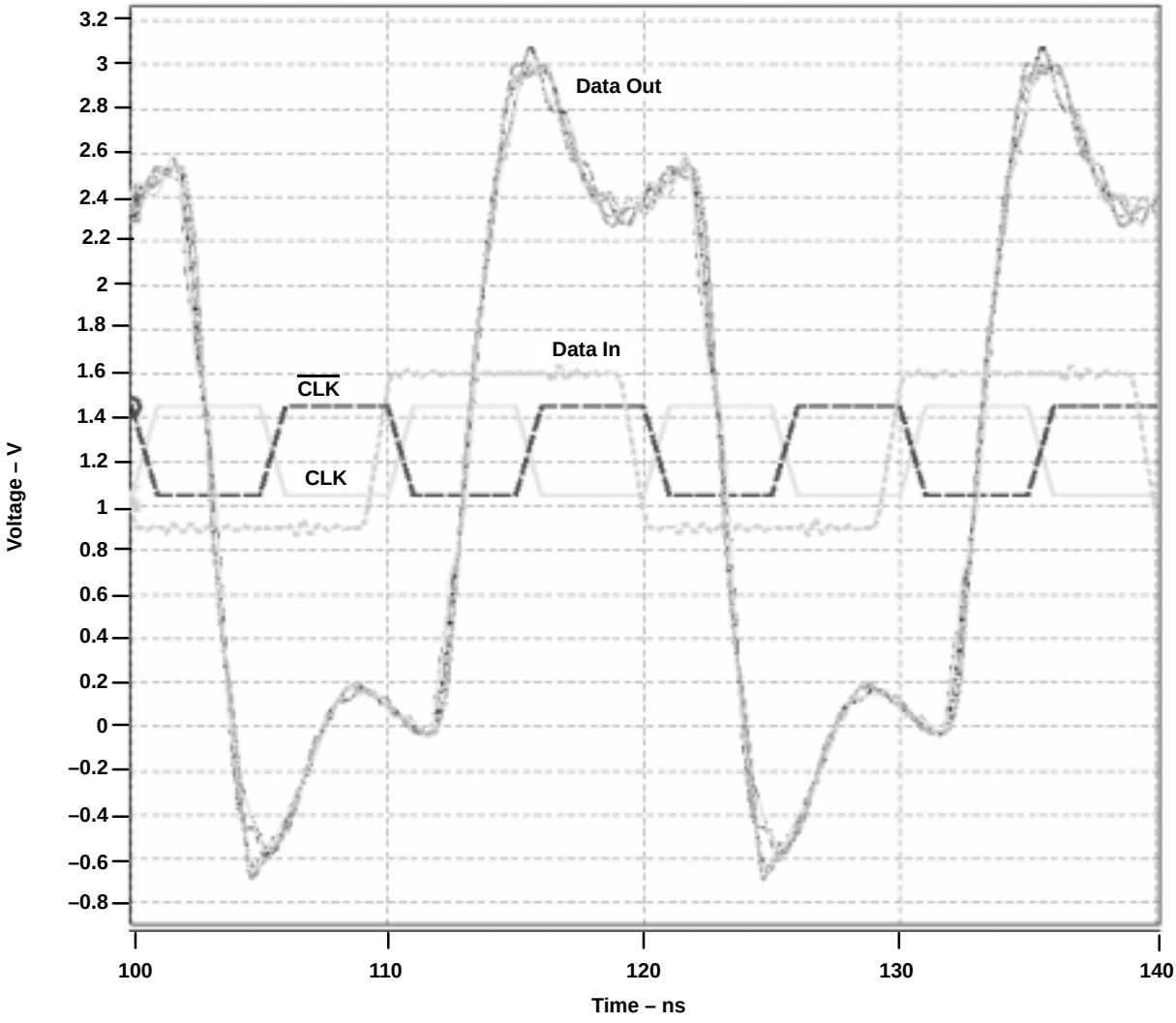


Figure 9. Simulation Results of SN74SSTV32852 Into a Raw-Card C Load

Figure 9 shows the CLK, $\overline{CLK}$, and data in the register. All signals, except data out of the register, are measured at the SN74SSTV32852 terminals. Also shown is the data out of the register, measured at the inputs of the SDRAM. Therefore, the signal integrity of the measured waveform is a true representation of the signal into the SDRAM.

Table 3 shows the SPICE simulation results of the SN74SSTV32852 in a Raw-Card C DIMM application load, with the effect of single outputs switching for different supply voltages, temperatures, and process conditions. The dc interface parameters are measured at the input terminals of the SDRAMs.

Table 3. SPICE Single-Bit Simulation Results for DC Interface Parameters Into Application Load

PARAMETER	VALUE			UNIT
	V_{DDQ} = 2.3 V WEAK PROCESS	V_{DDQ} = 2.5 V NOMINAL PROCESS	V_{DDQ} = 2.7 V STRONG PROCESS	
V_{OHP}	2.70	3.21	3.42	V
V_{OHV}	2.12	2.15	2.35	V
V_{OLP}	0.224	0.229	0.297	V
V_{OLV}	–0.648	–0.762	–0.816	V

The SN74SSTV32852 drives the SDRAMs, which have SSTL_2 inputs. Considering the worst-case scenario for SSTL_2 inputs, the V_{IL}(AC) is 0.84 V at V_{CC} = 2.3 V, and V_{IH}(AC) is 1.66 V at V_{CC} = 2.7 V. Table 1 shows that the SN74SSTV32852 is capable of driving the load and meets the SSTL_2 dc interface requirements.

Simultaneous Switching

One concern in IC design is the challenge of minimizing simultaneous-switching noise while increasing switching speed of the device. Table 4 shows the SPICE simulation results of the SN74SSTV32852 dynamic behavior with multiple outputs switching simultaneously. The data was collected using the strong process model at 0°C. These analyses are the outputs of SPICE simulation using the standard load specified in the parameter measurement information (see Appendix A).

Table 4. SPICE Simultaneous-Switching Results for DC Interface Parameters Into Data-Sheet Load

PARAMETER	VALUE			UNIT
	V_{DDQ} = 2.3 V	V_{DDQ} = 2.5 V	V_{DDQ} = 2.7 V	
V_{OHV}, 48 bits switching	2.044	2.228	2.400	V
V_{OHV}, 46 bits switching†	1.800	1.938	2.075	V
V_{OLP}, 48 bits switching	0.326	0.351	0.391	V
V_{OLP}, 46 bits switching†	0.673	0.755	0.838	V

† The two quiet bits not switched are left ideal high.

The simulation switching results indicate that V_{CC} droop and ground bounce, when 48 bits are switching simultaneously, do not violate the V_{IL} of 0.84 V (for V_{CC} = 2.3 V) and V_{IH} of 1.66 V (for V_{CC} = 2.7 V).

Considering the worst-case scenario for SSTL_2 inputs, the V_{IL}(AC) is 0.84 V at V_{CC} = 2.3 V, and V_{IH}(AC) is 1.66 V at V_{CC} = 2.7 V. Table 4 shows that even with all 48 bits switching simultaneously, the SN74SSTV32852 is capable of driving the load and meets the SSTL_2 dc interface requirements.

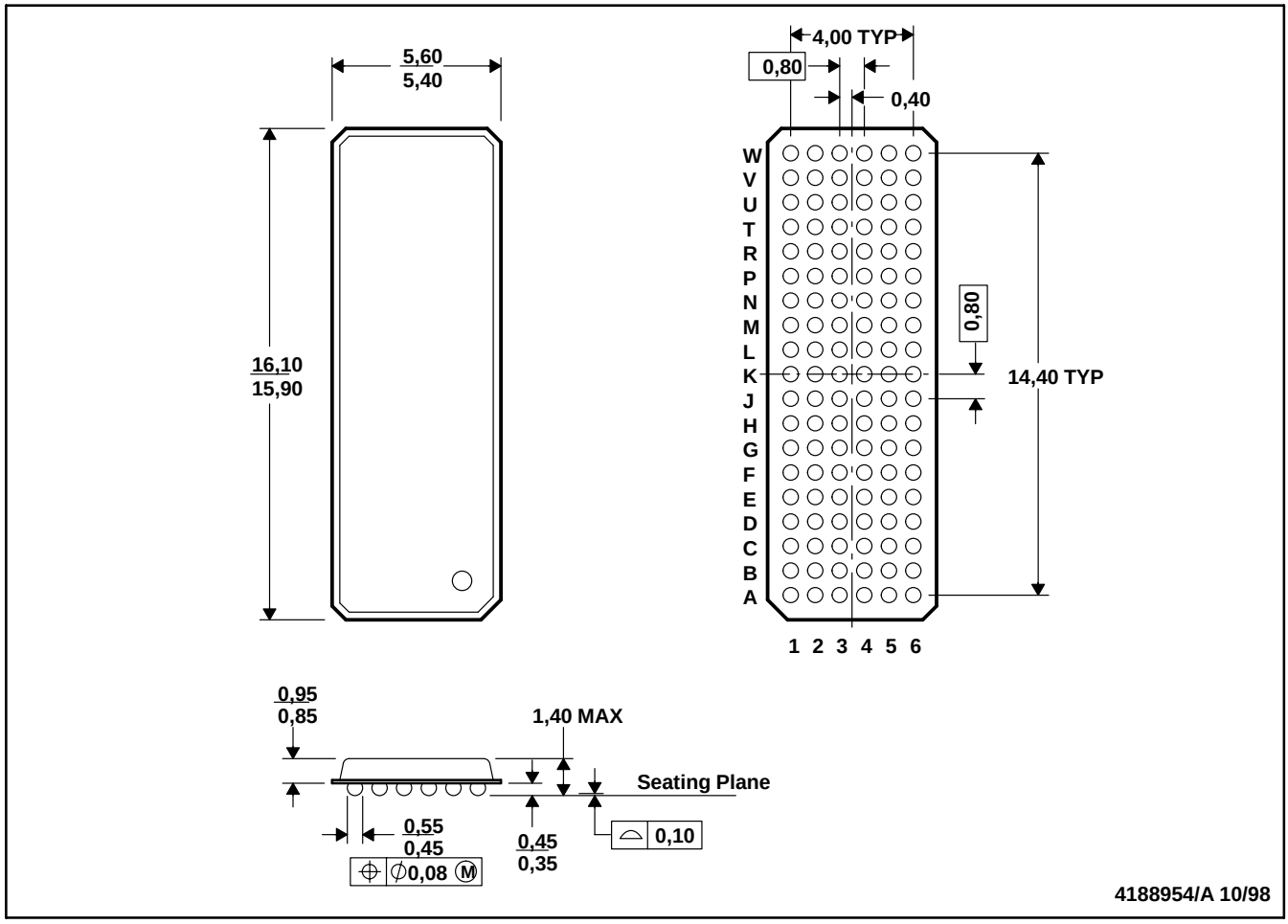
The propagation delay times of the SN74SSTV32852 given in the data sheets apply when only one bit switches at a time. If several bits switch simultaneously, the propagation delay times given in data sheet can be used only with reservations. The reason for this is that the package inductance of the supply voltage lines, as well the output lines, have a significant influence on the device and, thus, on the delay times. These inductances have the effect that the current in the power supply lines and, consequently, in the output of the device, have a limited rate of rise. For this reason, when several bits switch simultaneously, only a limited output current is available. SPICE simulation results of simultaneous switching reveal the propagation delay is increased by 200 ps.

Package Information

Mechanical Information

Figure 10 shows the dimensions of the GKF LFBGA package.

GKF (R-PBGA-N114) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

Figure 10. GKF Ball Grid Array Package Dimensions

Figure 11 shows the construction of the 114-ball LFBGA package.

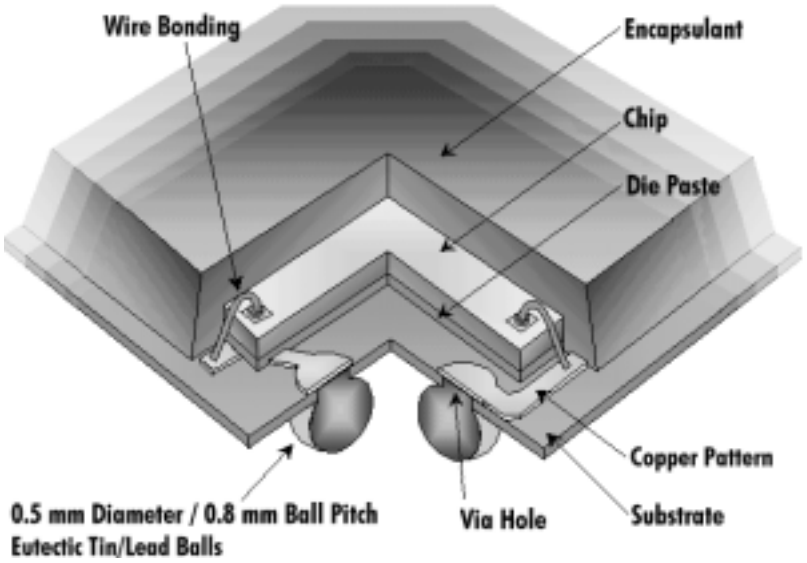


Figure 11. LFBGA Cross Section

Table 5 gives the package attributes of the 114-ball LFBGA package.

Table 5. Summary of LFBGA Package Attributes

Ball count	114
Ball configuration (rows, columns)	6 × 19
Square/rectangular	Rectangular
Ball-to-ball pitch (mm)	0.8
Ball diameter (mm)	0.5
Package body width (mm)	5.5
Package body length (mm)	16
Package thickness (mm)	1.2 Min –1.5 Max
Package weight (mg)	167
Shipping media, tape and reel (units)	1000
Desiccant pack	Level 3

Advantages of the LFBGA package are:

- Industry-accepted 0.8-mm ball pitch, easy pad-via-ball routing using common industry PWB technology
- Bottom-in/top-out, easy PWB layout and wiring
- Robust solderability due to 0.5-mm diameter ball

Board-Level Reliability

Figure 12 shows the board-level reliability (BLR) effect of selected package design attributes on cumulative distribution function or cumulative failures [F(t)] versus number of thermal cycles. In the 114-ball VFBGA design effort, these factors, along with PWB pad design and bond line thickness, were optimized to produce an affordable, reliable solution that meets industry requirements. It is important to note that the PWB pad design is not directly included in Figure 12, but it is the most significant factor affecting BLR that can be controlled by the original equipment manufacturer (OEM).

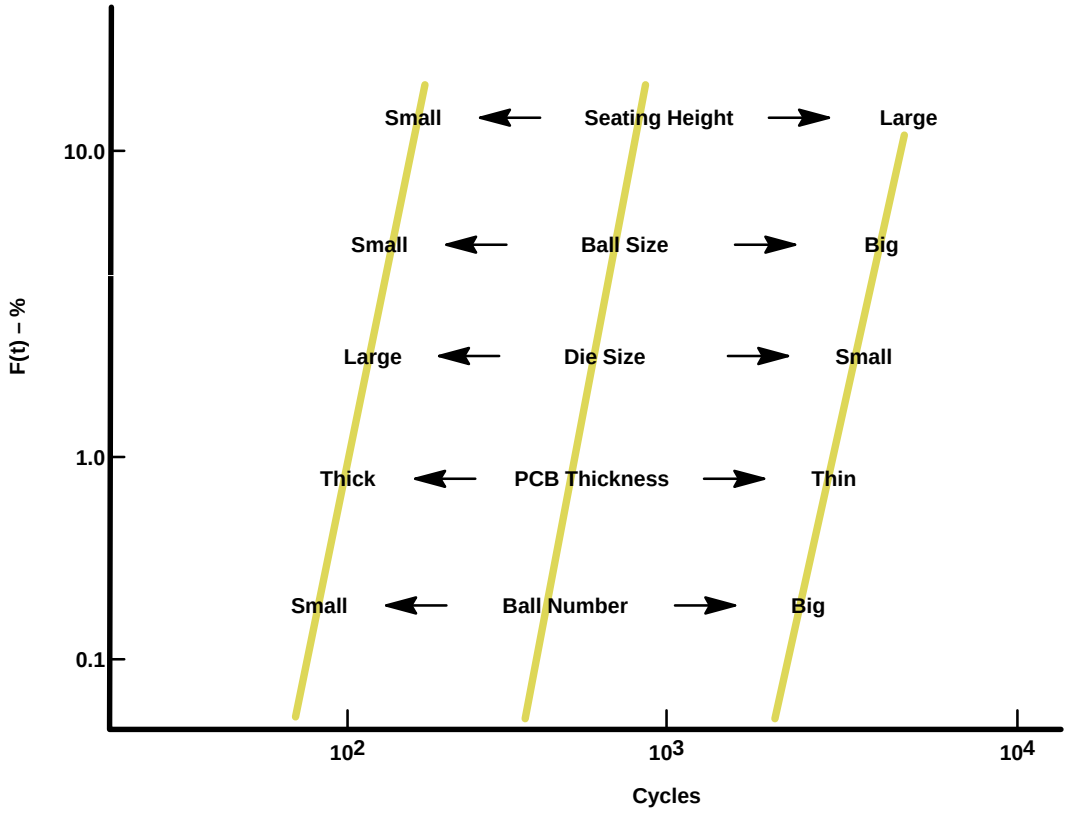


Figure 12. Factors Affecting Board-Level Reliability

Figure 13 shows the effect of pad design on ball behavior during temperature cycling. The choice of the PWB pad diameter, with respect to that of the internal (package) substrate via, is crucial to maximize BLR, and specific recommendations for pad design are discussed later in this section. From an internal perspective, bond line thickness of the die attach material also was optimized to improve performance by reducing the magnitude of inelastic strain (plasticity and creep) at the chip corners.

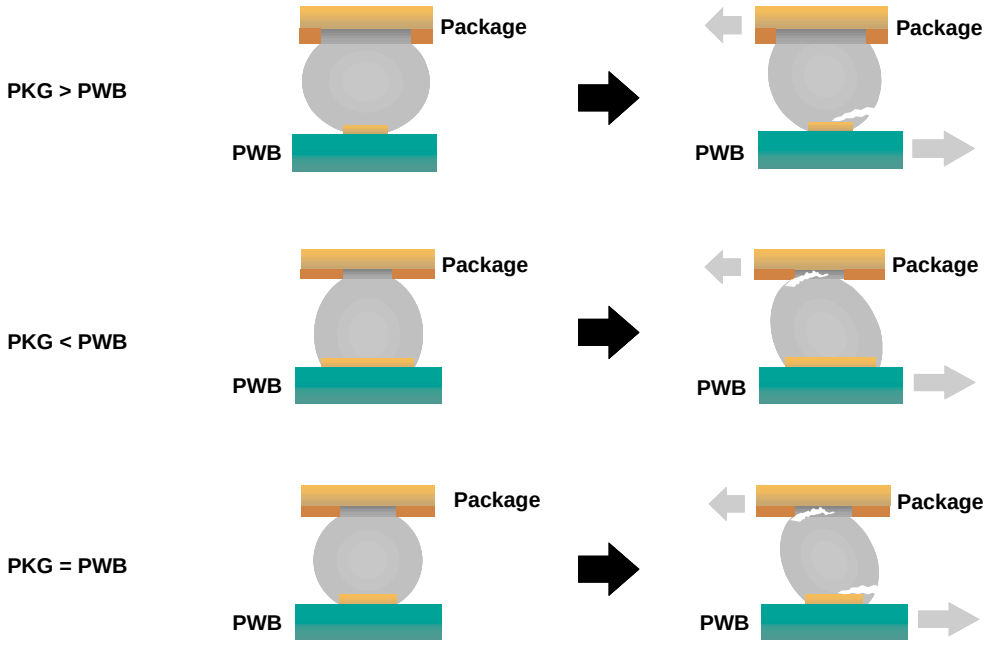


Figure 13. Solder-Ball Behavior During Thermal Cycling

With these factors in mind, the package is designed and tested under thermal cycling conditions of –40°C to 125°C, 10-minute dwell at extremes, 5-minute transition time, and completion of 2 cycles per hour. The PWB was 0.8-mm thick FR4, with non-solder-masked pads, a pad diameter of 0.35 mm, and a mask diameter of 0.50 mm. Table 6 summarizes the test results.

Table 6. Board-Level Reliability Statistics of 114-Ball LFBGA Package

CYCLES TO FIRST FAILURE	CYCLES TO 63.2%	SAMPLE SIZE	BETA
2141	3458	36	4.54

Testing failures occurred as expected due to the pad design matching the internal via in a 1:1 diameter ratio, as shown in the bottom line of Figure 13.

The beta term in Table 6 is the shape parameter of the failure distribution, which describes how the failures are distributed about the characteristic lifetime of the device when F(t) = 0.632 (or 1 – 1/e). A very conservative assumption of the operational environment for DIMM products would be from 10°C to 75°C, with three cycles per day. Using this assumption, the characteristic life of the 114-ball BGA package can be calculated using the modified Coffin-Manson Law.[4]

First, calculate the acceleration factor, Af:

$$Af = \left(\frac{f_o}{f_t}\right)^{1/3} \left(\frac{\Delta T_t}{\Delta T_o}\right)^{1.9} e^{1414\left(\frac{1}{T_{omax}} - \frac{1}{T_{tmax}}\right)} \quad (1)$$

Where:

f_t = temperature cycling frequency at test condition
f_o = temperature cycling frequency at operating condition
ΔT_t = temperature range at test condition
ΔT_o = temperature range at operating condition
T_{omax} = maximum temperature at operating condition
T_{tmax} = maximum temperature at test condition

For the assumed operational environment, the acceleration factor is calculated to be 5. The Weibull distribution in equation 2 can then be used to calculate the predicted characteristic life:

$$F(x) = 1 - e^{-\left[\frac{x}{(Af \times \lambda)}\right]^{\beta}} \quad (2)$$

Where:

x = independent variable
λ = characteristic life: Nf at F(1 – 1/e), or 63.2% failure of the population
Af = acceleration factor from equation 1
β = beta, the Weibull shape parameter

Substituting the acceleration factor Af = 5 into equation 2 gives a predicted characteristic life cycle of 17,291 cycles or 138,328 hours (15.8 years) of operation at F(t) = 0.632. Similarly, different values of Nf can be used instead of the characteristic life. At Nf = 1%, this failure distribution shows that 1% of the 114-ball BGA package population would fail in 9.2 years in the assumed environment, and at Nf = 0.1%, 0.1% would fail in 7.7 years.

Note that the assumed environmental conditions for the previous calculations are very conservative with respect to cycles; three per day or one per eight-hour shift. In a normal server environment, shutdown may occur only once a week for maintenance. Using the method described, the acceleration factor in this more realistic case is 1.8127, and that 63.2% of the population would fail in 120.2 years. Similarly, at Nf = 1% and Nf = 0.1%, the values are 70.0 years and 58.6 years, respectively.

PWB Design Recommendations

The design of the land pads on the PCB for the 114-ball BGA package is critical to achieve good manufacturability and optimum reliability. As previously mentioned, in an optimum design, the diameter of the land pad is equal to the diameter of the package vias, i.e., the fatigue life of the solder joints is improved when the ratio of these dimensions is 1.0.

There are two methods of defining land pads on PCB: solder-mask defined and non-solder-mask defined. In the solder-mask-defined method, the desired land area is defined by the opening of the solder mask. The advantage of this technique is that the land-pad size is controlled and the solder mask promotes the adhesion of the copper pad to the PCB. However, the copper-pad dimension is larger, which makes routing more difficult, plus, stress concentrations are induced into the solder ball at the mask/pad interface. In the non-solder-mask-defined method, the land area is etched inside the solder-mask area. The final land-pad dimension depends on the accuracy of the copper-etching method. The advantage of non-solder-mask-defined method over the solder-mask-defined methods is routability (the former method allows larger trace width/spacing between the solder balls). Figure 14 shows the land-pad dimension for the 114-ball BGA package using the solder-mask-defined and non-solder-mask-defined methods. Table 7 shows via design, and assumes a 0.2-mm (8-mil) via land-pad dimension and a 0.1-mm (4-mil) clearance between the via land pad and the adjacent land pad. Based on BLR studies and PWB-manufacturing-capability surveys, TI recommends the guidelines in Table 7 for PWB pad and via design.

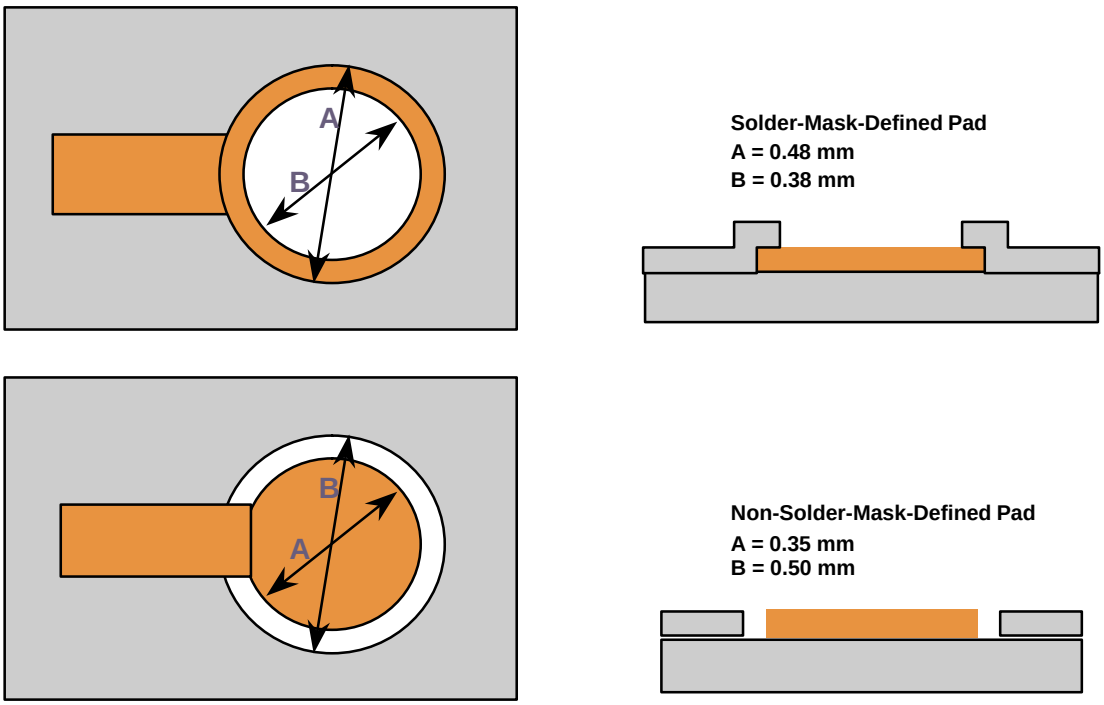


Figure 14. Land-Pad Dimensions for 114-Ball BGA Package

Table 7. PWB and Via Design Recommendations

	SOLDER-MASK-DEFINED LAND PAD	NON-SOLDER-MASK-DEFINED LAND PAD
Trace width/spacing	0.107 mm (4.2 mil)	0.150 mm (5.9 mil)
Drill-bit diameter	0.23 mm to 0.25 mm (9 mil to 10 mil)	0.35 mm to 0.38 mm (14 mil to 15 mil)
Unplated hole	0.23 mm to 0.25 mm (9 mil to 10 mil)	0.35 mm to 0.38 mm (14 mil to 15 mil)
Finished via size (plated)	0.178 mm to 0.2 mm (7 mil to 8 mil)	0.30 mm to 0.33 mm (12 mil to 13 mil)

Features and Benefits

Table 8 summarizes the features and benefits of the SN74SSTV32852.

Table 8. Features and Benefits of the SN74SSTV32852

FEATURES	BENEFITS
114-ball BGA solution	Known manufacturability
24-bit 1:2 register	Requires only one register per DIMM
Pinout optimized for vertical mounting	Ease of trace routing
Mounting area of 5.6 mm × 16.1 mm (90.16 mm^2)	Requires less board space. Enables use of stacked SDRAMs from multiple vendors. Enables use of currently qualified TSSOP PLL.
Single-chip solution	Improved reliability and lower cost
Supported by multiple logic vendors	Second sourcing available
Samples available	Enables DIMM designs

Conclusion

The TI SN74SSTV32852 24-bit to 48-bit registered buffer with SSTL_2 inputs and outputs is a unique single-chip register solution to the stacked 1U PC-1600/2100 DIMMs. The functional and electrical characteristics, performance, routing, and layout analysis of the SN74SSTV32852 in the stacked 1U PC1600/2100 DIMM are presented in this application report. Further, analyses of the use of the device in the intended application are also presented in this application report.

FAQs

Question 1: What is SSTL?

Answer: SSTL is Stub Series Terminated Logic. See JEDEC specifications JESD 8-8 SSTL_3 and JESD8-9 SSTL_2.

Question 2: What is the difference between SSTL and SSTV?

Answer: SSTL is the name of the JEDEC standard. SSTV is the industry-approved naming convention for 2.5-V (nominal) logic family for DDR DIMMs.

Question 3: How do I get a copy of the SN74SSTV32852 data sheet and samples?

Answer: The SN74SSTV32852 data sheet can be obtained by accessing http://www.ti.com/sc/docs/psheets/pids.htm. Samples of the SN74SSTV32852 can be obtained by contacting your local TI sales representative.

Question 4: How do I get a copy of the SN74SSTV32852 SPICE and IBIS models?

Answer: The SPICE model for the SN74SSTV32852 can be obtained by contacting your local TI sales representative. The IBIS model can be obtained by accessing http://www.ti.com/sc/docs/tools/logic/models/ibis.htm.

Question 5: What are the advantages of using the SN74SSTV32852 in a DIMM design?

Answer: The advantages of the SN74SSTV32852 device in a DIMM design include:

- Manufacturability known
- Only one register per DIMM required
- Trace routing is easy
- Less board space required, which enables the use of stacked SDRAMs from multiple vendors and enables the use of the currently qualified TSSOP PLL
- Reliability is improved and cost is lower
- Second sourcing is available
- 1U PC-1600/2100 DIMM design is enabled.

Question 6: Are there any alternate sources for the SN74SSTV32852?

Answer: Yes, five logic vendors currently support production devices in 114-BGA package and four support the SN74SSTV32852 device in the GKF package.

Question 7: What is the transistor count for the SN74SSTV32852 device?

Answer: The total number of transistors in the SN74SSTV32852 device is 1794.

References

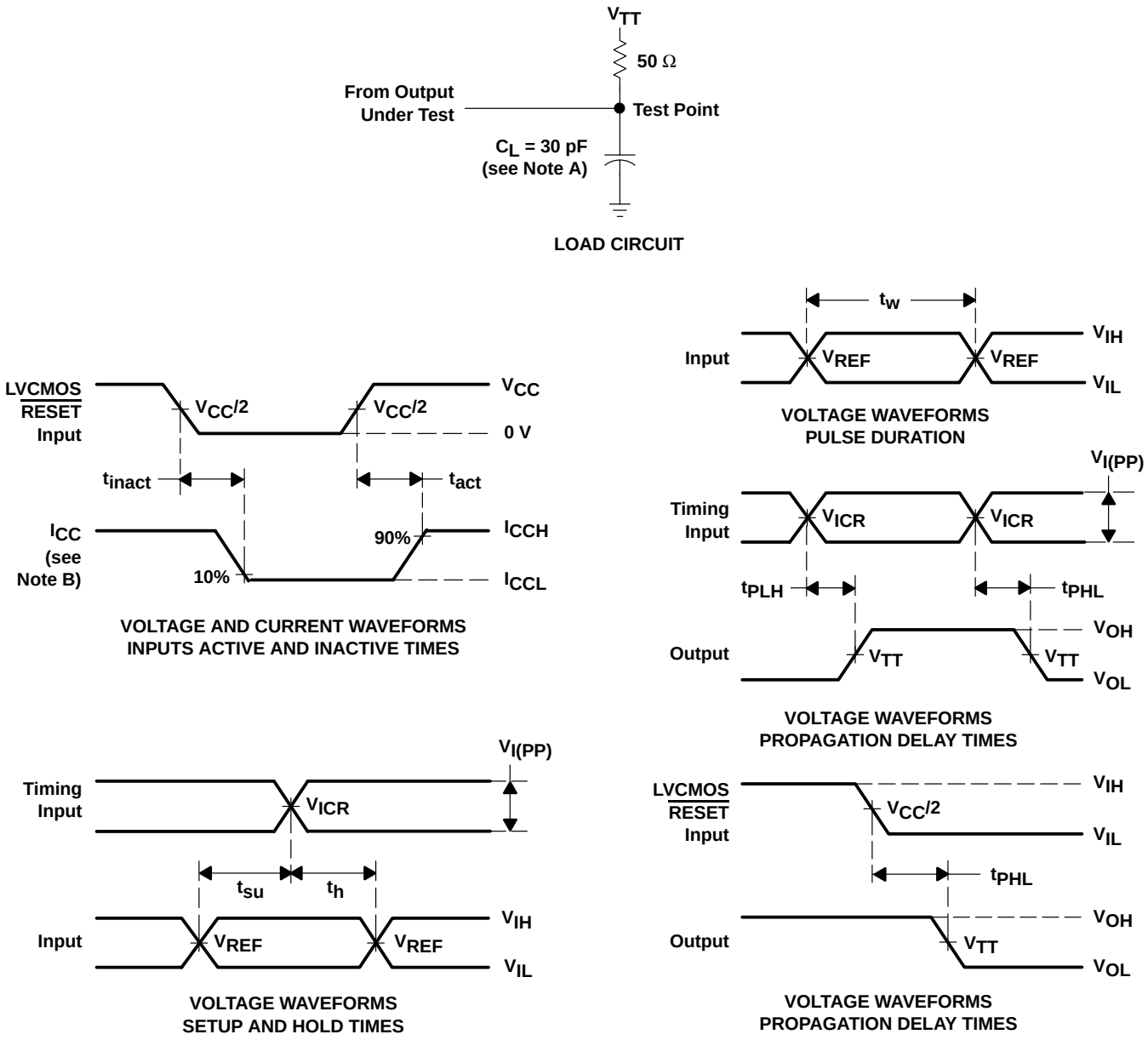
1. *Implications of Slow or Floating CMOS Inputs,* application report, literature number SCBA004C.
2. *Low-Power Support Using Texas Instruments SN74SSTV16857 and SN74SSTV16859 DDR-DIMM Registers,* application report, literature number SCEA020.
3. *SN74SSTV32852 24-Bit to 48-Bit Registered Buffer With SSTL_2 Inputs and Outputs,* data sheet, literature number SCES361.
4. JEDEC, *DDR SDRAM Registered DIMM Design Specification*, *Revision 1.0.*
5. JEDEC, *Stub Series Terminated Logic for 3.3 Volts (SSTL_3)*, August 1996.
6. JEDEC, *Stub Series Terminated Logic for 2.5 Volts (SSTL_3)*, September 1998.
7. Rao Tummala and Eugene Rymaszewski, *Microelectronics Packaging Handbook*, New York: Van Nostrand Reinhold, 1989.

Glossary

1U	Low profile – 1 unit of telecommunication equipment rack height
ac	Alternating current
BLR	Board-level reliability
CLK	Positive line of the differential pair of clock input signals that drives into the register (all register data inputs are sampled on the rising edge of their associated clocks)
$\overline{\text{CLK}}$	Negative line of the differential pair of clock input signals that drives into the register

CMOS	Complementary metal-oxide-silicon; a device technology that has balanced drive outputs and low power consumption
dc	Direct current
DDR	Double data rate
DIMM	Dual in-line memory module
FR4	Epoxy glass material used for manufacturing PCBs
IBIS	I/O buffer information specification
IC	Integrated circuit
JEDEC	Joint Electron Device Engineering Council
LFBGA	Low-profile fine-pitch ball grid array
LVCMOS	Low-voltage complementary metal-oxide-silicon
OEM	Original equipment manufacturer
PC-1600/2100	JEDEC-standard DIMMs using DDR-260 and DDR-266 SDRAM devices
PCB	Printed circuit board, also known as printed wire board (PWB)
PLL	Phase lock loop, also known as zero-delay clock buffer
PWB	Printed wire board, also known as printed circuit board (PCB)
SDRAM	Synchronous dynamic random access memory
SN74SSTV32852	24-bit to 48-bit registered buffer with SSTL_2 inputs and outputs
SPD	Serial presence detect EEPROM
SPICE	Simulation program with integrated circuit emphasis
SSTL_2	Stub series-terminated logic for 2.5 V
TI	Texas Instruments
TSSOP	Thin shrink small-outline package
VFBGA	Very-thin fine-pitch ball grid array
V_{OHP}	High-level output voltage peak
V_{OHV}	High-level output voltage valley
V_{OLP}	Low-level output voltage peak
V_{OLV}	Low-level output voltage valley

Appendix A Parameter Measurement Information



NOTES:
A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{TT} = V_{REF} = V_{DDQ}/2$
F. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ – 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure A–1. SSTV32852 Load Circuit and Voltage Waveforms

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