

Texas Instruments Enhanced Product Qualification and Reliability Report

TI qualification testing is a risk mitigation process that is engineered to assure device longevity in customer applications. Wafer fabrication processes and package level reliability are evaluated in a variety of ways that may include accelerated environmental test conditions with subsequent derating to actual use conditions. Manufacturability of the device is evaluated to verify a robust assembly flow and assure continuity of supply to customers. TI Enhanced Products are qualified with industry standard test methodologies performed to the intent of Joint Electron Devices Engineering Council (JEDEC) standards and procedures. Texas Instruments Enhanced Products are certified to meet GEIA-STD-0002-1 [Aerospace Qualified Electronic Components](#).

Qualification by Similarity (Qualification Family)

A new device can be qualified either by performing full scale quality and reliability tests on the actual device or using previously qualified device(s) through "Qualification by Similarity" (QBS) rules. By establishing similarity between the new device and those qualified previously, repetitive tests will be eliminated, allowing for timely production release. When adopting QBS methodology, the emphasis is on qualifying the differences between a previously qualified product and the new product under consideration. The QBS rules for a technology, product, test parameters or package shall define which attributes are required to remain fixed in order for the QBS rules to apply. The attributes which are expected and allowed to vary will be reviewed and a QBS plan shall be developed, based on the reliability impact assessment above, specifying what subset of the full complement of environmental stresses is required to evaluate the reliability impact of those variations. Each new device shall be reviewed for conformance to the QBS rule sets applicable to that device. See JEDEC JESD47 for more information.

Device Baseline			
<i>TI Device:</i>	74LVC1G3208MDBVTEP	<i>Assembly Site:</i>	ASEWH
<i>DLA VID:</i>	V62/13605-01XE	<i>Test Site:</i>	ASEWH
<i>Wafer Fab:</i>	FR-BIP-1	<i>Pin/Package Type:</i>	6 DBV SOT-23
<i>Fab Process:</i>	ASLNONC10	<i>Leadframe:</i>	Cu
<i>Fab Technology</i>	ASLNONC10	<i>Termination Finish:</i>	NiPdAu
<i>Die Revision:</i>	-	<i>Mount Compound:</i>	HENKEL C990J#316
<i>Die Name:</i>	RLVC1G3208IM	<i>Bond Wire:</i>	20.3 μm Au
<i>ESD CDM:</i>	1000V	<i>Mold Compound:</i>	SUMITOMO EME-G600
<i>ESD HBM:</i>	2000V	<i>Moisture Sensitivity:</i>	MSL 1 / 260°C

On-Going Life-Test Monitors For Technology		
<i>Reliability:</i>	0.5	FIT
<i>MTBF:</i>	1.99x10 ⁹	Hours
<i>Confidence Level:</i>	60	%
<i>Activation Energy:</i>	0.7	eV
<i>Stress Temperature:</i>	125	°C
<i>Derated Use Temperature:</i>	55	°C
<i>Test Duration:</i>	1000	Hours
<i>Sample Size:</i>	23240	Units
<i>Number of Failures:</i>	0	Units

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Enhanced Products New Device Qualification Matrix				
Note that qualification by similarity ("qualification family") per JEDEC JESD47 is allowed				
Description	Condition	Sample Size Used/Rejects	Lots Required	Test Method
<i>Electromigration</i>	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
<i>Wire Bond Life</i>	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
<i>Electrical Characterization</i>	TI Data Sheet	15	3	N/A
<i>Electrostatic Discharge Sensitivity</i>	HBM CDM	3 units/voltage	N/A	EIA/JESD22-A114 EIA/JESD22-C101
<i>Latch-up</i>	Per Technology	5/0	3	EIA/JESD78
<i>Physical Dimensions</i>	TI Data Sheet	5/0	1	EIA/JESD22- B100
<i>Thermal Impedance</i>	Theta-JA on board	Per Pin-Package	N/A	EIA/JESD51
<i>Bias Life Test</i>	125°C / 1000 hours or equivalent	45/0	3	JESD22-A108*
<i>Biased Humidity</i> or <i>Biased HAST</i>	85°C / 85% / 1000 hours or 130°C / 85% / 96 hours	77/0	3	JESD22-A101* JESD22-A110*
<i>Extended Biased Humidity</i> or <i>Extended Biased HAST</i>	85°C / 85% / 2600 hours (for reference) or 130°C / 85% / 250 hours (for reference)	77/0	1	JESD22-A101* JESD22-A110*
<i>Unbiased HAST</i>	130°C / 85% / 96 hours	77/0	3	JESD22-A.118*
<i>Temperature Cycle</i>	-65°C to +150°C non-biased for 500 cycles	77/0	3	JESD22-A104*
<i>Solder Heat</i>	260°C for 10 seconds	22/0	1	JESD22-B106
<i>Resistance to Solvents</i>	Ink symbol only	12/0	1	JESD22-B107
<i>Solderability</i>	Condition A (steam age for 8 hours)	22/0	1	ANSI/J-STD-002-92
<i>Flammability</i>	Method A / Method B	5/0	1	UL-1964
<i>Bond Shear</i>	Per wire size	5 units x 30/0 bonds	3	JESD22-B116
<i>Bond Pull Strength</i>	Per wire size	5 units x 30/0 bonds	3	ASTM F-459
<i>Die Shear</i>	Per die size	5/0	3	TM 2019
<i>High Temp Storage</i>	150 °C / 1,000 hours	15/0	3	JESD22-A103-A*
<i>Moisture Sensitivity</i>	Surface Mount Only	12	1	J-STD-020-A*

*Precondition performed per JEDEC Std. 22, Method A112/A113

For additional information or technical support please contact the Texas Instruments Customer Support Center at www.ti.com/support or send an email to support@ti.com

For more information on TI Enhanced Products please visit www.ti.com/ep

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