EVM User's Guide: TPLD1201

TPLD1201-RWB-EVM Evaluation Module

Description

The TPLD1201RWB evaluation module (EVM) is part of the TI Programmable Logic Device (TPLD) family of devices that feature versatile programmable logic ICs with combinational logic, sequential logic and mixed-signal functions to provide an integrated, compact, low power design to implement common system functions, such as timing delays, voltage monitors, system resets, power sequencers, and I/O expanders.

The TPLD1201 helps users to configure TPLD1201RWB devices without requiring the soldering of the devices to the board. Users can utilize InterConnect Studio (ICS) for fast evaluation, development, simulation, and programming. Once programmed, TPLD devices can be removed from the socket and placed in a user's system.

Get Started

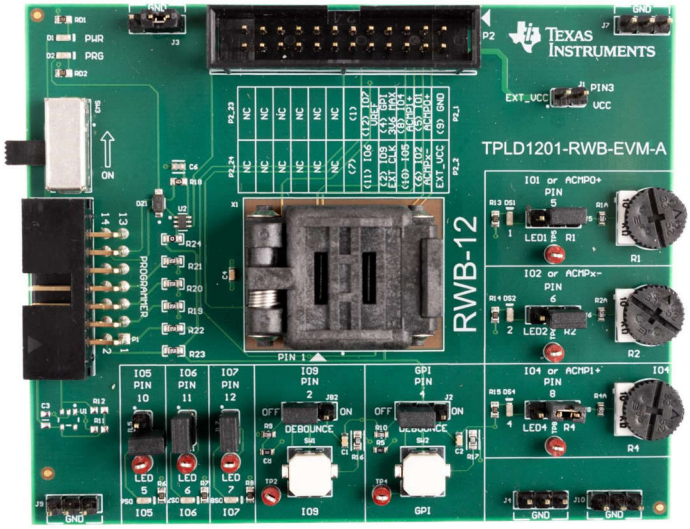
1. Order the TPLD1201-RWB-EVM and TPLD-PROGRAM
2. Download the latest version of InterConnect Studio (ICS)
3. Use the cables included the TPLD-PROGRAM kit to connect the system
4. Place an unprogrammed TPLD1201RWB into the socket and configure using ICS

Features

- RWB socket for easy programming and evaluation of TPLD1201RWB
- Input buttons, potentiometers, and output LEDs for quick evaluation
- Header pins and test points for interfacing with custom systems
- Interfaces with TPLD-PROGRAM using a standard keyed 14-pin cable

Applications

- Factory automation and control
- Communications equipment
- Retail automation and payment
- Test and measurement
- Pro audio, video and signage
- Personal electronics



1 Evaluation Module Overview

1.1 Introduction

This user's guide contains support documentation for the TPLD1201RWB evaluation module (EVM). Included is a description of how to set up and configure the EVM, how to use the EVM in conjunction with a TPLD-PROGRAM board, and how to use InterConnect Studio to configure the TPLD1201. Also included are the printed circuit board (PCB) layout, the schematic, and the bill of materials (BOM) of the TPLD1201-RWB-EVM.

Note

To program devices, the TPLD-PROGRAM board and InterConnect Studio are required.

TI only supports the use of the cables provided in the TPLD-PROGRAM kit to interface between the EVM and the programmer board.

1.2 Kit Contents

Table 1-1. TPLD1201-RWB-EVM Kit Contents

Item	Description	Quantity
TPLD1201-RWB-EVM	PCB	1
TPLD1201RWB	12-pin TI Programmable Logic Device	5
Quick start guide	Guide to setup system	1

1.3 Specification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Vcc	Powered by programmer		3.3		V
Vcc	External Power	1.71		5.5	V
Vi	Per pin input	0		Vcc	V
Vo	Per pin output	0		Vcc	V
GPI	Input	0		Vcc	V

1.4 Device Information

The TPLD1201 is part of the TI programmable logic device (TPLD) family of devices that features configurable I/O structures that extends compatibility within mixed-signal environments, reducing the number of discrete components required. System designers can create circuits and configure the macro-cells, I/O pins, and interconnections by temporarily emulating the non-volatile memory or by permanently programming the one-time programmable (OTP) through InterConnect Studio.

2 Hardware

2.1 Functional Blocks

This section covers the different functional blocks of the TPLD1201-RWB-EVM.

2.1.1 Test Points

Each GPIO and GPI pin of an socketed TPLD1201RWB part is connected directly to a test point to allow a user to access each pin of the device for probing and testing. The pins are connected to test points as follows:

Pin Number	IO name	Test Point
2	IO9	TP2
4	GPI	TP4
8	IO4	TP8
5	IO1	TP5
6	IO2	TP6
10	IO5	TP10
11	IO6	TP11
12	IO7	TP12

Each test point is connected directly to the corresponding pin, so any disconnected header pins do not disconnect the test points from the pins.

2.1.2 Programmer Header Block (P1)

The programmer header block accepts the 14-position cable used to connect the TPLD1201-RWB-EVM to the TPLD-PROGRAM. TI recommends using this header to connect only to the TPLD-PROGRAM using the cables included in the TPLD-PROGRAM kit. The header is keyed, so the 14-position cable can only be inserted to the case with the key facing the correct direction. To connect the TPLD1201-RWB-EVM to a TPLD-PROGRAM, follow the steps in Section 3.2.

SW3 connects the 3V3 line of the programmer header to the VCC line of the EVM. When powering the EVM from the TPLD-PROGRAM, the 3V3 line must be in the ON position.

2.1.3 External Connection Header Block

The P2 header block is intended to be used to interface the TPLD1201-RWB-EVM with an external system. Using the guide printed on the EVM silkscreen, the TPLD pins can be interfaced with an external system to allow for prototyping and testing in customer systems. When supplying power to the TPLD using the P2 header block, SW3 needs to be in the OFF position and a shunt placed on J1, connecting the external VCC supply from P2 (VCC_EXT) to the VCC net of the EVM. TI recommends not connecting the board to an external system and to the TPLD-PROGRAM at the same time to avoid the risk of damage to the TPLD-PROGRAM and the external system.

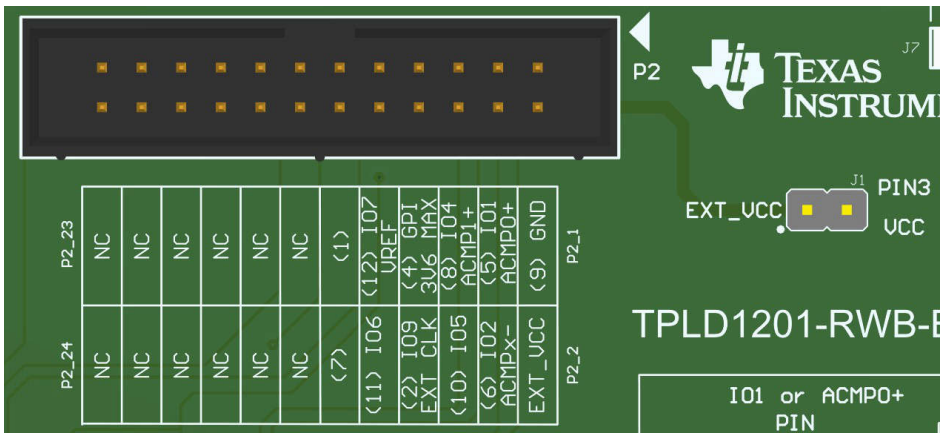


Figure 2-1. P2 and J1 Headers

2.1.4 GPI Protection Block

During the permanent programming process, 8 V is applied to the GPI pin of the TPLD. This circuit prevents the voltage at P2 from exceeding 3.3 V.

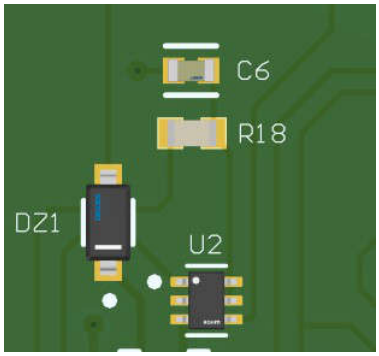


Figure 2-2. GPI Protection Block

2.1.5 RWB Socket

The RWB socket for testing and programming TPLD devices without soldering a device to the EVM.

To place a device in the socket, follow the steps in Section 3.2.

2.2 GPIO Testing Blocks

The 8 GPIO pins on the device are connected to various testing blocks to allow for prototyping. These connections are indicated by the table below.

Pin Number	IO Name	Testing Block	Testing Block Name
10	IO5	LED	LED5
11	IO6	LED	LED6
12	IO7	LED	LED7
2	IO9	SW	SW1
4	GPI	SW	SW2
8	IO4	LED/POT	LED4/R4
6	IO2	LED/POT	LED2/R2
5	IO1	LED/POT	LED1/R1

2.2.1 LED Blocks

Each LED block consists of an LED that can be connected or disconnected from the TPLD pin via a header. To connect the LED to the corresponding pin, place a shunt on the corresponding header between the two header pins.

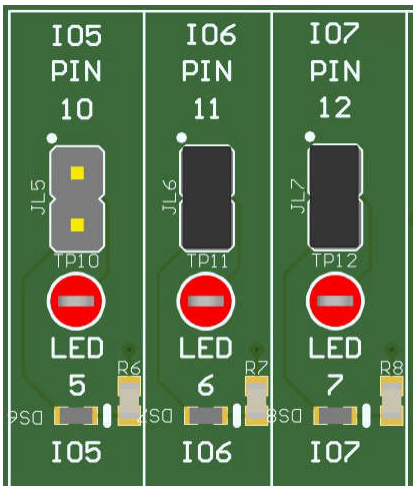


Figure 2-3. LED Blocks

2.2.2 Switch Blocks

Each SW block consists of a tactile switch and an optional debounce circuit. The switch can be connected to the corresponding TPLD pin via a 3-position header. One side of the 3-position header, labeled OFF, connects directly to the switch output, and the other side of the 3-position header, labeled ON, connects to a debounce circuit leading to the switch output. The middle pin of the header connects to the corresponding TPLD pin. To connect directly to the switch output, place a shunt between the middle pin of the header and the OFF pin. To connect to the debounce circuit, place a shunt between the middle pin of the header and the OFF pin. If no shunt is placed between either set of pins, the switch is not connected to the TPLD pin.

Note

The debounce circuit must not be connected on the GPI pin during programming.

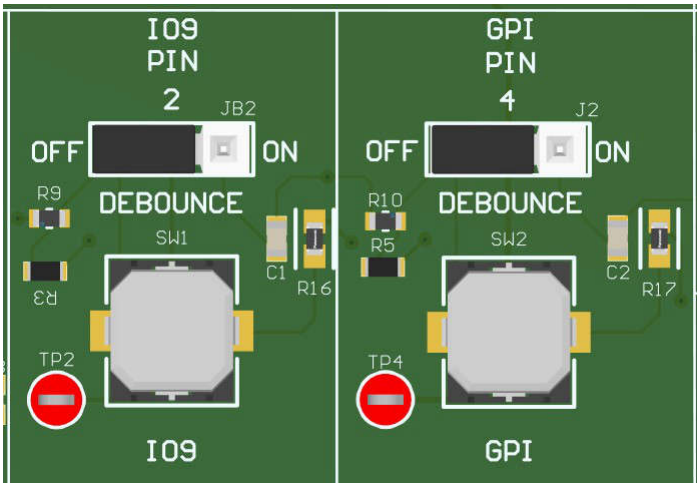


Figure 2-4. Switch Blocks

2.2.3 LED/Potentiometer Blocks

Each LED/POT block consists of a 3-state header pin that can be used the connect the corresponding GPIO pin to either a analog voltage source or an LED. The middle pin of the header connects to the corresponding GPIO pin of the TPLD. The left side of the header pin, marked LED, connects to the LED. The right side of the header pin, marked R, leads to the analog voltage source. To connect the corresponding GPIO to the LED, place a shunt between the middle pin and the LED pin. To connect the GPIO to the analog voltage source, place a shunt between the middle pin and the R pin.

The analog voltage source consists of a voltage divider using a POT. When the POT is turned fully clockwise, the analog voltage source outputs at most 0.2 V. When the POT is turned fully counterclockwise, the analog voltage source outputs at least VCC - 0.2 V.

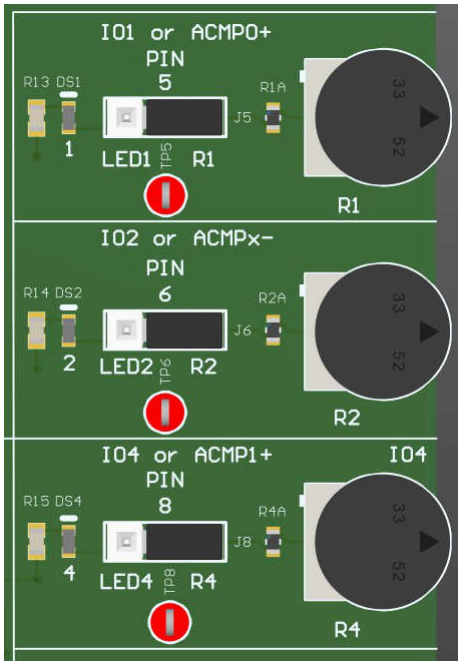


Figure 2-5. LED/POT Blocks

3 Software

3.1 Using the TPLD1201-RWB-EVM

This section covers using the TPLD1201-RWB-EVM to demo and program TPLD1201, using the TPLD1201 EVM Demo file as an example. For more help using InterConnect Studio (ICS) to create your own circuit, see the InterConnect Studio User's Guide.

3.1.1 Equipment Needed for Programming

To program a TPLD device with the TPLD1201-RWB-EVM, a TPLD-PROGRAM kit and a computer running InterConnect Studio are needed. The TPLD-PROGRAM kit includes everything required to interface a computer to the TPLD1201-RWB-EVM. InterConnect Studio can be downloaded from TI.com by following the instructions in Section 3.1.2.

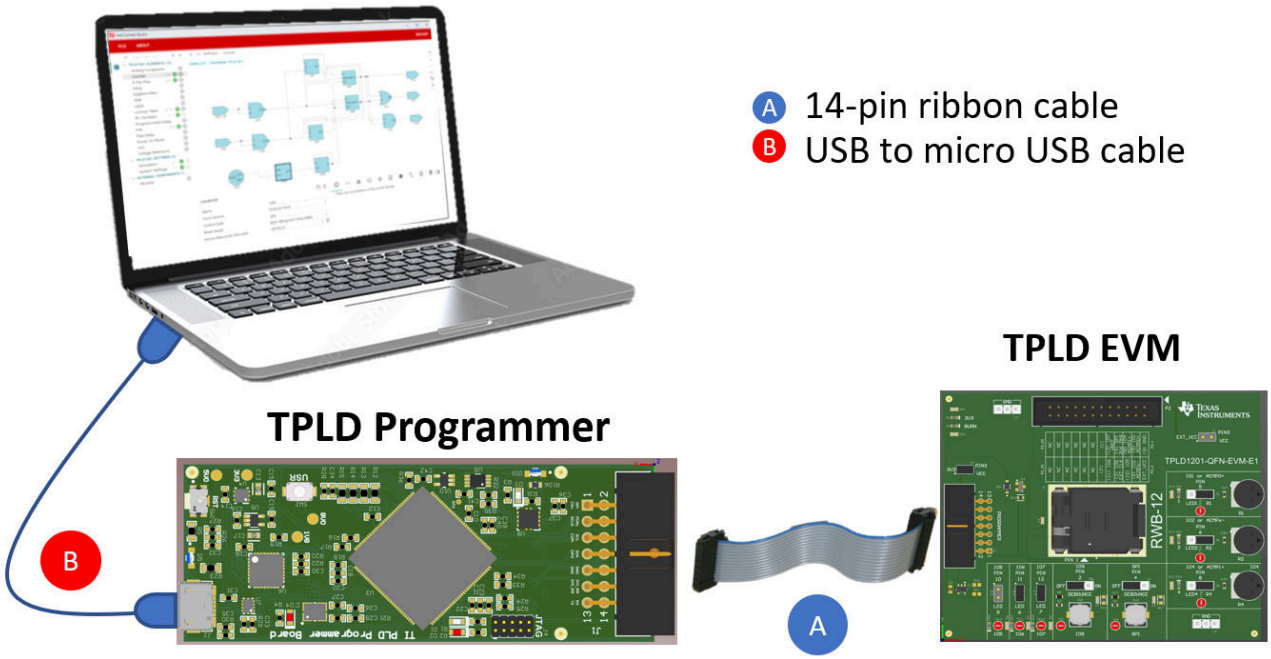


Figure 3-1. Connecting a TPLD EVM and Programmer

3.1.2 Installing Software

InterConnect Studio (ICS) is available free of charge at interconnect_studio.itg.ti.com

For more information on using InterConnect Studio (ICS), reference the InterConnect Studio User's Guide.

3.2 Configuring a TPLD Device

This section covers the steps to use the TPLD1201-RWB-EVM and a TPLD-PROGRAM kit to program a TPLD1201RWB.

3.2.1 TPLD1201-RWB-EVM Setup for Programming

Make sure that the following conditions are met:

1. Set SW3 to the ON position.
2. Set the GPI Pin 4 jumper (J2) to the OFF position or remove the jumper
3. Remove the EXT_VCC (J1) jumper
4. Disconnect P2 from any external system

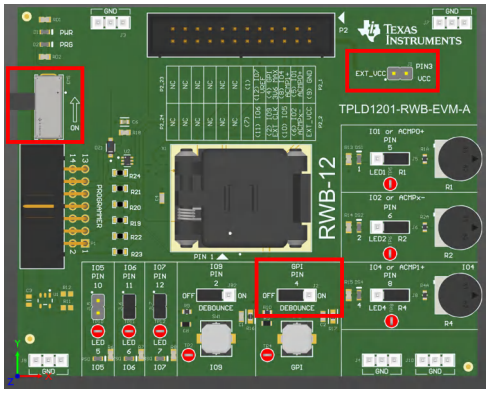


Figure 3-2. Components Considered in Programming Setup

3.2.2 Inserting a TPLD1201RWB into the RWB Socket

Do not remove, replace, or add a TPLD device to or from a powered board. Do not place fingers inside the socket or touch the contacts on the bottom of the socket. TI recommends following typical ESD protection procedures while handling the TPLD1201RWB.

1. Open the socket by gently pulling the latch until the lid snaps open.
2. Make sure that the socket is clean by blowing off socket contacts and device pads with clean compressed air.
3. Use a vacuum pen or antistatic tweezers to guide the part into the socket, aligning pin 1 of the part to pin 1 of the socket as shown below.
4. Close the socket lid until the latch snaps and holds the lid in place.

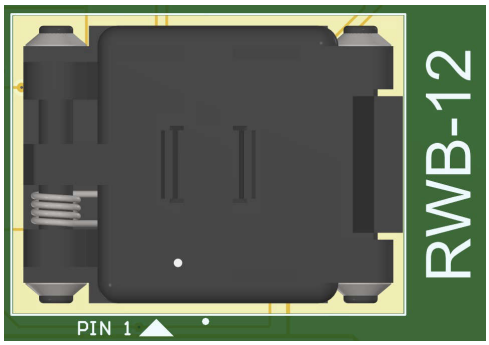


Figure 3-3. RWB Socket

3.2.3 Connecting the TPLD1201-RWB-EVM to a TPLD-PROGRAM Board

All cables included are keyed and can only be plugged in when facing the correct direction. If a cable cannot be inserted with the application of a gentle amount of force, try swapping the orientation of the cable and making sure that the header housings are unobstructed before trying again. Forcing the connections can cause damage to the cables and boards.

1. Connect the programmer board to a computer running InterConnect Studio using the provided USB cable. Make sure that a good connection is made between the TPLD-PROGRAM and the computer, indicated by the two blue LEDs on the TPLD-PROGRAM both being on. An example of a fully connected EVM can be seen in Figure 3-1.
2. Connect the TPLD-PROGRAM to the TPLD1201-RWB-EVM using the provided 14-position ribbon cable. Make sure that a good connection is made between the TPLD1201-RWB-EVM and the TPLD-PROGRAM, indicated by the 3V3 LED in the top left of the EVM being on.

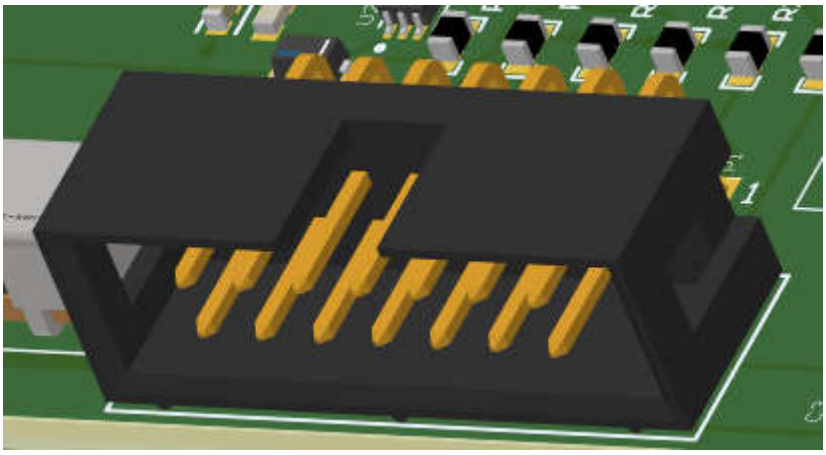


Figure 3-4. Keyed Header Socket

3.2.4 Temporarily Configuring a TPLD Device

This section covers using InterConnect Studio to configure a TPLD1201 using a pre-built demo circuit.

When the TPLD is temporarily configured, removing power from the device causes the TPLD to reset and the configured circuit to be erased. The TPLD can be reconfigured multiple times without needing to be reset between configurations.

1. Open InterConnect Studio on the computer to which the TPLD-PROGRAM is connected. Under *Design*, select *TPLD1201*. Under *Part:*, select *Default*. Under *Package:*, select *RWB (X2QFN, 12)*.
2. Search for *TPLD1201 EVM Demo* and select the demo from the list of pre-designed circuits, or select *Empty Design* to build a custom circuit.

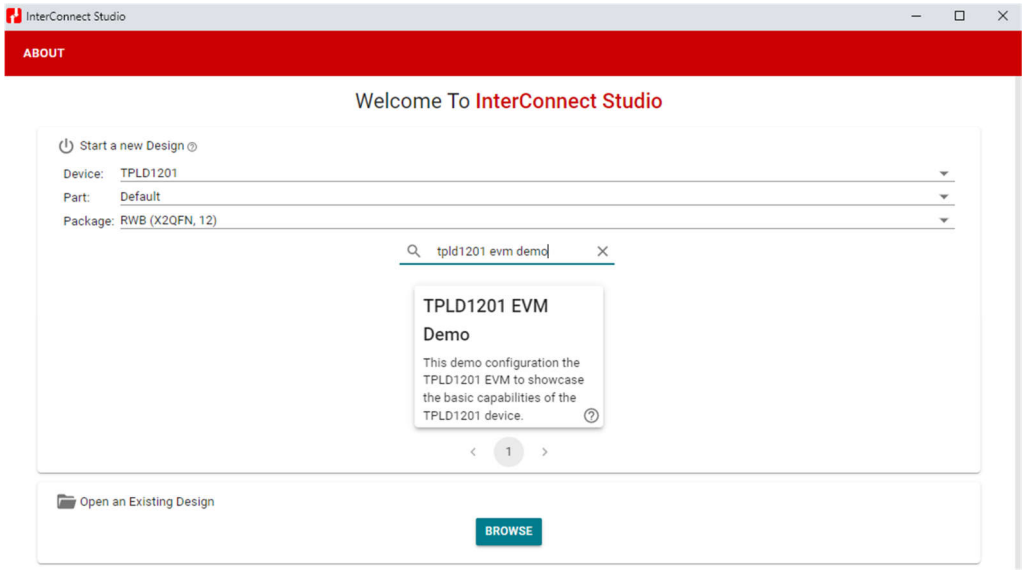


Figure 3-5. Selecting the Demo in ICS

See Section 3.3 for more details about the demo.

3. InterConnect Studio opens the chosen circuit.
4. Select *CONFIGURE TPLD1201* in the top left corner of InterConnect Studio to configure the TPLD in the socket of the EVM with the circuit shown by InterConnect Studio. Select the serial port connected to the TPLD-PROGRAM, then select *OK*.

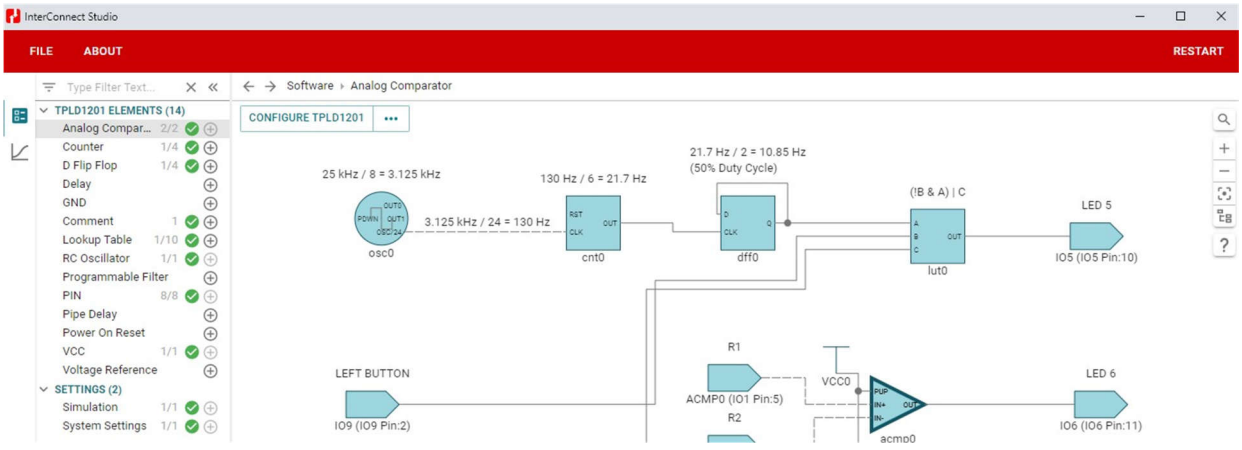


Figure 3-6. Temporarily Configuring in ICS

a. Some LEDs on the TPLD1201-RWB-EVM flash during the programming sequence, which is normal.
b. If the configuration fails, check the connections between the EVM and the computer, make sure SW3 is ON, check the connection between the TPLD device and the socket contacts, and retry.

Once the programming sequence is completed, the TPLD device on the board is temporarily configured with the circuit built in InterConnect Studio. The configured circuit can be tested using the buttons, potentiometers and LEDs provided on the EVM.

3.2.5 Permanently Programming a TPLD Device

This section covers using InterConnect Studio to permanently program a TPLD1201. Permanently programmed devices retain the configuration the devices are programmed with after power is reset.

Permanently programmed devices must not be permanently programmed again to avoid damaging the device.

1. Open the desired configuration to be permanently programmed in the TPLD1201 in InterConnect Studio.
2. Open the Configure Settings by selecting the three dots icon beside the *CONFIGURE TPLD1201* button.
3. Select *Permanently Configure Device*. If using a TPLD-PROGRAM to power the EVM, then leave the Power Source as *Programmer*. Select *OK*.

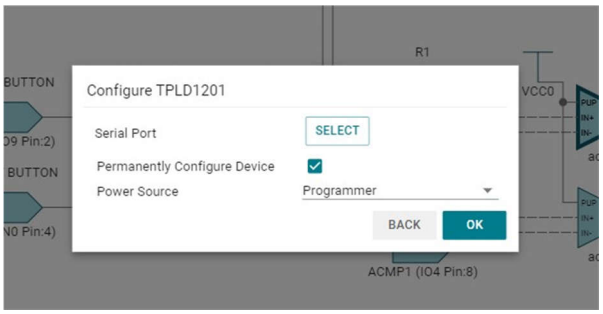


Figure 3-7. Permanent Programming in ICS

4. Select the serial port connected to the TPLD-PROGRAM, then select *OK* again.
   a. Some LEDs on the TPLD1201-RWB-EVM can flash during the programming sequence, which is normal.
   b. If the configuration fails, then check the connections between the EVM and the computer, make sure SW3 is ON, check the connection between the TPLD device and the socket contacts, and retry.
5. Remove power from the EVM before removing the permanently programmed TPLD1201.

3.3 Testing with the TPLD1201-RWB-EVM Demo

This section is intended to be an example on how to use the TPLD1201-RWB-EVM to test a temporarily configured circuit. The TPLD1201 demo is designed to show the key functions of the TPLD1201, such as the internal oscillators, flip-flops, counters, gates, and analog comparators.

3.3.1 TPLD1201 Demo Circuit

The TPLD1201 demo has four elements: analog inputs, digital inputs, digital outputs, and internal modules.

The demo has three analog inputs: ACMP0 (IO1), ACMPx (IO2) and ACMP1 (IO4). These inputs are fed into a pair of analog comparators, acmp0 and acmp1, which drive the digital outputs IO6 and IO7 respectively. When IO1 is held at a higher voltage than IO2, acmp0 drives IO6 high. When IO4 is held at a higher voltage than IO2, acmp1 drives IO7 high.

The demo uses an internal oscillator (osc0) with a frequency of 25 kHz, which is divided by eight to 3.125 kHz. A binary counter (cnt0) further divides the frequency by 24 Hz to 130 Hz, before using the divided oscillator as an input. The counter counts to 6, then outputs a high pulse and resets the count, effectively dividing the frequency of the signal by 6 to 21.7 Hz. The output of the binary counter is used as the clock input of a flip-flop (dff0) with an inverted output that is used as the data input, reducing the frequency of the signal to 10.85 Hz and changing the signal from being a pulse to a signal with a 50% duty cycle. The output of the flip-flop is then used as the A input of a look-up table (lut0).

The demo uses two digital inputs: IO9 and GPI. The two digital inputs are fed into the B and C inputs of the look-up table lut0, respectively. The look-up table uses the equation (!B & A) | C, so when neither of the digital inputs are high, the output of the look-up table follows the A input, which is the output of the flip-flop (dff0). When the GPI input is high, the look-up table outputs high, and when the IO9 input is high, the look-up table outputs low. The output of the look-up table drives the digital output IO5.

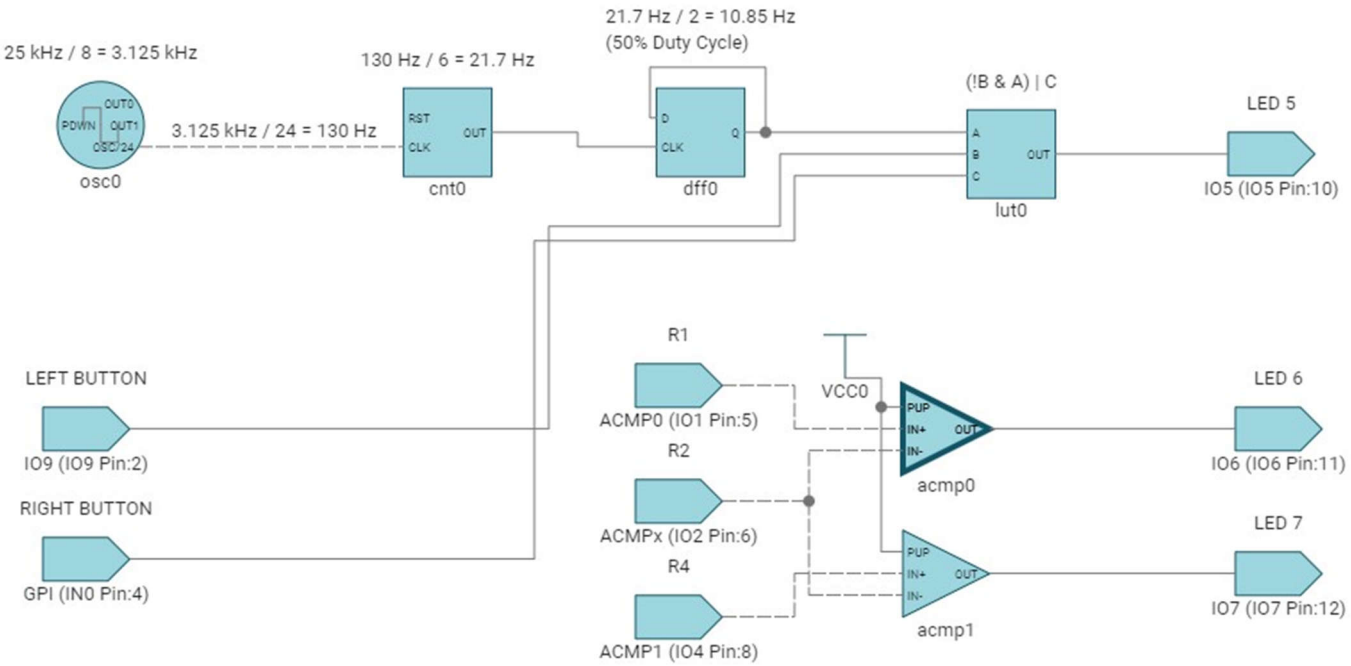


Figure 3-8. TPLD1201 EVM Demo

3.3.2 Testing the Demo

To test the demo as intended, set up the EVM with the following header connections:

1. Jumper on pin 10 header (JL5), pin 11 header (JL6), and pin 12 header (JL7)
2. Jumper on pin 2 header (JB2) between the middle pin and OFF
3. Jumper on pin 4 header (J2) between the middle pin and OFF
4. Jumper on pin 8 header (J8) between the middle pin and R4
5. Jumper on pin 6 header (J6) between the middle pin and R2
6. Jumper on pin 5 header (J5) between the middle pin and R1
7. SW3 in the ON position

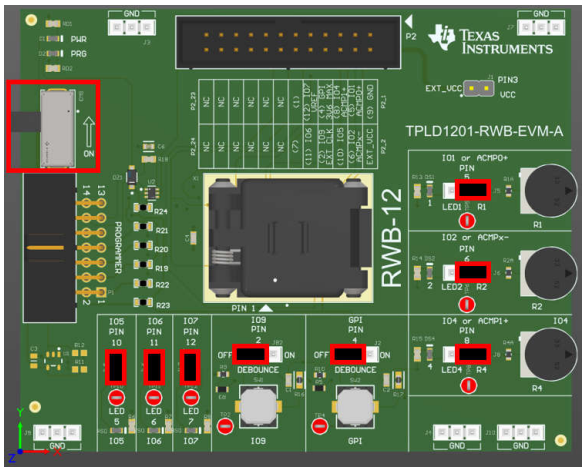


Figure 3-9. Headers and Switches used in Demo Configuration

Once the EVM is setup, first configure a blank TPLD1201RWB with the demo by following the steps in Section 3.2. Once the demo is correctly configured onto the TPLD on the EVM, LED5 begins flashing. Pressing the SW1 button turns LED5 off. Pressing the SW2 button turns LED5 on.

IO1, IO2, and IO4 are controlled by the potentiometers R1, R2, and R4, respectively. Turning the potentiometers clockwise increases the voltage supplied to the input pins, and turning the potentiometers counterclockwise decreases the voltage supplied to the input pins. R2 controls the negative input voltage reference to both analog comparators of the device. Set R2 to a middle value, then move R1 to see the trigger of the analog comparator ACMP0, output to LED6. Similarly, R4 can be turned to see the trigger of the analog comparator ACMP1 on LED7.

4 Hardware Design Files

4.1 Schematics

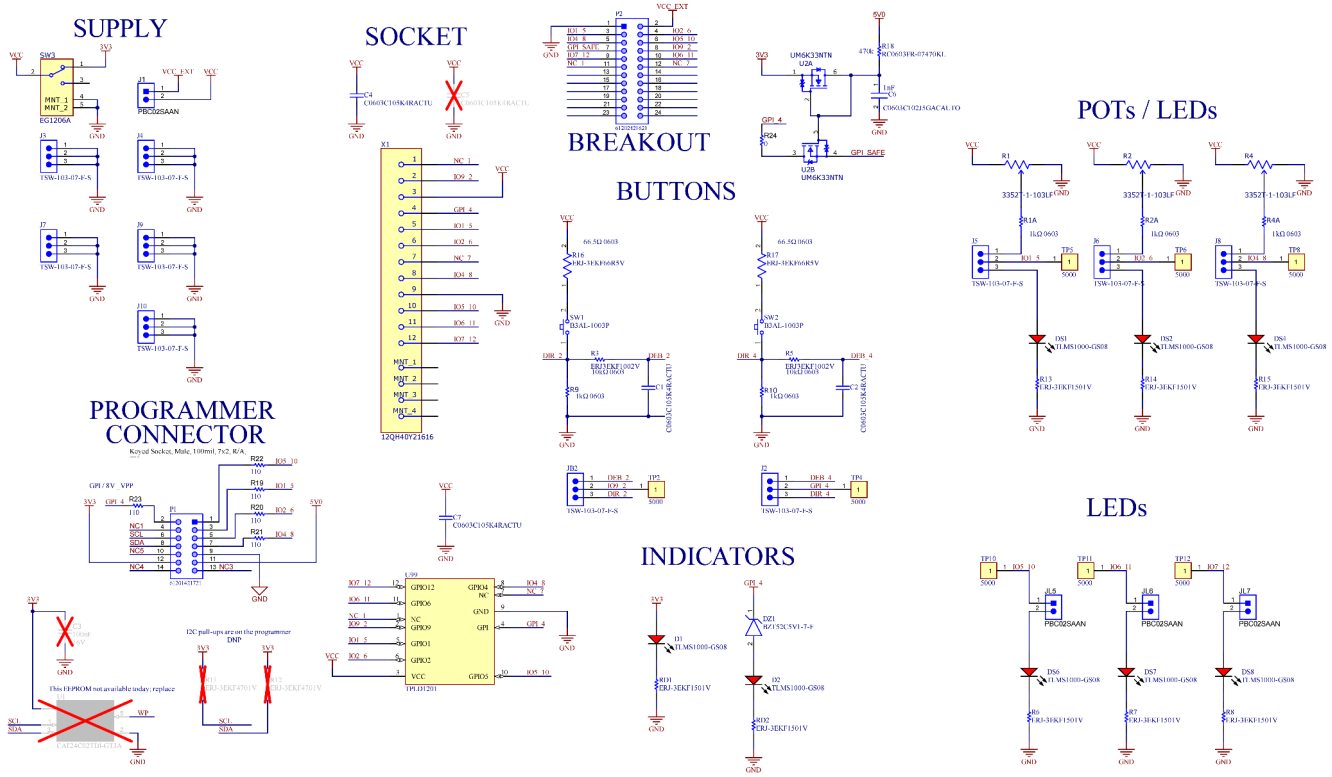


Figure 4-1. TPLD1201-RWB-EVM Schematic

4.2 PCB Layout

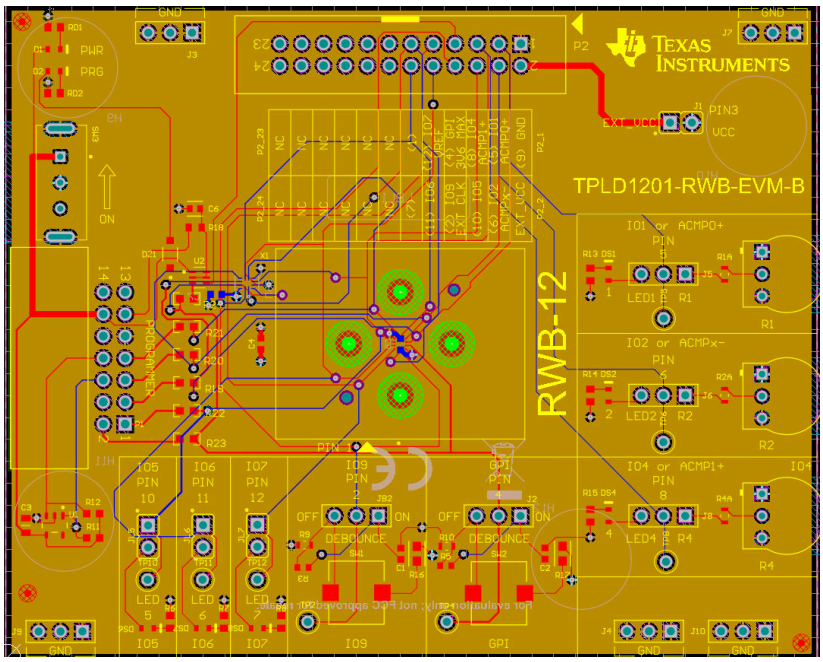


Figure 4-2. TPLD1201-RWB-EVM Layout

4.2.1 PCB Overview

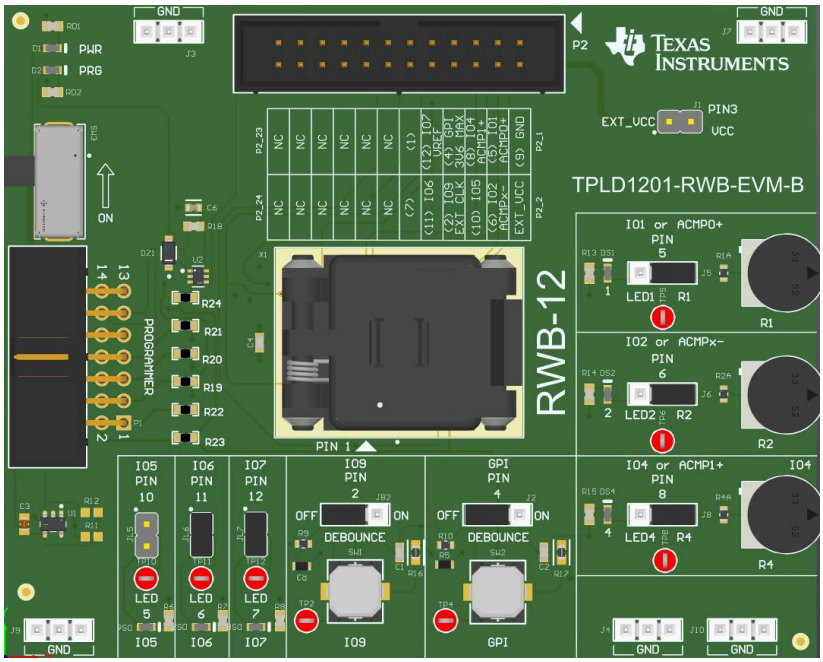


Figure 4-3. TPLD1201-RWB-EVM Board Front

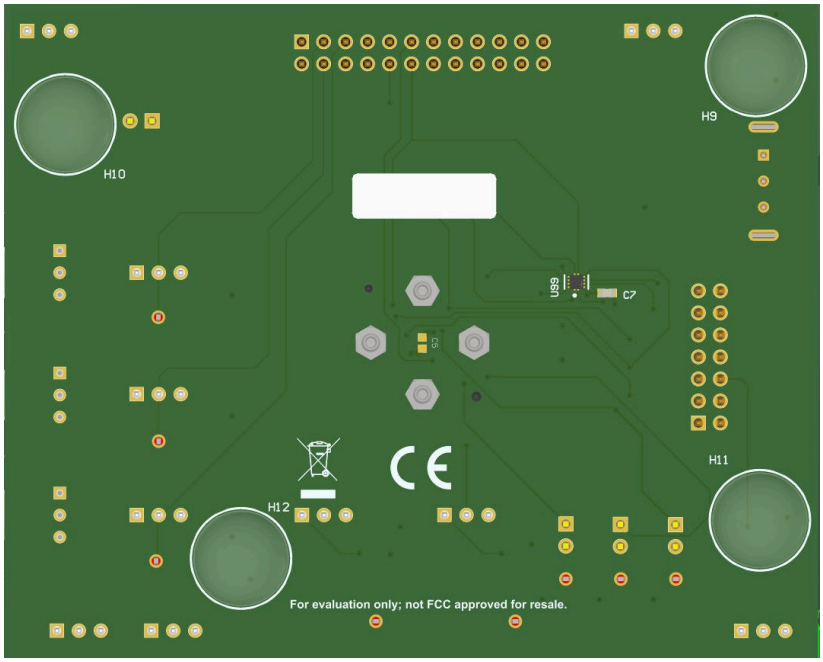


Figure 4-4. TPLD1201-RWB-EVM Board Bottom

4.3 Bill of Materials

This section provides information on the components that can be used with the TPLD1201-RWB-EVM. Other components can be used as long as the components are able to fit the provided plated holes and pads.

Table 4-1. Bill of Materials

Designator	Item	Value	Manufacture	Part Number
C1, C2, C4, C5	Capacitor	1 uF	Yageo	C0603C105K4RACTU
C3	Capacitor	DNP	Knowles Syfer	060330160104JXT
C6	Capacitor	1000 pF	KEMET	C0603C102J5GACAUTO
D1, D2, DS1, DS2, DS4, DS6, DS7, DS8	LED	Red	Vishay	TLMS1000-GS08
DZ1	Diode	5.1 V	Diodes	BZT52C5V1-7-F
H9, H10, H11, H12	Bumpon	Clear	3M	SJ-5303 (CLEAR)
J1, JL5, JL6, JL7	Header	2x1	Sullins	PBC02SAAN
J2, J3, J4, J5, J6, J7, J8, J9, J10, JB2	Header	3x1	Samtec	TSW-103-07-F-S
P1	Header	7x2	Wurth Electronics	61201421721
P2	Header	12x2	Wurth Electronics	61202421621
R1, R2, R4	Resistor	10 kΩ	Bourns	3352T-1-103LF
R1A, R2A, R4A, R9, R10	Resistor	1 kΩ	Vishay	CRCW06031K00FKEAC
R3, R5	Resistor	10 kΩ	Bourns	ERJ3EKF1002V
R6, R7, R8, R13, R14, R15, RD1, RD2	Resistor	1.5 kΩ	Panasonic	ERJ-3EKF1501V
R11, R12	Resistor	DNP	Yageo	ERJ-3EKF4701V
R16, R17	Resistor	66.5 Ω	Panasonic	ERJ-3EKF66R5V
R18	Resistor	470 kΩ	Yageo	RC0603FR-07470KL
R24	Resistor	0 Ω	Stackpole Electronics Inc	RMCF0603ZT0R00
R19, R20, R21, R22, R23	Resistor	110 Ω	Vishay Dale	CRCW0603110RJNEA
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	Shunt		Sullins Connector Solutions	SPC02SYAN
SW3	Switch	Slide	E-Switch	EG1206A
SW1, SW2	Switch	Tactile	Omron	B3AL-1003P
TP2, TP4, TP5, TP6, TP8, TP10, TP11, TP12	Test Point	Red	Keystone Electronics	5000
U1	EEPROM	DNP	Microchip / Atmel	CAT24C02TDI-GT3A
U2	Transistor		Rohm	UM6K33NTN
X1	Socket	RWB	Plastronics	12QH40Y21616

5 Additional Information

Trademarks

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6 References

1. Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2023) to Revision B (October 2024)	Page
• Updated marketing status to initial release	1

Changes from Revision * (November 2023) to Revision A (November 2023)	Page
• Updated hardware image	1
• Updated *Device Information* section	2

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