Functional Safety Information

TPS1211x-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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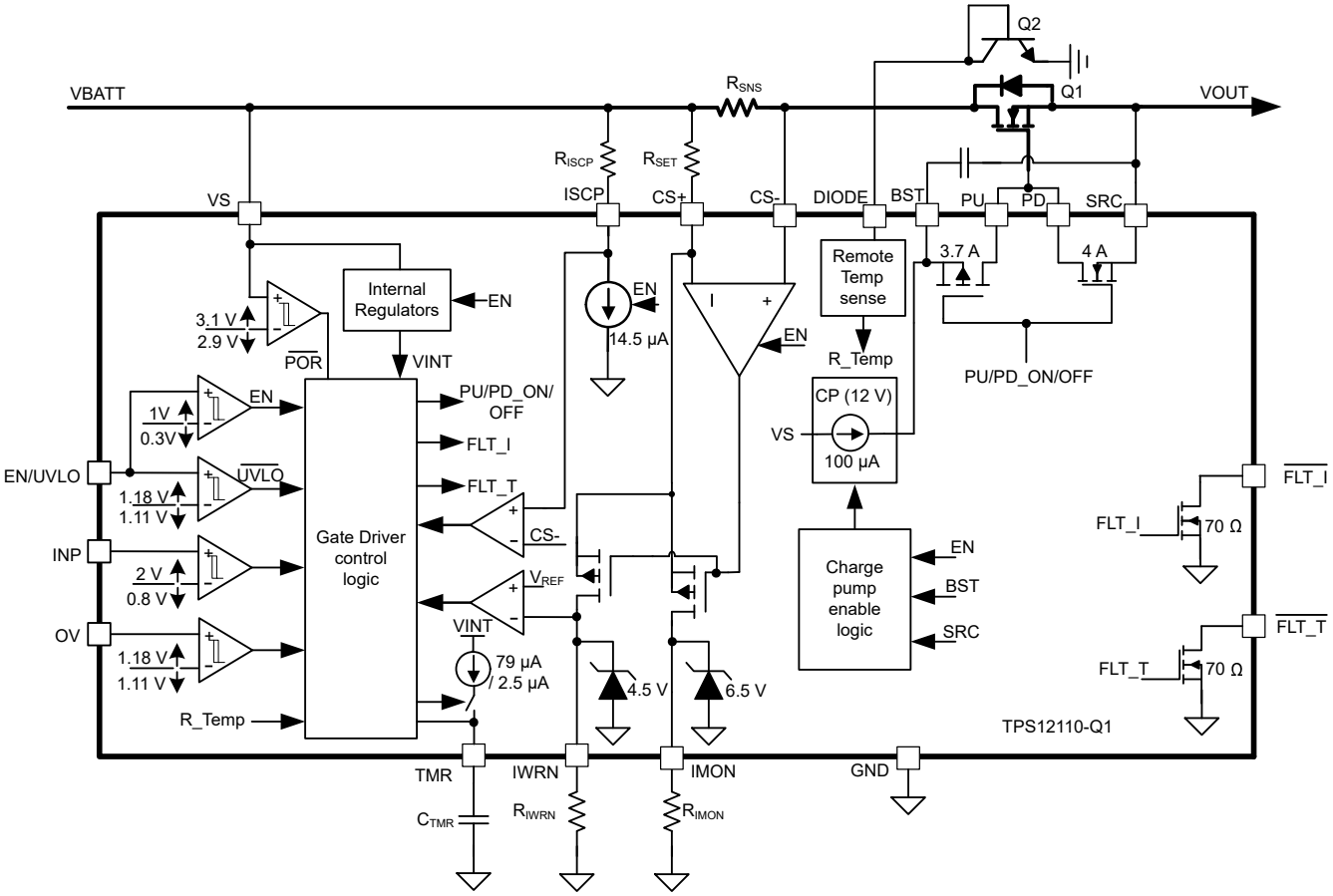
Trademarks

1 Overview

This document contains information for TPS1211x-Q1 (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



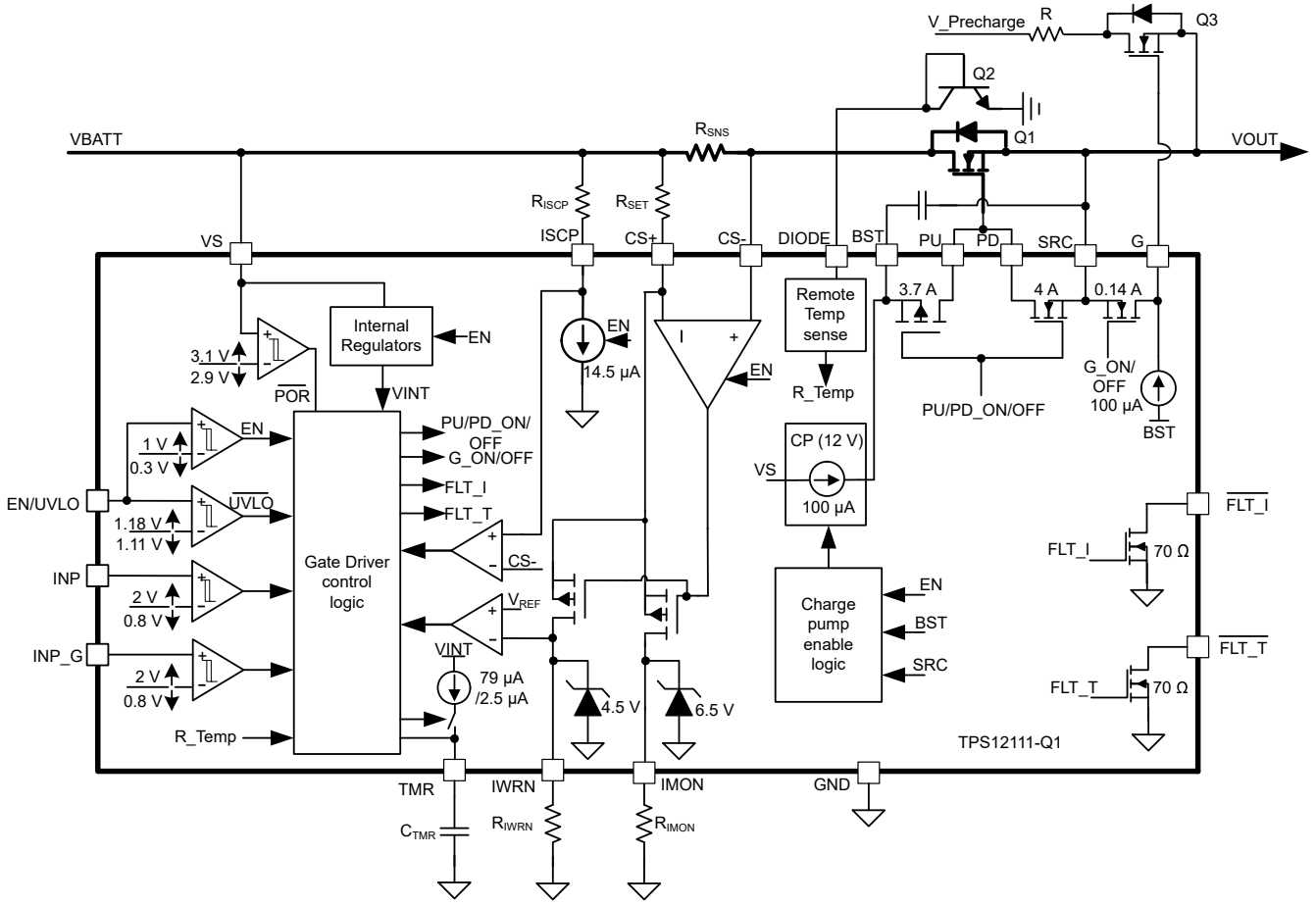


Figure 1-1. Functional Block Diagram

TPS1211x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS1211x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	9
Die FIT Rate	3
Package FIT Rate	6

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 27 mW
- Climate type: World-wide Table 8 IEC TR 62380
- Package factor (lambda 3): Table 17b IEC TR 62380
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS1211x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Gate output stuck high	13%
Gate output stuck low	40%
Gate output functional, not in specification voltage or timing	33%
Short circuit protection fails to trip or false trip	2%
IMON not in specification - current or timing	5%
UVLO, OV, TSD fails to trip or false trip	2%
Pin to Pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS1211x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-2)
- Pin short-circuited to an adjacent pin (see Table 4-2)
- Pin short-circuited to supply (see Table 4-2)

Table 4-2 through Table 4-2 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS1211x-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS1211x-Q1 data sheet.

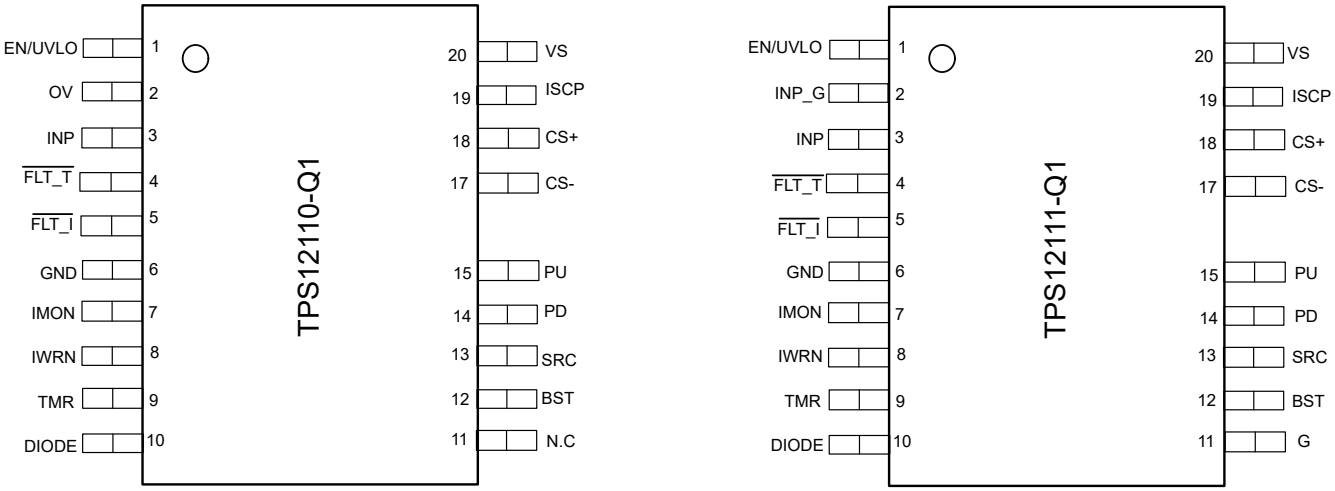


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follow data sheet recommendation for operating conditions, external component selection and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Normal operation. The device is disabled.	B
OV	2	TPS12110-Q1 only. OV functionality is disabled.	B
INP_G	2	TPS12111-Q1 only. Normal operation. The G output is low and the external pre-charge FET is off.	B
INP	3	Normal operation. The PD output is low and the external FET is off.	B
$\overline{\text{FLT\_T}}$	4	Overtemperature fault diagnostic cannot be reported.	B
$\overline{\text{FLT\_I}}$	5	Overcurrent fault diagnostic cannot be reported.	B
GND	6	Normal operation	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IMON	7	IMON output cannot be reported	B
IWRN	8	Overcurrent does not get detected hence overcurrent protection gets disabled.	B
TMR	9	Overcurrent does not get detected hence overcurrent protection gets disabled.	B
DIODE	10	Overtemperature does not get detected hence overtemperature protection gets disabled.	B
N.C	11	TPS12110-Q1 only. No effect.	D
G	11	TPS12111-Q1 only. With G grounded, if the pin voltage between SRC and G exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
BST	12	Gate Driver supply does not come up. FETs remain OFF.	B
SRC	13	Short to GND protection kicks in.	B
PD	14	With PD grounded, if the pin voltage between SRC and PD exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
PU	15	Gate Driver supply gets short circuited. FETs remain OFF.	B
CS-	17	Short circuit of input supply	B
CS+	18	With CS+ grounded, if the pin voltage between CS+ and CS– exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
ISCP	19	With ISCP grounded, if the pin voltage between ISCP and CS– exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
VS	20	Device supply grounded. Device does not power up.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Internal pulldown brings EN/UVLO to low disabling the device.	B
OV	2	TPS12110-Q1 only. OV functionality gets disabled as OV gets internally pulled down to 0 V.	B
INP_G	2	TPS12111-Q1 only. Internal pulldown brings INP_G to low, pulling G output low.	B
INP	3	Internal pulldown brings INP to low, pulling PD output low.	B
$\overline{\text{FLT\_T}}$	4	Overtemperature fault diagnostic cannot be reported.	B
$\overline{\text{FLT\_I}}$	5	Overcurrent fault diagnostic cannot be reported.	B
GND	6	Device does not power up and is disabled.	B
IMON	7	IMON voltage can get clamped to internal supply of 6.5 V.	B
IWRN	8	IWRN voltage can get clamped to internal supply of 4.5 V.	B
TMR	9	Overcurrent response time and auto-retry duration gets reduced to device minimum setting.	C
DIODE	10	Overtemperature protection gets disabled.	B
N.C	11	No effect	D
G	11	G output does not get controlled.	B
BST	12	External FET can get turned ON and OFF repetitively due to no capacitor connection at BST pin.	B
SRC	13	The external FET does not turned OFF as the FET source got disconnected from the internal pulldown driver.	B
PD	14	The external FET does not turn OFF as the FET GATE disconnects from the internal pulldown driver.	B
PU	15	The external FET does not turn OFF as the FET GATE disconnects from the internal pulldown driver.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CS-	17	CS– gets internally clamped to CS+ minus 2 diode drops. If IWRN feature is used, then the external FET can not turn ON due to false overcurrent detection.	B
CS+	18	IMON and overcurrent protection features get disabled.	B
ISCP	19	Short-circuit protection feature gets disabled.	B
VS	20	Device does not get powered up and is disabled.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	2 (OV)	TPS12110-Q1 only. When EN/UVLO is driven high then based on the EN/UVLO level the device can detect the OV event and turn off the external FET.	B
EN/UVLO	1	2 (INP_G)	TPS12111-Q1 only. When EN/UVLO is driven high then based on the EN/UVLO level INP_G can get detected high and G can go high turning ON the external pre-charge FET.	B
OV	2	3 (INP)	TPS12110-Q1 only. When INP is driven high then based on INP level the device can detect the OV event and turn off the external FET.	B
INP_G	2	3 (INP)	TPS12111-Q1 only. Both PU/PD and G is controlled together.	B
INP	3	4 ($\overline{\text{FLT\_T}}$)	When an overtemperature fault occurs then INP gets pulled low and it stays latched off in this state.	B
$\overline{\text{FLT\_T}}$	4	5 ($\overline{\text{FLT\_I}}$)	$\overline{\text{FLT\_T}}$ and $\overline{\text{FLT\_I}}$ gets ORd together.	B
$\overline{\text{FLT\_I}}$	5	6 (GND)	Overcurrent fault does not get indicated.	B
GND	6	7 (IMON)	IMON output does not get reported.	B
IMON	7	8 (IWRN)	IMON output range and IWRN set point gets changed based on the total bias currents flowing through the IMON and IWRN resistors.	C
IWRN	8	9 (TMR)	TMR and IWRN thresholds get affected. External FET shuts off at a different threshold than set by IWRN. During an overcurrent fault, TMR feature become inactive and the device is in Latch-off mode.	C
TMR	9	10 (DIODE)	Auto-retry feature is disabled. Overtemperature feature can give false errors and cause the external FET to turn OFF.	B
N.C	11	12 (BST)	TPS12110-Q1 only. No effect.	D
G	11	12 (BST)	TPS12111-Q1 only. When INP_G is driven low, BST (Gate driver supply) gets loaded through the internal G pulldown switch. Gate driver UVLO hits resulting in turning off the external FETs.	B
BST	12	13 (SRC)	Gate drive supply gets shorted and external FETs do not turn ON.	B
SRC	13	14 (PD)	Shorting of the pulldown switch (between PD and SRC) of the internal gate driver. External FET remains OFF.	B
PD	14	15 (PU)	Turn ON and OFF speeds of the external FETs can get impacted.	C
CS-	17	18 (CS+)	Bypasses the external current sense resistor. IMON, OCP features get disabled.	B
CS+	18	19 (ISCP)	Short-circuit threshold gets reduced.	C
ISCP	19	20 (VS)	Short-circuit protection gets set to minimum setting.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
OV	2	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
INP_G	2	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
INP	3	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
$\overline{\text{FLT\_T}}$	4	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
$\overline{\text{FLT\_I}}$	5	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
GND	6	Supply power is bypassed and device does not turn on.	B
IMON	7	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
IWRN	8	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
TMR	9	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
DIODE	10	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
N.C	11	TPS12110-Q1 only. No effect.	D
G	11	TPS12111-Q1 only. If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
BST	12	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
SRC	13	Output stuck on to supply	B
PD	14	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
PU	15	If pin voltage exceeds the pin data sheet range, it can cause device damage due to voltage breakdown on ESD circuit.	A
CS-	17	In the application, the external sense resistor gets bypassed and IMON, over current and short circuit protection will not work.	A
CS+	18	IMON and IWRN outputs get saturated. External FET can get turned OFF.	B
ISCP	19	Short-circuit protection gets set to minimum setting.	C
VS	20	No effect	D

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