Functional Safety Information

SN6507-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for SN6507-Q1 (DGQ-10 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

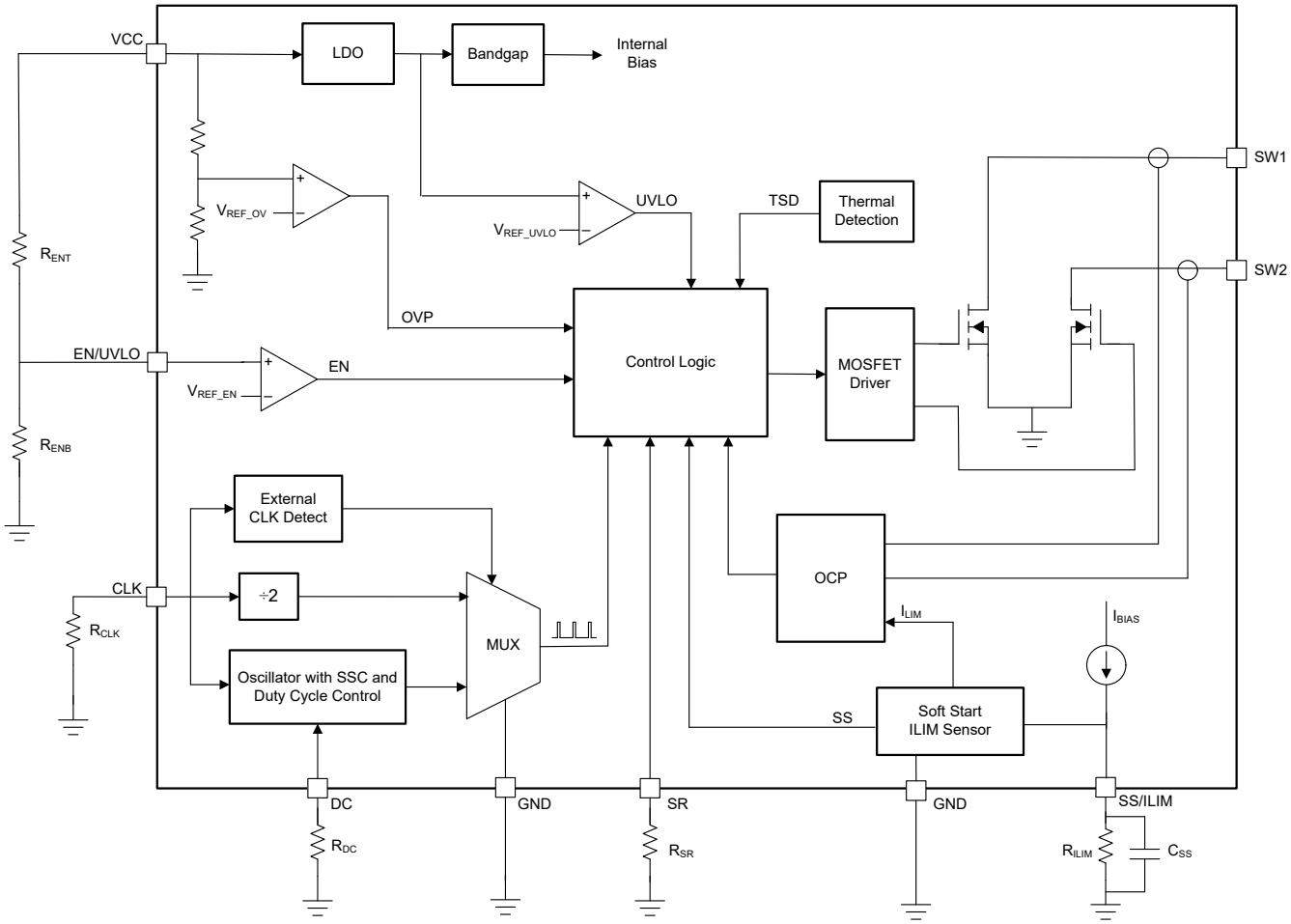

Figure 1-1. Functional Block Diagram

SN6507-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 (6) Package

This section provides Functional Safety Failure In Time (FIT) rates for DGQ-10 package of SN6507-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	9
Die FIT Rate	5
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 394 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25	55

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN6507-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW1 and/or SW2 FET stuck off	48%
SW1 and/or SW2 FET stuck ON	38%
SW1 and/or SW2 output not in timing or voltage specification	12%
SW1 and/or SW2 output undetermined	2%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN6507-Q1 (DGQ-10 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (seeTable 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External push-pull transformer connected with a winding between SW1 and V_{CC}, another winding connected between SW2 and V_{CC}.

4.1 DGQ-10 Package

Figure 4-1 shows the SN6507-Q1 pin diagram for the DGQ-10 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the SN6507-Q1 data sheet.

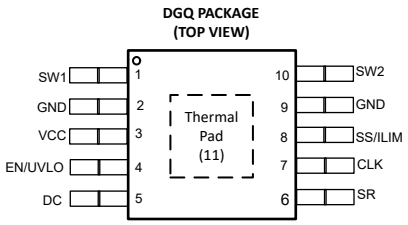

Figure 4-1. Pin Diagram (DGQ-10) package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW1	1	SW1 pin stuck low creates short circuit path between Vcc and ground through transformer winding, causing high current to flow and possible damage to transformer. Output voltage out of designed spec.	B
GND	2	Device continues to function as expected. Normal operation.	D
VCC	3	No power to the device. No isolated output voltage.	B
EN/UVLO	4	Enable stuck low, so the device remains in shutdown mode.	B
DC	5	No Clock output and No Push pull converter operation.	B
SR	6	No Push pull converter operation.	B
CLK	7	With CLK stuck low, external clock synchronization functionality is disabled. May have system level concerns if transformer not designed for 1MHz.	B
SS/LIM	8	The device will not transfer from soft-start to normal operation mode. No soft-start operation and No Push pull converter operation.	B
GND	9	Device continues to function as expected. Normal operation.	D
SW2	10	SW2 pin stuck low creates short circuit path between Vcc and ground through transformer winding, causing high current to flow and possible damage to transformer. Output voltage out of designed spec.	B
PowerPAD	11	Device continues to function as expected. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW1	1	With SW1 open, one primary transformer winding does not transfer energy. Isolated output supply out of intended set-point.	B
GND	2	Current returns through pin 9.	C
VCC	3	No power to device, so no switching action of SW1/SW2. Isolated output voltage does not build up.	B
EN/UVLO	4	Enable voltage is undefined, so the device remains in shutdown mode.	B
DC	5	Duty-cycle is configured to default.	C
SR	6	Slew-rate is configured to default.	C
CLK	7	With CLK pin open, swicthing functionality is stopped.	B
SS/LIM	8	No current limit or soft-start times set. Performance degradation.	C
GND	9	Current returns through pin 2.	C
SW2	10	With SW2 open, one primary transformer winding does not store energy. Isolated output supply out of intended set-point.	B
PowerPAD	11	Current returns through pin 2 and 9.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SW1	1	GND	SW1 stuck low. SW1 FET stays off, no current flows from supply to ground. Isolated output supply out of intended set-point.	B
GND	2	VCC	High current flows from supply to ground. No power to device.	B
VCC	3	EN/UVLO	Control to disable the device through EN/UVLO is lost.	B
EN/UVLO	4	DC	If EN/UVLO voltage exceeds DC pin Absolute Maximum Voltage Rating, device damage is plausible.	A
DC	5	EN/UVLO	Same as above	A
SR	6	CLK	The desired switching frequency or slew-rate performance may not be achieved. Slew-rate control circuit may not function.	B
CLK	7	SS/LIM	The desired switching frequency or current-limit/soft-start performance may not be achieved. Current limit/soft-start circuit may not function.	B
SS/LIM	8	GND	The device will not transfer from soft-start to normal operation mode. No soft-start operation and No Push pull converter operation.	B
GND	9	SW2	SW2 stuck low. SW2 FET stays off, no current flows from supply to ground. Isolated output supply out of intended set-point.	B
SW2	10	GND	SW2 stuck low. SW2 FET stays off, no current flows from supply to ground. Isolated output supply out of intended set-point.	B
PowerPAD	11	SW2	Same as above	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW1	1	SW1 stuck high. Makes potential difference between one transformer winding zero. When SW1 FET switches on, high current flows from supply to ground. Isolated output supply out of intended set-point.	A
GND	2	No power to device, so no switching action of SW1/SW2. Isolated output voltage does not build up.	B
VCC	3	No effect. Normal operation.	D
EN/UVLO	4	With EN stuck high, functionality to disable the device lost.	B
DC	5	If supply voltage exceeds DC pin Absolute Maximum Voltage Rating, device damage is plausible.	A
SR	6	If supply voltage exceeds SR pin Absolute Maximum Voltage Rating, device damage is plausible.	A
CLK	7	If supply voltage exceeds CLK pin Absolute Maximum Voltage Rating, device damage is plausible.	A
SS/LIM	8	If supply voltage exceeds SS pin Absolute Maximum Voltage Rating, device damage is plausible.	A
GND	9	No power to device, so no switching action of SW1/SW2. Isolated output voltage does not build up.	B
SW2	10	SW2 stuck high. Makes potential difference between one transformer winding zero. When SW2 FET switches on, high current flows from supply to ground. Isolated output supply out of intended set-point.	A
PowerPAD	11	No power to device, so no switching action of SW1/SW2. Isolated output voltage does not build up.	B

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