Functional Safety Information

LMR664x0 and LMR664x0-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LMR664x0 and LMR664x0-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 and Figure 1-2 show the functional block diagram of LMR664x0 and LMR664x0-Q1 for reference.

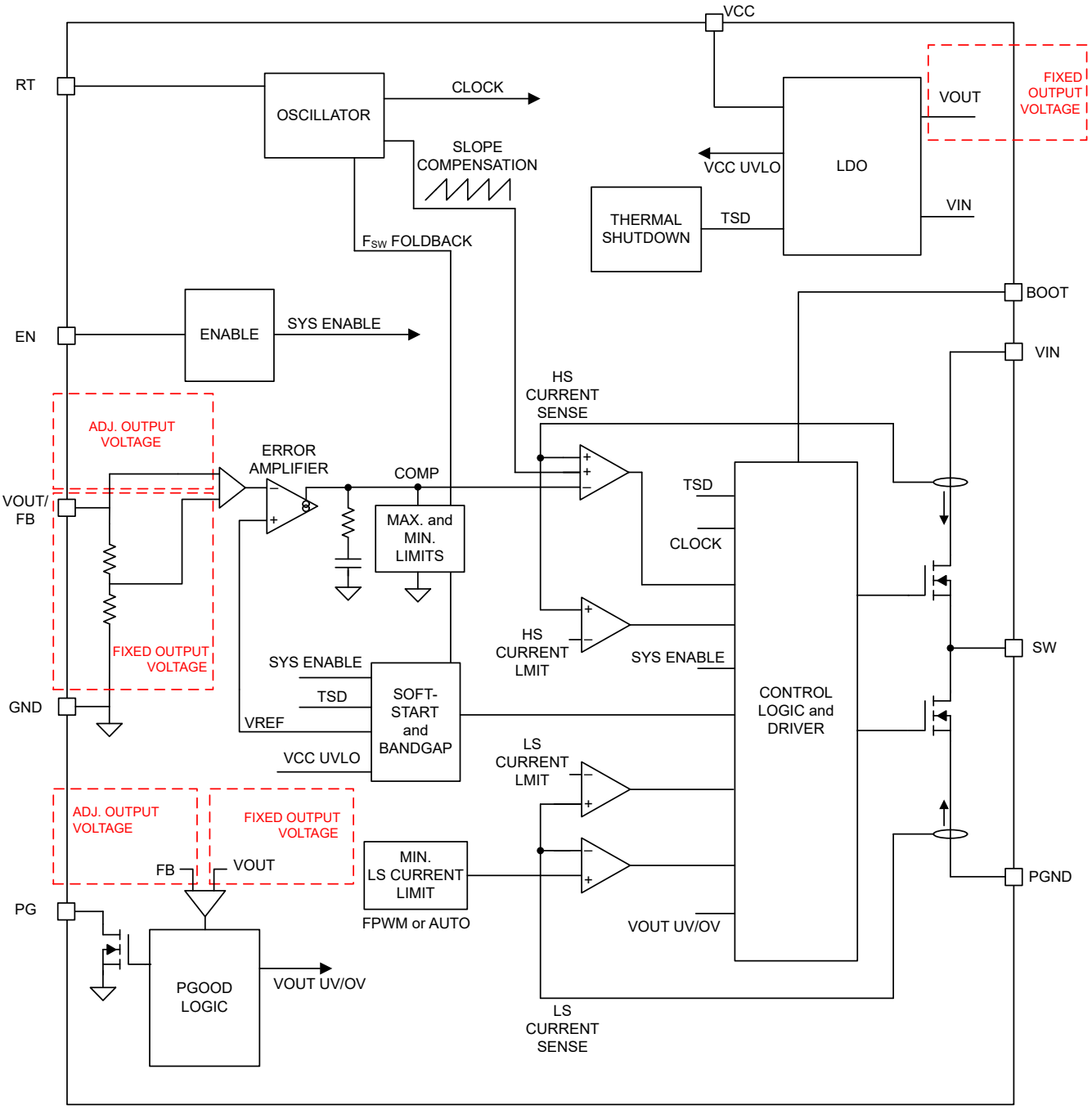

Figure 1-1. LMR664x0 Functional Block Diagram

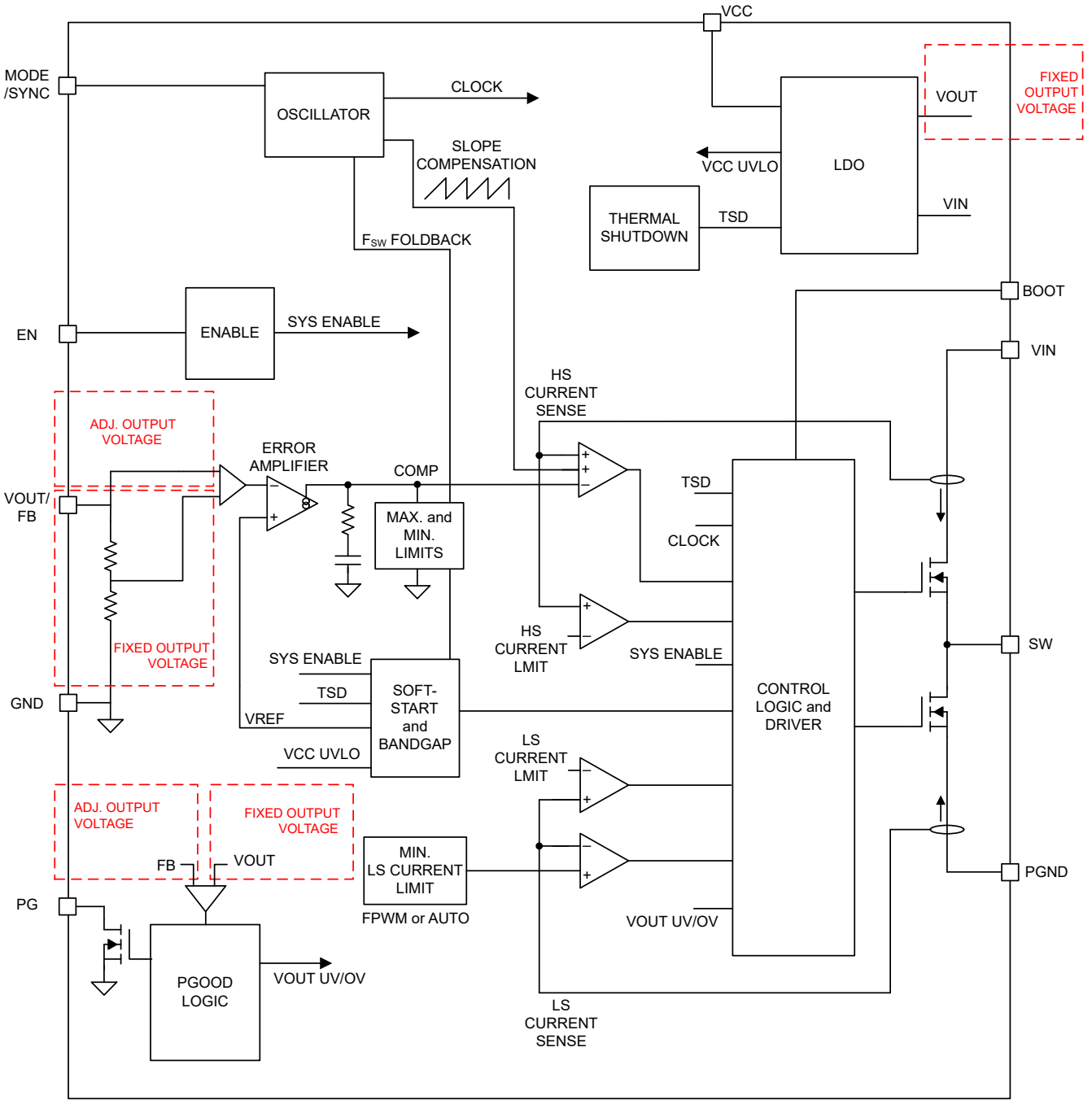

Figure 1-2. LMR664x0-Q1 Functional Block Diagram

LMR664x0 and LMR664x0-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LMR664x0 and LMR664x0-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	9
Die FIT Rate	4
Package FIT Rate	5

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 230 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs Analog & Mixed =< 50-V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR664x0 and LMR664x0-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60%
Output not in specification - voltage or timing	25%
Gate driver stuck on	5%
Power Good - false trip or failure to trip	5%
Short circuit between any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR664x0 and LMR664x0-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LMR664x0 and LMR664x0-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LMR664x0 and LMR664x0-Q1 data sheet.

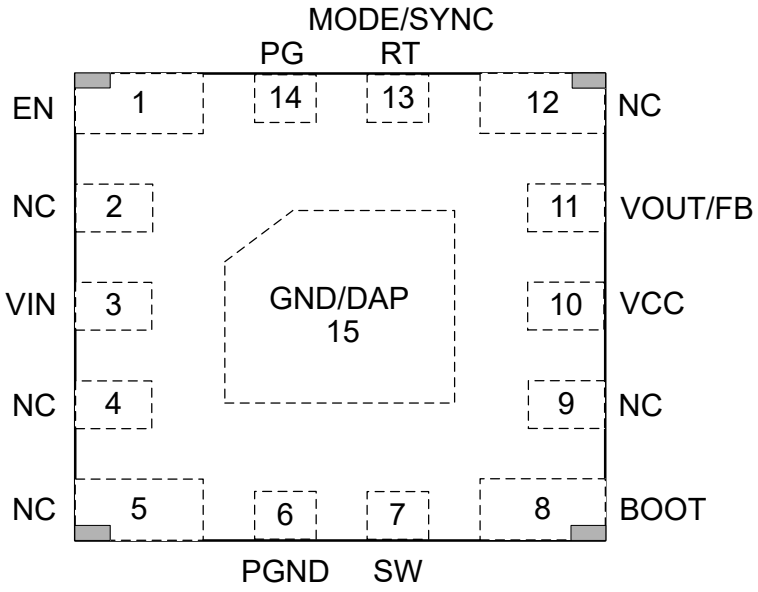

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LMR664x0 and LMR664x0-Q1 data sheets are used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	VOUT = 0 V, the part is disabled.	D
NC	2	VOUT is normal.	D
VIN	3	VOUT = 0 V.	B
NC	4	VOUT is normal.	D
NC	5	VOUT is normal.	D
PGND	6	VOUT is normal.	D
SW	7	Damage to HSFET.	A
BOOT	8	VOUT = 0 V, high side MOSFET won't turn on.	B
NC	9	V_{OUT} is normal.	D
VCC	10	VOUT = 0 V.	B
VOUT/FB	11	VOUT = 0 V.	B
NC	12	VOUT is normal.	D
RT or MODE/ SYNC	13	Switching frequency is 2.2 MHz.	D
PGOOD	14	When this pin is not in use it can be left grounded. PGOOD signal is not a valid signal, VOUT is normal.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	Pin cannot be left floating.	B
NC	2	VOUT is normal.	D
VIN	3	VOUT = 0 V.	B
NC	4	VOUT is normal.	D
NC	5	VOUT is normal.	D
PGND	6	VOUT can be abnormal because the reference voltage is not fixed.	B
SW	7	VOUT = 0 V.	B
BOOT	8	VOUT = 0 V, high side MOSFET does not turn on.	B
NC	9	VOUT is normal.	D
VCC	10	VCC output is unstable, can increase above 5.5 V.	A
VOUT/FB	11	VOUT = 0 V. Do not float this pin.	B
NC	12	VOUT is normal.	D
RT or MODE/ SYNC	13	If it is an RT part, then the frequency is not defined. If it is a MODE/SYNC part, then the part can go back and forth between FPWM and PFM. Part is up, part functional.	D
PGOOD	14	When not in use, PGOOD can be left open. PGOOD is not a valid signal, VOUT is normal.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	NC	VOUT is normal.	D
NC	2	VIN	VOUT is normal.	D
VIN	3	NC	VOUT is normal.	D
NC	4	NC	VOUT is normal.	D
NC	5	PGND	VOUT is normal.	D
PGND	6	SW	Damage to HSFET.	A
SW	7	BOOT	VOUT = 0 V, high side MOSFET does not turn on, CBOOT capacitor is shorted.	B
BOOT	8	NC	VOUT is normal.	D
NC	9	VCC	VOUT is normal.	D
VCC	10	VOUT/FB	The part can be functional, no damage occurs.	B
VOUT/FB	11	NC	VOUT is normal.	D
NC	12	RT of MODE/ SYNC	VOUT is normal.	D
RT or MODE/ SYNC	13	PGOOD	The absolute maximum voltage rating of this pin is 20 V. This pin can be damaged if PGOOD goes to 20 V.	A
PGOOD	14	EN/UVLO	If EN/UVLO > 20 V, this damages devices connected to the PGOOD pin.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/UVLO	1	VOUT is normal.	D
NC	2	VOUT is normal.	D
VIN	3	VOUT is normal.	D
NC	4	VOUT is normal.	D
NC	5	VOUT is normal.	D
PGND	6	VOUT = 0 V.	A
SW	7	Damage to LSFET.	A
BOOT	8	Damage occurs, BOOT ESD clamp is damaged.	A
NC	9	VOUT is normal.	D
VCC	10	If VIN > 5.5 V, damage occurs.	A
VOUT/FB	11	If VIN > 20 V, damage occurs.	A
NC	12	VOUT is normal.	D
RT or MODE/ SYNC	13	If VIN > 5.5 V, damage occurs. If VIN < 5.5 V, the switching frequency is 1 MHz.	A
PGOOD	14	IF VIN > 20 V, damage occurs.	A

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