Functional Safety Information

TMAG511x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview......2
2 Functional Safety Failure In Time (FIT) Rates......3
2.1 TMAG5110-Q1......3
2.2 TMAG5111-Q1......4
3 Failure Mode Distribution (FMD)......5
4 Pin Failure Mode Analysis (Pin FMA)......6
4.1 TMAG5110-Q1......6
4.2 TMAG5111-Q1......9
5 Revision History......10

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1 Overview

This document contains information for the TMAG511x-Q1 (DBV package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

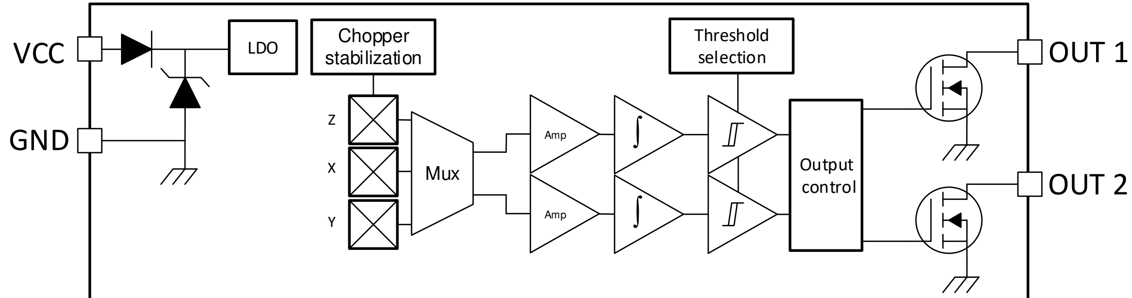

Figure 1-1. Functional Block Diagram

The TMAG511x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 TMAG5110-Q1

This section provides functional safety failure in time (FIT) rates for the TMAG5110-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	7
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 323mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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2.2 TMAG5111-Q1

This section provides functional safety failure in time (FIT) rates for the TMAG5111-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	7
Package FIT rate	2

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 323mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimations for the TMAG5110-Q1 in Table 3-1 and TMAG5111-Q1 in Table 3-2 come from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. TMAG5110-Q1 Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck in HIGH state	5
Output stuck in LOW state	25
Output stuck Hi-Z	25
Magnetic threshold error (BOP/BRP out of specification)	45

Table 3-2. TMAG5111-Q1 Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck in HIGH state	5
Output stuck in LOW state	25
Output stuck Hi-Z	25
Direction output toggle at incorrect moment	5
Magnetic threshold error (BOP/BRP out of specification)	40

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMAG511x-Q1 (DBV package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to VCC (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VCC and temperature are within the recommended operating conditions of the data sheet.
- Pullup resistors on OUT1 and OUT2 to limit ISINK are within the recommended range, <10mA.

4.1 TMAG5110-Q1

Figure 4-1 shows the TMAG5110-Q1 pin diagram for the DBV package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMAG5110-Q1 data sheet.

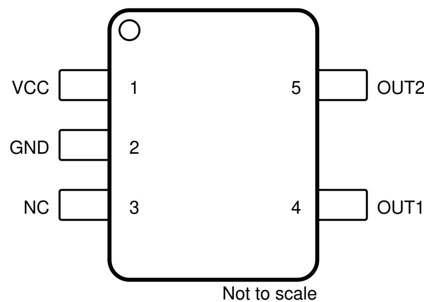

Figure 4-1. Pin Diagram DBV Package

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC	1	A lot of current can be sourced external to the device, with the current only limited by the source that supplies VCC and the total resistance between the supply and ground. Depending on the layout, a short can conduct enough heat to damage the part.	B or A
GND	2	Normal, recommended operation.	D
NC	3	Normal, recommended operation.	D
OUT1	4	OUT1 is always low, current is limited and heat dissipation is limited by the external pull-up resistor.	B
OUT2	5	OUT2 is always low, current is limited and heat dissipation is limited by the external pull-up resistor.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC	1	Device is unresponsive but not damaged	B
GND	2	Device is not functional and not damaged.	B
NC	3	Normal operation.	D
OUT1	4	Device output is disconnected from the system. Device is not damaged, functionality within the system is lost until open fixed.	B
OUT2	5	Device output is disconnected from the system. Device is not damaged, functionality within the system is lost until open fixed.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VCC	1	GND	A lot of current can be sourced external to the device, with the current only limited by the source that supplies VCC and the total resistance between the supply and ground. Depending on the layout, a short can conduct enough heat to damage the part.	B or A
GND	2	NC	Normal, recommended operation.	D
NC	3	OUT1	Functional and not damaged, however, not recommended.	D
OUT1	4	OUT2	Erroneous output. OUT1 and OUT2 are dominated by whichever is in the low state. Functionality is lost and increased consumption of current is possible.	B
OUT2	5	VCC	Device OUT2 is stuck high, the worst-case current is only limited by output drain $R_{DS(on)}$. If on sufficiently long, the output can be damaged.	B or A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC	1	Normal Operation	D
GND	2	A lot of current can be sourced external to the device, with the current only limited by the source that supplies VCC and the total resistance between the supply and ground. Depending on the layout, a short can conduct enough heat to damage the part.	B or A
NC	3	Not recommended, however, the part is expected to maintain functionality and not be damaged.	D
OUT1	4	Device OUT1 is stuck high, the worst-case current is only limited by output drain $R_{DS(on)}$. If on sufficiently long, the output can be damaged.	B or A
OUT2	5	Device OUT2 is stuck high, the worst-case current is only limited by output drain $R_{DS(on)}$. If on sufficiently long, the output can be damaged.	B or A

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4.2 TMAG5111-Q1

Figure 4-2 shows the TMAG5111-Q1 pin diagram for the DBV package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TMAG5111-Q1 data sheet.

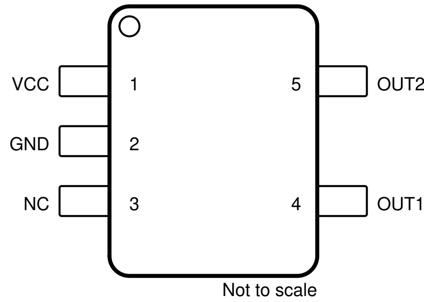

Figure 4-2. Pin Diagram (DBV Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC	1	A lot of current can be sourced external to the device, with the current only limited by the source that supplies VCC and the total resistance between the supply and ground. Depending on the layout, a short can conduct enough heat to damage the part.	B or A
GND	2	Normal, recommended operation.	D
NC	3	Normal, recommended operation.	D
OUT1	4	OUT1 is always low, current is limited and heat dissipation is limited by the external pull-up resistor.	B
OUT2	5	OUT2 is always low, current is limited and heat dissipation is limited by the external pull-up resistor.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC	1	Device is unresponsive but not damaged.	B
GND	2	Device is not functional.	B
NC	3	Normal operation.	D
OUT1	4	Device output is disconnected from the system. Device is not damaged, functionality within the system is lost until open fixed.	B
OUT2	5	Device output is disconnected from the system. Device is not damaged, functionality within the system is lost until open fixed.	B

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Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VCC	1	GND	A lot of current can be sourced external to the device, with the current only limited by the source that supplies VCC and the total resistance between the supply and ground. Depending on the layout, a short can conduct enough heat to damage the part.	B or A
GND	2	NC	Normal, recommended operation.	D
NC	3	OUT1	Functional, however, not recommended	D
OUT1	4	OUT2	Erroneous output. OUT1 and OUT2 are dominated by whichever is in the low state. Functionality is lost and increased consumption of current is possible.	B
OUT2	5	VCC	Device OUT2 is stuck high, the worst-case current is only limited by output drain $R_{DS(on)}$. If on sufficiently long, the output can be damaged.	B or A

Table 4-9. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC	1	Normal Operation.	D
GND	2	A lot of current can be sourced external to the device, with the current only limited by the source that supplies VCC and the total resistance between the supply and ground. Depending on the layout, a short can conduct enough heat to damage the part.	B or A
NC	3	Not recommended, however, the part is expected to maintain functionality and not be damaged.	D
OUT1	4	Device OUT1 is stuck high, the worst-case current is only limited by output drain $R_{DS(on)}$. If on sufficiently long, the output can be damaged.	B or A
OUT2	5	Device OUT2 is stuck high, the worst-case current is only limited by output drain $R_{DS(on)}$. If on sufficiently long, the output can be damaged.	B or A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

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