Functional Safety Information

PGA308 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the PGA308 (VSSOP (DGS) and VSON (DRK) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

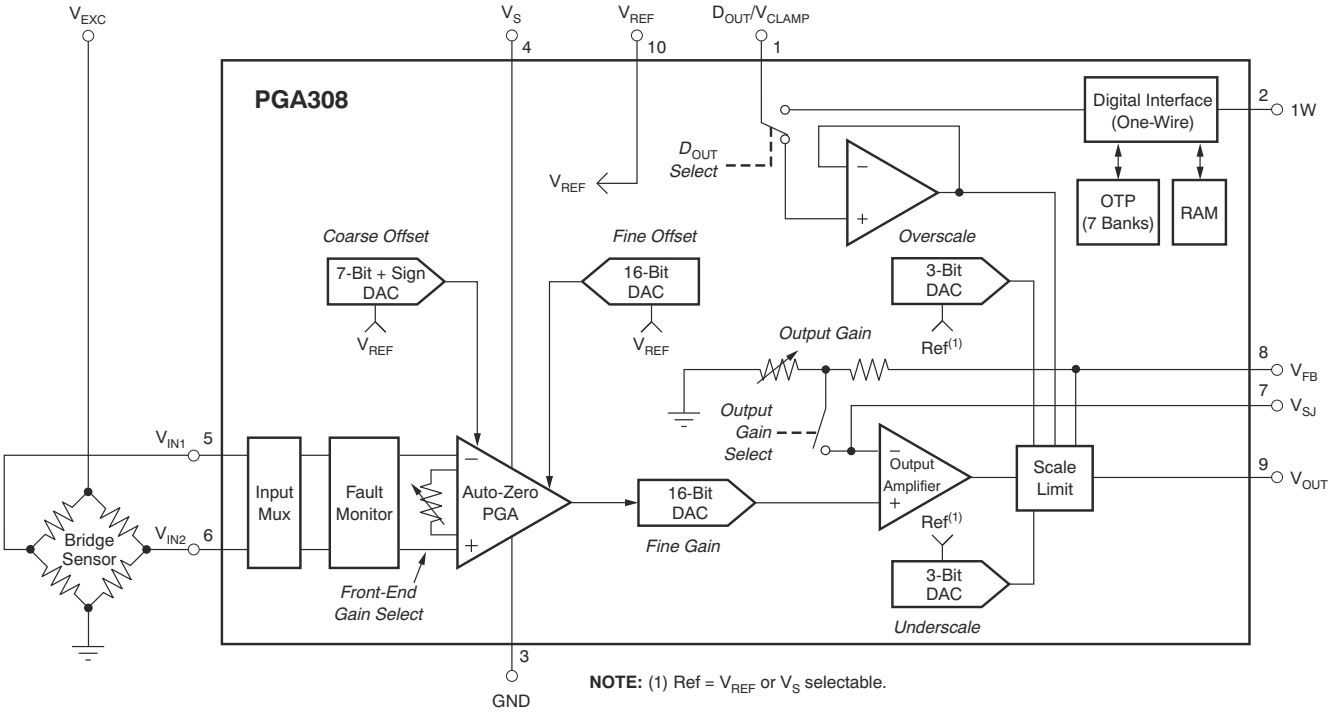

Figure 1-1. Functional Block Diagram

The PGA308 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSSOP (DGS) Package

This section provides functional safety failure in time (FIT) rates for the VSSOP (DGS) package of the PGA308 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 7.2mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSON (DRK) Package

This section provides functional safety failure in time (FIT) rates for the VSON (DRK) package of the PGA308 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	2
Package FIT rate	5

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 7.2mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the PGA308 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20
Output saturated high	25
Output saturated low	25
Output functional, out of specification voltage or timing	30

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the PGA308 (VSSOP (DGS) and VSON (DRK) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- *Short circuit to power* means short to V+
- *Short circuit to GND or ground* means short to V–
- V+ is equivalent to VCC and V– equivalent to VEE

4.1 VSSOP (DGS) Package

Figure 4-1 shows the PGA308 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the PGA308 data sheet.

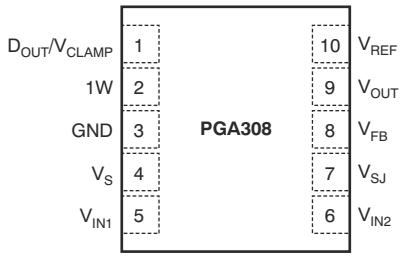

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
D_{OUT}/V_{CLAMP}	1	If configured as D_{OUT}, approaches absolute maximum rating for PIN 1 voltage, potentially degrading performance long-term. If configured as V_{CLAMP}, sets clamping voltage to VEE resulting in a loss of output signal.	B
1W	2	Loss of communication with device, PIN 1 remains in previous configuration.	D
V_S	4	Op-amp supplies are shorted together, leaving the VS pin at some voltage between the V_S and GND sources (depending on the source impedance).	A
V_{IN1}	5	V_{IN1} pin is shorted to ground, leaving the device outside the linear range resulting in unpredictable device output voltage.	B
V_{IN2}	6	V_{IN2} pin is shorted to ground, leaving the device outside the linear range resulting in unpredictable device output voltage.	B
V_{SJ}	7	There is potential for device damage depending on circuit configuration.	A
V_{FB}	8	Loss of device functionality, damage to the device is not likely.	B
V_{OUT}	9	Depending on the circuit configuration, the device can be forced into a short-circuit condition with the V_{OUT} voltage ultimately forced to the GND voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V_{REF}	10	Loss of device functionality, damage to the device is not likely.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
D_{OUT}/V_{CLAMP}	1	If configured as D_{OUT}, digital communication is lost with external sensors resulting in a loss of device functionality. If configured as $V_{CLAMP,}$ clamping voltage, at some voltage between VEE and VCC, potentially result in the device output not functioning as intended.	B
1W	2	Loss of communication with device, PIN 1 remains in previous configuration.	D
GND	3	Negative supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
V_S	4	Positive supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
V_{IN1}	5	Signal input voltage 1 is left floating. V_{IN1} voltage can end up at the positive or negative rail because of leakage on the ESD diodes, possibly resulting in a device output voltage between the negative and positive rails.	B
V_{IN2}	6	Signal input voltage 2 is left floating. V_{IN2} voltage can end up at the positive or negative rail because of leakage on the ESD diodes, possibly resulting in a device output voltage between the negative and positive rails.	B
V_{SJ}	7	Loss of external compensation, device can continue to function.	D
V_{FB}	8	Depending on circuit configuration, V_{OUT} can be forced to either VCC or VEE.	B
V_{OUT}	9	No negative feedback or ability for V_{OUT} to drive the application.	B
V_{REF}	10	Loss of functionality for course offset DAC, fine offset DAC, underscale DAC, overscale DAC, and fault monitor.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
D_{OUT} / V_{CLAMP}	1	2	If configured as D_{OUT}, results in a loss of device functionality. If configured as V_{CLAMP}, clamping voltage is set to 1W voltage, potentially resulting in device output not functioning as intended.	B
1W	2	3	Loss of communication with device, PIN 1 remains in previous configuration.	D
GND	3	4	Op-amp supplies are shorted together, leaving the GND pin at some voltage between the GND and V_S sources (depending on the source impedance).	A
V_S	4	5	V_{IN1} pin is shorted to supply, leaving the device outside the linear range resulting in unpredictable device output voltage.	B
V_{IN1}	5	6	Both inputs are tied together. Output voltage is set to some value-based device gain configuration and the course offset value is set by V_{REF} voltage.	B
V_{IN2}	6	7	Oscillation is possible due to additional capacitance on the V_{SJ} pin resulting in erratic behavior on the output.	B
V_{SJ}	7	8	Depending on circuit configuration, erroneous gain can result in a loss of intended functionality. Potential stability issues can arise by shorting the isolation resistor, typically found between V_{SJ} and V_{FB}.	B
V_{FB}	8	9	No loss of functionality and no potential damage to the device. If an external filter is used, the filter is bypassed.	D
V_{OUT}	9	10	Device output behaves unpredictably, resulting in a loss of functionality. No potential damage to the device.	B
V_{REF}	10	1	If PIN 1 is configured as D_{OUT}, the output voltage is unpredictable, resulting in a loss of functionality. If PIN 1 is configured as V_{CLAMP}, clamping voltage is set to V_{REF} voltage, potentially resulting in an erroneous output voltage, if the V_{REF} voltage is less than the intended output.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Class
D_{OUT}	1	If configured as D_{OUT}, approaches the absolute maximum rating for PIN 1 voltage, potentially degrading performance long term. If configured as V_{CLAMP}, sets clamping voltage to VCC, allowing the full output range.	C
1W	2	Loss of communication with device, PIN 1 remains in previous configuration.	D
GND	3	Op-amp supplies are shorted together, leaving the GND pin at some voltage between the GND and V_S sources (depending on the source impedance).	A
V_{IN1}	5	V_{IN1} pin is shorted to supply, leaving the device outside the linear range, resulting in an unpredictable device output voltage.	B
V_{IN2}	6	V_{IN2} pin is shorted to supply, leaving the device outside the linear range, resulting in an unpredictable device output voltage.	B
V_{SJ}	7	Device damage is possible depending on circuit configuration.	A
V_{FB}	8	Loss of device functionality, damage to the device is not likely.	B
V_{OUT}	9	Depending on the circuit configuration, the device can be forced into a short-circuit condition with the V_{OUT} voltage ultimately forced to the V_S voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V_{REF}	10	Loss of device functionality, damage to the device is not likely.	B

4.2 VSON (DRK) Package

Figure 4-2 shows the PGA308 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the PGA308 data sheet.

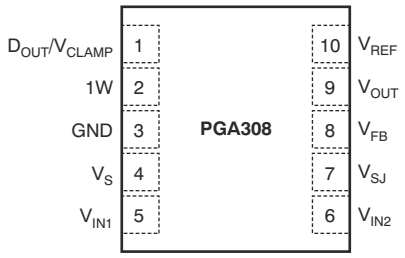

Figure 4-2. Pin Diagram

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
D_{OUT}/V_{CLAMP}	1	If configured as D_{OUT}, approaches the absolute maximum rating for PIN 1 voltage, potentially degrading performance long term. If configured as V_{CLAMP}, sets clamping voltage to VEE resulting in a loss of output signal.	B
1W	2	Loss of communication with device, PIN 1 remains in previous configuration.	D
V_S	4	Op-amp supplies are shorted together, leaving the VS pin at some voltage between the V_S and GND sources (depending on the source impedance).	A
V_{IN1}	5	V_{IN1} pin is shorted to ground, leaving the device outside the linear range, resulting in an unpredictable device output voltage.	B
V_{IN2}	6	V_{IN2} pin is shorted to ground, leaving the device outside the linear range, resulting in an unpredictable device output voltage.	B
V_{SJ}	7	There is potential for device damage depending on circuit configuration.	A
V_{FB}	8	Loss of device functionality, damage to the device is not likely.	B
V_{OUT}	9	Depending on the circuit configuration, the device can be forced into a short-circuit condition with the V_{OUT} voltage ultimately forced to the GND voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V_{REF}	10	Loss of device functionality, damage to the device is not likely.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
D_{OUT}/V_{CLAMP}	1	If configured as D_{OUT}, digital communication is lost with external sensors resulting in a loss of device functionality. If configured as V_{CLAMP}, clamping voltage, at some voltage between VEE and VCC, potentially results in the device output not functioning as intended.	B
1W	2	Loss of communication with device, PIN 1 remains in previous configuration.	D
GND	3	Negative supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
V_S	4	Positive supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
V_{IN1}	5	Signal input voltage 1 is left floating. V_{IN1} voltage can end up at the positive or negative rail because of leakage on the ESD diodes, potentially resulting in a device output voltage between the negative and positive rails.	B
V_{IN2}	6	Signal input voltage 2 is left floating. V_{IN2} voltage can end up at the positive or negative rail because of leakage on the ESD diodes, potentially resulting in a device output voltage between the negative and positive rails.	B
V_{SJ}	7	Loss of external compensation, device potentially continues to function.	D
V_{FB}	8	Depending on circuit configuration, V_{OUT} is forced to either VCC or VEE.	B
V_{OUT}	9	No negative feedback or ability for V_{OUT} to drive the application.	B
V_{REF}	10	Loss of functionality for course offset DAC, fine offset DAC, underscale DAC, overscale DAC, and fault monitor.	D

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
D_{OUT} / V_{CLAMP}	1	2	If configured as D_{OUT}, results in a loss of device functionality. If configured as V_{CLAMP}, clamping voltage is set to 1W voltage, potentially resulting in the device output not functioning as intended.	B
1W	2	3	Loss of communication with device, PIN 1 remains in previous configuration.	D
GND	3	4	Op-amp supplies are shorted together, leaving the GND pin at some voltage between the GND and V_S sources (depending on the source impedance).	A
V_S	4	5	V_{IN1} pin is shorted to supply, leaving the device outside the linear range, resulting in unpredictable device output voltage.	B
V_{IN1}	5	6	Both inputs are tied together. Output voltage is set to some value-based device gain configuration and the course offset value is set by V_{REF} voltage.	B
V_{IN2}	6	7	Oscillation is possible due to additional capacitance on the V_{SJ} pin, resulting in erratic behavior on the output.	B
V_{SJ}	7	8	Depending on circuit configuration, erroneous gain can result in a loss of intended functionality. Potential stability issues can arise by shorting the isolation resistor, typically found between V_{SJ} and V_{FB}.	B
V_{FB}	8	9	No loss of functionality and no potential damage to the device. If an external filter is used, the filter is bypassed.	D
V_{OUT}	9	10	Device output behaves unpredictably, resulting in a loss of functionality. No potential damage to the device.	B
V_{REF}	10	1	If PIN 1 is configured as D_{OUT}, output voltage is unpredictable, resulting in a loss of functionality, If PIN 1 is configured as V_{CLAMP}, clamping voltage is set to V_{REF} voltage, potentially resulting in an erroneous output voltage if the V_{REF} voltage is less than the intended output.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Class
D_{OUT}	1	If configured as D_{OUT}, approaches the absolute maximum rating for PIN 1 voltage, potentially degrading performance long term. If configured as V_{CLAMP}, sets clamping voltage to VCC allowing the full output range.	C
1W	2	Loss of communication with device, PIN 1 remains in previous configuration.	D
GND	3	Op-amp supplies are shorted together, leaving the GND pin at some voltage between the GND and V_S sources (depending on the source impedance).	A
VIN1	5	V_{IN1} pin is shorted to supply, leaving the device outside the linear range, resulting in an unpredictable device output voltage.	B
V_{IN2}	6	V_{IN2} pin is shorted to supply, leaving the device outside the linear range, resulting in an unpredictable device output voltage.	B
V_{SJ}	7	Device damage is possible, depending on circuit configuration.	A
V_{FB}	8	Loss of device functionality, damage to the device is not likely.	B
V_{OUT}	9	Depending on the circuit configuration, the device can be forced into a short-circuit condition with the V_{OUT} voltage ultimately forced to the V_S voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V_{REF}	10	Loss of device functionality, damage to the device is not likely.	B

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265