Functional Safety Information

TPS3703 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS3703 (DSE package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

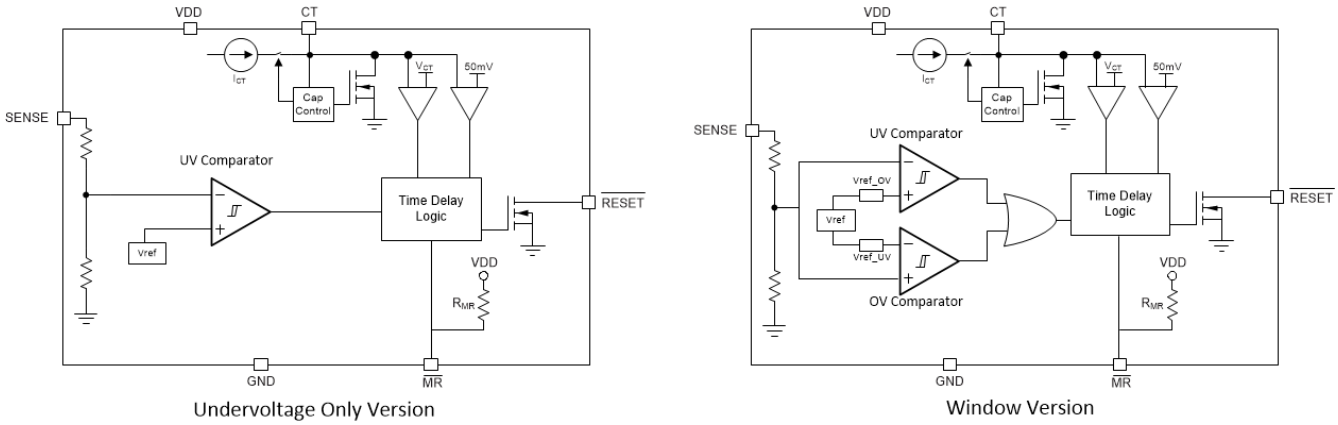

Figure 1-1. Functional Block Diagram

The TPS3703 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS3703 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 5mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3703 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
nRESET fails to trip	15
nRESET false trip	15
nRESET trip outside specification (voltage or time)	65
nRESET delay outside specification	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS3703. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)
- Pin short-circuited to /RESET is also included (see Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS3703 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS3703 data sheet.

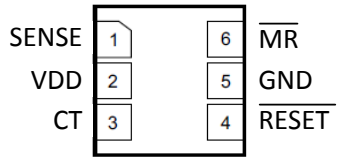

Figure 4-1. Pin DiagramDSE Package 6-Pin WSON

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VDD = 3.3V, V_SENSE = 1.2V, /RESET pulled-up to VDD unless stated otherwise

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SENSE	1	No damage to device, can affect application functionality. Shorts voltage supply to ground, increases current.	C
VDD	2	No damage to device, can affect application functionality. Shorts voltage supply to ground, increases current.	C
CT	3	Normal operation, device in latch mode. Usually has pull-down resistance to limit currEnt.	D
/RESET	4	No damage to device, can affect application functionality. Forces /reset to be asserted.	C
GND	5	Normal operation.	D
/MR	6	Normal operation in some cases, but forces /reset to be asserted.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SENSE	1	No damage to device, can affect application functionality. /Reset tends to be low.	C
VDD	2	No damage to device, but device is not powered. /Reset tends to be low.	C
CT	3	Normal operation.	D
/RESET	4	Open drain output requires pull-up voltage for functionality.	C
GND	5	No damage to device, but device is not powered. /Reset tends to be low.	C
/MR	6	Normal operation. Pin is internally pulled up to VDD.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SENSE	1	VDD	Normal operation in some applications. Functionality affected with separate supply for sense, but no damage.	C
VDD	2	CT	Normal operation. Usually has pull-up resistance to limit current.	D
CT	3	/RESET	No damage to device, but device is not powered. /Reset tends to be low.	C
/RESET	4	GND	No damage to device, can affect application functionality. Forces /reset to be asserted.	C
GND	5	/MR	Normal operation in some cases, but forces /reset to be asserted.	C
/MR	6	SENSE	Undefined operation, but functionality can be affected. When MR is asserted, SENSE shorts to GND.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SENSE	1	Normal operation in some applications. Functionality affected with separate supply for sense, but no damage.	C
VDD	2	Normal operation.	D
CT	3	Normal operation. Usually has pull-up resistance to limit current.	D
/RESET	4	Normal operation. Usually has pull-up resistance to limit current.	D
GND	5	No damage to device, can affect application functionality. Shorts voltage supply to ground, increases current.	C
/MR	6	Normal operation, but increased leakage current. Internally pulled-up to VDD to limit current.	D

Table 4-6. Pin FMA for Device Pins Short-Circuited to /RESET

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SENSE	1	No damage to device, can affect application functionality. Forces /reset to equal sense voltage.	C
VDD	2	Normal operation. Usually has pull-up resistance to limit current.	D
CT	3	No damage to device, can affect application functionality. /Reset tends to be low.	C
/RESET	4	Normal operation.	D
GND	5	No damage to device, can affect application functionality. Forces /reset to be asserted.	C
/MR	6	No damage to device, can affect application functionality. Forces /RESET to latch.	C

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265