

SN74LVC1G66-Q1

Functional Safety FIT Rate, FMD and Pin FMA



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1 Overview

This document contains information for SN74LVC1G66-Q1 (SOT-23 and SOT-SC70 packages) to aid in a functional safety system design. Information provided is:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

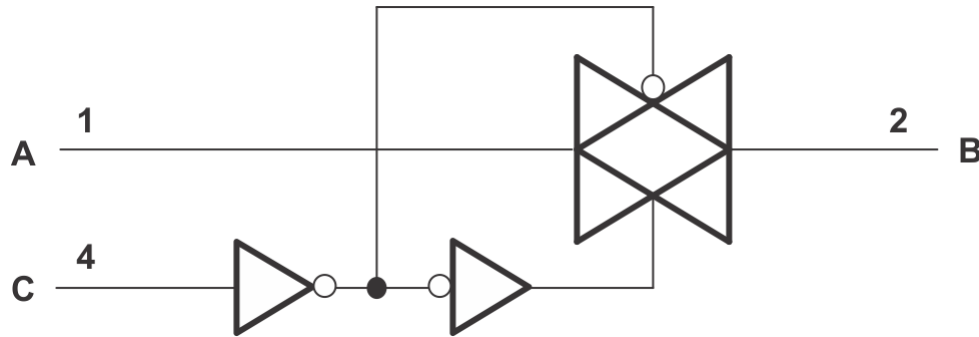


Figure 1-1. Functional Block Diagram

SN74LVC1G66-Q1 was developed using a quality-managed development process but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 package of the SN74LVC1G66-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	5
Die FIT rate	3
Package FIT rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from Table 11
- Power dissipation: 87.5mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
3	CMOS Analog switch, Bus Interface FCT, HC, LV, LVC, ALVC, VHC, and so forth	5 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOT-SC70 Package

This section provides functional safety failure in time (FIT) rates for the SOT-SC70 package of the SN74LVC1G66-Q1 based on two different industry-wide used reliability standards:

- [Table 2-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	6
Die FIT rate	4
Package FIT rate	2

The failure rate and mission profile information in [Table 2-3](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from Table 11
- Power dissipation: 87.5mW
- Climate type: world-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
3	CMOS Analog switch, Bus Interface FCT, HC, LV, LVC, ALVC, VHC, and so forth	5 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-4](#) comes from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74LVC1G66-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SWITCH no output (Hi-Z)	42.5
SWITCH channel stuck on	7.5
SWITCH channel stuck off	7.5
SWITCH functional out-of-specification voltage or timing	42.5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the SN74LVC1G66-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to VCC (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

[Figure 4-1](#) shows the pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the SN74LVC1G66-Q1 data sheet.

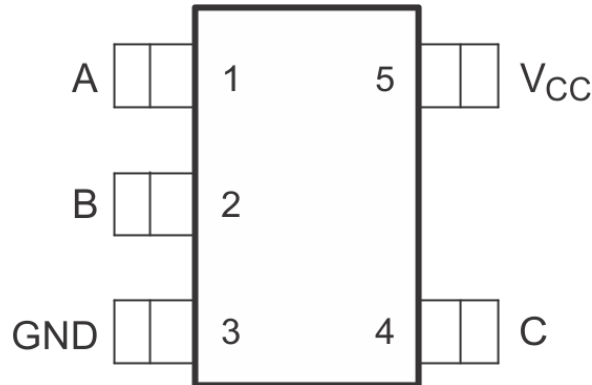


Figure 4-1. Pin Diagram (SOT-23 and SOT-SC70 Packages)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A	1	Corruption of analog signal on A. If there is no limiting resistor in the switch path, device damage is possible.	A
B	2	Corruption of analog signal on B. If there is no limiting resistor in the switch path, device damage is possible.	A
GND	3	No effect, normal operation.	D
C	4	C stuck low. Cannot control switch state.	B
VCC	5	Device is not powered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A	1	Corruption of analog signal on A.	B
B	2	Corruption of analog signal on B.	B
GND	3	Device is not powered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A
C	4	Loss of control of IN pin. Switch in undefined state.	B
VCC	5	Device is not powered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage is possible.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effects	Failure Effect Class
A	1	B	Corruption of analog signal on A.	B
B	2	GND	Corruption of analog signal on B.	B
GND	3	C	Not considered. This is a corner pin.	D
C	4	VCC	C stuck to VCC. Cannot control switch states	B
VCC	5	A	Not considered, Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A	1	Corruption of analog signal on A. If there is no limiting resistor in the switch path, device damage is possible.	A
B	2	Corruption of analog signal on B. If there is no limiting resistor in the switch path, device damage is possible.	A
GND	3	Device is not powered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met. Otherwise, device damage is possible.	A
C	4	C stuck to VCC. Cannot control switch states.	B
VCC	5	No effect, normal operation.	D

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