Application Report
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PGA460 full-bridge driver solutions for ultrasonic transducers

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ABSTRACT

This document offers various implementations to achieve a full-bridge driver to excite an ultrasonic transducer when using the PGA460. Because the PGA460 was only designed to excite transducers in the transformer-driven or half-bridge driver modes, external circuitry is required to enable a full-bridge driver. The recommended solution is based on combining the functionality of the PGA460 with the DRV8870 to enable the excitation voltage to swing between ±45 V. Low-cost discrete alternatives are also discussed.

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Trademarks

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1 Introduction

The PGA460 ultrasonic sensor signal conditioner integrates two complimentary low-side drivers to support excitation of a transducer through a center-tap transformer. For applications that require a weaker excitation voltage, or if power consumption is to be minimized, only one of the integrated low-side drivers can be leveraged for a single-ended transformer or half-bridge direct-driver mode.

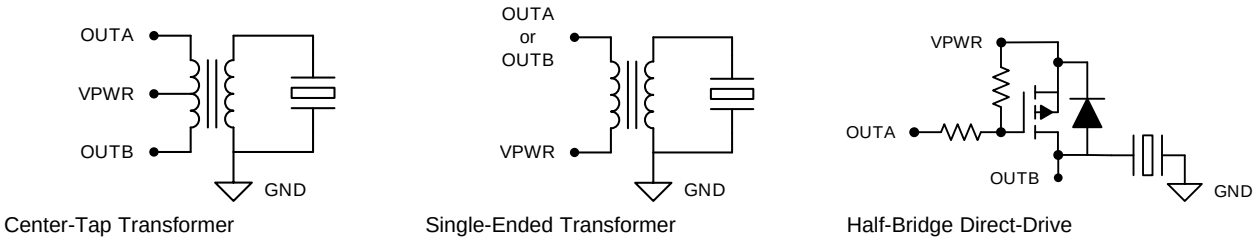

Figure 1. PGA460 Readily-Supported Drive Modes

Typically, a weaker excitation voltage is used by applications requiring one or more of the following:

- Does not require a long range of ultrasonic measurement or proximity detection
- The cost of the transformer or PCB real-estate requirements are too demanding
- The maximum rated excitation voltage transducer is limited to the battery-supply or other regulated voltage

Many open-top transducers do not require more than tens of volts to generate the maximum transmittable sound pressure level (SPL), so a transformer is not necessary, and a direct-driver mode is recommended. Closed-top transducers can also be excited in the direct-drive mode, but their effective range is limited due to the typical requirement of hundreds of volts to generate the maximum transmittable SPL. The full-bridge direct-driver mode may be preferred when attempting to maximize the peak-to-peak excitation voltage of an open-top transducer or to increase the effective range of a closed-top transducer.

2 Problem Statement

Although the PGA460 can support the half-bridge direct-drive mode with the use of an external single channel P-MOSFET, the full-bridge direct-drive implementation is not as reliable when using an external two channel P-channel MOSFET. In both implementations, the open-drain of the low-side also serves as the complementary high-side gate driver. This is an unconventional driver configuration; thus, yielding an increased risk in driving failure.

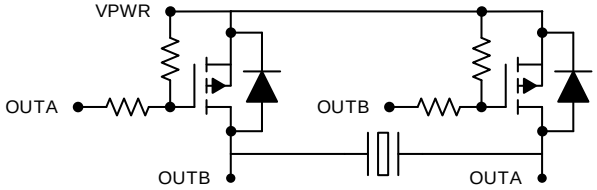

Figure 2. Original Full-Bridge Direct-Driver Circuit for PGA460 in Bi-Static Mode

Some transducers can be driven in this original full-bridge implementation, but others experience a latching phenomenon after a certain number of driver cycles or beyond a certain high-side voltage level. This latching prevents the transducer from being excited properly because the open-drain of one low-side driver constantly holds the shared transducer terminal high while its compliment is constantly held low. The following low-voltage based waveforms assume serial impedances of 1 kΩ and 0.1 kΩ to create the voltage divider at the gates of each P-MOSFET.

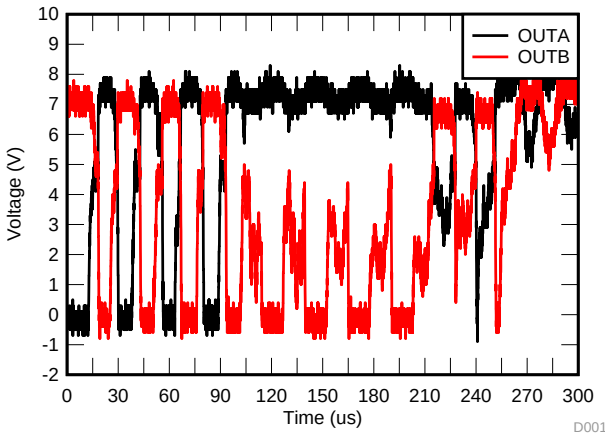

Figure 3. Full-Bridge Latching at 8 V for Murata™ MA40S4S

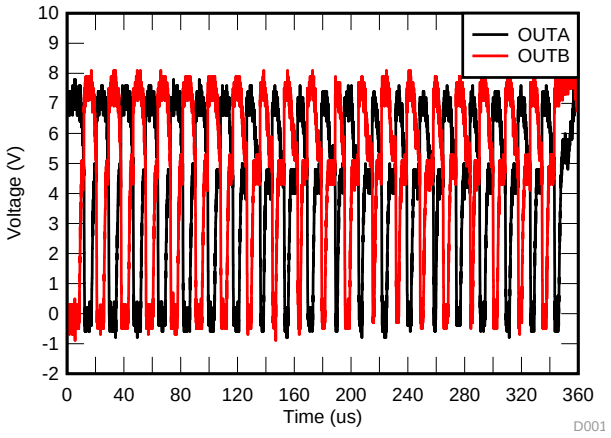

Figure 4. Full-Bridge Fading Success at 8 V for Murata™ MA58MF14-7N

(1)

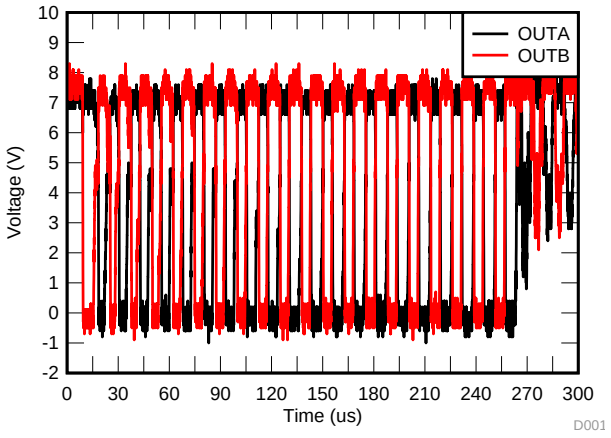

Figure 5. Full-Bridge Success at 8 V for Kobitone™ 255-400PT160-ROX

This conditional latching is explained by one of two reasons:

- The internal RLC branch of the transducer builds charge over time, such that the inductive element eventually holds too large of a charge, preventing the otherwise natural resonance of the transducer. Because the charge is held at the load (also the open-drain at the low-side), the opposing driver are not triggered. Depending on the RLC characteristics of a transducer, the pulse at which the latching occurs are different.
- The external high-side P-MOSFET is being driven either too strongly or weakly at the gates. Due to the unconventional implementation of an open-drain gate driver, this adds additional switching uncertainty. Ideally, the high-side gates would not be controlled by the complimentary and resonant sink paths of the load, but by a completely independent gate driver.

(1) Murata MA58MF14-7N can only be sold to automotive applications.

The primary driving architecture of the PGA460 is oriented around a center-tap transformer implementation, which is why complications of the full-bridge direct-driver have not been fully evaluated or accounted for. The deadtime control of the PGA460 is the only device variable which can help to mitigate latching. The solutions in the following sections are able to completely mitigate the possibility of full-bridge latching by allocating the low-side drivers externally to the PGA460. This means that the OUTA and OUTB pins of the PGA460 are repurposed to exclusively function as gate drivers.

3 PGA460 and DRV8870 Full-Bridge Solution

3.1 Description

For the simplest full-bridge driver solution, TI's DRV8870 motor driver is used to integrate all four MOSFETs of the full-bridge. The number of components (including the resistive passives) required for the bi-static variant of the DRV8870 implementation is identical to that of the original circuit which is prone to latching. The advantage of this implementation is that the DRV8870 is not prone to latching, the high-side can reference up to 45 V, and the specified frequency of the logic inputs controlling the H-bridge supports ultrasonic transducers with a center-frequency up to 200 kHz. An optional current regulator pin is also offered in the case where shoot-through current is of concern. Disadvantages of this implementation include the cost and 3-mA operating current of the DRV8870.

3.2 Block Diagram

Figure 6 and Figure 7 show the block diagrams of the DRV solutions.

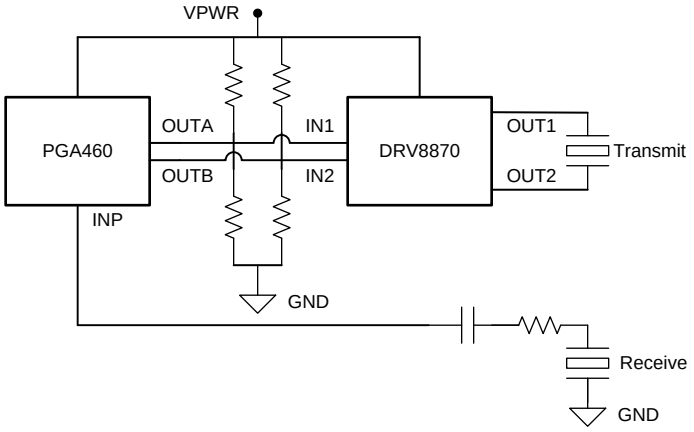

Figure 6. PGA460 and DRV8870 Bi-Static Block Diagram

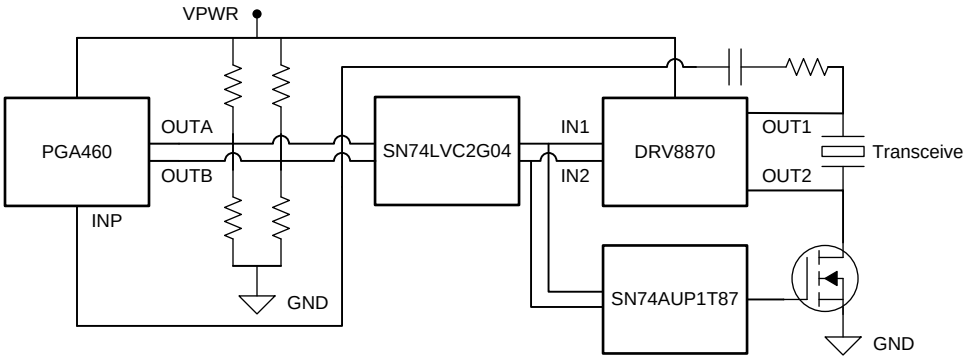

Figure 7. PGA460 and DRV8870 Mono-Static Block Diagram

Considering that the PGA460 is limited to a 30-V supply, the 45-V operating voltage of the DRV8870 is the primary benefit to using this integrated solution for maximizing transmittable SPL. Even if the original circuit were not prone to latching, the high-side reference is limited to the maximum supply voltage of 30 V or 60-V total peak-to-peak excitation voltage. The DRV8870 references its supply voltage up to 45 V to achieve a maximum of 90-V total peak-to-peak excitation voltage. Because the OUTA and OUTB pins of the PGA460 are only used as drivers in this implementation, the PGA460 is never exposed to the 45-V voltage. For weaker full-bridge excitation, the DR8870 supply voltage can also be minimized to 6.5 V to nearly match the 6-V recommended minimum supply voltage of the PGA460. If more than 30 V is to be applied to the DRV8870, ensure the PGA460 supply is separated or down-regulated to sub-30 V.

Although the integrated low-side drivers of the PGA460 are no longer connected directly to the transducer for excitation, OUTA and OUTB are repurposed to drive the logic inputs of the DRV8870. Because the logic inputs are limited to VREF as sourced by the IOREG of the PGA460, the logic input level must be limited to either 3.3 V or 5 V. By default IOREG creates a 3.3 V output unless the PGA460 TEST pin is pulled-high during start-up. For the mono-static configuration, 3.3 V is required to supply the exclusive-NOR gate of the SN74AUP1T87 from TI. To ensure the logic high input of the DRV8870 is limited to 3.3 V, a resistive voltage divider is implemented. The resistor divider values are dependent on the supply voltage of the PGA460, or the DRV8870, or both. Because the resistive voltage divider constantly draws current, select the resistor values to optimize both the continuous power dissipation and logic transition rate to trigger the logic input of the DRV8870 at a timely speed. The lower the resistor values of the divider, the more power continuously dissipated, but the more efficient the logic driver on and off timing becomes.

In the bi-static transducer configuration, the logic inputs are allowed to idle high to enter the brake (low-side slow decay) output mode of the DRV8870 because activity at the transmit-transducer is irrelevant for the receive-transducer. Brake mode operation is recommended for bi-static transducers to help minimize the decay energy of the transmit-transducer from coupling to the receive-transducer. However, in a mono-static transducer configuration, the transducer must be floating in the listen state. Therefore, a mono-static configuration, the DRV8870 must first toggle in the forward and reverse modes during burst, then immediately return to the coast (high-impedance) mode during listen. Due to the DRV8870 low-logic input requirement to enable the coast mode, TI's SN74LVC2G04 inverter is placed in between the resistive voltage divider output and the logic input pins of the DRV8870 for mono-static transducer mode.

Because the analog front end of the PGA460 is a single-channel input, rather than differential, the listen-transducer must be grounded at the negative terminal, while the positive terminal must remain floating to detect a return echo. In a bi-static configuration, the negative terminal of the listen-transducer can be permanently fixed to ground. However, in a mono-static configuration, the negative terminal of the transducer should only be forced to ground after the burst cycle is completed. In combination with the coast mode of the DRV8870, which sets both transducer terminals to high-impedance, the SN74AUP1T87 then drives an external N-MOSFET to force the negative terminal to ground when both OUTA and OUTB are either inactive high or low. This allows the positive terminal to remain in the coast mode of the DRV8870 to detect returning echoes.

A limitation of the DRV8870 based solution is that the DRV8870 enters sleep mode when inactive. When the IN1 and IN2 pins are both low for approximately 1 ms, the DRV8870 device enters a low-power sleep mode where the outputs remain High-Z, and the devices uses micro-amperes of current. If the DRV8870 is powered up while both inputs are low, it immediately enters sleep mode. Only after the IN1 or IN2 pins are high for at least 5 µs (when the PGA460 initiates a burst command), the device becomes operational 40 µs to 50 µs later to drive the transducer. During these 40 µs to 50 µs, the transducer is floating and does not become excited even though the OUTA and OUTB pins from the PGA460 are toggling. Depending on the drive frequency, the user must set the pulse count to a value slightly larger than the actual required pulse count to account for the loss of pulses during the DRV8870's wake-up time. These additional pulses serve as blank or void pulses while the DRV8870 wakes-up from its low-power mode.

3.3 Half-Bridge vs Full-Bridge Performance

To compare the performance of a half-bridge driver versus a full-bridge driver, both driver modes are tested under the same device register settings, supply voltage, and environmental conditions.

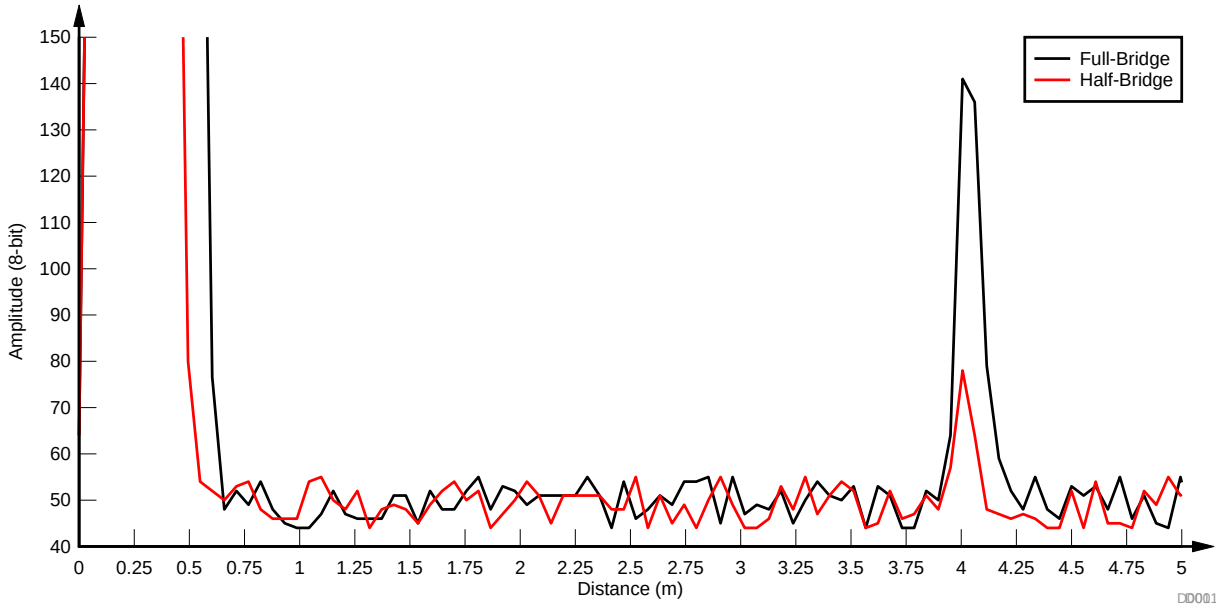

Figure 8. Mono-Static Murata™ MA58MF14-7N Echo Data Dump Targeting ISO-Pole at 4 m With a 24-V Supply, 20 Pulses, and 74 dB of AFE Gain

3.4 Schematic, Layout, and BOM

The PGA460Q1SFF-DDFB reference design files are available as SLAC761 for bi-static and SLAC756 for mono-static. The files included are the schematic and layout files of the design, the bill of materials, and the Gerber-based output files.

3.4.1 Schematic

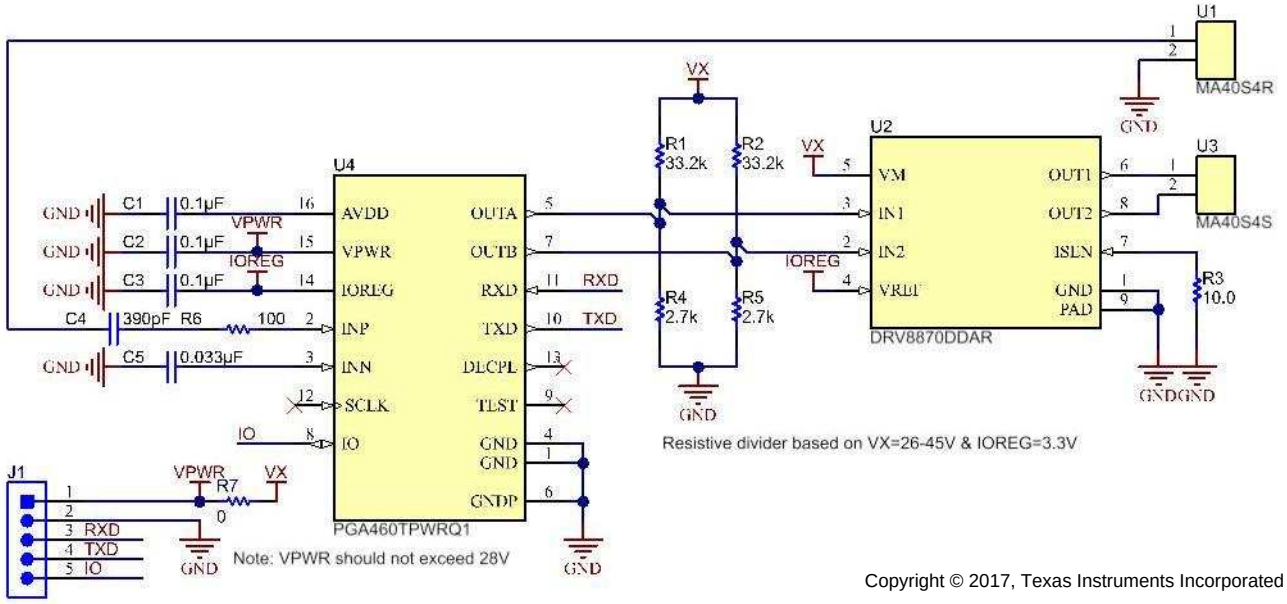

Figure 9. PGA460Q1SFF-DDFB Bi-Static Schematic

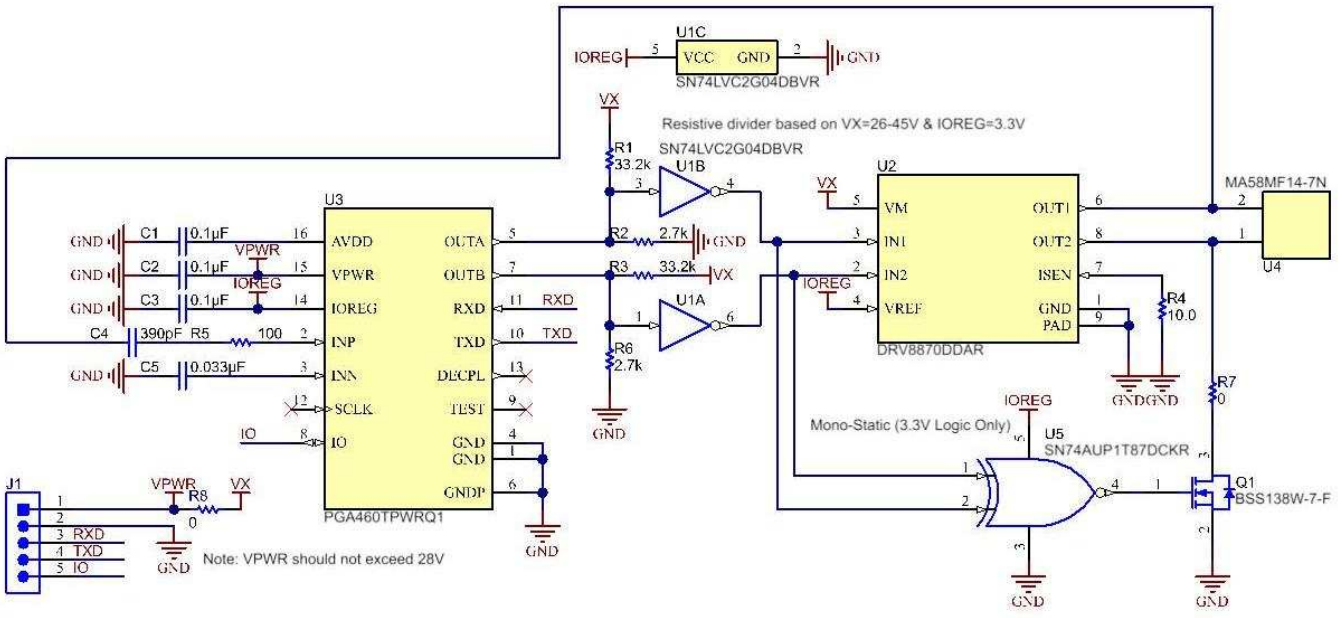

Figure 10. PGA460Q1SFF-DDFB Mono-Static Schematic

3.4.2 Layout

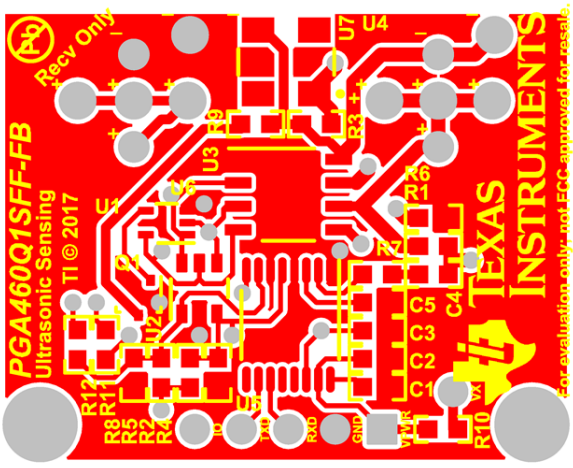

Figure 11. Top Layer Copper and Overlay

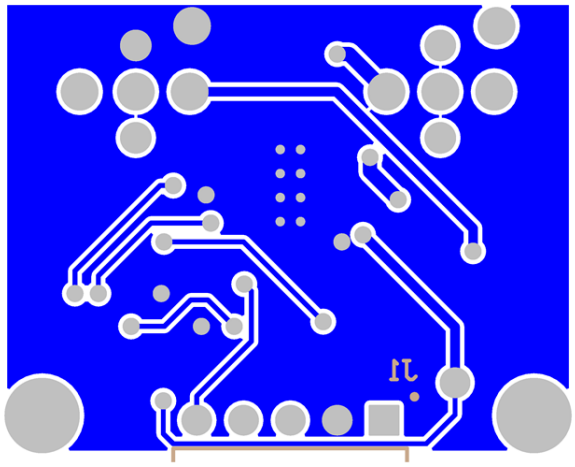

Figure 12. Bottom Layer Copper and Overlay

3.4.3 Bill of Materials (BOM)

Table 1. Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE	PART NUMBER	MANUFACTURER
C1, C2, C3	3	0.1 µF	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	0603	C1608X7R1H104K080AA	TDK
C4	1	390 pF	CAP, CERM, 390 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C2A391JA01D	Murata
C5	1	0.033 µF	CAP, CERM, 0.033 µF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H333KA61D	Murata
J1	1		Header, 100mil, 5x1, Gold, R/A, TH	5x1 R/A Header	TSW-105-08-G-S-RA	Samtec
R2, R5	2	33.2 k	RES, 33.2 k, 1%, 0.1 W, 0603	0603	CRCW060333K2FKEA	Vishay-Dale
R4, R8	2	2.7 k	RES, 2.7 k, 5%, 0.1 W, 0603	0603	CRCW06032K70JNEA	Vishay-Dale
R6	1	10.0	RES, 10.0, 1%, 0.25 W, 0603	0603	CRCW060310R0FKEAHP	Vishay-Dale
R7	1	100	RES, 100, 5%, 0.1 W, 0603	0603	CRCW0603100RJNEA	Vishay-Dale
R10, R11, R12	3	0	RES, 0, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
U1	1	40 kHz	Ultrasonic Sensor, for Receiver, 40 kHz, TH	D9.9xH7.1 mm	MA40S4R	Murata
U3	1		3.6A Brushed DC Motor Driver (PWM Ctrl), DDA0008E (SOIC-8)	DDA0008E	DRV8870DDAR	Texas Instruments
U4	1	40 kHz	Ultrasonic Sensor, for Transmitter, 40 kHz, TH	D9.9xH7.1 mm	MA40S4S	Murata
U5	1		Automotive Ultrasonic Signal Processor & Transducer Driver, PW0016A (TSSOP-16)	PW0016A	PGA460TPWRQ1	Texas Instruments
Q1	1	50 V	MOSFET, N-CH, 50 V, 0.2 A, SOT-323	SOT-323	BSS138W-7-F	Diodes Inc.
R1, R9	2	0	RES, 0, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R3	1	2.0 k	RES, 2.0 k, 5%, 0.1 W, 0603	0603	CRCW06032K00JNEA	Vishay-Dale
U2	1		Dual Inverter, DBV0006A, LARGE T&R	DBV0006A	SN74LVC2G04DBVR	Texas Instruments
U6	1		LOW POWER, 1.8/2.5/3.3-V INPUT, 3.3-V CMOS OUTPUT, 2-INPUT EXCLUSIVE-NOR GATE, DCK0005A (SOT-SC70-5)	DCK0005A	SN74AUP1T87DCKR	Texas Instruments

4 PGA460 and Discrete Full-Bridge Solutions

In the case where the DRV8870 is too costly or the power consumption is too large, the PGA460 can still be operated in a full-bridge mode using a discrete implementation. Similar to the DRV8870 implementation, the entire full-bridge circuit is external to the PGA460, and the OUTA and OUTB pins are repurposed exclusively for driving the external gates. Two discrete full-bridge implementations have been tested: holistic and minimalist.

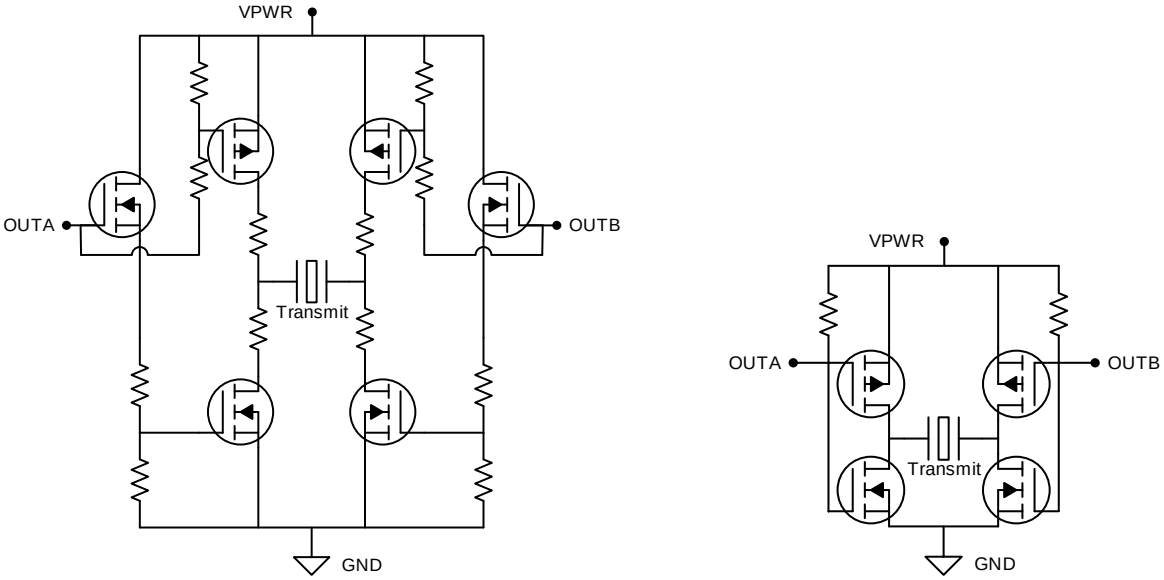

Figure 13. Discrete Full-Bridge Driver Block Diagrams for PGA460

The following solutions demonstrate the discrete implementation for bi-static modes only. The idle state of these discrete solutions forces both low-side critical-paths to ground—similar to the brake mode of the DRV8870 implementation. To enable a discrete mono-static mode, an OUTA-OUTB based XOR gate and additional N-MOSFET in series to the positive terminal's low-side critical path must be introduced to force the positive terminal to a high-impedance state while listening for return echoes.

4.1 Discrete-Holistic

The discrete-holistic implementation gives the user access to all of the MOSFETs and passives to balance the response and power dissipation of the full-bridge circuit.

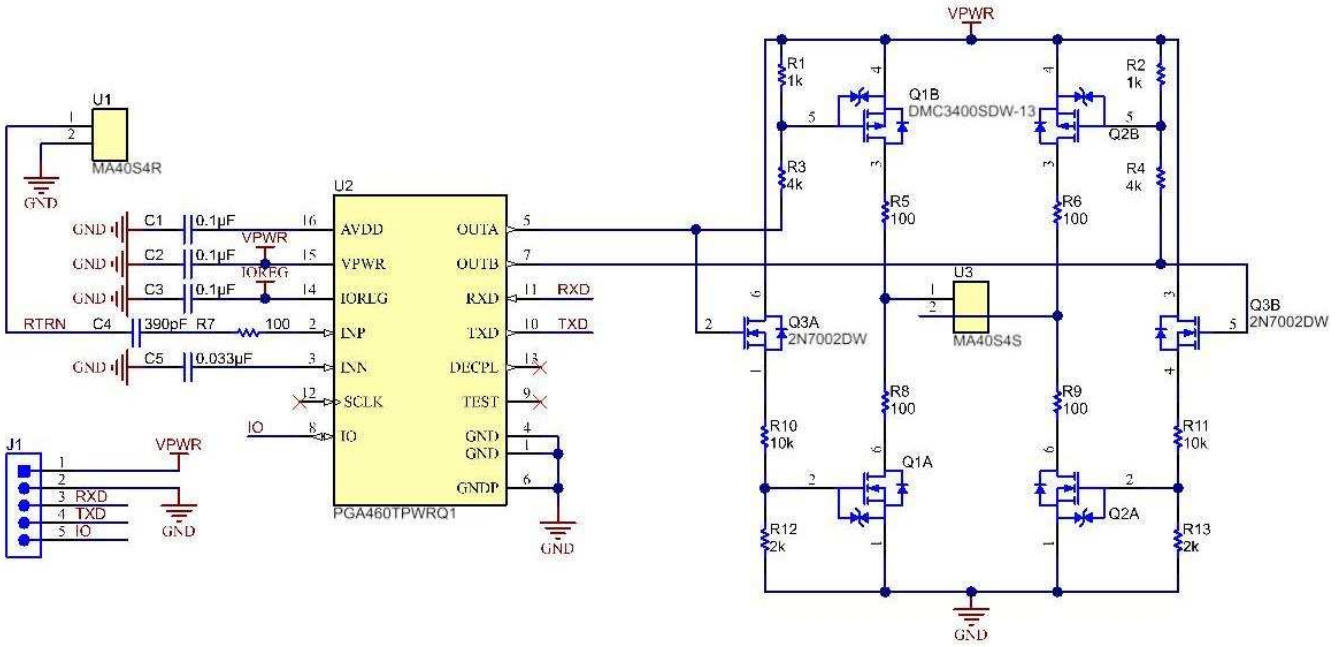

Figure 14. Discrete-Holistic Full-Bridge Driver Schematic

The disadvantage of the discrete-holistic implementation is continuous static current and shoot-through current present throughout both sides of the bridge circuit.

4.1.1 Continuous Static Current

Similarly to the DRV8870 implementation, the holistic implementation requires continuous power dissipation to drive the MOSFETs correctly.

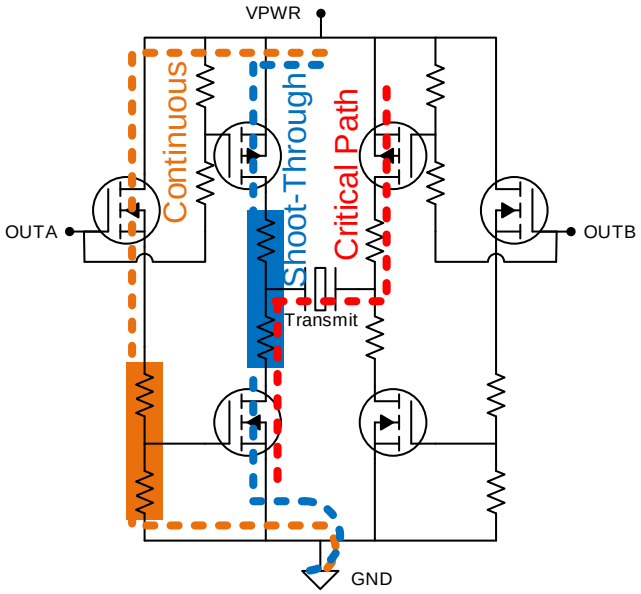

Figure 15. Continuous and Shoot-Through Currents of Discrete-Holistic

The continuous static current can be limited to sub-mA levels, but the extended turnon and turnoff delays created by the larger current limiting resistances cause the critical path of the bridge circuit to sink shoot-through current during the burst cycle for longer durations. Consider the trade-offs when selecting the resistive values of the gate driver:

- Reduce the continuous static current consumption to sub-mA levels, but allow for a larger and longer shoot-through current level and duration to sink only during the burst period.
- Allow for a continuous static current consumption upwards of 3 to 5 mA, and reduce the shoot-through current to a brief transient duration during the burst-period.

4.1.2 Limiting Shoot-Through Current

The resistors placed in series to the critical path of the bridge circuit are intended to reduce the shoot-through current, without excessively loading the transducer. For example, a value of 100 Ω has a negligible impact on the peak-to-peak excitation of the transducer but only limits the peak shoot-through current to 250 mA. However, while a value 1 kΩ halves the peak shoot-through current to 125 mA, this resistance does not allow the transducer to properly charge and discharge at the resonant frequency, which yields a loss in peak-to-peak excitation voltage. A value of 4 kΩ shows no shoot-though current but severely hinders peak-to-peak excitation voltage to less than 50% efficiency.

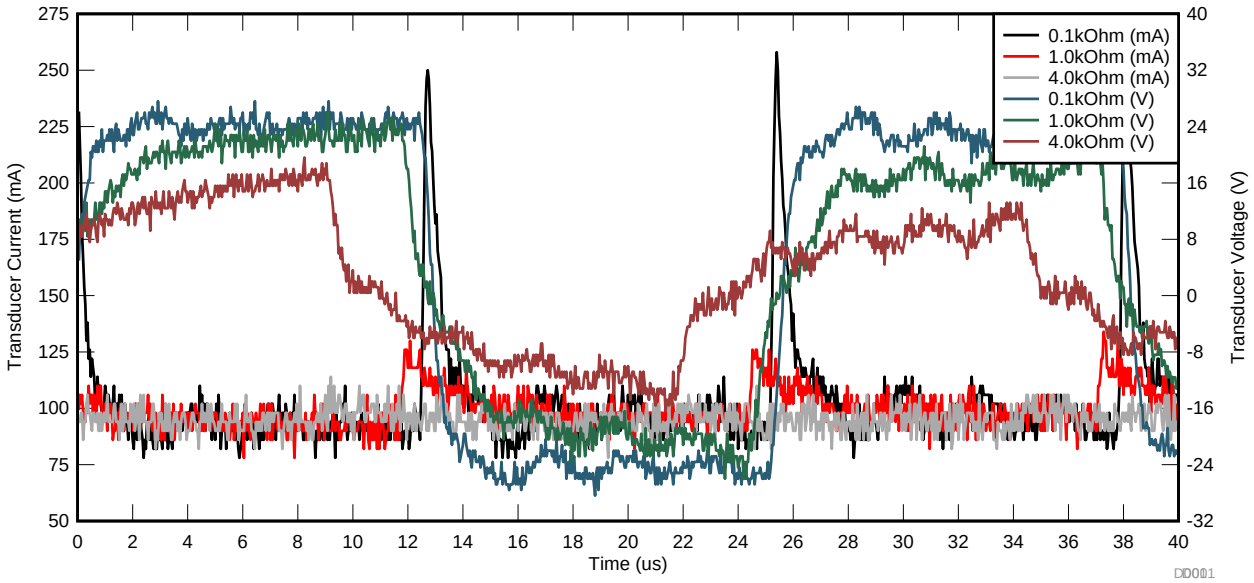

Figure 16. Shoot-Through Current Across Various Critical Path Resistance at 24-V Reference

Optimization of the shoot-through current limiting resistors is dependent on the specific transducer but should typically be limited to sub-kΩ values for maximum transmit performance. Critical path resistors are not required on both high and low sides (can be placed on high or low side only), but fine-tuning and balancing the signal integrity of the excitation voltage is possible by splitting the shoot through current limiting resistors at both the high and low sides. The user must determine how much shoot-through current is acceptable while considering the impact on peak-to-peak excitation voltage.

4.2 Discrete-Minimalist

To avoid the complexities of the discrete-holistic implementation, the discrete-minimalist implementation mainly relies on the MOSFET ratings of the critical path. By eliminating the two external N-MOSFETs used to drive the critical path N-MOSFETs and driving the P-MOSFETs directly using OUTA and OUTB, only two high-side P-MOSFETs and two low-side N-MOSFETs are required for the discrete-minimalist implementation.

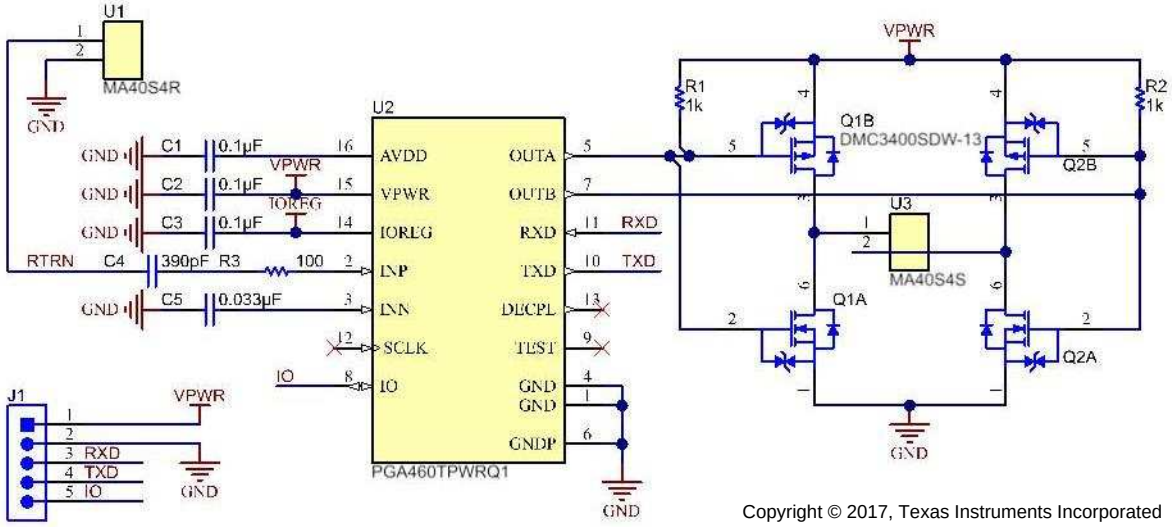

Figure 17. Discrete-Minimalist Full-Bridge Driver Schematic

Considering the high-side supply voltage, the gate-source (VGS) and drain-source (VDS) voltage ratings should not be violated to prevent damage to the MOSFETs in the critical path. Because the majority of cost-effective MOSFETs typically tend to have a VGS rating of < 20 V, finding components for the discrete-minimalist implementation at larger supply voltages may become a more difficult and costly task. The holistic-discrete implementation has the benefit of leveraging P-MOSFETs with a VGSS rating of 20 V and still be able to support a high-side voltage greater than 20 V due to the additional pair of N-MOSFET gate drivers and resistive voltage dividers at the gates of the MOSFETs in the critical path.

Though the discrete-minimalist circuit excludes the negative the shoot-through current-limit resistors, these can still be added (recommended) in series to the critical path in the event the transients are too strenuous on the high-side voltage supply or if the MOSFETs are not rated to support large instantaneous forward currents.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October2017) to A Revision	Page
• Deleted Removed figure 3 and 4 from the image matrix.	2
• Deleted Removed row 19 from table 1.	9

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