Collin Wells, Ting Ye

TI Precision Designs: Verified Design

Band-Pass Filtered, Inverting -40 dB Attenuator, 10 Hz – 100 kHz, 0.1 dB Error

TEXAS INSTRUMENTS

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TINA-TI™	SPICE Simulator
OPA1611	Product Folder

Circuit Description

An attenuator circuit is required when the magnitude of an input signal needs to be reduced. This version of an inverting attenuator features an easily tunable band-pass filter that is useful to limit noise and also allows for independent control of the dc output level. The circuit can be used in a variety of applications from low-level signal generation to large input signal attenuation.

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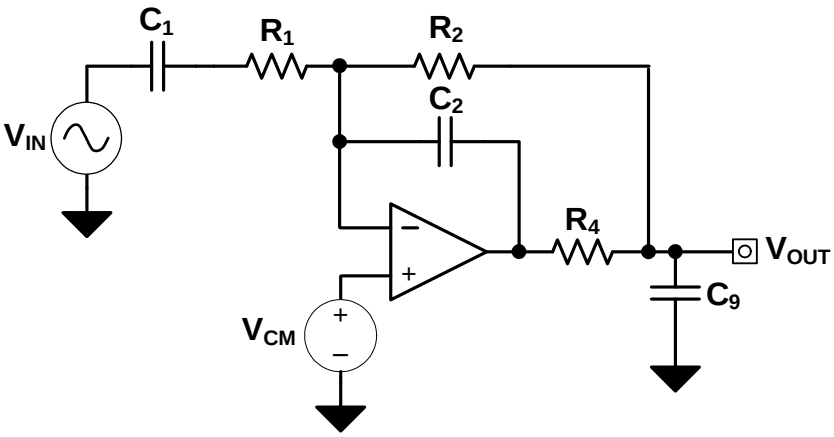

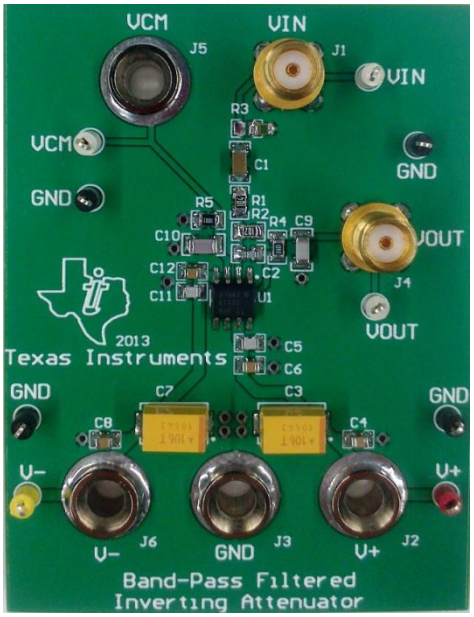

1 Design Summary

The design requirements are as follows:

- Supply Voltage: +/-15 V
- Input: 100 mVpp to 50 Vpp
- Output: -40 dB

The design goals and performance are summarized in Table 1. Figure 1 depicts the ac transfer function of the design measured from 1 Hz to 10 MHz.

Table 1. Comparison of Design Goals, Simulated, and Measured Performance

	Goals	Simulated	Measured
Offset (mV)	1	0.0623	0.11388
10 Hz Gain Error (dB)	0.5	0.122	0.11
1 kHz Gain Error (dB)	0.1	0.0061	0.01
100 KHz Gain Error (dB)	0.5	0.5876	0.05
Output Noise 10 MHz (µVrms)	5	2.327	3.521
Quiescent Current (mA)	5	3.797	3.844

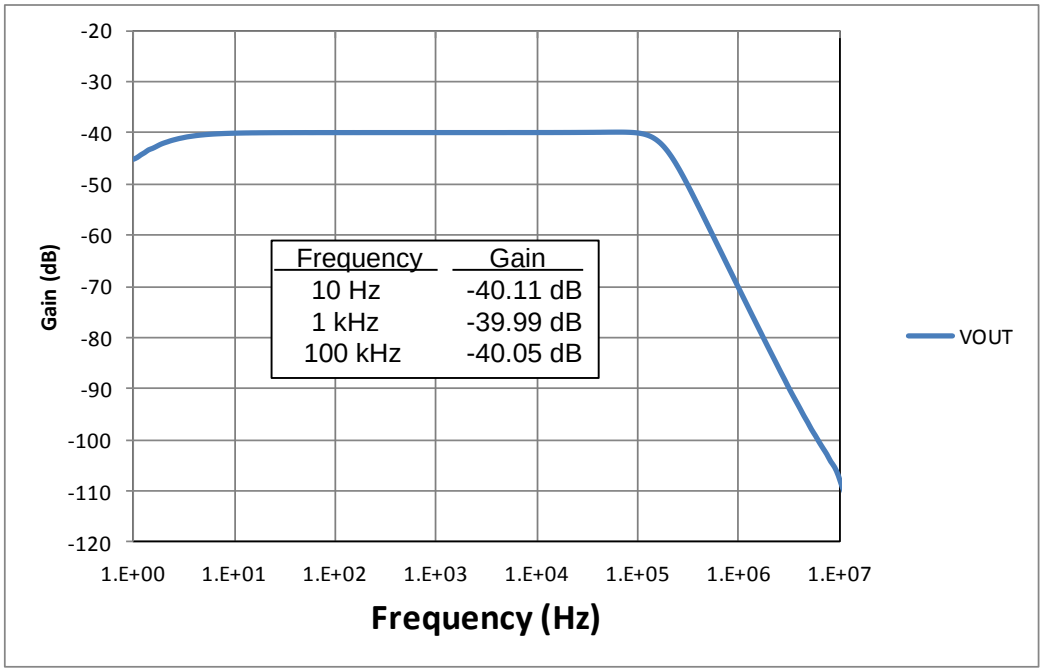

Figure 1: Measured ac transfer function

2 Theory of Operation

A more complete schematic for this design is shown in Figure 2 and the full transfer function is shown in Equation 1. Although the full transfer function looks daunting, the circuit can be broken down into a few easy to design subsections. The circuit is based on a standard inverting amplifier and the ratio of the input resistor, R_1, and the feedback resistor, R_2, set the pass-band attenuation. The combination of R_1 and the input capacitor, C_1, create the 1st order high-pass filter and R_2, C_2, the output resistor, R_4, and the output capacitor, C_9, make up the 2nd order low-pass filter. R_5 and C_{10} are used to provide decoupling of the V_{CM} signal and to ensure that the non-inverting input of the amplifier does not float if the reference voltage, V_{CM}, is not connected. R_3 is used to terminate a 50 Ω input signal and can be removed if not desired. The values of R_3, R_5, and C_{10} do not affect the transfer function of this design.

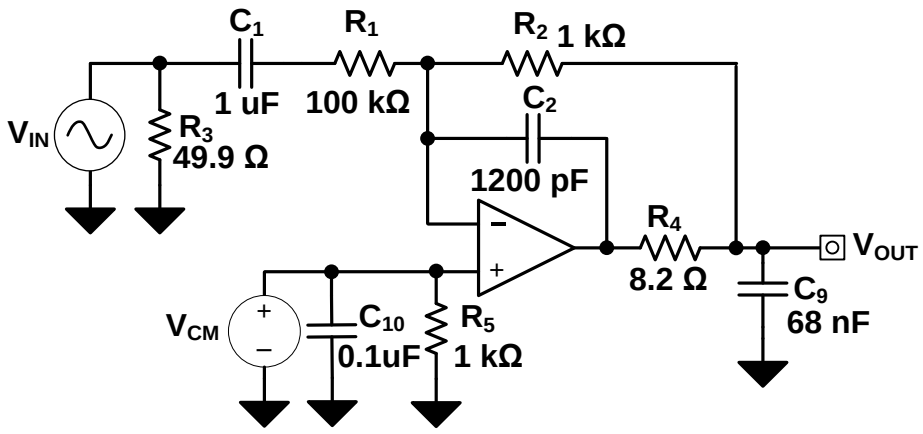

Figure 2: Circuit schematic

$$\frac{V_{OUT}}{V_{IN}} = -\frac{(R_2C_1)s}{\left(1+\left((R_1C_1)+(R_2C_2)+(R_4C_2)\right)s+\left((R_1R_2C_1)+(R_1R_4C_1)+(R_2R_4C_9)\right)s^2+\left((R_1R_2R_4C_1C_2C_9)\right)s^3\right)} + V_{CM} \quad (1)$$

In the following sections, a brief circuit stability overview will be provided and then the circuit will be divided into two sub-circuits that allow for easier design of the pass-band gain, 2nd order low-pass filter, and 1st order high-pass filter.

2.1 Circuit Stability

A full stability analysis is outside the scope of this document and can be reviewed using the first reference is Section 9. However, the two design requirements that must be met to keep this design stable will be explained. The first requirement is that the output resistor, R_4, must be large enough to effectively cancel the interaction of the output capacitor, C_9, and internal op amp output impedance (not shown). This can be determined in SPICE by setting the amplifier as a non-inverting buffer driving the output resistor in series with the output capacitor. Then, input a 25 mV – 100 mV step to the input and observe the overshoot and ringing on the output of the amplifier. Continue to increase the series output resistor until a stable response with less than 25% overshoot is achieved which correlates to roughly 45° of phase margin. In this design it was determined that an 8.2 Ω series resistor properly compensated capacitive loads up to 100 nF and will therefore be used for the value of R_4 in this design.

The second requirement is that once the output capacitor and resistor have been chosen, the design must ensure that the low-pass filter formed by R_4 and C_9, LPF_{POLE1}, is greater than the frequency of the low-pass filter formed by R_2, R_4, and C_9, LPF_{POLE2}, by at least two times. This will ensure there is not any undesired gain peaking or rapid phase shifts in the feedback path which could lead to instability.

2.2 Pass-Band Gain and Low-Pass Filter Design Theory

To simplify the design of the pass-band gain and the 2nd order low-pass filter, it will be assumed that C_1 acts as a short (0 Ω) for frequencies above the high-pass filter frequency of 10 Hz. Figure 3 displays the resulting circuit after shorting C_1 while leaving the other components populated.

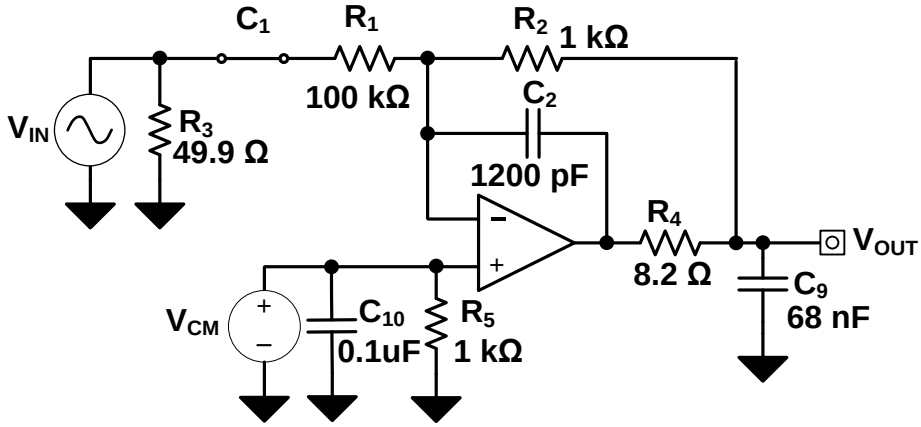

Figure 3: Simplified attenuator circuit with C_1 shorted

Equation 2 shows the s-domain transfer function of the circuit in Figure 3. The equation shows there is an inverting gain set by R_1 and R_2, and two poles that are set by the relationship between R_2, R_4, C_2, and C_9.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1\left(1+\left(\left(R_2+R_4\right)\times C_2\right)s+\left(R_2\times R_4\times C_4\times C_9\right)s^2\right)} \tag{2}$$

2.2.1 Pass-Band Gain

The inverting gain that will be present in the pass-band of the final transfer function is defined in Equation 3.

$$Gain_{PASS\text{-}BAND} = -\frac{R_2}{R_1} \tag{3}$$

To set the pass-band gain to -40 dB (0.01 V/V), R_2 must be 100 times smaller than R_1. The input resistor, R_1, will set the ac input resistance and also will be a contributor to the final noise of the circuit. Setting it to 100 kΩ will allow for proper noise performance and will allow for the calculation of the other values in the circuit.

$$R_2 = \frac{R_1}{Gain_{PASS\text{–}BAND}} = \frac{100\,k\Omega}{100\,V/V} = 1k\Omega \tag{4}$$

2.2.2 2nd Order Low-Pass Filter

This design is supposed to operate with a relatively flat response over the frequency range of 10 Hz to 100 kHz. Therefore, the low-pass cutoff frequency must be set greater than 100 kHz to ensure a flat response up to 100 kHz. The cutoff frequencies will therefore be set greater than 150 kHz.

The design of the 2nd order low-pass filter can be simplified using Equations 5 and 6.

$$LPF_{POLE1} = \frac{1}{2\times\pi\times R_4\times C_9} \tag{5}$$

$$LPF_{POLE2} = \frac{1}{2 \times \pi \times (R_2 + R_4) \times C_2} \quad (6)$$

R_4 is in series with the output of the amplifier and should be kept small to prevent large voltage drops from forming across it if the circuit needs to deliver current to a load. The R_2 feedback path will compensate for any voltage drop across R_4 but only as long as the op amp can increase its output voltage high enough to compensate for the drop which is limited by the supply voltage and the output swing-to-rail performance of the op amp. Also, as further described in Section 2.1, the value of R_4 must properly compensate the capacitive load presented by C_9. Based on analysis also further described in Section 2.1, R_4 will be selected to be 8.2 Ω, allowing for the calculation of C_9.

As described further in Section 2.1, the frequency of LPF_{POLE2} must be less than the frequency of LPF_{POLE1}, preferably by at least two times, to ensure proper stability of the circuit. Therefore to enable LPF_{POLE2} to be set to 150 kHz, LPF_{POLE1} will be set to 300 kHz.

$$C_9 = \frac{1}{2 \times \pi \times R_4 \times LPF_{POLE1}} = \frac{1}{2 \times \pi \times 8.2\,\Omega \times 300\,kHz} = 64.7\,nF \quad (7)$$

Based on the calculation, a standard value for C_9 of 68 nF was selected.

Setting LPF_{POLE2} to 150 kHz enables the calculation of C_2.

$$C_2 = \frac{1}{2 \times \pi \times (R_2 + R_4) \times LPF_{POLE2}} = \frac{1}{2 \times \pi \times 1008.2\,\Omega \times 150\,kHz} = 1052pF \quad (8)$$

A larger standard value of 1200 pF was chosen for C_2 over a smaller value to ensure the stability of the design was maintained.

2.3 1st Order High-Pass Filter

To simplify the design of the pass-band gain and the 1st order high-pass filter, it will be assumed that C_2 and C_4 act as open circuits (>1 GΩ) for frequencies below the low-pass filter frequency of 100 kHz. Figure 4 displays the resulting circuit after opening C_2 and C_9 while leaving the other components populated.

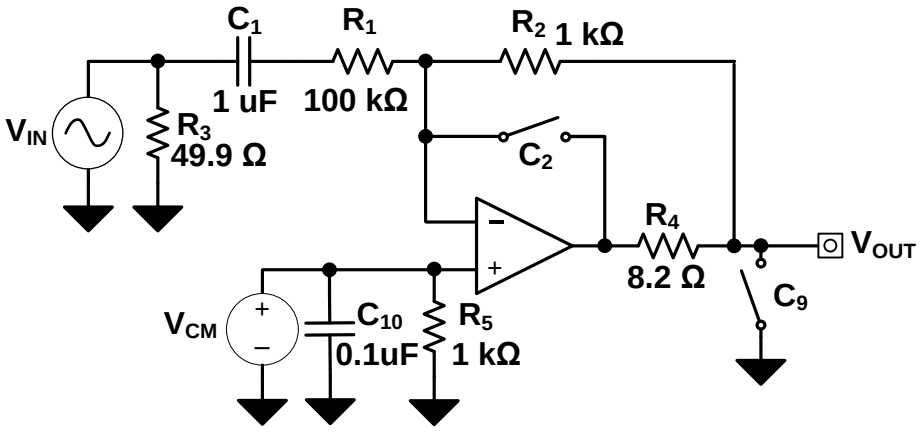

Figure 4: Attenuator circuit with C_2 and C_9 open

The s-domain transfer function for this part of the circuit is shown in Equation 9. The equation shows that there will be a zero at the origin (s = 0) and then a pole to flatten the response at the pass-band gain forming the 1st order high-pass filter.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{(R_2 \times C_1)s}{1+(R_1 \times C_1)s} \quad (9)$$

The pole that defines the high-pass filter cutoff frequency, HPF_{POLE1}, is shown in Equation 10.

$$HPF_{POLE1} = \frac{1}{2 \times \pi \times R_1 \times C_1} \quad (10)$$

To ensure little attenuation at 10 Hz, set the high-pass filter cutoff frequency below 2.5 Hz by choosing C_1.

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times HPF_{POLE1}} = \frac{1}{2 \times \pi \times 100\,k\Omega \times 2.5\,Hz} = 0.636\,uF \quad (11)$$

Choosing a standard value of 1 uF for C_1 pushes the high-pass cutoff frequency a little lower helping to further reduce attenuation at 10 Hz.

3 Component Selection

3.1 Operational Amplifier

Since this is primarily an ac application, the op amp used in this design should have **low noise, low total-harmonic-distortion (THD), high slew-rate, wide bandwidths, high open-loop gain (A_{OL})**. A rail-to-rail output stage is desirable to allow for lower supply voltage operation while maintaining good output swing capabilities.

The OPA1611 high-performance bipolar input audio op amp has only 1.1nV/√Hz input noise and 0.00015% THD at 1 kHz, 27V/us slew rate, 40 MHz bandwidth, and 130 dB of A_{OL} making it an excellent choice for a high performance version of this circuit.

Other amplifier options for this application include the chopper-stabilized OPA211, OPA134, or OPA234 as further discussed in Section 7.

3.2 Passive Component Selection

The most critical passive components to meet the 0.1 dB gain error specification for this design are the resistors that set the pass-band gain, R_1 and R_2. These resistors were chosen to be 0.1% tolerance to ensure good gain accuracy without calibration. Resistors R_1 and R_4 and capacitors C_2 and C_9 were selected for the lowest tolerances reasonably available 1% and 5% respectively. If tighter accuracy of the AC frequency points is desired, use lower tolerance devices for these components as well.

Any capacitors in the signal path should be sized for a voltage coefficient that well exceeds the voltage that will be placed across them to ensure that the values don't change in circuit during normal operation. To keep the signal distortion to a minimum, use C0G/NP0 dielectric capacitors when possible. When C0G/NP0 capacitors are not available due to the need for higher capacitance values or voltage ratings choose X7R dielectrics.

The tolerance of the other passive components in this design may be selected for 1% or greater because they will not directly affect the pass-band transfer function of this design.

4 Simulation

The TINA-TI™ schematic shown in Figure 5 includes the circuit values obtained in the design process. A dc offset voltage of 62.6 µV and dc quiescent current of 3.797 mA were reported by the simulation.

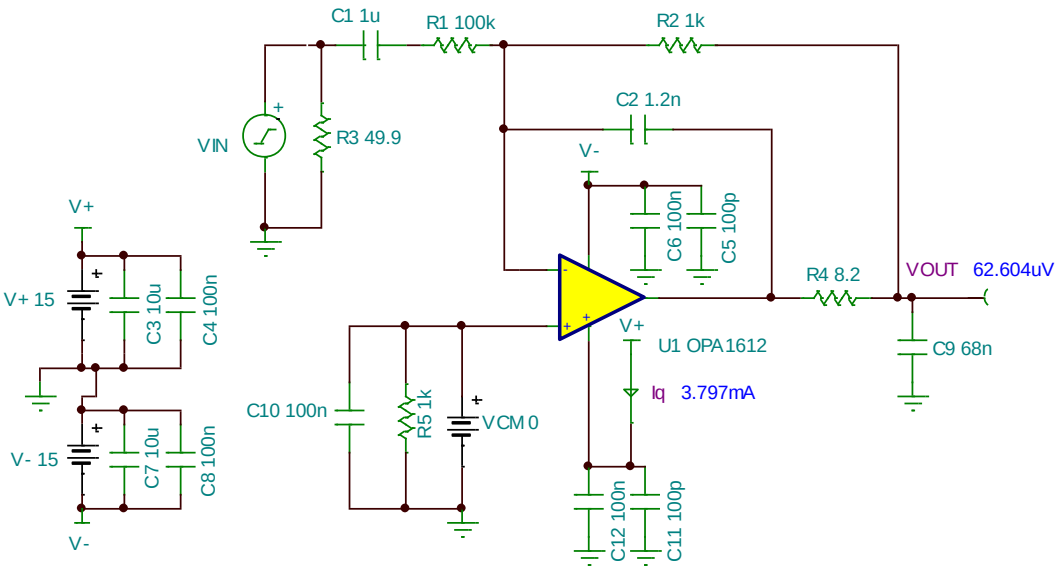

Figure 5: TINA-TI™ simulation schematic showing dc output offset and quiescent current

4.1 AC Transfer Function

The ac transfer function results of the circuit, shown in Figure 6, show the proper pass-band gain and filter frequencies based on the component values calculated in Section 2.

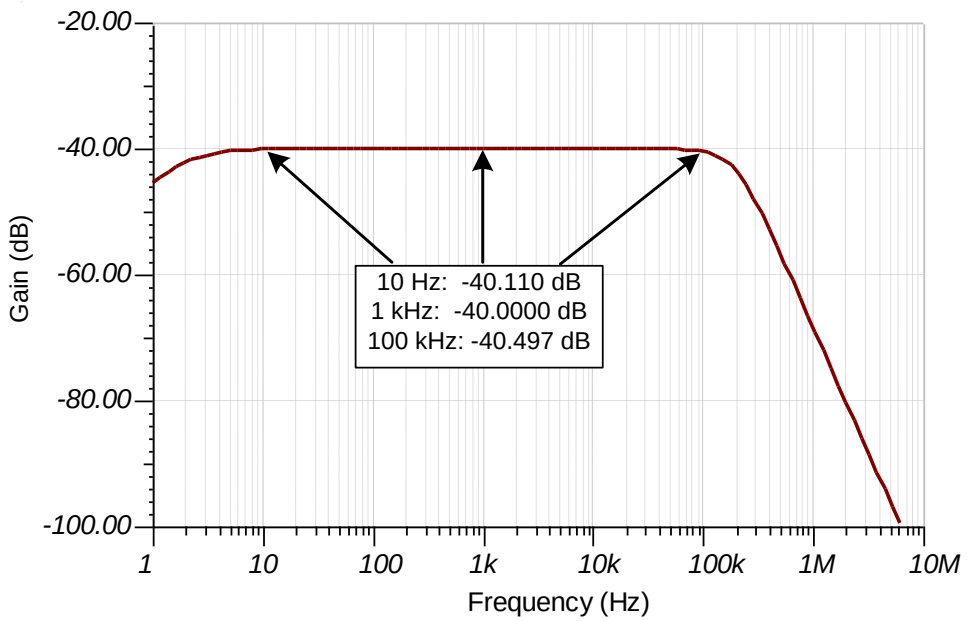

Figure 6: Simulated Full-Scale Transfer Function

A 100-sweep Monte-Carlo simulation was run with the component tolerances specified in Section 3 to produce more realistic results. Figure 7 shows a zoomed-in version of the ac transfer function allowing the deviation between the Monte-Carlo cases to be viewed easier.

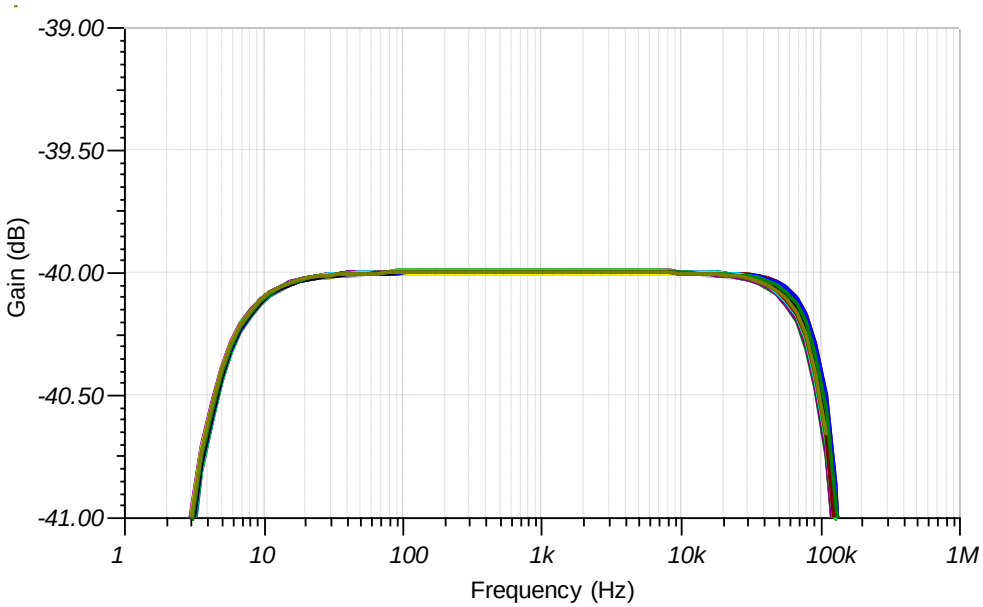

Figure 7: Simulated Monte-Carlo Full-Scale Transfer Function

The numerical results of the Monte-Carlo simulation are displayed in Table 2. To determine the total gain error in dB at a given frequency, take the standard deviation and multiply it by three times (3-σ) to cover roughly 99.7% of the units. The 3-σ value can then be added to the difference of the average results from the ideal gain of -40 dB to determine a realistic gain error that a population of built units would show.

$$\text{GainError(dB)} = (3\times\sigma) + \left|\mu - \text{Gain}_{\text{IDEAL}}\right| = (3\times 0.00195) + \left|(-39.9998) - (-40)\right| = 0.0061 \quad (9)$$

Table 2: Monte-Carlo DC Transfer Results

	Min	Max	Average (μ)	Std. Dev. (σ)	3-σ Gain Error
Gain at 10 Hz (dB)	-40.1183	-40.097	-40.1083	0.00458	0.122
Gain at 1 kHz (dB)	-40.0043	-39.9952	-39.9998	0.00195	0.0061
Gain at 100 kHz (dB)	-40.5583	-40.4388	-40.4959	0.03055	0.5876

4.2 Transient Response

The transient response of the design with a 100 mVpp, 1 kHz sine-wave input signal is shown in Figure 8. As expected, the output is 1 mVpp with the small dc offset reported in Table 1. This test case is an example of a useful application of this circuit for attenuating the outputs of function generators which commonly have minimum output amplitudes of 100 mVpp.

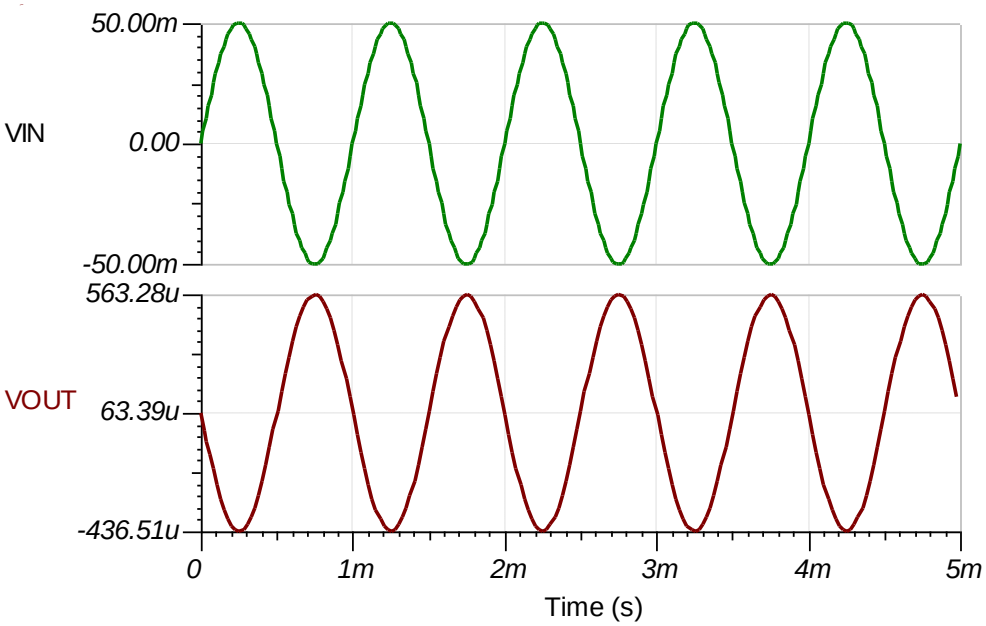

Figure 8: TINA-TI™ - Low-level signal generation with 100 mVpp input and 1 mVpp output

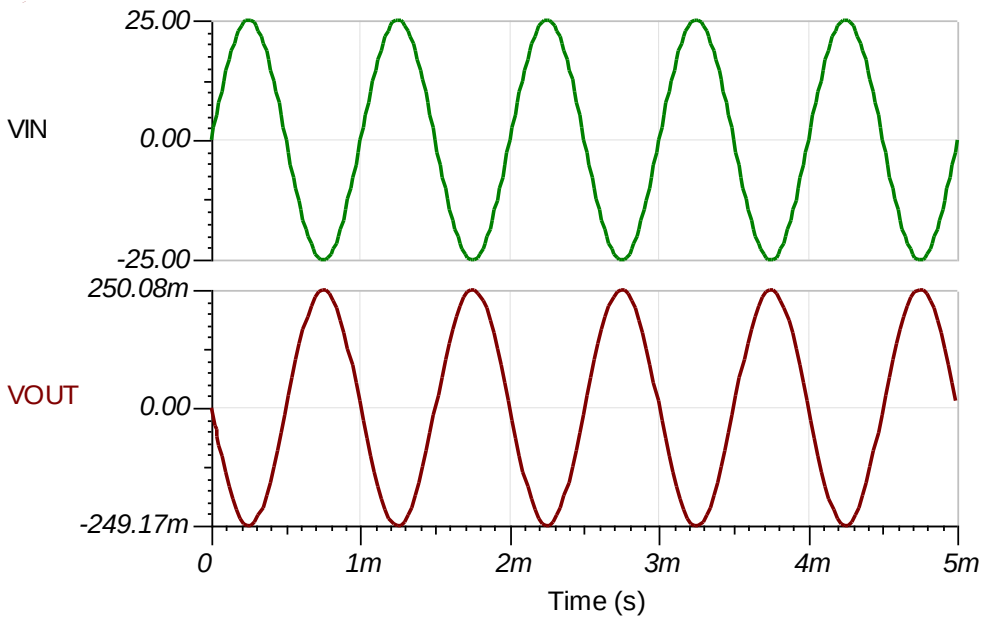

Figure 9: TINA-TI™ - Large signal attenuation with 50 Vpp input and 500 mVpp output

4.3 Step Response

The small-signal stability of the system was verified by shorting V_{IN} to GND and applying a step response to the non-inverting input of the op amp that caused the output to change by roughly 100 mV. The results are shown in Figure 10.

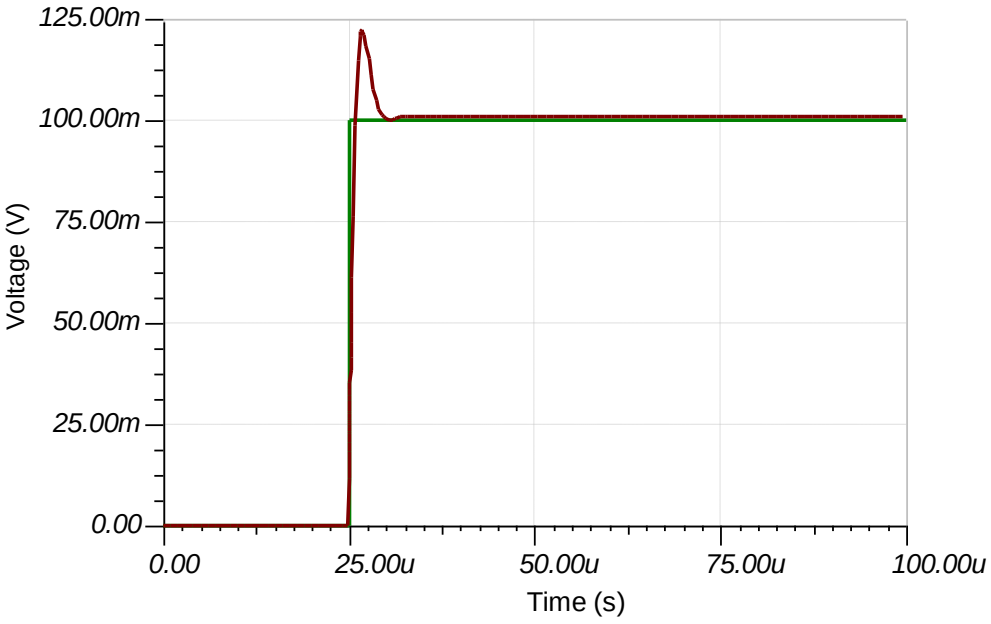

Figure 10: TINA-TI™ - Small-Signal Step Response Simulation

4.4 Noise Testing

The total noise of the circuit was simulated from 1 Hz to 10 MHz. The results, shown in Figure 11 display the noise bandwidth of the circuit to be roughly 450 kHz.

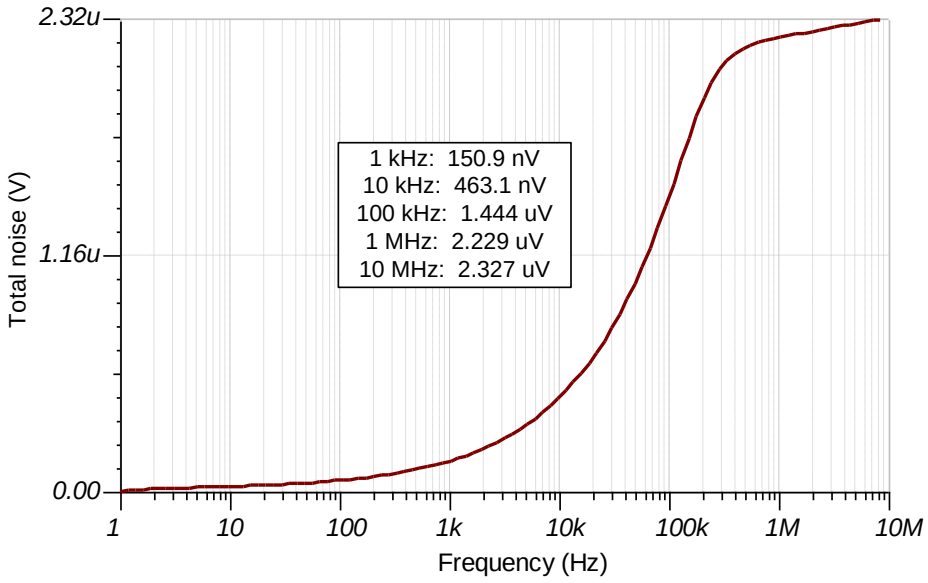

Figure 11: TINA-TI™ - Total output noise from 1 Hz to 10 MHz

4.5 Simulated Result Summary

The simulation results are compared against the design goals in Table 3.

Table 3: Simulated Result Summary

	Goals	Simulated
Offset (mV)	1	0.0623
10 Hz Gain Error (dB)	0.5	0.122
1 kHz Gain Error (dB)	0.1	0.0061
100 KHz Gain Error (dB)	0.5	0.5876
Output Noise 10 MHz (µVrms)	5	2.327
Quiescent Current (mA)	5	3.797

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.1 and A.2.

5.1 PCB Layout

For optimal performance in this design follow standard precision PCB layout guidelines including: using ground planes, proper power supply decoupling, keeping the summing node as small as possible, and using short thick traces for sensitive nodes. The layout for the design is shown in Figure 12.

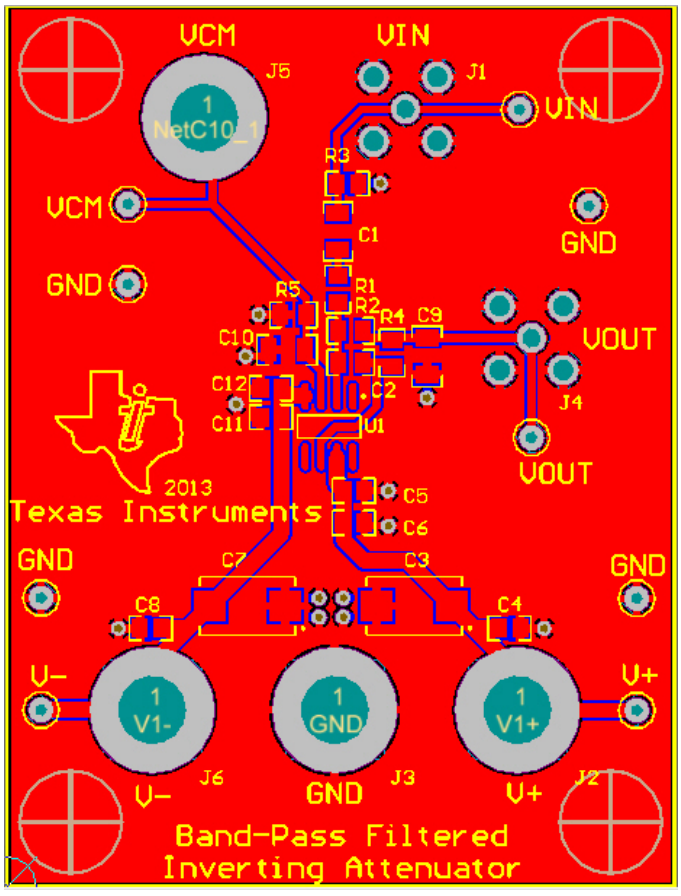

Figure 12: Altium PCB Layout

6 Verification and Measured Performance

6.1 AC Transfer Function

AC transfer function data was collected using a gain phase analyzer that swept the input signal from 1 Hz – 10 MHz while measuring the output signal. The results are displayed in Figure 13 and Table 5.

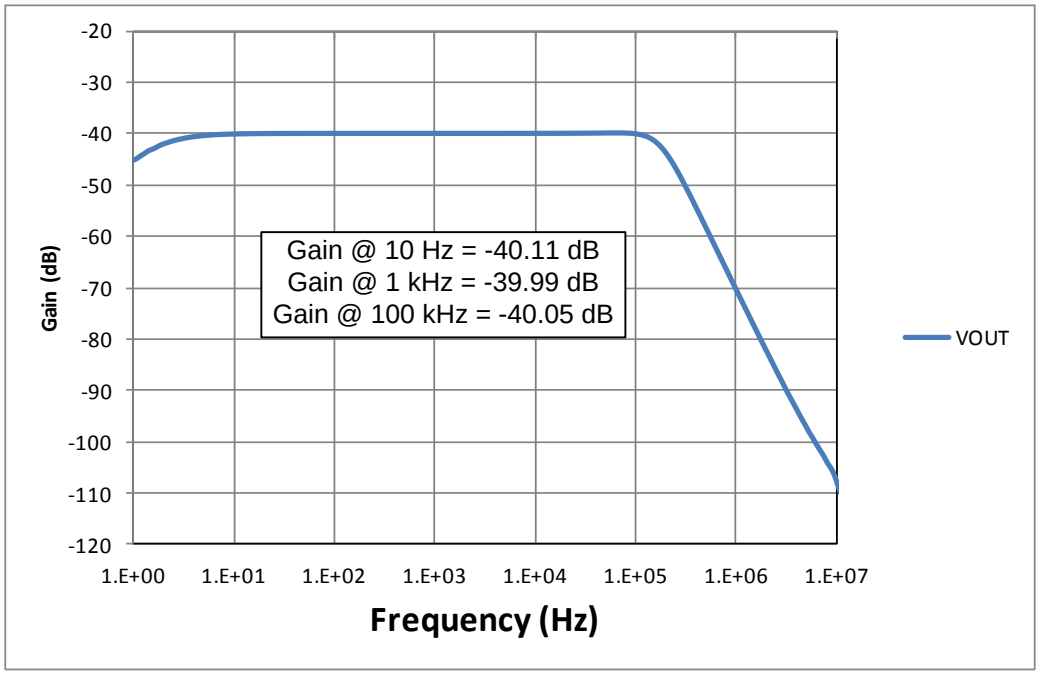

Figure 13: Measured ac transfer function

Table 4: Measured ac result summary

	Measured
10 Hz Gain Error (dB)	0.11
1 kHz Gain Error (dB)	0.01
100 KHz Gain Error (dB)	0.05

6.2 DC Measurements

DC measurements were made for the offset voltage and the quiescent current for five units. The average values are reported in Table 5 below.

Table 5: Measured dc result summary

	Measured
Output Offset Voltage (mV)	0.11388
Quiescent Current (mA)	3.844

6.3 Transient Measurements

6.3.1 Small Signal Generation

Testing a high-gain input stage requires a low-level test signal source to prevent the input stage from saturating. This circuit is useful for attenuating the outputs of common function generators to create these low-level test signals. Figure 14 displays the generation of a 1 mVpp output signal from a 100 mVpp input signal.

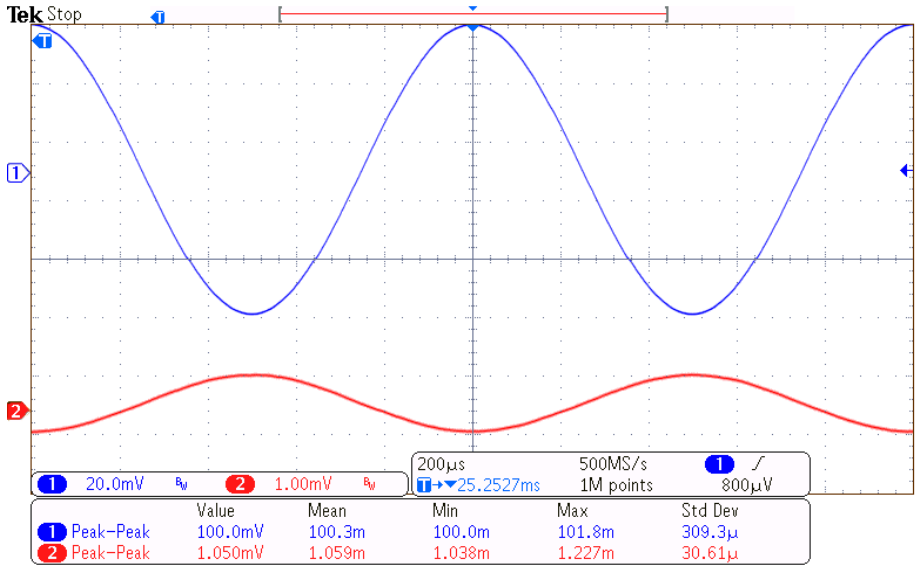

Figure 14: Measured transient response with 100 mVpp input and 1 mVpp output

6.4 Large Signal Attenuation

The topology used for this design accommodates input signals that are above the supply rails applied to the op amp. This is demonstrated in Figure 15 where a 50 Vpp input signal is applied when only +/-15 V (30 Vpp) supplies were used to power the op amp. The circuit can tolerate higher voltages but extreme caution should be used when testing with voltages above 50 V.

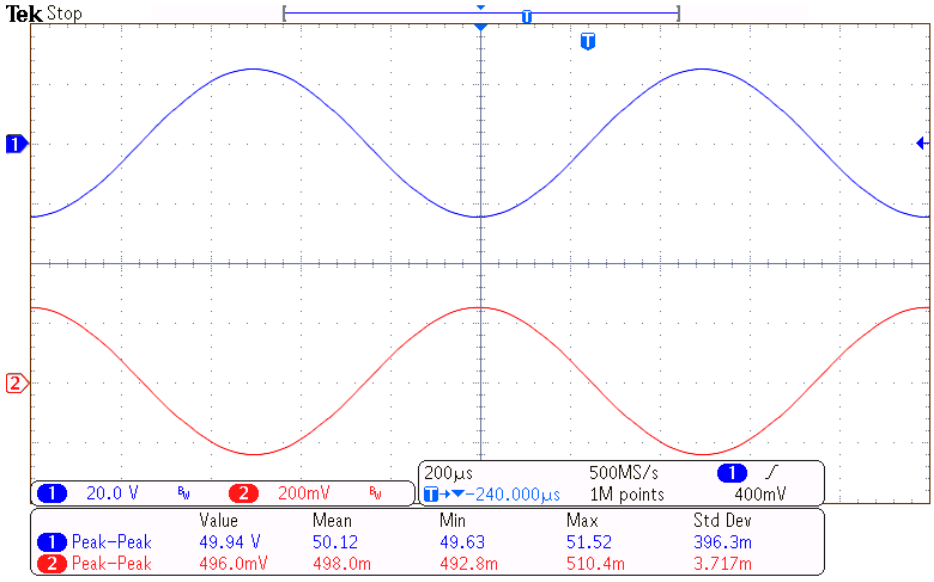

Figure 15: Measured transient response with 50 Vpp input and 500 mVpp output

6.5 Small-Signal Stability

The small-signal response is indicative of the stability of a circuit design. An unstable design presents unwanted overshoot, ringing, and long settling times. Figure 16 displays the output of the attenuator circuit when a 100 mV step input (Channel 1) is applied to the non-inverting input of the circuit. The output Channel 2) quickly settles to the input level with almost no overshoot or ringing indicating a stable design.

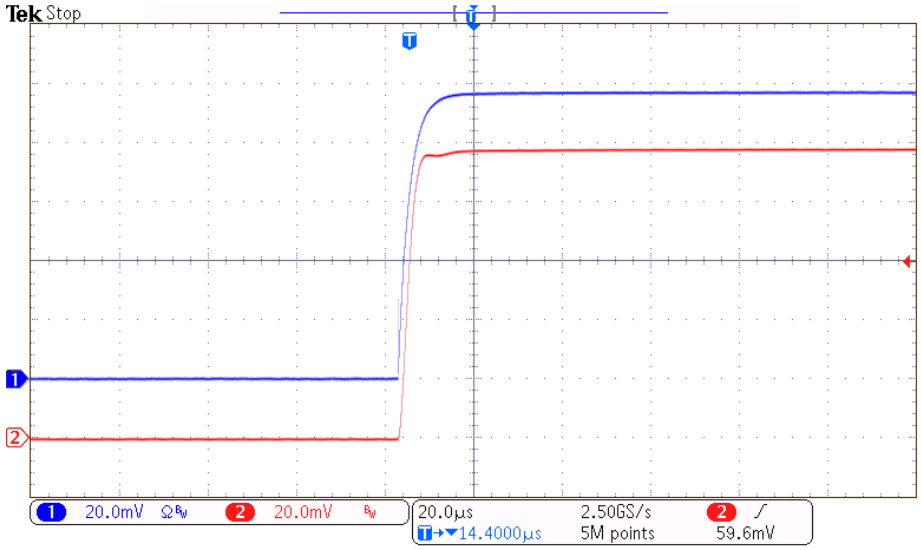

Figure 16: Measured small signal step response for stability analysis

6.6 Output FFT

The FFT was taken from 20 Hz to 100 kHz to view the output spectrum of the circuit with a 1 Vrms 1 kHz input signal. The output spectrum shows the expected -40 dB output at 1 kHz and the rest of the frequency spectrum is very clean with a low noise floor.

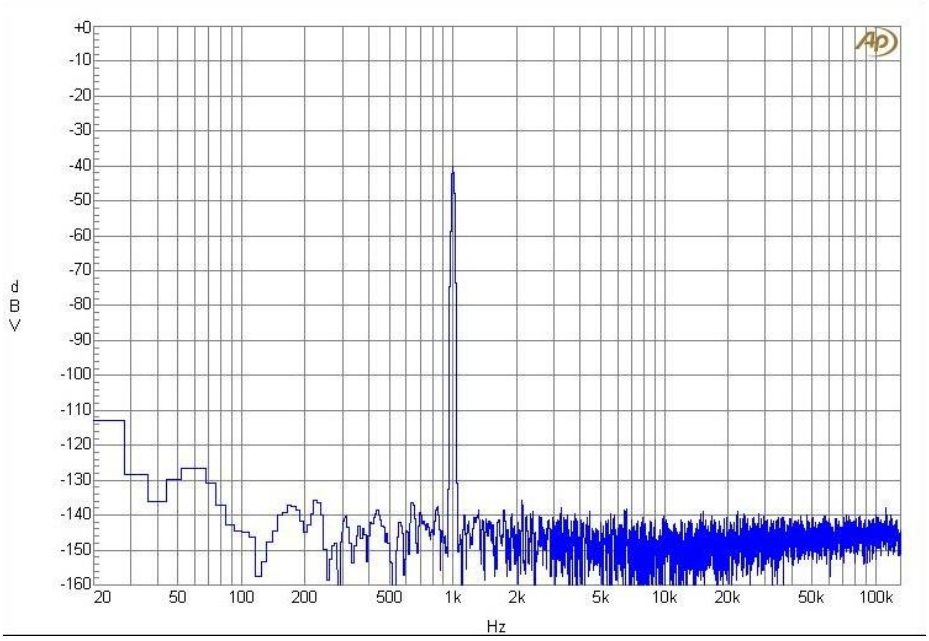

Figure 17: Measured FFT with 1 kHz 1 Vrms input and 1 Vrms reference

6.7 Output Noise

The output noise of this attenuator was measured to a 10 MHz bandwidth using a 101 V/V, low-noise, band-pass filtered gain stage to increase the noise output of the attenuator circuit to a level measurable by common lab equipment. For more information on op amp circuit noise and the calculation, simulation, and measurement of noise see the second reference in Section 9. A TINA-TI™ representation of the 101 V/V filtered gain stage is shown in Figure 18. The output of the attenuator circuit is high-pass filtered by C_{G1} and R_{G1}, then gained by 101 V/V by U2, R_{G2}, and R_{G3}, and then lastly is low-pass filtered at 10 MHz by R_{G4} and C_{G2}.

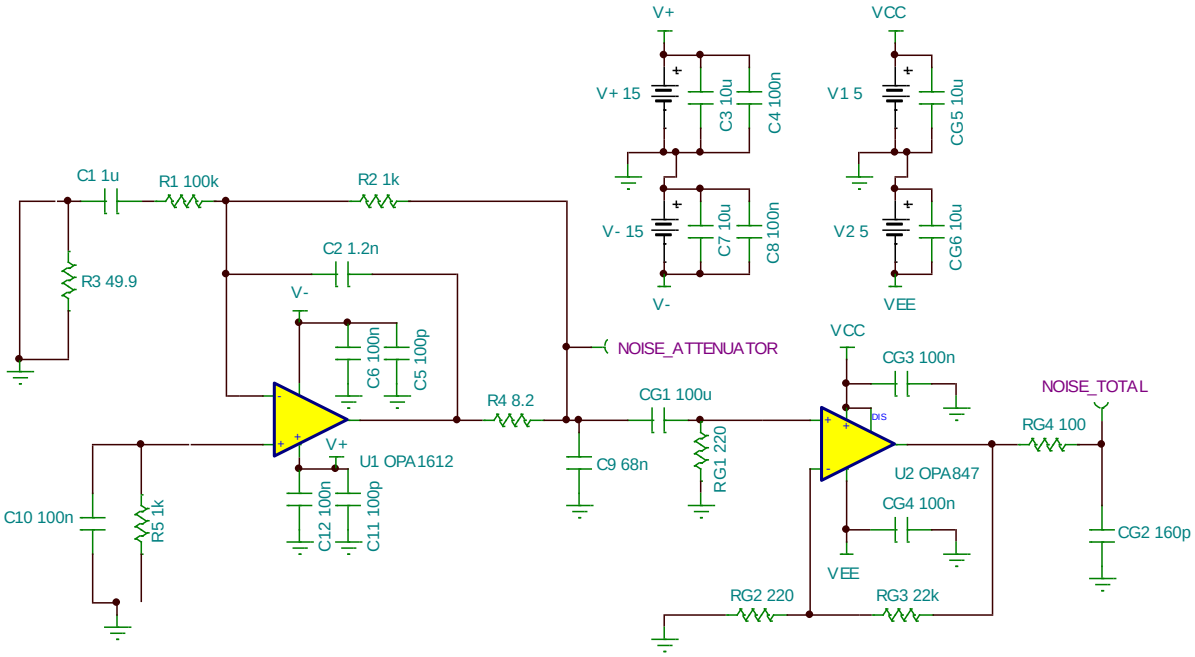

Figure 18: TINA-TI™ – Attenuator circuit noise measurement test configuration

The output noise of the circuit shown in Figure 18 ($Noise_{TOTAL}$) is measured and then the output noise of the attenuator circuit ($Noise_{ATTENUATOR}$) is calculated by first vector subtracting the calibrated output noise of both the filtered gain circuit ($Noise_{GAINSTAGE}$) and the measurement instrument ($Noise_{SCOPE}$) yielding the gained attenuator noise ($Noise_{ATTENUATOR\_GAIN}$). The final attenuator circuit noise can then be obtained by dividing by the 101 V/V gain of the filtered gain circuit. A final conversion into V_{RMS} may or may not be required depending on the output of the instrument. An example of these calculations is shown for the oscilloscope measurements in the following equations:

$$Noise_{SCOPE} = 0.26\,mVpp \tag{12}$$

$$Noise_{GAINSTAGE} = 5.6\,mVpp \tag{13}$$

$$Noise_{TOTAL} = 6\,mVpp \tag{14}$$

$$Noise_{ATTENUATOR\_GAIN} = \sqrt{Noise_{TOTAL}^{\ 2} - Noise_{GAINSTAGE}^{\ 2} - Noise_{SCOPE}^{\ 2}} = 2.138\,mVpp \tag{15}$$

$$Noise_{ATTENUATOR} = \frac{Noise_{ATTEND\_GAN}}{101V/V} = 21.17\,\mu Vpp \tag{16}$$

$$Noise_{ATTENUATOR}(V_{RMS}) = \frac{Noise_{ATTENUATOR}}{6} = 3.529\,\mu Vrms \tag{17}$$

The output noise was measured using a few different instruments to ensure correlation between measurement methods. Measurements made with the spectrum analyzer were converted from a spectral density (nV/√Hz) to µVrms based on the bandwidth of the measurement (BW) and the correction factor (K_n) based on the order of the filter used. For a 1st order low-pass filter, K_n is equal to 1.57.

$$Noise_{VRMS} = Noise_{nV/\sqrt{Hz}} \times \sqrt{BW * 1.57} \quad (18)$$

Table 6: Measured Noise Result Summary

	10 MHz BW
Spectrum Analyzer (µVrms)	3.521
Oscilloscope (µVrms)	3.529

6.8 Measured Result Summary

The measured results are compared against the design goals in Table 7.

Table 7: Measured Result Summary

	Goals	Simulated	Measured
Offset (mV)	1	0.0623	0.11388
10 Hz Gain Error (dB)	0.5	0.122	0.11
1 kHz Gain Error (dB)	0.1	0.0061	0.01
100 KHz Gain Error (dB)	0.5	0.5876	0.05
Output Noise 10 MHz (µVrms)	5	2.327	3.521
Quiescent Current (mA)	5	3.797	3.844

7 Modifications

Almost any amplifier can perform this application but certain amplifiers are better for high performance designs. High performance versions of this circuit will benefit from an amplifier with low-noise, low THD, high A_{OL}, wide bandwidths, and high supply voltages. Other +36 V amplifiers for this application are the OPA627, OPA827, OPA211, OPA140, OPA134. Single-supply versions of this circuit could be created with the OPA320, OPA350, OPA365, or OPA376 devices.

Table 8: Alternate +36V Amplifiers

Amplifier	Max Offset Voltage (µV)	Noise at 1 kHz (nV/√Hz)	THD at 1 kHz (%)	A_{OL} (dB)	Bandwidth (MHz)	Quiescent Current (mA)
OPA1611	500	1.1	0.000015	130	40	3.6
OPA134	2	8	0.00008	120	8	4
OPA140	120	5.1	0.00005	126	11	1.8
OPA211	50	1.1	0.000015	130	45	3.6
OPA627	100	5.2	0.00003	120	16	7
OPA827	150	4	0.00004	126	22	4.8

Table 9: Alternate Op Amps

Amplifier	Max Offset Voltage (µV)	Noise	THD	A_{OL}	Bandwidth (MHz)	Quiescent Current (mA)
OPA320	150	8.5	0.0005	130	20	1.6
OPA350	500	17	0.0006	122	38	5.2
OPA376	25	7.5	0.00027	134	5.5	0.76
OPA365	200	12	0.0004	120	50	4.6

8 About the Authors

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

Ting Ye is a field application engineer based in Taipei who supports industrial and precision customers. She performed a six month rotation working with the Precision Linear group where she supported op amp and current loop products for industrial applications.

9 Acknowledgements & References

1. *Green, Tim, Operational Amplifier Stability Parts 1-11, November 2008, Available: http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712*

2. *Kay, A., Operational Amplifier Noise, Newnes, 2012*

Appendix A.

A.1 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure A.1.

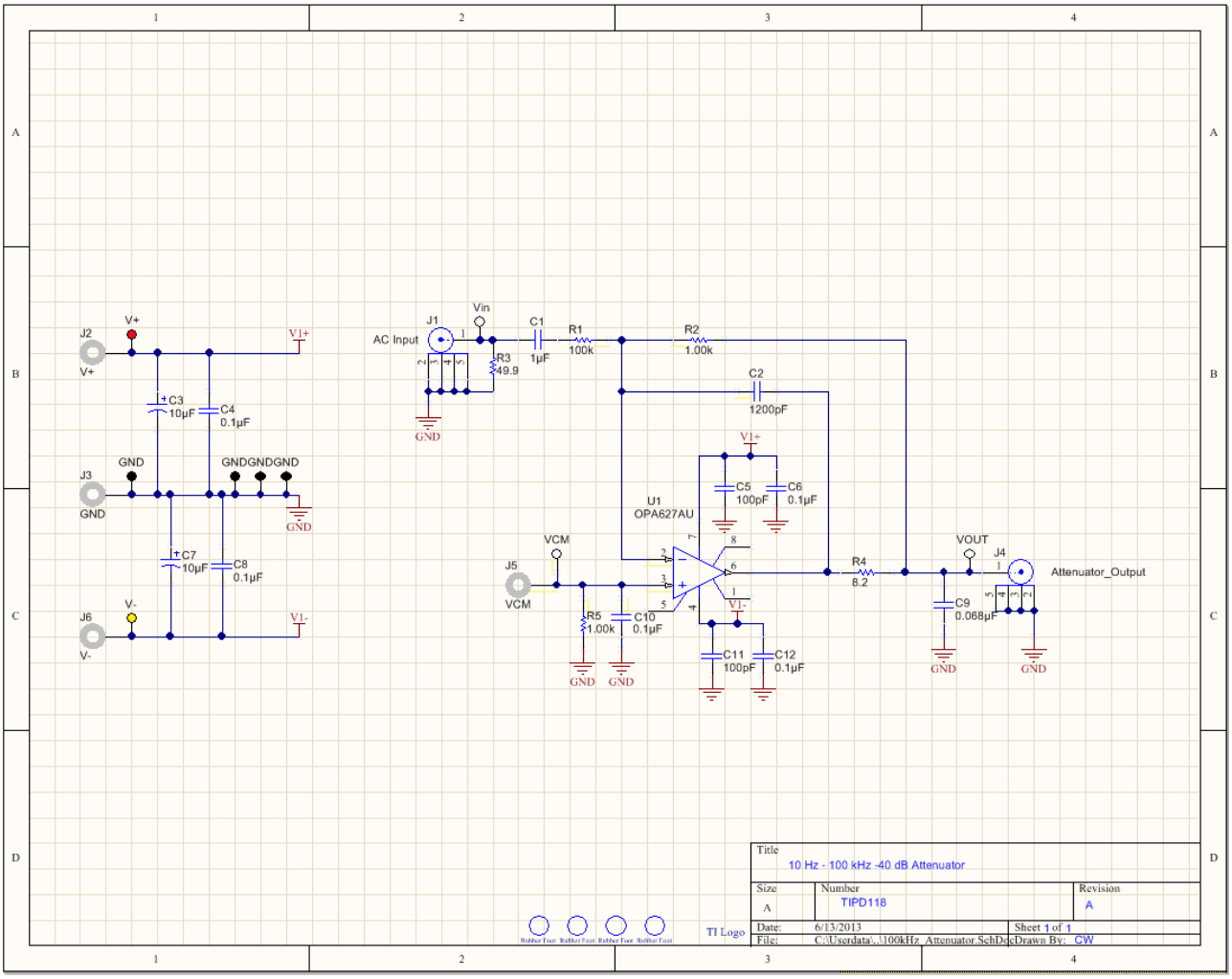

Figure A-1: Electrical Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure A.2.

Line #	Quantity	Designator	Value	Description	Manufacturer	PartNumber	Supplier Part Number 1
1	1	C1	1uF	CAP, CERM, 1uF, 100V, +/-10%, X7R, 1206	MuRata	GRM31CR72A105KA01L	490-3909-1-ND
2	1	C2	1500pF	CAP, CERM, 1500pF, 100V, +/-5%, C0G/NP0, 0805	MuRata	GRM2165C2A152JA01D	GRM2165C2A152JA01D-ND
3	2	C3, C7	10uF	CAP, TANT, 10uF, 50V, +/-10%, 0.4 ohm, 7343-43 SMD	AVX	TPSE106K050R0400	478-3361-1-ND
4	4	C4, C6, C8, C12	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0805	MuRata	GRM21BR71H104KA01L	490-1666-1-ND
5	2	C5, C11	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0805	MuRata	GRM2165C1H101JA01D	490-1615-1-ND
6	1	C9	0.068uF	CAP, CERM, 0.068uF, 50V, +/-5%, C0G/NP0, 1206	MuRata	GRM31C5C1H683JA01L	490-3360-1-ND
7	1	C10	0.1uF	CAP CER 0.1UF 50V 5% NP0 1206	TDK Corporation	CGJ5L2C0G1H104J160AA	445-8219-1-ND
8	2	J1, J4		Connector, TH, SMA	Emerson Network Power	142-0701-201	J500-ND
9	4	J2,J3,J5,J6		Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	575-4K-ND
10	1	R1	100k	RES, 100k ohm, 0.1%, 0.125W, 0805	Susumu Co Ltd	RG2012P-104-B-T5	RG20P100KBCT-ND
11	1	R2	1.00k	RES, 1.00k ohm, 0.1%, 0.125W, 0805	Susumu Co Ltd	RG2012P-102-B-T5	RG20P1.0KBCT-ND
12	1	R3	49.9	RES 49.9 OHM 0.20W 0.1% 0805	Vishay Thin Film	PAT0805E49R9BST1	PAT49.9BCT-ND
13	1	R4	8.2	RES 8.2 OHM 1/10W 1% 0805 SMD	Yageo	RJ0805FRE078R2L	311-8.2VCT-ND
14	1	R5	1.00k	RES, 1.00k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW08051K00FKEA	541-1.00KCCT-ND
15	3	TP1,TP7,TP8	White	Test Point, TH, Miniature, White	Keystone	5002	5002K-ND
16	1	TP2	Red	Test Point, TH, Miniature, Red	Keystone	5000	5000K-ND
17	4	TP3, TP4, TP5, TP6	Black	Test Point, TH, Miniature, Black	Keystone	5001	5001K-ND
18	1	TP9	Yellow	Test Point, TH, Miniature, Yellow	Keystone	5004	5004K-ND
19	1	U1		IC OPAMP AUDIO 40MHZ SGL 8SOIC	Texas Instruments	OPA1611AID	296-24958-5-ND

Figure A-2: Bill of Materials

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