ADCxxQJxx00 Evaluation Module

User's Guide

Literature Number: SLAU808
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This user’s guide describes the characteristics, operation, and use of the ADCxxQJxx00 evaluation module (EVM). This user's guide discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the ADCxxQJxx00EVM. In the following sections of this document, the ADCxxQJxx00 evaluation board is referred to as the *EVM* and the ADCxxQJxx00 device is referred to as the *ADC* device. This document also includes an electrical schematic, printed circuit board (PCB) layout drawings, and a parts list for the EVM.

Trademarks

Introduction

The ADCxxQJxx00EVM is an evaluation board used to evaluate the ADCxxQJxx00 family (ADC09QJ1300 and ADC12QJ1600) of analog-to-digital converters (ADC) from Texas Instruments. The ADCxxQJxx00 is a quad channel, 9 or 12-bit ADC, capable of operating at sampling rates up to 1.6 Giga-samples per second (GSPS) with four analog input channels. The ADCxxQJxx00EVM output data is transmitted over a standard JESD204C high-speed serial interface. This evaluation board also includes the following important features:

- Transformer-coupled signal input network allowing a single-ended signal source from 10 MHz to 4 GHz. Option to bypass the transformer and use DC coupled differential inputs
- The LMK04828 onboard system clock generator generates ADC sampling clock, SYSREF and FPGA reference clocks for the high-speed serial interface
- Transformer-coupled clock input network to test the ADC performance with an external low-noise clock source
- LM95233 temperature sensor
- High-speed serial data output over a High Pin Count FMC interface connector

NOTE: To improve signal routing quality, serial lanes are mapped differently with respect to the standard FMC VITA-57 signal mapping. Signal mapping is shown in Table C-1).

- Device register programming through USB connector and FTDI USB-to-SPI bus translator

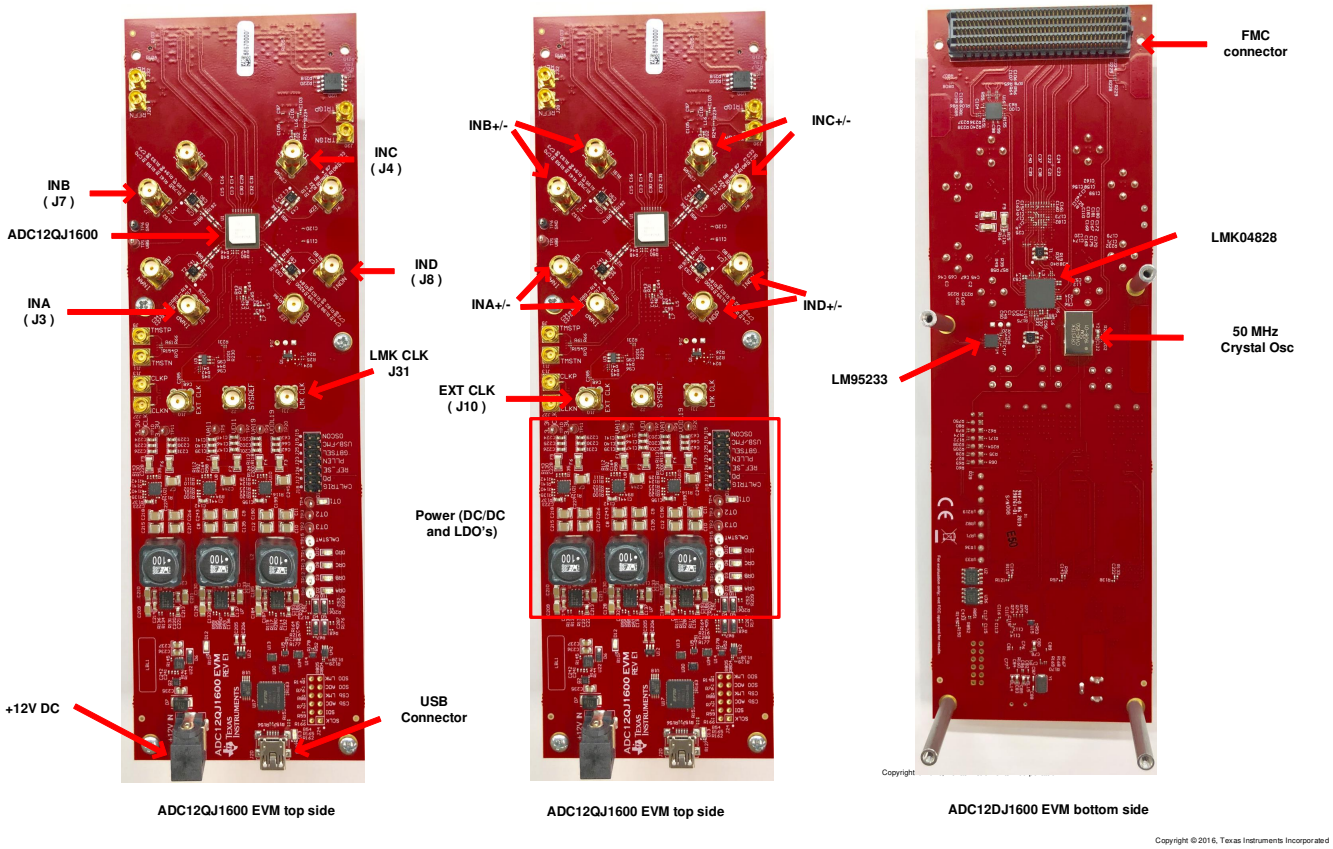

Figure 1-1. EVM Orientation

The digital data from the ADCxxQJxx00EVM board is quickly and easily captured with the TSW14J57EVM data capture boards.

NOTE: The TSW14J57EVM cannot be used for JMODES (4 to 8, 14 and 15) that use 64b/66b encoding, or SERDES lane rate above 15 Gbps.

The TSW14J57EVM captures the high-speed serial data, decodes the data, stores the data in memory, and then uploads it to a connected PC through a USB interface for analysis. The High-Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.

With proper hardware selection in the HSDCpro software, the TSW14J57 device is automatically configured to support a wide range of operating speeds of the ADCxxQJxx00EVM, but the device may not cover the full operating range of the ADC device. Serial data rates of 15 Gbps down to 1 Gbps are supported.

Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the ADC device.

2.1 Evaluation Board Feature Identification Summary

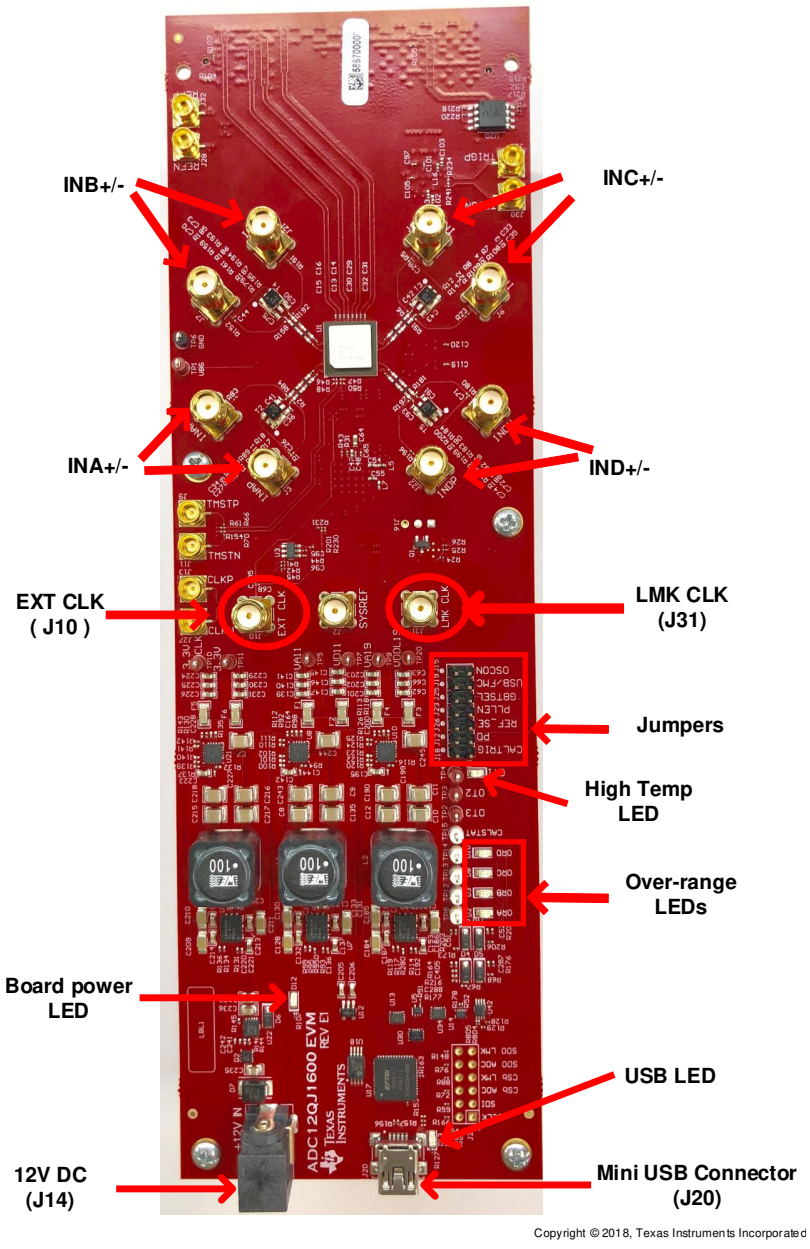

Figure 2-1. EVM Feature Locations

2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- Mini-USB cable
- Power cable

The following equipment is **not** included in the EVM evaluation kit, but is required for evaluation of this product:

- TSW14J57EVM data capture board and related items
- PC computer running Microsoft® Windows® 7, or 10
- One low-noise signal generator for DEVCLK (Sampling clock) . TI recommends the following generators:
  - Rohde & Schwarz® SMA100B
  - Rohde & Schwarz® SMA100A
- One low-noise signal generator for analog input. TI recommends the following generators:
  - Rohde & Schwarz® SMA100B
  - Rohde & Schwarz® SMA100A
- Bandpass filter for analog input signal (97 MHz or desired frequency). The following filters are recommended:
  - Bandpass filter, greater than or equal to 60-dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5-dB insertion loss
  - Trilithic™ 5VH-series tunable BPF
  - K&L Microwave™ BT-series tunable BPF
  - TTE KC6 or KC7-series fixed BPF
- Signal-path cables, SMA or BNC (or both SMA and BNC)

By default, the ADCxxQJxx00EVM is configured to use LMK04828 in distribution mode to provide the sampling clock to the ADC (In the GUI this option is labeled as "Ext CLK from LMK to ADC"). A few small board modifications allow the direct external sampling clock option(In the GUI this option is labeled as "Ext Direct CLK to ADC"). If direct external clocking option is used, the following additional equipment is recommended.

- Signal generators for providing the FPGA reference clock . TI recommends similar models to the DEVCLK clock source.

NOTE: The frequency of clock source used to drive the FPGA reference clock (labeled DEV CLK J31) is displayed on the first page of the GUI under FPGA Reference Clock. The FPGA reference clock frequency is calculated by the GUI using JMODE and the sampling frequency (Fs) entered by the user. If "Ext Direct CLK to ADC" the FPGA reference clock generator and device clock generator must be frequency-locked using a common 10-MHz reference.

Setup Procedure

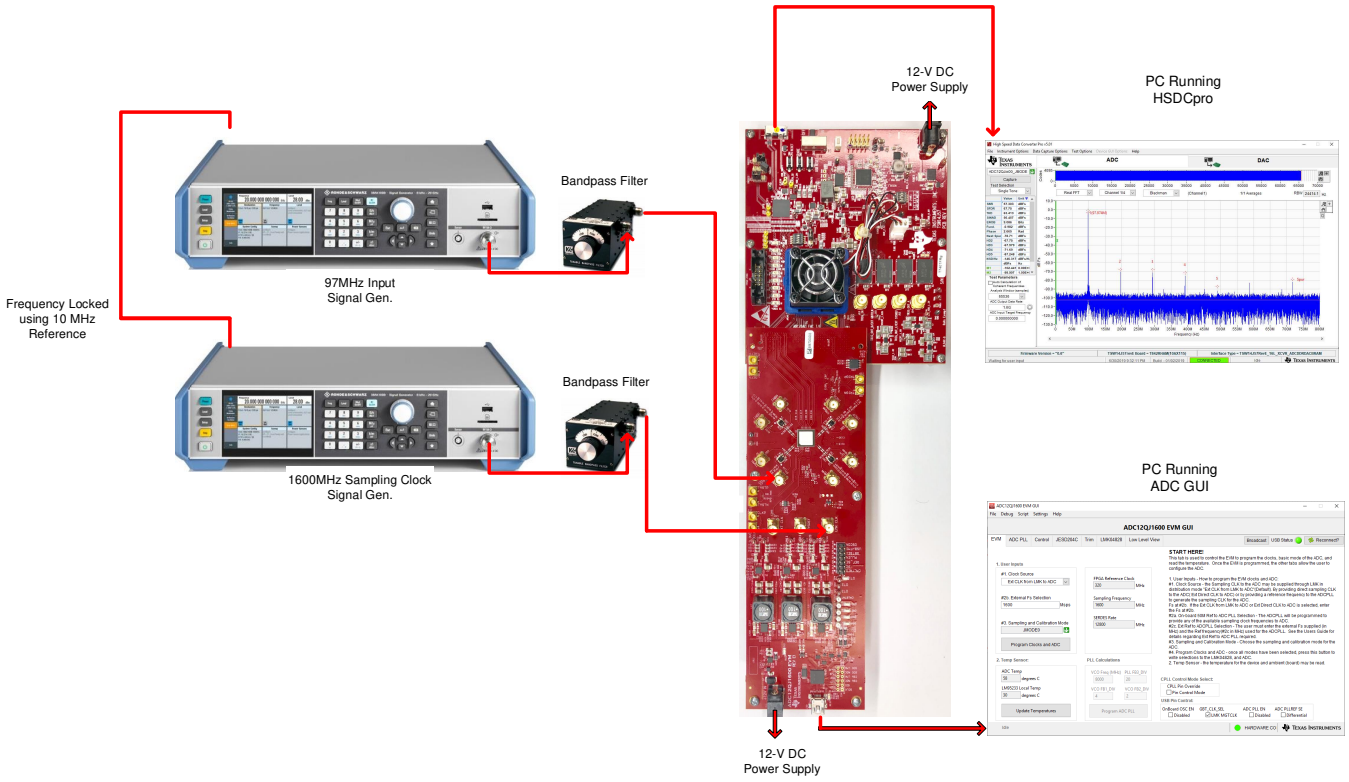

Figure 3-1. EVM Test Setup

NOTE: The HSDC Pro software must be installed before connecting the TSW14J57EVM to the PC for the first time.

3.1 Install the High Speed Data Converter (HSDC) Pro Software

1. Download the most recent version of the HSDC Pro software from www.ti.com/tool/dataconverterpro-sw. Follow the installation instructions to install the software.
2. Download and copy all the INI files required to the HSDCpro directory from ADC12QJ1600EVM webpage. The INI files should be copied to following location C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J57revE Details\ADC files

3.2 Install the Configuration GUI Software

1. Download the ADC12QJ1600EVM configuration GUI software from ADC12QJ1600EVM webpage.
2. Extract files from the .zip file.
3. Run the executable file (setup.exe), and follow the instructions. Make sure to install and run the software as an administrator.

3.3 Connect the ADCxxQxx00EVM and TSW14J57EVM

With the power off, connect the ADCxxQJxx00EVM to the TSW14J57EVM through the FMC connector as shown in Figure 3-1. Ensure that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards (Power Off)

1. Confirm that the power switch on the TSW14J57EVM is in the off position. Connect the power cable to a 12-V DC (minimum 3 A) power supply. Ensure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the EVM power connector.
2. Confirm that the power switch for the ADCxxQJxx00EVM's power supply is in the off position. Connect the power cable to a 12-V DC (minimum 1.5 A) power supply. Ensure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12 V. Connect the power cable to the EVM power connector.

CAUTION

Ensure the power connections to the EVMs are the correct polarity. Failure to do so may result in immediate damage.

Leave the power switches in the off position until directed later.

3.5 Connect the Signal Generators to the EVM (RF Outputs Disabled Until Directed)

Connect a signal generator to the INAP (J3) input of the ADCxxQJxx00EVM through a bandpass filter and at the SMA connector. This must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal from the generator. Configure the signal generator for 97 MHz, 6 dBm.

When LMK04828 is used for clocking the ADC(Default)

a. Connect a signal generator to the LMK CLK (J31) input of the EVM through a bandpass filter. This signal generator must be a low-noise signal generator. TI recommends a Trilithic-tunable bandpass filter to filter the signal coming from the generator. Configure the signal generator for the desired clock frequency in the range of 0.5 to 1.6 GHz. For best performance when using an RF signal generator, the power input to the LMK CLK SMA connector must be 5 dBm (1.125 Vpp into 50 Ω). The signal generator must increase above 5 dB by an amount equal to any additional attenuation in the clock signal path, such as the insertion loss of the bandpass filter. For example, if the filter insertion loss is 2 dB, the signal generator must be set to 5 dBm + 2 dB = 7 dBm.

b. Skip this step for default("Ext CLK from LMK to ADC") evm setup. This step should only be followed when *Ext Direct CLK to ADC* mode is desired. The ADC sampling clock of desired frequency(1600 MHz) is applied to the SMA connector EXT CLK(J10) and the FPGA reference signal input for the EVM at is applied at LMC CLK(J31). Configure the signal generator for the FPGA reference desired (320MHz) clock frequency. Set the output power to approximately 6–9 dBm.

NOTE:

1. The FPGA Reference clock frequency can be obtained from the ADCxxQJxx00EVM GUI. Once the ADCxxQJxx00EVM GUI is configured to the desired JMODE mode and clock rate. The Reference Clock frequency required by the EVM is displayed on first page of the GUI shown with red square in Figure 3-2
2. Ensure that the DEVCLK and FPGA Reference clock sources are frequency-locked using a common 10-MHz reference to ensure functionality. Frequency locking the input signal generator to the other generators can also be done if coherent sampling is desired.
3. Do not turn on the RF output of any signal generator at this time.

3.6 Turn On the TSW14J57EVM Power and Connect to the PC

1. Turn on the power switch of the TSW14J57EVM.
2. Connect the USB cable from the PC to the TSW14J57EVM.
3. If this is the first time connecting the TSW14J57EVM to the PC, follow the on-screen instructions to automatically install the device drivers. See the TSW14J57EVM user's guide for specific instructions.

3.7 Turn On the ADCxxQJxx00EVM Power Supplies and Connect to the PC

1. Turn on the 12-V power supply to power up the EVM.
2. Connect the EVM to the PC with the mini-USB cable.

3.8 Turn On the Signal Generator RF Outputs

Turn on the RF signal output of the signal generator connected to INAP and sampling clock(LMK CLK). If direct external sampling clocking is used, turn on the RF signal outputs connected to EXT CLK(Sampling frequency) and LMK CLK(set to the FPGA reference frequency shown in ADC GUI.)

3.9 Open the ADCxxQJxx00EVM GUI and Program the ADC and Clocks

The Device Configuration GUI is installed separately from the HSDC Pro installation and is a stand-alone GUI.

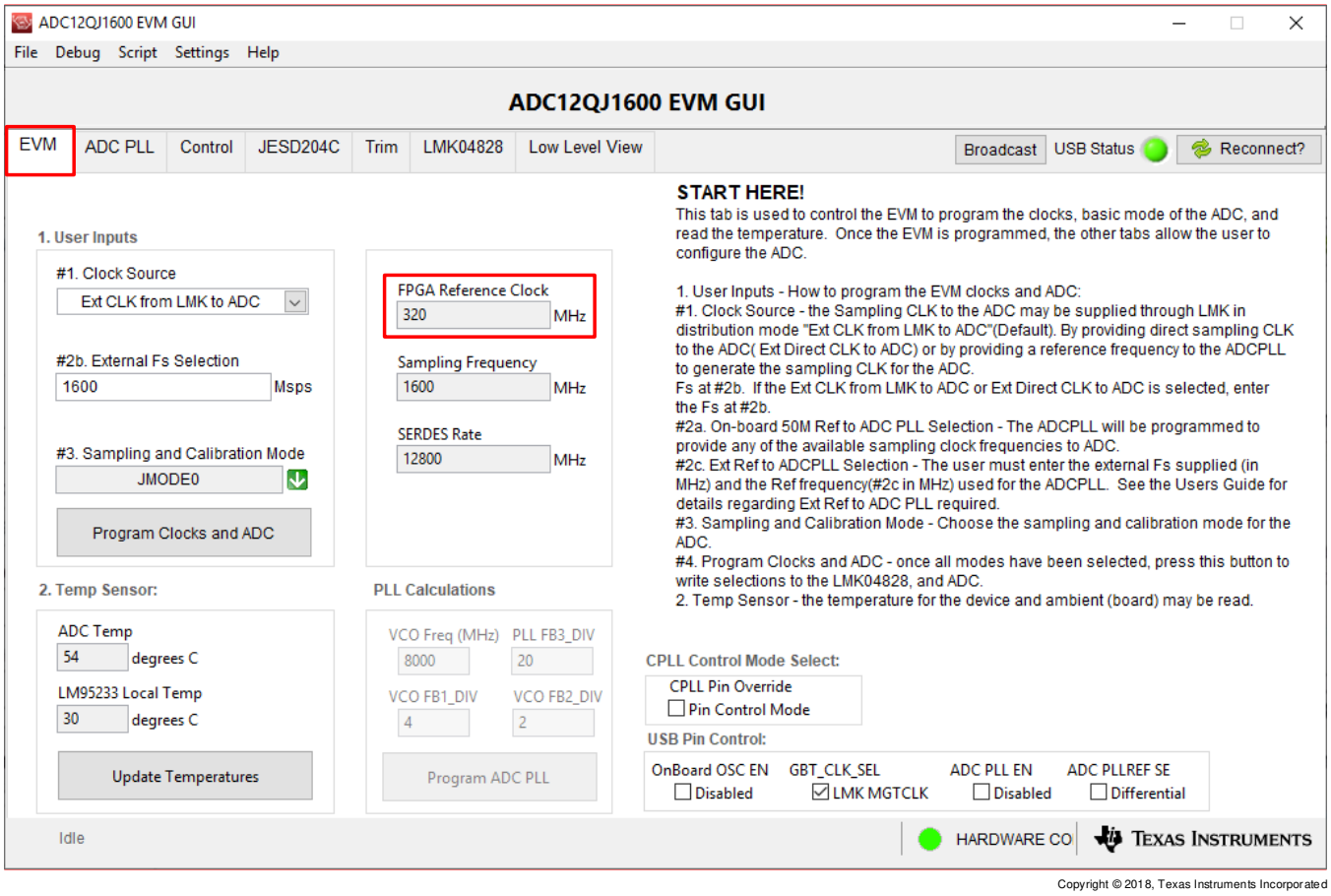

Figure 3-2. Configuration GUI EVM Tab

Figure 3-2 and Figure 3-3 show the GUI open to the *EVM* tab and *Control* tab respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has two configurable devices, namely the ADCxxQJxx00 and LMK04828. **The register map for each device is provided in the device data sheet**, LMK0482xB Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner w/ Dual Loop PLLs

1. Launch the ADCxxQJxx00EVM GUI (run as an administrator). The GUI will launch and display the EVM tab.
2. Select the "Ext CLK from LMK to ADC" as the clock source.
3. Enter Fs = 1600 MHz MSPS as the external Fs selection Or (1300 MHz if ADC09QJ1300EVM is used)
4. Select JMODE0 for the sampling and Calibration mode.
5. Click *Program Clocks and ADC* (Note: This action overwrites any previous device register settings.)

3.10 Calibrate the ADC Device on the EVM

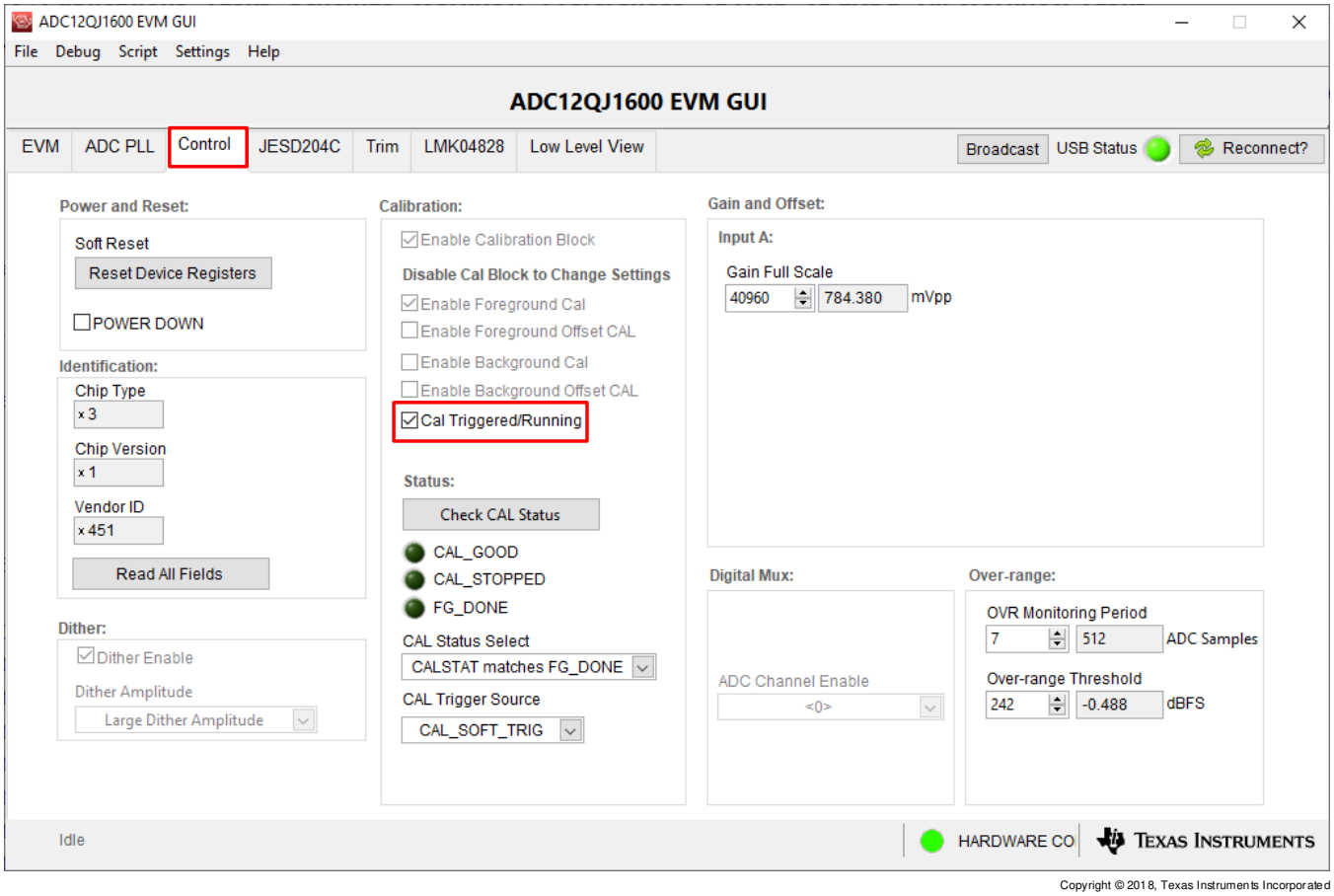

Figure 3-3. Configuration GUI ADC Control

1. With the EVM GUI open on the PC, navigate to the *Control* tab.
2. To calibrate the ADC, click *Cal Triggered/Running* once, then click it again. This stops and re-starts the Calibration engine.

NOTE: This calibrate button executes a calibration sequence that is required for full performance. This calibration is performed automatically during the Section 3.9 step but must be performed again, any time the sampling rate changes, after significant temperature change of the ADC, or after exiting the power-down mode. See the ADCxxQJxx00 device data sheet, (SBAS960) for details regarding the necessary calibration sequence.

3. To enable background calibration, use the following steps:
   - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to stop the JESD204C block.
   - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
   - Click on *Enable Background Cal*.
   - If background offset calibration is desired also, click on *Enable Background Offset Cal*.
   - Click on *Enable Calibration Block* to re-enable the calibration subsystem
   - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to re-start the JESD204C block.
   - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.
4. To disable background calibration, use the following steps:
   - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to stop the JESD204C block.
   - Navigate back to the *Control* tab and click on *Enable Calibration Block* to disable calibration and allow setting changes.
   - If background offset calibration was enabled, click on *Enable Background Offset Cal* to disable the feature.
   - Click on *Enable Background Cal* to disable the feature.
   - Click on *Enable Calibration Block* to re-enable the calibration subsystem.
   - Navigate to the *JESD204C* tab and click on *JESD Block Enable* to re-start the JESD204C block.
   - Navigate back to the *Control* tab and click the *Cal Triggered/Running* button once, then click it again. This restarts the Calibration engine.

3.11 Open the HSDCpro Software and Load the FPGA Image to the TSW14J57EVM

1. Launch the HSDC Pro software (run as an administrator).
2. Click *OK* to confirm the serial number of the TSW14J57EVM device. If multiple TSWxxxxx boards are connected, select the model and serial number for the one connected to the ADCxxQJxx00EVM.
3. Select the ADC12QJxx00_JMODE0 device from the ADC select drop-down in the top left corner.
4. When prompted, click *Yes* to update the firmware.

NOTE: If the user configures the EVM with options other than the default register values, different instructions may be required for selecting the device in HSDC Pro. See Appendix B for more details.

5. Enter the ADC Output Data Rate ($f_{(SAMPLE)}$) as "1600M" or the desired output sample rate. This number must be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

3.12 Capture Data Using the HSDC Pro Software

The following steps show how to capture data using the HSDC Pro software (see Figure 3-4):

1. Select the test to perform.
2. Select the data view.
3. Select the channel to view.
4. Click the capture button to capture new data.

Additional tips:

- Use the *Notch Frequency Bins* from the *Test Options* file menu to remove bins around DC (eliminate DC noise and offset) or the fundamental (eliminate phase noise from signal generators).
- Open the *Capture Option* dialog from the *Data Capture Options* file menu to change the capture depth or to enable Continuous Capture or FFT averaging.
- For analyzing only a portion of the spectrum, use the *Single Tone* test with the *Bandwidth Integration Markers* from the *Test Options* file menu. The *Channel Power* test is also useful.
- For analyzing only a subset of the captured data, set the *Analysis Window (samples)* setting to a value less than the number of total samples captured and move the green or red markers in the small transient data window at the top of the screen to select the data subset of interest.

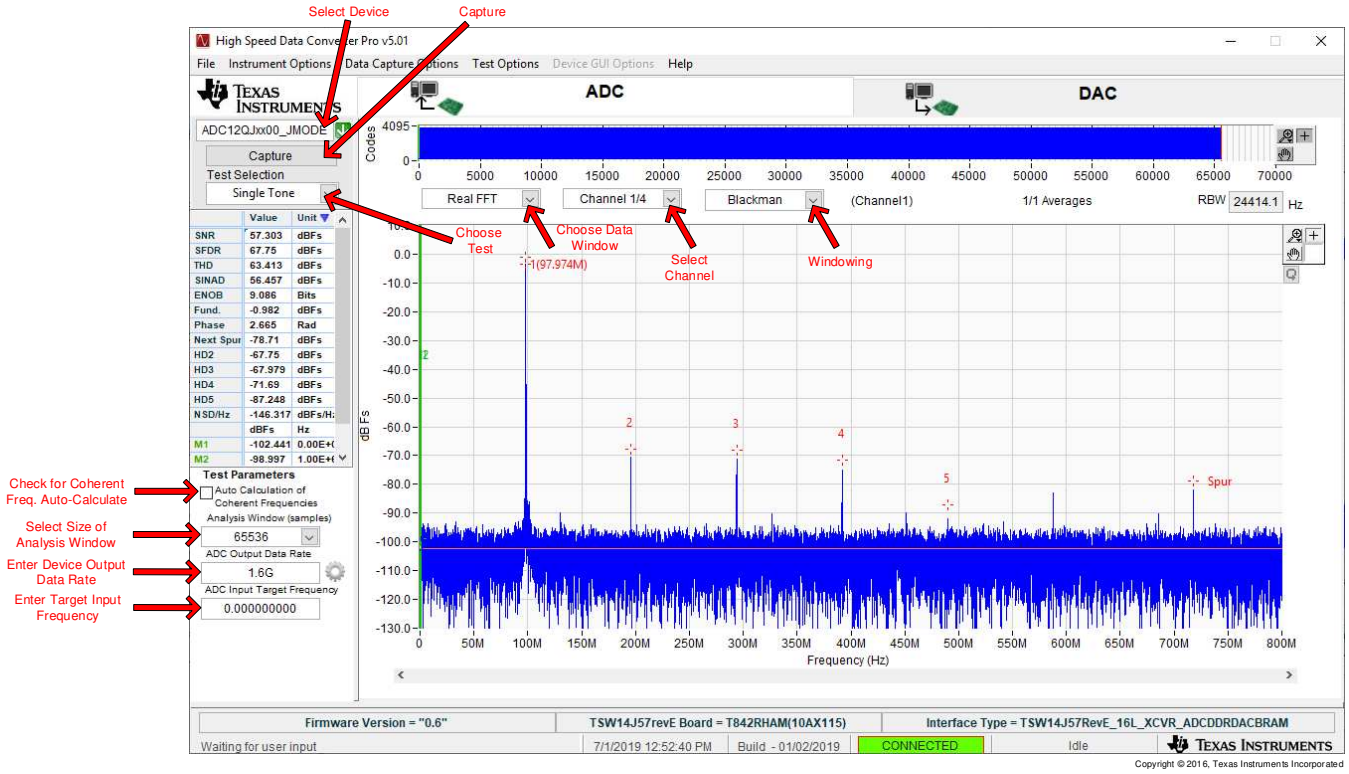

Figure 3-4. High Speed Data Converter Pro (HSDC) GUI

After the capture, If SYSREF leakage is observed in the ADC's spectrum as shown in Figure 3-5, change the continuous SYSREF to pulses by going to the ADCxxQJxx00EVM GUI. The Figure 3-6 shows the steps needed to update the GUI.

1. Goto the LMK04828 tab on ADC12DJxx00 EVM GUI
2. Under the LMK04828 tab goto SYSREF and SYNC tab
3. Under the SYSREF Source, change the "SYSREF Continuous" to "SYSREF Pulses"

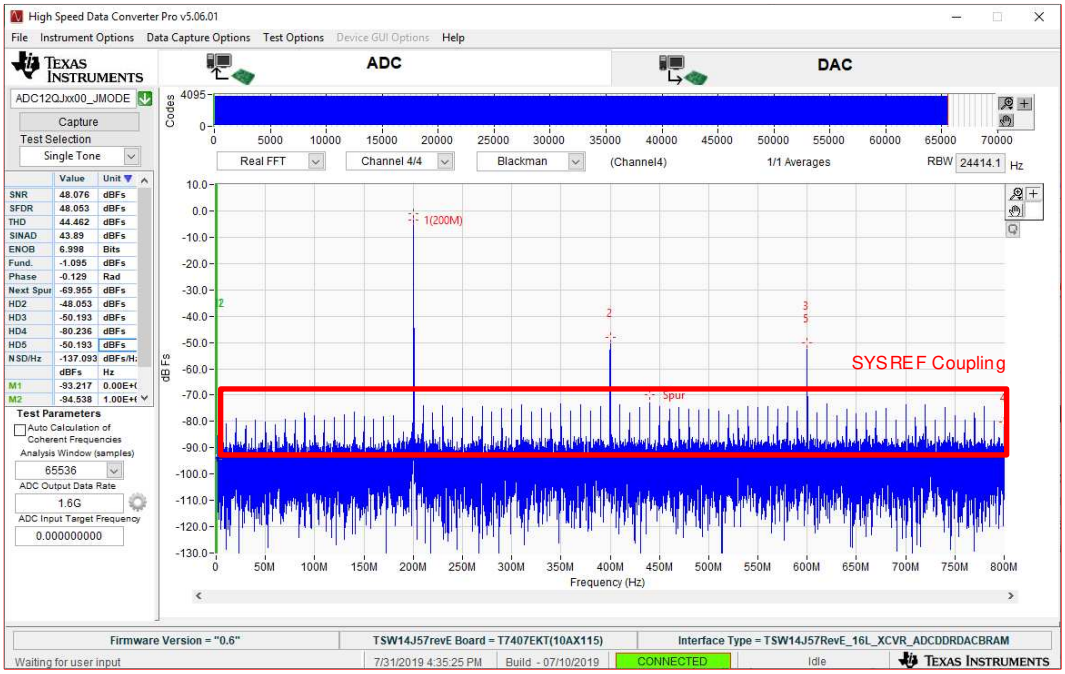

Figure 3-5. SYSREF Coupling

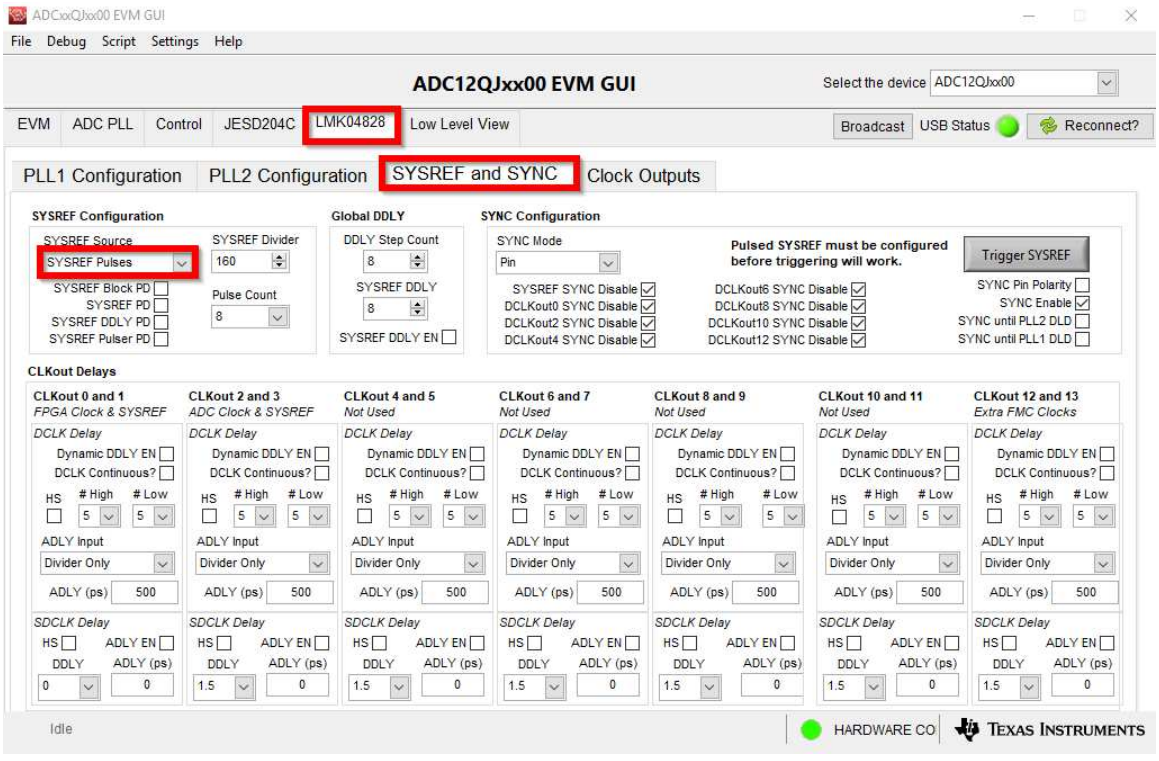

Figure 3-6. SYSREF Pulses

Device Configuration

The ADC device is programmable through the serial programming interface (SPI) bus accessible through the FTDI USB-to-SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

4.1 Supported JESD204C Device Features

The ADC device supports some configuration of the JESD204C interface. Due to limitations in the TSW14J57EVM firmware, all JESD204C link features of the ADC device are not supported. Table 4-1 lists the supported and non-supported features.

Table 4-1. Supported and Non-Supported Features of the JESD204C Device

JESD204C Feature	Supported by ADC Device	Supported by TSW14J57EVM
Number of lanes per link (L)	L = 2, 3, 4, 6, 8 (1)	L = 1, 2, 3, 4, 6, 8 supported
Total number of lanes active	2,,3 4, 6, 8	2, 4, 6, 8, 12, 16
Number of frames per multiframe (K)	K_{min} = 4–256, (1) K_{max} = 256, K_{step} = 4, 16 or 32	Most values of K supported, constrained by requirement that $K \times F = 4^n$
Scrambling	Supported	Supported
Encoding	8B/10B and 64B/66B	8B/10B
Test patterns	PRBS7, PRBS9, PRBS15, PBRS23, PRBS31, Ramp, Transport Layer test, D21.5, K28.5, Repeat ILA, Modified RPAT, Serial Out 0, Serial Out 1, Clock test, ADC Test Pattern (1)	ILA, Ramp, Long/Short Transport
Speed	Lane rates from 0.8 to 17.12 Gbps (1)	Lane rates from 2 to 15 Gbps $f_{(SAMPLE)}$ parameter must be properly set in HSDC Pro GUI.

(1) Dependent on bypass or decimation mode and output rate selection. Always disable the JESD204 block before changing any of the JESD204C settings. Once the settings are changed, re-enable the JESD204 block.

4.2 Tab Organization

Control of the ADC device features are available in the EVM, ADC PLL, Control and JESD204C tabs.

4.3 Low-Level Control

The *Low Level View* tab, illustrated in Figure 4-1, allows configuration of the devices at the bit-field level. At any time, the controls in Table 4-2 can be used to configure or read from the device.

Table 4-2. Low-Level Controls

Control	Description
Register map summary	Displays the devices on the EVM, registers for those devices, and the states of the registers • Clicking on a register field allows individual bit manipulation in the register data cluster • The value column shows the value of the register at the time the GUI was last updated • The 0-7 column shows the value of the register at the time the register was last read
Write register button	Write to the register highlighted in the register map summary with the value in the *Write Data* field
Write all button	Update all registers shown in the register map summary with the values shown in the *Register Map* summary
Read register button	Read from the register highlighted in the *Register Map* summary and display the results in the *Read Data* field Can be used to re-synchronize the GUI with the state of the hardware
Read-all button	Read from all registers in the *Register Map* summary and display the current state of the hardware
Load Configuration button	Load a configuration file from disk and register address/data values in the file
Save Configuration button	Save a configuration file to disk that contains the current state of the configuration registers
Register Data cluster	Manipulate individual accessible bits of the register highlighted in the register map summary
Individual register cluster with read or write register buttons	Perform a generic read or write command to the device shown in the *Block* drop-down box using the address and write data information

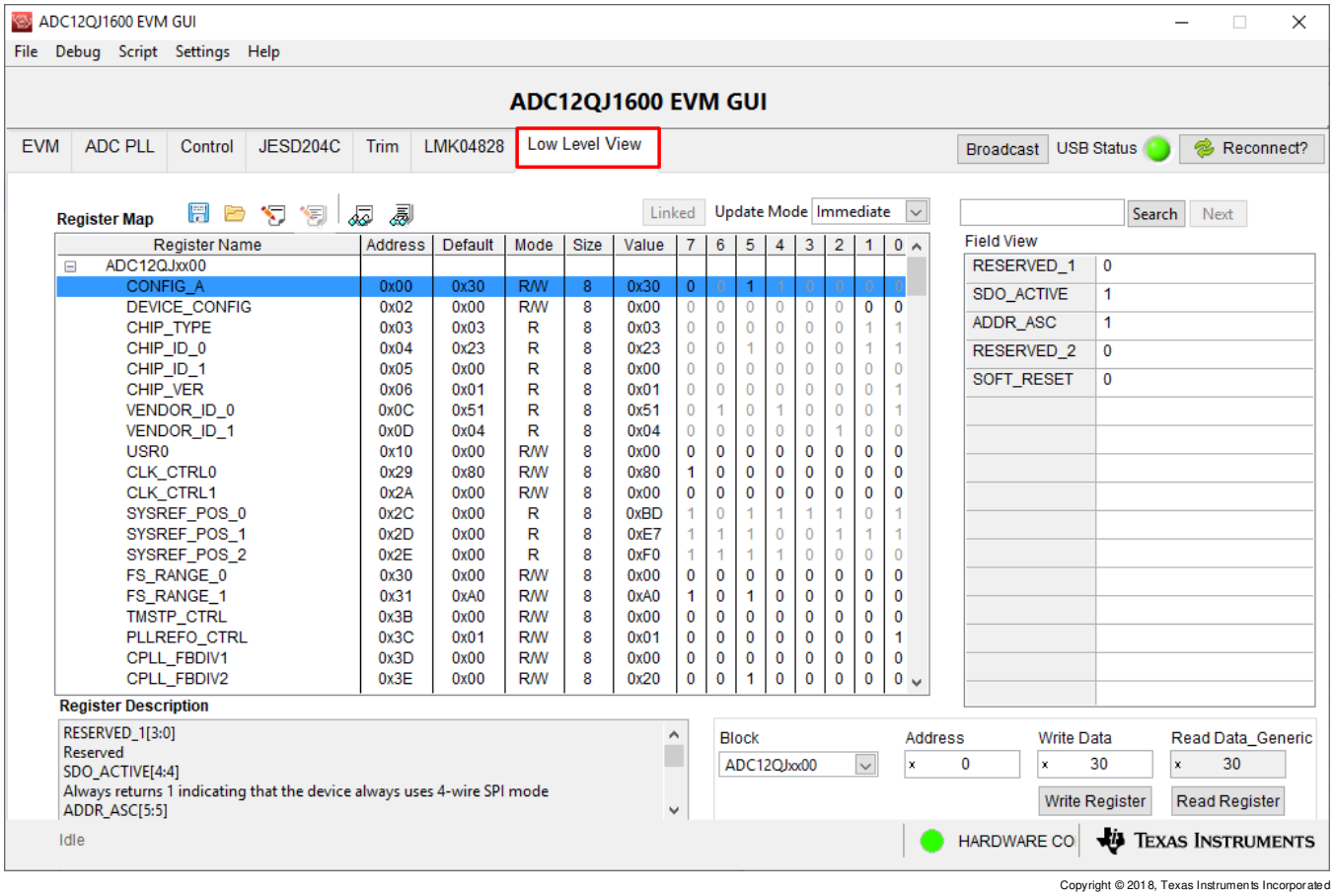

Figure 4-1. Low-Level Register Control Tab

Troubleshooting the ADCxxQJxx00EVM

Table 5-1 lists some troubleshooting procedures.

Table 5-1. Troubleshooting

Issue	Troubleshoot
General problems	• Verify the test setup shown in Figure 3-1, and repeat the setup procedure as described in this document. • Check power supply to EVM and TSW14J57EVM. Verify that the power switch is in the on position. • Check signal and clock connections to EVM. • Visually check the top and bottom sides of the board to verify that nothing looks discolored or damaged. • Ensure the board-to-board FMC connection is secure. • Try pressing the CPU_RESET button on the TSW14J57EVM. Also try clicking *Instrument Options → Reset Board* after changing the ADC configuration. • Try power-cycling the external power supply to the EVM, and reprogram the LMK and ADC devices.
TSW14J57 LEDs are not correct	• Verify the settings of the configuration switches on the TSW14J57EVM. • Verify that the clock going to the CLK input is connected and the appropriate LEDs are blinking. • Verify that the ADC device internal registers are configured properly. • If LEDs are not blinking, reprogram the ADC EVM devices. • Try pressing the CPU_RESET button on the TSW14J57EVM. • Try capturing data in HSDC Pro to force an LED status update
Configuration GUI is not working properly	• Verify that the USB cable is plugged into the EVM and the PC. • Check the computer device manager and verify that a *USB serial device* is recognized when the EVM is connected to the PC. • Verify that the green *USB Status* LED light in the top right corner of the GUI is lit. If it is not lit, click the *Reconnect FTDI* button. • Try restarting the configuration GUI.
Configuration GUI is not able to connect to the EVM	• Use the free FT_PROG software from FTDI chip and verify that the onboard FTDI chip is programmed with the product description *ADC12QJxx00 or ADC09QJxx00 respectively*.
HSDC Pro software is not capturing good data or analysis results are incorrect.	• Verify that the TSW14J57EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDC software. • Check that the proper ADC device mode is selected. The mode should match in HSDC Pro and the ADC GUI. • Check that the analysis parameters are properly configured.
HSDC Pro software gives a time-out error when capturing data	• Try to reprogram the LMK device and reset the JESD204 link. • Verify that the ADC sampling rate is correctly set in the HSDC software. • Try pressing the *CPU_RESET* button on the TSW14J57EVM. Also try clicking *Instrument Options → Reset Board* after changing the ADC configuration. Try to recapture again. • Select *Instrument Options → Download Firmware* and download 'TSW14J57RevE_16L_XCVR_ADCDDRDACBRAM.rbf'. Try to capture again.
Sub-optimal measured performance	• Try clicking *Cal Triggered/Running* button 2× to re-calibrate the ADC in the current operating conditions. It is located on the *Control* tab of the configuration GUI. • Check that the spectral analysis parameters are properly configured. • Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.

References

This section provides references to technical documents and user's guides.

A.1 Technical Reference Documents

- ADC12QJ1600 datasheet
- High-Speed Data Converter Pro GUI User's Guide, also available in the help menu of the software
- LMK04828 data sheet
- FTDI USB to Serial Driver Installation Manual (www.ftdichip.com/Support/Documents/InstallGuides.htm)

A.2 TSW14J57EVM Operation

Refer to the TSW14J57EVM user guide for configuration and status information.

HSDC Pro Settings for Optional ADC Device Configuration

This appendix provides settings for optional ADC device configuration in HSDC Pro.

B.1 Changing the Number of Frames per Multi-Frame (K)

Changing the number of frames per multi-frame output by the JESD204 transmitter (ADC device) is configured using the K parameter(when using modes with 8B/10B encoding) on the *JESD204C* tab in the *Configuration* GUI. This parameter must be matched by the receiving device, and the SYSREF frequency must also be programmed to a compatible frequency. Ensure that the K value complies with the *K Min* and *Step* values for the selected JMODE. Refer to the ADCxxQJxx00 operating modes table in the device datasheet.

B.2 Customizing the EVM for Optional Clocking Support

The ADCxxQJxx00EVM can be clocked using four different methods: Ext CLK from LMK to ADC clocking option, Ext Direct CLK to ADC clocking option, Onboard 50M ref to ADC PLL clocking option and Ext Ref to ADC PLL clocking option.

Ext CLK from LMK to ADC and Ext Direct CLK to ADC clocking options are the only two clocking option which are currently supported by TSW14J57EVM capture solution. The Onboard 50M ref to ADC PLL clocking option and Ext Ref to ADC PLL requires custom firmware and FPGA Evaluation Board & Development kit hardware.

B.2.1 "Ext CLK from LMK to ADC" (Default)

By default, the EVM is configured to use the "Ext CLK from LMK to ADC" clock option. The user provide and external clock signal to LMK04828 at SMA connector J31 (LMK CLK). In this clocking option the LMK04828 is used in clock distribution mode and provides ADC sampling clock, the FPGA reference clock, FPGA SYSREF signal and ADC SYSREF signal. If coherent sampling is desired the ADC analog input signal generator and ADC sampling clock signal generator should be frequency locked to each other. Figure B-1 shows the block diagram of external clocking option:

The EVM can be configured to use Ext CLK from LMK to ADC with the following steps (see Figure B-5):

1. Modify the hardware:
   a. Remove C45, C46, C2 and C3 and populate C67 and C69.

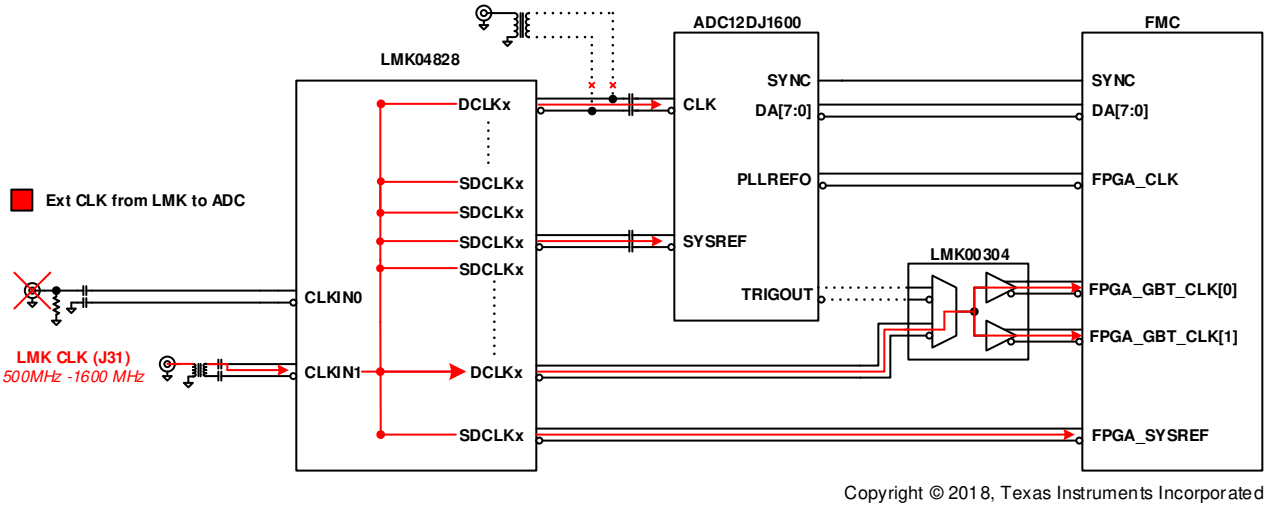

Figure B-1. ADCxxQJxx00EVM Clocking System Block Diagram

B.2.2 "Ext Direct CLK to ADC Clocking Option"

The sampling clock(DEVCLK) for the ADC is provided directly from External signal generator on SMA labeled EXT CLK(J10) . The second signal generator is used to provide the CLK to the LMK04828. The LMK04828 is used in clock distribution mode to provides the FPGA reference clock, FPGA SYSREF signal and ADC SYSREF signal. Ensure that the DEVCLK and FPGA Reference clock sources are frequency-locked using a common 10-MHz reference to ensure functionality. Frequency locking the input signal generator to the other generators can also be done if coherent sampling is desired. Figure B-2 shows the block diagram of Ext Direct CLK to ADC clocking option:

The EVM can be configured to use Ext Direct CLK to ADC clocking option with the following steps Figure B-6:

- Remove C45, C46, C67 and C69 and populate C2 and C3.

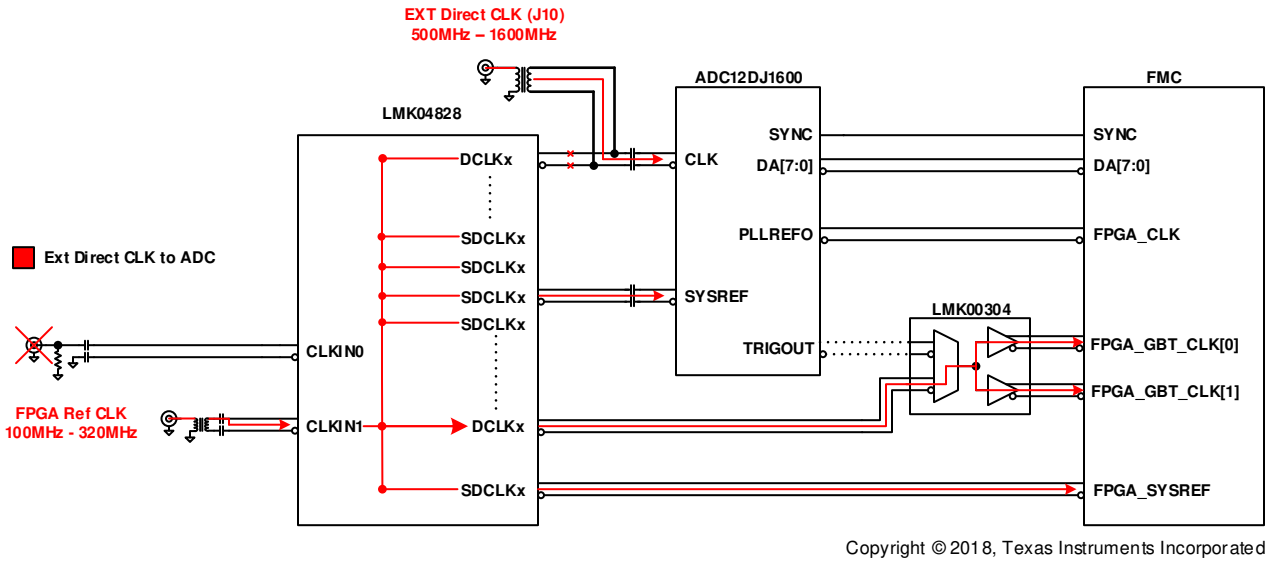

Figure B-2. Ext Direct CLK to ADC System Block Diagram

B.2.3 "Onboard 50M Ref to ADC PLL"

The 50MHz onboard crystal oscillator is use provide reference signal to ADC's single ended clock input. The ADC PLL generate a sampling clock for the ADC from this 50MHz. In this clocking mode ADC also generate the reference clock signal for FPGA. FPGA takes this reference clock and generates the SYSREF signal for the ADC and feed it back to the ADC. Figure B-3 shows the block diagram of Onboard 50M Ref to ADC PLL clocking option:

No hardware change is needed to use this mode. If deterministic latency is desired, the SYSREF signal from FPGA should be routed to the ADC and following changes is required

- Remove C60 and C61 and populate R233 and R235 with 0.1uF caps

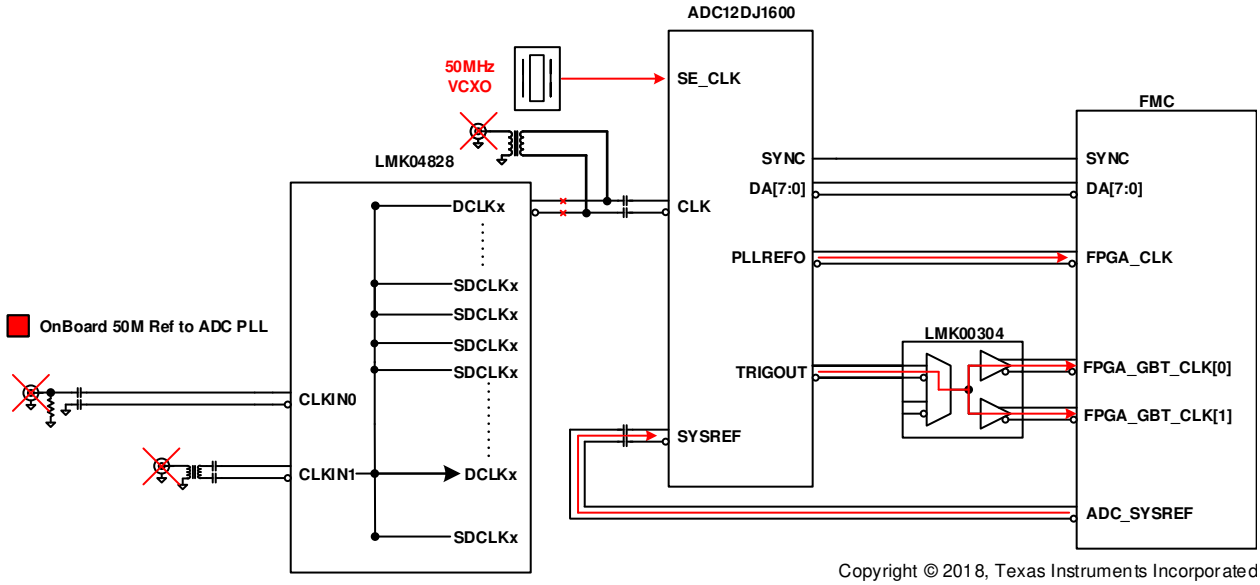

Figure B-3. Onboard 50M Ref to ADC PLL System Block Diagram

B.2.4 "Ext Ref to ADC PLL"

The reference signal for the ADC PLL is provided externally from External signal generator on SMA labeled EXT CLK(J10) . The sampling clock is generate by ADC PLL, from this external provided PLL reference signal. In this clocking mode ADC also generate the reference clock signal for FPGA. FPGA takes this reference clock and generates the SYSREF signal for the ADC and feed it back to the ADC. Figure B-4shows the block diagram of Ext Ref to ADC PLL clocking option:

The EVM can be configured to use Ext Direct CLK to ADC clocking option with the following steps Figure B-6:

- Remove C45, C46, C67 and C69 and populate C2 and C3
- If deterministic latency is desired, the SYSREF signal from FPGA should be routed to the ADC and following changes is required
- Remove C60 and C61 and populate R233 and R235 with 0.1uF caps

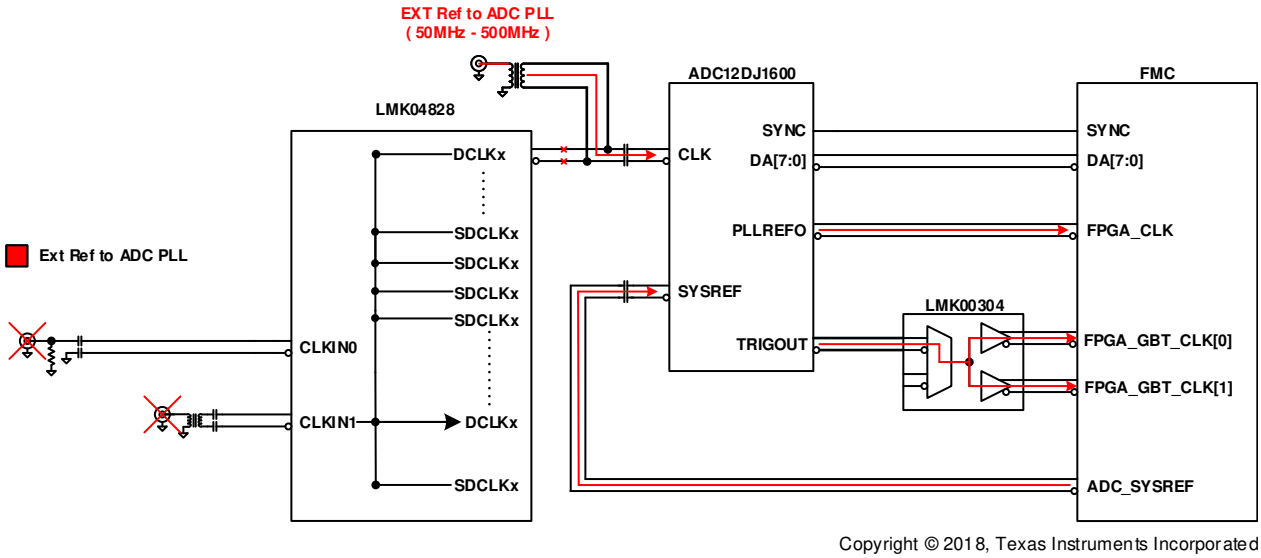

Figure B-4. Ext Ref to ADC PLL System Block Diagram

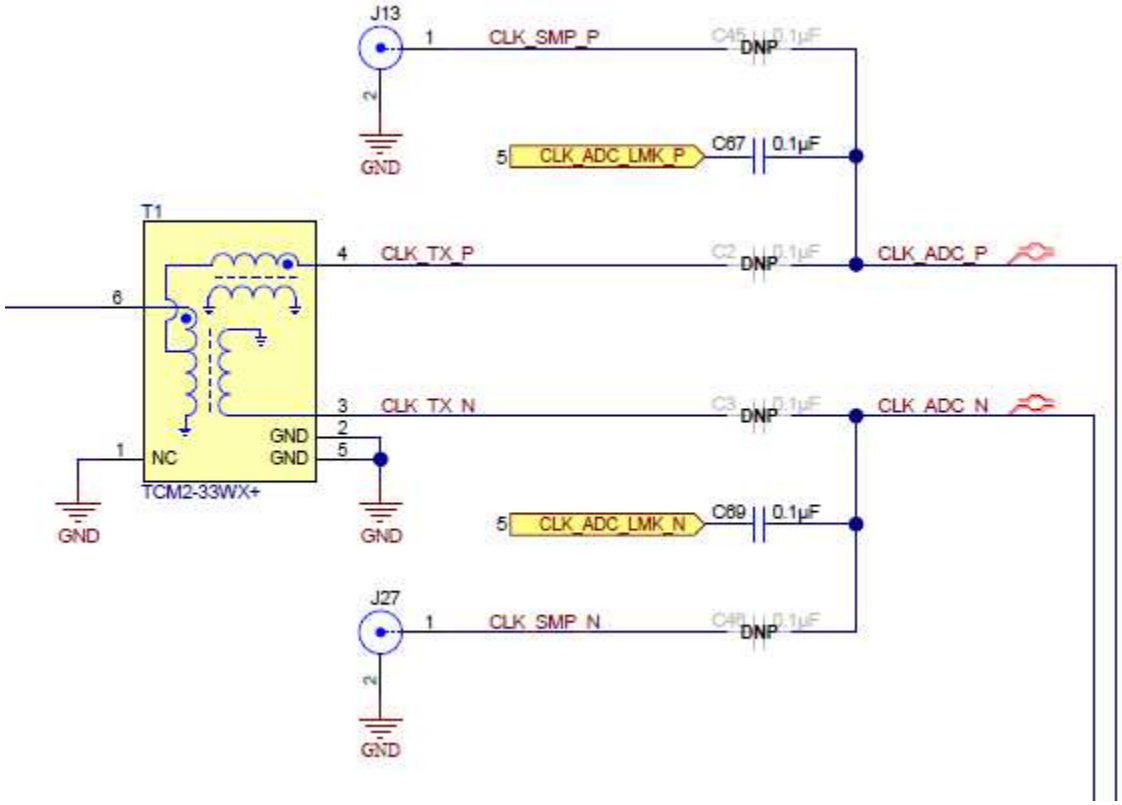

Figure B-5. Ext CLK from LMK to ADC Configuration

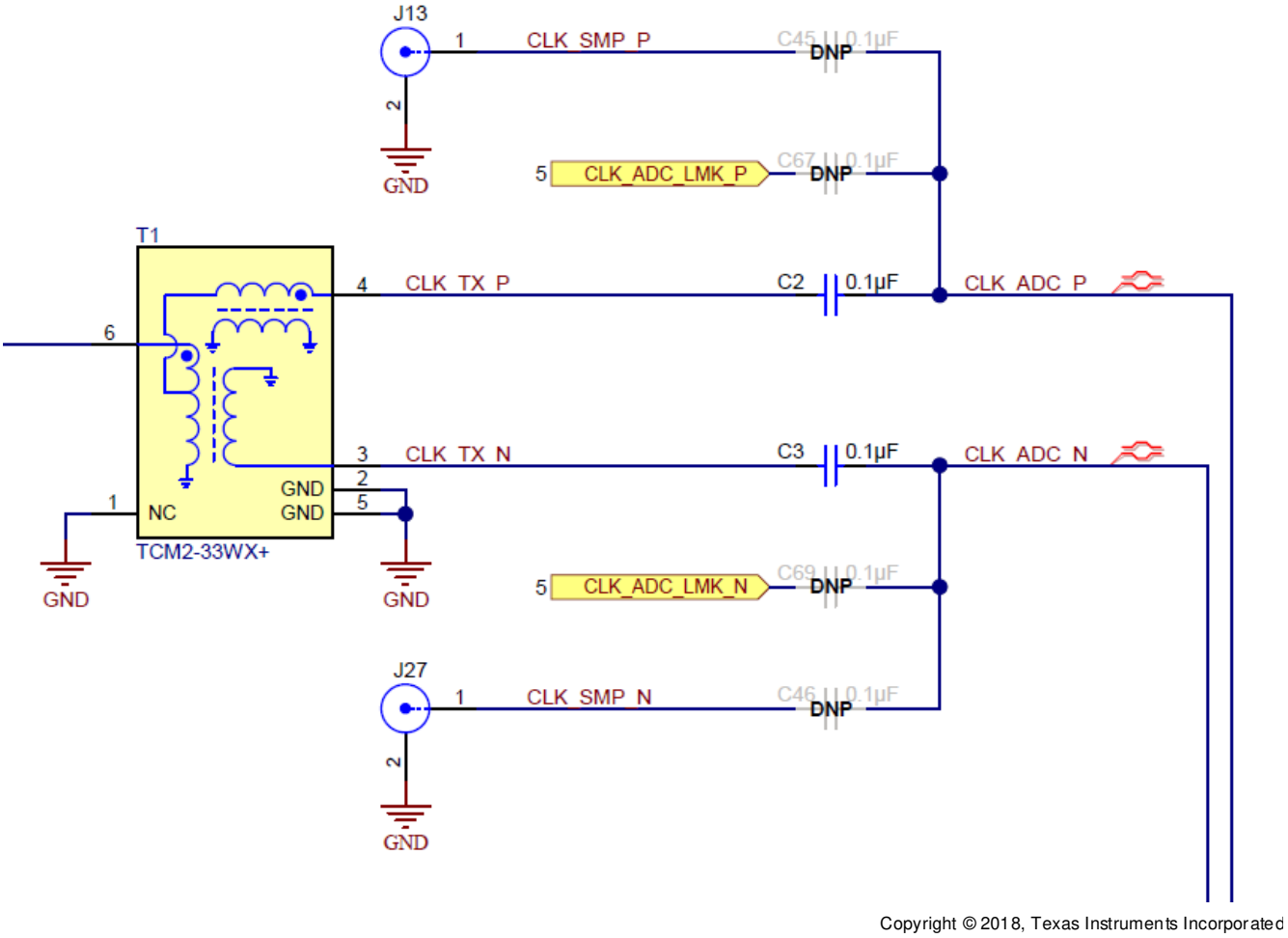

Figure B-6. Ext Direct clock to ADC Configuration

Signal Routing

C.1 Signal Routing

Table C-1 provides the signal routing details for the ADCxxQJxx00EVM.

Table C-1. ADCxxQJxx00EVM Signal Routing

JESD204C Output	LID	FMC Pins
D0	0	A10,A11
D1	1	A6,A7
D2	2	C6,C7
D3	3	A2,A3
D4	4	A18,A19
D5	5	B16,B17
D6	6	A14,A15
D7	7	B12,B13

Analog Inputs

Table D-1 provides the different settings for setting the analog inputs path.

Table D-1. Analog Input Path

Coupling	Input	SMA to Use	C26,C27,C44,C70,C28,C33,C71 and C72	R1,R2,R84,R152,R158,R192, R5,R6,R91 R180, R181, R197
AC (default)	S/E Balun (10MHz to 4GHz)	INAP(J3), INBP(J7), INCN(J4), INDN(J8)	0.1uF	DNI
DC	Differential	INAP(J3), INAN(J5), INBP(J7), INBN(J21),INCP(J6), INCN(J4), INDP(J22), INDN(J8)	DNI	0 Ω

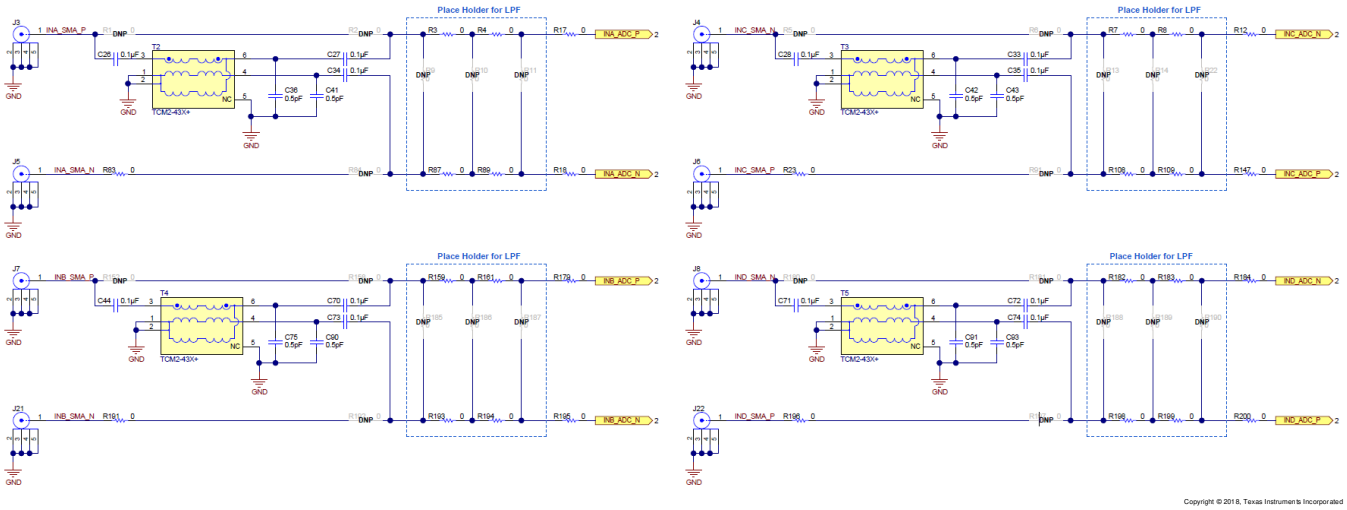

Figure D-1. Analog Input Path

Jumpers and LEDs

E.1 Jumper settings

Table E-1 shows the jumper settings and Table E-2 shows the LED functionality.

Table E-1. Jumper Settings

Label	Description	Function
J12	ADC power down jumper.	Installed: ADC powered down. Uninstalled: ADC powered up(default)
J15	Enable to 50MHz Oscillator.	Installed: Oscillator Enabled(default). Uninstalled: Oscillator disabled
J18	When hardware calibration trigger option is enabled. The ADC's calibration routine is can be enable using external signal	Installed: ADC's calibration routine is triggered. Uninstalled: ADC's calibration routine is not triggered(default).
J19	Selects the source for SPI signals	Installed: SPI signals from FMC connector are controlling the devices on the EVM. Uninstalled: SPI signal from the onboard FTDI IC is controlling the devices on the EVMs(default)
J23	ADC PLL enable control. When hardware pin control option is enabled. The ADC PLL can be enabled by setting this pin to high	Installed: ADC PLL is enabled. Uninstalled: ADC PLL is disabled(default)
J25	FPGA GBTCLK source selection option	Installed: GBTCLK is supplied by ADC's TRIGOUT signal. Uninstalled: GBTCLK is provided by the LMK04828(default).
J26	Select between single ended reference clock or differential reference clock or ADC PLL.	Installed: Single ended reference selected. Uninstalled: Differential reference clock is selected(default).

Table E-2. LEDs

Label	Function
D1	High temp indicator
D2	High input power on channel A
D3	High input power on channel B
D8	High input power on channel C
D10	High input power on channel D
D12	12V power is connected to the EVM
D13	USB is connected to EVM

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