Application Note

TDP1204 Configuration Guide

David Liu

ABSTRACT

The TDP1204 is a HDMI 2.1 redriver supporting datarates up to 12Gbps. It is backwards compatible to HDMI 1.4b and HDMI 2.0b. The high-speed differential inputs and outputs can be either AC-coupled or DC-coupled, which qualifies the TDP1204 to be used as a DP++ to HDMI level shifter, HDMI redriver, or a DisplayPort™ redriver. The TDP1204 can support both 3 and 4 lane HDMI2.1 FRL at 3, 6, 8, 10, and 12Gbps and DisplayPort up to 13.5Gbps (UHBR13.5).

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Trademarks

1 Introduction

This guidelines serves as a starting point for configuring the TDP1204 device for your application.

2 General Configuration Pin

EN: When low, TDP1204 is held in reset. The EN pin has a internal 250k pull-up to VIO. For passive circuitry implementation, it is recommended to add an external 0.22 µF pulldown capacitor on the EN pin.

VIO: The TDP1204 supports 1.2-V, 1.8-V, and 3.3-V LVCMOS levels depending on the source I/O voltage requirement. The VIO pin is used to select which voltage level is used for the following 2-level control pins: LV_DDC_SDA, LV_DDC_SCL, SCL/CFG0, and SDA/CFG1.

Table.title

VIO Pin	LVCMOS Signaling Level
VIO < 1.5 V	1.2 V
1.5 V < VIO < 2.5 V	1.8 V
VIO > 2.5 V	3.3 V

Mode (pin-strap or I2C mode): The MODE pin provides four modes of operation: three pin-strap modes and one I2C mode.

In pin-strap mode, if using the LV_DDC_SDA and LV_DDC_SCL for DDC snooping, the internal DDC buffer must be disabled. But, if using the HV_DDC_SDA and HV_DDC_SCL for DDC snooping, the internal DDC buffer must be enabled.

In I2C mode, DDC snoop feature is enabled by default but can be disabled by a register.

Table.title

Mode	Description
0	Pin-strap mode with internal DDC buffer enabled and fixed receiver equalizer
R	Pin-strap mode with internal DDC buffer disabled and adaptive receiver equalizer
F	I2C mode
1	Pin-strap mode with internal DDC buffer enabled and adaptive receiver equalizer

SCL/CFG0: In pin-strap mode, this is the CFG0 pin. It is recommended to tie this pin to '0' for normal HDMI mode. In I2C mode, this is the SCL pin.

SDA/CFG1: In pin-strap mode, this is the CFG1 pin. The CFG1 pin needs to be set to '0' for normal lane ordering, but set to '1' if the input/output lane order is swapped. In I2C mode, this is the SDA pin.

LINEAR_EN pin: The TDP1204 supports both linear and limited redriver. In pin-strap mode, the LINEAR_EN sets the TDP1204 into either linear or limited redriver mode. It provides the option to dynamically switch between limited and linear based on the HDMI mode of operation. It is recommended to set the LINEAR_EN pin = "1".

Note

When LINEAR_EN is set to "1", the HDMI1.4 and 2.0 is operating in limited mode while HDMI2.1 is operating in linear mode. For HDMI2.1 in linear mode, the GPU transmitter must meet the following requirement.

GPU TX Transmitter	Min	Max	Units
Single-ended SWING	400	500	mV
Rise/Fall time for 3, 6, 8, 10, 12Gbps FRL		16	mV/ps

HPDOUT_SEL: The HPDOUT_SEL selects whether the HPD_OUT pin is push/pull or open-drain. HPDOUT_SEL needs to be set to "0" for push/pull and set to "1" for open-drain.

3 Transmitter Configuration

AC_EN: In pin-strap mode, the AC pin selects between AC-coupled or DC-coupled transmitter

Table.title

AC_EN	Description
0	DC-coupled
1	AC-coupled

TXPRE: The TDP1204 provides pre-emphasis/de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP1204 outputs and a TMDS receiver. Pre-emphasis/de-emphasis is not implemented on the clock lane unless the TDP1204 is in HDMI 2.1 FRL mode and at which time the clock lane becomes a data lane. There are two methods to implement pre-emphasis, pin strapping or through I2C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

When using pin-strap mode, the TXPRE pin controls four different global pre-emphasis/de-emphasis values for all data lanes when TDP1204 is operating in HDMI 1.4 or HDMI 2.0. In HDMI 2.1 FRL mode, the TXPRE pin has no effect and the de-emphasis value used is based on the DDC TXFFE snooped value.

Table.title

TXPRE	HDMI1.4 Or 2.0	HDMI2.1 TXFFE Level
0	3.5 dB pre-emphasis	Refer to TXFFE Level
R	–2.5 dB de-emphasis	Refer to TXFFE Level
F	0 dB	Refer to TXFFE Level
1	6 dB pre-emphasis	Refer to TXFFE Level

FRL TX FFE Level	De-emphasis (dB)
TXFFE0	-2.5
TXFFE1	-3.5
TXFFE2	-3.7
TXFFE3	-4.6

TXSWG: The TDP1204 transmitter swing level can be adjusted in both pin-strap and I2C mode.

In I2C mode, TX swing settings are controlled independently for each lane (both clock and data) through registers. In pin strap mode with limited mode enabled, the TXSWG pin adjust the default 1000 mV swing. These settings apply only to the data lanes. The clock lane remains at default value. In pin-strap mode with linear enabled, the linearity range is fixed at the highest level (1200mVpp) so TXSWG pin is not used.

Table.title

TXSWG	Limited Mode	Linear Mode
0	Default + 10%	1200 mVpp
R	Default-5%	1200 mVpp
F	Default (1000 mVpp)	1200 mVpp
1	Default + 15%	1200 mVpp

4 Receiver Configuration

CTLEMAP_SEL: The TDP1204 in pin-strap mode has three CTLE HDMI Datarate Maps: Map A, Map B, and Map C. Map A and C should be used if TDP1204 is used in a source application and Map B for a sink application.

	CTLEMAP_SEL PIN Setting			
	"0"	"R'	"F"	"1"
CTLE Data Rate Map	A	C	A	B

Receiver equalization: The receiver equalizer is used to clean up inter-symbol interference (ISI) jitter. TDP1204 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins in pin-strap mode or through I2C register. TDP1204 also supports adaptive equalization (AEQ) for HDMI2.1 FRL as determined by the MODE pin configuration. The adaptive equalization starts when FRL link training begins. It will also re-adapt each time the datarate changes. The adaption will only occur during the TXFFE0 portion of FRL link training when LTP5, LTP6, LTP7, or LTP8 is being received.

References

- Texas Instruments: *12-Gbps AC-Coupled to TMDS and FRL Level Shifter Redriver Data Sheet* (SLLSFI6)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265